# COMPARATIVE ASSESSMENTS OF CONTINUOUS AND SELF-DRIVEN PWM FOR HIGH FREQUENCY CONVERTER DESIGN

By

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DISSERTATION REPORT

Submitted to the Electrical & Electronics Engineering Programme in Partial
Fulfillment of the Requirements for the Degree
Bachelor of Engineering (Hons)
(Electrical & Electronics Engineering)

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## CERTIFICATION OF APPROVAL

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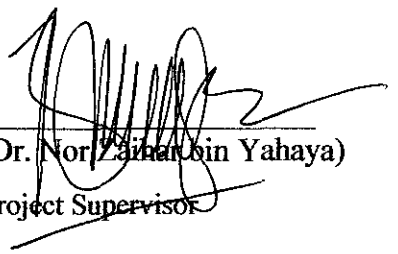

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TRONOH, PERAK

May 2011

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

Siti Munirah Binti Khalid

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# ABSTRACT

In this project the comparison of the continuous gate drivers and self driven gate drivers' characteristics, performance, operation modes, advantages, and disadvantages are analyzed and observed. Both of the gate drivers will be applied at synchronous buck converter, SBC as the output circuit and also with switching frequency of 1 MHz. PSPICE software is used in designing and simulating the respective circuit. The comparison is carried out based on the output voltage, current, node voltage, output ripple voltage and current, gate-to-source voltage, and body diode conduction loss of the continuous and self-driven gate drivers. Type III compensator and AGD are applied to both switches in the SBC circuit. At the end of the simulation, adding AGD to the SBC reduces the dead time, body diode conduction and also cross-conduction losses in DCM. SBC shows an improvement up to 9.70 % and 9.78 % on output voltage, current and also has virtually zero on the body diode conduction losses when both compensator and AGD are applied. For CCM and DCM, it is observed that SBC with CGD, AGD and compensator-AGD produce high output current in CCM compared to DCM. CGD with SBC, the output current in CCM improves 12.22 % compared to DCM. Besides, AGD with SBC is the least preferable circuit compared to compensator-AGD, MPPT-$V_{pulse}$, parallelism, and CGD because of the lower output voltage and current produced, higher output ripple for voltage and current, and higher body diode conduction loss in the SBC. Here the output voltage and current is reduced to 15.30 % and 15.21 % respectively as it is compared to MPPT-$V_{pulse}$.

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# LIST OF ABBREVIATIONS

| | |
|---|---|
| AGD | Adaptive Gate Drive |
| CCM | Continuous Conduction Mode |
| CGD | Conventional Gate Driver |
| $D$ | Duty cycle |
| DBW | Desired Bandwidth |
| DC | Direct Current |
| DCM | Discontinuous Conduction Mode |
| DCR | DC resistance of the output inductor |
| ESR | Equivalent Series Resistance of the output capacitor |
| $FESR$ | Zero frequency |
| $FLC$ | Double pole frequency |
| FPGA | Field Programmable Gate Array |
| MOSFET | Metal Oxide silicon field effect transistor |
| MPPT | Maximum Power Point Tracker |
| PWM | Pulse Width Modulation |
| RGD | Resonant Gate Driver |
| SBC | Synchronous Buck Converter |
| TTL | Transistor-transistor logic |
| $f_s$ | Switching frequency |

| | |
|---|---|
| $I_{L1}$ | Inductor current |
| $P_{BD}$ | Body diode conduction losses |
| $t_{bd}$ | Body diode conduction time |
| $t_D$ | Dead time |
| $T_f$ | Fall time |
| $T_r$ | Rise time |
| $V_{L1}$ | Inductor voltage |
| $V_{ds}$ | Drain to source voltage |
| $V_{gs}$ | Gate to source voltage |
| $V_{pulse}$ | Pulse voltage source |
| $V_{th}$ | Threshold voltage |

# CHAPTER 1
# INTRODUCTION

## 1.1 Background of Study

There are two types of the gate drivers to be studied and evaluated. They are the continuous and self-driven gate drivers. Both of them will be observed for their advantages and disadvantages based on the application of converter circuit. The comparisons of both gate drivers will be within scope of high frequency and high power switch converter, power MOSFET, soft switching techniques, analogue study and power electronics study.

In this project, the significant differences between both of the drivers have become a guideline in proposing new solution to solve the gate drivers' issues, and at the same time can help the electrical and electronics company improve their product's quality and reduce cost in purchasing the suitable component.

The operation and characteristic for both drivers will be observed and analyzed effectively via the output results. Synchronous Buck Converter (SBC) which is widely used in industry for lower power conversion. Here the switches in SBC are connected to compensator and adaptive control circuit. This is to observe the switches performance when the circuit is self driven. Thus throughout the project, knowledge in those related topics will be applied.

## 1.2 Research Rationale

In this work the resultant output of the SBC is observed based on the implementation of both gate drivers. SBC with the continuous gate driver acts as the initial condition for all aspects such as the output voltage and current, body diode conduction losses, and dead time between operating switches. This is because, all effects like switching characteristics, node voltage and resultant outputs of the SBC with continuous gate driver will be noted and compared when it is upgraded to be the self driven circuit as the self driven gate driver is applied to it. Besides, by doing this project also can shows self driven gate driver or the continuous gate driver can give better performance for high frequency converter design.

## 1.3 Objectives

The objectives of this project are:

1) To understand the concept and theory of the gate drivers.
2) To study the differences between the continuous and self-driven gate drivers.
3) To apply the compensator and adaptive control technique to the gate drivers.
4) To be able to analyze the advantages, disadvantages, issues, switching and other losses such as the body diode conduction loss on the converter application with respect to continuous and self-driven gate drivers.

## 1.4 Scope of Study

In this project, the study on the fundamental of the power electronics is applied in order to understand the operation and concept of the gate drivers. The designing, simulating and analyzing on the continuous and self driven gate drivers will be conducted for high power and high frequency DC-DC converter application. Then the understanding on the fundamental study of the control scheme and compensator technique is applied in designing the self driven gate driver. The evaluation on both gate drivers' performance based on the selected design will be studied so that the significant difference of each gate driver can be assessed and compared.

In this work, the evaluations are narrowed down to the output voltage and current, node voltage, output ripple peak-to-peak voltage and current, and the body diode conduction loss. In addition, all circuits' parameters are calculated based on the SBC conduction mode which is in CCM and DCM. For CCM, the values used are $C_1$= 0.625 μF, $L_1$= 15 μH, and R=3.5 Ω, meanwhile in DCM the values are $C_1$ = 9.375 μF, $L_1$ = 1 μH and R = 4 Ω [19]. 1 MHz of switching frequency is used.

## 1.5 Problem statement

As stated in the project background, there are two gate drivers to be evaluated in terms of their differences and effectiveness. However, both of them have issues when they come to the high switching frequency applications. This is because nowadays the power converter's switching frequency is being pushed to MHz range to provide small component size and fast transient response. This contributes to the turn-on and turn-off losses, lower efficiency and excessive power loss of the gate drivers.

Furthermore, many researches claim that the self-driven gate driver is better than the continuous gate driver. But, there are limitations based on specific application. Thus the study of continuous and self-driven gate drivers needs to be investigated thoroughly in order to see the significant differences between them. By analyzing the issues, this can also lead to proper solutions which contribute to the improvement of both gate drivers. They will be designed and the differences between them are noted and analyzed using SBC.

# CHAPTER 2

# LITERATURE REVIEW

## 2.1 Pulse Width Modulation

Pulse width Modulation, PWM techniques are used in digital-to-analog conversion, power conversion and DC-DC voltage conversion. The 'high' and 'low' signals of digital pulses are used to create analogue outputs. The duty ratio, *D* which is known as the percentage of on-time in one complete switching cycle to produce voltage in range of 0 %-10 % of the maximum supplied voltage, is adjusted depending on the PWM resolution. The period of the PWM is the arbitrary time given and this is based on the switching circuit.

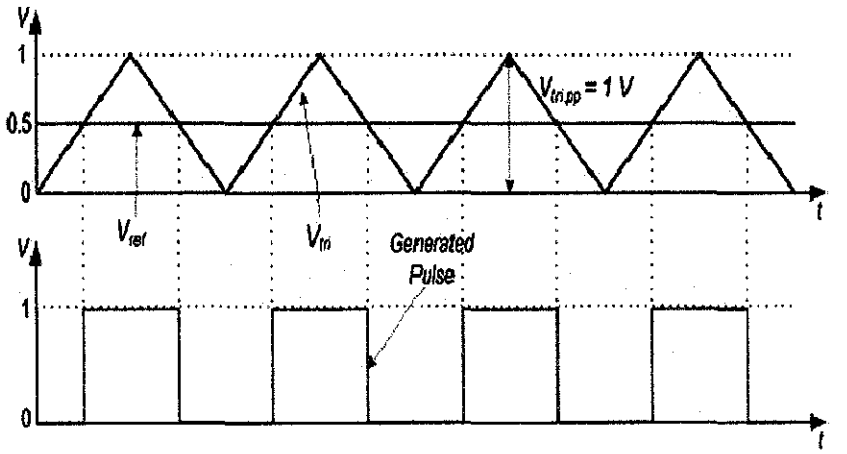



Figure 1: PWM signals [1]

Two types of PWM used nowadays are the digital and analogue PWM. The analogue PWM signals can be generated when comparing the triangular waveform voltage, $V_{tri}$ with the reference voltage $V_{ref}$ using ramp generator and comparator as illustrated in Figure 1.

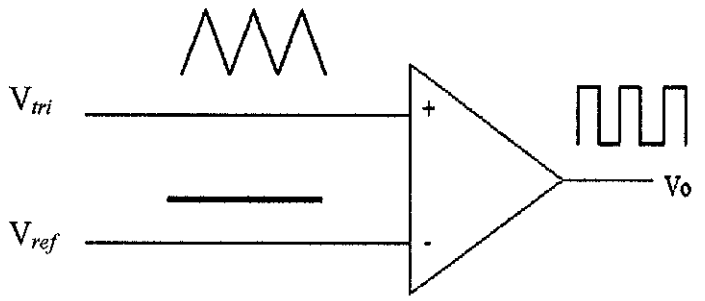



Figure 2: PWM generator

Figure 2 shows the PWM generator where both of the signals that are feeding into the comparator will be compared. The comparator will generate the output voltage, $V_o$ when the $V_{tri}$ goes above the $V_{ref}$. The output voltage depends on the swing voltage applied to the comparator. Meanwhile for the digital PWM, it is generated using the combinational logic circuits such as TTL chips, FPGA or ASIC programming.

In driving MOSFET switch, an accurate design of PWM is needed especially for the gate driver application. This is because, the range of the gate voltage should be above its threshold voltage, $V_{th}$ so that it can turn on with sufficient charge.

However, when it comes to high switching frequency for example in megahertz application, the output of the PWM usually contains high harmonic distortion and noise making the design more complex. Besides that, the use of the

PWM at higher switching frequency normally causes considerable losses due to the switching behaviour on the semiconductor device [1].

## 2.2 Gate Driver Circuit

Gate driver is an interface between control for low power electronics and high power switch and it is used in activation of on and off signals to the switch. This circuit amplifies control signal to a level required to drive the power switch. It also provides electrical isolation between the power switch and logic level [2].

It is also an electronic circuit that applies correct power levels to Metal Oxide Silicon Field effect, (MOSFET) transistor and insulated gate bipolar transistor, (IGBT). With power MOSFETs, the gate driver can be implemented as transformers, discrete transistors or dedicated integrate circuits, IC and it is also integrated within the controller ICs. Most of high frequency applications use silicon based devices such as MOSFETs and IGBT. To drive the power MOSFETs at very high frequencies, partitioning the gate-drive function of controllers that use the pulse width modulation, PWM are needed to improve the controller stability by eliminating the high peak currents and heat dissipation [3].

There are three losses in driving the power MOSFET which are:

a) Conduction loss – It refers to the power loss dissipated by the gate resistor.
b) Cross-conduction – This is caused by the ''shoot-through'' current going through the power MOSFET. "Shoot- through" current is defined as the condition when both MOSFETs are either fully or partially turned on. This results in providing a path for current to "shoot-through" from input voltage to ground.
c) Switching loss – This is a loss of the crossover between the voltage and current of each power MOSFET switch.

Since the PWM period is arbitrary time given based on the switching circuit, the fundamental of the PWM timing can be categorized into two categories which are the self driven and continuous driven. Thus, the gate driver can also be classified into two types: the continuous and self-driven gate driver.

### *2.2.1 Continuous Gate Driver*

Continuous gate driver is a driver where the signal pulses are provided continuously to the switch. It will continuously turn on and supply the voltage to the power MOSFET circuit when it receives the signal. One of the examples of continuous gate driver is the conventional gate driver. This gate driver has been developed since 1970s where all gate drivers have the same circuit configuration of half bridge structure which is also known as the totem-pole driver [1], and they use fixed gate resistance for turn on and turn off sequences.

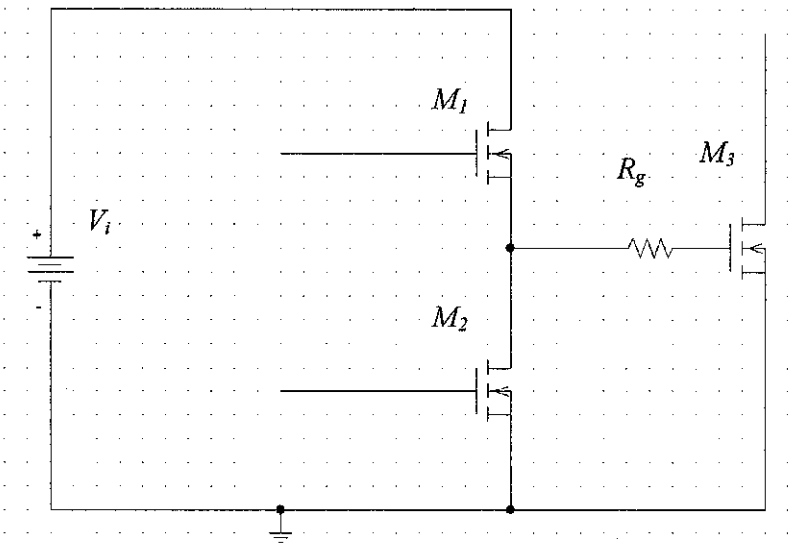



Figure 3: Conventional Gate Driver

Figure 3 shows the conventional gate drive circuit that contains the bipolar totem-pole pair of driving switches, $M_1$, and $M_2$, equivalent driving resistor $R_g$ between the driving switches and the Power MOSFET [1]. This circuit is widely used in present power converters. For fast driving capability in both $M_1$ and $M_2$, they receive the control signal from the PWM controllers. As PWM signals supplied to $M_1$ and $M_2$, the switches will turn on when the gate voltage, $V_G$ for both of them reach or above their $V_{th}$ and this is indicated in the black circle shown in Figure 4. As illustrated in Figure 4 also, $V_{th}$ for $M_1$ and $M_2$ is 4 V (IRFP250).

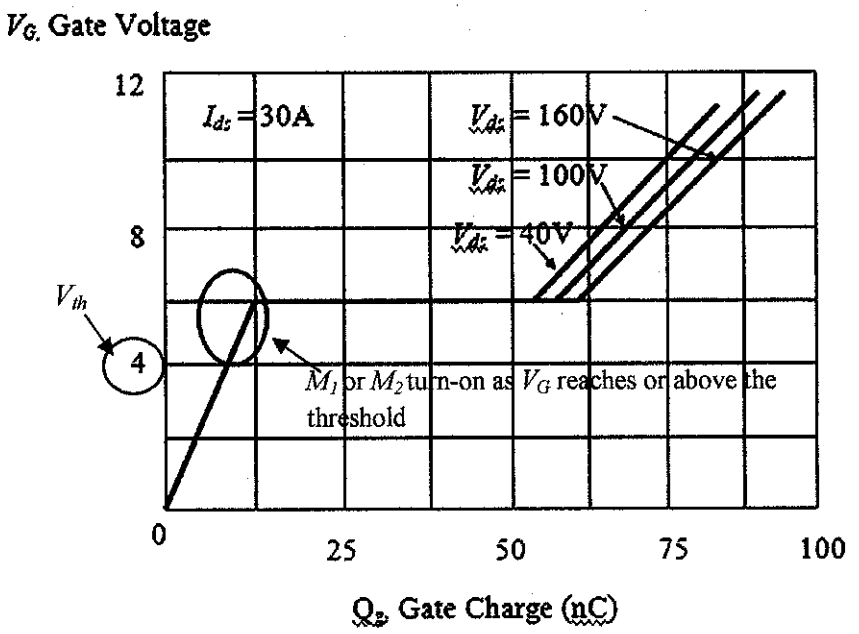



Figure 4: $V_G$ versus $Q_g$

The switches will turn on alternately based on the duty ratio that has been set in the PWM setting. The charging and discharging of the gate capacitance of power MOSFET for this gate driver can cause the gate energy loss. The gate energy is dissipated $M_1$, $M_2$ and the external resistance $R_g$ [5]. This conventional

gate driver will be used to control the turn on and turn off of the Synchronous Buck Converter (SBC) circuit.

*2.2.1.1 Continuous Gate Driver Issues*

The issues here will be based on conventional gate driver, (CGD) since it has similar characteristics and operation as the continuous gate driver. When the switching frequency increases up to 200 kHz, the driving loss causes high power dissipation in the external resistor $R_g$ [1, 5].

Therefore, it is observed that it has limitations in high frequency applications, where it experiences significant gate driving losses especially in high-current applications that require large die size active switches [4]. The gate driving loss is proportional to switching frequency. As a result, this gate driving loss may often offset the advantages gained by the lower conduction losses with a large die size MOSFET.

In addition, the switching speed of this driver is limited since it operates with voltage source RC type. Due to RC charge and discharge, this driver has a longer turn on and off time which is not helpful in reducing the switching loss. The MOSFET gate current is also limited to a value less than the peak driver current during the turn on and off times [5].

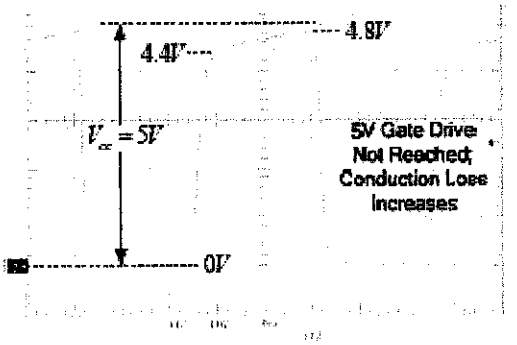



Figure 5: Typical MOSFET gate voltage; UCC37322 driving IRF6618 at 1MHz [5]

Moreover, CGD also has large source impedance where it has several resistors presence in circuit. Due to that, when the MOSFET is turned on, the gate drive voltage is often less than the supply voltage, $V_{cc}$ and it is shown in Figure 5. This leads to greater conduction loss since MOSFET's $R_{DSon}$ will decrease with increasing gate voltage. The typical MOSFET gate voltage waveform does not reach the control voltage of 5V. Moreover very large source impedance leads to slower turn on and hence higher turn on switching loss. [5].

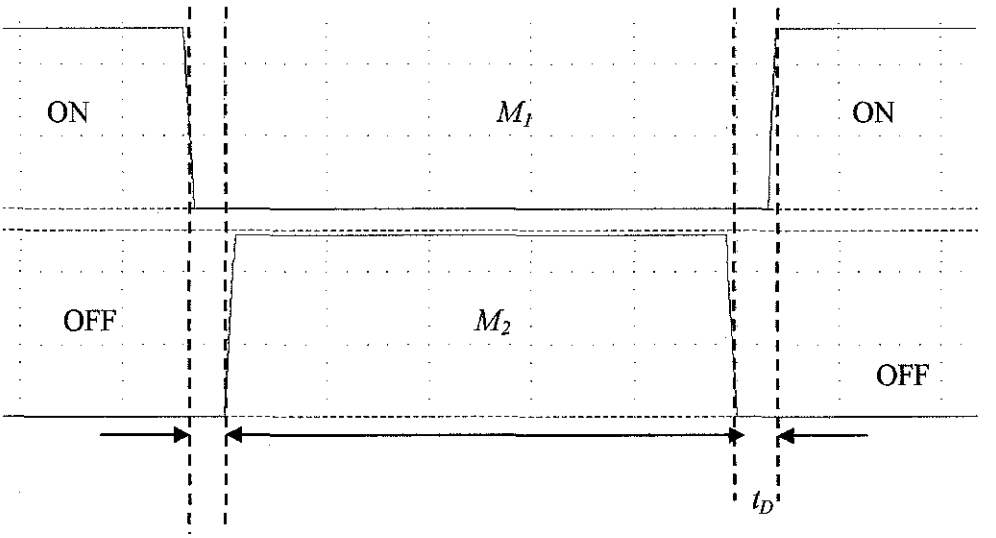



Figure 6: Dead time

CGD also experiences higher gate driving loss comparable to the conduction loss when it is operated at higher frequency and the efficiency also decreases as the losses of the driver increases. Moreover, based on Figure 6, the dead time, $t_D$, known as the duration of neither one of the switches is turned on is one of the important parameters in designing the conventional gate driver. This is because it can contribute to the losses if the $t_D$ of the switches at the CGD is too long. These losses are due to the body diode conduction. Body diode conduction is the situation when $M_1$ and $M_2$ are off, the parasitic body diode of $M_2$ is forward biased and eventually will generate an undershoot of negative voltage.

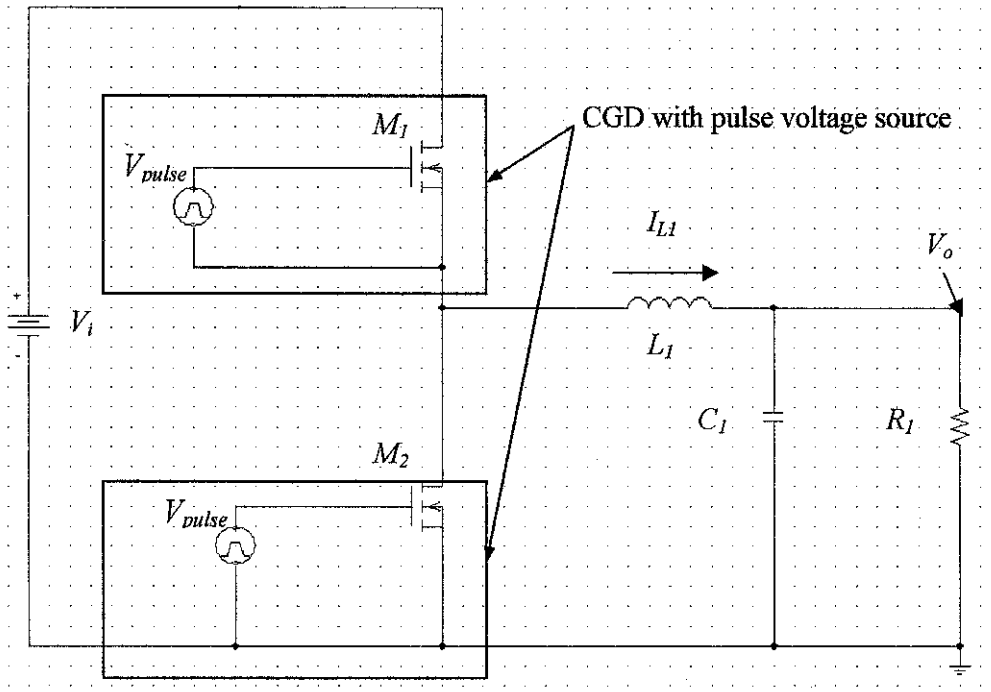



Figure 7: Conventional SBC with conventional gate driver

The issue in losses can also be observed in the SBC application by referring to Figure 7 where the turn-on and turn-off of the circuit are controlled by the CGD using the pulse voltage source $V_{pulse}$. The longer the $t_D$, the longer the body diode conduction will be. This allows the inductor current $I_{L1}$ to flow through the body diode of $M_2$, and hence reduces the overall efficiency of the SBC circuit since it contributes to the losses.

### *2.2.2 Self-driven Gate Driver*

Self-driven gate driver receives its signal and power internally from the circuit [6]. Besides, there is also a feedback or other circuit such as the voltage mode control and compensator circuit that can be used to supply the PWM signals to the application circuit instead of using the PWM supply or $V_{pulse}$.

The use of self driven concept in designing the gate driver can reduce the gate losses issues. For example the body diode conduction loss can be reduced where there is no need to set up the $t_D$ between the controls MOSFET of which the conventional external drivers usually do. In addition, this concept also contributes in simplified the driving circuitry and also recycles the partial driving energy. This will result in a low cost and high efficient gate driver [7]. Similar to the CGD, the self driven gate driver will be applied in the SBC as shown in Figure 7 where both of the switches, $M_1$ and $M_2$ will be controlled by compensator and the adaptive circuit respectively.

*2.2.2.1 Self driven Gate Driver issues.*

The issues of the self driven gate driver can be observed based on the implementation of compensator and adaptive gate drive in the SBC. In terms of the driving circuitry, it becomes more complex because there are two main circuits to be added to the SBC. The difficulty in setting up the $t_D$ is also one of the self driven gate driver's issues. $t_D$ needs to be provided accordingly so that both of the MOSFETs current will not experience shoot through which can result in increasing the ringing, reduced efficiency, and higher MOSFET temperature especially in $M_1$ [8].

In addition, when the AGD control circuit is applied to $M_2$, the starting point of the body diode conduction is difficult to detect because of the inaccurate measurement of the zero voltage transition that affects the control loop operations [9]. Since $M_1$ is connected to the compensator, the design of the compensator type is not easy. The most suitable type of compensator needs to be determined for driver.

The output of the gate driver and application circuits might be different from the desired result, so the selection of appropriate compensator circuit needs to based on its characteristics such as the phase margin, crossover frequency, loop

gain and etc, where each of them need to be determined and designed. The compensation gain should not exceed the error amplifier open loop gain because this is the limiting factor of the compensator [10].

## 2.3 Synchronous Buck Converter (SBC)

It is the modified version of basic buck converter where the diode is replaced by $M_2$, as shown in Figure 7. This results in having two switches, where both of them will be operating alternately and synchronously. By having $M_2$ turn on, the efficiency of the converter is improved.

$M_1$, is called the high side or controlled MOSFET and $M_2$, is called the lower side or synchronous MOSFET. The ratio $V_o$ /$V_i$ is controlled by $D$ of $M_1$. The use of $M_2$ in the SBC results in low voltage, high frequency and high current applications. When the diode is replaced by $M_2$, the power losses are reduced. This is shown by the following Eq. (1)

$$P_{M2} = I_{out}^{\ 2} . R_{DS(ON)} . (1 - D) \qquad (1)$$

Where $P_{M2}$ is the power loss at $M_2$, $R_{DS(ON)}$ is the active resistance of $M_2$ and $D$ is the duty cycle. This can be shown that the power loss depends on $R_{DS(ON)}$ and the diode.

Besides, in order to avoid the cross conduction between the two switches of the circuit, it is important to have $M_2$ turn on when $M_1$ is turned off. However the efficiency might be reduced due to $t_D$. Besides, this converter can also experience the shoot-through state where both of the switches turn on simultaneously and result in a short circuit in the input voltage source [11].

*2.3.1 SBC issues*

When diode is replaced with $M_2$, this may decrease the efficiency of the converter at light load where it allows $I_{L1}$ from entering the Discontinuous Conduction Mode, (DCM) and maintaining operation in Continuous Conduction Mode, (CCM). This means that SBC can operate at higher switching frequency but will produce low efficiency at low output power. Then the complexity of the converter is increased as a complementary output switch driver is needed.

SBC also suffers from cross conduction losses where both MOSFETs are either fully or partially turned on. In this condition, it provides a path for the current to shoot through from the input voltage to ground. Thus the cross conduction will lead to the excessive power dissipation in both switches due to the current that short the power supply to the ground through them, and hence it might damage one or both of switches practically [1,9].

Furthermore, SBC requires two passive filter components which are the inductor, capacitor and also a resistor. These components will increase the overall size of the SBC. So this actually increases the cost of the converter. Since SBC uses MOSFETs as the switches, this causes variable switching delays due to the variations in gate charge and threshold voltage from one MOSFET to another.

As mentioned before, SBC also experiences $t_D$ where both switches are turned off. This is due to the standard control circuits which compensate for the variations in gate charge and threshold of the MOSFETs by delaying the turn on drive of the $M_2$, until the gate voltage of the $M_1$ falls below a threshold. Because of the delay, $t_D$ is created and the efficiency of the converter is degraded [12].

## 2.4 Adaptive Gate Drive (AGD)

To improve the efficiency of the power conversion, $t_D$ has to be minimized. However it must not be too small since it can damage both of the switches. Thus an adaptive control scheme is introduced to the power conversion applications. It can produce the shortest of $t_D$ for MOSFET without producing shoot-through. This is because this gate driver holds a dynamic compensation of $t_D$ in order to avoid short circuit and keeping the $t_D$ itself to be minimized. Thus, the body diode losses can be reduced. In addition, it looks at the $V_{gs}$ of the MOSFET where it is driven off to determine when to turn on one of the MOSFET in the SBC. So control loop is used to detect the state of MOSFET before allowing $M_2$ to turn on.

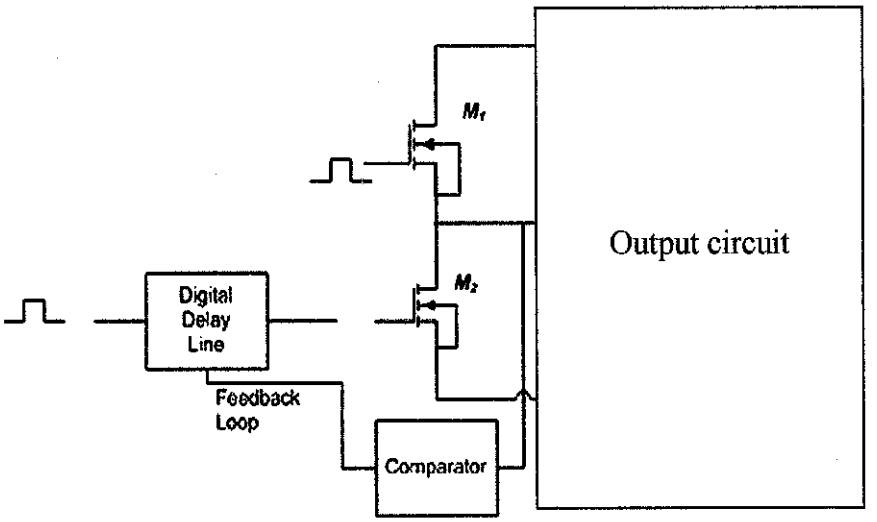



Figure 8: Block Diagram for AGD Control Circuit

Based on Figure 8, the control loop has a digital delay line which detects the phase difference between the state transition of $M_1$ and $M_2$. It also provides a delay that corresponds to magnitude of the phase difference. For the feedback loop, a delay control circuit is adapted to send the delay PWM signal to the switch. Here the comparator is used to detect the drain source voltage of the $M_2$ so

that the digital delay line can adjust the amount of delay applied to turn on the $M_2$. It is turned on only when the switch node voltage is zero without considering the propagation delays [1,13]. Moreover in between $M_2$ turn off and $M_1$ turn on, the $t_D$ needs to be set accordingly so that cross conduction can be avoided during the state transition.

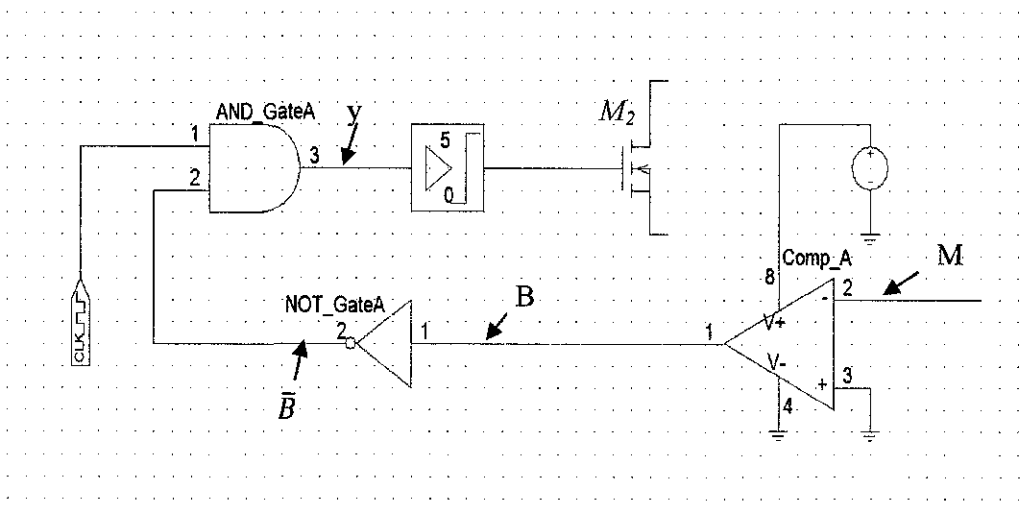



Figure 9: Digital Delay Line for AGD Control Circuit

Meanwhile, Figure 9 shows the digital delay line for AGD control circuit which consists of an inverter, NOT_GateA and AND_Gate A that controls $M_2$. This circuit ensures $M_2$ will only turn on when the node voltage is fully turned off. The output y of the AND_Gate A is derived from the Truth Table and Boolean expression of the digital delay line where $y = M \bullet \overline{B}$

Table 1: Truth Table of the Digital Delay Line

| Input | | | Output |
|---|---|---|---|
| $M$ | $B$ | $\overline{B}$ | $y$ |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |

From Table 1, output 0 shows that the switch is off at zero voltage and 1 indicates that the switch is on representing the maximum voltage. The digital clock will trigger the switch as the input is equal to 1 but again it is noted that switch $M_2$ will not turn on until the switch node voltage is zero [1, 9].

## 2.5 Compensator

Compensator is also one of the techniques, used to control the switch of the gate driver circuit. The input of the compensator is the output voltage of the application circuit. Here, the compensator is applied to $M_1$ switch of the SBC circuit. There are two common types of compensator implemented to the SBC. There are Type II and Type III compensator.

The compensation circuit design is important for system performance of the circuit. For integrated design, the low value of compensation capacitors, $C_{z3}, C_{p1}$ and $C_{z2}$ are chosen in order to stabilize the system with a very limited available space. The advantage of the integration process is the ability to achieve high switching frequency which leads to the opportunity in designing high bandwidth loop compensation. The feedback design should have the following characteristics [14, 15]:

a) DC gain must be large so that the steady-state error between the output and the reference signal is small.
b) For the phase margin, it is preferred to be more than 45°. The recommended values for the SBC system stability is between 45° and 60°.
c) Gain at the switching frequency should be small enough so that the output of the error amplifier has smaller ripple.
d) Error amplifier gain at switching frequency should be designed with appropriate value in order to prevent jitter of the switching waveform.

*2.5.1 Type II Compensator*

Type II Compensator helps shape the profile of the gain with respect to frequency and also gives the 90° boost to the phase. The boost is to counteract the effects of the resonant output filter at the double pole. Figure 10 is the Type II compensator network.

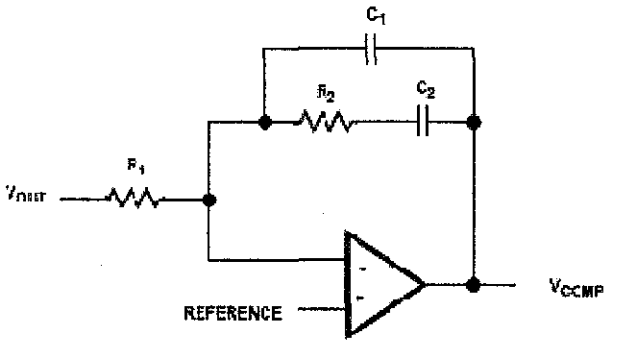



Figure 10: Type II compensator [10, 12]

However, Type II compensator used in converters with output capacitor filter, $C_1$ has a high ESR. It is also usually used in first-order filter such as the current mode converter [12, 28]. This work has low output capacitor ESR and hence it is not practical to apply Type II compensator to the SBC. The most suitable compensator is Type III compensator where it will be discussed in section 2.5.2.

*2.5.2 Type III Compensator*

In this work, the Type III compensator is used for PWM signal generation at $M_1$. This is because usually designers use this type of compensator to compensate the high switching frequency buck and synchronous converters with the output ceramic capacitors. Type III network shapes the profile of the gain with respect to the frequency in order to utilize two zeros so that a phase boost of 180° can be reached. This is to counteract the effects of an under damped resonance of the output filter at the double pole [12, 14]. Figure 11 is the Type III circuit used in this work.

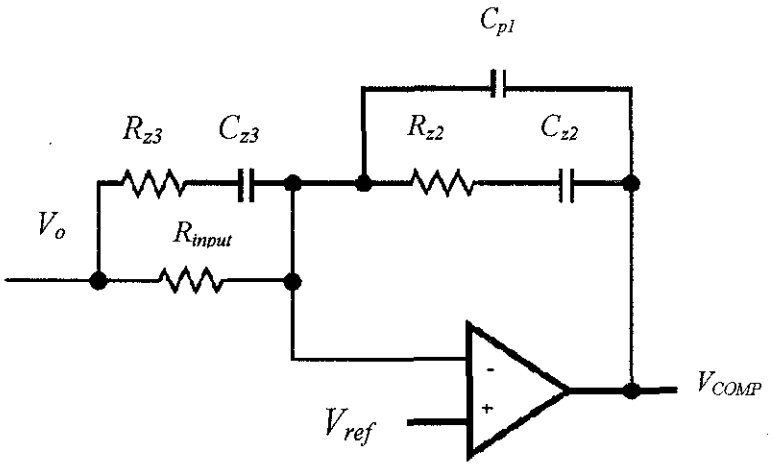



Figure 11: Type III compensator [10, 12]

Based on Figure 11, $V_o$ of the SBC circuit will be fed into the compensator circuit. Then it is compared with the $V_{ref}$ by the comparator. If $V_o$ is more than 3 V or equal to 3 V, the value of the $V_o$ of the SBC is chosen to be the output of the compensator and will be used to turn on $M_1$.

## 2.6 Continuous Conduction Mode (CCM)

CCM means that the current in the energy transfer inductor never goes to zero between switching cycles. The inductor current cannot be instantaneously interrupted. When $M_1$ is turn-on, it will result in a sudden change in the inductor current. Thus $M_2$ must be turned on alternately so the continuity of the current can be maintained. In second-order converters that depend on the arrangement of the switches and $L$, the possible topologies are buck, boost and buck-boost [16].

## 2.7 Discontinuous Conduction Mode (DCM)

In DCM, the inductor current goes to zero during the part of switching cycle. Hence there is a short interval where the inductor current will be zero. This operation is frequently encountered in dc-dc converters because they normally operate under the open load conditions [16]. This mode will result in significant changes in steady-state conversion ratio and the closed-loop dynamic charges. Besides it also affects the voltage gain (M), where M becomes load-dependent, the output impedance is increased and the control output voltage may be lost when load is removed [17].

## 2.8 Body diode Conduction Loss

Body diode conduction occurs during a brief period just before or just after the switching transition, during which the freewheeling MOSFET conducts the current with zero gate voltage [18]. This means that it occurs when $M_1$ and $M_2$ are turned off. The parasitic body diode of $M_1$ or $M_2$ is forward biased due to the continuity of inductor current. As a results an undershoot of approximately -0.7 V is generated at node voltage.

The whole negative duration indicates the duration of body diode conduction. The conduction of the body diode of each MOSFET is detected when the drain current $I_{ds,}$ of the MOSFET has negative value. For example, $M_2$ body diode is turned on by the circulating inductor current that flows into the inductor as soon as $M_1$ is turned off. Same goes to $M_1$ body diode, it will turn on once the $M_2$ is turned off.

Figure 10 shows the effect of the body diode for both of the switches. They can be noted as shown in the black circles.

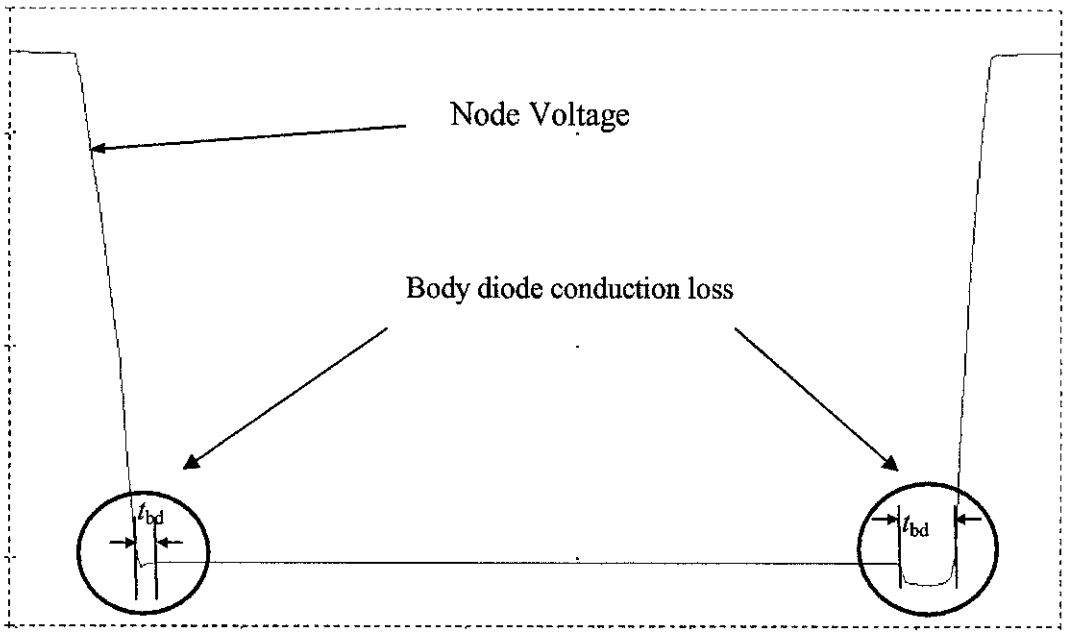



Figure 12: Body diode conduction loss effect

The period of the body diode conduction is related to the dead time of the MOSFET. Normally the body diode conduction period is longer as the dead time of the MOSFET is longer. This is proven as in the Eq. (2) below:

$$P_{BD} = t_{\mathrm{bd}} \times V_f \times I_o \times f_s \qquad (2)$$

where:

$V_f$ = body diode forward voltage drop

$t_{bd}$ = body diode conduction time

The loss is proportional to the body diode conduction time. Thus smaller dead time is required in order to reduce the losses if the SBC operates in high switching frequency. Besides by allowing the inductor current to flow through each body diode of the MOSFET, this can degrade the overall efficiency of SBC since it contributes to the losses.

## 2.9 Summarizing of continuous and self driven gate driver

Based on the research conducted it is noticed that, continuous and self driven gate driver have their own advantages and disadvantages .Table 2 shows the summary of the comparisons for both gate drivers.

Table 2: Summary of Continuous and Self driven gate Driver

| Paper | Continuous gate driver | Paper | Self-driven gate driver |
|---|---|---|---|
| [1],[6] | • It receives its signal from a control circuit such as PWM control circuit.<br>• Gate losses increase when switching frequency increases.<br>• It is considered to be the fastest gate driver and simple in design.<br>• If the $t_D$ of the switches at the gate driver is too long, the body diode conduction losses become higher. | [6] | • It receives its signal and power internally from the circuit.<br>• Gate losses are lower but have possibility to experience shut down when the dead time occur.<br>• Results in fast switching speeds, no timing issues and simple designs.<br>• The circuit can be more complex if the gate driver circuit is upgraded for improvement such as adding the adaptive control scheme to compensate the signal delay time. |
| [4] | • It experiences significant gate driving losses especially in high-current application that require large die size active switches. | [7] | • The driving circuitry is simplified, and partial driving energy can be recycled. This results in low cost and high efficiency solution. |
| [5] | • Switching speed of this driver is limited since it operates with voltage source RC.<br>• During turn on and off time of the MOSFET, the gate current is limited to a value that less than the peak driver current.<br>• It also has large source impedance presence in the circuit that makes the gate drive voltage of the MOSFET less than the supply voltage. | [9] | • If the adaptive control scheme is applied to the gate drivers, the starting point of body diode conduction is difficult to detect. |

Further investigation will be done for both gate drivers on SBC circuit. The output of SBC will then be observed and analyzed so that the differences between them can be notified: output voltage, current, body diode conduction losses, output ripple peak-to-peak voltage and current.

# CHAPTER 3

# METHODOLOGY

## 3.1 Procedure Identification

The overall design methodology throughout this project is shown in Figure 10 below:

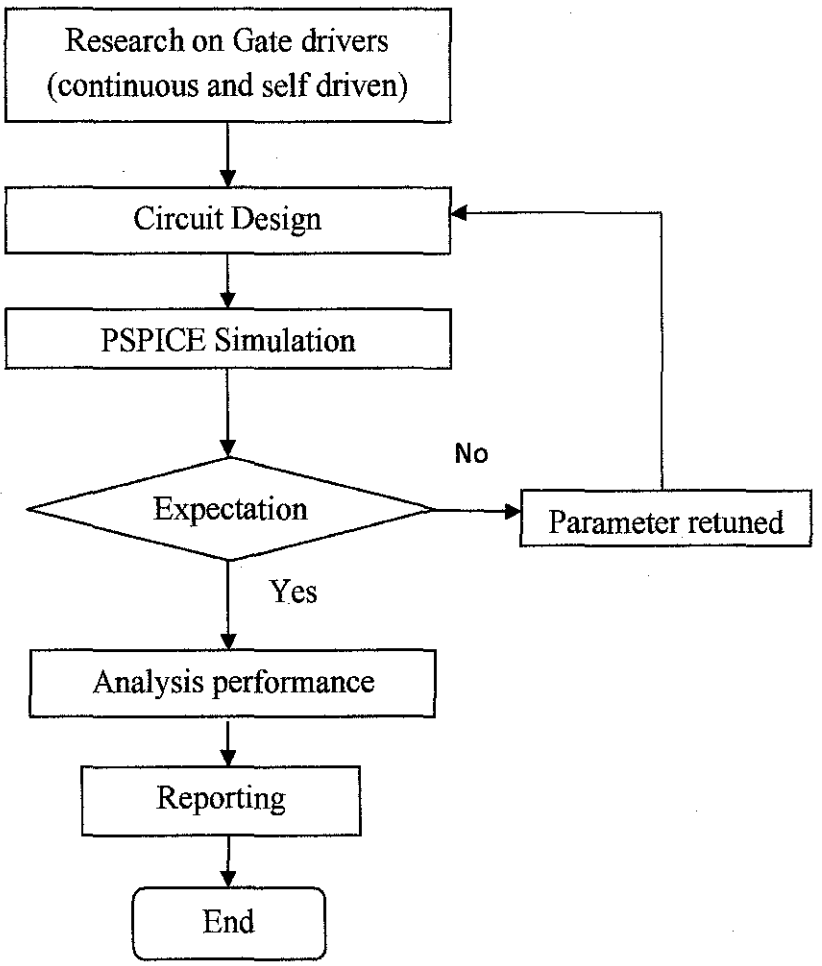



Figure 13: Flowchart of the methodology for this project

### 3.2 Research

Research is conducted with respect to basic operation and concept for both gate drivers. All information such as related waveforms, issues, and associated techniques in designing the gate drivers are gathered from the internet, journals and thesis. The purpose is to understand, investigate the issues and also to obtain the characteristics and differences between both gate drivers. Further research has also been carried out on the improvement and performances of the drivers and this will be based on the SBC circuit.

### 3.3 Circuit design

The project starts with designing and simulating the basic CGD circuit, followed by SBC with CGD, AGD with SBC and the combination of Type III compensator and AGD with the SBC. Thorough analysis on the performance of the SBC is done to obtain the differences in performance between the continuous and self driven.

In this step the continuous and self-driven gate drivers are designed. All related topologies, selection of the suitable components, parameters and calculations will be determined. Here the conventional and self driven gate driver circuits are designed based on the design specifications as follows:

Design specification

a) $D$ : 0.25
b) $V_i$: 12V
c) $V_o$: 3V
d) Switching frequency $f_s$ = 1 MHz

The output circuit for both of them is the SBC circuit. The purpose having SBC circuit as the application circuit is because this circuit is widely used in the

industry and also in many electronics applications such as the voltage regulator in the laptop. This is because, SBC is good in converting the 12 V-24 V typical battery voltage in a laptop down to the few volts needed by the process. When the power is transferred in the "reverse" direction, it acts much like a boost converter. Besides it is also used as the DC-DC converter in stepping down the 12 V car battery to 3 V in order to run the personal CD player. Thus, in this project, there are four circuits that will be designed in this project. There are:

1) Conventional gate driver, CGD.
2) CGD with SBC.
3) Adaptive gate driver, AGD with SBC
4) Compensator-AGD with SBC.

### 3.3.1 *Circuits schematics*

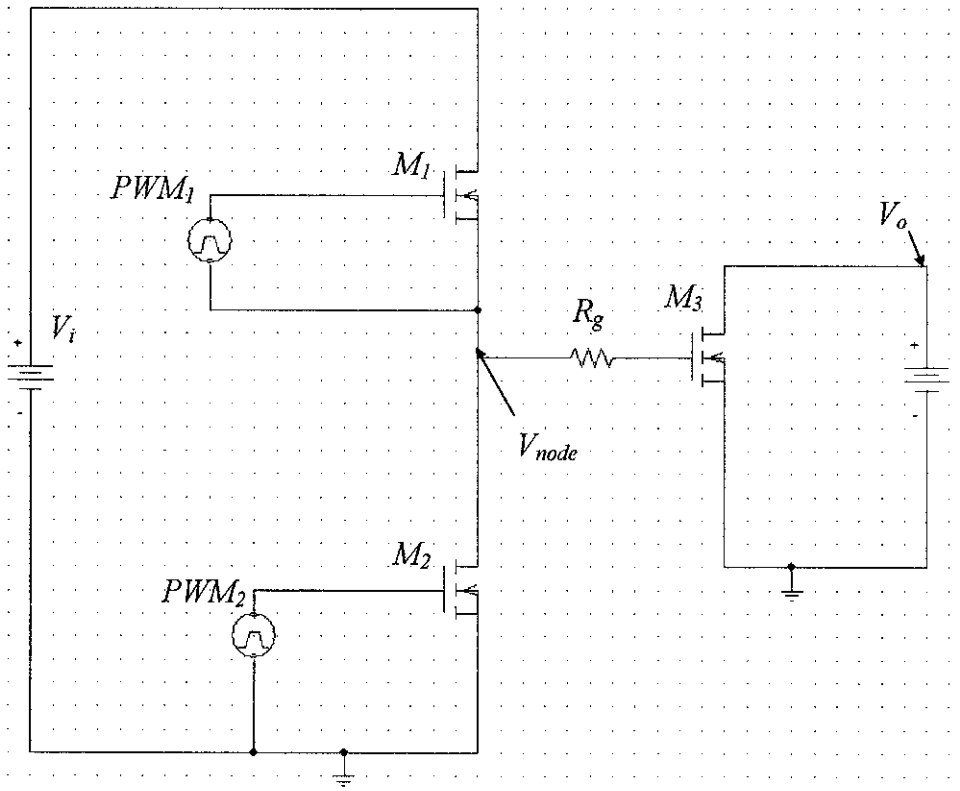



Figure 14: Conventional Gate Driver

Figure 14 shows the CGD schematic circuit designed for driving the Power MOSFET switch. This circuit is used to supply correct PWM signals to $M_3$. The setting of $PWM_1$ and $PWM_2$ are fixed and used also in CGD with SBC, AGD with SBC and also the combination of the compensator and AGD with SBC.

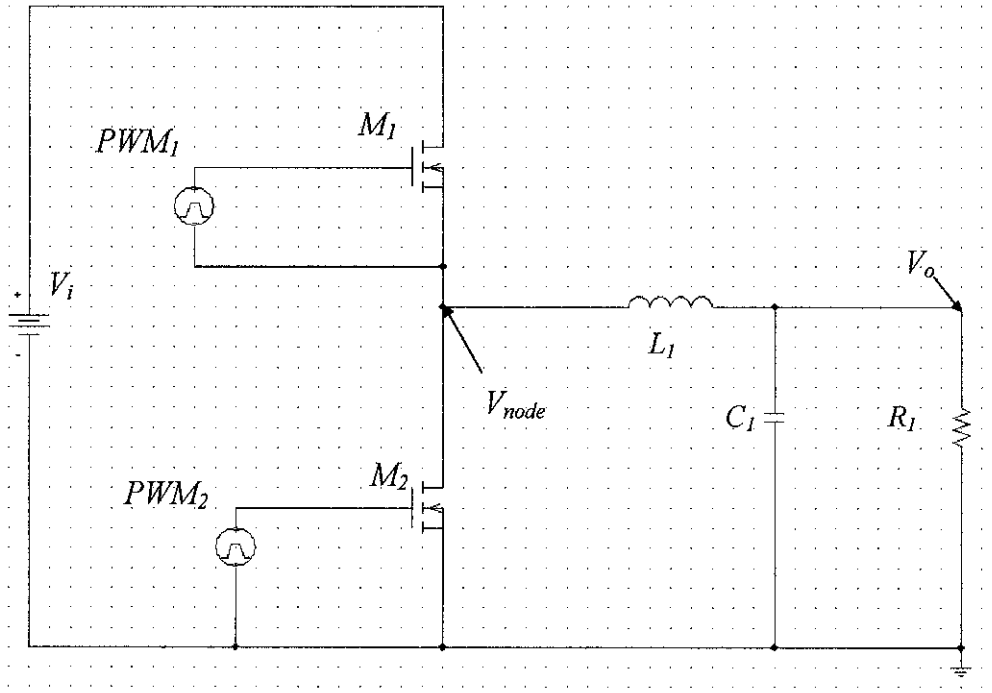



Figure 15: CGD with SBC

Meanwhile for CGD with SBC circuit schematic is shown in Figure 15. The PWM settings for both $M_1$ and $M_2$ are based on the CGD circuit. The value of inductor, capacitor and resistor for this circuit is determined based on the SBC conduction mode. Here all the calculated values for CCM and DCM use the design equations from Eq. (3) to Eq. (7) [11].

Inductor voltage, $V_L = L1\frac{di}{dt} = V_{in} - V_o$ (3)

Output Ripple voltage, $\Delta V_L(t) = \frac{\Delta I_{L1}(t) T_S}{8C_1}$ (4)

Inductor ripple current, $\Delta I_L(t) = 8C_1 f_s . \Delta V_L(t)$ (5)

Output inductor, $L_1 \geq DT_S \frac{V_{in} - V_o}{\Delta I_L(t)}$ (6)

Output capacitor, $C_1 = \frac{\Delta I_L}{8 f_s \Delta V_o}$ (7)

Output filter cut-off frequency, $f_c = \frac{1}{2\pi\sqrt{L_1 C_1}}$ (8)

After that, the circuit is simulated and the node voltage, output voltage, current and also the inductor current are observed. Node voltage is observed to ensure the PWM or switching pulses are generated correctly. For the output voltage and current, they are measured based on their average values. Then the inductor current is determined to check the operation of the SBC whether it is in CCM or DCM.

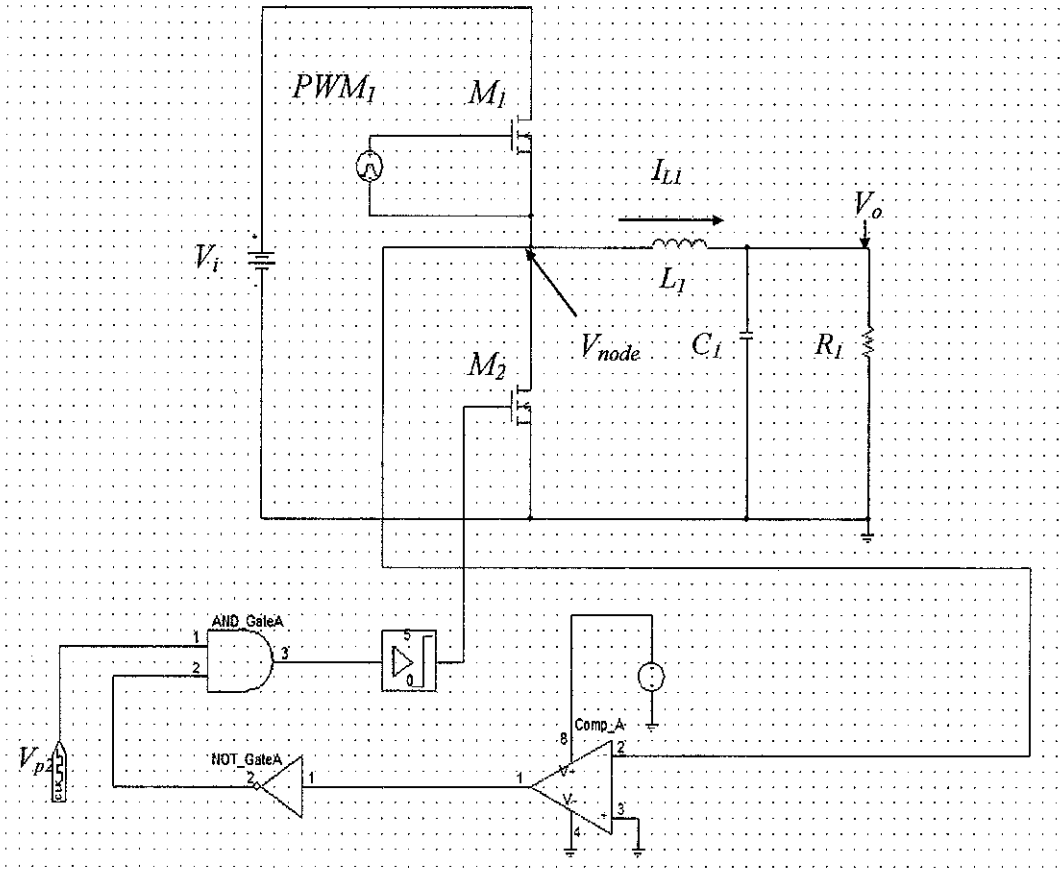



Figure 16: AGD with SBC

Figure 16 shows the SBC circuit with $M_2$ connected to the AGD circuit. In this circuit $M_1$ is turned on by the PWM signals supplied by $PWM_1$ while $M_2$, the PWM signals used to turn it on are controlled by the AGD circuit. Here the $V_{p2}$ is set based on the duty ratio of $M_1$. This is to ensure there will be no cross conduction between the two switches. Similar to circuit in Figure 15, the parameters are determined according to the SBC conduction modes.

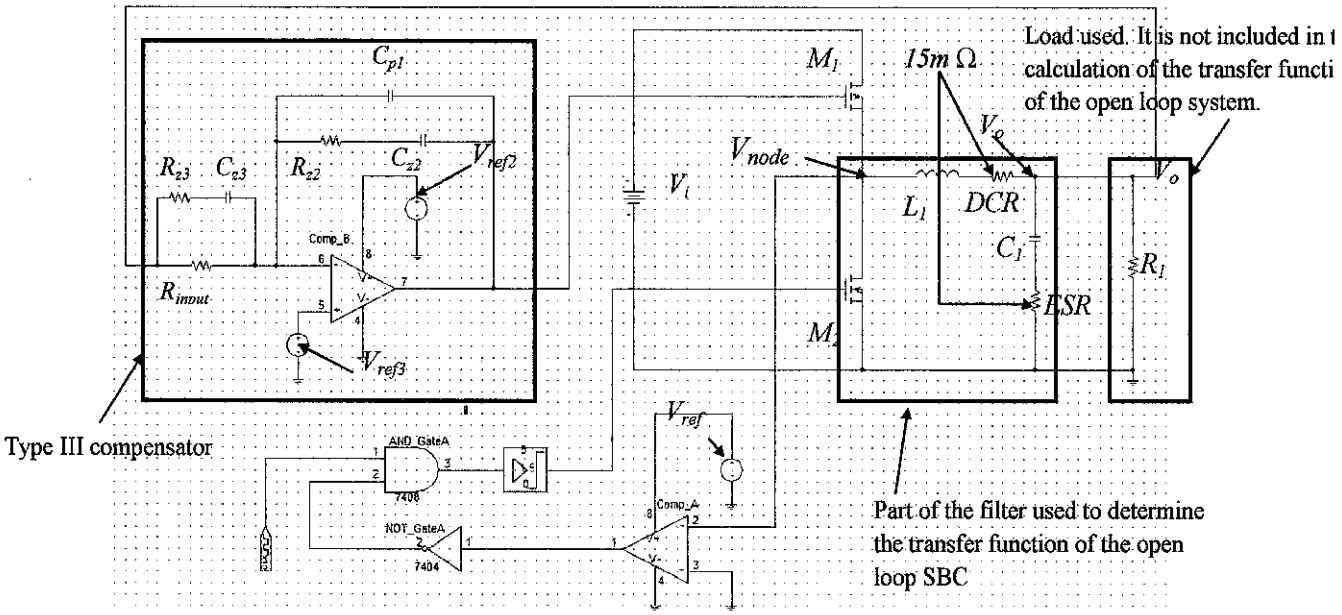



Figure 17: Compensator-AGD with SBC

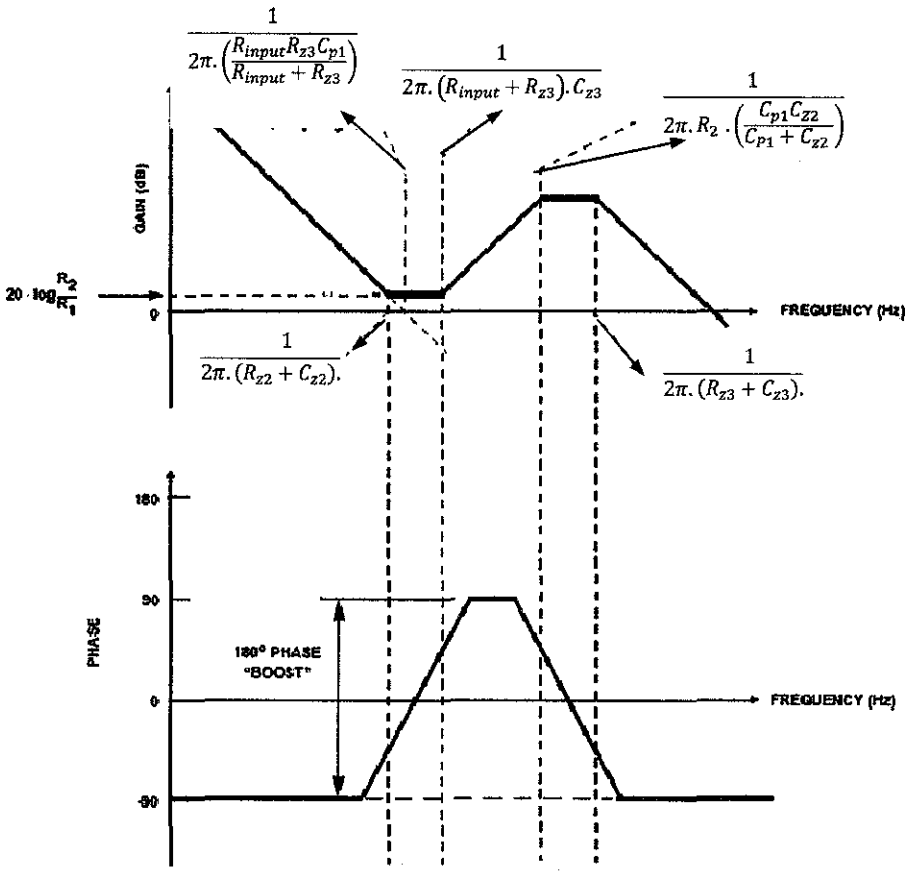



Figure 18: Generic Type III compensation [10,12]

Figure 17 shows the combination of Type III compensator and AGD with SBC. Whereas Figure 18 shows the Generic Type III compensator which shows the placement of the poles and zeros. Then the transfer function of Type III compensator is obtained and it is derived based on circuit in Figure 11 shown in Eq (9):

$$\frac{R_{input}+R_{z3}}{R_{input}.R_{z3}C_{p1}}\left[\frac{\left(s+\frac{1}{R_{z2}C_{z2}}\right)\left(s+\frac{1}{(R_{input}+R_{z3})C_{z3}}\right)}{s\left(s+\frac{C_{p1}+C_{z2}}{R_{z2}C_{p1}C_{z2}}\right)\left(s+\frac{1}{R_{z3}C_{z3}}\right)}\right] \tag{9}$$

According to circuit in Figure 17, there is no modulator implemented to the SBC. So in this case, the gain of the modulator is neglected. Hence the transfer function for open and closed loop of the SBC system will be generated without

the presence of the modulator. This in line with the purpose of designing the circuit in Figure 17 where the SBC is constructed as the self driven circuit. Below are several guidelines that can be followed for positioning the zeros and poles and also in determining the parameters values [10, 13] :

a) Value $R_{input}$ is chosen between 2 kΩ to 5 kΩ. In this project, 3 kΩ is chosen.

b) Next, a gain, ($R_2$/ $R_{input}$) is selected. This is to shift the Open Loop Gain up to give the desired bandwidth. The purpose of it is to allow the 0 dB crossover to occur in the frequency range where Type III network has its second flat gain. Eq.(10) below is used to calculate $R_{z2}$:

$$R_{Z2} = \frac{\text{DBW}}{\text{FLC}} R_{input} \tag{10}$$

DBW is 0.3 from the switching frequency.

c) Then is placing the zero is positioned at 50 % of the output filter double pole frequency. By doing that, parameter $C_{z2}$ can be obtained as in Eq. (11):

$$C_{Z2} = \frac{1}{\pi . R_{z2} . \text{FLC}} \tag{11}$$

d) The first pole is placed at the ESR zero frequency to determine the $C_{p1}$ value. Eq.(12) shows how the value of $C_{p1}$ is determined:

$$C_{p1} = \frac{1}{(2\pi . R_{z2} . C_{Z2} . \text{FESR}) - 1} \tag{12}$$

e) The second pole is at half switching frequency and second zero is set at the output filter double pole. Hence the value of $C_{z3}$ and $R_{z3}$ can be calculated as in Eq.(13) and Eq.(14).

$$R_{z3} = \frac{R_{input}}{\left(\frac{f_{sw}}{2FLC}\right) - 1} \tag{13}$$

$$C_{z3} = \frac{1}{\pi R_{z3} f_{sw}} \tag{14}$$

Then the open loop transfer function of the SBC system is derived. It is based on Figure 17 where KVL rule is used. The transfer function is calculated as follows:

Transfer function of open loop for SBC system: $\frac{V_o}{V_i}$

From Figure 15, $V_o = (ESR + \frac{1}{C_s})$ i(s)

$$V_i = (L_s + DCR + ESR + \frac{1}{C_s})\, i(s)$$

Therefore,

$$\frac{V_o}{V_i} = \frac{ESR + \frac{1}{C_S}}{L_S + DCR + ESR + \frac{1}{C_S}}$$

The equation is simplified and the final transfer function is shown in Eq. (15):

$$\left[\frac{1 + s.ESR.C_1}{1 + s.(ESR + DCR).C_1 + s^2.L_1.C_1}\right] \tag{15}$$

Next step is to obtain the closed loop of the SBC system. The closed loop system is when the SBC system is added with the type III compensator. Thus for the transfer function, it is the resultant of the combination of the compensator and SBC open loop transfer functions and it is given by Eq.(16):

$$\frac{R_{input} + R_{Z3}}{R_{input}.R_{Z3}C_{p1}} \left[\frac{\left(s + \frac{1}{R_{Z2}C_{Z2}}\right)\left(s + \frac{1}{(R_{input} + R_{Z3})C_{Z3}}\right)}{s\left(s + \frac{C_{p1} + C_{Z2}}{R_{Z2}C_{p1}C_{Z2}}\right)\left(s + \frac{1}{R_{Z3}C_{Z3}}\right)}\right] \left[\frac{1 + s.ESR.C_1}{1 + s.(ESR + DCR).C_1 + s^2.L_1.C_1}\right] \tag{16}$$

After obtaining all the transfer functions, the stability of the SBC system is verified using MATLAB (APPENDIX A). In MATLAB, a coding is written and simulated for the bode plots. The bode plots represent the gain and the phase margin for SBC system after and before it is stabilized by the compensator.

### 3.4 PSPICE simulation

The purpose of this simulation is to check whether the circuit designed meet the expectation and produce the desired output. Here all parameters are set in the PSPICE simulation. The graphs obtained will be observed. This is to ensure the correct output from the designed circuit can be determined. If simulation results do not show the expectation graph, the circuit will be re-designed. Table 3 below shows the simulation parameters for CGD, SBC and AGD and combination of compensator and AGD with SBC. The circuits are designed with 20 ns as the print step time and 500000 ns as the final time.

Table 3: Simulation Parameters of CGD, AGD and Compensator with SBC for $f_s$: 1 MHz

| Components | Parameter Settings in PSPICE simulator and Component used. | |
|---|---|---|
| $PWM_1$ | V1=0, V2=5V, $T_d$ = 0ns $T_r$ = 5ns, $T_f$ = 5ns, PW = 240ns, PER= 1000ns | |
| $PWM_2$ | V1=0, V2=5V, $T_d$ = 265ns, $T_r$ = 5ns, $T_f$ = 5ns, PW = 710ns, PER= 1000ns | |
| $V_{p2}$ | Delay = 255ns, On time = 729ns, Off time = 271ns | |
| $M_1$, $M_2$, $M_3$ | IRFP250 | |
| $M_1$ (compensator -AGD) | IRFR9212 | |
| $R_g$ | 10 Ω | |
| *Operation* | CCM | DCM |
| $R_1$ | 3.5 Ω | 4 Ω |
| $V_i$ | 12 V | 12 V |
| $L_1$ | 15 µH | 1 µH |
| $C_1$ | 0.625 µF | 9.375 µF |
| $C_{z3}$ | 915 pF | 915 pF |
| $C_{p1}$ | 0.54 pF | 8.31 pF |
| $C_{z2}$ | 354 pF | 354 pF |
| $R_{z2}$ | 17.3 k Ω | 17.3 k Ω |
| $R_{z3}$ | 348 Ω | 348 Ω |
| *Rinput* | 3 kΩ | 3 kΩ |
| Comp_A, Comp_B | MAX942CPA/MXM | |
| Not_GateA | 7404 | |
| And_GateA | 7408 | |
| $V_{ref}$ | 5 V | |
| $V_{ref2}$ | 4 V | |
| $V_{ref3}$ | 3 V | |

The variation in pulses of $PWM_1$ and $PWM_2$ influence the operating duty ratio $D$. Here $D$ is to determine the length of conduction time of power MOSFET.

MAX942CPA/MXM is used as Comp_A and Comp_B because it is applicable and suitable for circuit with high switching frequency. For compensator and AGD with SBC circuit, P-MOSFET is used as $M_1$.

### 3.5 Analysis performance

In this step, all graphs and data are obtained from the PSPICE simulation and they will be categorized based on continuous and self drive behaviour. The performance analysis is carried out to satisfy the objectives of this project which includes the dead time of the switches, output voltage and current waveform, losses and also the node voltage of the SBC. The comparisons on the characteristics, advantages and disadvantages of each gate drivers are based on this analysis. The analysis performance is also narrowed down to node voltage, output voltage and current, gate to source voltage, body diode conduction loss, and output ripple peak-to-peak voltage and current. By having this analysis, the performance of the SBC can be assessed thoroughly.

In node voltage analysis, the presence of the body diode conduction loss is evaluated. The body diode conduction loss is measured as in Figure 19 where the body diode conduction time, $t_{bd}$ and the undershoot voltage or forward voltage $V_f$ are observed:

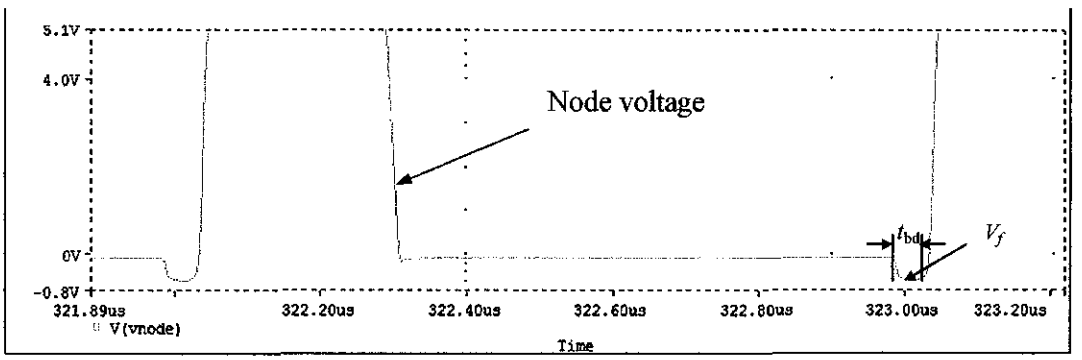



Figure 19: Body diode conduction loss

After obtaining all values, the body diode loss is calculated using Eq. (2). In order to ensure there exists body diode conduction in the SBC, $I_{ds}$ and $V_f$ have to be observed. If $I_{ds}$ is negative and the $V_f$ is more than -0.3 V, this indicates the body diode in the respective MOSFET is conducting. If $I_{ds}$ is positive but the $V_f$ is more than -0.3 V, it still considers having a body diode conduction although there is no current flow in the body diode because the value of $V_f$ is big enough to allow the current to flow in the body diode of the MOSFET. If $V_f$ is less than -0.3 V, but $I_{ds}$ is negative, it also has the potential to allow for body diode conduction in the respective MOSFET due to presence of current flowing in it.

### 3.6 Reporting

This is the last step in the project where all findings will be compiled and written as technical report and hard-bounded thesis.

### 3.7 Tools or Software

In order to obtain the results, the PSPICE software is used. Here the type of PSPCE software used is the MicroSim version 8. It is common software that is widely used by many researches circuit simulation. This software can test various types of the electronics components based on their manufacturer. So it is one of the advantages for the users as they can choose the most suitable components for their electronics circuit. In this project all circuits are designed and simulated using this software. All data such as the output voltage, current, and etc, will be obtained.

### 3.8 Comparative Assessment

In this part, both circuits for AGD and Compensator-AGD with SBC circuit are compared with the combination of CGD [19], parallelism [26], and MPPT-$V_{pulse}$ [27] with SBC. The comparisons are done based on the output voltage, current, output ripple peak-to-peak voltage and current and the body diode conduction loss incurred in the SBC. Each of the data will be compiled in the tables and appropriate graphs are plotted to see the significant differences between them. The differences will be studied and discussed based on the respective chosen parameters.

# CHAPTER 4

# RESULTS AND DISCUSSIONS

## 4.1 Results and Discussion

This project discusses on the comparative assessments between continuous and self-driven PWM high frequency converters. With SBC as the output circuit, the CGD, AGD and Type III compensator are implemented in order to investigate the differences in performance between them. The continuous driven characteristics are observed when CGD is applied to the SBC. Then the circuit is modified by adding the AGD to $M_2$ while Type III compensator to $M_1$. Adding those circuits to SBC will result in generation of PWM signal without using $V_{pulse}$.

Graph on PWM signals, node voltage, inductor voltage, inductor current, output voltage and current are obtained for all the circuits. Those graphs are observed to analyze the performance of the SBC for all circuits. First, correct PWM signals are fed into the switch of the converter application. The voltage at node has to be equal to the input voltage. This indicates the correct PWM signals are used to turn on both of the switches. Meanwhile for the inductor current, it indicates the operation of SBC either in CCM or DCM.

*4.1.1 Conventional Gate Driver,CGD*

The following waveforms are the simulated results for circuit designed in Figure 12.

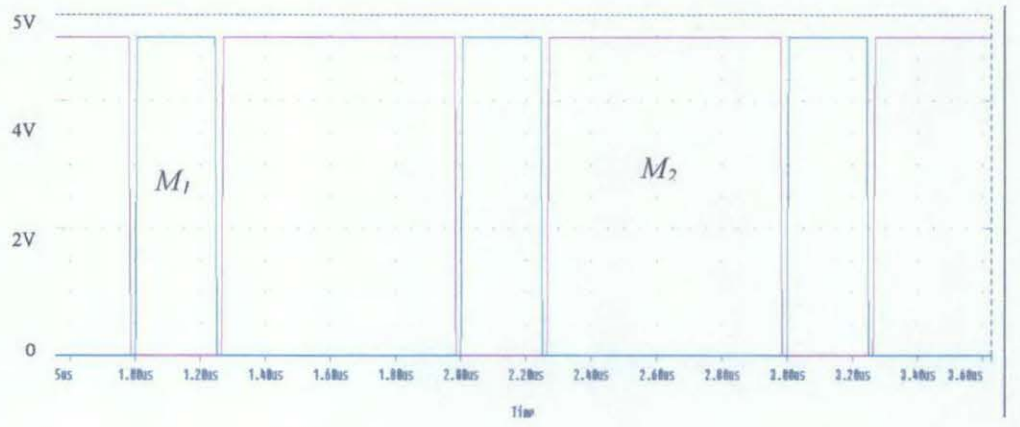



Figure 20: PWM of the CGD

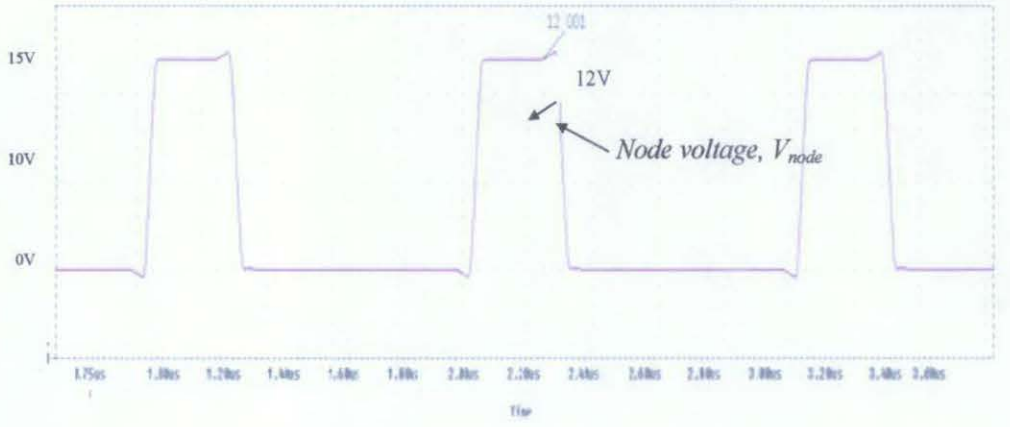



Figure 21: Node voltage of CGD, $V_{node}$

Figure 20 and Figure 21 show the PWM signals and node voltage, $V_{node}$ of CGD circuit. To ensure the PWM signal is generated correctly, $V_{node}$ has to be equal to the input voltage, $V_i$. Thus the value of 12 V from the graph above shows the correct PWM has been generated to turn on both of the switches.

The PWM specifications as in Table 3 are applied to both $M_1$ and $M_2$. They are determined based on the switching frequency, $f_s$ of which is 1 MHz. The purpose of using high switching frequency is to reduce the board size and component of the inductor and capacitor.

From the switching frequency, the total period will be 1000 ns and the time rise, $T_r$, dead time, $t_D$ and time fall, $T_f$ are assumed and equally divided to both switch $M_1$ and $M_2$. This correct PWM signal for CGD is applied to the load circuit, SBC.

*4.1.2 CGD with SBC*

In Figure 15, there are two sets of parameters that have been determined for CCM and DCM. Therefore, each of the conduction modes has its own distinct parameter values [19]. Meanwhile for the PWM pulses, they use the same PWM setting as in the CGD circuit.

At first, ripple voltage is assumed to be 0.01 or 1 % so that, $\Delta V_L = 0.03$. For CCM, output inductor is fixed to $L_1 = 15\ \mu$H [19]. Based on this value, the output capacitor is determined by using Eq. (3) to Eq. (7). As a result, the output capacitor, $C_1$ is $0.625\ \mu$F [19]. These steps are repeated for DCM where the output inductor is set to $L_1 = 1\ \mu$H [19]. Thus the resultant output capacitor is $9.375\ \mu$F[19].

*4.1.2.1 CGD with SBC Simulation Graph*

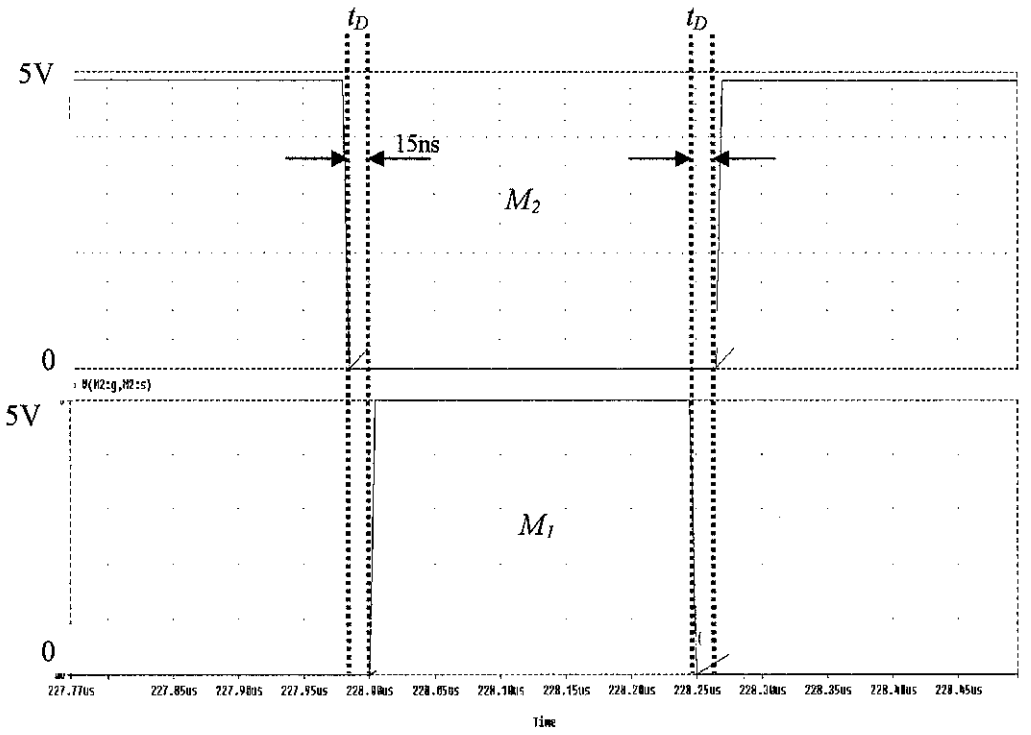



Figure 22: PWM of the SBC with CGD

Figure 22 shows the PWM signal for SBC with CGD. It is noted that $t_D$ of both $M_1$ and $M_2$ are 15 ns. With this $t_D$ the SBC does not experience cross conduction loss when both of the switches are partially or fully on. However with large $t_D$, it can experience some drawbacks which can be observed based on the resultant waveforms. One of the drawbacks seen in this project is the body diode conduction losses. Here, the body diode conduction losses increase with dead time. The body diode conduction losses in the SBC will be explained in detail in section 4.2.2.

*4.1.2.2 CGD with SBC Simulation Graph for CCM*

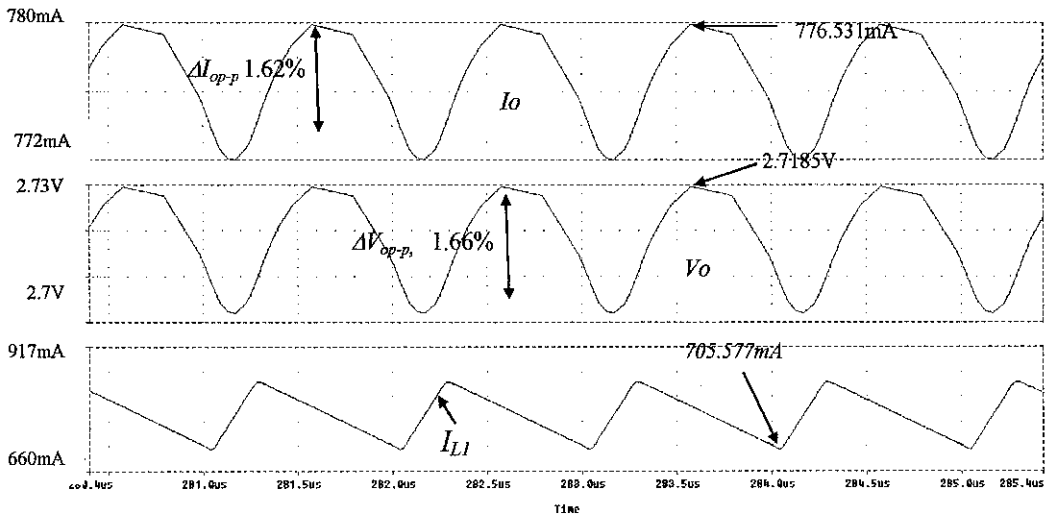



Figure 23: $I_o$, $V_o$, and $I_{L1}$ CGD with SBC_CCM

CCM occurs when current in the energy transfer inductor never goes to zero between the switching cycles. This means that inductor current cannot be instantaneously interrupted. As $M_1$ is conducting, it results in a sudden change in the inductor current. SBC as shown in Figure 23 operates in the CCM where there is no negative value of the inductor current. Here the lower peak of the inductor current shows in Figure 23 is equal to 705.577 mA. This CCM operation implies low output power in SBC. Hence it introduces a drawback if standby efficiency is

a major concern because, once the MOSFET's conduction loss comes into picture, the total power dissipation will be relatively large [20]. Both of the output voltage and current in the Figure 21 have peak to peak ripples of 1.66 % $\left(\frac{2.7185-2.6959}{2.7185} \times 100 \times 2\right)$ and 1.62 % $\left(\frac{776.531m-770.260m}{776.531m} \times 100 \times 2\right)$ respectively.

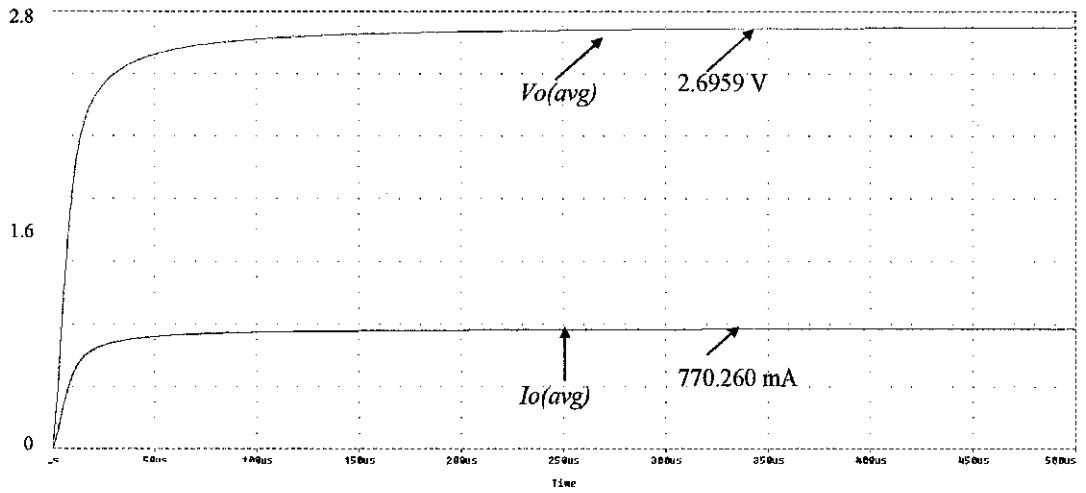



Figure 24: $V_{o(avg)}$ and $I_{o(avg)}$ of the SBC_CCM

The average output voltage, $V_{o(avg)}$ is 2.6959 V, and the average output current $I_{o(avg)}$ is 770.260 mA. Both values are shown in Figure 24. The voltage obtained slightly differs from the theoretical value, 3 V. This is due to the ripples that occur at the resultant output as shown in Figure 23 where both of the output voltage and current's waveforms have high ripples values. Besides, the losses that dissipated in the gate drivers and SBC, such as the body diode conduction losses and switching losses can also affect the resultant output voltage and current. So in order to have an accurate result, it is imperative to ensure that the ripples are small enough and also reduce the possible losses such as the body diode conduction losses.

*4.1.2.3 CGD with SBC Simulation Graph for DCM*

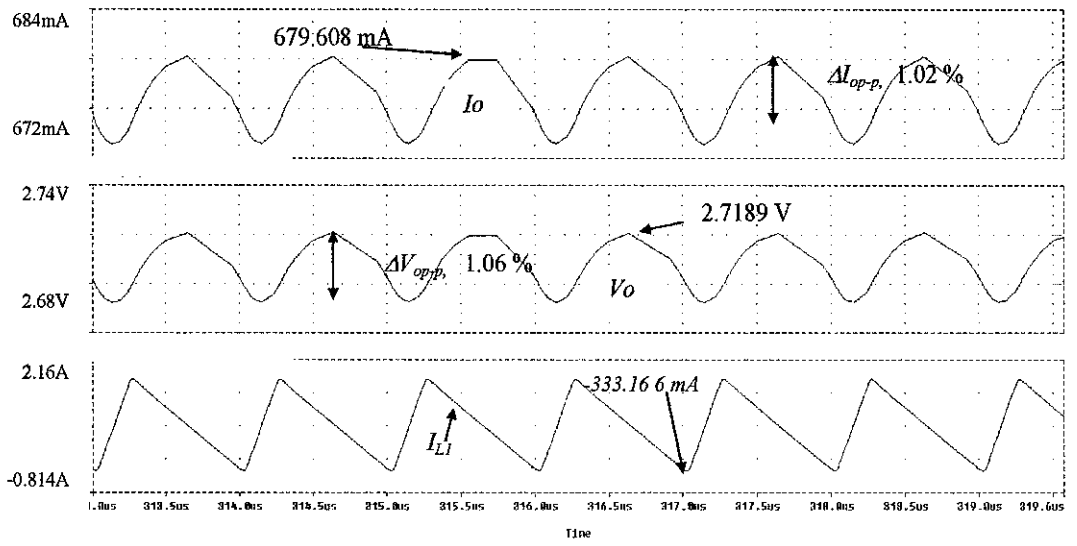



Figure 25: $I_o$, $V_o$, and $I_{L1}$ CGD with SBC_DCM

As for DCM, the inductor current goes to zero during the part of switching cycle. There will be a short interval where the inductor current is zero and this is shown in Figure 25, where there is a negative polarity at lower peak of the inductor current having the value of -333.166 mA. In addition, the output voltage and current have fewer ripples compared to when it is in CCM. Here the output ripples peak-to-peak for both output voltage and current are 1.06 % $\left(\frac{2.7189-2.7045}{2.7189} \times 100 \times 2\right)$ and 1.02 % $\left(\frac{679.608m-676.129m}{679.608m} \times 100 \times 2\right)$ respectively.

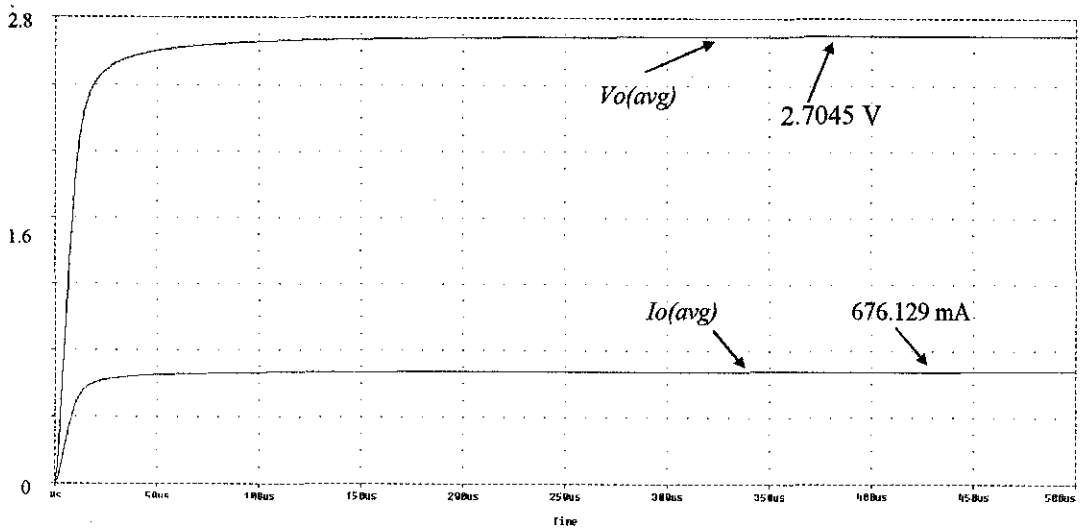



Figure 26: $V_{o(avg)}$ and $I_{o(avg)}$ of the SBC_DCM

Figure 26 shows the average output voltage and current for CGD with SBC circuit. The $V_{o(avg)}$ is observed to be 2.7045 V which is same as when the SBC operates in CCM. However, $I_{o(avg)}$ is found to be much lower than in CCM which has a value of 676.129 mA.

Table 4 : CGD with SBC for CCM and DCM

| | CGD [19] | | |
|---|---|---|---|
| | CCM | DCM | Improvement of CGD_CCM to DCM (%) |
| $V_{o(avg)}$, (V) | 2.70 | 2.70 | 0.00 |
| $I_{oavg}$, (mA) | 770.26 | 676.13 | 12.22 |
| $I_{Lmax\ peak}$ (A) | 0.85 | 1.72 | -50.58 |
| $\Delta V_{op\text{-}p}$ (%) | 1.66 | 1.06 | -36.14 |
| $\Delta I_{op\text{-}p}$ (%) | 1.62 | 1.02 | -37.04 |
| $P_{BD}$ (mW) | 16.87 | 6.29 | 62.71 |

Table 4 shows the comparisons of the output results between CCM and DCM for CGD with SBC circuit. It can be noted that, the output current is

reduced when the SBC operates in DCM condition. However, in DCM condition the body diode conduction loss, $P_{BD}$ is reduced to 62.71 %. This is because by allowing inductor current $i_{Lo}$ to operate in DCM, can help minimize the losses has caused by the switches, where the $M_1$ switch will experience switching loss and a reverse recovery loss in switch $M_2$ body diode [19].

*4.1.3 AGD with SBC*

Next part in this work is to evaluate AGD which is connected to $M_2$ of the SBC circuit as shown in Figure 16. Again, PWM signal for $M_1$ is supplied from pulse voltage source, $V_{pulse}$ having the same setting as mentioned in table 3.

As for the AGD circuit, the delay is set by digital clock stimulus, $V_{p2}$. The setting of $V_{p2}$ has to be based on the $V_{pulse}$ at $M_1$. This is to avoid the cross conduction between the two switches. Having AGD in the circuit helps control the dead time between the two switches and improve the performance of SBC by reducing the body diode conduction loss.

As illustrated in Figure 16, the node voltage is captured and fed into the input of the comparator. $V_{node}$ is then compared with the reference voltage, $V_{ref}$. The digital clock in the circuit is fed into the AND gate so that when it is triggered with output 1, $M_2$ will not turn on until the $V_{node}$ is equal to zero. AGD with SBC circuit is operating in two conduction modes: CCM and DCM. The parameters used are the same for CGD and SBC circuit as previously mentioned in Table 3.

*4.1.3.1 AGD with SBC simulation graphs for PWM*

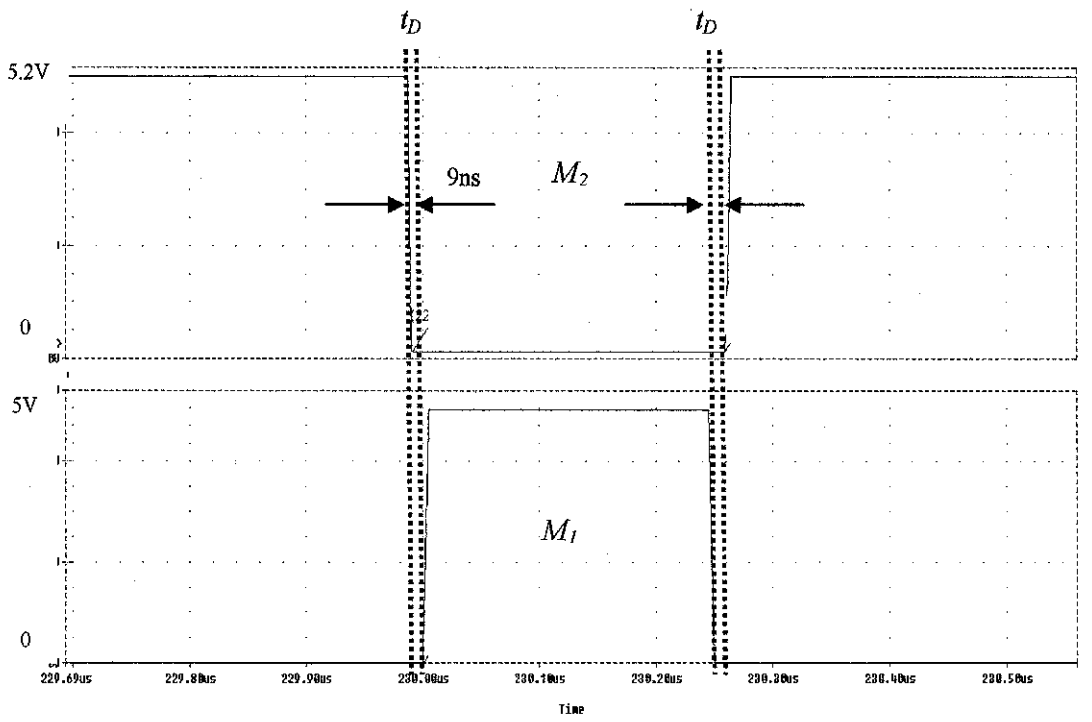



Figure 27: PWM for AGD with SBC

PWM in Figure 27 shows that the $t_D$ between both of the switches are smaller than CGD with SBC. Here $t_D$ is equal to 9 ns. Having smaller $t_D$ results in smaller body diode conduction loss. This is because the body diode conduction period is related to the $t_D$ of the MOSFET and this is proven as in Eq. (2).

Based on Figure 27 also, it is noted that PWM for $M_2$, does not reach 0 V as it is turned off. This shows that $M_2$ does not fully turn off due to some factors such as the effect of the parasitic capacitance where the charging and discharging of it can actually affect the turn on and off of the $V_{gs}$ of $M_2$. Besides the setting of the AGD can control the dead time between $M_1$ and $M_2$. This is one of the reasons why the issue occurs. It is because, an appropriate dead time has to be set accordingly based on the duty ratio of $M_1$ since it has rapid turn on and off conditions which can produce a stress to $M_2$ switching condition.

However in this case, $M_2$ considered off because, it has the value of 134 mV which is smaller than the threshold voltage, $V_{th}$ of $M_2$ which is 4 V. The $V_{th}$ of $M_2$ depends on the type of MOSFET. Since the MOSFET used is from IRFP250 family, the $V_{th}$ value is obtained from IRFP250 datasheet [21].

### *4.1.3.2 AGD with SBC Simulation Graph for CCM*

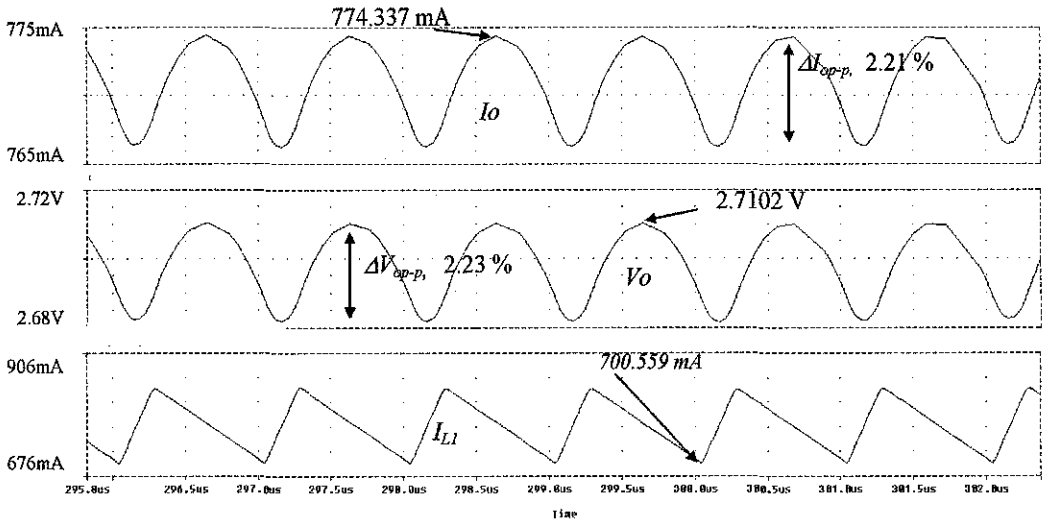



Figure 28: $I_o$, $V_o$, and $I_{L1}$ AGD with SBC_CCM

Figure 28 shows the resultant output voltage, current and inductor current for AGD with SBC in CCM, where it shows the lower peak value of inductor current equal to 700.559 mA. Meanwhile the generated output waveforms have the resultant output ripple peak-to-peak of voltage and current which are given as 2.23 % $\left(\frac{2.7102-2.680}{2.7102} \times 100 \times 2\right)$ and 2.21 % $\left(\frac{774.337m-765.764m}{774.337m} \times 100 \times 2\right)$ respectively.

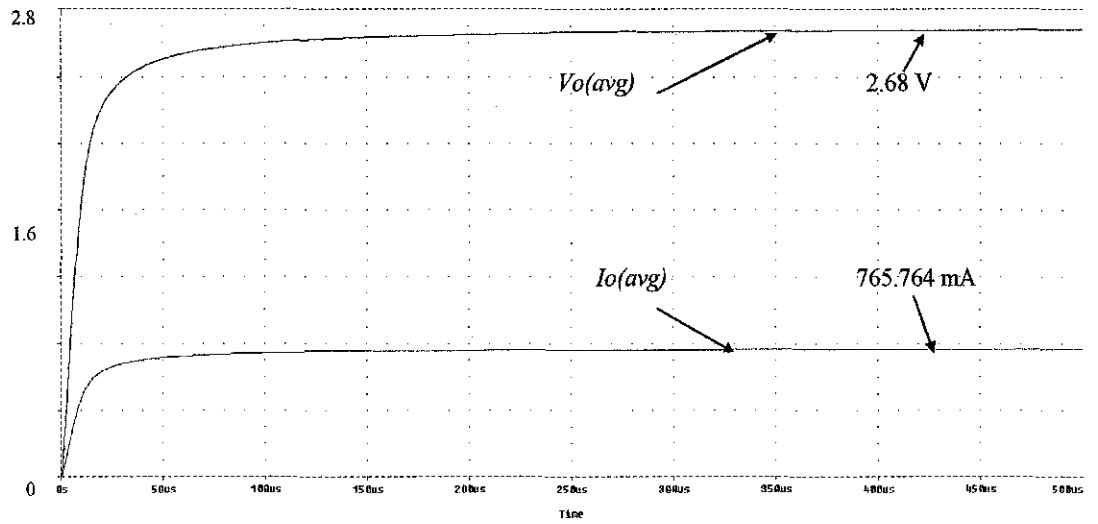



Figure 29: $V_{o(avg)}$ and $I_{o(avg)}$ of the AGD with SBC_CCM

From Figure 29, the average of both output current and voltage are recorded and it is observed that by adding AGD control scheme, the output voltage and current are slightly decreased compared to CGD with SBC. Here the 2.68 V of output voltage and 765.764 mA of output current have been obtained after the circuit is simulated.

### *4.1.3.3 AGD with SBC Simulation Graph for DCM*

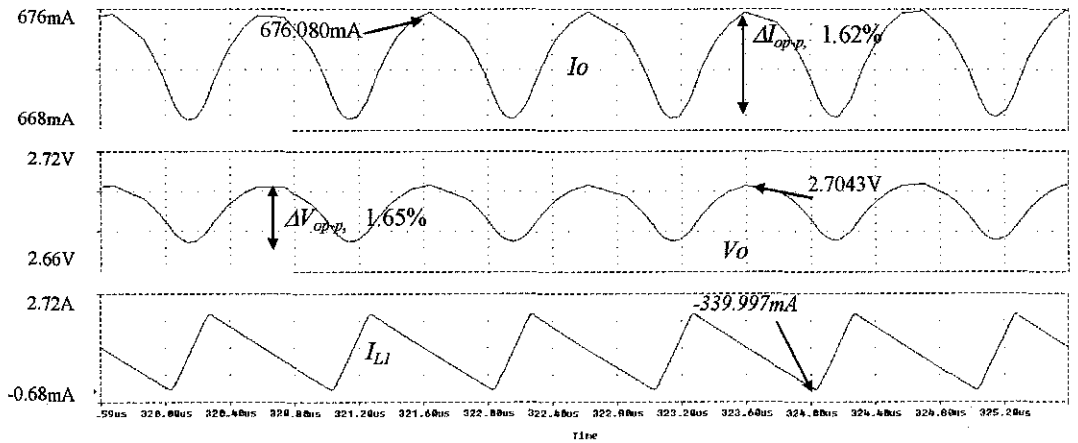



Figure 30: $I_o$, $V_o$, and $I_{L1}$ AGD with SBC_DCM

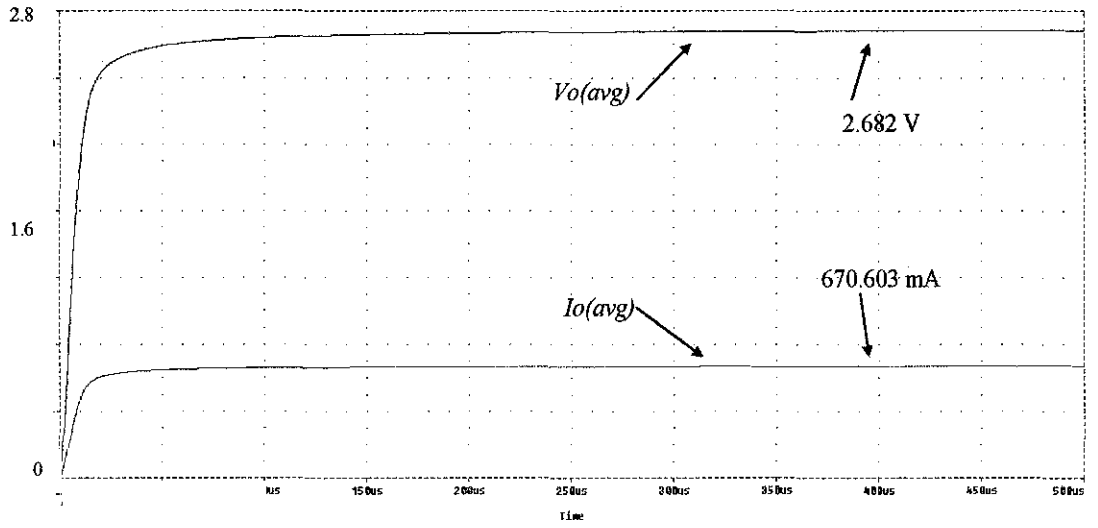



Figure 31: $V_{o(avg)}$ and $I_{o(avg)}$ of the AGD with SBC_DCM

In DCM, it yields same results as CGD with SBC in DCM where, the ripples that present in resultant output voltage and current are much less compare when it is in CCM. They are illustrated in Figure 28. The output ripples here are measured from peak-to-peak, where 1.65 % $\left(\frac{2.7043-2.682}{2.7043} \times 100 \times 2\right)$ is the ripple at the output voltage and 1.62 % $\left(\frac{676.080m-670.603m}{676.080m} \times 100 \times 2\right)$ is the ripple output current. The negative value which is -339.997 mA proves that this SBC operates in DCM. Meanwhile in Figure 31, the average values for both of them are 2.682V and 670.603mA. Based on the average values, it shows that the current decreases when SBC enters the DCM.

Table 5: AGD with SBC for CCM and DCM

| | AGD | | |
|---|---|---|---|
| | CCM | DCM | Improvement of AGD_CCM to DCM(%) |
| $V_{o(avg),}$ (V) | 2.68 | 2.68 | 0.00 |
| $I_{oavg,}$ (mA) | 765.76 | 670.60 | 12.43 |
| $I_{Lmax\ peak}$ (A) | 0.84 | 1.72 | -51.16 |
| $\Delta V_{op\text{-}p}$ (%) | 2.23 | 1.65 | 26.01 |
| $\Delta I_{op\text{-}p}$ (%) | 2.21 | 1.62 | 26.70 |
| $P_{BD}$ (mW) | 20.79 | 4.63 | 77.73 |

Same goes for Table 4 for AGD with SBC in CCM, where it also results in higher output voltage and current when it is in CCM condition and reduction in the $P_{BD}$ up to 77.73 % when operating in DCM condition.

### *4.1.4 Compensator-AGD with SBC*

The Type III compensator and AGD are added to the SBC. Same for other circuits, all parameters for the output circuit are determined based on its conduction mode. In this case, there is no $V_{pulse}$ used to supply the PWM signal to both switches. $M_1$ is controlled by the compensator and for $M_2$, AGD is applied to control the signal.

The purpose of the compensator is to have a close loop of the SBC network where it allows load perturbations or changes in the input voltage that might affect the output. Thus a proper compensator network has to be designed so that the system can allow the predictable bandwidth with unconditionally stability

[10]. In this part, Type III compensator as in Figure 11 is designed to compensate the SBC network.

Therefore an ideal Bode plot with a gain that roll off at a slope of -20 dB/decade, crossing 0 dB at the desired bandwidth and phase margin which greater than $45^{\circ}$ has to be obtained. This type of compensator utilizes two zeroes that give a phase boost of $180^{\circ}$. This will counteract the effect of under damped resonance of the output filter at the double pole. In SBC network, the bandwidth for the compensator designed is taken between 20 %-30 % of the switching frequency [10, 12].

Before the parameters are chosen, transfer functions of SBC, compensator and the combination of both of them have to be determined. The SBC system, the transfer function is given in Eq. (15). As for Type III compensator transfer function, it is obtained after the positioning of zeros and poles locations given as in Eq. (9).

Since only $M_1$ is applied with the compensator network, all bode plots and transfer functions of the SBC system are generated based on the buck converter application. This includes the overall bode plot and transfer function of the SBC with the compensator. Thus the overall of the system's transfer function is shown in Eq. (16).

*A) Bode plot for SBC system*

There are two parts of bode plot for this system. First is when the SBC is conducting in CCM and the other is when it is in DCM. These bode plots will show the stability of the SBC systems before and after adding the compensator.

*i) SBC system (CCM)*

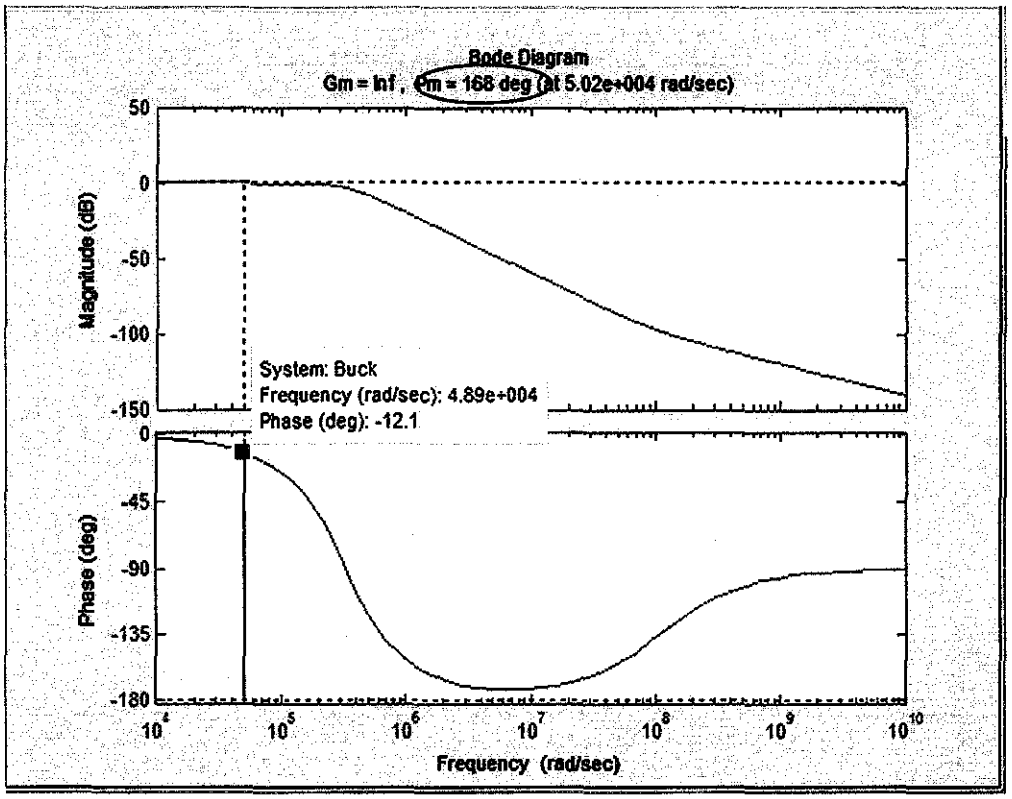



Figure 32: Bode plot of SBC_CCM

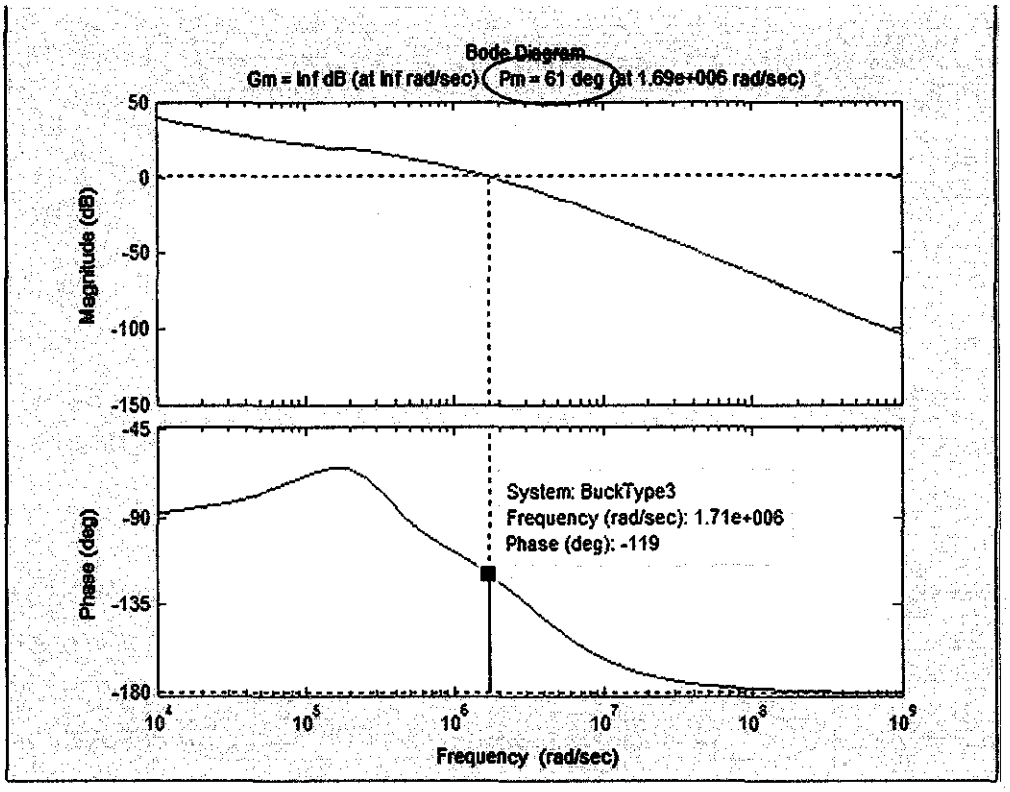



Figure 33: Bode plot of SBC with Compensator_CCM

Figure 32 and Figure 33 show the phase margin after and befire applying the Type III compensator. Here it is observed that the phase margin is decreased from 168° to 61°. The phase margin is determined by the differences between the phase at 0 dB gain to the -180°, where -180° is the critical output phase angle of the operational amplifier. Thus before the compensator is added the resultant phase margin is -12.1° - (-180°) = 167.9° which is almost accurate to the MATLAB simulation shown in Figure 32. This value shows that the system is less stable due to the phase margin obtained is beyond the feedback design characteristics. But once Type III compensator is added, the phase margin is given by -119°-(-180°) = 61°. This shows that the stability of the SBC system has been improved when constructed with the compensator.

*ii) SBC system (DCM)*

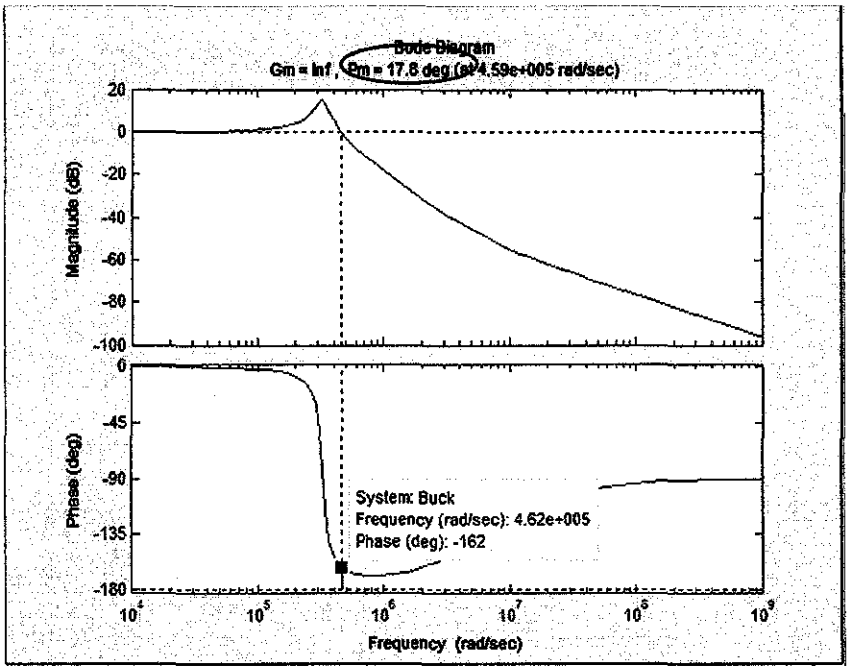



Figure 34: Bode plot of SBC_DCM

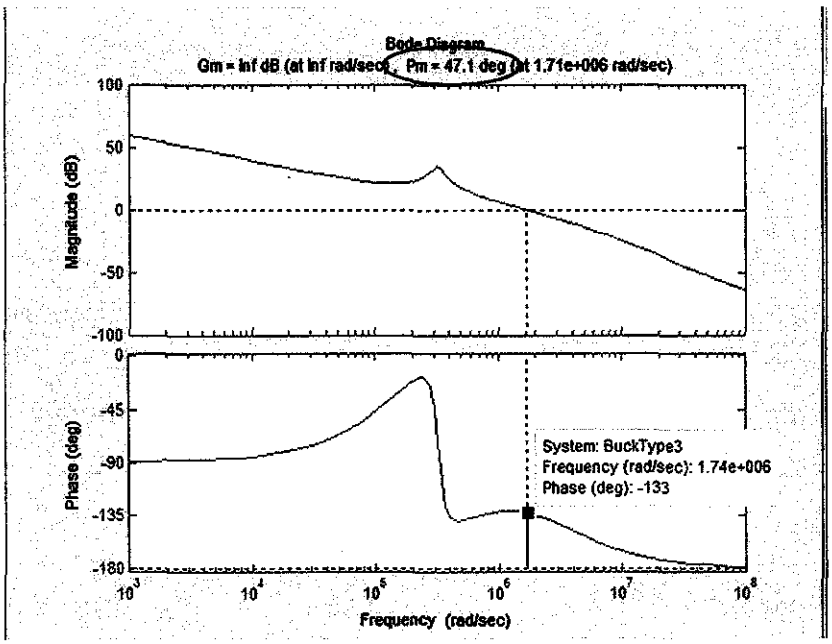



Figure 35: Bode plot of SBC with Compensator_DCM

Same goes when it is conducted in DCM. The bode plots as in Figure 34 and Figure 35 show the phase margin of the SBC increased from 17.8° to 47.1° which is good enough to ensure stability of the system. The phase margin for the SBC system without the compensator is given by -162° – (-180°) = 18°. Similarly, in CCM, the value obtained is almost the same to the MATLAB simulation result. After the system is modified with the compensator, the phase margin obtained is -133°-(-180°) = 47°. Although the phase margin does not reach up to 61° like in CCM, it still considers to be in the stabilized condition because it satisfies the feedback design characteristic where to ensure the stability of a system, the phase margin has to be more than 45° as stated in section 2.5.

#### *4.1.4.1 Compensator-AGD with SBC Simulation Graph for CCM*

After the compensator is designed, the SBC is ready to be resimulated completely with AGD at $M_2$ and the resultant waveforms for the converter are observed and analyzed.

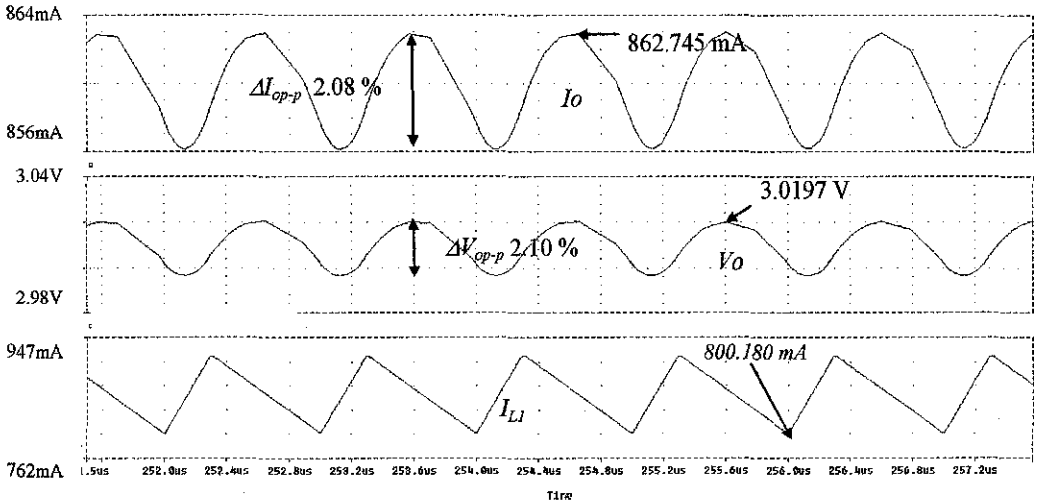



Figure 36: $I_o$, $V_o$, and $I_{L1}$ Compensator-AGD with SBC_CCM

Figure 36 shows the output voltage, current and inductor current for SBC. It is noticeable that the output voltage and current have increased compared to the circuit in Figure 15 and Figure 16. Besides, the output voltage and current waveforms have smaller ripples that present in it. Here output ripple voltage peak-to-peak, $\Delta V_{op\text{-}p}$ is 2.10 % $\left(\frac{3.020-2.988}{3.020} \times 100 \times 2\right)$ and output ripple current, $\Delta I_{op\text{-}p}$ also equal to 2.08 % $\left(\frac{862.745m-853.766m}{862.745m} \times 100 \times 2\right)$. For $I_{L1}$, it proves that the operation of the converter is in CCM where, there is no negative polarity shown in the waveforms.

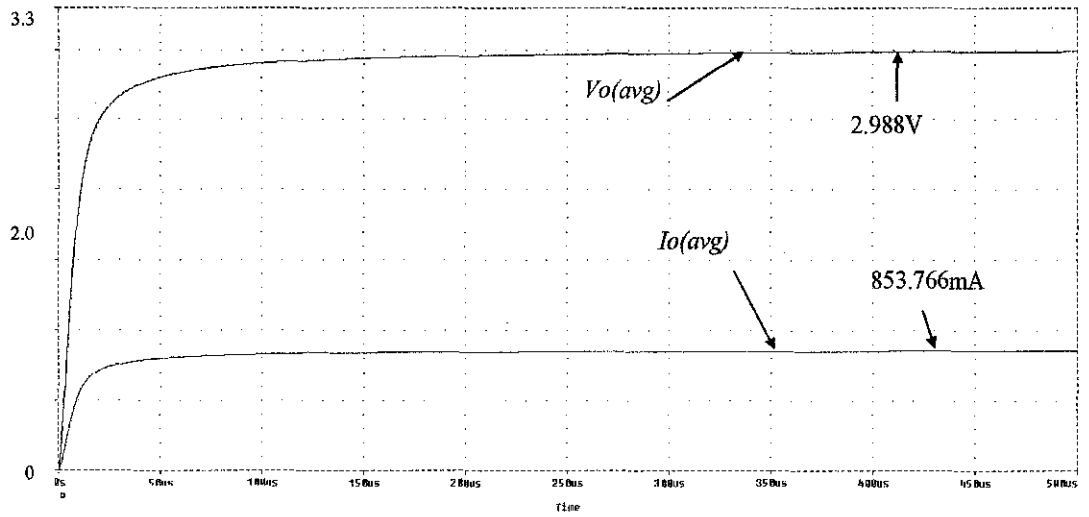



Figure 37: $V_{o(avg)}$ and $I_{o(avg)}$ Compensator-AGD with SBC _CCM

Figure 37 shows the average output voltage and current where the values are 2.988 V and 853.766 mA respectively. The value of the voltage almost satisfies the theoretical value for the SBC which is 3 V. Moreover, there are also some drawbacks occurred when both of the controllers are applied to the SBC. One of the drawbacks is shown in Figure 38.

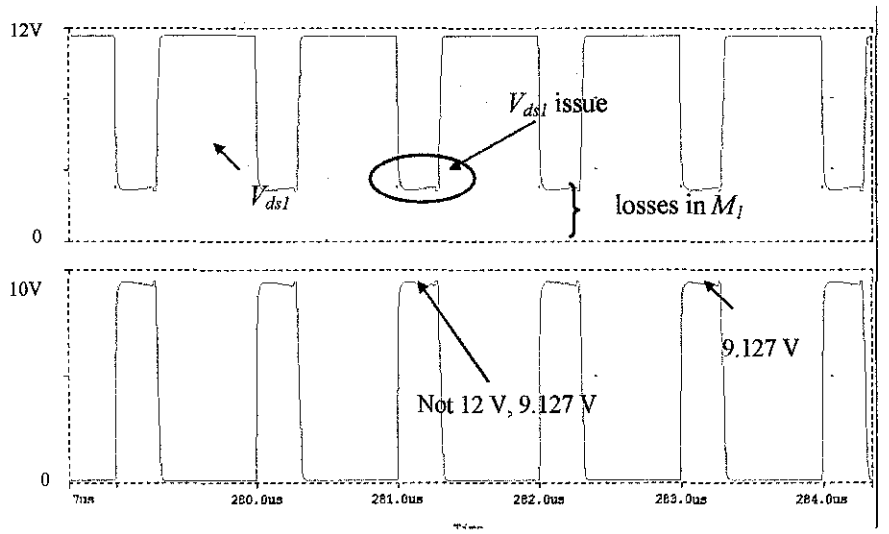



Figure 38: $V_{node}$, and $V_{ds1}$ for Compensator-AGD with SBC_CCM

Figure 38 above shows that $V_{node}$ is not 12 V. It only reaches to 9.127 V. Another 3 V is found to be in $M_1$. This is indicated in the black circle where the switching characteristic of the $V_{ds1}$ does not meet the expectation. In switching characteristic, the drain to source voltage, $V_{ds}$ is considered to turn off when the voltage is below than 1 V. But in this case the voltage only indicates at 3 V.

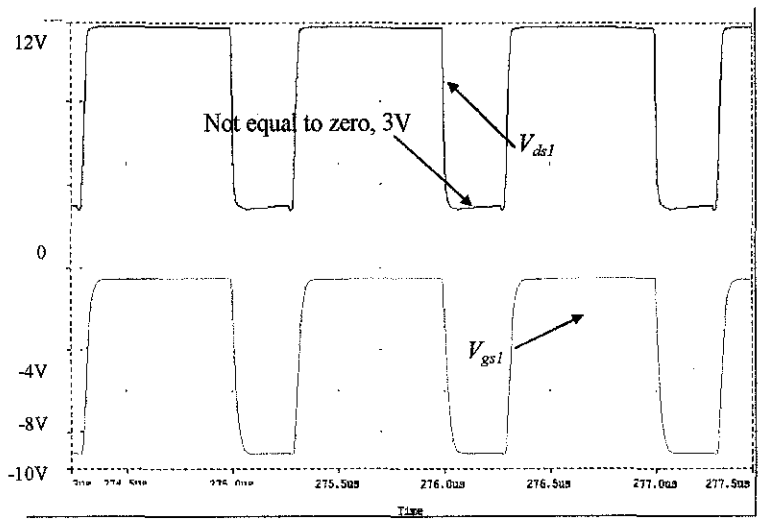



Figure 39: $V_{gs1}$ and $V_{ds1}$for Compensator-AGD with SBC_CCM

Based on the theory, when the gate to source voltage, $V_{gs}$ is turned on, the $V_{ds}$ has to be turned off and vice versa. As shown in Figure 39, $V_{ds1}$ for $M_1$ is not fully turned off when the $V_{gs1}$ is turned on. In this case, p-MOSFET is used as $M_1$ of the SBC and hence $V_{gs1}$ *is* turned on when negative voltage is supplied to $M_1$. Due to the improper turn-on and turned-off of the $V_{ds1}$ appear in SBC, this situation contributes to switching issue at $M_1$. However, $V_{node}$ obtained is considered to be enough to produce 3 V of output voltage since the voltage drop at the output inductor, $L_1$ is around 6 V. This is illustrated in Figure 40.

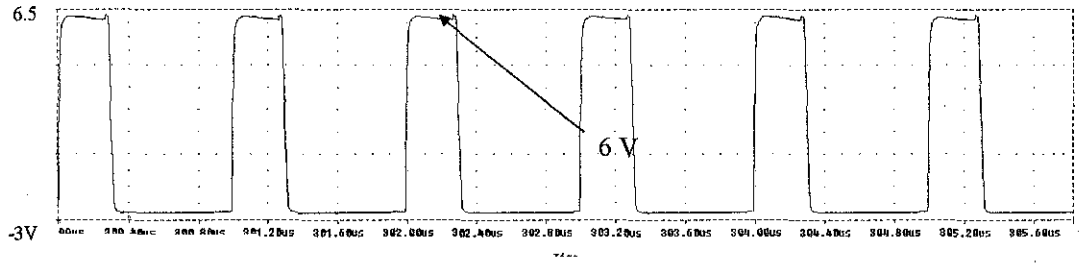



Figure 40: $V_{L1}$ for Compensator-AGD with SBC_CCM

### *4.1.4.2 Compensator-AGD with SBC Simulation Graph for DCM*

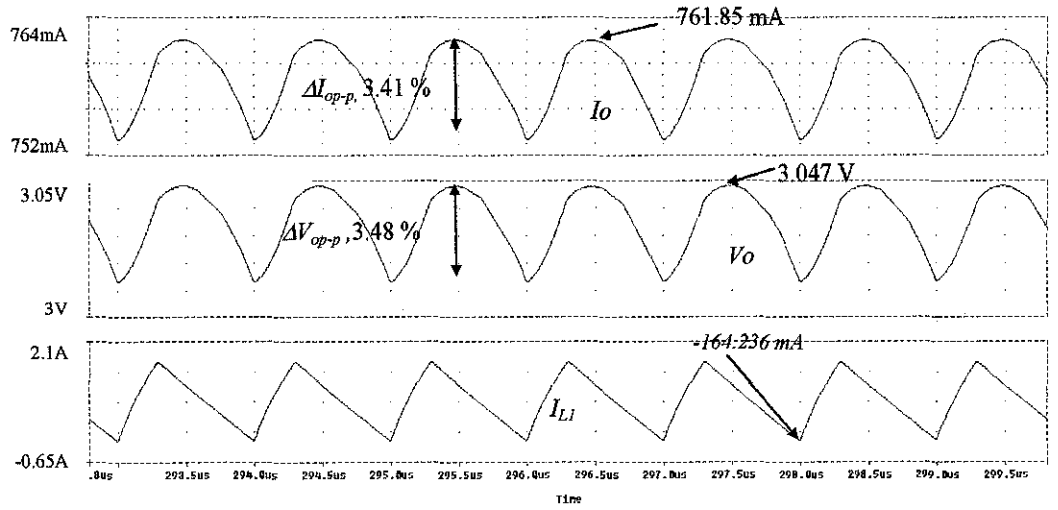



Figure 41: $I_o$, $V_o$, and $I_{L1}$ Compensator-AGD with SBC_DCM

Same as in CCM, Figure 41 illustrates the output current, voltage and inductor current for SBC in DCM. The, $\Delta V_{op\text{-}p}$ and $\Delta I_{op\text{-}p}$ are higher than in CCM. In this case, $\Delta V_{op\text{-}p}$ and $\Delta I_{op\text{-}p}$ reach up to 3.48 % $\left(\frac{3.047-2.994}{3.047} \times 100 \times 2\right)$ and 3.41 % $\left(\frac{761.85m-748.86m}{761.85m} \times 100 \times 2\right)$ respectively. Due to high ripples, the $I_o$ decreases compared to CCM and this is shown in Figure 40. For $V_o$, the average value of 2.994 V also shows that this value almost satisfies the theoretical value of 3 V. Then for $I_o$ the average value of 748.85 mA indicating that the current is decreasing as the SBC enters DCM. Both of the average values are shown in Figure 42.

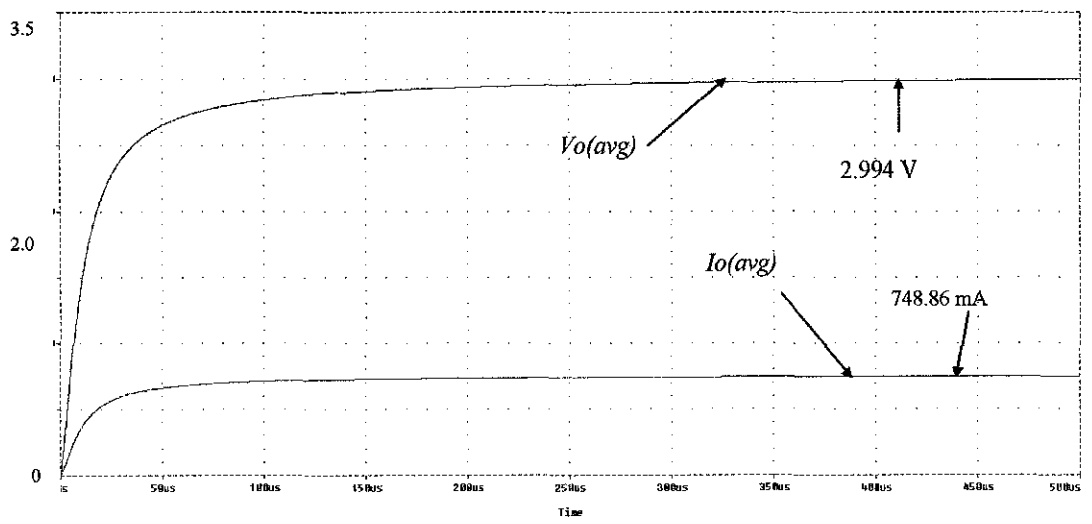



Figure 42: $V_{o(avg)}$ and $I_{o(avg)}$ Compensator-AGD with SBC _DCM

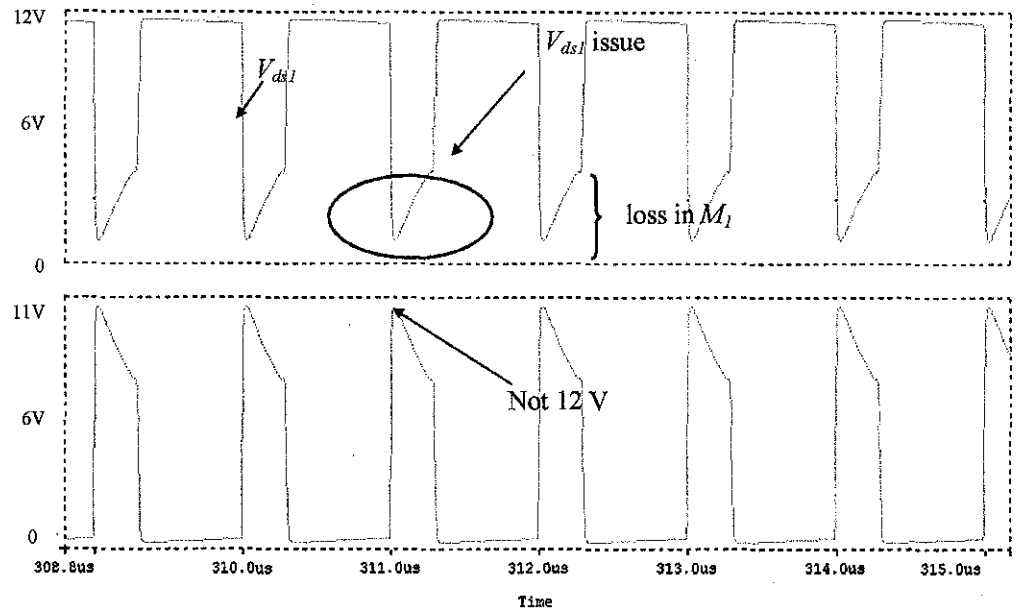



Figure 43: $V_{node}$, and $V_{ds1}$ for Compensator-AGD with SBC_DCM

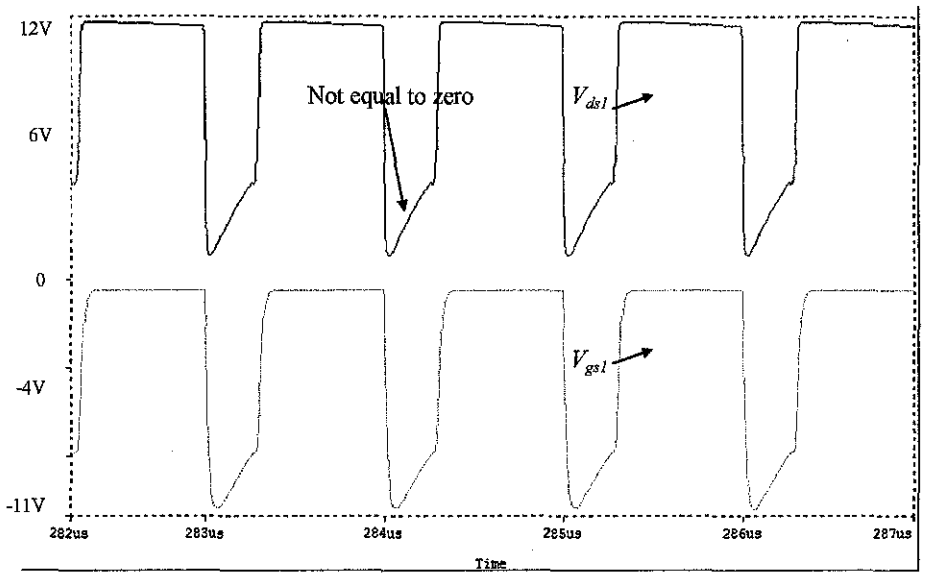



Figure 44: $V_{gs1}$ and $V_{ds1}$ for Compensator-AGD with SBC_DCM

The SBC also experiences the issue where $V_{node}$ which is not equal to 12 V and it is shown in Figure 43. This is due to the same reason as in CCM where the $V_{ds1}$ does not meet the switching characteristics. Both of them also experience same problem as in CCM where $V_{gs1}$ and $V_{ds1}$ issue are not theoretically correct. This is shown in Figure 44.

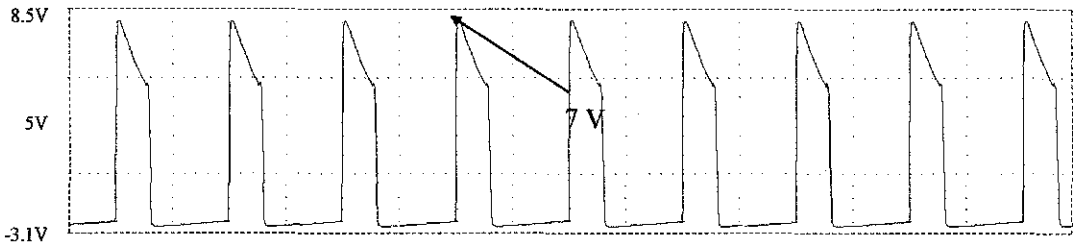



Figure 45: $V_{L1}$ for Compensator-AGD with SBC_DCM

But the resultant waveforms for this converter still manage to produce 3 V of output voltage because the voltage across the inductor is 7 V as shown in Figure 45.

Table 6: Compensator- AGD with SBC for CCM and DCM

| | Compensator-AGD | | |
|---|---|---|---|
| | CCM | DCM | Improvement of Compensator-AGD_CCM to DCM (%) |
| $V_{o(avg)}$, (V) | 2.99 | 2.99 | 0.00 |
| $I_{oavg}$, (mA) | 853.77 | 748.86 | 12.29 |
| $I_{Lmax\ peak}$ (A) | 0.92 | 1.63 | -77.17 |
| $\Delta V_{op\text{-}p}$ (%) | 2.10 | 3.48 | 65.71 |
| $\Delta I_{op\text{-}p}$ (%) | 2.08 | 3.41 | 63.94 |
| $P_{BD}$ (mW) | 0.00 | 0.00 | 0.00% |

Based on Table 6, it has same results similar to Table 5 where the resultant output for voltage and current have higher values in CCM and lower in DCM. Besides, it results in smaller ripple values compared to AGD with SBC circuit which is shown in Figure 28. But the ripples increase as it enters the DCM. This is due to the small value of inductor used that results in large peak inductor current

and output ripple current which generates large switching noise and ripple voltages at the output [22].

## 4.2 Comparison of Continuous and Self-driven PWM in High Frequency Converter.

Here the continuous driven behaviour will be observed based on CGD with SBC circuits. For the self-driven, it will be represented by the AGD with SBC and Compensator-AGD on SBC circuits. In this work the differences between all the circuits are observed for their node voltage, body diode conduction losses, output voltage and current, and the gate voltages, $V_{gs}$ for $M_1$.

It is found that they are some improvements at the output voltage and current and also some drawbacks seen when the controllers are applied to both $M_1$ and $M_2$. Hence each of the waveforms obtained are compared in order to see the significant differences between all the designed circuits for both CCM and DCM.

*4.2.1 Node Voltage*

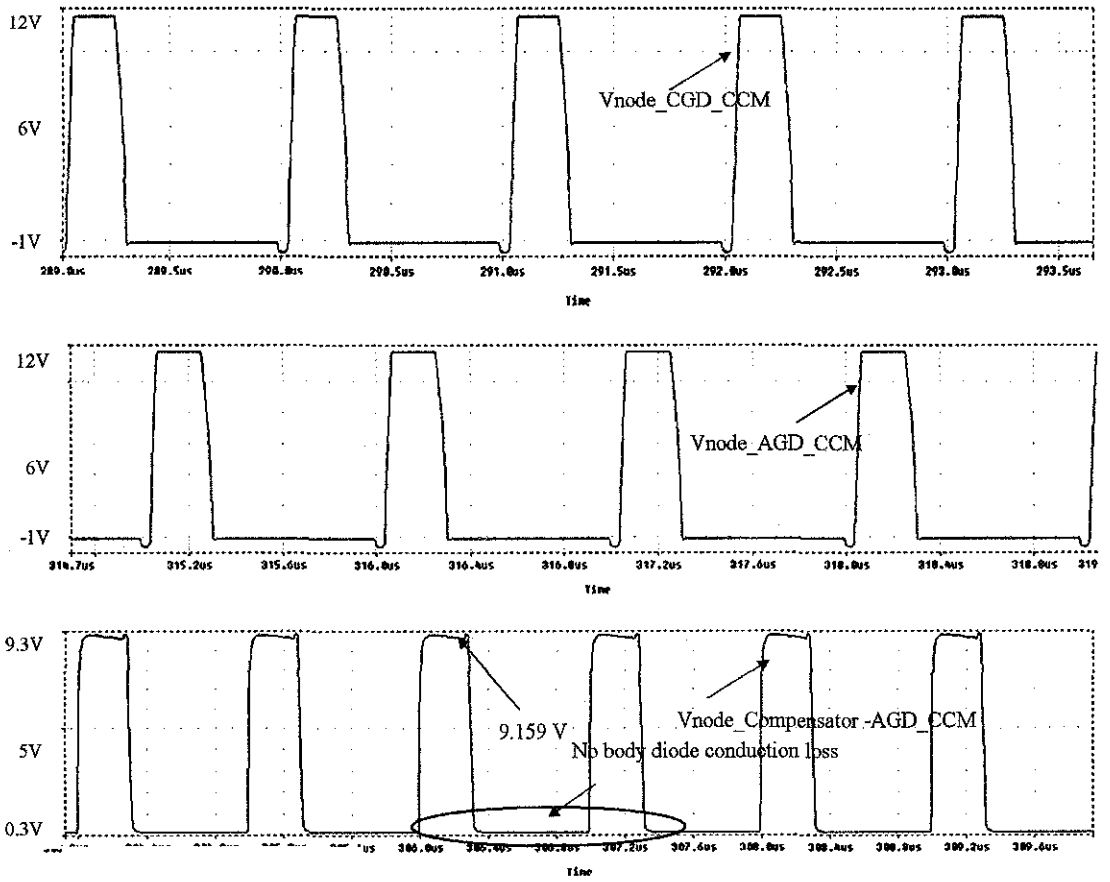



Figure 46:$V_{node}$, body diode for CGD, AGD, Compensator-AGD_CCM

As mentioned before, node voltage is one of the important points to be observed. It indicates the correct switching signal that will be fed into the converter. For all the conduction modes, $V_{node}$ has to be close to the input voltage. Figure 46, shows the $V_{node}$ of all the circuits in CCM. For Figure 47, it shows the $V_{node}$ in DCM.

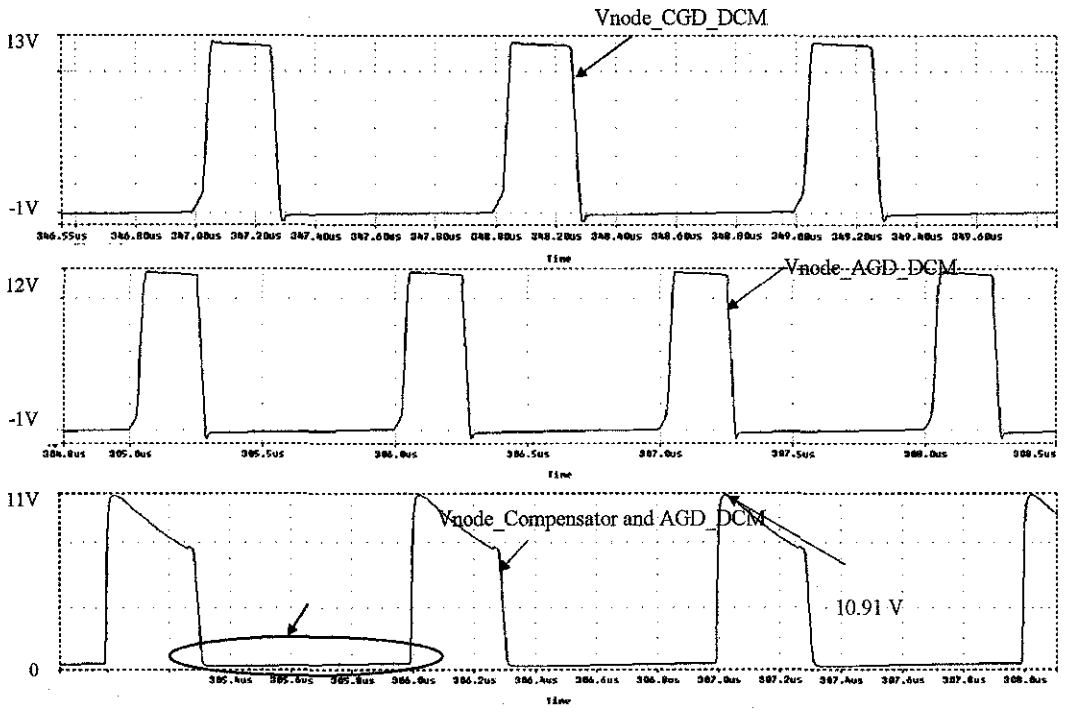



Figure 47: $V_{node}$, body diode for CGD, AGD, Compensator-AGD_DCM

From Figure 46 and Figure 47, $V_{node}$ for the combination of Type III compensator and AGD is not equal to the input voltage. It has the value of 9.159 V for CCM and 10.91 V for DCM. The remaining voltages are dissipated in $M_1$. This can be observed where the $V_{ds1}$ as shown in Figure 38 and Figure 43 does not fully turn on and off correctly. Both the turn-on and turned-off states for $V_{ds1}$ start and stop at 3 V due to the same switching issue which is stated in section 4.1.4.1 This is also similar for the SBC operating in DCM. Although the switching signal is not really accurate when the compensator and AGD are applied, it is still able to produce 3 V of the output voltage. Eventually, the voltage across the inductor for CCM and DCM are 6 V and 7 V respectively and this is proven by $V_0 = V_{node} - V_{L1}$.

*4.2.2 Body Diode Conduction Loss*

Body diode conduction loss is detected when $M_1$ and $M_2$ are switched off. So it is important to keep the dead time for both switches small enough so that, the losses can be minimized.

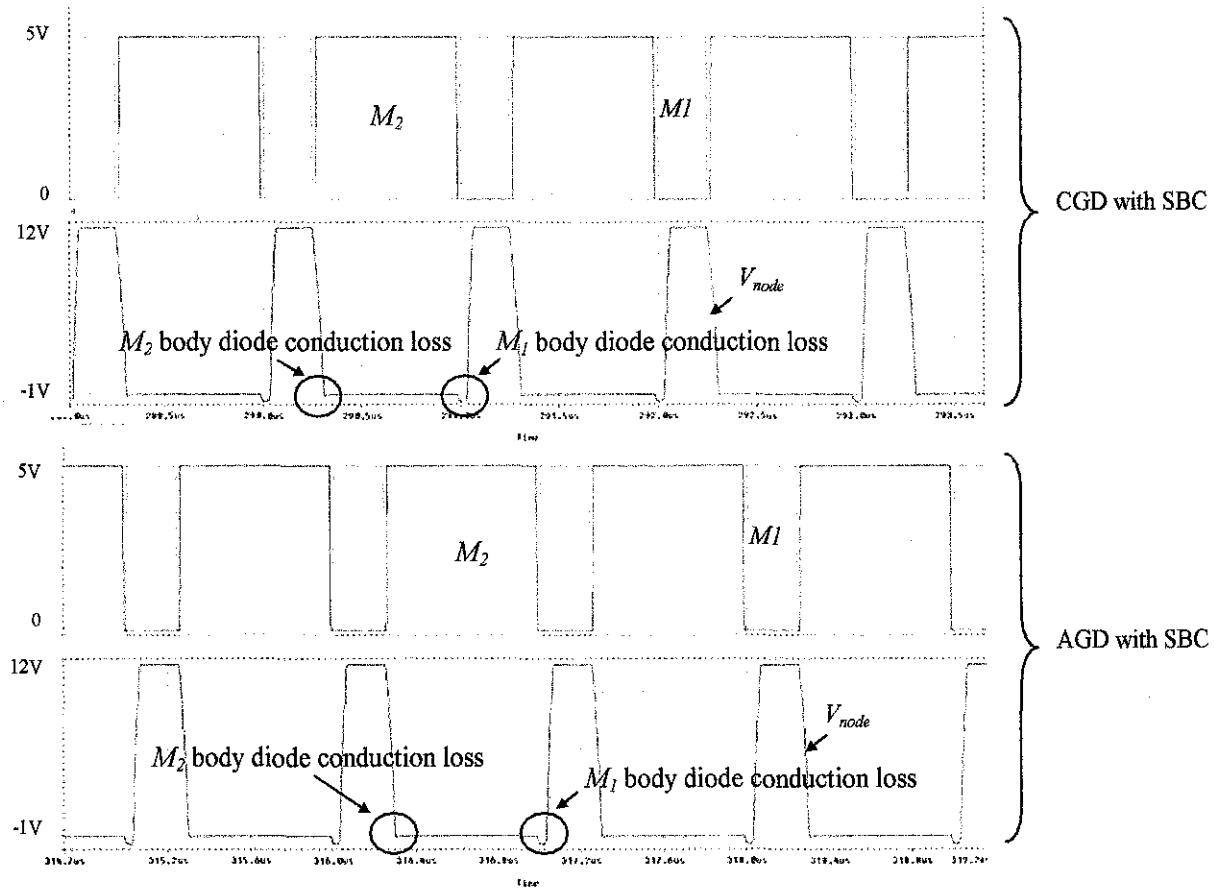



Figure 48: Body diode co for CGD with SBC and AGD with SBC_CCM

Figure 48 indicates the body diode conduction for CGD with SBC and AGD with SBC circuits in CCM. In CCM mode, the body diode conduction occurs at both $M_1$ and $M_2$. Although it is seen that the $M_2$ body diode undershoot voltage is less than -0.3 V, it is still counted as the body diode conduction loss because there is current of $I_{ds2}$ flowing in it. $I_{ds2}$ has the negative value which

indicates the duration of body diode conduction of $M_2$. Figure 49 below shows the $I_{ds2}$ and $V_{node}$ for CGD with SBC and AGD with SBC circuits in CCM.

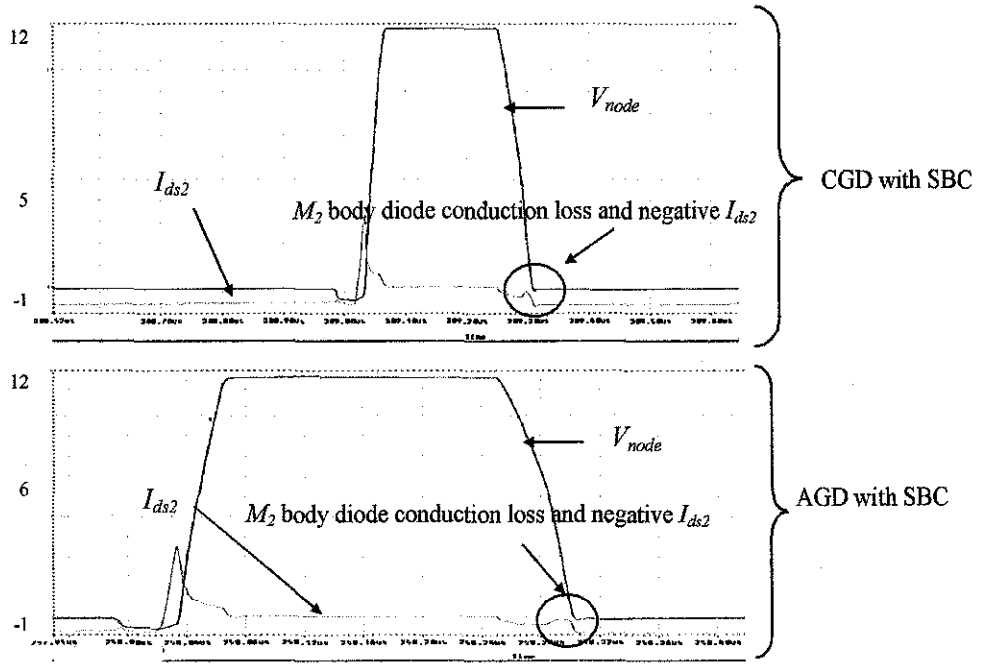



Figure 49: $I_{ds2}$ and $V_{node}$ for CGD and AGD with SBC_CCM

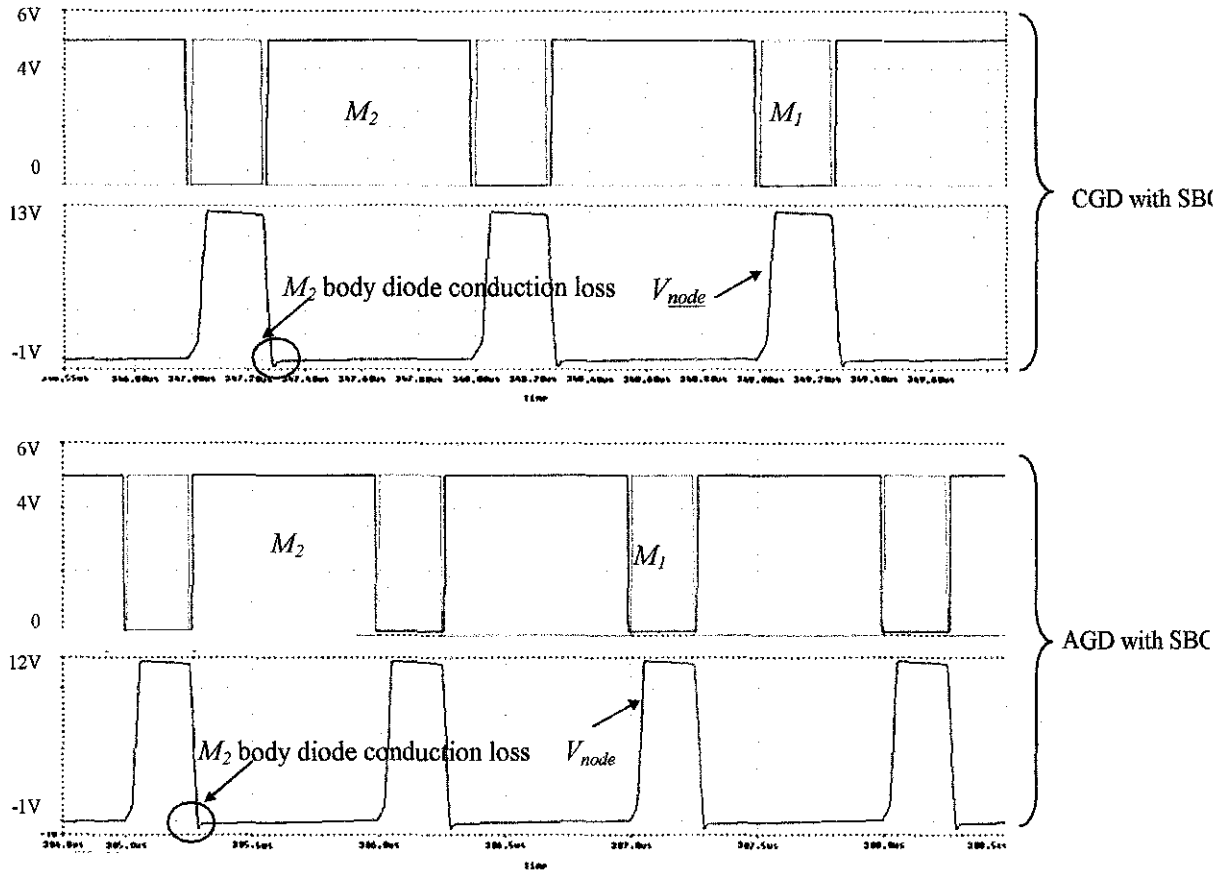



Figure 50: Body diode conduction for CGD with SBC and AGD with SBC_DCM

For DCM there is only $M_2$ body diode conduction in both CGD with SBC and AGD with SBC which is proven in Figure 50. Thus the total of body diode conduction loss in DCM is much smaller than it is in CCM. Meanwhile when Type III compensator and AGD are implemented in the SBC circuit, there is no body diode loss in the converter for both CCM and DCM. This is shown in Figure 46 and Figure 47. By having a controller that controls the switching of both $M_1$ and $M_2$, this can improve the performance of the SBC since the dead time between them can be adjusted accordingly.

### *4.2.3 Output Voltage and Current*

Having AGD to control $M_2$ of the SBC, this has slightly decreased the output voltage and current. But as it is implemented with the compensator, the output voltage almost satisfies the theoretical value of 3V as illustrated in Figure 37 and Figure 42. Besides, the output current also increases for CCM and DCM compared when the SBC is constructed with the AGD and CGD. However, the combination of compensator and AGD results in high output voltage and current ripples when it is operated in DCM. They have the highest ripple percentage compared to the SBC with AGD and also with CGD. So implementing both with the controllers to the SBC also gives some disadvantages and advantages.

### *4.2.4 Gate to Source Voltage, $V_{gs1}$ of $M_1$*

In this project, the gate to source voltage of $M_1$, $V_{gs1}$ is observed. This is because, for the compensator and AGD with SBC, type p-MOSFET is used to turn on the converter. The purpose of using this type of MOSFET is to regulate voltage and current regulation by means of suitable feedback [23]. Since the compensator is also one of the feedback circuits, p-MOSFET is chosen to be the $M_1$ switch so that the converter can have correct switching voltage. Besides, having p-MOSFET used as $M_1$ in a totem-pole arrangement with an n-MOSFET will simulate high current and high power complementary MOS, CMOS arrangement [24].

Thus the difference in the $V_{gs1}$ for this circuit requires a negative voltage to turn on the p-MOSFET. For CGD and AGD with SBC circuits, positive voltage is needed since they use n-MOSFET as $M_1$. Figure 51 shows the $V_{gs1}$ for, CGD with SBC, AGD with SBC and Compensator- AGD with SBC.

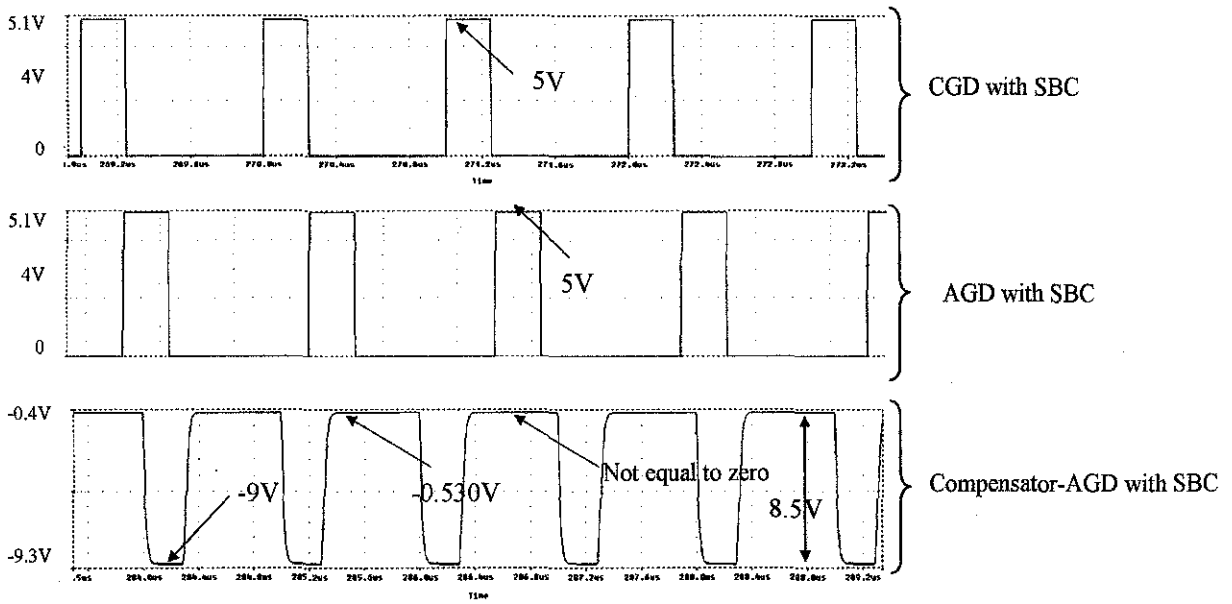



Figure 51: $V_{gs1}$ for CGD, AGD and Compensator-AGD with SBC

From Figure 51, it is noticed that $V_{gs1}$ for Compensator-AGD with SBC, does not reach zero when they are turned off. It has the value of -0.530 V. However, it is considered to be off because the value of -0.530V is below the $V_{th}$ of the p-MOSFET. The $V_{th}$ of the MOSFET can be obtained based on the type of the p-MOSFET used. Here the p-MOSFET used is from IRFR9212 family having -4V of $V_{th}$ [25]. Besides $V_{gs1}$ for compensator-AGD circuit gives high switching voltage that is around 8.5 V compared to CGD and AGD with SBC circuits which is only 5 V.

Table 7: Comparison between AGD and Compensator- AGD for CCM

| | CCM | | |
|---|---|---|---|
| | AGD | Compensator-AGD | Improvement of Compensator-AGD to AGD (%) |
| $V_{o(avg)}$, (V) | 2.68 | 2.99 | 10.37 |
| $I_{oavg}$, (mA) | 765.76 | 853.77 | 10.31 |
| $I_{Lmax\ peak}$ (A) | 0.84 | 0.92 | 8.70 |
| $\Delta V_{op\text{-}p}$ (%) | 2.23 | 2.10 | 6.19 |
| $\Delta I_{op\text{-}p}$ (%) | 2.21 | 2.08 | 6.25 |
| $P_{BD}$ (mW) | 20.79 | 0.00 | 100 |

Table 8: Comparison between AGD and Compensator - AGD for DCM

| | DCM | | |
|---|---|---|---|
| | AGD | Compensator - AGD | Improvement of Compensator-AGD to AGD (%) |
| $V_{o(avg)}$, (V) | 2.68 | 2.99 | 10.37 |
| $I_{o(avg)}$, (mA) | 670.60 | 748.86 | 10.45 |
| $I_{Lmax}$ peak (A) | 1.72 | 1.63 | 5.52 |
| $\Delta V_{op\text{-}p}$ (%) | 1.65 | 3.48 | -52.59 |
| $\Delta I_{op\text{-}p}$ (%) | 1.62 | 3.41 | -52.49 |
| $P_{BD}$ (mW) | 4.63 | 0.00 | 100 |

Table 7 and Table 8 show the improvements between AGD and Compensator-AGD circuit with SBC based on their conduction mode. Overall it is seen that adding controllers to the conventional SBC shows several improvements especially in increasing the output voltage, current, lowering the ripples and also eliminating the body diode conduction loss. However, it still has drawbacks such as an increase in output voltage and current ripples when the converter enters the DCM.

On the other hand, implementing AGD to $M_2$, is not really practical because based on Table 7 and Table 8, it shows that the combination of two controllers are much better than adding AGD only to the SBC. This is because, AGD only controls the dead time of both switches and by constructing it with the SBC, it results in decreasing the output voltage and current. Therefore this AGD control scheme is not recommended for $M_2$ of the SBC, since the purpose of this project is to obtain output current as high as possible.

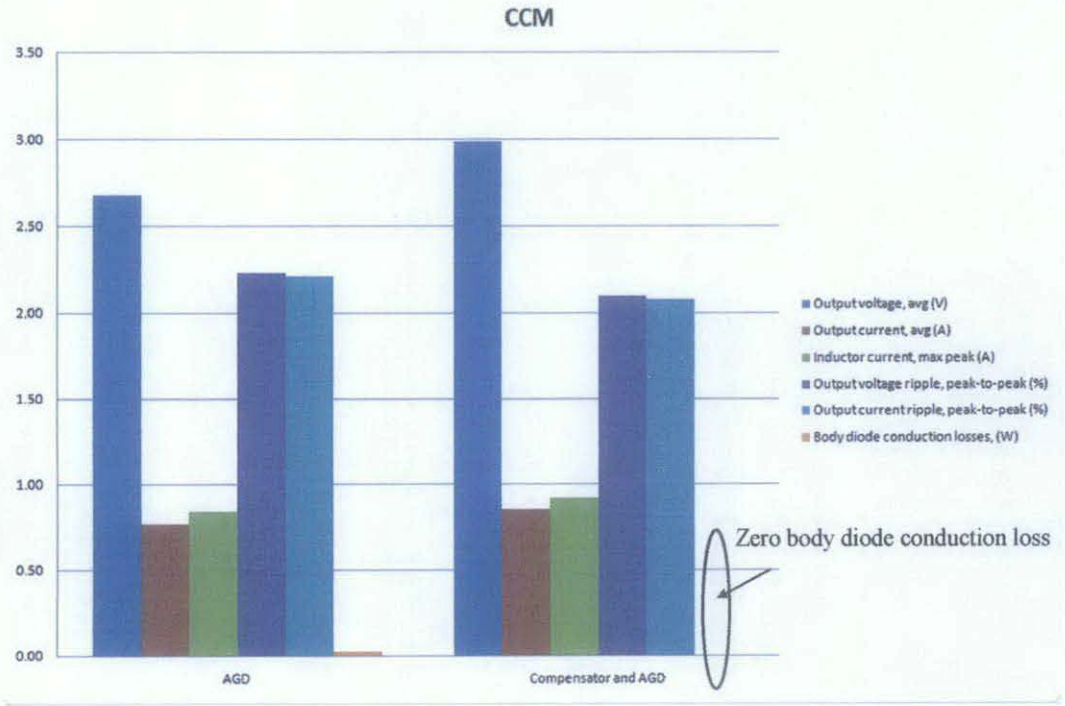



Figure 52: Comparison between AGD and Compensator-AGD for CCM

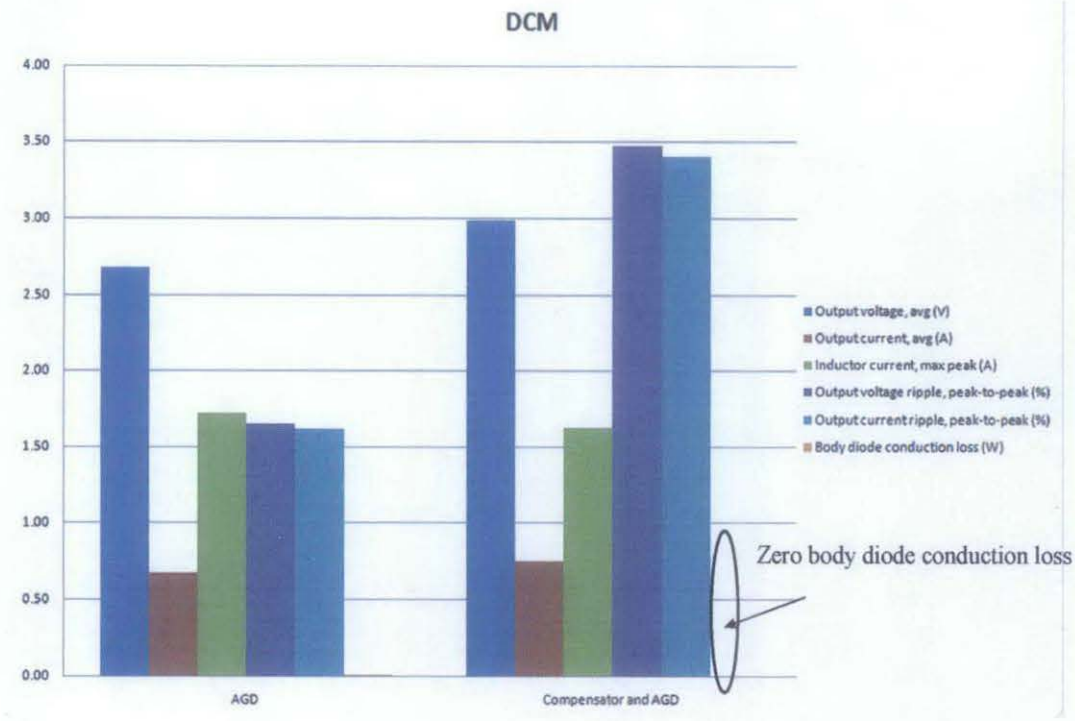



Figure 53: Comparison between AGD and Compensator-AGD for DCM

Figure 52 and Figure 53 show the comparison between AGD and the combination of compensator and AGD for CCM and DCM respectively. The figures indicate that the output voltage and current have improved when the converter is modified to be a self-driven circuit. In addition the body diode conduction loss becomes zero as both controllers are implemented to the circuit. This shows that both $M_1$ and $M_2$ fully turn on and off alternately without allowing the circulating inductor current flows into the body diode. Here both of the controllers manage to compensate the dead time for $M_1$ and $M_2$ to minimum as possible.

However, not all self driven gate drivers can guarantee a perfect and desired output since it also needs some improvements and modifications. Thus the continuous and self driven PWM have their own advantages and drawbacks when they are applied to the SBC circuit.

## 4.3 Comparative Assessments of SBC with Continuous and Self Driven Gate Drive circuits.

In this project the conventional SBC is also compared with the CGD, AGD, Compensator-AGD, MPPT-$V_{pulse}$ circuit (APPENDIX B) and also the parallelism of $M_1$ and $M_2$ (APPENDIX B). The continuous driven behaviour is analyzed based on the SBC constructed with CGD and when both of the switches are paralleled with more than one MOSFET. For the self-driven characteristics, three circuits will be compared. They are SBC modified by adding the AGD to $M_2$, combining Type III compensator with AGD and also the combination of the MPPT and $V_{pulse}$.

The analysis is done based on the output voltage, current, peak-to-peak ripple and body diode conduction losses. In parallelism technique, $M_1$ is paralleled with four MOSFET and it is applied to the CCM [26]. Meanwhile for DCM, $M_1$ is paralleled with four MOSFETs and for $M_2$, with three MOSFETs. All data are tabulated in Table 9 and Table 10 for the CCM and Table 11 and Table 12 for DCM.

Table 9: Comparison between CGD, AGD, Compensator-AGD, Parallelism, and MPPT_CCM

| | CCM | | | | |
|---|---|---|---|---|---|
| | CGD [19] | AGD | Compensator -AGD | Parallelism- $M_1$:4, $M_2$:1 [26] | MPPT- $V_{pulse}$ [27] |
| $V_{o(avg)}$, (V) | 2.70 | 2.68 | 2.99 | 2.69 | 3.09 |
| $I_{oavg}$, (mA) | 770.26 | 765.76 | 853.77 | 863.84 | 882.27 |
| $\Delta V_{o\ p\text{-}p}$ (%) | 1.66 | 2.23 | 2.10 | 1.86 | 0.95 |
| $\Delta I_{o\ p\text{-}p}$ (%) | 1.62 | 2.21 | 2.08 | 2.36 | 0.95 |
| $P_{BD}$ (mW) | 16.87 | 20.79 | 0.00 | 10.70 | 0.00 |

Table 10: Improvement of CGD, AGD, Compensator-AGD, Parallelism and MPPT_CCM

| | CCM | | | | | | |
|---|---|---|---|---|---|---|---|
| | Improvement of AGD to CGD (%) | Improvement of AGD to Parallelism (%) | Improvement of AGD to MPPT (%) | Improvement of Compensator-AGD to CGD (%) | Improvement of Compensator – AGD to AGD (%) | Improvement of Compensator-AGD to Parallelism (%) | Improvement of Compensator-AGD to MPPT-$V_{pulse}$ (%) |
| $V_{o(avg)}$, (V) | -0.75 | -0.37 | -15.30 | 9.70 | 10.37 | 10.03 | -3.34 |
| $I_{oavg}$, (mA) | -0.59 | -12.81 | -15.21 | 9.78 | 10.31 | -1.18 | -3.34 |
| $\Delta V_{o\ p\text{-}p}$ (%) | -25.56 | -16.59 | -57.40 | -20.95 | 6.19 | -11.43 | -54.76 |
| $\Delta I_{o\ p\text{-}p}$ (%) | -26.70 | 6.79 | -57.01 | -22.12 | 6.25 | 13.46 | -54.33 |
| $P_{BD}$ (mW) | -18.86 | -48.53 | -100 | 100.00 | 100.00 | 100.00 | 0.00 |

Table 11: Comparison between CGD, AGD, Compensator-AGD, Parallelism, and MPPT_DCM

| | DCM | | | | |
|---|---|---|---|---|---|
| | CGD [19] | AGD | Compensator - AGD | Parallelism- $M_1$:4, $M_2$: 3 [26] | MPPT- $V_{pulse}$ [27] |
| $V_{o(avg),}$ (V) | 2.70 | 2.68 | 2.99 | 2.74 | 3.11 |
| $I_{oavg,}$ (mA) | 676.13 | 670.60 | 748.86 | 758.52 | 777.81 |
| $V_{o\ p\text{-}p}$ (%) | 1.06 | 1.65 | 3.48 | 1.34 | 1.35 |
| $I_{o\ p\text{-}p}$ (%) | 1.02 | 1.62 | 3.41 | 1.00 | 1.35 |
| $P_{BD}$ (mW) | 6.29 | 4.63 | 0.00 | 0.00 | 0.00 |

Table 12: Improvement of CGD, AGD, Compensator-AGD, Parallelism, and MPPT_DCM

| | DCM | | | | | | |
|---|---|---|---|---|---|---|---|
| | Improvement of AGD to CGD (%) | Improvement AGD to parallelism (%) | Improvement AGD to MPPT (%) | Improvement of Compensator-AGD to CGD (%) | Improvement of Compensator-AGD to AGD (%) | Improvement of Compensator-AGD to Parallelism (%) | Improvement of Compensator-AGD to MPPT-$V_{pulse}$ (%) |
| $V_{o(avg),}$ (V) | -0.75 | -2.24 | -16.05 | 9.70 | 10.37 | 8.36 | -4.01 |
| $I_{oavg,}$ (mA) | -0.82 | -13.11 | -15.99 | 9.71 | 10.45 | -1.29 | -3.87 |
| $V_{o\ p\text{-}p}$ (%) | -35.76 | -18.79 | -18.19 | -69.54 | -52.59 | -61.49 | -61.21 |
| $I_{o\ p\text{-}p}$ (%) | -37.04 | -38.27 | -16.67 | -70.09 | -52.49 | -70.67 | -60.41 |
| $P_{BD}$ (mW) | 35.85 | -100 | -100 | 100 | 100.00 | 0.00 | 0.00 |

### *4.3.1 Comparison in CCM*

Table 9 and Table 10 indicate the comparisons and improvements of the CGD, AGD, compensator, MPPT and parallelism of the SBC in CCM respectively. From the tables, it is observed that AGD with SBC has the lowest values for output voltage and current compared to others. Besides, the SBC has the highest body diode conduction loss when AGD is added to $M_2$ compared to when it is implemented with the other circuits. Here the value of the body diode conduction loss is 20.79 mW (Table 9).

In terms of output voltage ripples, the AGD with SBC circuit has the highest value where the ripple is 2.23 % (Table 9). However when the SBC is upgraded by combining the Type III compensator to $M_1$, this proposed SBC becomes the third best circuit. This is because, there are some improvements to the output voltage, current and also reduction in body diode conduction losses. Here the body diode conduction loss in the circuit is equal to zero.

For the output voltage, it satisfies the design requirement. Similar in adding AGD only to $M_2$, the combination of compensator and AGD also results in highest output peak-to-peak voltage ripple, 2.10 % (Table 9). For the output peak-to-peak ripple current, the SBC results in highest value when $M_1$ is paralleled with four MOSFETs.

Thus from the observations, SBC with AGD implemented to $M_2$, does not meet the desired results as it decreases the output voltage, current and increases the voltage and current ripple and also the body diode conduction losses. Even the CGD with SBC can produce higher output voltage and current compared when it is modified with the AGD control scheme. The CGD improves the output voltage by 0.75 % and 0.59 % (Table 10) for the output current.

In addition when the compensator is constructed with AGD in SBC circuit, those parameters which are the output voltage and current have improved. But it is

the third best circuit because, the best results that SBC can achieve is when the MPPT control circuit is applied.

As in Table 9, when the SBC with MPPT controller [27] is applied to it, this improves the output voltage up to 3.09 V, output current up until 882.27 mA and also lowers the output ripple peak-to-peak for both voltage and current to 0.95 % only. Similar to compensator-AGD, adding MPPT controller can also reduce the body diode conduction losses to zero.

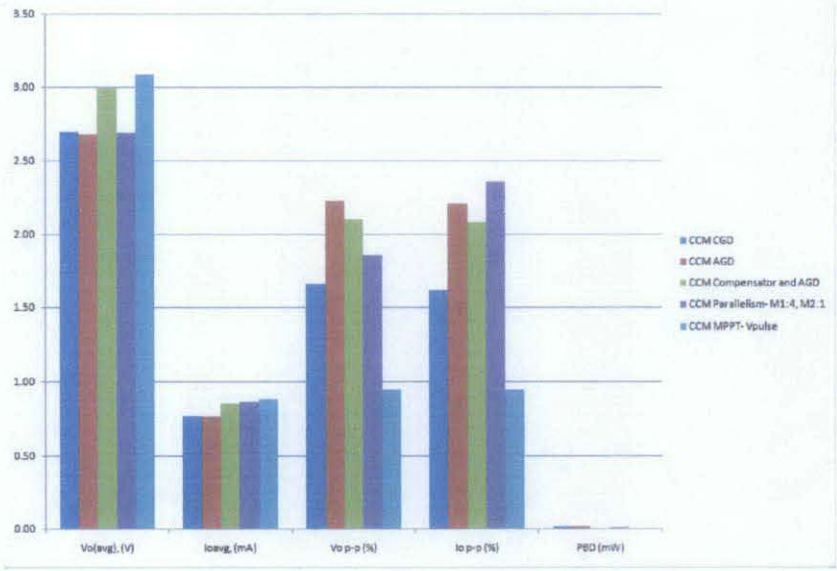



Figure 54: Comparison between CGD, AGD, Compensator-AGD, Parallelism and MPPT-$V_{pulse}$ for CCM

Figure 54 illustrates the performance of SBC with CGD, AGD, parallelism, compensator-AGD and MPPT-$V_{pulse}$ circuits operating in CCM. It shows that the MPPT-$V_{pulse}$ has the best performance due to high output voltage and current and smaller output peak-to-peak ripples which are much smaller when compared to others. For AGD with SBC only, it becomes the least best circuit because of the lowest output voltage and current values and highest ripples at the output. As for the combination of compensator and AGD, it requires to have some

improvements so that the resultant output peak-to-peak ripples can be less and hence improve the efficiency of the SBC. To eliminate the body diode conduction loss, compensator-AGD and MPPT-$V_{pulse}$ are most recommended controllers to be applied to the SBC.

### *4.3.2 Comparison in DCM*

In DCM, Table 11 and Table 12 show the comparisons and improvements of CGD, AGD, parallelism, Compensator-AGD and MPPT-$V_{pulse}$ circuits implemented to SBC respectively. In this case, comparison is almost similar in CCM where, by implementing AGD to SBC results in the lowest output current and voltage. The only different is in term of the body diode conduction losses where CGD with SBC, this results in highest value which is given by 6.29mW (Table 11). When adding AGD only to $M_2$, the body diode conduction loss is reduced by 35.85% (Table 12). This in line with the function of the AGD controller where it controls the dead time to the smallest value.

The combination of compensator and AGD also is the third best circuit when the output voltage and current are taken into account. Both of the output parameters increase once the two controllers are constructed with SBC. However SBC with MPPT circuit would be the most preferable combination since it yields the highest output voltage and current.

The compensator-AGD with SBC circuit gives the highest output peak-to-peak ripple voltage and current. Here the ripples are 3.48% and 3.41% respectively (Table 11). Thus it can be said that the performance of the SBC decreased due to the high ripple when the controllers are applied to SBC.

Compared to CGD and the parallelism, both of them have less output voltage and current ripples. It is observed when SBC's switches are paralleled with more than one MOSFET where the output ripple current reduces to 1% (Table 11).

On the other hand, in DCM the SBC experiences the reduction in body diode conduction loss for the case of parallelism, Compensator- AGD and MPPT-$V_{pulse}$. This is shown as in Table 11.

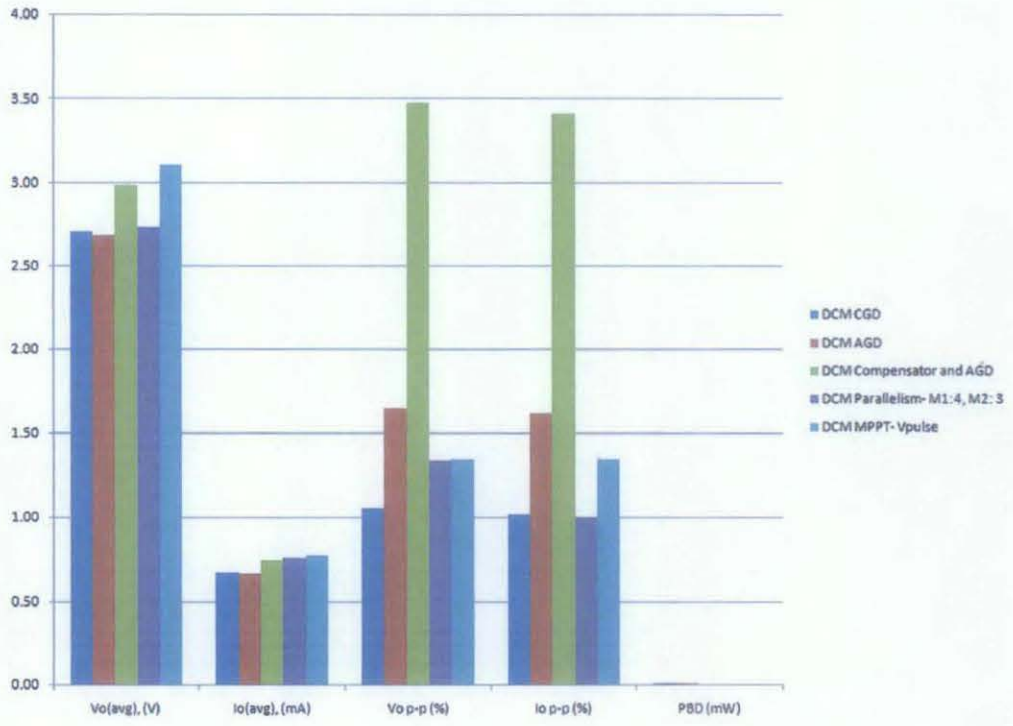



Figure 55: Comparison between CGD, AGD, Compensator-AGD, Parallelism and MPPT-$V_{pulse}$ for DCM

Figure 55 illustrates the performance of SBC with SBC, AGD, Compensator-AGD, parallelism, and MPPT-$V_{pulse}$ circuits as it is in DCM. From the figure, the SBC with compensator-AGD results in the highest ripples values compared to CGD, AGD, parallelism and MPPT-$V_{pulse}$. Having more ripples at the

output which can decrease the overall performance of the SBC. Similarly in CCM, applying AGD controller only to the SBC is not practical because from overall observation, it actually results in lowest output voltage and current, and also higher ripples at the output. Furthermore, although the resultant ripples in the Compensator-AGD with SBC are the highest, it still produces higher output current, voltage and reduces the body diode conduction loss. It just needs some improvements and modifications such as selecting the appropriate p-MOSFET based on designed specification in order to further reduce the output ripples.

# CHAPTER 5

# CONCLUSIONS AND RECOMMENDATIONS

## 5.1 Conclusions

Throughout the research, two types of gate drivers are designed and constructed. The first gate driver is the conventional gate driver, (CGD) which can be categorized as the continuous gate driver and the self driven gate driver. Both of the gate driver circuits are integrated with the synchronous buck converter, (SBC). As for the self driven gate driver, an AGD circuit has been implemented to $M_2$ and Type III compensator to the $M_1$ of the SBC circuit.

Based on the results, adding AGD to $M_2$ can reduce the body diode conduction loss and provide the shortest $t_D$ between $M_1$ and $M_2$ without producing shoot-through. Modifying the SBC by adding both controllers have improved the performance as this result in virtually zero $P_{BD}$ and less ripples compared to AGD. For SBC in CCM, it shows that the converter with both types of the gate drivers can produce high output current compared to DCM. However in DCM, the body diode conduction loss for the SBC is reduced.

In addition, the AGD and Compensator-AGD with SBC circuits are compared with the MPPT-$V_{pulse}$ with SBC and the parallelism of the SBC's switches. Based on the comparisons made, applying AGD directly

to $M_2$ switch gives the least best combination circuit for the SBC compared to others. This is because, regardless to the lowest output voltage and current produced, it actually degrades the performance of the converter since it produces higher output peak-to-peak ripple for both voltage and current for CCM and DCM.

However, since AGD can help reduce the $t_D$ of the $M_1$ and $M_2$, it gives smaller body diode conduction loss when it is compared with the CGD with SBC circuit. This is proven when the SBC conducts in DCM. So, AGD with SBC circuits works better during the DCM because it results in smaller output peak-to-peak ripple current and voltage, and also it has smaller body diode conduction loss. For the parallelism technique, it improves the SBC by reducing the output peak-to-peak ripple for both voltage and current by 1 %.

## 5.2 Recommendations

The suitable type of MOSFETs for the SBC switching must be selected in order to upgrade the SBC when operating in the self-driven mode. This is because, some drawbacks have been identified when AGD and compensator are applied to SBC. The SBC experiences the switching problem as mentioned in 4.1.4.1 and 4.1.4.2. Thus $M_1$ switch must be selected based on its electrical properties when operating in high switching frequency. Besides, investigation on the issue of $V_{ds1}$ and $V_{node}$ of the SBC has to be carried out thoroughly so that the cause can be determined. Despite of the SBC issue occurred in self-driven mode, having controllers implemented at $M_1$ and $M_2$ can eventually produce higher output voltage and current. So if the SBC requires higher current with a specific voltage at the load, it is recommended to apply this proposed SBC circuit with better feedback control scheme.

## REFERENCES


[1] N.Z. Yahaya K.M. Begam, M.Awan, 2010 "Analysis of Proposed High Frequency Resonant Gate Driver for A New Soft-switched SRBC circuit", PhD. Dissertation Department of Electrical and Electronic Engineering, Universiti Teknologi PETRONAS, Malaysia, June 2010

[2] Dr. Z Salam, Power Electronics and Drives (Version 2), 2002 "(Base/gate) Driver circuit" pp 32, 2002, available at : http://encon.fke.utm.my/notes/Introduction-2002.pdf

[3] Gate Drivers, (http://www.globalspec.com/learnmore/semiconductors/power_management_chips/gate_drivers), accessed on 22 October 2010

[4] S. Pan & P. K. Jain, "A New Resonant Gate Driver with Two Half Bridge Structures for Both Top Switch and Bottom Switch", *Queen's University Department of Electrical and Computer Engineering 19 Union Street, Kingston, On, Canada K7L3N6, Fellow, IEEE CHiL Semiconductor Corporation 1 Highwood Drive, Tewksbury*, pp 1-2, 2007.

[5] W. A. T. Eberle, "MOSFET Current Source Gate Drivers, Switching Loss Modelling and Frequency Dithering Control For MHz Switching Frequency DC-DC converters", PhD. Dissertation of Electrical and Computer Engineering, Queen's University, Kingston, Ontario, Canada, pp17, Feb 2008

[6] D. R. Sterk "Compact Isolated High Frequency DC/DC Converters Using Self-Driven Synchronous Rectification", M.S, thesis, Faculty of the Virginia Polytechnic Institute and State University, Blacksburg, Virginia Tech, December 17, 2003

[7] J. Zhou, M. Xu, Julu Sun, K. Yao and F. C. Lee, "1MHz Self-Driven DC-DC Converter for Non-Isolated 12V VRs", *Center for Power Electronics Systems The Bradley Department of Electrical and Computer Engineering, Virginia Polytechnic Institute and State University, Blacksburg, VA 24061, USA*, May 2004 .

[8] J. Klein, "Shoot-through" in Synchronous Buck Converters", *Fairchild Semiconductor, Application Report,* AN6003, 2003

[9] N. H. Ramlan, " Performance Analysis of Fixed Duty Ratio and Adaptive Gate Drive in High Frequency Gate Driver Design'', Bachelor dissertation, Department of Electrical and Electronic Engineering, Universiti Teknologi PETRONAS, Malaysia June 2009

[10] D. Mattingly "Designing Stable Compensation Networks for Single Phase Voltage Mode Buck Regulators", Intersil, Technical Brief December 2003. Available at: http://www.intersil.com/data/tb/tb417.pdf, December 2003

[11] A. Sattar, IXYS Corporation "DC to DC Synchronous Converter Design IXAN0068" , available at: http://www.ixyspower.com/images/technical_support/Application20Notes20By20Topic/Power20mosfets/IXAN0069.pdf, August 2008, pg 4, pg 2.

[12] M. S. Rahman "Buck Converter Design Issues", M.S thesis, Dept. Elect. Eng, Linköping Institute of Technology, Sweeden, July 2007.

[13] M.L. Chiang and L.C. Fu, "Adaptive Control of Switched Systems with Application to HVAC System," *Control Applications, 16th IEEE International Conference,* pp 367-372, 1-3 Oct. 2007

[14] Y. Nour , M. Orabi , A. Lotfi "Integrated ZVS POL Synchronous Buck Converter for Portable Applications," *APEARC, Aswan Faculty of Engineering, South Valley University, Aswan 81542 Egyp*, Enpirion Inc., 53 Frontage Road, Suite 210 Hampton, NJ 08827, USA, July 2010.

[15] M. El-Zanaty 1, M. Orabi 1, IEEE Member, M. Z. El-Sadek 2"Review of Synchronous Buck Converter Design Optimization",*1 APEARC, Aswan Faculty of Engineering, South Valley University, Aswan, Egypt, orabi@ieee.org2 Faculty of Engineering, Assuit University, Assuit, Egypt* , June 2008.

[16] I. Batarseh, Power Electronics Circuit, pp 132-138, John Wiley & Son, Inc, Wiley, United Stated, 1st Edition, 2004.

[17] Fundamental of Power Electronic, "Introduction to Discontinuous Conduction Mode (DCM)". Available at: http://ecee.colorado.edu/~pwrelect/book/slides/Ch5slide.pdf (accessed on 21st Sept 2010)

[18] P.Markowsk, "Estimating MOSFET Switching Losses Means Higher Performance Buck Converters", Available at : http://www.eetimes.com/electronics-news/4164421/Estimating-MOSFET-switching-losses-means-higher-performance-buck-converters (accessed on 12 March 2011)

[19] N.F.I Ahmad, "The Study and Evaluation of Output Parameters in SRBC", Bachelor Dissertation, Department of Electrical and Electronic Engineering, Universiti Teknologi PETRONAS, Malaysia, May 2011.

[20] L. K. Wong and T. K. Man, National Semiconductor , "Tip of the Week: How to best implement a synchronous buck converter" 26th April 2008. Available at : http://www.eetimes.com/design/power-management-design/4012225/Tip-of-the-Week-How-to-best-implement-a-synchronous-buck-converter. (access on 21 Sept 2010).

[21] IRFP250 ,*Fairchild Semiconductor datasheet,* January 2002.

[22] Zongqi HU & Dongsheng MA, "A Pseudo-CCM Buck Converter With Freewheel Switching Control", IEEE Technical Report, *Department of Electrical and Computer Engineering, University of Arizona, Tucson, Arizona 85721*, May 2005.

[23] *International IOR Rectifier* "How P-Channel MOSFETs Can Simplify Your Circuit", *Application Note* AN-940, March 2007.

[24] Vishay Siliconix, "P-Channel MOSFETs, the Best Choice for High-Side Switching". Available at: http://www.vishay.com/docs/70611/70611.pdf, December 2004 (access on 4th February 2011).

[25] IRFR 9212, *HEXFET Transistor P-Channel datasheet,* March 2008.

[26] N.A.Makthtar, "The Study of MOSFETs Parallelism & Effects on SRBC Circuit", Bachelor dissertation, Department of Electrical and Electronic Engineering, Universiti Teknologi PETRONAS, Malaysia, May 2011.

[27] A.A.A Abu Zamir. "The Study and Analysis of MPPT Controller for SRBC", Bachelor dissertation, Department of Electrical and Electronic Engineering, Universiti Teknologi PETRONAS, Malaysia, May 2011.

[28] H.Huang, "Loop Gain Digital Design",DCDC Technical White Paper, Astec Power, March 2005.

# APPENDICES

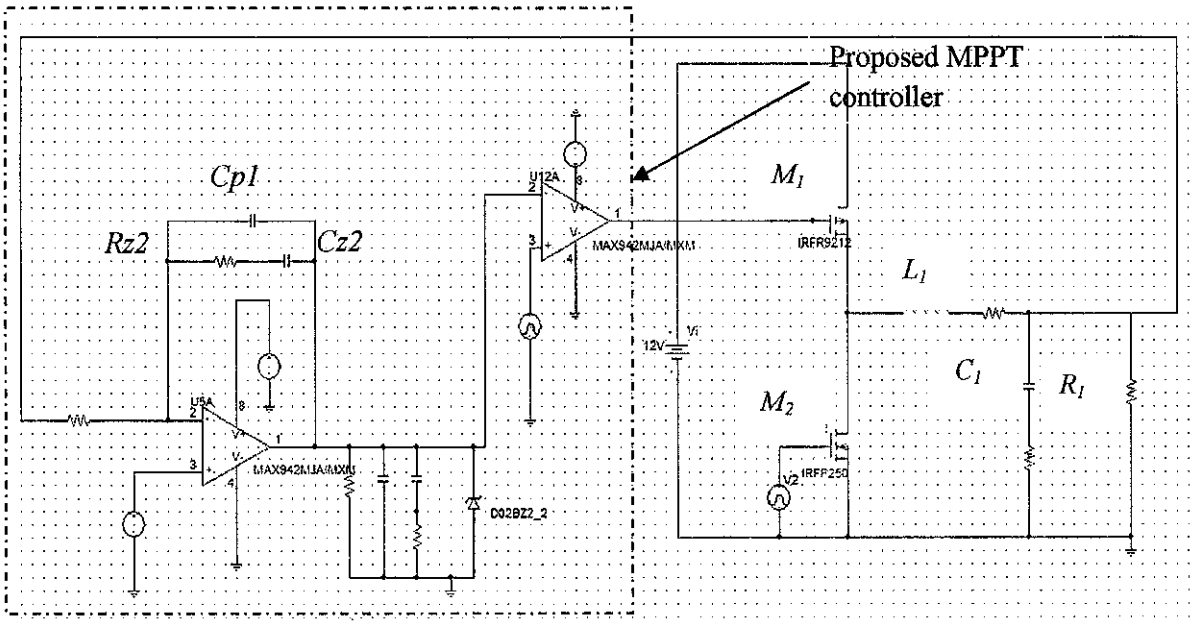
# APPENDIX A

Type III compensator MATLAB codes.

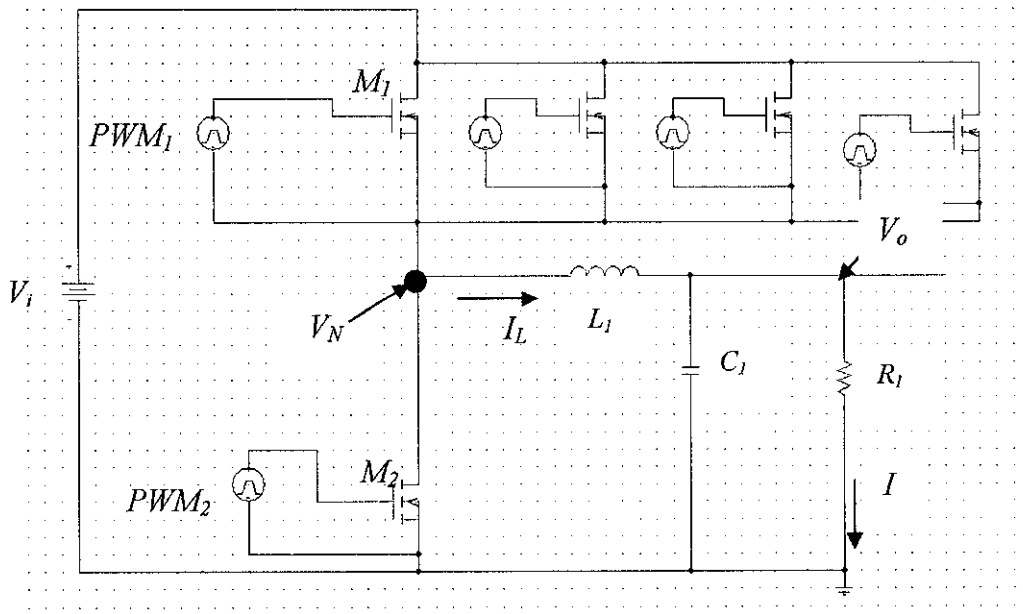
```
% Calculates all the values and plots all the graphs for a
Type III

% Compensation
function buck()

Vd = input(' Enter input voltage ');
Vo = input(' Enter output voltage ');
R =  input(' Enter the load ');
fsw = input(' Enter Switching Frequency in MHz ');
Ripple = input(' Enter allowed percentage ripple ');
fsw = fsw*1E6
deltaV = (Ripple/100)*Vo
DC = Vo/Vd;
C = input(' Enter value of Cin uF ' );
C = C*1E-6;
L = input (' Enter value of Lin uF ');
L = L*1E-6;
R1 = input(' Enter value of R1 (K) between 2 & 5 ');
R1 = R1*1E3;
rC = input(' Enter value of ESR ');
rL = input(' Enter value of DCR ');
DBW = 0.3*fsw
FESR = 1/(2*3.1415926535*rC*C)
FLC = 1/(2*3.1415926535*sqrt(L*C))
Rz2 = (DBW/FLC)*R1
Cz2 = 1/(3.14159*Rz2*FLC)
Cp1 = Cz2/((2*3.14159*Rz2*Cz2*FESR)-1)
Rz3 = R1/((fsw/(2*FLC))-1)
Cz3 = 1/(3.14159*Rz3*fsw)
s = tf('s');


% Transfer Function of Buck Converter
%G = Vd/Vr; % 1/Vr is the effect of PWM
N = 1+s*(rC*C);
D = 1+s*((L+((rC+rL)*R*C))/R)+(s^2)*(L*C);
Buck = N/D;
figure(1)
margin(Buck)
```

```
% transfer function of compensator
G1 = (R1+Rz3)/(R1*Rz3*Cp1);
N1 = s+(1/(Rz2*Cz2));
N2= s+(1/((R1+Rz3)*Cz3));
D0 = s;
D1 = s+((Cp1+Cz2)/(Rz2*Cp1*Cz2));
D2 = s+(1/(Rz3*Cz3));
Type3 = G1*((N1*N2)/(D0*D1*D2));
figure(2)
bode(Type3)
grid


%Total open loop transfer function of Buck Converter.
BuckType3 = Buck*Type3
figure(3)
margin(BuckType3)
grid
```

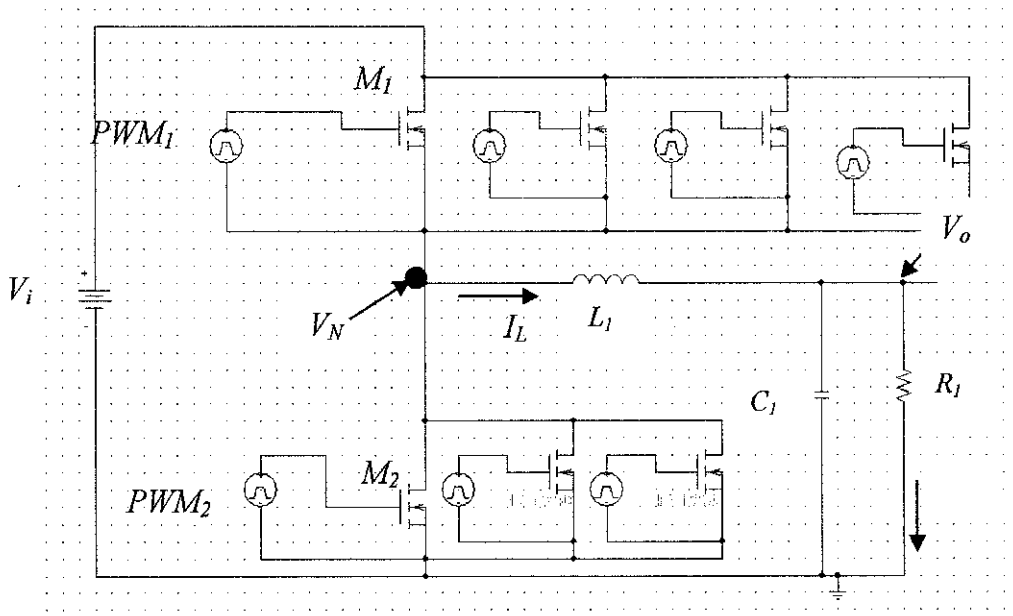
## APPENDIX B




MPPT- $R_1$ with SBC [27]




Parallelism CCM_$S_1$:4, $S_2$:1 [26]




Parallelism DCM_$S_1$:3, $S_2$:2 [26]

## APPENDIX C

## GANTT CHART FOR FINAL YEAR PROJECT 1

| No. | Detail/ Week | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | Selection and Confirmation of Project Title | | | | | | | | | | | | | | | | | | | | |
| 2 | Literature review of Continuous and Self driven gate driver | | | | | | | | | | | | | | | | | | | | |
| 3 | Submission of Preliminary Report | | | | | | | | MID | | | | | | | | | | | | |
| 4 | Circuit design I (Conventional gate driver and SBC) | | | | | | | | | | | | | | | | STUDY | | EXAM | | |
| 5 | Submission of Progress Report | | | | | | | | SEMESTER | | | | | | | | | | | | |
| 6 | Circuit Design II (Adaptive gate driver with SBC) | | | | | | | | | | | | | | | | WEEK | | WEEK | | |
| 7 | Literature review on compensator | | | | | | | | | | | | | | | | | | | | |
| 8 | Seminar | | | | | | | | | | | | | | | | | | | | |
| 9 | Circuit Design III (Type III Compensator and AGD with SBC) | | | | | | | | BREAK | | | | | | | | | | | | |
| 10 | Submission of Interim Draft Report | | | | | | | | | | | | | | | | | | | | |
| 11 | Submission of Interim Final Report | | | | | | | | | | | | | | | | | | | | |
| 12 | Oral Presentation | | | | | | | | | | | | | | | | | | | | |

## APPENDIX D

## GANTT CHART FOR FINAL YEAR PROJECT 2

| No. | Detail/ Week | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | Type III compensator designed | | | | | | | | | | | | | | | | | | | | |
| 2 | Results and discussions update part I (individual analysis) | | | | | | | | | | | | | | | | | | | | |
| 3 | Results and discussions update part II (common analysis) | | | | | | | | | | | | | | | | | | | | |
| 4 | Progress Report | | | | | | | | | | | | | | | | | | | | |
| 5 | Methodology update | | | | | | | | | | | | | | | | | | | | |
| 6 | Literature review update | | | | | | | | | | | | | | | | | | | | |
| 7 | Conclusion and recommendation update | | | | | | | | | | | | | | | | | | | | |
| 8 | Draft report | | | | | | | | | | | | | | | | | | | | |
| 9 | Final report and technical report (soft cover) | | | | | | | | | | | | | | | | | | | | |
| 10 | Viva | | | | | | | | | | | | | | | | | | | | |
| 11 | Final report (hard cover) | | | | | | | | | | | | | | | | | | | | |
| 12 | | | | | | | | | | | | | | | | | | | | | |

MID SEMESTER BREAK

STUDY WEEK

EXAM WEEK