125KHZ RFID READER DESIGN

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ELECTRICAL & ELECTRONICS ENGINEERING
UNIVERSITI TEKNOLOGI PETRONAS
JUNE 2010

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by

Fairoz Nadrah bte Mohd Ikhsan

Dissertation submitted
in partial fulfilment of the requirements for the
Bachelor of Engineering (Hons)
(Electrical and Electronics Engineering)

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CERTIFICATION OF APPROVAL

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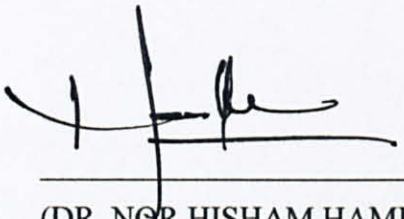

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Project Supervisor

UNIVERSITI TEKNOLOGI PETRONAS
TRONOH, PERAK
JUNE 2010

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

FAIROZ NADRAH BTE MOHD IKHSAN

ABSTRACT

Radio Frequency Identification (RFID) is an automatic identification method that can read, store, and retrieve data wirelessly. RFID systems are widely used in Universiti Teknologi PETRONAS (UTP) especially for lecturer's attendance, library as well as staff parking. The system is typically supplied by external vendors which can be very costly. The aim of this Final Year Project (FYP) is to develop a low cost RFID system to be an alternative to the expensive option. RFID system composed of RFID tags and reader. This project focuses on developing the RFID reader. There are four sub-blocks of RFID architecture namely, transmit stage, rectangular coil antenna, receiving section and microcontroller part. These sub-blocks are designed, simulated, build and tested. Each of these sub-blocks were successfully implemented and tested. These sub-blocks were then put together on a PCB for the full RFID reader implementation.

ACKNOWLEDGEMENTS

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LIST OF ABBREVIATIONS

AC	Alternating Current
DC	Direct Current
FSK	Frequency Shift Keying
FYP	Final Year Project
ID	Identification Number
HF	High Frequency
kHz	KiloHertz
LF	Low Frequency
PCB	Printed Circuit Board
RF	Radio Frequency
RFID	Radio Frequency Identification
UHF	Ultra High Frequency
UTP	Universiti Teknologi PETRONAS

CHAPTER 1

INTRODUCTION

1.1 Background Study

In recent years, the applications of Radio Frequency Identification (RFID) in many final year projects in UTP are very encouraging. There is average of six RFID application projects were developed every semester in Electrical and Electronics Engineering Department in UTP. The department spends thousands of Ringgit to buy the RFID reader for the application purpose but none of the FYP project is to develop their own reader.

The focus of this project is to design a low cost hardware part of a 125 kHz RFID reader which consists of designing the transmit stage, rectangular coil antenna, filters and programming a microcontroller. The reader can send RF signal to the tag, detect the data from a tag and then later send the data received from the tag to the host system.

RFID systems use radio frequency to identify, locate and track people, assets, and animals. Passive RFID systems are composed of three components: a reader, a passive tag, and a host computer [1]. A tag has an ID and a reader recognizes the information from the tag. The reader sends out a signal which supplies power to a tag. The tag transmits its ID to the reader and the reader consults an external database with received ID to recognize the information.

The tag is composed of an antenna coil and a silicon chip that includes basic modulation circuitry and non-volatile memory. The tag is energized by a time-varying electromagnetic RF wave that is transmitted by the reader. This RF signal is called a carrier signal. When the RF field passes through an antenna coil, there is an AC voltage generated across the coil. This voltage is rectified to supply power to the tag. The information stored in the tag is transmitted back to the reader. This is often called backscattering. By detecting the modulated signal, the information stored in the tag can be fully identified [2].

Data decoding for the received signal is accomplished using a microcontroller. The microcontroller is written in such a way to transmit the RF signal, decode the incoming data and communicate with the host computer. Typical, reader is a read only device [3]. RFID reader is a device that activates the tag and retrieves the information stored in its IC and then passes the data to a computer for processing.

RFID systems currently operate in the Low Frequency (LF), High Frequency (HF) and Ultrahigh Frequency (UHF) bands. The frequency used to design the RFID reader is a low frequency which is 125 kHz. Frequency refers to the size of the radio waves used to communicate between the RFID systems components [4]. Each frequency has advantages and disadvantages relative to its capabilities. Generally a lower frequency means a lower read range and slower data read rate, but increased capabilities for reading near or on metal or liquid surfaces.

1.2 Problem Statement

Normally, UTP will buy the RFID reader that is costly for any project or applications. University usually bought the reader that might cost around RM450 and above. This project will design RFID reader that can retrieve data from the passive tag and send the data to the host computer.

1.3 Objective

The main objectives of this project are:

(a) To design and develop a low cost RFID reader using a microcontroller (PIC16F877A) that capable of reading a 125 kHz RFID tag.
(b) To design a reader that can read the RFID tag numbers and transmit them to a host computer for data collection and storage

1.4 Scope of Study

The scope of study for this project consists of a few tasks and research that need to be conducted. However, the main scope of this project is the study of RFID focusing on designing the RFID reader part. The first stage of study is to know the theoretical background of the RFID reader design, the block diagram of the RFID reader, circuit design for each block and the expecting output for each block of circuit. Understanding on this theoretical knowledge will assist the student to work on the problem during the designing process. On top of that, the student needs to develop each block of circuit and must obtain the expected output. The successful of the reader design is depending on how the student manages to integrate each of the blocks of circuit to produce a working RFID reader.

CHAPTER 2

LITERATURE REVIEW AND THEORY

2.1 RFID Components

The purpose of an RFID system is to enable data to be transmitted by a portable device, called a tag, which is read by an RFID reader and processed according to the needs of a particular application [5].

Figure 1 shows a basic RFID system consists of three hardware components which are RFID tag, reader and host system. In general, a reader generates a radio frequency signal sends this signal to the tag. The reader also has a receiver that captures a reply signal from the tags and decodes the signal [6]. Upon receiving the reader's signal, the tag transmits its code to the reader. The data transmitted by the tag may provide information or specifics about the product tagged. The information is send to the host computer for application used.

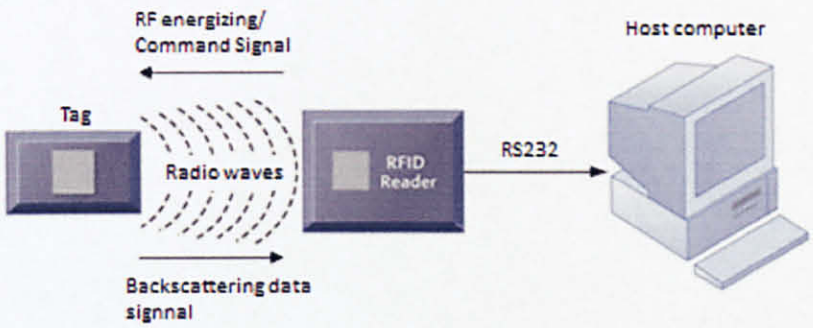


Figure 1: RFID basic components

2.1.1 RFID Tag

Tags are the heart of an RFID system, because they store the information that describes the object being tracked. Specific object information is stored in the memory of tags and is accessed via the radio signal of RFID readers [7].

Data is transferred between a tag and a reader via low-power radio waves, which are tuned to the same frequency. To obtain information from a tag, a reader must send a signal to the RFID tag, causing the tag to transmit its information to the reader. The transceiver then reads the signal, converts it to a digital format, and transmits it to a designated application such as an inventory management system [7].

Tags may be active or passive and read-only, write-once, or read-write. Below is a description of each:

(a) Passive Tags have no power source of their own and generally operate at a maximum distance of 3 meters or less, and have power only when in communication with an RFID reader [6].

(b) Active tags, with their own power source, can actively and intensively transmit and processing data, and over considerable physical distances. Active tags can communicate with readers 100 meters or more away. Active tags need much less signal from the RFID reader than passive tags require [6].

(c) Write-once tags enable a user to write data to the tag one time during production or distribution. This information can be a serial number or other data, such as a lot or batch number [7].

(d) Full read-write tags allow new data to be written to the tag as needed and written over the original data [7].

2.1.2 RFID Reader

RFID readers are devices that convert radio waves from RFID tags into a form that can be passed to the host computer. An RFID reader uses antennas to communicate with the RFID chip inside the RFID tag. Reader requirements vary depending on the type of task and application, and almost all applications will require multiple forms of readers to make a successful system [7]. The full architecture of RFID reader is shown in figure 6 and the full system is discussed in detail in this report.

2.1.3 Host Computer

The data acquired by the readers is then passed to a host computer, which may run specialist RFID software or middleware to filter the data and route it to the correct application and to be processed into useful information.

2.2 Signal Waveform

Figure 2 below shows a general RFID system together with the signal waveform of the system. The 125 kHz carrier signal is generated from the microcontroller. When the carrier signal passes through an antenna coil, there is an AC voltage generated across the coil. This voltage is rectified to supply power to the tag. The information stored in the tag is transmitted back to the reader. This is often called backscattering. By detecting the FSK modulated signal, the information stored in the tag can be identified. [2].

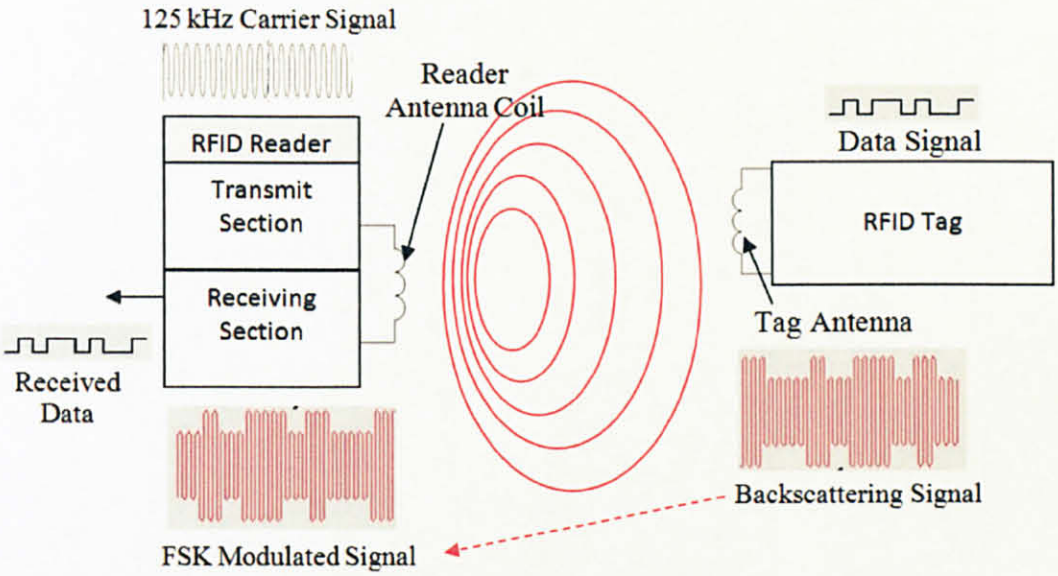


Figure 2: RFID System Signal Waveform

2.2.1 Carrier Signal

Carrier signal is the transmitting radio frequency of reader. This RF carrier signal provides energy to the tag device, and is used to detect modulation data from the tag using backscattering. In this project, carrier frequency generated is 125 kHz as shown in figure 3. The 125 kHz carrier signal is generated by dividing a 4 MHz crystal oscillator signal. The carrier signal is amplified before fed into antenna tuning circuit [2].

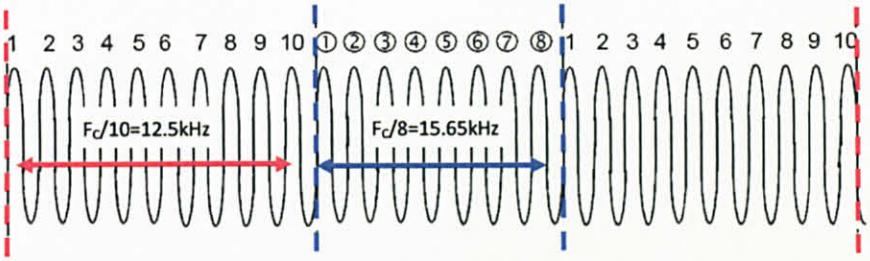


Figure 3: 125 kHz Carrier Signal

2.2.2 Backscattering Modulation

Backscattering terminology refers to the communication method used by a passive RFID tag to send data back to the reader. This backscattering-modulation loading of the reader's transmitted field provides a communication path back to the reader. RFID tags using backscatter technology reflect back to the reader radio waves from a reader, usually at the same carrier frequency. The reflected signal is modulated to transmit data. The data bits can then be encoded or further modulated using FSK modulation [8].

2.2.3FSK Modulated Signal

The passive RFID tag uses backscattering of the carrier frequency for sending data from the tag to reader. Although all the data is transferred to the host by backscatter modulation the carrier, the actual modulation of 1's and 0's is accomplished by FSK Modulation Method [9].

Modulation is the process of varying the RF carrier in some manner as a means of conveying information. The common modulation type for the RFID tag is FSK. As shown in figure 4, The FSK modulation uses two different frequencies for data transfer which represent a '0' and a '1'. A '0' and a '1' are represented by $F_C/8$ and $F_C/10$, respectively. F_C is the carrier frequency. The amplitude modulation of the 125kHz carrier thus switches from 125kHz/8=15.65kHz to 125kHz/10=12.5kHz corresponding to 0's and 1's in the bit stream, and the reader has only to count cycles between the peak-detected clock edges to decode the data. FSK allows for a simple reader design, provides

very strong noise immunity, but suffers from a lower data rate than some other forms of data modulation [2].

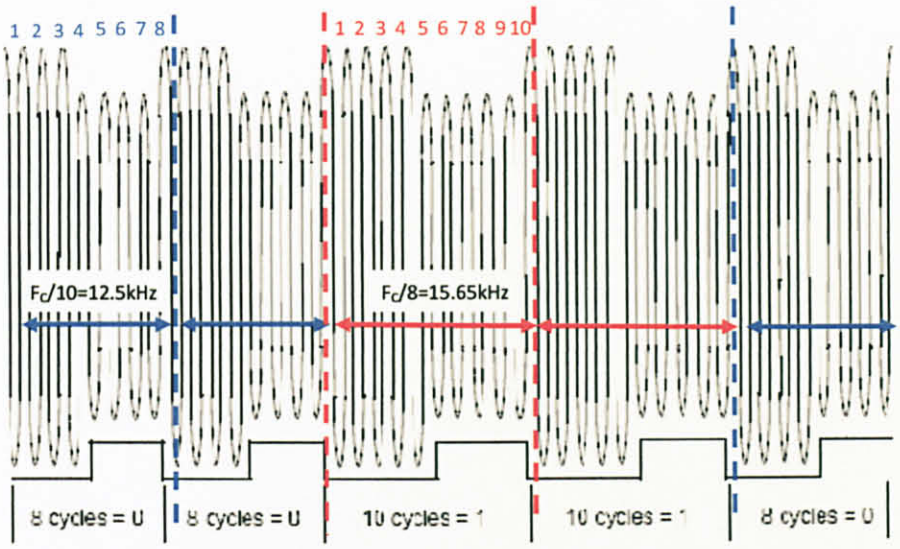


Figure 4: FSK Modulated Signal [2]

2.2.4 Data Signal

Figure 5: Data Signal

A data signal stores in the tag is a binary data signal. The longer data period remains high between pulses represents a binary-1 and a short data period represents a binary-0 as shown in the figure 5. Computers can interpret these digits as digital information. The data in the tag is later displayed at the host computer.

2.3 RFID Reader Architecture

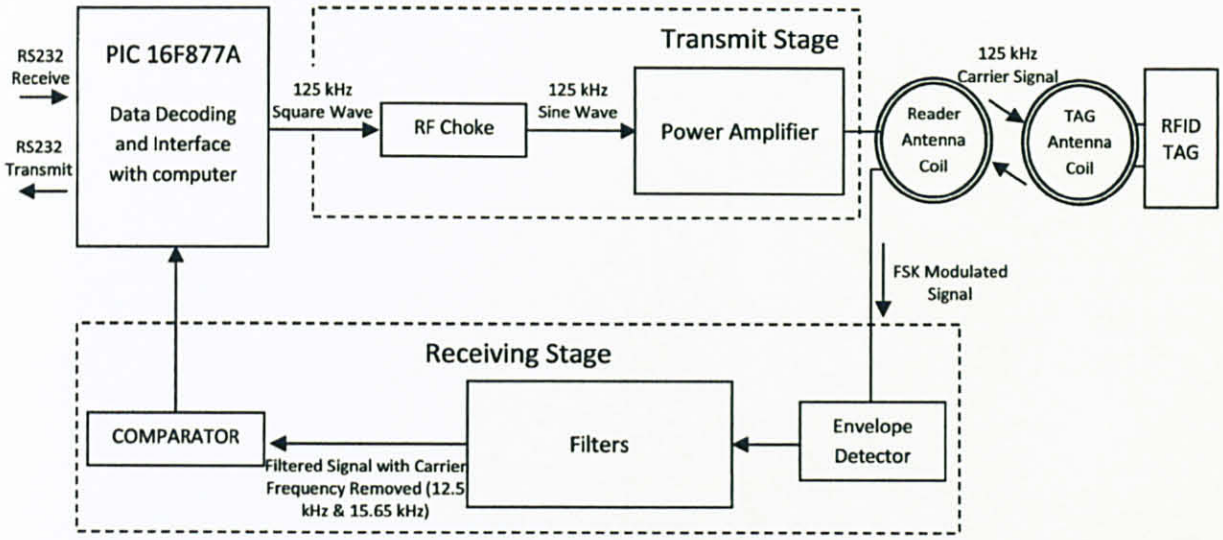


Figure 6: RFID reader block diagram

Figure 6 shows RFID reader block diagram. The RFID reader consists of transmitting section, receiving section and an antenna. It transmits a carrier signal, receives the backscattering signal, and performs the data processing [2]. The job of the reader circuit is to sends out a signal which supplies power to a tag, retrieve the data stored in the tag and display the data to the host computer. In order to interpret the data, the carrier frequency must be removed, and the enveloping frequencies must be magnified into something measureable.

2.4 Transmit Stage

A transmit stage consists of an RF choke followed by a current buffer and half-bridge amplifier. These transmit stage removes high frequency components from the input square wave to create a sine wave. The voltage and current are then amplified to drive the antenna through the power amplifier.

2.4.1 RF Choke

Chokes are fixed inductors primarily intended to "choke" off alternating currents, including RF from DC supply lines. The RF choke is designed to have high impedance over a large range of frequencies.

In the RFID reader design, RF choke is used to filter out the upper harmonic frequencies found in the square wave, leaving the fundamental frequency, 125 kHz, as a sine wave to be amplified.

2.4.2 Current Buffer

A buffer amplifier is one that provides electrical impedance transformation from one circuit to another. Two main types of buffer exist: the voltage buffer and the current buffer.

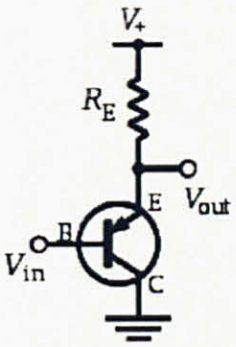


Figure 7: PNP Current Buffer

Typically a current buffer amplifier is used to transfer a current from a first circuit, having a low output impedance level, to a second circuit with a high input impedance level. The interposed buffer amplifier prevents the second circuit from loading the first circuit unacceptably and interfering with its desired operation [10].

2.4.3 Half-Bridge Amplifier

RF signals received by antennas are often very weak. Power amplifiers are widely used in RF transmission systems to increase the signal strength of the received signal. An RF power amplifier is a type of electronic amplifier used to convert a low-power radio-frequency signal into a larger signal of significant power, typically for driving the antenna of a transmitter.

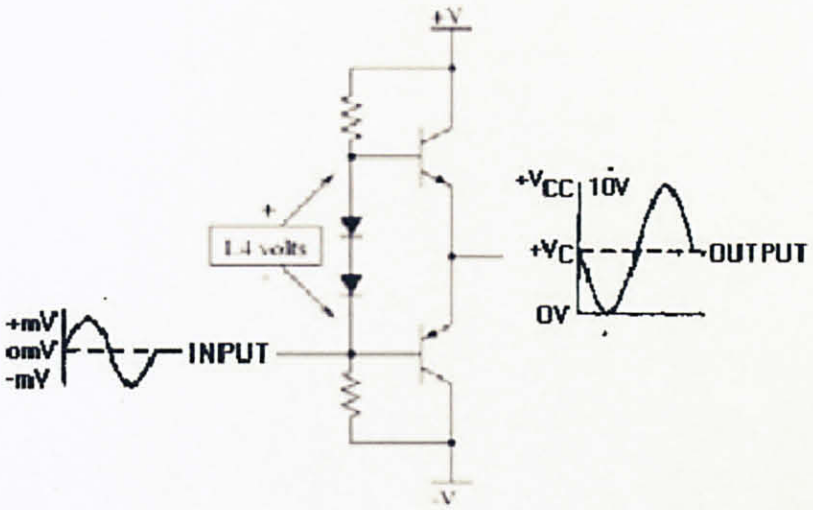


Figure 8: Half Bridge Power Amplifier

Figure 8 shows the half-bridge power amplifier circuit. The half-bridge power amplifiers use two transistors. Each transistor is turned on for half of the time. One transistor operates during the positive cycle of the input, while the other is used for the negative cycle. Therefore in theory, both are never on at the same time. When there is no input, both transistors are turned off and no power appears at the output. For this reason, efficiency is good. However, due to the fact that transistors take some time to turn on, there is a moment when no power appears at the output. This powerless region is called the crossover region. The performance is improved by the addition of two diodes that eliminate the crossover region and allows both transistors to be turned on at the same time [11]. This power amplifier has very good efficiency and good accuracy too.

2.5 Reader Antenna Coil

Passive RFID tags work in such a way that they are actually powered by an external signal, which, in most cases is the carrier signal from the reader circuit. The reader and tag communicate using magnetic coupling since their respective antennas can sense changes in magnetic field, which is observed as a change in voltage in the reader circuit [3].

One of the limiting factors in low frequency passive RFID is reading distance. Maximum reading distance is determined by frequency, power and signal interference. Typical reading distance for RFID is only a few centimeters. Because increasing power and frequency is not always practical, a common solution to increase reading distance is modify antenna being used.

Figure 9 shows a series resonant circuit that consists of the antenna coil and a capacitor. The series resonant circuit results in minimum impedance at the resonance frequency. Therefore, it draws a maximum current at the resonance frequency. Because of its simple circuit topology and relatively low cost, this type of antenna circuit is suitable for proximity reader antenna [2]. Generally, RF antenna is a series resonance circuit of inductance (L) and capacitor (C). The relation of component L and C is [1]:

$$f = \frac{1}{2\pi\sqrt{LC}}$$

f = resonate frequency (Hertz)
L = inductance (Henries)
C = Capacitance (Farad)

An oscilloscope can be used to examine how the LC circuit responds to the frequency produce by sine wave generator. The peak response will be at the frequency of natural resonance of the circuit.

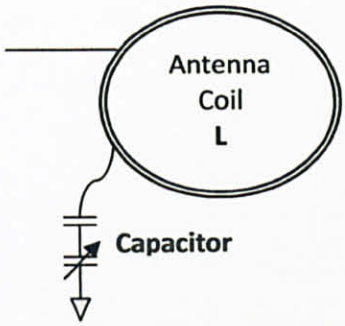


Figure 9: Antenna Series Resonant Circuit Topology

The magnetic induction type antenna used for low frequency RFID is constructed from multiple turns of magnetic core in a loop. The inductance of antenna coil is dependent on shape, size and the number of turns in the antenna coil [12]. To construct an antenna with the necessary inductance, a coil of copper wire is used. Inductance of a multilayer rectangular coil is determined by the following equation:

$$L = \frac{0.0276[(x + y + 2h)N]^2}{1.908(x + y + 2h) + 9b + 10h}$$

[13]

L = inductance (μH)

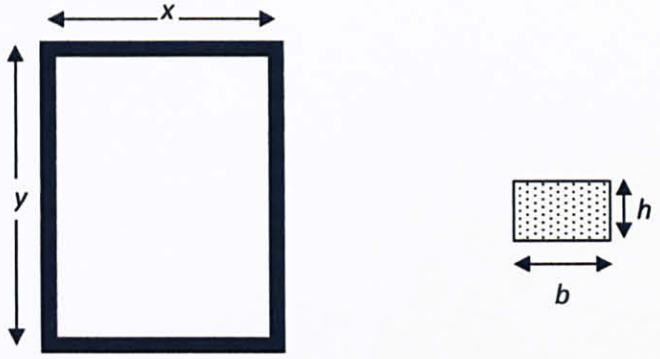
x = width of the coil (cm)

y = length of the coil (cm)

h = height of cross section (cm)

b = width across the conducting part of the coil (cm)

N = number of turns



(a) top view (b) cross sectional view

Figure 10: N-turn Square Loop coil with Multilayer

The factor of selecting the shape of the antenna as it proved that the rectangular-shaped coil antenna has better resonant than the circular-shaped coil antenna [13].

2.6 Detector

In order to detect the information that being sent by the RF signals, it needs two steps for a full recovery of the data. The first step is demodulating the signal, and the second step is detecting the frequency or period of the demodulation signal. The demodulation is accomplished by detecting the envelope of the modulated signal. Figure 11 shows a simplified model of an envelope detector. A half-wave capacitor-filtered rectifier circuit is used for the demodulation process. A diode detects the peak voltage of the signal. The voltage is then fed into an RC filter circuit [2].

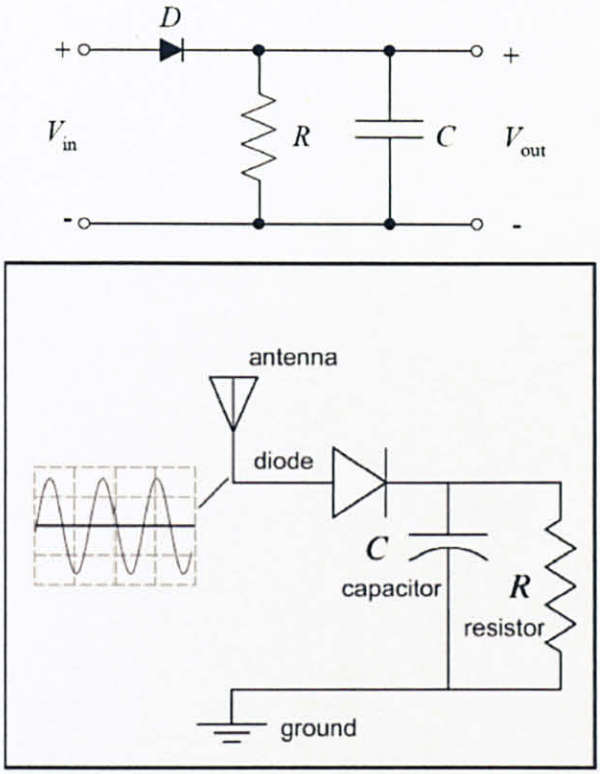


Figure 11: Envelope Detector

2.7 Filtering Stage

Filters are essential components in any electrical systems. In the RFID reader, filters are required to remove undesired signals at different stages of the receiving process, such as noise from incoming signals the antenna receives, undesired signals at the image frequency, and harmonics after the mixing operation. All analogue filters fall in one of two categories: passive or active. In this low frequency RFID system, active filters are used because of the following advantages [6]:

- Active filter can generate gain larger than one.
- Higher order filters can easily be cascaded since each Op-amp can be second order.
- Filters are small in size as long as no inductors are used, which make it very useful as integrated circuit.

A pair of active Twin-T filters and an active Butterworth filter is design as the gain element. An active band-pass filter is used for the RFID system to reject all signals outside the (10-20) kHz signals and to amplify the low antenna signal. These are because the ID signals from the tag are 12.5 kHz and 15.65 kHz and signal power is very low [14].

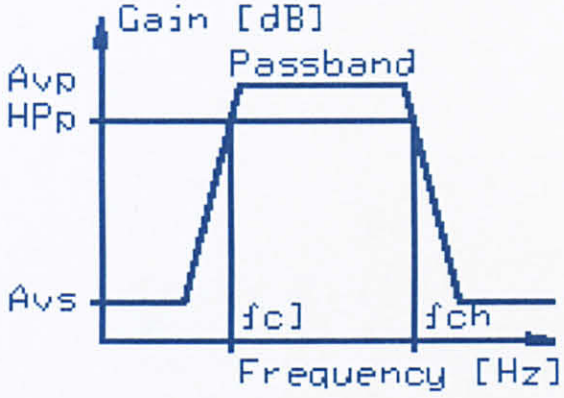


Figure 12: Frequency Response for Bandpass Filter

Avp = attenuation in passband

Avs = attenuation in stopband

HPp = Half-Power point (0.707 of voltage)

fcl = low cutoff frequency

fch = high cutoff frequency

Bandpass filters are called into action to pass a range of frequencies only. Figure 12 shows a frequency respond for a bandpass filter. There are few ways describe the filter shape:

(a) **Center frequency, fo.** The center of the band, typically the peak of the frequency response curve.

(b) **Bandwidth, BW = f_H - f_L.** The upper and lower frequencies, f_H and f_L, are defined as the frequencies where the gain has dropped to 0.707 of the mid-band gain.

(c) **Quality factor, Q = fo / BW.** The Q tells about the width of the pass-band: Low Q → Wide bandwidth; High Q → Narrow bandwidth.

(d) **Mid-band Gain, H = Vo / Vin.** This is voltage gain at the center frequency fo.

2.7.1 Twin t Active Filter

A Twin T Filter is a two pole filter topology. Figure 13 illustrates a circuit diagram for an active twin t filter. In the twin-T band-pass filter, the signal is first amplified, and then split. One part of the signal passes through a second, variable amplifier, and the second part passes through the twin-T notch filter. The two signals are then recombined in a differential amplifier. In this way, the sharp attenuation properties of the twin-T notch filter create a sharp spike filter.

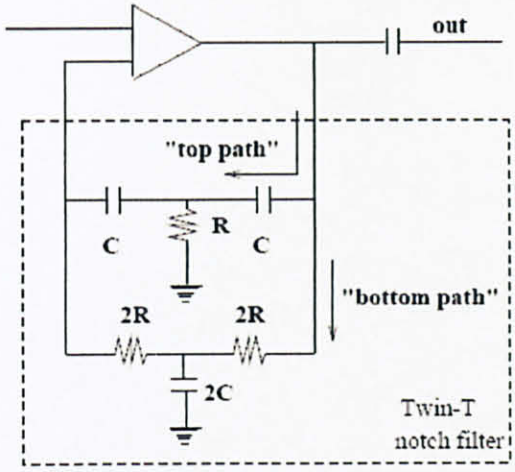


Figure 13: Active Twin t Filter

2.7.2 Butterworth Active Filter

The most common filter responses are the Butterworth, Chebyshev, and Bessel types. Among these responses, Butterworth type is used to get a maximally-flat response. Also, it exhibits a nearly flat pass band with no ripple. Butterworth filter is chosen because of its simplicity compared to other known architectures such as multiple feedback and state variable, where the latter is for precision performance [14].

Butterworth filter response is used to get the maximum flat gain. The Active - RC Butterworth filters have a range of advantages when used for lower order of the filter: have excellent linearity, have low power dissipation and are easy to design and analyze [14]. Figure 14 is the Butterworth active filter circuit diagram.

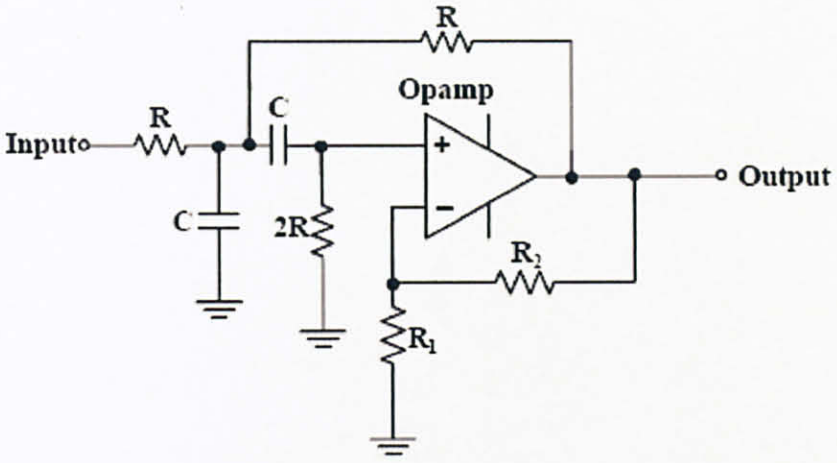


Figure 14: 2nd Order Butterwort Band-pass Active Filter

2.8 Comparator

Figure 15 is the comparator circuit. Comparator implies these circuits are used to compare two voltages. When one is higher than the other the comparator circuit output is in one state, and when the input conditions are reversed, then the comparator output switches to the other state. Comparator generates a nice inverted square wave from the filter output before going into the PIC16F877A microcontroller.

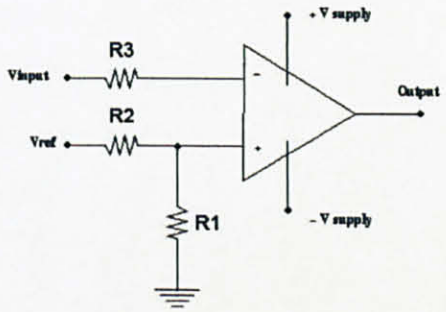


Figure 15: Comparator Circuit

2.9 Microcontroller

The PIC16F877A microcontroller performs data decoding for the receiving signal. The microcontroller is written in such a way to transmit the RF signal, decode the incoming data and communicate with the host computer via RS232 serial interface.

A PIC16F877A microcontroller is used in the RFID reader design. This microcontroller is a compact standalone computer, optimized for control application. Entire processor, memory and the I/O interfaces are located on a single piece of silicon so, it takes less time to read and write to external devices.

PIC16F877A is one of the most commonly used microcontrollers especially in automotive, industrial, appliances and consumer applications.

Following are the reason why microcontrollers are incorporated in control system:

(a) Cost: Microcontrollers with the supplementary circuit components are much cheaper than a computer with an analogue and digital I/O.
(b) Size and Weight: Microcontrollers are compact and light compared to computers.
(c) Simple applications: If the application requires very few number of I/O and the code is relatively small, which do not require extended amount of memory and a simple LCD display is sufficient as a user interface, a microcontroller would be suitable for this application.
(d) Reliability: Since the architecture is much simpler than a computer it is less likely to fail.
(e) Speed: All the components on the microcontroller are located on a single piece of silicon. Hence, the applications run much faster than it does on a computer.

Figure 16 shows the output pin assign to the PIC16F877A.

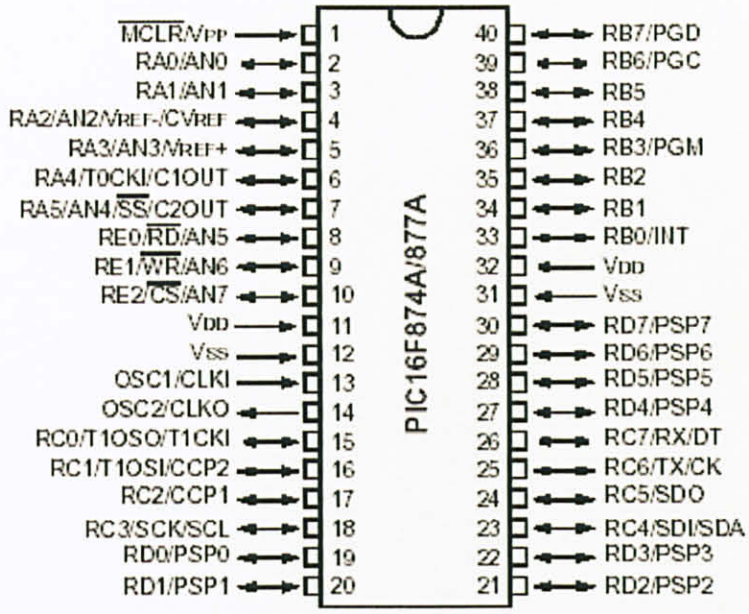


Figure 16: PIC16F877A Pin-Outs

CHAPTER 3

METHODOLOGY

3.1 Procedure Identification

Several structured procedure are performed in order to complete this particular project. The methodology of the project is split down into two parts. The section sequence as shown in figure 17 below:

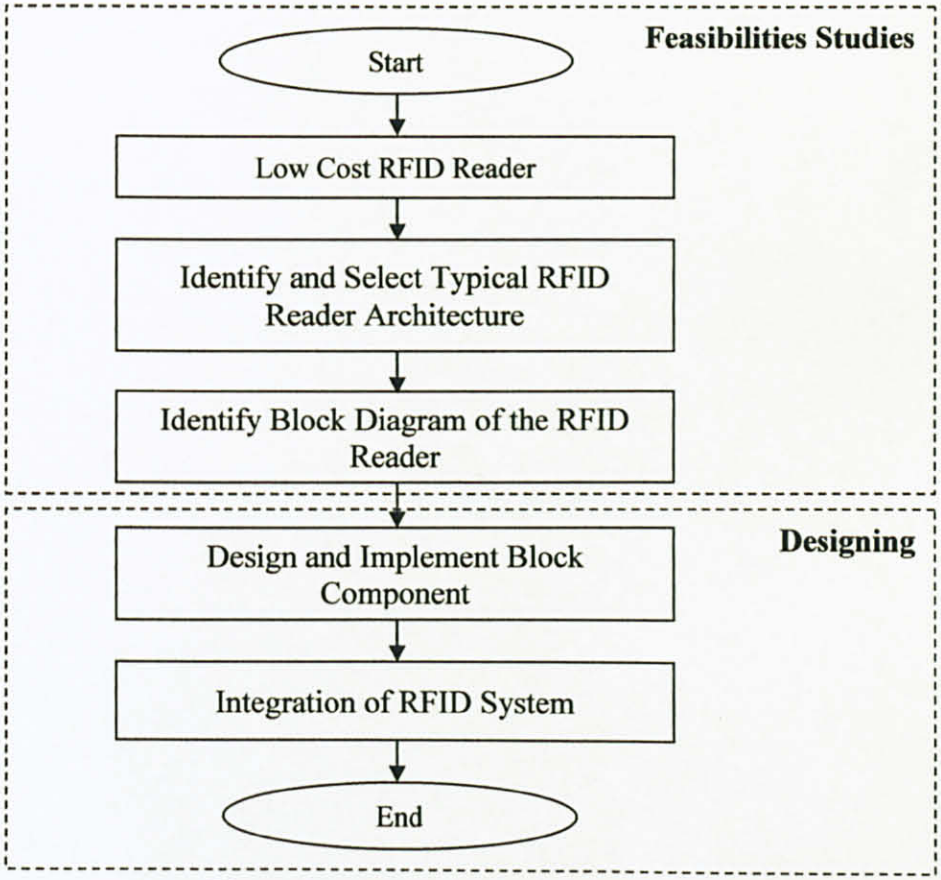


Figure 17: Project Methodology

3.2 Feasibilities Studies

3.2.1 Identify and Select RFID Reader Architecture

In order to identify and select the RFID reader architecture, a various type of research has been done. A research also defines what the activity of research is, how to proceed, how to measure progress, and what constitutes success. For the purpose of this project, the research type included:

a) Full articles and journals of a variety RFID reader design
b) Reading the title and abstract of each citation and reviewing the key word list.
c) Scanning the abstract for methods/ tools used for RFID reader design that being applied

An RFID system is differentiated based on the frequency range it uses. Low-frequency RFID systems are typically 125 KHz. This frequency band provides a shorter read range and slower read speed than the higher frequencies. Low-frequency systems have short reading ranges and lower system costs. The frequency bands must be selected carefully for applications because each one has its own advantages and disadvantages. The frequency used to design the RFID reader project is 125 kHz.

3.2.2 Identify Block Diagram

The block diagram in figure 18 shows a connection between all elements in the RFID reader. The main objective in this stage is to clearly show how the elements and the components in the RFID reader related to each other and also to describe the function of all elements and components involved. Figure 8 shows the block diagram of the RFID reader.

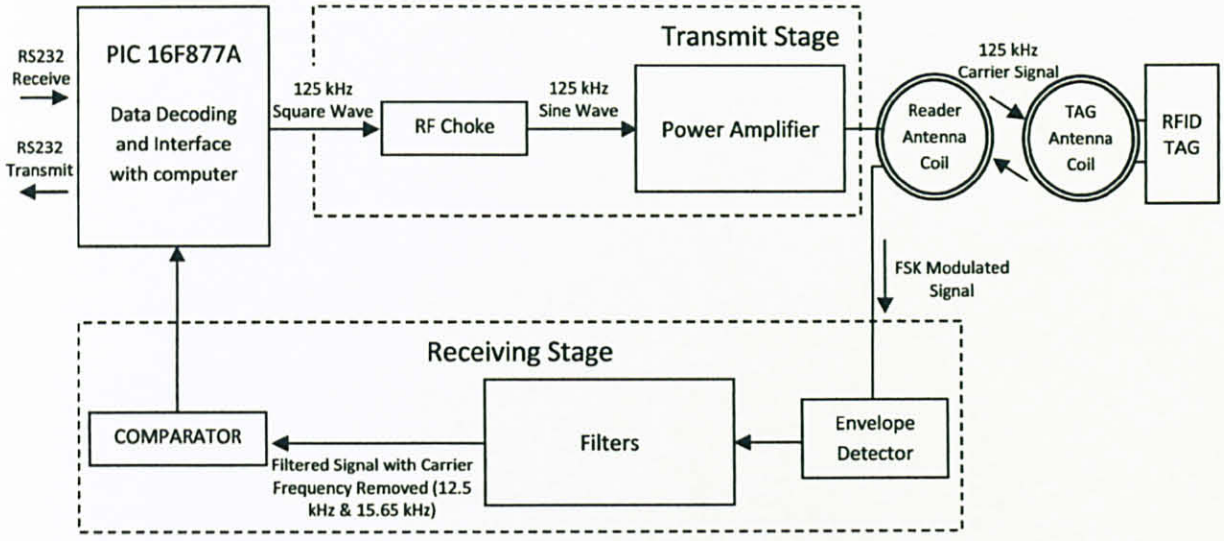


Figure 18: RFID reader block diagram

The transmitting section contains circuitry far a carrier signal (125 kHz), RF choke, and power amplifiers. The 125 kHz carrier signal is typically generated by dividing a 4 MHz crystal oscillator signal. The signal is amplified before it is fed into the antenna coil. A power amplifier circuit is used to boost the transmitting signal level [2].

An antenna impedance tuning circuit consisting of capacitors is used to maximize the signal level at the carrier frequency. This tuning circuit is also needed to form an exact LC resonant circuit for the carrier signal [2].

On the receiving end, the signal is first half-wave rectified, and is then fed through a half-wave R-C filter to help knock out most of the 125 KHz carrier and detect the envelope signal. This signal is then bandpass filtered using a series a Twin-T active bandpass filters, and lowpass filtered with an active Butterworth filter to further decrease gain in frequencies outside of the 10-20 KHz area and increase gain of the envelope signals such that it saturates the op-amps of the filters. As a final stage the signal is put through a comparator and resistive divider to produce a nice square wave at logic levels [15].

The microcontroller is written in such a way to transmit the RF signal, decode the incoming data and communicate with the host computer via RS232 serial interface.

3.3 Designing

Based on research done, the basic concept of the project has been acquired. From the theory, concept, design architecture and improvement methods, the draft circuit of the project has been designed. The design process has considered all the requirements needed so that the circuits assured to meet the project objective. The draft circuit then will be simulated using PSPICE to check its performances.

From the designated circuit, the project moves to the next phase which is the integration of the RFID reader system.

3.3.1 Detailed Designing Work Flow

Figure 19 shown the detailed of the project flow involved in the designing stage:

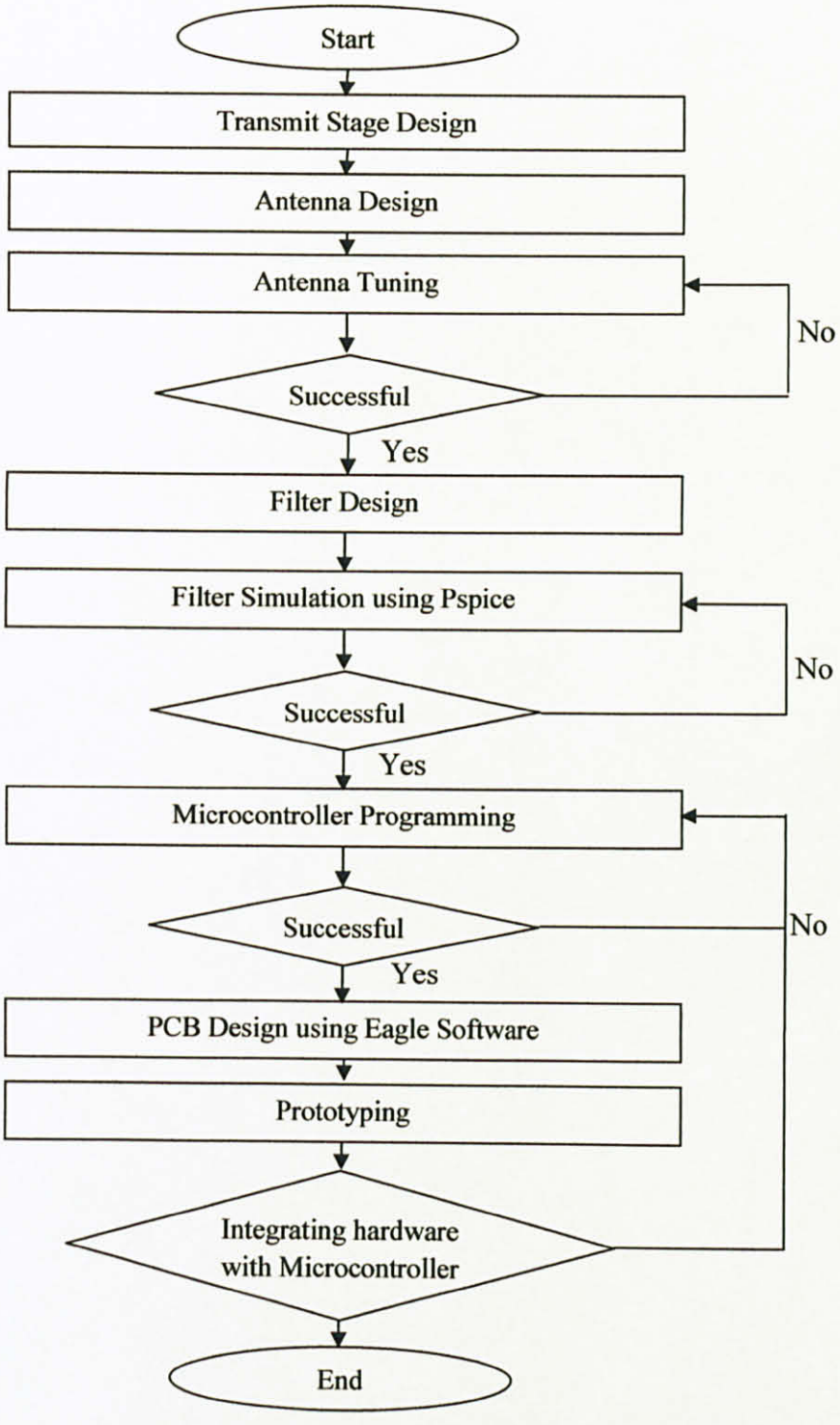


Figure 19: RFID Reader Detailed Design

CHAPTER 4

RESULT AND DISCUSSION

4.1 Transmit Stage

The circuit of Figure 20 is an RF choke followed by a current buffer and half-bridge amplifier. The RF choke is used to filter out the upper harmonic frequencies found in the square wave output from the microcontroller, leaving the fundamental frequency, 125 KHz, as a sine wave to be amplified. The square wave generator is used to test the circuit which actuality, the output from the microcontroller and a set of inverters to ramp up the current. The voltage and current are then amplified to drive the antenna. In the RFID reader design 2N3904 and 2N3906 NPN and PNP BJT transistors are used for the transmit stage since they were cheap and convenient.

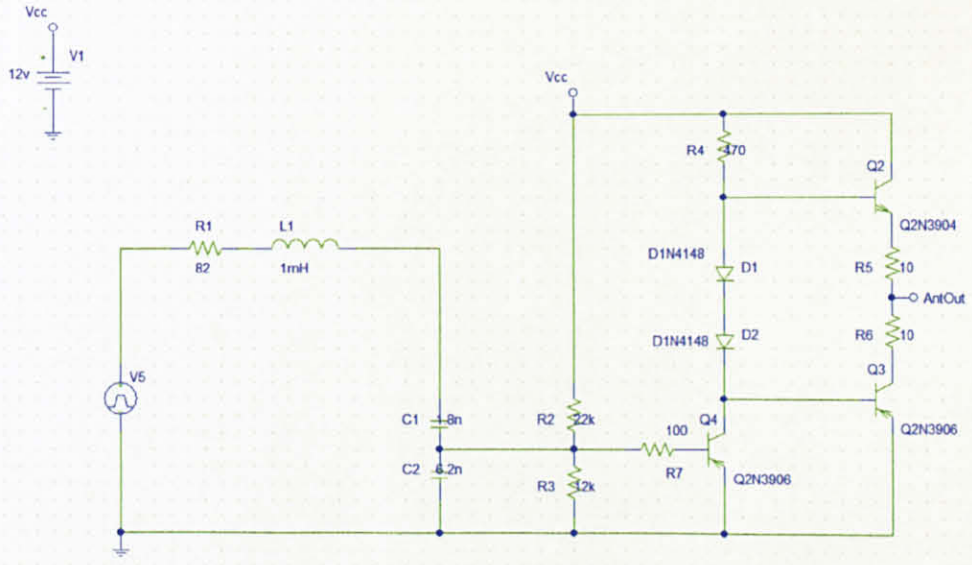


Figure 20: Circuit Diagram for Transmit Stage

Figure 21 illustrates an oscilloscope reading for 125 kHz square wave from a function generator used to test the transmit stage circuit which actuality in the real RFID reader, the square wave output is coming from the microcontroller.

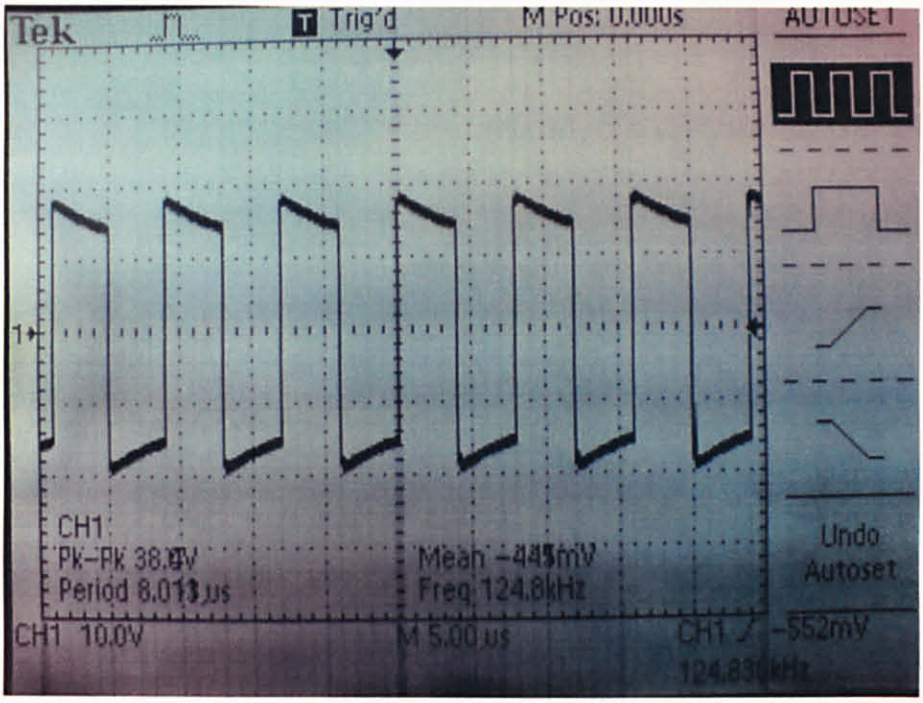


Figure 21: 125 kHz Input Square Wave

Figure 22 shows that 125 kHz of sine wave after the square wave passing through the RF choke. It is proven that RF choke is used to filter out the upper harmonic frequencies found in the square wave output from the function generator, and give the output of 125 KHz sine wave. The peak to peak voltage for the signal is 15.2 Volt. Later, the 125 kHz sine wave will be amplified through the amplifier.

The signal waveform in figure 23 illustrate that the signal is being amplified after passing through the current buffer and half bridge amplifier. The voltage and current is amplified to drive the antenna. The peak to peak voltage is 38Volt which is higher than the fundamental sine wave signal. The addition of two diodes proven to eliminate the crossover region and allows both transistors

to be turned on at the same time [11]. This power amplifier has very good efficiency and good accuracy too.

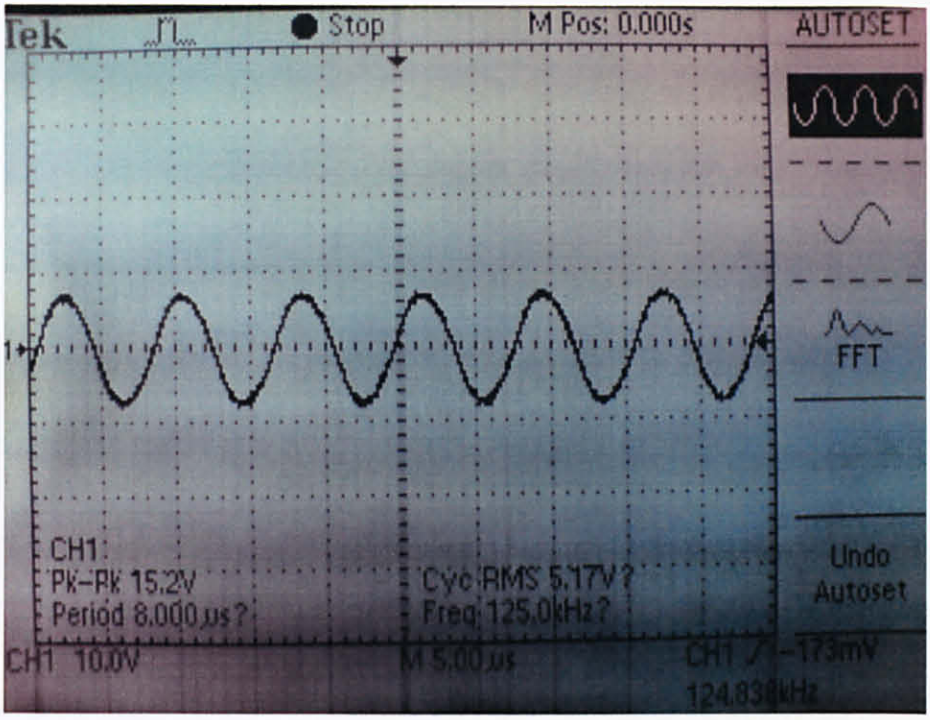


Figure 22: 125 kHz Fundamental Frequency Sine Wave

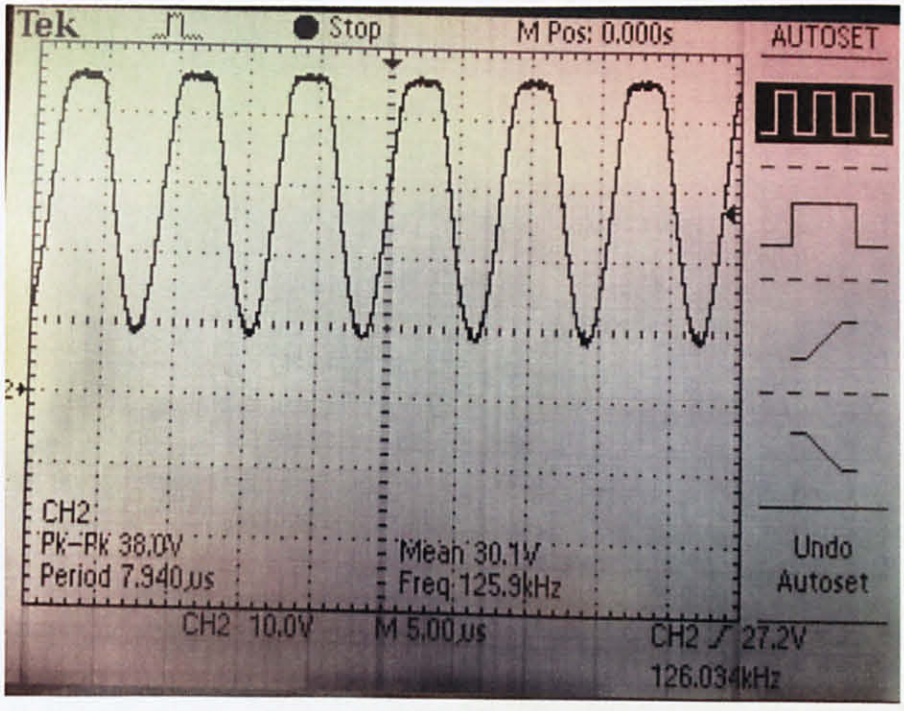


Figure 23: Amplified Signal

4.2 Resonant Antenna Design

In a RFID system, operating frequency is fixed, consequently the resonant frequency is fixed [16] which are 125 kHz. In order to be able to calculate roughly the inductance L of the coil, it is necessary to estimate the capacitance C of the circuit. The capacitance is determined and the estimated value of the coil capacitance is 1000pF. As a result, inductance L is:

$$L = \frac{1}{(2\pi f)^2 C}$$

$$L = \frac{1}{[2\pi(125k)]^2 C}$$

$$\boldsymbol{L = 1.62\ mH}$$

The numbers of turns for the rectangular coil with the width of the coil, x is 7cm and length, y of the coil are 13.8cm and the thickness, h is 0.3cm. The inductance value used is 1.62mH and below is the estimated number of turns for the rectangular coil antenna:

$$N = \frac{\sqrt{\frac{L[1.908(x+y+2h)+9b+10h]}{0.0276}}}{(x+y+2h)}$$

$$N = \frac{\sqrt{\frac{1620[1.908(7+13.8+2(1))+9(0.3)+10(1)]}{0.0276}}}{(7+13.8+2(1))}$$

$$\boldsymbol{N = 80\ turns}$$

The number of turns out to be 80 turns and finished coil is extracted and secured with tape which shown in figure 24.

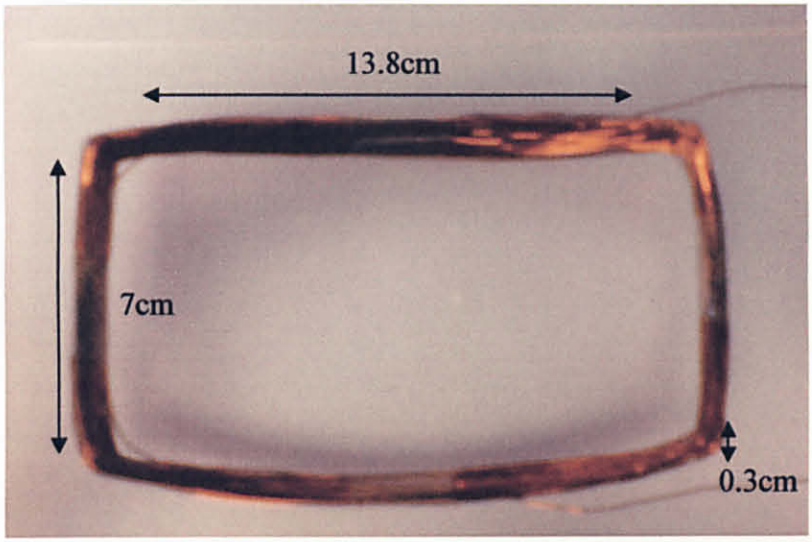


Figure 24: Rectangular coil antenna

To fine tune the resonant frequency of the entire system is simply by changing the capacitance value until the oscilloscope displayed the highest resonant voltage from the carrier frequency. Figure 25 illustrates the result obtains from the oscilloscope for the resonant voltage after tuning the antenna. From the oscilloscope, observed that capacitance value of 1000pF gives the highest resonant voltage.

An antenna coil with a 1.62mH inductance and a resonant capacitor 1000 pF form a series resonant circuit for a 125 kHz resonance frequency. Since the capacitor is grounded, the carrier signal 125 kHz is filtered out to ground after passing the antenna coil. The circuit provides minimum impedance at the resonance frequency. This result in maximizing the antenna current, and therefore, the magnetic field strength is maximized [1].

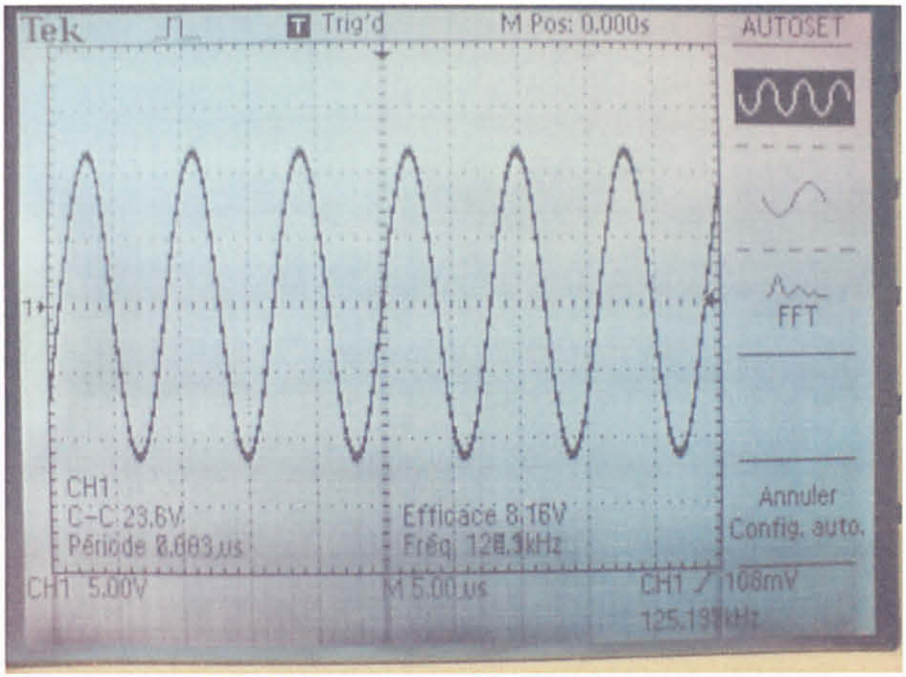


Figure 25: Resonant voltage for 1000pF capacitance

4.3 Filtering Stage

Once signal leaves detector, it passes through a set of filters which a pair of active Twin-T filters and an active Butterworth filter with the TL084 OpAmp as the gain element. The circuit diagram for the filters is in the figure26.

For Twin T and Butterworth Active Filter, the parameters below are used to design both filters:

Pass Band Frequency = 10 kHz-20 kHz

Mid Frequency, f_o = 15 kHz

Bandwidth, BW = $f_H - f_L$ = 10 kHz

Quality Factor, Q = 1.5/10 =1.5

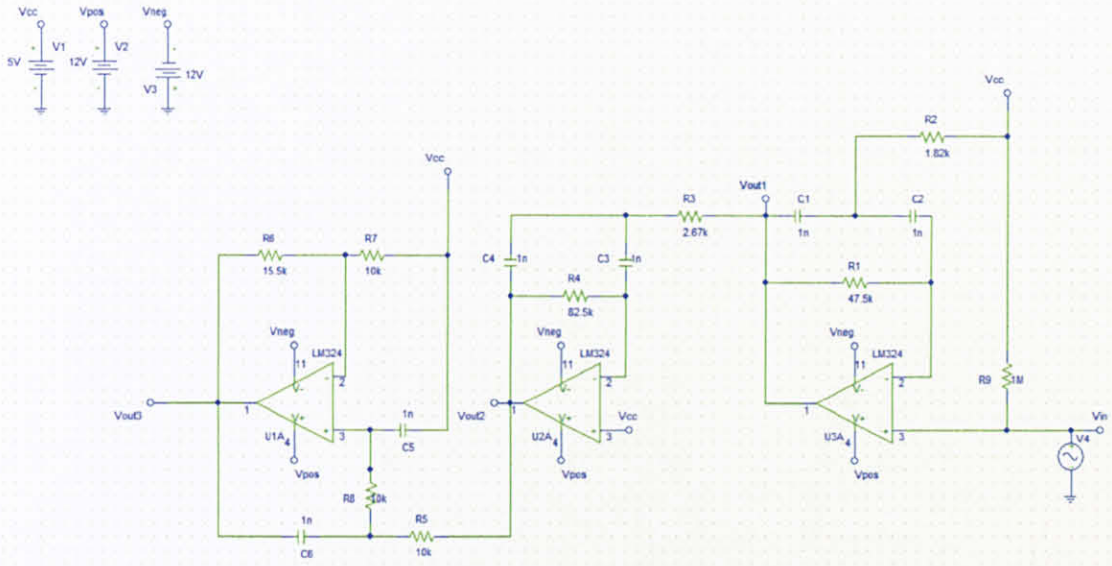


Figure 26: Circuit diagram for filter stage

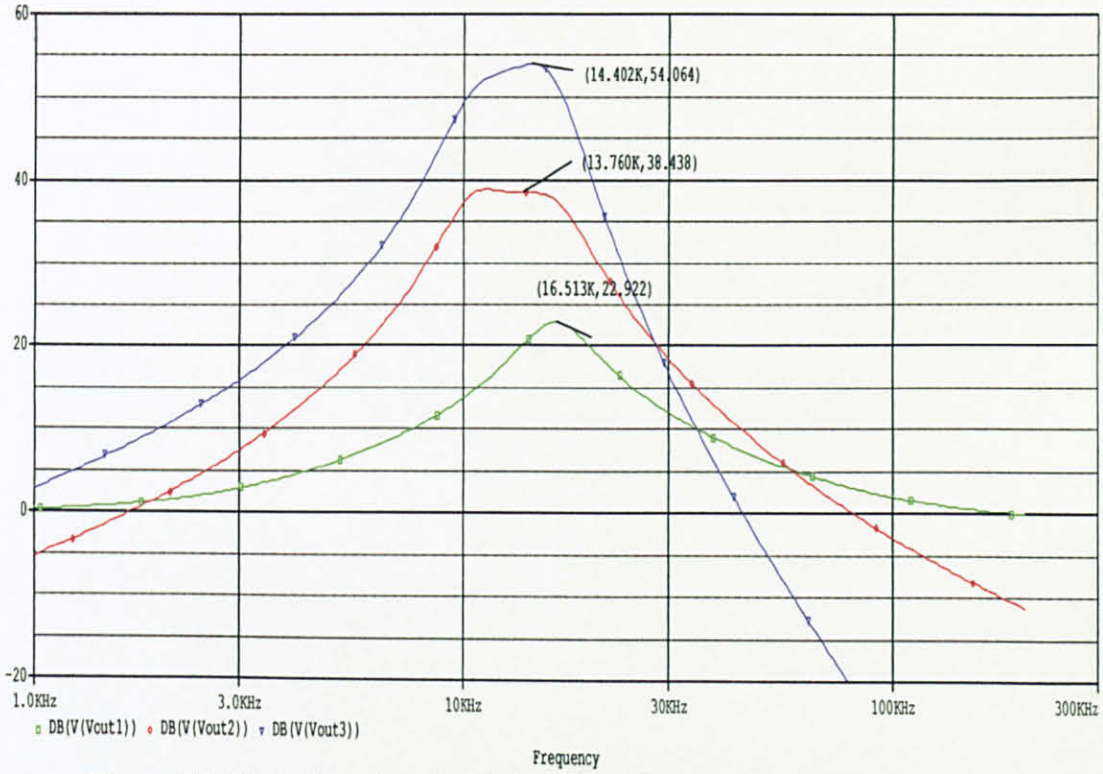


Figure 27: Bode Plot showing behaviors of all three active filters

As can be seen from the Magnitude Plot in figure 27, the first filter mostly isolates the pass band (10-20 KHz), with roughly unity gain for all frequencies outside the pass band. The second filter further accentuates gain in the pass-band while slightly reducing the magnitude of frequencies outside the passband. After this, the signal goes through a Butterworth filter to drastically increase gain of lower frequencies already in the pass band and virtually eliminate the higher frequencies, including the 125 KHz carrier signal [15]. The filter circuit designed achieved its objective which to allow only 10-20 kHz frequency to pass through the active bandpass filter.

4.4 PCB Design

Figure 28 and 29 is the circuit schematic for RFID reader system which combines the entire block of the circuit. The schematic is designed using Express PCB software.

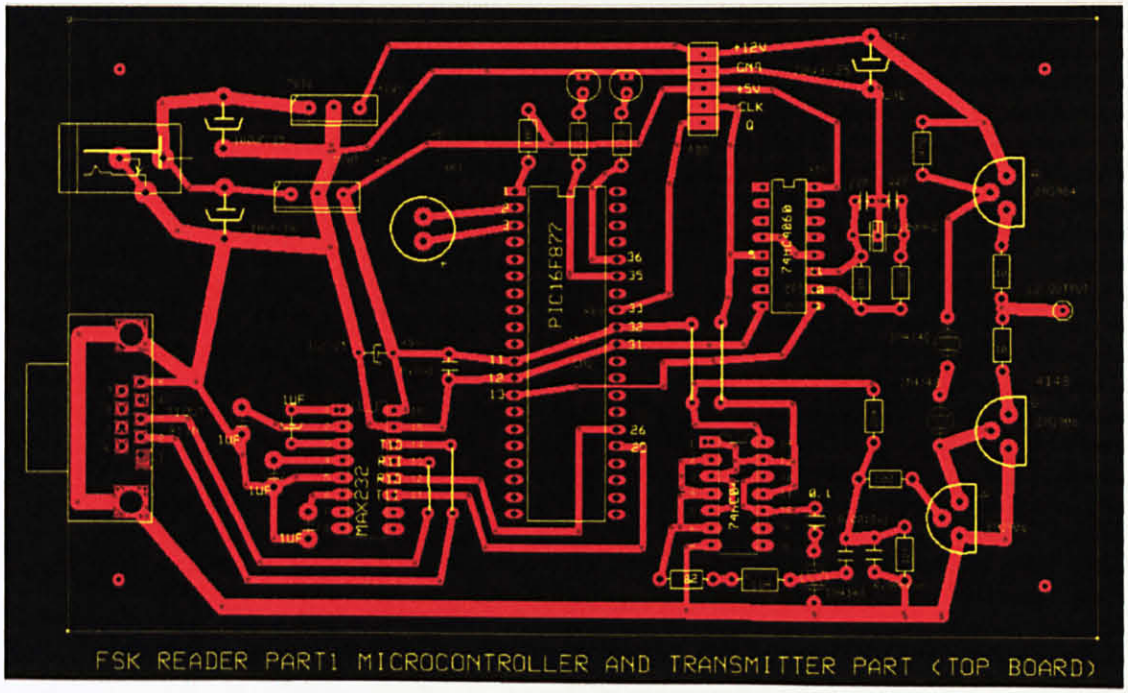


Figure 28: PCB Layout Design for Microcontroller and Transmitter Part

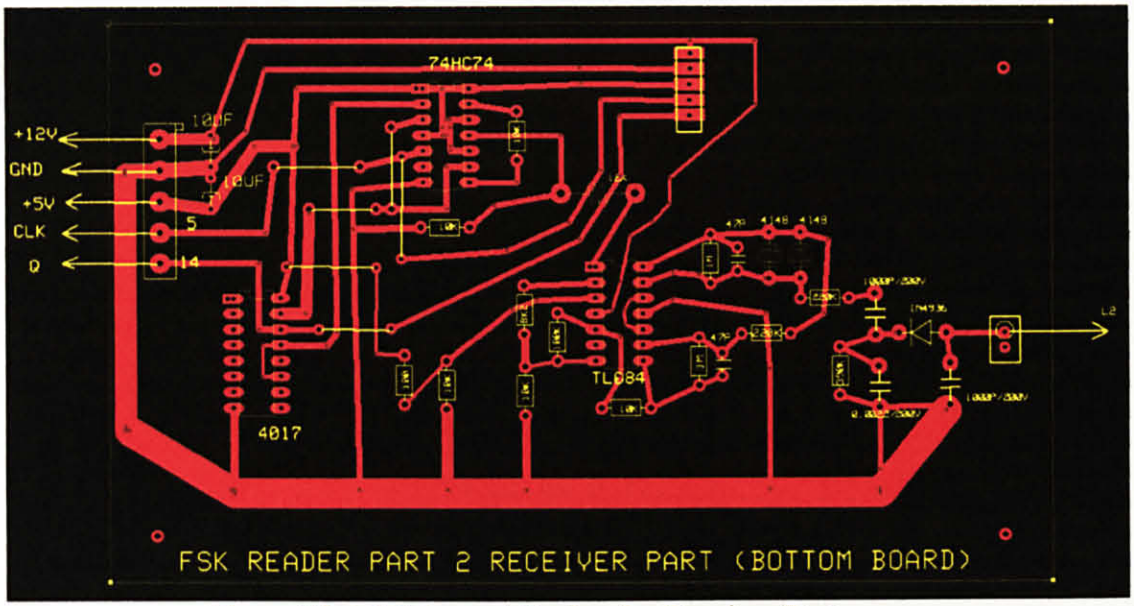


Figure 29: PCB Layout Design for Receiver Part

Figure 28 shows a microcontroller and transmit stage for the RFID reader while figure 20 is the receiver part.

Once the PCB is ready, then the actual circuits were implemented. Figure 30 is the actual PCB circuit for Microcontroller, transmitter and antenna part while figure 31 is the actual PCB circuit for RFID reader receiver part. Figure 32 shows the integration of transmit stage, rectangular antenna coil, receiver, active filter and microcontroller.

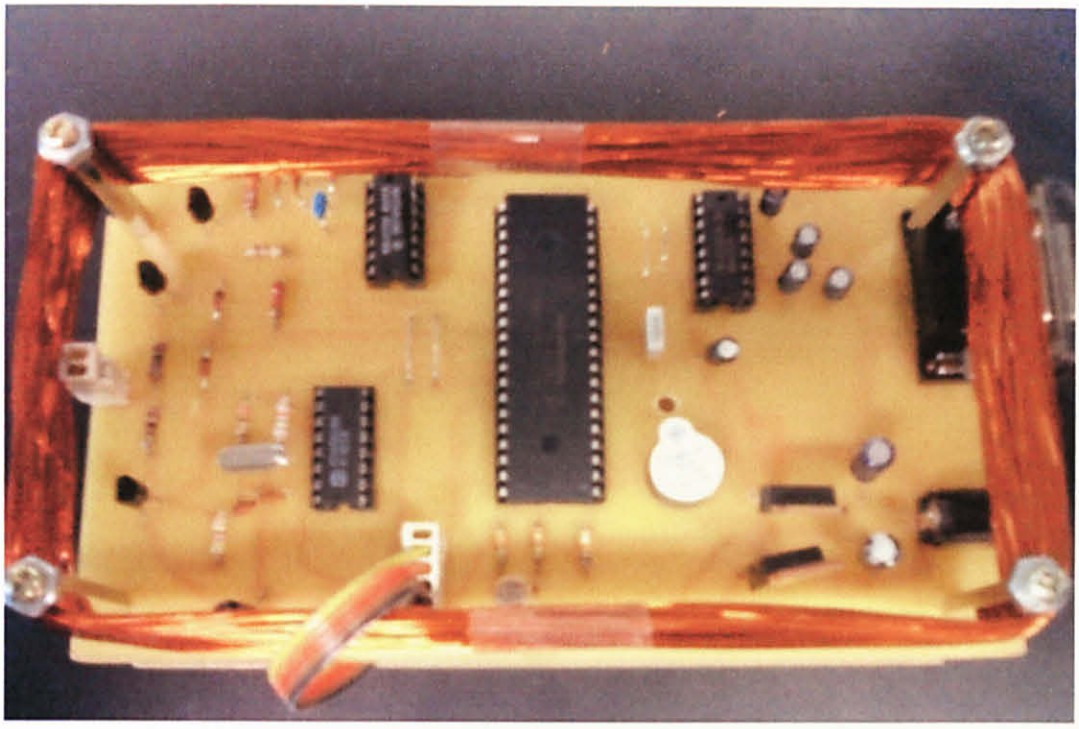


Figure 30: Actual PCB Circuit for Microcontroller, Transmitter and Antenna Part

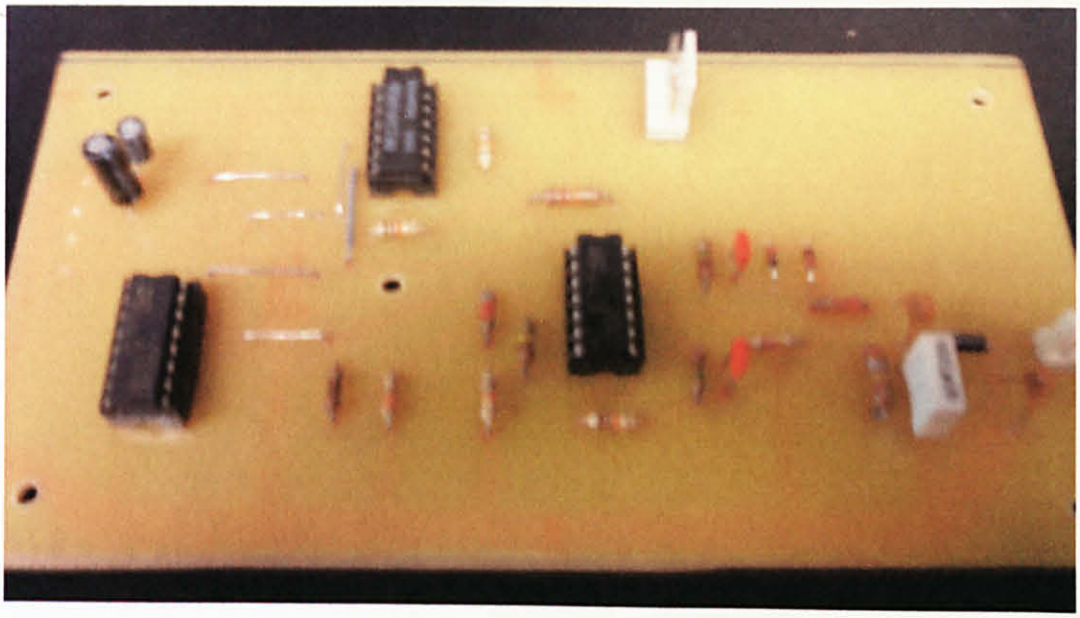


Figure 31: Actual PCB Circuit for Receiver Part

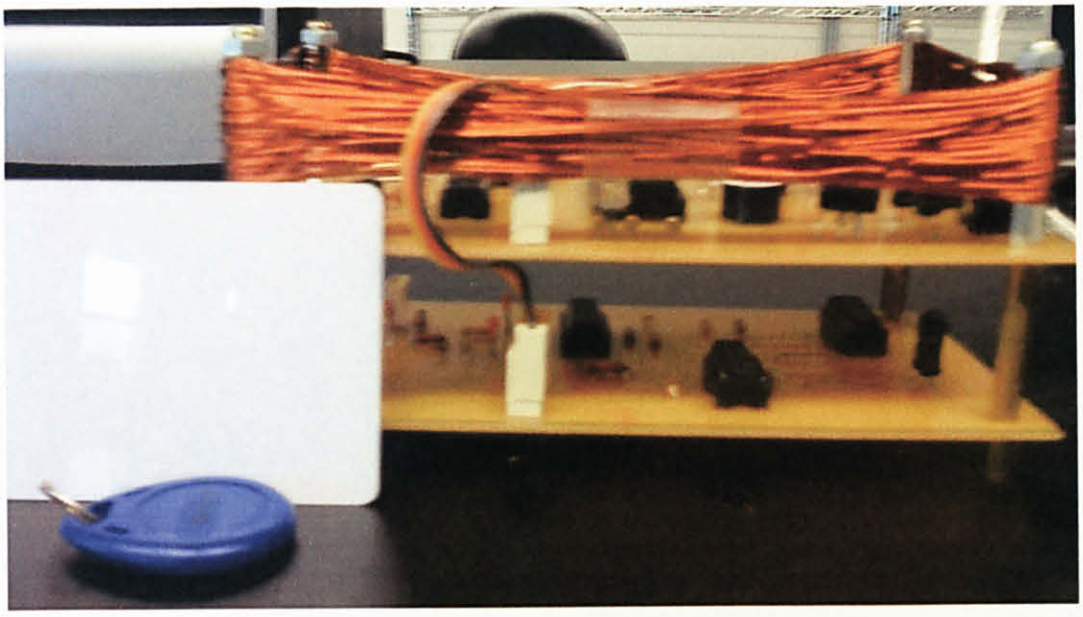


Figure 32: Full Design of RFID Reader Circuit

During the integration part, the circuit is not working as expected. Troubleshooting is conducted in order to determine the problem that might cause the circuit not to work accordingly. The possible issue that might be the cause of the failure of the circuit are:

(a) Through continuity check, the connections between each component are checked and some are not connected well. Improper soldering might be the cause that some of the components having no connection between each other.

(b) Incorrect programming code might also lead to the failure of the system. Since the microcontroller part is the heart of the system, faulty at the programming cause the circuit not to function and not giving a desired output. For RFID reader system, the main faction of microcontroller is to perform data decoding for the receiving signal.

CHAPTER 5

CONCLUSION AND RECOMMENDATION

5.1 Conclusion

A basic passive RFID system is composed of three main components which are reader, passive tag, and host computer. This project focus on designing an RFID reader which can sends out a signal to supplies power to a tag, retrieve the data stored in the tag and display the data to the host computer. The reader composed of a transmit stage, a rectangular coil antenna, an active filter as well as a microcontroller part.

The transmit stage consists of an RF choke followed by a current buffer and half-bridge amplifier. It is proven that RF choke removes high frequency components from the input square wave to create a sine wave. The voltage and current are then amplified to drive the antenna through a power amplifier.

The RF antenna is a series resonance circuit and was designed in a rectangular shape using a coil. The rectangular coil antenna is fine tuned by simply changing the capacitance value until the oscilloscope displayed the highest resonant voltage from the carrier frequency. A 1000pF of capacitor gives the highest resonant voltage.

The active filter components were simulated using Pspice. The filtering stage which consists of an active band pass filter is to extract the FSK signal and reject the signals outside 10-20 kHz signals. The simulation through Pspice for the active filter design proved that the filter designed gives desirable outputs

which eliminate the higher frequencies, including the 125 KHz carrier signal and allow only frequency range from 10-20 kHz to pass through the filters.

The integration part which to combine all the circuit block into one system is achieved by developing the PCB. Even though each block of circuit gives the desirable results, the integration part is not 100% working and this project needs further improvement in order to ensure that the RFID reader system designed is working successful.

5.2 Recommendation

Even though the objectives of the author are soon to be met, there is still room for improvement. When talking about future tasks of an RFID project, the possibilities are endless, however few of the recommendation are included in this report. An important characterization of the performance of an RFID system is read range, which is defined as the maximum distance between a reader and a tag where the radiation field from the reader is strong enough to power up the tag and the backscatter signal from the tag is strong enough to be detected correctly by the reader [8].

As mention in the report, the frequency used is a low frequency which is 125 kHz of carrier signal. Lower frequency means a lower read range and slower data read rate. The student would like to recommend designing a higher frequency reader that have a faster data transfer rate and longer read ranges than a lower frequency RFID.

The current RFID Reader being implemented by student is not working as expected, the next possible recommendation would be to integrate the whole system and ensure that the designed reader can transmit a carrier signal to the tag, received the tag's ID and display the ID to the host computer.

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APPENDICES

Appendix A: Milestone for the Final Year Project

No.	Detail/ Week	1	2	3	4	5	6	7	8		9	10	11	12	13	14	15	16
1	Project work continues																	
2	Submission of Progress Report 1				19/2													
3	Project work continues																	
4	Submission of Progress Report 2								26/3									
5	Project Work continues																	
6	Pre-EDX Poster Exhibition																	
7	Submission of Draft Report														28/4			
8	Submission of Final Report (Soft Cover) and Technical Report															5/5		
9	Oral presentation																	
10	Submission of Project Dissertation (Hard Bound)																	25/6

MID SEMESTER BREAK

Milestone Process

Appendix B: PIC codes for microcontroller, PIC16F877A

```
        processor 16F877
        #include "p16f877.inc"
              __config b'11111111101001
              ;Code Protected on, power-up timer on, WDT off,

#define _CARRY              STATUS,0
#define _ZERO               STATUS,2
#define _TO                 STATUS,4
#define _RP0                STATUS,5

#define _BUZZ1              PORTA,0
#define _BUZZ2              PORTA,1
#define _RS232TX            PORTC,6
#define _RS232RX            PORTC,7
#define _T0CK1              PORTA,4
StartPORTA          = b'01100
StartTRISA          = b'11000
BeepPort            = PORTA
Beep0               = StartPORTA
Beep1               = StartPORTA | b'00001
Beep2               = StartPORTA | b'00010

#define _DATA_IN    PORTB,0
#define _UNUSED1    PORTB,1
#define _LED1       PORTB,2
#define _LED2       PORTB,3
#define _UNUSED2    PORTB,4
#define _UNUSED3    PORTB,5
#define _UNUSED4    PORTB,6
#define _UNUSED5    PORTB,7

StartPORTB          = b'00000000
StartTRISB          = b'00000001

StartOPTION         = b'00001111'

BO3                 = h'0C'
DelayReg            = h'0C'
BitCtr              = h'0D'
BeepCtrHi           = h'0D'
TxByte              = h'0E'
BeepCtrLo           = h'0E'
Buffer0             = h'10'
Buffer1             = h'11'
Buffer2             = h'12'
Buffer3             = h'13'
Buffer4             = h'14'
Buffer5             = h'15'
Buffer6             = h'16'
Buffer7             = h'17'
Buffer8             = h'18'
Buffer9             = h'19'
BufferA             = h'1A'
BufferB             = h'1B'
;BufferC            = h'1C'
;Buffer0            = h'1D'
;Buffer0            = h'1E'
```

```
;Buffer0             = h'1F'
Old0                = h'20'
Old1                = h'21'
Old2                = h'22'
Old3                = h'23'
Old4                = h'24'
Old5                = h'25'
Old6                = h'26'
Old7                = h'27'
Old8                = h'28'
Old9                = h'29'
OldA                = h'2A'
OldB                = h'2B'
;OldC               = h'2C'
;OldD               = h'2D'
;OldE               = h'2E'
;OldF               = h'2F'

SKIP macro
            BTFSC PCLATH, 7

endm

       org h'0000'
       CLRF   PCLATH
       CLRF   INTCON
       CLRF   STATUS
       GOTO   RESET_A

       org h'0004'
       CLRF   INTCON
       CLRF   STATUS
       GOTO   RESET_A

;***** Subroutines

Delay07
            NOP
Delay06
            NOP
Delay05
            NOP
Delay04
            RETLW  0

RS232CR
            MOVLW  d'13'
            GOTO   RS232TxW
RS232TxDigit
            ANDLW  h'0F'
            MOVWF  TxByte
            MOVLW  h'0A'
            SUBWF  TxByte,W
            BTFSS  _CARRY
            GOTO   DigitLT10

DigitGE10
            MOVLW  'A'-'0'-h'0A'
            ADDWF  TxByte,f
DigitLT10
            MOVLW  '0'
            ADDWF  TxByte,W
RS232TxW
            MOVWF  TxByte
```

```
RS232Tx
              BSF           _RS232TX
              MOVLW  d'35'
              MOVLW  DelayReg
RS232TxD1
              DECFSZ DelayReg,f
              GOTO   RS232TxD1
              BCF           _RS232TX
              NOP
              MOVLW  d'32'
              MOVWF  DelayReg
RS232TxD2
              DECFSZ DelayReg,f
              GOTO   RS232TxD1
              CLRF   BitCtr
              BSF           BitCtr,3
RS232TxL1
              BTFSC  TxByte,0
              GOTO   RS232TxBit1
              NOP
RS232TxBit0
              BCF           _RS232TX
              BCF           _CARRY
              GOTO   RS232TxBitDone
RS232TxBit1
              BSF           _RS232TX
              BSF           _CARRY
              GOTO   RS232TxBitDone
RS232TxBitDone
              RRF           TxByte,f
              MOVLW  d'30'
              MOVWF  DelayReg
              GOTO   RS232TxD3
RS232TxD3
              DECFSZ DelayReg,f
              GOTO   RS232TxD3
              DECFSZ BitCtr,f
              GOTO   RS232TxL1
              CALL   Delay04
              BSF           _RS232TX
              RETLW  0

;***** End of Subroutines

RESET_A
              CLRWDT

              CLRF   STATUS
              CLRF   FSR
              MOVLW  StartPORTA
              MOVWF  PORTA
              MOVLW  StartPORTB
              MOVWF  PORTB
              BSF           _RP0
              MOVLW  StartTRISA
              MOVWF  TRISA
              MOVLW  StartTRISB
              MOVWF  TRISB
              MOVLW  StartOPTION
              MOVWF  OPTION_REG
              BCF           _RP0
              CLRF   Old0
              CLRF   Old1
              CLRF   Old2
```

```
                CLRF    Old3
                CLRF    Old4
                CLRF    Old5
                CLRF    Old6
                CLRF    Old7
                CLRF    Old8
                CLRF    Old9
                CLRF    OldA
                CLRF    OldB

BigLoop1
;303-581-1041

                BSF             _LED1
                CALL            Delay07
                BCF             _LED2
                MOVLW           h'09'
                CALL            RS232TxW
                MOVLW           d'96'
                MOVWF           BitCtr

GetEdge
                BTFSC           _DATA_IN
                GOTO            PreSync_H
                NOP
PreSync_L
                BTFSC           _DATA_IN
                GOTO            PreSync_H
                BTFSC           _DATA_IN
                GOTO            PreSync_H
DoSync_L
                CLRWDT
                BTFSS           _DATA_IN
                GOTO            DoSync_L
                BTFSS           _DATA_IN
                GOTO            DoSync_L
                GOTO            Sync_Done

PreSync_H
                BTFSS           _DATA_IN
                GOTO            PreSync_L
                BTFSS           _DATA_IN
                GOTO            PreSync_L

DoSync_H
                CLRWDT
                BTFSC           _DATA_IN
                GOTO            DoSync_H
                BTFSC           _DATA_IN
                GOTO            DoSync_H
                GOTO            Sync_Done
Sync_Done

                MOVLW   d'62'
                MOVWF   DelayReg
ReadBit
                GOTO    ReadBitD1
ReadBitD1
                DECFSZ  DelayReg,f
                GOTO    ReadBitD1
                CLRF    BO3
                BTFSC   _DATA_IN
                INCF    BO3,f
                BTFSC   _DATA_IN
```

```
                INCF    BO3,f
                BTFSC   _DATA_IN
                INCF    BO3,f
                BCF             _CARRY
                BTFSC   BO3,1
                BSF             _CARRY
                RLF             Buffer0,f
                RLF             Buffer1,f
                RLF             Buffer2,f
                RLF             Buffer3,f
                RLF             Buffer4,f
                RLF             Buffer5,f
                RLF             Buffer6,f
                RLF             Buffer7,f
                RLF             Buffer8,f
                RLF             Buffer9,f
                RLF             BufferA,f
                RLF             BufferB,f

                MOVLW   d'124'
                MOVWF   DelayReg
                DECFSZ  BitCtr,f
                GOTO    ReadBit

HeadSearch
                MOVLW   d'96'
                MOVWF   BitCtr
HeadSearchL1
                MOVLW   h'80'
                XORWF   BufferB,W
                BTFSS   _ZERO
                GOTO    NotHead0
                MOVLW   h'2A'
                XORWF   BufferA,W
                BTFSS   _ZERO
                GOTO    NotHead0
                GOTO    HeadFound
NotHead0
                RLF             Buffer0,f
                RLF             Buffer1,f
                RLF             Buffer2,f
                RLF             Buffer3,f
                RLF             Buffer4,f
                RLF             Buffer5,f
                RLF             Buffer6,f
                RLF             Buffer7,f
                RLF             Buffer8,f
                RLF             Buffer9,f
                BCF             Buffer0,0
                BTFSC   _CARRY
                BSF             Buffer0,0
                DECFSZ  BitCtr,f
                GOTO    HeadSearchL1
                GOTO    BigLoop1
HeadFound

CheckSame
                MOVF    Buffer0,W
                XORWF   Old0,W
                BTFSS   _ZERO
                GOTO    NotSame
                MOVF    Buffer1,W
                XORWF   Old1,W
                BTFSS   _ZERO
```

```
                GOTO    NotSame
                MOVF    Buffer2,W
                XORWF   Old2,W
                BTFSS   _ZERO
                GOTO    NotSame
                MOVF    Buffer3,W
                XORWF   Old3,W
                BTFSS   _ZERO
                GOTO    NotSame
                MOVF    Buffer4,W
                XORWF   Old4,W
                BTFSS   _ZERO
                GOTO    NotSame
                MOVF    Buffer5,W
                XORWF   Old5,W
                BTFSS   _ZERO
                GOTO    NotSame
                MOVF    Buffer6,W
                XORWF   Old6,W
                BTFSS   _ZERO
                GOTO    NotSame
                MOVF    Buffer7,W
                XORWF   Old7,W
                BTFSS   _ZERO
                GOTO    NotSame
                MOVF    Buffer8,W
                XORWF   Old8,W
                BTFSS   _ZERO
                GOTO    NotSame
                MOVF    Buffer9,W
                XORWF   Old9,W
                BTFSS   _ZERO
                GOTO    NotSame
                MOVF    BufferA,W
                XORWF   OldA,W
                BTFSS   _ZERO
                GOTO    NotSame
                MOVF    BufferB,W
                XORWF   OldB,W
                BTFSS   _ZERO
                GOTO    NotSame
                GOTO    Same
NotSame
                MOVF    Buffer0,W
                MOVWF   Old0
                MOVF    Buffer1,W
                MOVWF   Old1
                MOVF    Buffer2,W
                MOVWF   Old2
                MOVF    Buffer3,W
                MOVWF   Old3
                MOVF    Buffer4,W
                MOVWF   Old4
                MOVF    Buffer5,W
                MOVWF   Old5
                MOVF    Buffer6,W
                MOVWF   Old6
                MOVF    Buffer7,W
                MOVWF   Old7
                MOVF    Buffer8,W
                MOVWF   Old8
                MOVF    Buffer9,W
                MOVWF   Old9
                MOVF    BufferA,W
```

```
                MOVWF   OldA
                MOVF    BufferB,W
                MOVWF   OldB
                GOTO    BigLoop1
Same

TxTag
                BSF             _LED2
                CALL    Delay07
                BCF             _LED1
                MOVLW   d'4'
                MOVWF   BeepCtrHi
                MOVLW   d'0'
                MOVWF   BeepCtrLo
BeepLoopJ1
                GOTO    BeepLoopJ2
BeepLoopJ2
                MOVLW   Beep1
                MOVWF   BeepPort
                MOVLW   d'34'
                MOVWF   DelayReg
BeepD1
                CLRWDT
                DECFSZ  DelayReg,f
                GOTO    BeepD1
                MOVLW   Beep2
                MOVWF   BeepPort
                MOVLW   d'32'
                MOVWF   DelayReg
                NOP
                GOTO    BeepD2
BeepD2
                CLRWDT
                DECFSZ  DelayReg,f
                GOTO    BeepD2
                DECFSZ  BeepCtrLo,f
                GOTO    BeepLoopJ1
                DECFSZ  BeepCtrHi,f
                GOTO    BeepLoopJ2
                NOP
                MOVLW   Beep0
                MOVWF   BeepPort

                CALL    RS232CR
                MOVLW   'F'
                CALL    RS232TxW
                MOVLW   'S'
                CALL    RS232TxW
                MOVLW   'K'
                CALL    RS232TxW
                MOVLW   ' '
                CALL    RS232TxW
                MOVLW   '/'
                CALL    RS232TxW
                MOVLW   '8'
                CALL    RS232TxW
                MOVLW   '-'
                CALL    RS232TxW
                MOVLW   '/'
                CALL    RS232TxW
                MOVLW   '1'
                CALL    RS232TxW
                MOVLW   '0'
                CALL    RS232TxW
```

```
MOVLW  'T'
CALL   RS232TxW
MOVLW  'b'
CALL   RS232TxW
MOVLW  'i'
CALL   RS232TxW
MOVLW  't'
CALL   RS232TxW
MOVLW  '='
CALL   RS232TxW
MOVLW  '5'
CALL   RS232TxW
MOVLW  '0'
CALL   RS232TxW
MOVLW  'T'
CALL   RS232TxW
MOVLW  'c'
CALL   RS232TxW
MOVLW  'y'
CALL   RS232TxW
CALL   RS232CR
MOVLW  'C'
CALL   RS232TxW
MOVLW  'o'
CALL   RS232TxW
MOVLW  'n'
CALL   RS232TxW
MOVLW  's'
CALL   RS232TxW
MOVLW  't'
CALL   RS232TxW
MOVLW  'a'
CALL   RS232TxW
MOVLW  'n'
CALL   RS232TxW
MOVLW  't'
CALL   RS232TxW
CALL   RS232CR
MOVLW  'T'
CALL   RS232TxW
MOVLW  't'
CALL   RS232TxW
MOVLW  'a'
CALL   RS232TxW
MOVLW  'g'
CALL   RS232TxW
MOVLW  '='
CALL   RS232TxW
MOVLW  '9'
CALL   RS232TxW
MOVLW  '6'
CALL   RS232TxW
MOVLW  'T'
CALL   RS232TxW
MOVLW  'b'
CALL   RS232TxW
MOVLW  'i'
CALL   RS232TxW
MOVLW  't'
CALL   RS232TxW
CALL   RS232CR
MOVLW  'p'
CALL   RS232TxW
MOVLW  'o'
```

```
                CALL    RS232TxW
                MOVLW   'l'
                CALL    RS232TxW
                MOVLW   'a'
                CALL    RS232TxW
                MOVLW   'r'
                CALL    RS232TxW
                MOVLW   'i'
                CALL    RS232TxW
                MOVLW   't'
                CALL    RS232TxW
                MOVLW   'y'
                CALL    RS232TxW
                MOVLW   ' '
                CALL    RS232TxW
                MOVLW   '0'
                CALL    RS232TxW
                CALL    RS232CR

                MOVLW   BufferB
                MOVWF   FSR
TxLoop1
                SWAPF   INDF,W
                CALL    RS232TxDigit
                MOVF    INDF,W
                CALL    RS232TxDigit
                DECF    FSR,f
                BTFSC   FSR,4
                GOTO    TxLoop1
                CALL    RS232CR

                GOTO    BigLoop1

end


end
```

MICROCHIP PIC16F874A/877A

40-Pin Enhanced FLASH Microcontroller Product Brief

High Performance RISC CPU:

- Only 35 single word instructions to learn
- All single cycle instructions except for program branches, which are two cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle
- Up to 8K x 14 words of FLASH Program Memory, Up to 368 x 8 bytes of Data Memory (RAM), Up to 256 x 8 bytes of EEPROM data memory
- Pinout compatible to other 40-pin PIC16CXXX and PIC16FXXX microcontrollers

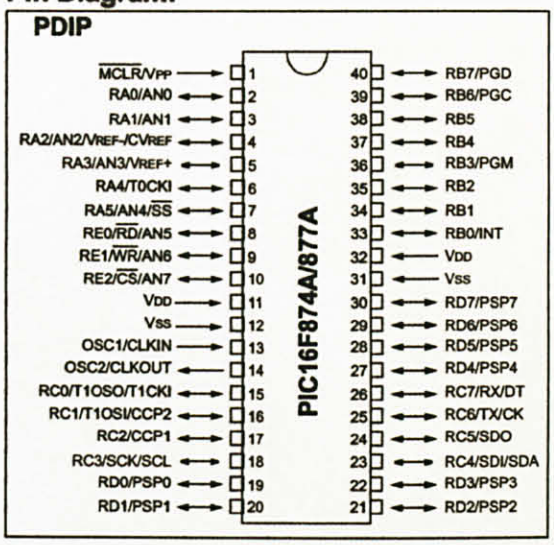
Peripheral Features:

- Timer0 module: 8-bit timer/counter with 8-bit prescaler
- Timer1 module: 16-bit timer/counter with prescaler, can be incremented during SLEEP via external crystal/clock
- Timer2 module: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Two Capture, Compare, PWM modules
- Master Synchronous Serial Port (MSSP) module. Two modes of operation:
  - 3-wire SPI™ (supports all 4 SPI modes)
  - I^2C™ Master and Slave mode
- Addressable USART module:
  - Supports interrupt on Address bit
- Parallel Slave Port (PSP) module 8-bits wide, external $\overline{RD}$, $\overline{WR}$ and $\overline{CS}$ controls
- High Sink/Source Current: 25 mA

Analog Features:

- 10-bit 8-ch Analog-to-Digital Converter (A/D)
- Brown-out Reset (BOR)
- Analog Comparator module with:
  - Two analog comparators
  - Programmable on-chip voltage reference (V_{REF}) module
  - Programmable input multiplexing from device inputs and internal voltage reference
  - Comparator outputs are externally accessible

Pin Diagram:



CMOS Technology:

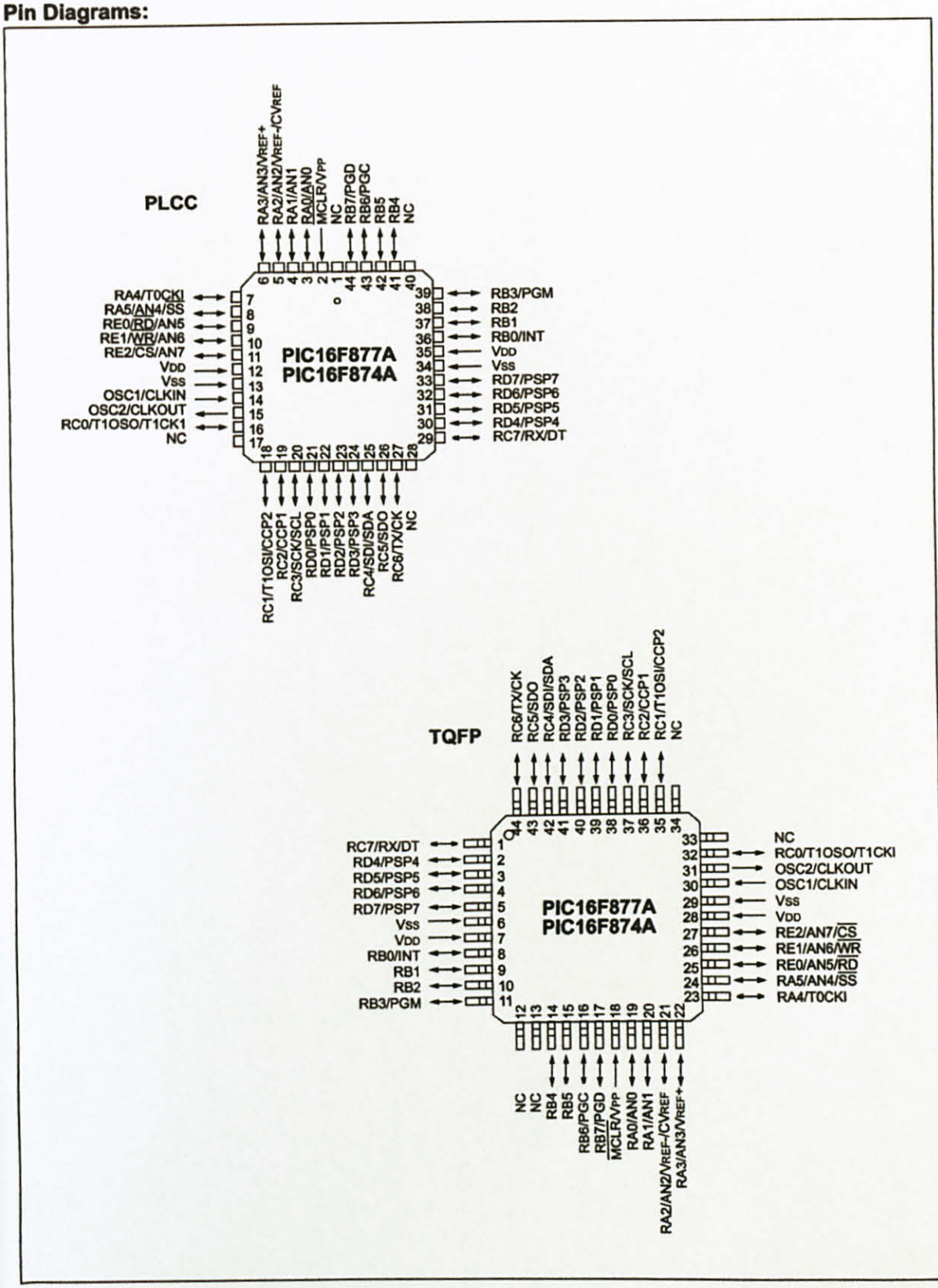
- Low power, high speed FLASH/EEPROM technology
- Fully static design
- Wide operating voltage range (2.0V to 5.5V)
- Commercial and Industrial temperature ranges
- Low power consumption

Special Microcontroller Features:

- 100,000 erase/write cycle Enhanced FLASH program memory typical
- 1,000,000 erase/write cycle Data EEPROM memory typical
- Data EEPROM Retention > 40 years
- Self reprogrammable under software control
- In-Circuit Serial Programming™ (ICSP™) via two pins
- Single supply 5V In-Circuit Serial Programming
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code protection
- Power saving SLEEP mode
- Selectable oscillator options
- In-Circuit Debug (ICD) via two pins

Device	Program Memory		Data SRAM (Bytes)	EEPROM (Bytes)	I/O	10-bit A/D (ch)	CCP (PWM)	MSSP		USART	Timers 8/16-bit	Comparators
	Bytes	# Single Word Instructions						SPI	Master I^2C			
PIC16F874A	7.2K	4096	192	128	33	8	2	Yes	Yes	Yes	2 / 1	2
PIC16F877A	14.3K	8192	368	256	33	8	2	Yes	Yes	Yes	2 / 1	2

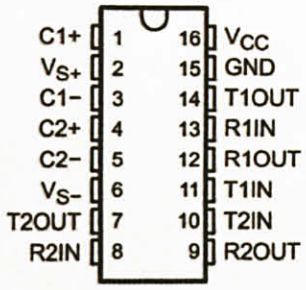
Pin Diagrams:



SLLS047L – FEBRUARY 1989 – REVISED MARCH 2004

- **Meets or Exceeds TIA/EIA-232-F and ITU Recommendation V.28**
- **Operates From a Single 5-V Power Supply With 1.0-μF Charge-Pump Capacitors**
- **Operates Up To 120 kbit/s**
- **Two Drivers and Two Receivers**
- **±30-V Input Levels**
- **Low Supply Current . . . 8 mA Typical**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
- **Upgrade With Improved ESD (15-kV HBM) and 0.1-μF Charge-Pump Capacitors is Available With the MAX202**
- **Applications**
  - **TIA/EIA-232-F, Battery-Powered Systems, Terminals, Modems, and Computers**

MAX232 . . . D, DW, N, OR NS PACKAGE
MAX232I . . . D, DW, OR N PACKAGE
(TOP VIEW)



description/ordering information

The MAX232 is a dual driver/receiver that includes a capacitive voltage generator to supply TIA/EIA-232-F voltage levels from a single 5-V supply. Each receiver converts TIA/EIA-232-F inputs to 5-V TTL/CMOS levels. These receivers have a typical threshold of 1.3 V, a typical hysteresis of 0.5 V, and can accept ±30-V inputs. Each driver converts TTL/CMOS input levels into TIA/EIA-232-F levels. The driver, receiver, and voltage-generator functions are available as cells in the Texas Instruments LinASIC™ library.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (N)	Tube of 25	MAX232N	MAX232N
	SOIC (D)	Tube of 40	MAX232D	MAX232
		Reel of 2500	MAX232DR	
	SOIC (DW)	Tube of 40	MAX232DW	MAX232
		Reel of 2000	MAX232DWR	
	SOP (NS)	Reel of 2000	MAX232NSR	MAX232
−40°C to 85°C	PDIP (N)	Tube of 25	MAX232IN	MAX232IN
	SOIC (D)	Tube of 40	MAX232ID	MAX232I
		Reel of 2500	MAX232IDR	
	SOIC (DW)	Tube of 40	MAX232IDW	MAX232I
		Reel of 2000	MAX232IDWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

National Semiconductor

January 2000

LM78LXX Series
3-Terminal Positive Regulators

General Description

The LM78LXX series of three terminal positive regulators is available with several fixed output voltages making them useful in a wide range of applications. When used as a zener diode/resistor combination replacement, the LM78LXX usually results in an effective output impedance improvement of two orders of magnitude, and lower quiescent current. These regulators can provide local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow the LM78LXX to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment.

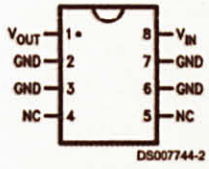
The LM78LXX is available in the plastic TO-92 (Z) package, the plastic SO-8 (M) package and a chip sized package (8-Bump micro SMD) using National's micro SMD package technology. With adequate heat sinking the regulator can deliver 100 mA output current. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistors is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

Features

- LM78L05 in micro SMD package
- Output voltage tolerances of ±5% over the temperature range
- Output current of 100 mA
- Internal thermal overload protection
- Output transistor safe area protection
- Internal short circuit current limit
- Available in plastic TO-92 and plastic SO-8 low profile packages
- No external components
- Output voltages of 5.0V, 6.2V, 8.2V, 9.0V, 12V, 15V

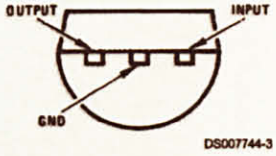
Connection Diagrams

SO-8 Plastic (M)
(Narrow Body)



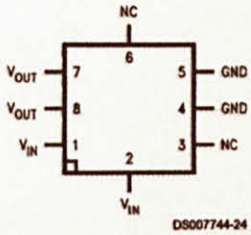
Top View

(TO-92)
Plastic Package (Z)



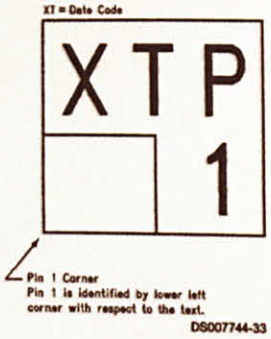
Bottom View

8-Bump micro SMD



Top View
(Bump Side Down)

micro SMD Marking Orientation



Top View

National Semiconductor

August 2005

LM341/LM78MXX Series
3-Terminal Positive Voltage Regulators

General Description

The LM341 and LM78MXX series of three-terminal positive voltage regulators employ built-in current limiting, thermal shutdown, and safe-operating area protection which makes them virtually immune to damage from output overloads.

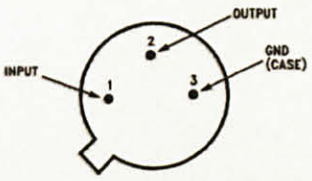
With adequate heatsinking, they can deliver in excess of 0.5A output current. Typical applications would include local (on-card) regulators which can eliminate the noise and degraded performance associated with single-point regulation.

Features

- Output current in excess of 0.5A
- No external components
- Internal thermal overload protection
- Internal short circuit current-limiting
- Output transistor safe-area compensation
- Available in TO-220, TO-39, and TO-252 D-PAK packages
- Output voltages of 5V, 12V, and 15V

Connection Diagrams

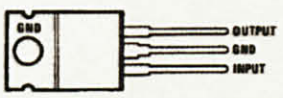
TO-39 Metal Can Package (H)



01048405

Bottom View
Order Number LM78M05CH, LM78M12CH or LM78M15CH
See NS Package Number H03A

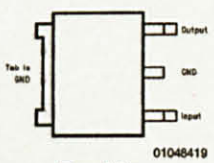
TO-220 Power Package (T)



01048406

Top View
Order Number LM341T-5.0, LM341T-12, LM341T-15, LM78M05CT, LM78M12CT or LM78M15CT
See NS Package Number T03B

TO-252



01048419

Top View
Order Number LM78M05CDT
See NS Package Number TD03B

 DS010484

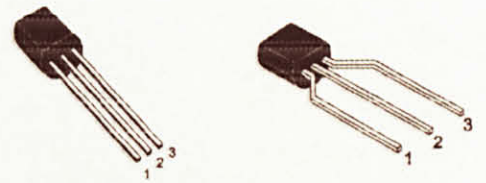
SMALL SIGNAL NPN TRANSISTOR

PRELIMINARY DATA

Ordering Code	Marking	Package / Shipment
2N3904	2N3904	TO-92 / Bulk
2N3904-AP	2N3904	TO-92 / Ammopack

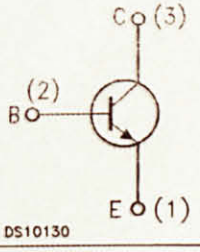
- SILICON EPITAXIAL PLANAR NPN TRANSISTOR
- TO-92 PACKAGE SUITABLE FOR THROUGH-HOLE PCB ASSEMBLY
- THE PNP COMPLEMENTARY TYPE IS 2N3906

APPLICATIONS
- WELL SUITABLE FOR TV AND HOME APPLIANCE EQUIPMENT
- SMALL LOAD SWITCH TRANSISTOR WITH HIGH GAIN AND LOW SATURATION VOLTAGE



TO-92 Bulk | TO-92 Ammopack

INTERNAL SCHEMATIC DIAGRAM



DS10130

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-Base Voltage (I_E = 0)	60	V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)	40	V
V_{EBO}	Emitter-Base Voltage (I_C = 0)	6	V
I_C	Collector Current	200	mA
P_{tot}	Total Dissipation at T_C = 25 °C	625	mW
T_{stg}	Storage Temperature	-65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

2N3906

Preferred Device

General Purpose Transistors

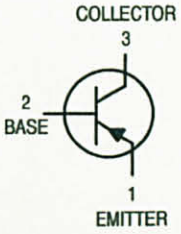
PNP Silicon

ON Semiconductor®

http://onsemi.com

Features

- Pb–Free Packages are Available*



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector – Emitter Voltage	V_{CEO}	40	Vdc
Collector – Base Voltage	V_{CBO}	40	Vdc
Emitter – Base Voltage	V_{EBO}	5.0	Vdc
Collector Current – Continuous	I_C	200	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Total Power Dissipation @ T_A = 60°C	P_D	250	mW
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS (Note 1)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	83.3	°C/W

1. Indicates Data in addition to JEDEC Requirements.

TO–92
CASE 29
STYLE 1

MARKING DIAGRAMS

Y = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

June, 2004 – Rev. 2

Publication Order Number:
2N3906/D

- Low Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- Low Total Harmonic Distortion . . . 0.003% Typ
- High Input Impedance . . . JFET-Input Stage
- Latch-Up-Free Operation
- High Slew Rate . . . 13 V/μs Typ
- Common-Mode Input Voltage Range Includes V_{CC+}

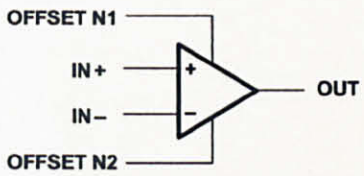
description

The TL08x JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient. Offset adjustment and external compensation options are available within the TL08x family.

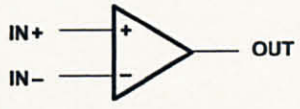
The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The Q-suffix devices are characterized for operation from –40°C to 125°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

symbols

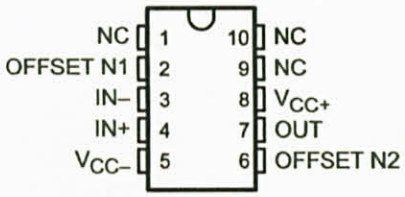
TL081



TL082 (EACH AMPLIFIER)
TL084 (EACH AMPLIFIER)



TL081M
U PACKAGE
(TOP VIEW)



TL082M
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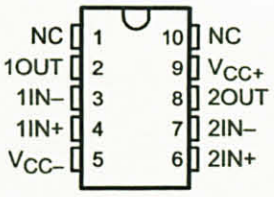
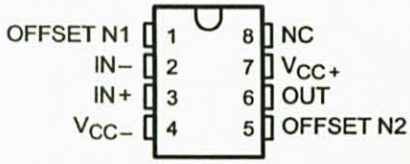
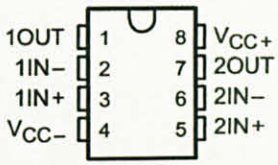


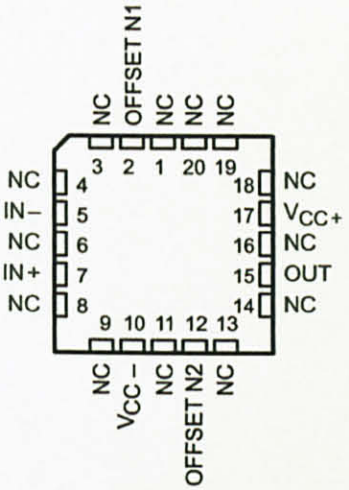
TL081, TL081A, TL081B
D, JG, P, OR PW PACKAGE
(TOP VIEW)



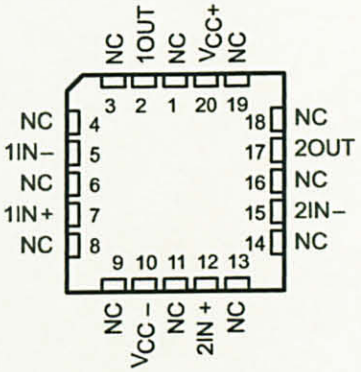
TL082, TL082A, TL082B
D, JG, P, OR PW PACKAGE
(TOP VIEW)



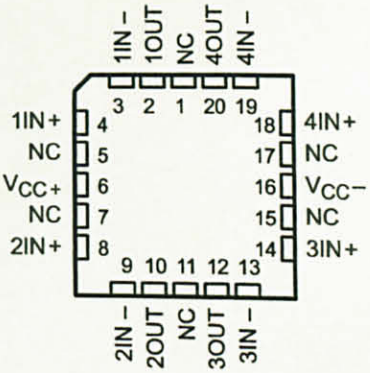
TL081M . . . FK PACKAGE
(TOP VIEW)



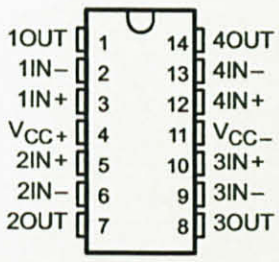
TL082M . . . FK PACKAGE
(TOP VIEW)



TL084M . . . FK PACKAGE
(TOP VIEW)



TL084, TL084A, TL084B
D, J, N, PW, OR W PACKAGE
(TOP VIEW)



NC – No internal connection

High-speed diodes 1N4148; 1N4448

FEATURES

- Hermetically sealed leaded glass SOD27 (DO-35) package
- High switching speed: max. 4 ns
- General application
- Continuous reverse voltage: max. 75 V
- Repetitive peak reverse voltage: max. 100 V
- Repetitive peak forward current: max. 450 mA.

APPLICATIONS

- High-speed switching.

DESCRIPTION

The 1N4148 and 1N4448 are high-speed switching diodes fabricated in planar technology, and encapsulated in hermetically sealed leaded glass SOD27 (DO-35) packages.

The diodes are type branded.

Fig.1 Simplified outline (SOD27; DO-35) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{RRM}	repetitive peak reverse voltage		–	100	V
V_R	continuous reverse voltage		–	75	V
I_F	continuous forward current	see Fig.2; note 1	–	200	mA
I_{FRM}	repetitive peak forward current		–	450	mA
I_{FSM}	non-repetitive peak forward current	square wave; T_j = 25 °C prior to surge; see Fig.4			
		t = 1 μs	–	4	A
		t = 1 ms	–	1	A
		t = 1 s	–	0.5	A
P_{tot}	total power dissipation	T_{amb} = 25 °C; note 1	–	500	mW
T_{stg}	storage temperature		–65	+200	°C
T_j	junction temperature		–	200	°C

Note

1. Device mounted on an FR4 printed circuit-board; lead length 10 mm.

14-stage binary ripple counter with oscillator 74HC/HCT4060

FEATURES

- All active components on chip
- RC or crystal oscillator configuration
- Output capability: standard (except for R_{TC} and C_{TC})
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4060 are high-speed Si-gate CMOS devices and are pin compatible with "4060" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4060 are 14-stage ripple-carry counter/dividers and oscillators with three oscillator terminals (RS, R_{TC} and C_{TC}), ten buffered outputs (Q_3 to Q_9 and Q_{11} to Q_{13}) and an overriding asynchronous master reset (MR).

The oscillator configuration allows design of either RC or crystal oscillator circuits. The oscillator may be replaced by an external clock signal at input RS. In this case keep the other oscillator pins (R_{TC} and C_{TC}) floating.

The counter advances on the negative-going transition of RS. A HIGH level on MR resets the counter (Q_3 to Q_9 and Q_{11} to Q_{13} = LOW), independent of other input conditions.

In the HCT version, the MR input is TTL compatible, but the RS input has CMOS input switching levels and can be driven by a TTL output by using a pull-up resistor to V_{CC}.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	RS to Q_3		31	31	ns
	Q_n to Q_{n+1}		6	6	ns
t_{PHL}	MR to Q_n		17	18	ns
f_{max}	maximum clock frequency		87	88	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1, 2 and 3	40	40	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V
3. For formula on dynamic power dissipation see next pages.

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	Q_{11} to Q_{13}	counter outputs
7, 5, 4, 6, 14, 13, 15	Q_3 to Q_9	counter outputs
8	GND	ground (0 V)
9	C_{TC}	external capacitor connection
10	R_{TC}	external resistor connection
11	RS	clock input/oscillator pin
12	MR	master reset
16	V_{CC}	positive supply voltage

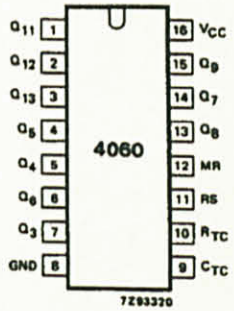


Fig.1 Pin configuration.

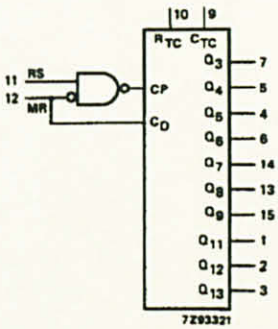


Fig.2 Logic symbol.

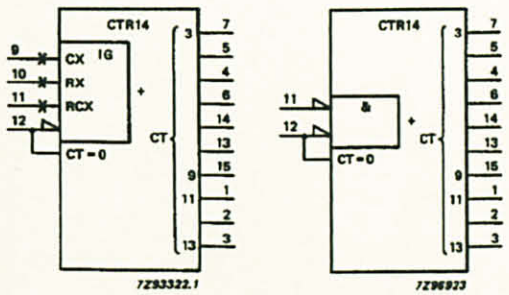


Fig.3 IEC logic symbol.