1 MHz PWM Generation Using Intersective Method

By

Muhammad Afiq bin Mohd Sadli

Dissertation submitted in partial fulfillment
of the requirements for the
Bachelor of Engineering (Hons)
(Electrical and Electronics Engineering)

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CERTIFICATION OF APPROVAL

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CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

……

(MUHAMMAD AFIQ BIN MOHD SADLI)

ABSTRACT

This project serves as a basis to investigate the performance of a PWM generator circuit. This is due to available PWM generation method cannot cover a wide operation frequency and wide duty cycle range. PWM signal had been used in various application including power system, communication and control systems. Pulse-width modulation (PWM) is a very efficient way of providing intermediate amounts of electrical power between fully on and fully off. A simple power switch with a typical power source provides full power only, when switched on. PWM is a comparatively-recent technique, made practical by modern electronic power switches. This project will focus on PWM generation in high frequency of 1 MHz. The aim of this work is to generate PWM signal at 1 MHz frequency with duty cycle ranging from 30 % to 70 %. During the process, various parameters like duty cycle, rise and fall time, and signal resolution is observed to determine the quality of PWM signal generated. From the findings, this work will determine the suitable conditions that can be implemented in suitable application using this PWM generation technique, intersective method.

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Last but not least, I thank my parents for their endless support and encouragement in the course of doing my degree.

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LIST OF ABBREVIATIONS

Wherever applicable the meaning of each abbreviation used in this preliminary report is given. The abbreviations in the following list are most widely used throughout this preliminary report.

Abbreviations

AC	-	Alternating current
DC	-	Direct current
IC	-	Integrated circuit
OP-AMP	-	operational amplifier
NPN	-	Negative-Positive-Negative
MOSFET	-	metal–oxide–semiconductor field-effect transistor

CHAPTER 1

INTRODUCTION

1.1 Background of Study

Pulse Width Modulation (PWM) is the widely used technique various switching applications. The implementation of PWM over traditional linear switching is preferable as the switching loss (I^2R loss) found in traditional linear switching is not present in PWM switching. Pulse-width modulation (PWM) is a very efficient way in providing intermediate amounts of electrical power between fully on and fully off. A simple power switch with a typical power source provides full power only, when switched on. PWM is a comparatively-recent technique, made practical by modern electronic power switches, in example; switching of MOSFETs in power electronic converters namely AC to DC converter (rectifier), DC to AC converter (inverter), DC to DC converter (chopper) and AC to AC converter (cycloconverter).

Pulse-width modulation (PWM) of a signal or power source involves the modulation of its duty cycle, to either convey information over a communications channel or control the amount of power sent to a load.

In this work, PWM is generated using intersective method by comparing the sawtooth waveform as modulating signal and DC level voltage as reference voltage in 1 MHz frequency.

1.2 Problem Statements

The available means of PWM generation is basically restricted in terms of operating frequency (usually low frequency) and duty cycle ranges. Apart from that, the complexity of the circuit and the cost itself is the main drawback of generating high frequency PWM signal. The first challenge of this project is how to generate PWM signal at 1 MHz frequency with varying duty cycles ranging from 30 % to 70 %. PWM signal is derived from sawtooth waveform. So, it is important to study how sawtooth waveform is generated and then manipulating the signal using several methods to get PWM signals. The sawtooth waveform is derived from the function generator and PWM generator circuit is built to get 1 MHz PWM signal. This work will investigate the performance of the proposed circuit in terms of range of duty cycles and the resolutions of PWM signals in 1 MHz frequency. This work will be verified with several PWM chips found in the market.

1.3 Objective and Scope of Study

The objective of this study is to determine whether the proposed PWM generator circuit is able to perform in 1 MHz with wide range of duty cycle and have good resolution. Sawtooth waveform as the modulating signal in PWM circuit will be studied as well. This includes the study of various ways to generate sawtooth signal and make comparison between the methods. The scope of study will cover the theory of PWM generation and the theory of operation of the proposed circuit. The quality of generated PWM signal will be observed in terms of resolution and noise.

CHAPTER 2

LITERATURE REVIEW

2.1 PWM Signal

PWM is important to control power switches as it provides intermediate electrical power between fully on and fully off. The interval during fully on time will determine the amount of power being transferred by the power switch. The proportion of on time in regular interval or period of time is termed as duty cycle and express in percentage. 100% means the switch is being fully switched on while 0% means the switch is being fully switch off. Hence, the duty cycle value determines the amount of power transferred [1]. Duty cycle is directly proportional to the amount of power transferred. So, low duty cycle indicates low power and high duty cycle indicates high power. Duty cycle, *D* is given by:

$$D = \frac{\tau}{T} \tag{1}$$

Where τ = duration of time when fully ON

T = the period of the function

The PWM in this project is obviously applied for power application in the converter circuit. PWM has several advantages [2] of normal switching method. PWM provides lesser power loss during switching (power loss in the form of heat from I^2R losses), faster switching hence high frequency circuit application is possible and relatively low cost as the devices needed is lesser and the circuit construction is made simpler with the use of semiconductor switches and devices.

2.2 Sawtooth Waveform

Sawtooth waveform is used as modulating signal in PWM generation. Sawtooth waveform is a kind of non-sinusoidal waveform. The name sawtooth is derived from its resemblance to the teeth on the blade of a saw. Sawtooth wave ramps upward and then sharply drops.

The general mathematical form of sawtooth waveform, is based on the floor function of time *t*, in the range −1 to 1, and with period *a*, can be expressed in (2) below:

$$x(t) = 2\left(\frac{t}{a} - \text{floor}\left(\frac{t}{a} - \frac{1}{2}\right)\right) \tag{2}$$

RMS voltage, V_{rms} and average voltage, V_{avg} in sawtooth signal is related with peak voltage, V_{pk}, frequency, f and duration of the signal itself [3]. The RMS voltage, V_{rms} is expressed in (3) below:

$$V_{rms} = V_{pk}\sqrt{\frac{fT}{3}} \tag{3}$$

As for average voltage, V_{avg}, it is expressed in (4) below:

$$V_{avg} = \frac{V_{pk} \times T \times f}{2} \tag{4}$$

Sawtooth signal is derived directly from the function generator which is set at 1 MHz frequency and fed to the inverting input of the OP-AMP or comparator in the PWM generator circuit.

2.3 Comparator

A comparator is an electronic device which compares two voltages or currents and switches its output to indicate which is larger. The operational amplifier or op-amp is suitable way to implement voltage comparator as it has a well balanced difference input and high gain [4]. These characteristics allow the op-amps to serve as comparator. To make op-amp to operate as comparator, the op-amp should operate in open-loop configuration.

The output of op-amp will be at the most positive voltage when non-inverting input voltage (V+) is higher than inverting input (V-). Otherwise, the op-amp output is at the most negative voltage it can when the non-inverting input (V+) drops below the inverting input (V-).

2.4 Comparator Feedbacks

The effect of output in different feedback configuration in the op-amp also needs to be investigated to determine the suitable feedback configuration that fits the purpose of this project.

2.4.1 Positive feedback

In this configuration, the output voltage is routed back to the non-inverting input as shown in Figure 1.

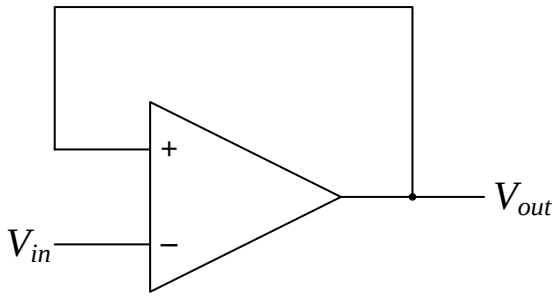


Figure 1 : Positive feedback comparator

In this configuration, the output tends to be in the state that its already in. A slight change in the voltage would not change the output state. The output state only occurs when the voltage is at the most positive or at the most negative input [5]. Therefore, we can say that it *latches* between one of the two states, saturated positive or saturated negative. This condition is known technically as *hysteresis*.

2.4.2 Negative feedback

This configuration is realized by connecting the output with the inverting input as shown in this Figure 4:

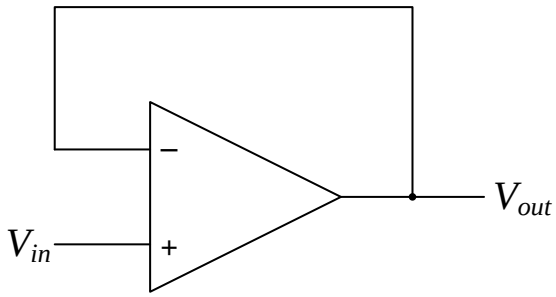


Figure 2: Negative feedback comparator

In this configuration, a voltage follower is created when op-amp is directly connected to the inverting input (-). Any signal voltage that is impressed to the non-inverting input will be seen at the output. With this feedback configuration, the op-amp will always try to drive the output voltage to any differential voltage necessary to make the voltage difference practically zero. It can be concluded that op-amp in this configuration always try to reach a point of equilibrium [6].

2.5 Transistor biasing

Transistors must be properly biased to ensure correct operation. Biasing is commonly consists of resistor networks. There are various ways of biasing transistor including fixed bias, self-bias and combination bias. In the proposed circuit, fixed bias technique is used. Using this bias method, a biasing resistor is connected between the collector supply, R_C and the base, R_B [7]. This is a very simple arrangement and the connection is shown in the Figure 3 below.

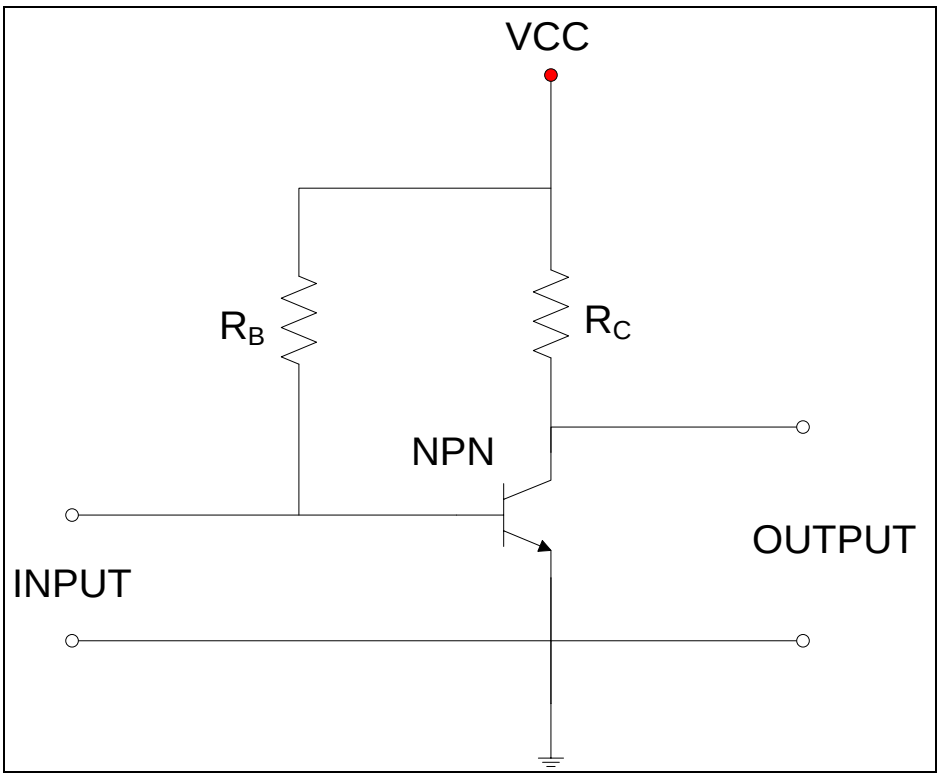


Figure 3 : Fixed biasing diagram

2.6 Common emitter connection

There are three ways that a transistor can be connected in a circuit: Common emitter, common base and common collector [7]. In this proposed circuit, the transistor is connected using common emitter connection. This transistor connection provides amplification of signal in the circuit. It features good voltage, current and power gain sufficient enough for this circuit's purpose. It has low input resistance. The input signal is applied between the base and the emitter, a low resistance and low current circuit. When the input signal goes to positive values, the base goes to positive values, decreasing the forward bias hence reducing the corrector current and increases the collector voltage. The collector current that flows through the high resistance reversed bias junction also flows through a high resistance load resulting in high level of amplification. The output signal goes negative when the input signal goes positive. The connection is shown in Figure 4 below.

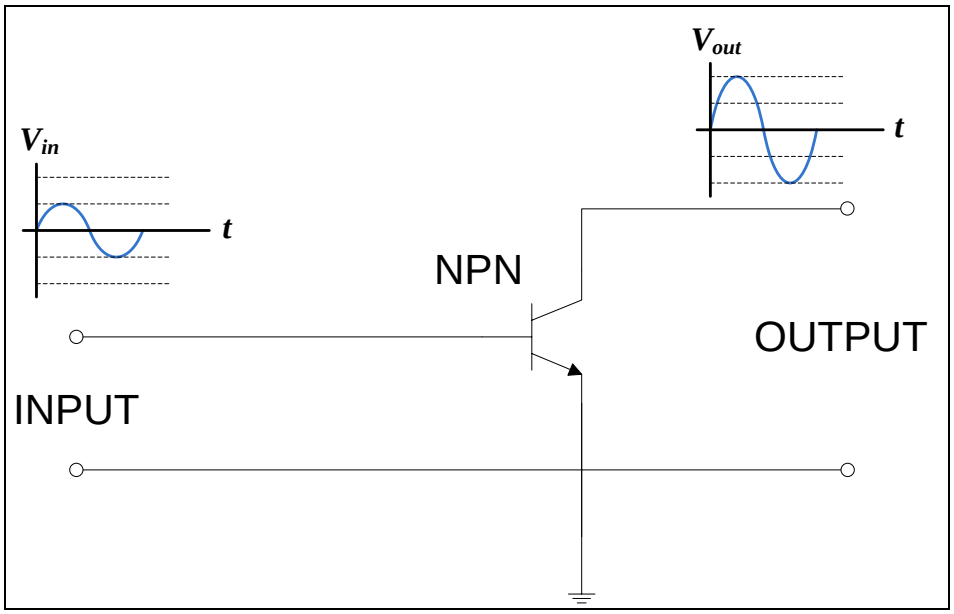


Figure 4 : Amplification using common emitter connection

The amplification amount is called Gain. It is the ratio of the output over the input. Different value of gain is obtained with different transistor configurations although the same transistor is used. The selection of configuration to be selected is subject to the type of application. The current gain, β or also expressed as h_{FE} in the common emitter connection is the relationship of collector current to base current as expressed in (5) below [8]:

$$h_{FE} = \beta = \frac{\Delta I_C}{\Delta I_B} \tag{5}$$

Resistance gain, R is the ratio of output resistance and input resistance as expressed in (6) below:

$$R = \frac{R_{out}}{R_{in}} \tag{6}$$

Voltage gain, E is the sum of current gain, β multiplied by resistance gain, R as expressed in (7) below:

$$E = \beta \times R \tag{7}$$

Power gain, P is the sum of current gain, β multiplied by voltage gain, E as described in (8) below:

$$P = \beta \times E \tag{8}$$

2.7 Creation of PWM signal

To create PWM signal, the sawtooth waveform as modulation signal and DC sine waveform as reference signal are fed to the comparator as shown in Figure 5.

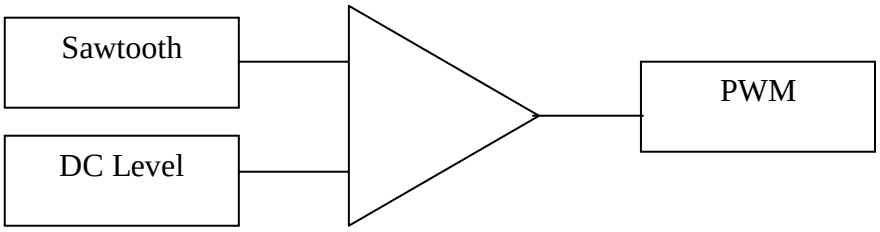


Figure 5 : PWM generator block diagram

This method is called intersective method [9]. When the value of DC reference signal (**green**) is greater than the sawtooth modulation signal (**red**) the PWM signal (**blue**) is in high state as shown in Figure 6. When the DC reference signal value is smaller than the sawtooth modulation signal, the PWM signal enters the low state. It is noted that the duty cycle width is determined by the reference voltage V_{ref} of the DC level signal.

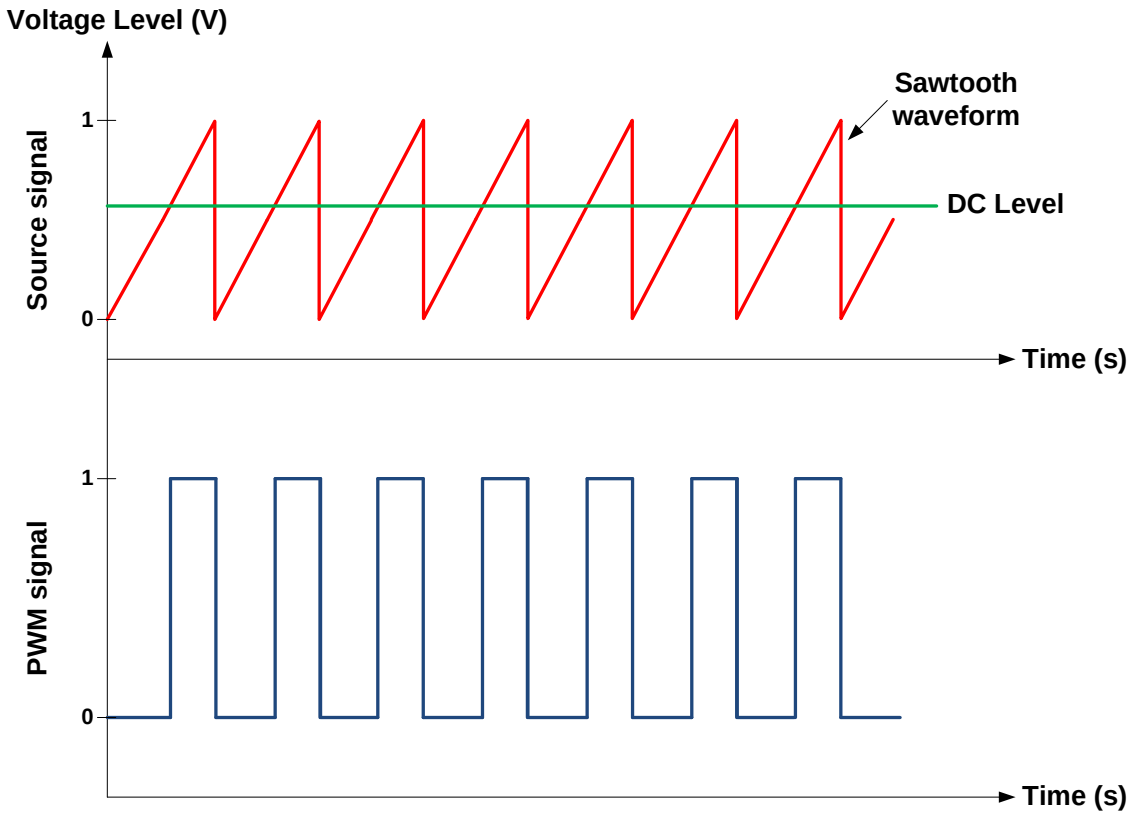


Figure 6: Source signal and PWM signal graph

2.8 Rise time and fall time

In practical application, the PWM signal is not perfectly a square wave. It will take some time to change from one voltage level to another known rise time, t_r and fall time, t_f. Rise time, t_r is the difference between the time when the signal crosses a low state to the time when the signal crosses the high state while fall time, t_f is the difference between the time when the signal crosses a high state to the time when the signal crosses the low state [10]. This can be represented in Figure 7 below.

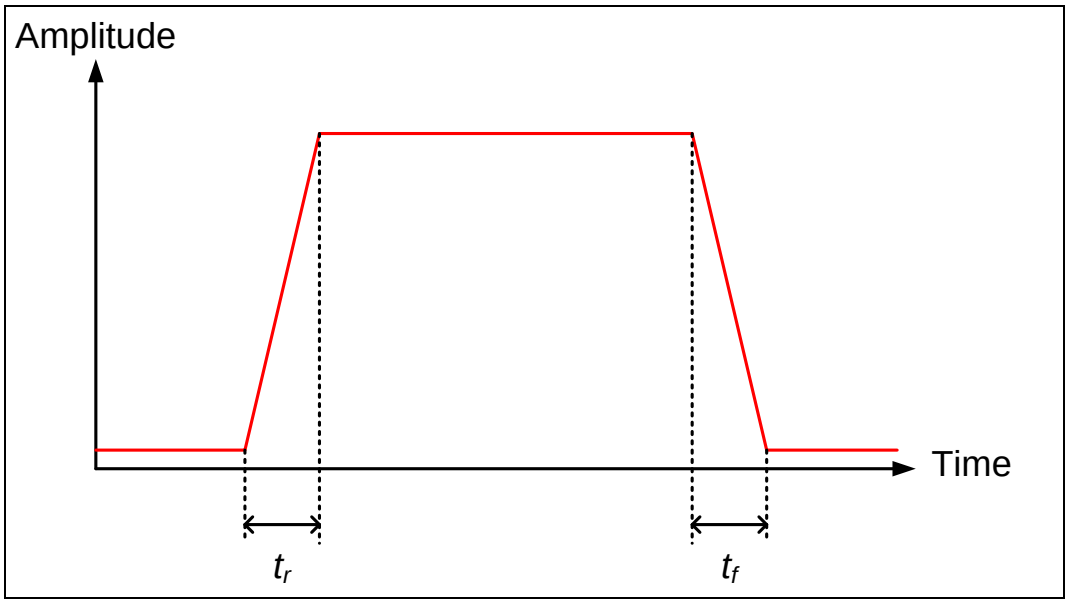


Figure 7 : Rise time and fall time in PWM signal.

2.9 Resolution of PWM signal

From rise time and fall time, the resolution of PWM signal can also be determined. The resolution of the signal determines the quality of the signal [11]. Resolution is the time taken between the 10% and 90% point of the rise time as shown in Figure 8 below.

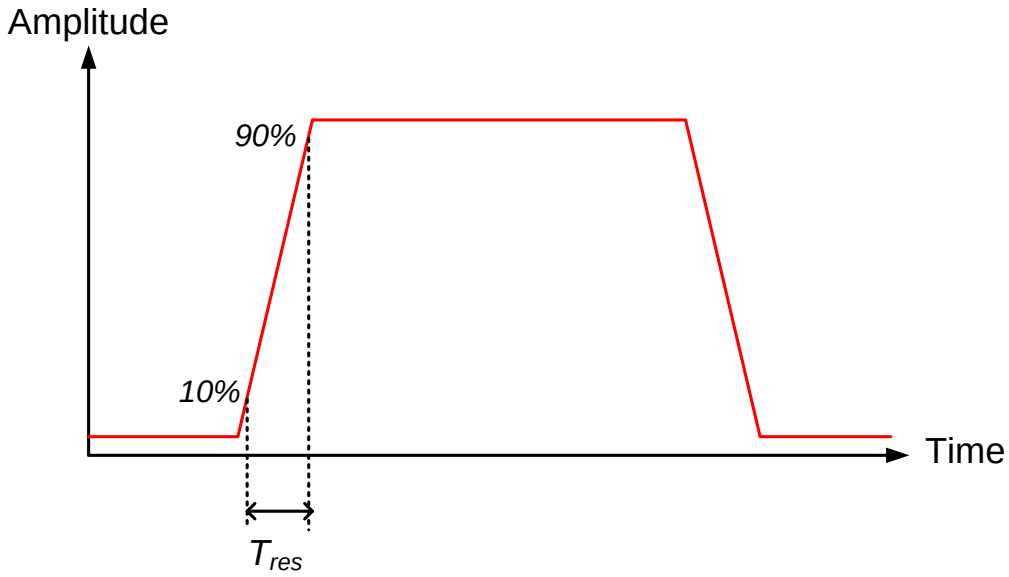


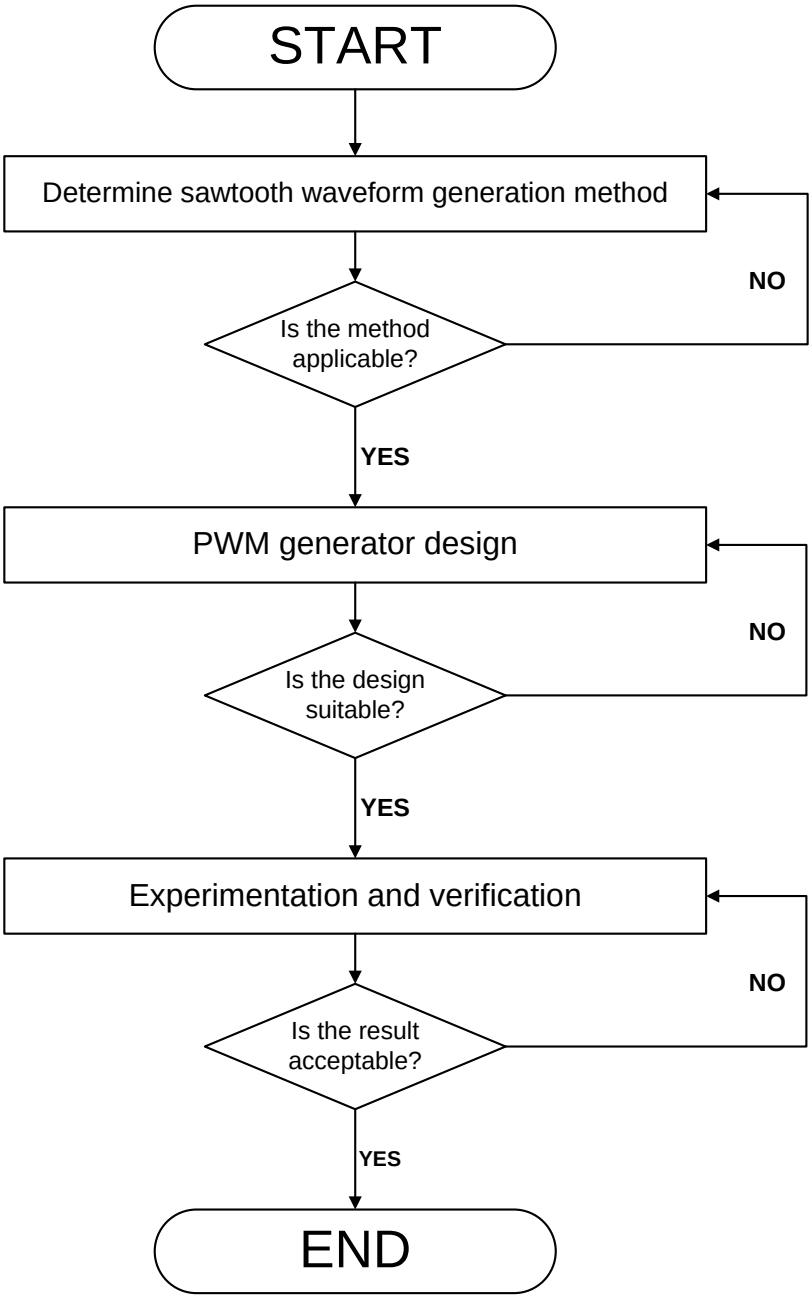
Figure 8 : Determining resolution of a PWM signal

Resolution is expressed in nanoseconds (ns). Smaller time (in nanoseconds) will give better resolution to the signal. In high frequency PWM, the resolution will be measured to determine the performance of PWM signal generation using intersective method at 1 MHz frequency.

CHAPTER 3

METHODOLOGY

3.1 Process Flowchart



3.2 Required Hardware

In this experimentation, the hardware is needed to build the related circuits for analysis and testing purposes.

Table 1 : Required hardware and software

Hardware	Functions / Use
Voltage comparator (operational amplifier)	Compares sawtooth waveform input with DC level reference voltage to generate PWM signal.
Function generator	Produces needed waveform and signal for experimentation activities.
Oscilloscope	Captures the waveform in the circuit for analysis.
Digital Multimeter (DMM)	To take important readings (voltage, current, resistance etc.) on the physical circuit.
Printed Circuit Board (PCB)	Provide mean of building a circuit and customize it when needed.

3.3 Components and Tools

3.3.1. Comparator

As for comparator, MAX944 is the component of choice [12]. The advantage of this comparator is it uses single supply thus reducing the circuit complexity. This IC houses for comparators that is suitable for generating multiple PWM signal. The basic specifications are as follows:

Supply voltage : 2.7V – 6.0V

Input voltage range : -0.2V to +0.2V

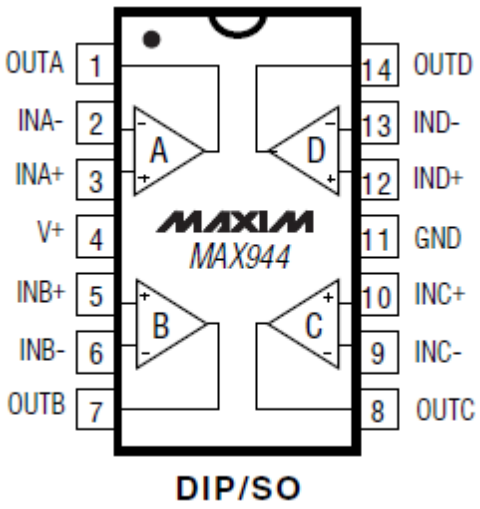


Figure 9: MAX944 pin layout [12]

3.3.2. Transistor Characteristics

For amplification purposes, the circuit uses PN2222A, NPN general purpose amplifier. This component can be used as a medium power amplifier for the circuit [13]. The important electrical characteristics are as follows:

Table 2 : On characteristics of PN2222A NPN transistor

Symbol	Parameter	Test condition	Min.	Max.	Units
h_{FE}	DC Current Gain	IC = 0.1mA, VCE = 10V	35		
		IC = 1.0mA, VCE = 10V	50		
		IC = 10mA, VCE = 10V	75		
		IC = 10mA, VCE = 10V, (Ta = -55°C)	35		
		IC = 150mA, VCE = 10V *	100	300	
		IC = 150mA, VCE = 10V *	50		
		IC = 500mA, VCE = 10V *	40		
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	IC = 150mA, VCE = 10V		0.3	V
		IC = 500mA, VCE = 10V		1.0	V
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	IC = 150mA, VCE = 10V	0.6	1.2	V
		IC = 500mA, VCE = 10V		2.0	V

3.3.3. Sawtooth Generation

For the first attempt to generate sawtooth waveform, a circuit has been built as shown in Figure 10 below [14]:

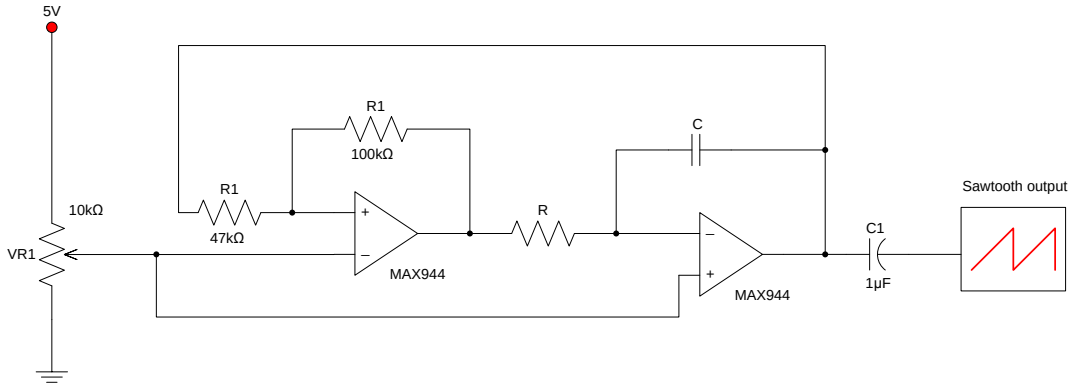


Figure 10 : Sawtooth generator circuit

The oscillation frequency of the triangle wave by choosing the suitable *R* and *C* values and they are related by equation 9:

$$f_{osc} = \frac{1}{2 \times R \times C} \tag{9}$$

However, it is difficult to precisely tune the circuit at 1 MHz. This is due to there are no component with correct value available and tolerance in resistor. The resistors actual values are measured using digital multimeter first to investigate the effect of component values to the frequency. The *R* and *C* value combinations are shown in Table 3.

Table 3 : Capacitor value combinations and observed oscillation frequency

Capacitor, *C* value (F)	**Actual Resistor, *R* value (Ω)**	**Actual Frequency, *F* (Hz)**
1 nF	500.00 Ω	970.874 kHz
4.7 nF	106.38 Ω	1.063 MHz
220 pF	2.40 kΩ	946.97 kHz
330 pF	1.515 kΩ	1.0101 MHz
470 pF	1.063 kΩ	1.0638 MHz

To simplify the process and reduce the variations in oscillation frequency of the sawtooth wave, the wave is derived from a function generator that is able to provide more precise waveform with the desired frequency of 1 Mhz. This function generator will replace the circuit above and will be used throughout the project onwards.

3.3.4. PWM Generator Circuit

This circuit as shown in Figure 11 below has been constructed to derive PWM signal for this project's purposes [15].

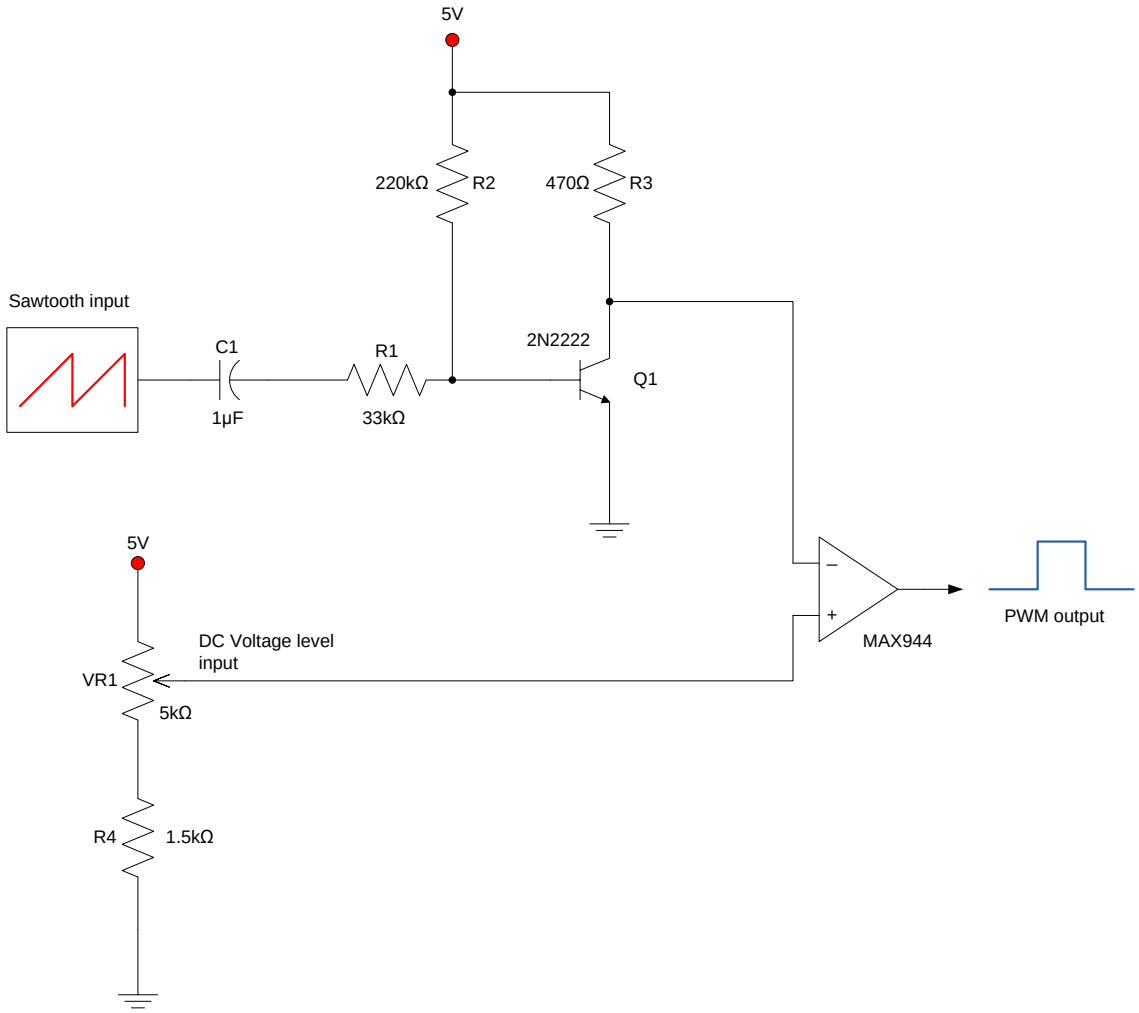


Figure 11: PWM generator circuit schematic

The required PWM signal for this experimentation is 20% - 90% duty cycle at frequency of 1000 kHz (1 MHz). The frequency of the signal is controlled by the frequency of the sawtooth wave input from the function generator. To make sure

that sawtooth signal is fully detected by the reference signal, capacitor C_1 and resistor R_1 is added to shift up a bit the sawtooth waveform. This is to ensure that this circuit can generate PWM signal with duty ratio from 30% to 70%. The power delivered by the PWM is heavily influenced by the power supplied (V_{CC}=5V) to the circuit and PWM duty ratio, D as shown in (10) below:

$$P_{delivered} = V_{CC} \times D \tag{10}$$

The duty ratio can also be expressed by the ON time, t_{on} over the period of the function, T_s as shown in (11):

$$D = \frac{t_{on}}{T_s} = \frac{V_{DC}}{V_{sawtooth}} \tag{11}$$

This circuit amplifies the signal a bit using 2N2222 NPN transistor connected in common emitter configuration. The current gain, β for this transistor is 75 is a ratio between current in collector, I_C and base current I_B (12).

$$\beta = \frac{I_C}{I_B} \tag{12}$$

The determination of resistor at the base, R_2 and resistor at the load, R_3 are as follows (13) and (14):

$$R_2 = \frac{V_B - V_{BE}}{I_B} \tag{13}$$

$$R_3 = \frac{V_{CC} - V_{CE}}{I_C} \tag{14}$$

It is noted that rectangular pulse is inverse to the sawtooth waveform. However, since this transistor is an inverting amplifier, the PWM signal produced is not inverted. For controlling DC reference signal, voltage divider circuit is used. The amount of DC voltage is related by equation (15) below:

$$V_{DC} = \frac{V_{CC} \times R_4}{VR_1 + R_4} \tag{15}$$

Resistor R_4 is connected before ground to prevent DC voltage from falling too much under the bottom edge of the shifted sawtooth signal. By doing this, the whole range of potentiometer *VR1* will have active influence on PWM duty cycle. Hence, PWM duty ratio is set by adjusting the potentiometer *VR1* in the circuit.

CHAPTER 4

RESULTS AND DISCUSSIONS

4.1 PWM waveform in various frequencies

To determine the frequency operation of this PWM generator circuit, the frequency of sawtooth waveform is varied by adjusting frequency knob of the function generator. The duty cycle is fixed at 50 % to compare the quality of PWM signal generated at different frequency. It is observed that the higher the frequency, the signal is more susceptible to noise as shown in these figures below.

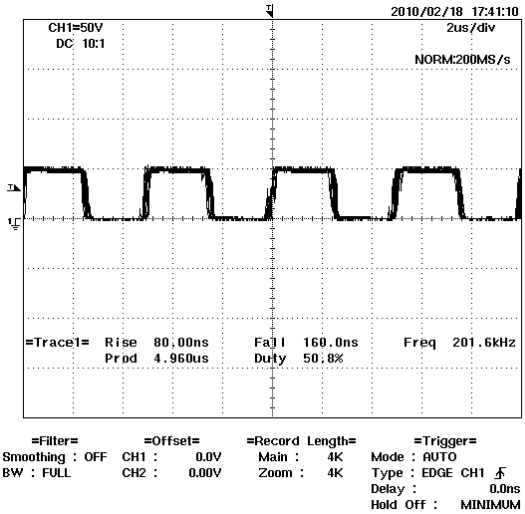


Figure 12 : 50 % duty cycle PWM signal at 200 kHz

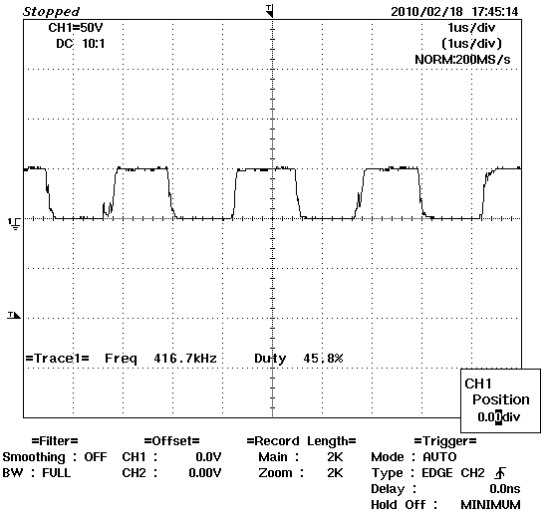


Figure 13 : 50 % duty cycle PWM signal at 400 kHz

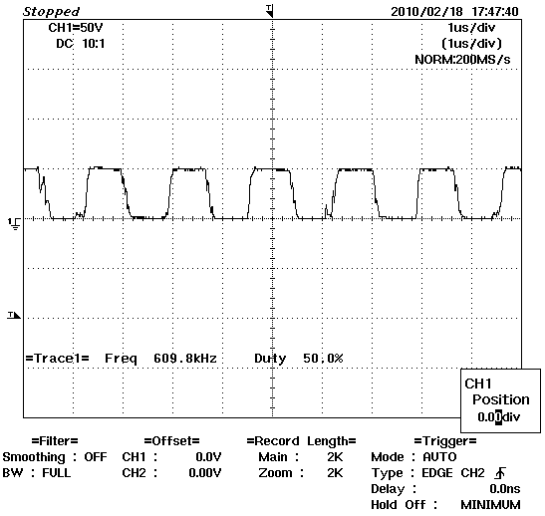


Figure 14 : 50 % duty cycle PWM signal at 600 kHz

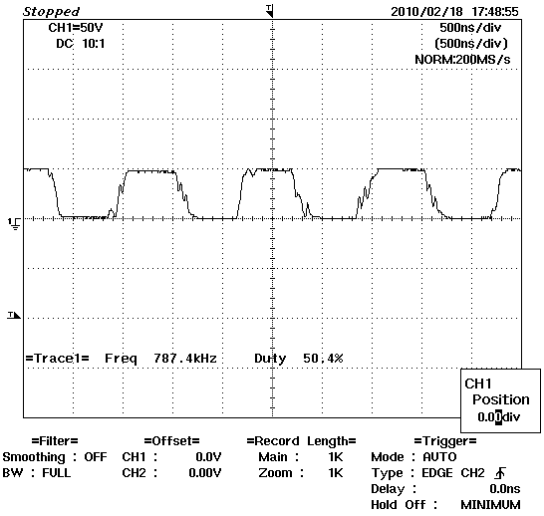


Figure 15 : 50 % duty cycle PWM signal at 800 kHz

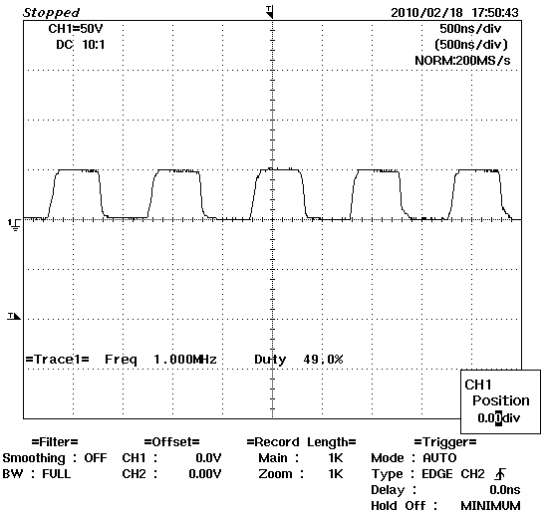


Figure 16 : 50 % duty cycle PWM signal at 1000 kHz (1 MHz)

The frequency of each 50 % duty cycle PWM signal and its respective peak voltages are recorded in Table 4 below:

Table 4 : Frequency and Peak Voltage for 50 % Duty Cycle PWM

Frequency, *f* (kHz)	**Peak Voltage, V_{pk} (V)**
200 kHz	50 V
400 kHz	50 V
600 kHz	50 V
800 kHz	50 V
1000 kHz (1 MHz)	50 V

From Table 4, it is observed that the circuit is able to generate PWM signal with 50 % duty cycle from frequency of 200 kHz up to 1 MHz and maintaining the same peak voltage. This shows that the generator circuit can maintain the same peak voltage within that frequency range.

4.2 PWM waveform of 1 MHz frequency with varying duty cycles

To determine performance of this PWM generator circuit at 1 MHz frequency, the duty cycle is varied by changing the value of DC level voltage. This is done by adjusting the resistance value of potentiometer *VR1* in the circuit. The duty cycle is varied from 20 % to 90 % to compare the quality of PWM signal generated at different duty cycles. It is observed that the PWM signal is less susceptible to noise when the duty cycle is between 30 % to 70 %. The rise time and fall time of each signal is also recorded.

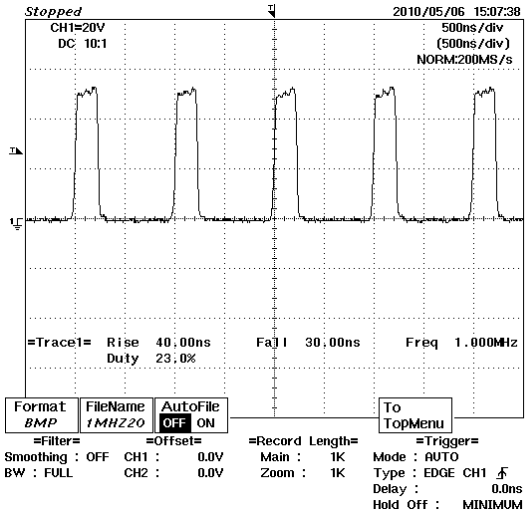


Figure 17 : 1 MHz PWM with 20 % duty cycle

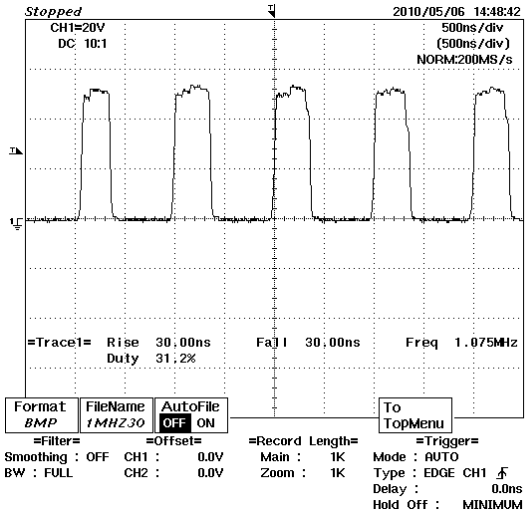


Figure 18 : 1 MHz PWM with 30 % duty cycle

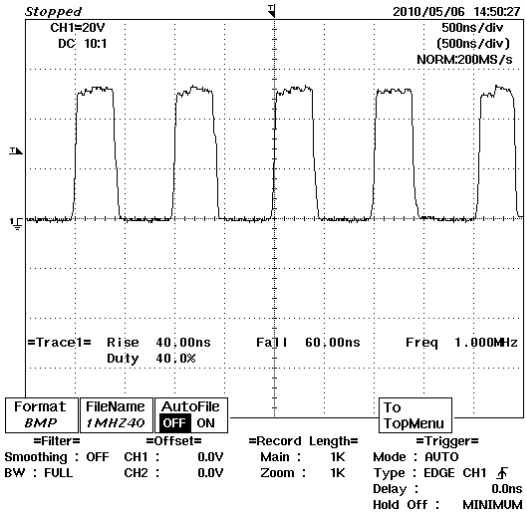


Figure 19 : 1 MHz PWM with 40 % duty cycle

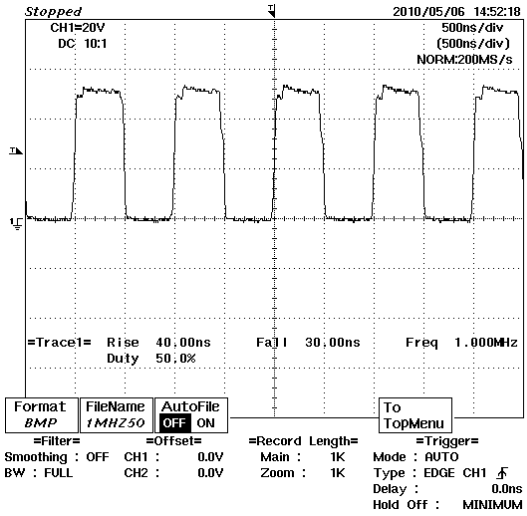


Figure 20 : 1 MHz PWM with 50 % duty cycle

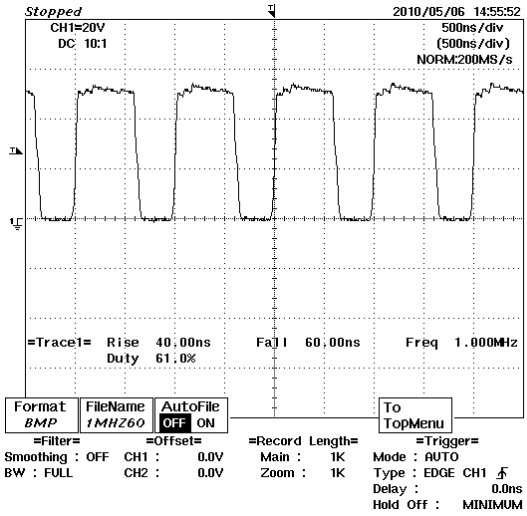


Figure 21 : 1 MHz PWM with 60 % duty cycle

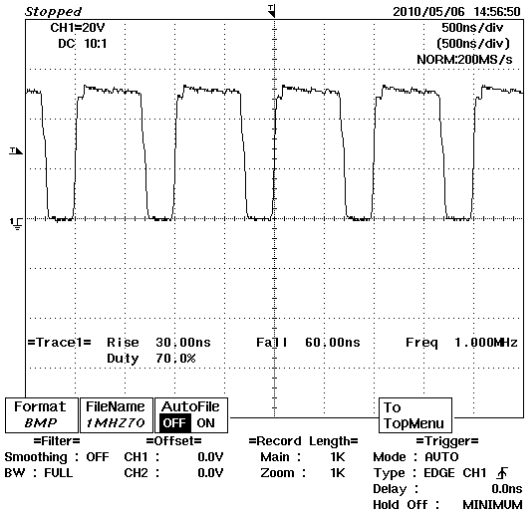


Figure 22 : 1 MHz PWM with 70 % duty cycle

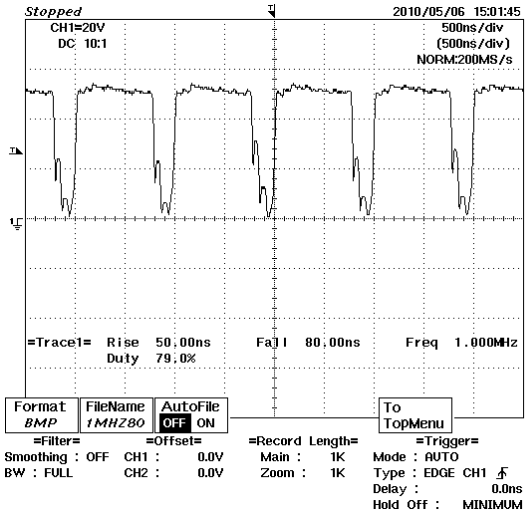


Figure 23 : 1 MHz PWM with 80 % duty cycle

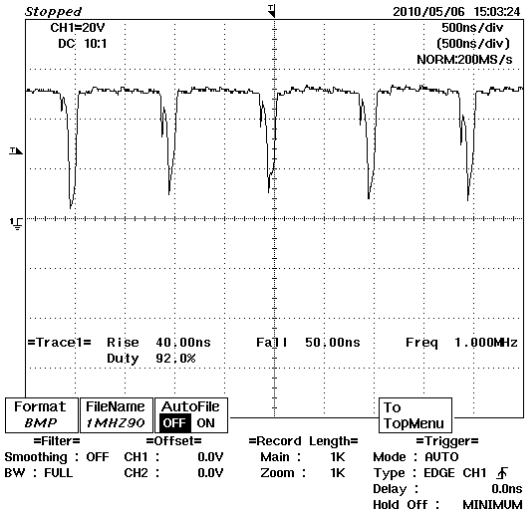


Figure 24 : 1 MHz PWM with 90 % duty cycle

The rise time, fall time and average peak voltage at every duty cycle is recorded in Table 5 below:

Table 5 : Rise time, fall time and average peak voltage of 1 MHz PWM signal at different duty cycles

Duty Cycle (%)	**Rise time, t_r (ns)**	**Fall time, t_f (ns)**	**Average Peak Voltage, V_{pk} (V)**
20 %	40.00 ns	30.00 ns	48 V
30 %	30.00 ns	30.00 ns	48 V
40 %	40.00 ns	60.00 ns	48 V
50 %	40.00 ns	30.00 ns	48 V
60 %	40.00 ns	60.00 ns	48 V
70 %	30.00 ns	60.00 ns	48 V
80 %	50.00 ns	80.00 ns	48 V
90 %	40.00 ns	50.00 ns	48 V

From Table 5, the average rise time is 38.75 ns and average fall time is 50.00 ns. However, the average peak voltage is maintained at 48 V in each duty cycles. The best range of operation of this PWM generator circuit is from 30 % to 70 % duty cycle at 1 MHz because the rise time shows little variation in this range.

4.3 Resolutions of PWM signals

The resolution of 1 MHz PWM signals at various duty cycles are also recorded as shown in these figures below. The resolution of PWM signals generated is acceptable and the best resolution and low noise combination is observed between 30 % and 70 % duty cycle. This shows that the lower the signal noise, the better the resolution. The signal resolutions are also listed in the Table 6 below.

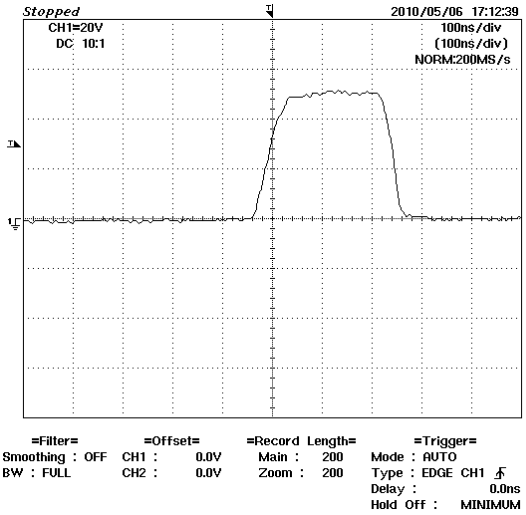


Figure 25: Resolution of 20 % duty cycle 1 MHz PWM

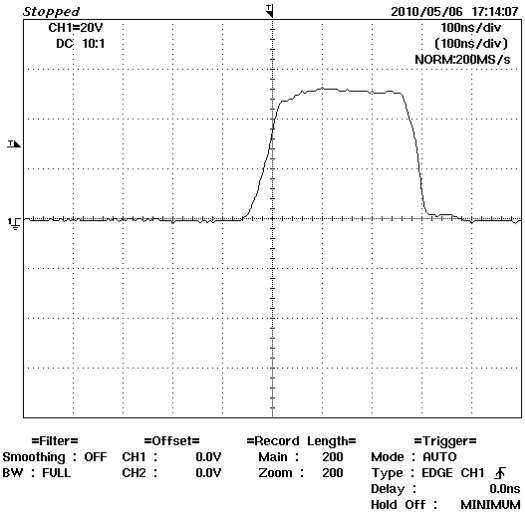


Figure 26 : Resolution of 30 % duty cycle 1 MHz PWM

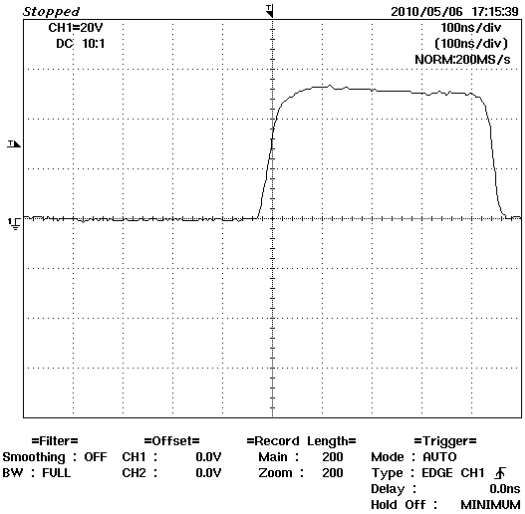


Figure 27 : Resolution of 40 % duty cycle 1 MHz PWM

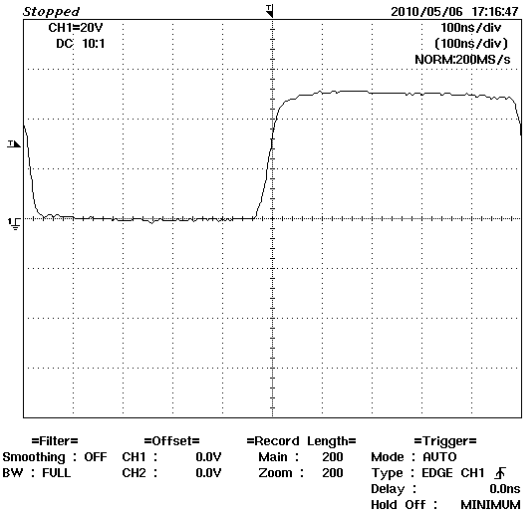


Figure 28 : Resolution of 50 % duty cycle 1 MHz PWM

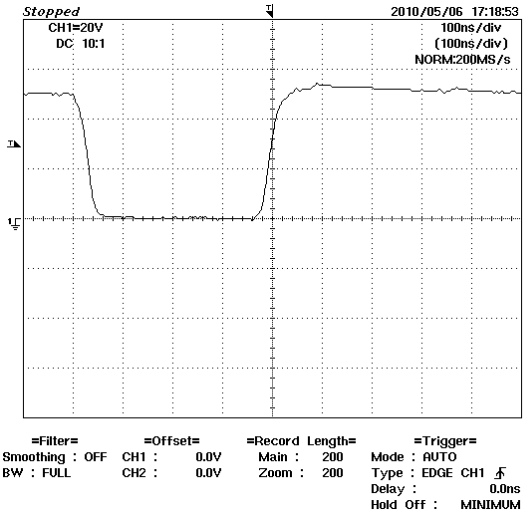


Figure 29 : Resolution of 60 % duty cycle 1 MHz PWM

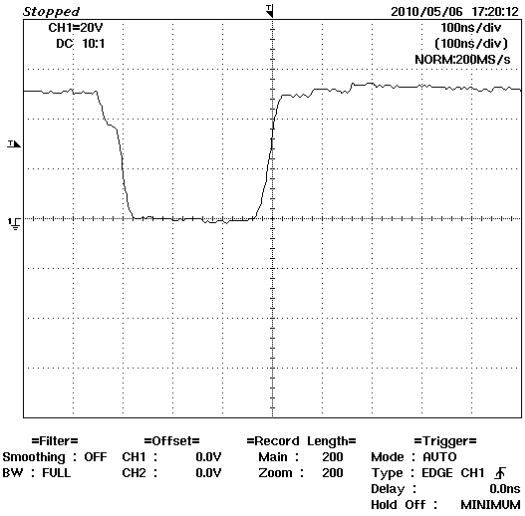


Figure 30 : Resolution of 70 % duty cycle 1 MHz PWM

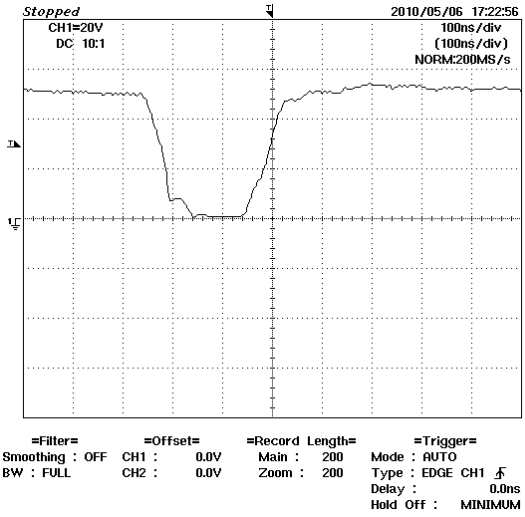


Figure 31 : Resolution of 80 % duty cycle 1 MHz PWM

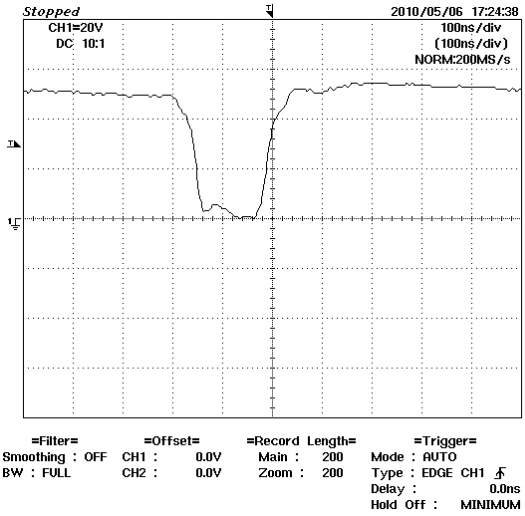


Figure 32 : Resolution of 90 % duty cycle 1 MHz PWM

The PWM signal resolutions are recorded in Table 6 below:

Table 6 : 1 MHz PWM signal resolutions at different duty cycles

Duty Cycle	**Resolution (ns)**
20 %	0.30 div × 100 ns/div = **30 ns**
30 %	0.40 div × 100 ns/div = **40 ns**
40 %	0.20 div × 100 ns/div = **20 ns**
50 %	0.20 div × 100 ns/div = **20 ns**
60 %	0.20 div × 100 ns/div = **20 ns**
70 %	0.18 div × 100 ns/div = **18 ns**
80 %	0.40 div × 100 ns/div = **40 ns**
90 %	0.30 div × 100 ns/div = **30 ns**

The average resolution for 1 MHz PWM signal at different duty cycles as computed from Table 6 is 27.25 ns. From the resolution table, it is observed that from 40 % to 70 % duty cycle, the resolution is the most consistent.

CHAPTER 5

CONCLUSION AND RECOMMENDATION

In general, the attempt to generate PWM signal at 1 MHz had been successful with certain limitation. At low frequency, from 200 kHz to 600 kHz, the circuit is less susceptible to noise. It is observed that the circuit is not fully capable of varying the duty cycle very much at 1 MHz. The best PWM that the circuit can generate is in the range of 30 % to 70 % duty cycle at 1 MHz frequency. This capability is sufficient enough for driving power MOSFETs in power electronic converters (buck/boost converter). Very wide duty cycle range is not really needed as the variation of duty cycle is minimal. This is the most demanding application that requires high frequency operation. However, this circuit had at least surpassed the capability of some PWM chips found in the market. PWM chip in the market had two limitations. The first limitation is the operating frequency is not as high as 1 MHz although the range of duty cycle it can operate is high (from 0 % to 100 %). Second limitation is the narrow duty cycle range of PWM available although been able to operate at 1 MHz. This circuit had addressed to this limitation better by providing wider duty cycle range and the ability to operate at high frequency (1 MHz).The comparison can be observed in Table 7 [16][17][18]:

Table 7 : Comparison of different PWM generation methods

PWM Generation Method	Frequency	Duty Cycle
PWM Generator Circuit	0 kHz – 1000 kHz (1 MHz)	20 % – 90 %
TL494 chip	10 kHz	0 % – 45 %
UC3823A chip	0.9 MHz – 1.1 MHz	< 100 %
SG3526 chip	1 kHz – 400 kHz	0 % – 45 %

The circuit's performance can be better by revising and modifying the original circuit construction. In this circuit, the transistor is biased using fixed-bias. The arrangement is very simple in this type of bias but carries a heavy withdraw [19]. This type of bias is very sensitive to variation in temperature. The DC operating point or quiescent point (Q-point) will change from change in ambient temperature or from current flow within the transistor. The change in Q-point is undesirable because it affects the amplification gain and may result into distortion on the output signal. The suggested biasing for this circuit is by using combination bias [20]. This configuration combines fixed and self bias type of transistor biasing. Using this configuration, the stability of transistor operation can be improved and the limitations on other configurations are overcome. For sensitive high frequency PWM, operation it is recommended to use PWM function generator despite the limited availability of such devices. The use of PWM generator chip is recommended if PWM duty cycle variation is not really needed. However, the circuit used in this project is an average performer due to its wide frequency and duty cycle range. It is suitable for testing purposes where acquiring of those PWM chips and PWM function generator is not possible.

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APPENDICES

APPENDIX A

MAX944 HIGH-SPEED, LOW-POWER, 3V/5V, RAIL-TO-RAIL, SINGLE SUPPLY COMPARATORS DATA SHEET

APPENDIX B

PN2222A NPN GENERAL PURPOSE AMPLIFIER DATA SHEET

APPENDIX C

TL494 PULSE-WIDTH-MODULATION CONTROL CIRCUITS DATA SHEET

APPENDIX D

UC3823A HIGH-SPEED PWM CONTROLLER DATA SHEET

APPENDIX E

SG3526 PULSE WIDTH MODULATION CONTROL CIRCUIT DATA SHEET