STUDY OF ASDT DRIVE FOR THREE PHASE LOAD

Study Of IGBT Drive For Three Phase Load

By

Mohd Khairul Hanafi Bin Mhd Jamin

Dissertation Report submitted in partial fulfillment of
the requirements for the
Bachelor of Engineering (Hons)
(Electrical & Electronics Engineering)

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CERTIFICATION OF APPROVAL

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Approved by:

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TRONOH, PERAK

Jun 2010

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

MOHD KHAIRUL HANAFI BIN MHD JAMIN

ABSTRACT

This dissertation discusses the project, "Study of IGBT drive three for three phase load". This project deals with the IGBT theory, the three phase inverter and the gate driver characteristics. The objective of this project is to study and simulate the IGBT drive for the three phase load. This report also describe the hardware description that were used in this project that is the SEMIKRON SKiiP 39ACT4V1 Three-phase Bridge Rectifier and the SEMIKRON SKHI 23/12 (R) Driver. The methodology chapter explained the procedures of handling the project, starting from the problem statement until the procedure identification. It also lists out the tools and equipments needed to execute this project. The last chapter discusses the summarized information of the overall project. Throughout of this project, the author had deal with the new software and work with a lot of people. Some information in this report had been taken from other source and all had been credited in the reference.

ACKNOWLEDGEMENTS

First and foremost the author would like to take this opportunity to express his appreciation to all the parties that is involved in making Final Year Project (FYP) a success. The undergoing of this project would have not been possible without the assistance and guidance of certain individuals and organization whose contributions have helped in its completion.

The author would like to express his deepest appreciation to his project supervisor, Mr. Saiful Azrin Bin Mohd Zulkifli for his endless support, guidance and consultation regarding this project throughout the year.

Special thanks to lab technologist; Mdm. Siti Hawa who has given countless technical support to the author in providing both advice and components, hardware, or software the author requires in completion of the project and also Mr. Isnani who had given technical support during the fabricating process.

Last but not least, the author would like to give out her thanks to all those who have contributed directly or indirectly to the success of this project.

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CHAPTER 1

INTRODUCTION

1.1 Background Of Study

The insulated gate bipolar transistor or IGBT is a three-terminal power semiconductor device, noted for high efficiency and fast switching [1].Nowadays, IGBT has been widely use in the power electronics application. It switches electric power in many modern appliances: electric cars, variable speed refrigerators, air-conditioners, and even stereo systems with switching amplifiers.

This project focuses on the application of the IGBTs as the inverter for the three-phase output system. In conjunction with that, this project also focusing on the gate driver characteristic that will drives the IGBTs gate to switch and implement it on the testing.

1.2 Problem Statement

In order to operate a three phase load, an AC power supply is needed to supply the load. Therefore, an inverter is needed to convert the DC supply to the AC if the user desired to produce a three-phase output from the single phase supply.

Current control is often used to improve the performance and reliability for the motor drives. A common type for a current control is consisting MOSFETs and it is not capable of conducting a high DC voltage. By implementing the IGBT on the current control, a higher level of DC voltage can be applied to the drive.

1.3 Objectives

The objective of this project is to study the characteristic of the IGBT gate drive to the three phase output. Cost will be minimized to achieve minimal expenses throughout project.

There are a few objectives need to be achieved by the end of project completion:

1. To study and familiarize with off-the-shelf IGBTs drive.
2. To design and configure required interfacing from drive to the PXI controller.
3. To build IGBT inverter by using individual IGBTs pairs and the gate driver.
4. To consider incorporate additional functionality such as overcurrent and overvoltage protection to the circuitry.
5. To incorporate protection functions monitoring of IGBT drive (e.g. overvoltage / over-current) using NI LabVIEW (software programming and configuration)
6. To test and commission IGBT inverter to the motor.

CHAPTER 2

LITERATURE REVIEW

2.1 Insulated-Gate Bipolar Transistor (IGBT)

2.1.1 Introduction of IGBT

The insulated gate bipolar transistor or IGBT is a three-terminal power semiconductor device. IGBT is well known for high efficiency and fast switching period. IGBT acts as electric power switches and widely use electric cars, variable speed refrigerators, air-conditioners, and even stereo systems with switching amplifiers. [2]

The IGBT combines the simple gate-drive characteristics of the MOSFETs with the high-current and low–saturation-voltage capability of bipolar transistors by combining an isolated gate FET for the control input, and a bipolar power transistor as a switch, in a single device.

The IGBT is used in medium- to high-power applications such as switched-mode power supply, traction motor control and induction heating. Large IGBT modules typically consist of many devices in parallel and can have very high current handling capabilities in the order of hundreds of amps with blocking voltages of 6,000 V [3].

The IGBTs combines the positive attributes of Bipolar Junction Terminal (BJTs) and MOSFETs. BJTs have lower conduction losses in the on-state, especially in devices with larger blocking voltages, but have longer switching times, especially at turn-off while MOSFETs can be turned on and off much faster, but their on-state conduction losses are larger, especially in devices rated for higher blocking voltages. Hence, IGBTs has lower on-state voltage drop with high blocking voltage capabilities in addition to fast switching speeds.[3]

IGBT has a vertical structure as shown in Figure 2 below. This structure is quite similar to that of the vertical diffused MOSFET except for the presence of the p+ layer that forms the drain of the IGBTs.

This layer forms a pn junction (labeled J1 in the Figure 2), which injects minority carriers into what would appear to be the drain drift region of the MOSFET. The gate and source of the IGBTs are laid out in interdigited geometry similar to that used for the vertical MOSFET.

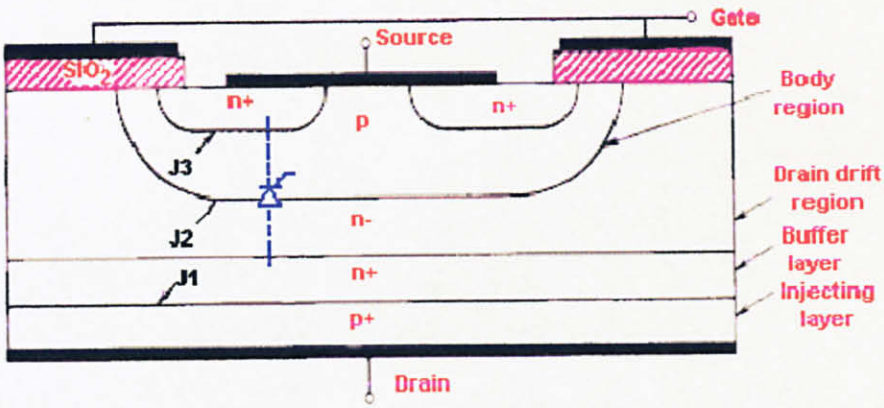


Figure 1: Physical structure of an IGBT

The IGBT structure shown in Figure 2 has a parasitic thyristor, which could latch up in IGBTs if it is turned on.The n+ buffer layer between the p+ drain contacts and the n+ drift layer, with proper doping density and thickness, can significantly improve the operation of the IGBTs in two important respects.

It can lower the on-state voltage drop of the device and shorten the turn-off time. On the other hand, the presence of this layer greatly reduces the reverse blocking capability of the IGBTs.

2.1.2 IGBT Switching Characteristics.

An important performance feature of any semiconductor-switching device is its switching characteristics. User must really understand this characteristic. By having understanding this device switching characteristics, user can improve its utilization in the various applications.

The main performance switching characteristics of power semiconductor switching devices are the turn-on and turn-off switching transients in addition to the safe operating area (SOA) of the device

Since most loads are inductive in nature, which subjects devices to higher stresses, the turn-on and turn-off transients of the IGBTs are obtained with an inductive load test circuits as shown in Figure 4 below.

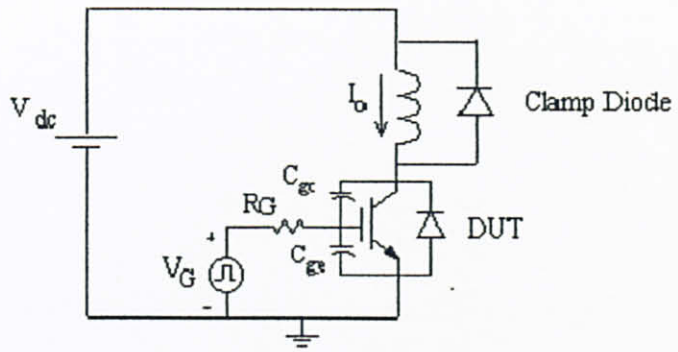


Figure 2: Inductive load test circuit

The load inductance is assumed to be high enough so as to hold the load current constant during switching transitions. The freewheeling clamp diode is required to maintain current flow in the inductor when the device under test is turned off.

2.1.3 Turn-on Transients

The turn-on switching transients of IGBT are very similar to MOSFET since the IGBT is essentially acting as a MOSFET during most of the turn-on interval.

With gate voltage applied across the gate to emitter terminals of the IGBTs, the gate to emitter voltage rises up in an exponential fashion from zero to $V_{GE(th)}$ due to the circuit gate resistance (R_G) and the gate to emitter capacitance (C_{ge}). The Miller effect capacitance (C_{gc}) effect is very small due to the high voltage across the device terminals.[3]

Beyond $V_{GE(th)}$, the gate to emitter voltage continues to rise as before and the drain current begins to increase linearly as shown above. Due to the clamp diode, the collector to emitter voltage remains at Vdc as the IGBTs current is less than Io.

The gate to emitter voltage becomes temporarily clamped to VGE, Io. This means that the voltage required the IGBT current at Io. At this stage, the collector to emitter voltage starts decreasing in two distinctive intervals t_{fv1} and t_{fv2}.

The first time interval corresponds to the traverse through the action region while the second time interval corresponds to the completion of the transient in the ohmic region. During these intervals, the Miller capacitance becomes significant where it discharges to maintain the gate to source voltage constant.

When the Miller capacitance is fully discharged, the gate to emitter voltage is allowed to charge up to VG and the IGBT goes into deep saturation. The resultant turn on switching losses are shown in equation below:

The on energy loss is approximately estimated via this equation:

$$Eon = \frac{Vdc\ Io}{2} ton$$

where,

Eon = the on energy loss

Vdc = DC Voltage

Io = Current

2.1.4 *Turn-off Transients*

When a negative gate signal is applied across the gate to emitter junction, the gate to emitter voltage starts decreasing in a linear fashion. Once the gate to emitter voltage drops below the threshold voltage ($V_{GE(th)}$) , the collector to emitter voltage starts increasing linearly.

The IGBTs current remains constant during this mode since the clamp diode is off. When the collector to emitter voltage reaches the dc input voltage, the clamp diode starts conducting and the IGBTs current falls down linearly.

The rapid drop in the IGBT current occurs during the time interval tfi1, which correspond to the turn-off of the MOSFET. The tailing of the collector current during the second interval tfi2 is due to the stored charge in the n-drift region of the device.

This is due to the fact that the MOSFET is off and there is no reverse voltage applied to the IGBTs terminals that could generate a negative drain current so as to remove the stored charge.

The only way for stored charge removal is by recombination within the n-drift region. Since it is desirable that the excess carrier's lifetime be large so as to reduce the on-state voltage drop, the duration of the tail current becomes long.

This will result in additional switching losses within the device. This time increases also with temperature similar to the tailing effect in BJTs. A trade off between the on-state voltage drop and faster turn-off times must be made.

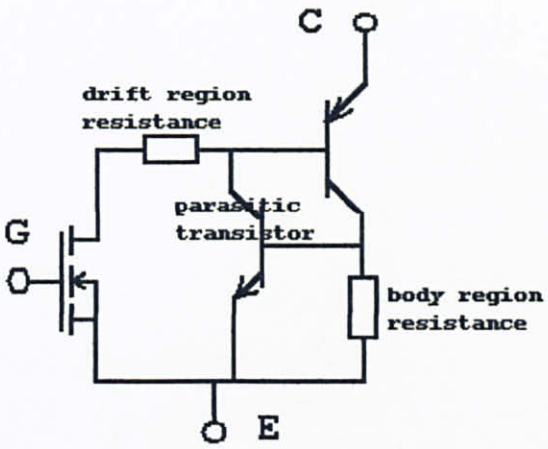


Figure 3: Equivalent circuit of the IGBTs

The removal of stored charge can be greatly enhanced with the addition of a n+ buffer layer, which acts as a sink for the excess holes and significantly shortens the tail time.

This layer has a much shorter excess carrier life time which results in a greater recombination rate within this layer. The resultant gradient in hole density in the drift region causes a large flux of diffusing holes towards the buffer region which greatly enhances the removal rate of holes from the drift region and shortens the tail time.[3]

This structure is referred to as Punch-Through (PT) IGBT while the structure without the n+ buffer region is referred to as Non Punch-Through (NPT) IGBT. The turn off energy loss, can be evaluated in a similar fashion as the turn-on losses.

2.2 Inverter

2.2.1 Inverter in Power Electronics

An inverter is an electrical device that converts direct current (DC) to alternating current (AC); the converted AC can be at any required voltage and frequency with the use of appropriate transformers, switching, and control circuits. An inverter is essentially the opposite of a rectifier. [4]

Static inverters have no moving parts and are used in a wide range of applications, from small switching power supplies in computers, to large electric utility high-voltage direct current applications that transport bulk power. Inverters are commonly used to supply AC power from DC sources such as solar panels or batteries.

The electrical inverter is a high-power electronic oscillator. It is so named because early mechanical AC to DC converters was made to work in reverse, and thus were "inverted", to convert DC to AC.

2.2.2 Three Phase Inverter

Three-phase inverters are used for variable-frequency drive applications and for high power applications such as HVDC power transmission. A basic three-phase inverter consists of three single-phase inverter switches each connected to one of the three load terminals. [5]

For the most basic control scheme, the operation of the three switches is coordinated so that one switch operates at each 60 degree point of the fundamental output waveform. This creates a line-to-line output waveform that has six steps.

The six-step waveform has a zero-voltage step between the positive and negative sections of the square-wave such that the harmonics that are multiples of three are eliminated as described above.

When carrier-based PWM techniques are applied to six-step waveforms, the basic overall shape, or *envelope*, of the waveform is retained so that the 3rd harmonic and its multiples are cancelled.

2.3 Gate Driver

Gate drivers are electronic circuits that apply correct power levels to insulated gate bipolar transistors (IGBTs).

With power-IGBTs, gate drivers can be implemented as transformers, discrete transistors, or dedicated integrated circuits (IC). They can also be integrated within controller ICs. Partitioning the gate-drive function of controllers that use pulse width modulation (PWM) improves controller stability by eliminating the high peak currents and heat dissipation needed to drive power-IGBTs at very high frequencies. [6]

With IGBTs, gate drivers serve as isolation amplifiers and often provide short-circuit protection. Because of their insulated gates, IGBTs require a continuous gate circuit in order to sustain gate current.

There are four basic types of gate drivers. High-side gate drivers are used to drive IGBTs that are connected to a positive supply and not ground referenced (floating). Conversely, low-side gate drivers are used to drive IGBTs that are connected to a negative supply.

Dual gate or half-bridge gate drivers have both low-side and high-side gates. Three-phase drivers derive their name from the fact that they are used in three-phase applications. These drivers have three independent low-side and high-side referenced output channels. Typically, gate drivers have 1, 2, or 4 output channels. Their output voltage can be either inverted or non-inverted. [7]

CHAPTER 3

METHODOLOGY OF PROJECT WORK

3.1 Procedure Identification

The process flow of the project will be done based on this simple flow below, which is applied throughout for this project.

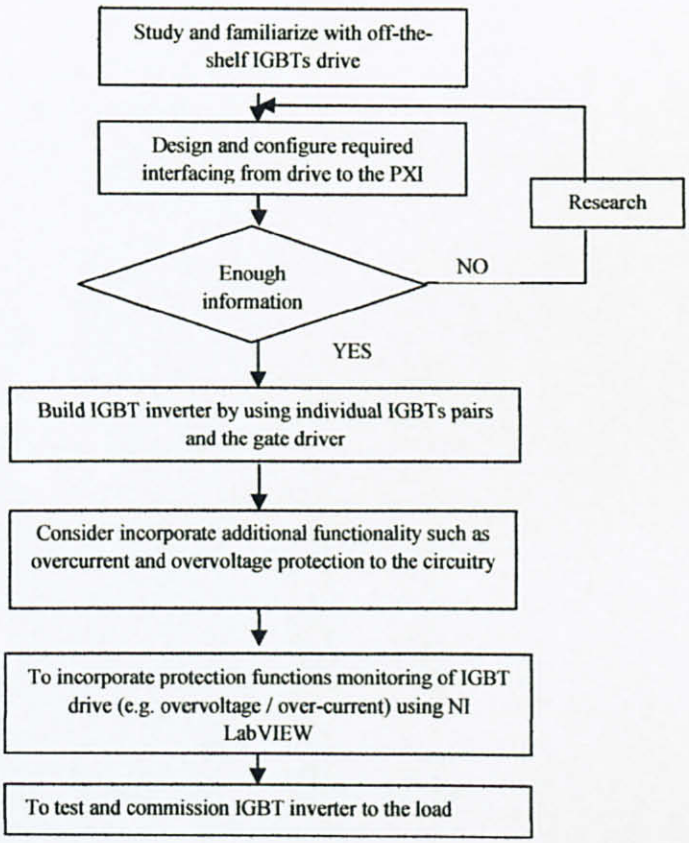


Figure 4: The flow Chart of the process involved in FYP

3.2 Tools and Equipment Required

The tools and equipment which are required in this Final Year Project are a Windows based PC together with the programs such as Microsoft Office and National Instruments LABview software which is used to incorporate protection functions monitoring of IGBT drive and analyse the data obtained.

For the (Printed Circuit Board) PCB layout design, the EAGLE Layout Editor Software and the GC-Power Station Layout Editor Software were used for the designing process of fabricating the PCB board.

Apart from that, equipment needed basically would be data from the internet and other references. Microsoft Office programs include Microsoft Word used to type reports, Microsoft Excel to draw graphs and rearranging of data.

For the hardware, the SEMIKRON SKHI 23/12 (R) the dual IGBT driver and the SEMIKRON 39 AC12T4V1 the three-phase bridge inverter will be used.

3.3 Project Works

3.3.1 Intensive Literature Reviews

Intensive literature reviews has been done on the IGBT inverter application. There are two references that the author used for gaining knowledge on how to operate the IGBT inverter together with the gate driver. Resources from related books, internet and online journals have been accessed. The reviews are crucial to identify the method, tools and equipments that are needed for implementation of the device.

3.3.2 Selecting a suitable off-the-shelf IGBT inverter and the gate driver

After considering several products that are available on the market, the most suitable gate driver and the IGBTs inverter for this project will be chosen. In conjunction with that, the author must also be familiarized with the device characteristics by studying and doing research from the product's user manual and from the journals.

3.3.3 Fabricating and Troubleshooting

The fabrication of the unit will be the final step of this project. After fabrication completed, various testing will be done in order to make sure the expected result will gain and troubleshooting technique will be implement to overcome the encountered problems.

CHAPTER 4

RESULTS AND DISCUSSION

4.1 SEMIKRON SKHI 23/12 (R) Dual IGBT Gate Driver

4.1.1 Device Description

The SKHI 23/12 (R) Dual IGBT Gate Driver is used throughout for this project. SKHI 23/12 (R) device is a power semiconductor subsystem. By using SKHI 23/12 (R) driver, it can drives all SEMIKRON IGBTs with V_{CES} up to 1200V. [8]

For this project, three units of the SKHI 23/12 gate driver will be implementing on the IGBTs inverter. Figure below shows this gate driver physical setup.

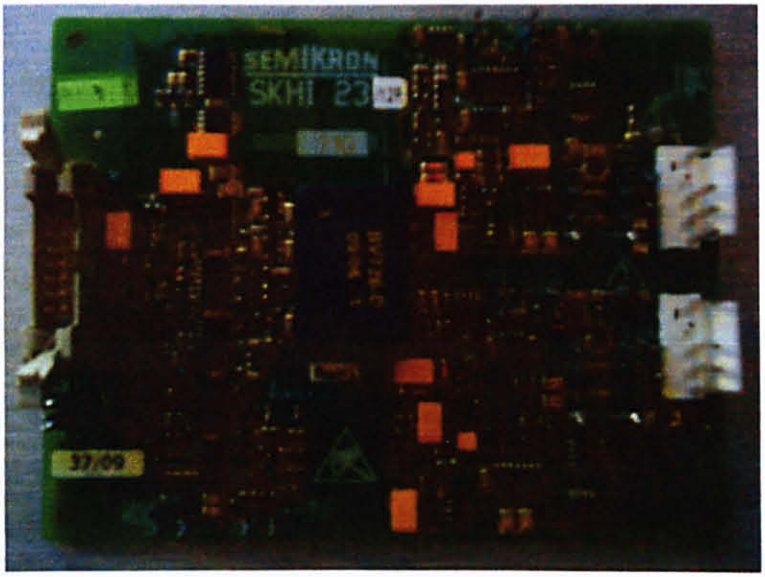


Figure 5: Top View

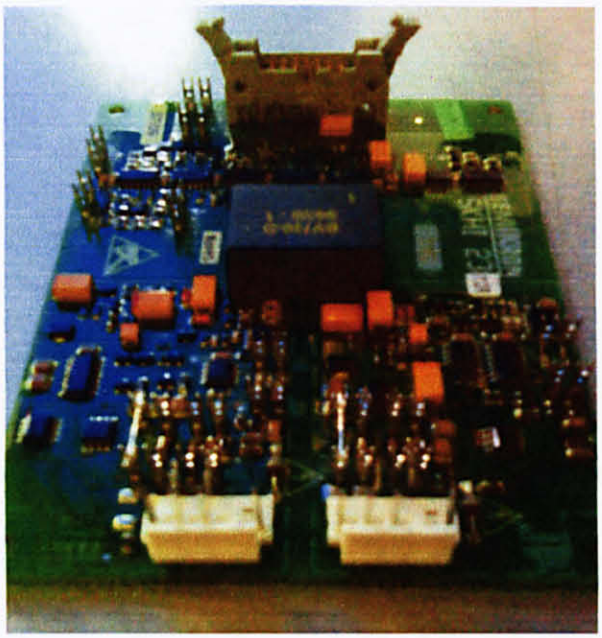


Figure 6: Side View

Figure 7: SKHI 23/12(R) Dual IGBT Gate Driver

Here are this gate driver features:

- ✓ Input Level Selector

  The SKHI 23 has an input level selector circuit for two different levels. It is preset for CMOS (15V) level, but can be changed by the user to HCMOS (5V) [8]

- ✓ Interlock

  An INTERLOCK circuit prevents the two IGBTs of the half bridge to switch-on at the same time.

✓ Error Memory

The ERROR MEMORY blocks the transmission of all turn-on signals to the IGBT if either a short circuit or malfunction of Vs is detected. During that time ,a signal is sent to the external control board through an open collector transistor.

✓ Vs Monitor

This feature makes sure that the Vs actual is not below 13V and if the Vs is below 13V, a signal will be sent to the user.

✓ Ferrite Transformer

With a FERRITE TRANSFORMER the information between primary and the secondary may flow in both directions and high levels of dc/dt and isolation are obtained.[8]

✓ DC/DC converter

A high frequency DC/DC CONVERTER avoids the requirement of external isolated power supplies to obtain the necessary gate voltage .An isolated ferrite transformer in half-bridge configuration supplies the necessary power to the gate of the IGBT. With this feature, user can use the same power supply used in the external control circuit, even if user using more than one SKHI 23 such that in this project in three phase configuration.[8]

✓ Output Buffer

The correct current to the gate of the IGBT will be control by the OUTPut BUFFER. If these signals do not have sufficient power, the IGBT will not switch properly.

✓ Reset

When there is zero value for both of the input Vin, the RESET is performed

This gate driver needs to be powered up by 15V which is suitable for this project. Figure below shows how to connect the SKHI 23/12 (R) by using the short cables.

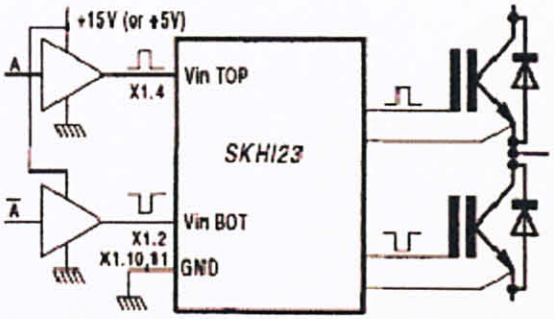


Figure 8: Connecting the SKHI 23/12 (R) with short cables.

4.2 SEMIKRON SKiiP 39ACT4V1 Three-phase Bridge Rectifier

SEMIKRON SKiiP 39ACT4V1 is a trench 4 IGBTs build-up inverter. In this project, the SKiiP 39ACT4V1 will use to invert the DC supply up to 240V AC in order to produce the three-phase output.

Figures below show the physical view of the SEMIKRON SKiiP 39ACT4V1 unit.[9]

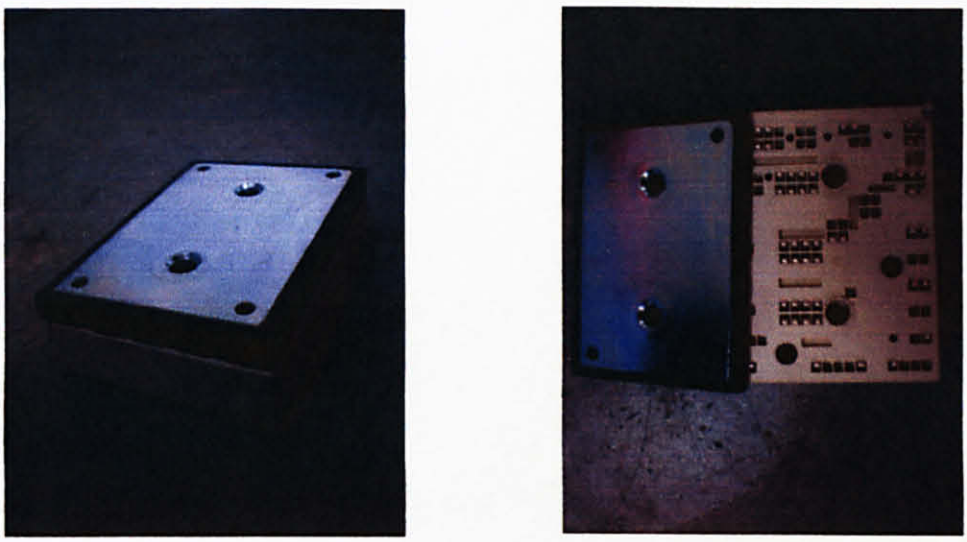


Figure 9: SEMIKRON SKiiP 39ACT4V1 physical view.

Figure below shows the block diagram of this bridge rectifier.The author had recognized all of the pins on the device and assigned each corresponding pin on the bridge inverterto the gate driver for the interfacing steps.

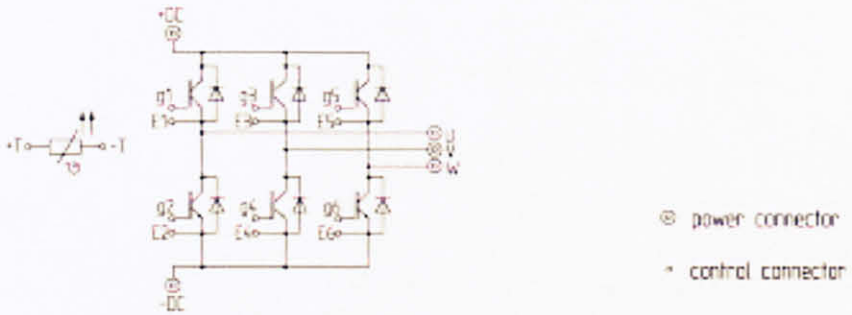


Figure 10: The block diagram of the bridge rectifier

4.3 Drafting the Block Diagram Connection of devices

For the first step into this project, the author had done a study about the interconnection between the gate driver and the inverter. The basic block diagram of the connection also has been constructed in order to be the guide of the next step which is the interfacing the devices together.

4.4 Plug Connectors PCB Driver

For the connection of the plug connectors to the PCB driver, the author had verified the types of connection that will use for the connection. Table 4.1 below shows the types of connection used:

Driver Type	Input Connector (Primary Side to Controller)		Output Connector (Secondary Side to IGBT)	
	Male	Female	Male	Female
SKHI 23/12 (R)	DIN 41651 (14 pins)	plug 14 pins DIN 41651	MOLEX Series 41791 (5 pins)	MOLEX Series 41695

Table 1: Plug Connectors

4.5 Fabricating the PCB board for the interfacing between gate driver and the IGBTs

In order to do the interfacing between the gate driver and the IGBTs, the author must design a PCB board. The designed PCB board should take account all of the connection points between the gate driver and the inverter via the connectors that will be connected to the PCB board.

For the first phase of the designed process, the author had decided to use the EAGLE Layout Editor Software for the PCB layout software. The design should consider all of the pins on the bridge inverter in order to make this device fully operate.

4.5.1 EAGLE Layout Editor Software Designing Process

By using EAGLE Layout Editor Software, the process of designing the layout of the PCB board is been designed. Firstly, the entire dimension between the pins on the gate inverter is measured.

The details of the measurement can be getting from the SEMIKRON SKiiP 39ACT4V1 data sheet. Figure below shows the dimension of the inverter.

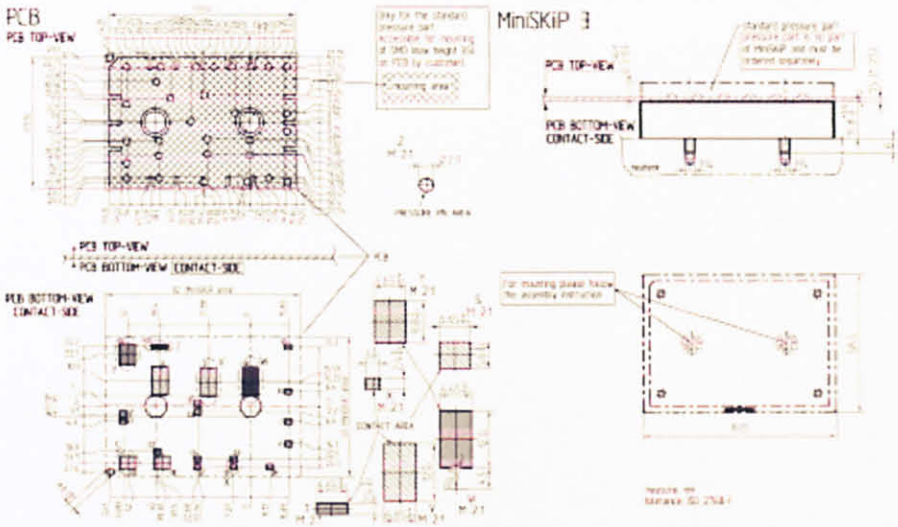


Figure 11: The Layout Dimension of inverter

Then after considering the dimension of the desired designed PCB board, the new project is created in the EAGLE Layout Editor.

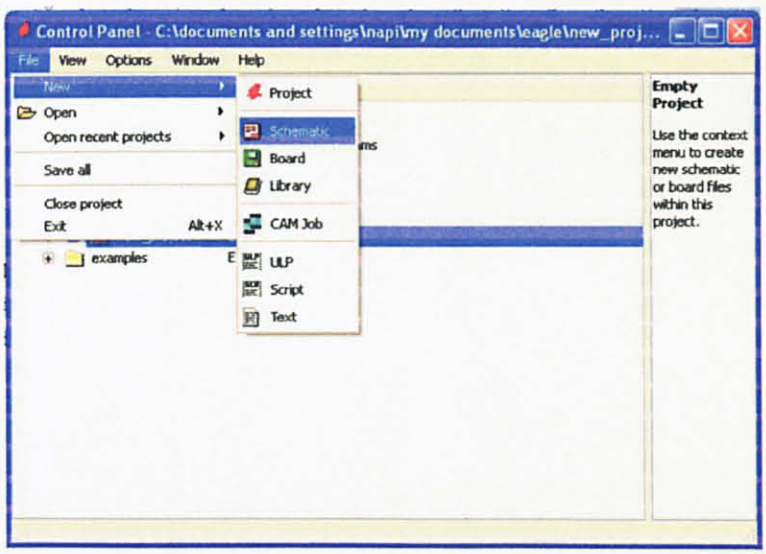


Figure 12: Creating a new project in editor menu

In this designing process, the author had the problem of choosing the correct block set in the library that is matching with the pins on the inverter.

After discussing with the PCB Lab Technician, Mr. Isnani and the supervisor, Mr. Saiful Azrin bin Mohd Zulkifli, the author had decided to choose the designation of the pins on the PCB is by using the pinhead block set that is available in the library of EAGLE Layout Editor.

By choosing to use the pinhead block in the library, the author had to consider placing a 56 set of pinheads on the design PCB board. To add the component on the schematic, the author use the add mode on the schematic menu.

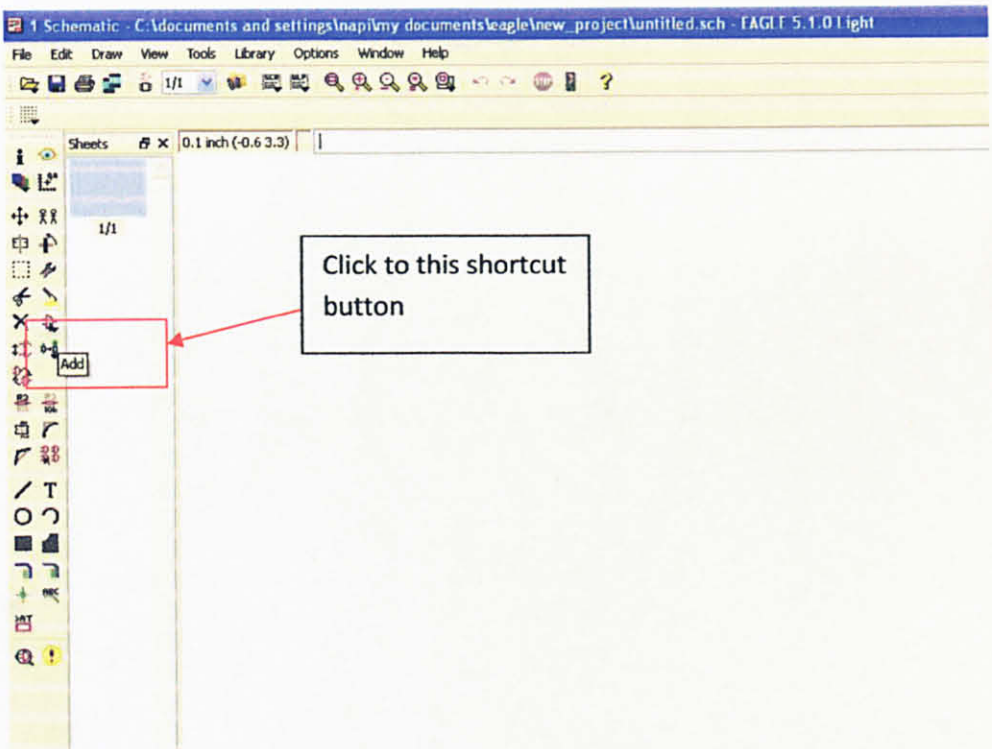


Figure 13: Add menu on the schematic

Then in the library menu, the pin header block set was choose .The pin header block set name is PINHD-1X1 PINHEADER.

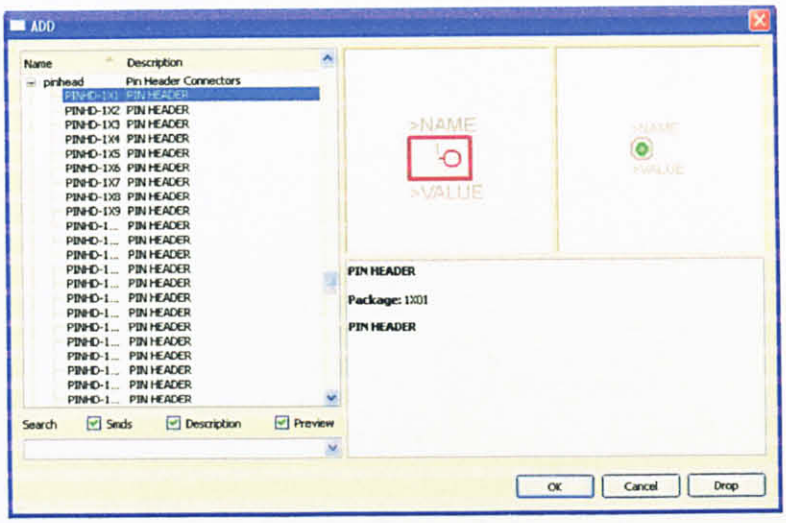


Figure 14: The Pin header component menu

In the schematic view, all of the 56 units of pin headers were placed on the window. The view of the 56 units of pin headers can be seen as in Figure 15.

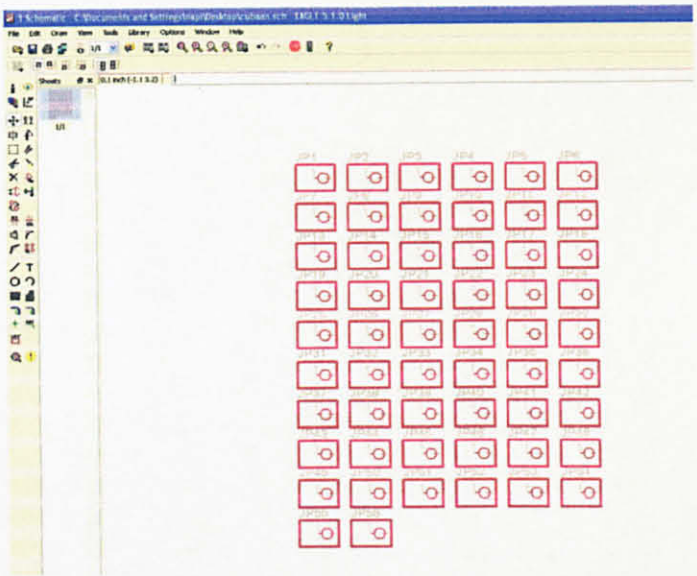


Figure 15: 56 units of pin headers in the schematic view

In order to place each unit of the pin header correctly according to the dimension of the actual pins on the inverter, from this schematic view the author had to use the switch to board menu from the layout editor menu.

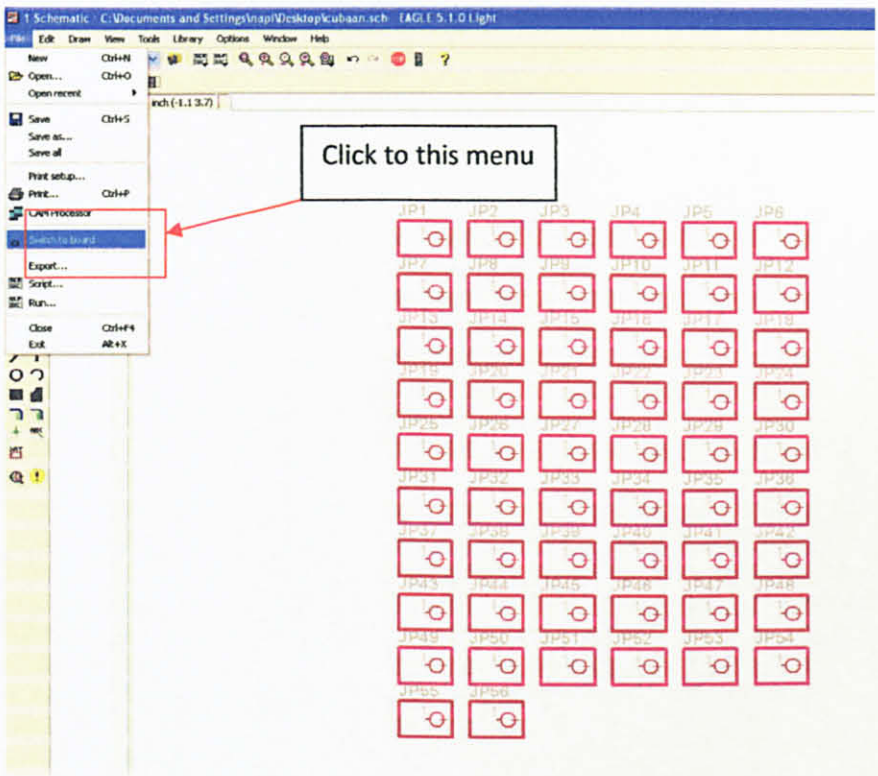


Figure 16: Switch to board menu

After switching to board view, then the step of locating each of the pin headers can be implementing. Before proceeding, the author had set the grid setting in the View > Grid menu in the board view. The setting for the board view can be seen in Figure 17.

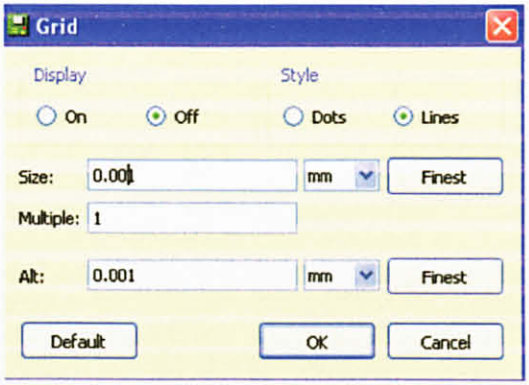


Figure 17: Grid Setting

For the grid setting, the grid size is set to 0.001 mm and the Alt is set to 0.001 mm. This setting will be applied for throughout of this design.

Then, by referring to the actual dimension of the pins on the inverter from the schematic diagram, the pin headers were placed on the board view. Figure 18 below shows the process of plotting the pin headers on the board.

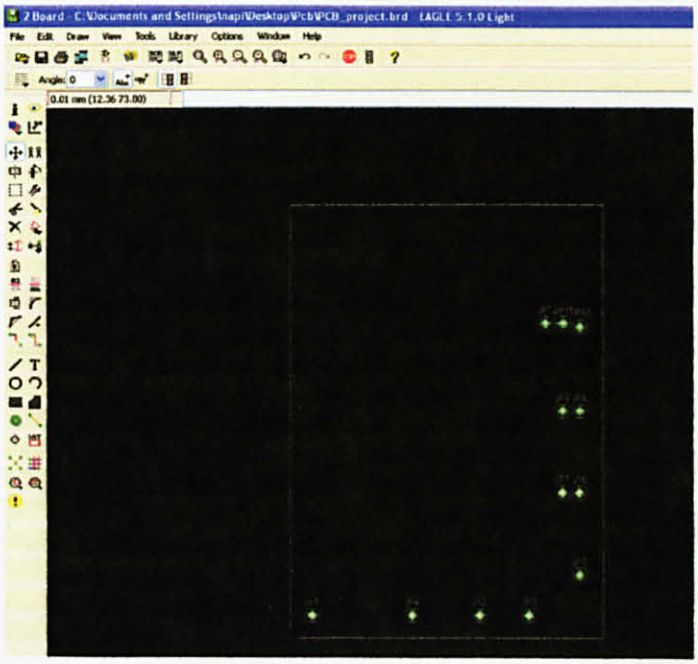


Figure 18: Plotting pin headers on the board

After plotting all of the 56 points of the pin headers, Figure 19 below shows the complete board.

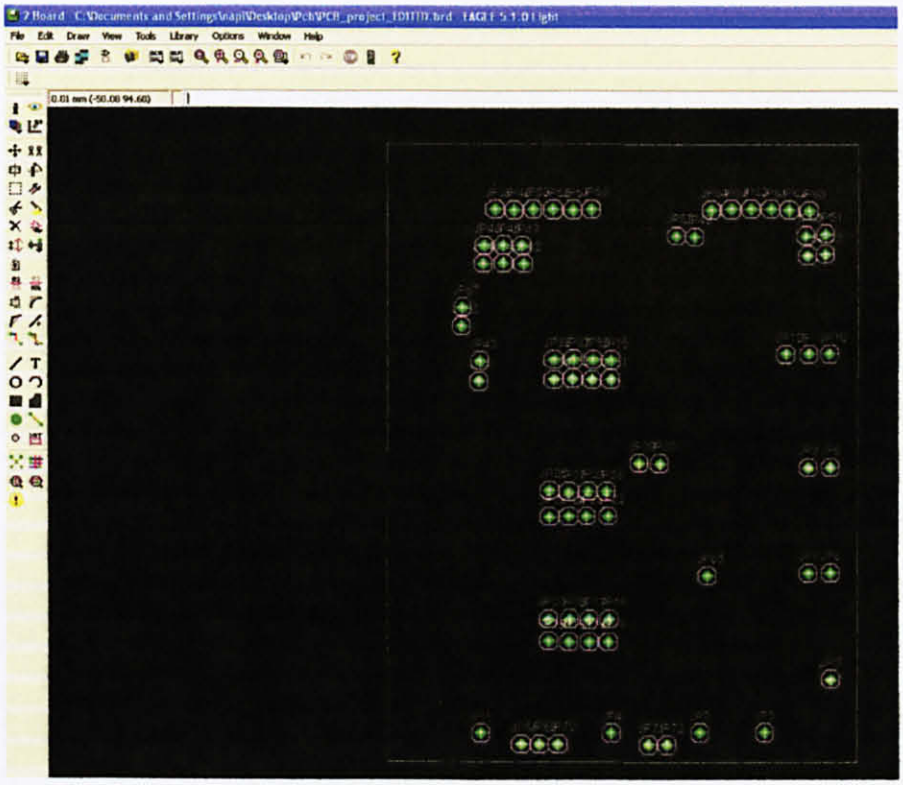


Figure 19: Completed Board

4.5.2 Problem Encountered

The designed PCB board is not fully functional due to the plotting error on the design stage of this board.

Some of the pins on the inverter are not touching the PCB pinheads; therefore the author had to redesign it again by considering the main problem.

Figure 20 below shows the area of error in the design. The error occurred due to the precision during the plotting process.

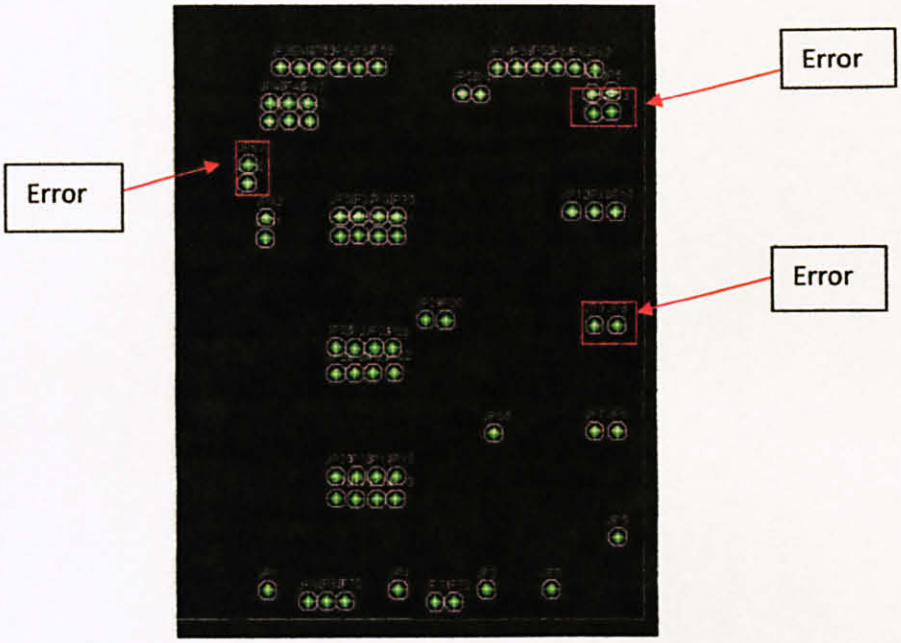


Figure 20: Error on the Board

Thus, to over come this error the author had decided to use another PCB layout editor that is more accurate and easy to use and detect the error during the design process.

4.5.3 GC-Power Station Layout Editor Software PCB Designing Process.

Because of the author's first design of the PCB board was not functional due to the error in the pin headers plotting process, therefore the author had decided to use another PCB layout editor that is more accurate and easy to use.

Firstly, a new project file is created. The layout of the GC-Power Station software can be seen as in Figure 21.

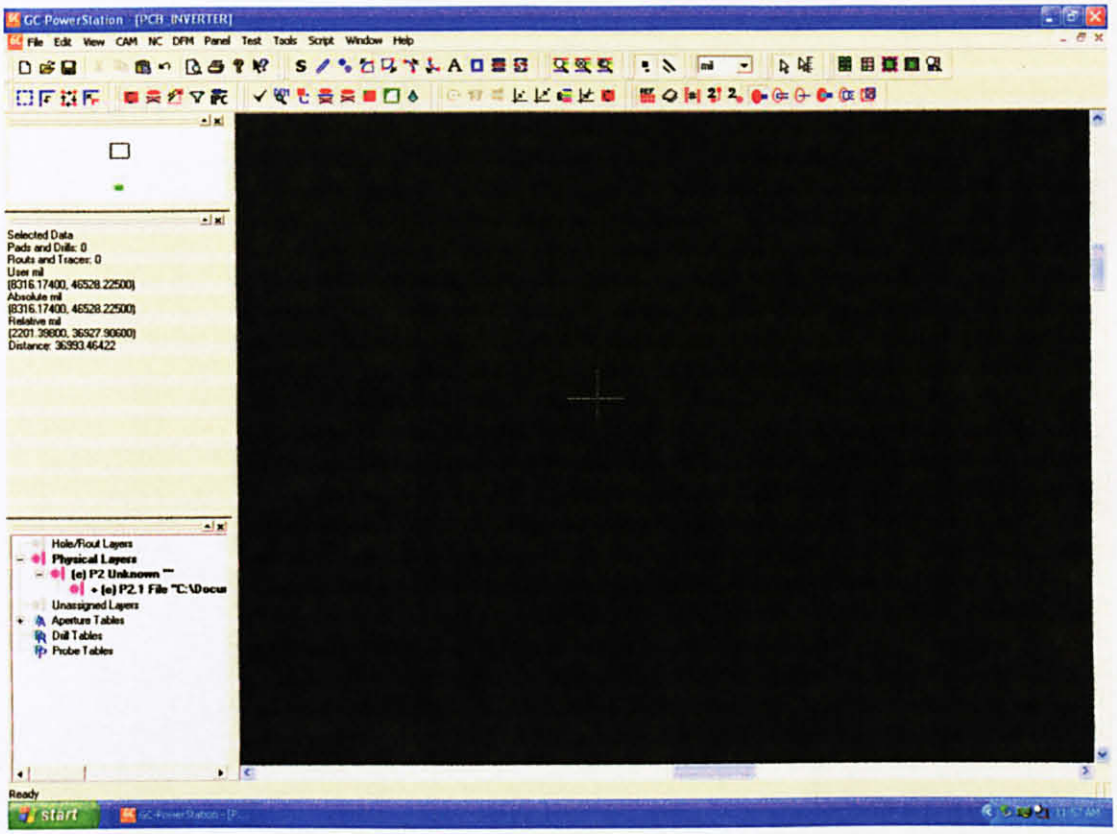


Figure 21: The Open New File View

After that all of the pins point on the inverter were designed and placed correctly on the board. Then the process of placing the pin point for the connection between the E-connector and the E-points on the inverter (E1, E2, E3, E4, E5, and E6) was done. Figure 22 below shows the process of drawing the connection points.

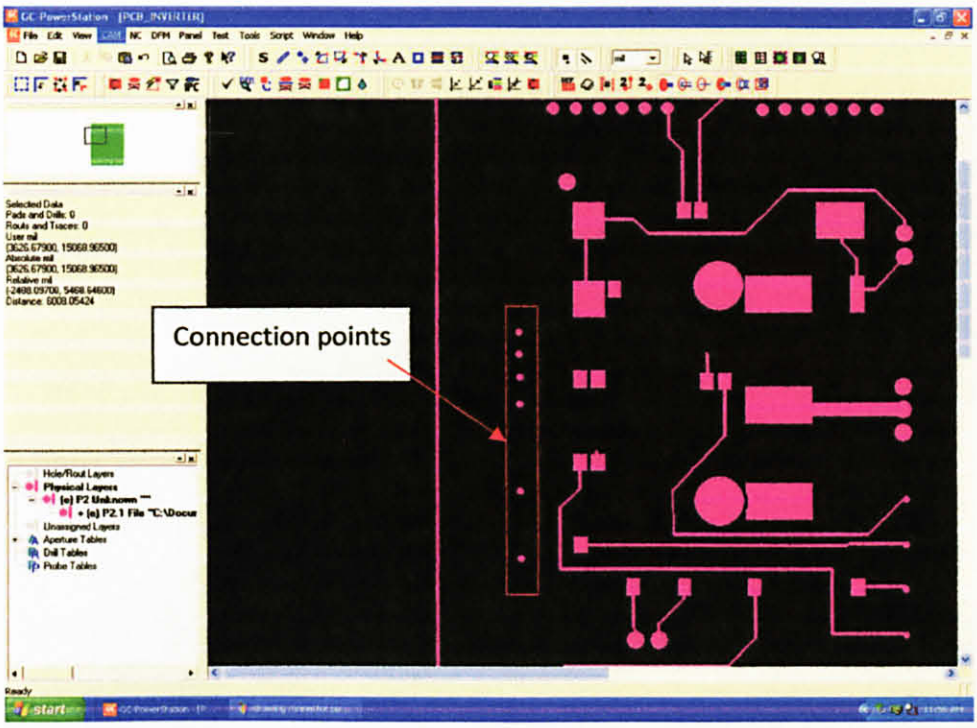


Figure 22: Drawing the connection points on the board

These connection points will make the process of connecting between the connector point and the E-points on the inverter easier. Moreover, by using this technique the author can easily detecting and correcting the error on the connection route.

Then the points will be connected to the connector points via the connection points made. Figure 23 below shows the completed connection between the connection points and the connector's points.

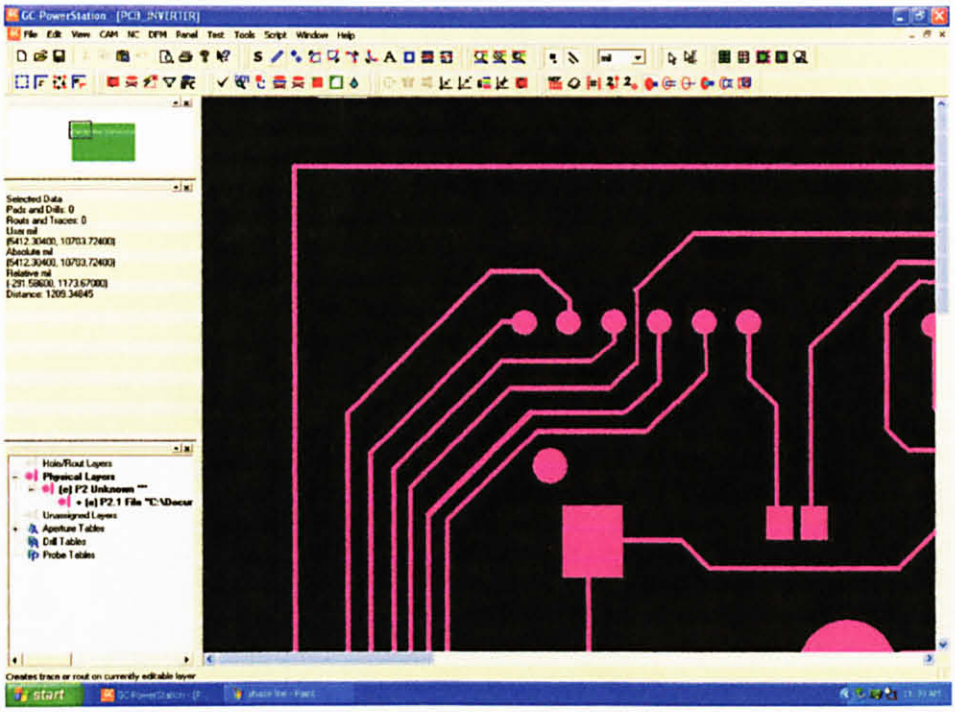


Figure 23: The Completed connection between E-connectors and E-points

The same technique was applied to other points that were G-points, T-points, DC+ and DC-.For the output phase points , the design is slightly different from this technique. This is due to the capacity for the output phase voltage and current are higher. Figure below shows the route settings of the connection route.

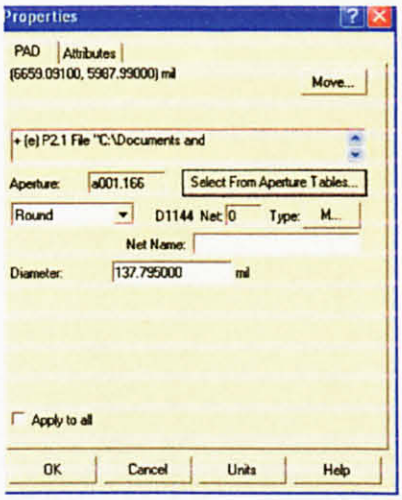


Figure 24: The route setting

Figure 25 below shows the process of drawing the output connection point. For the connection points, a bigger diameter size was chosen.

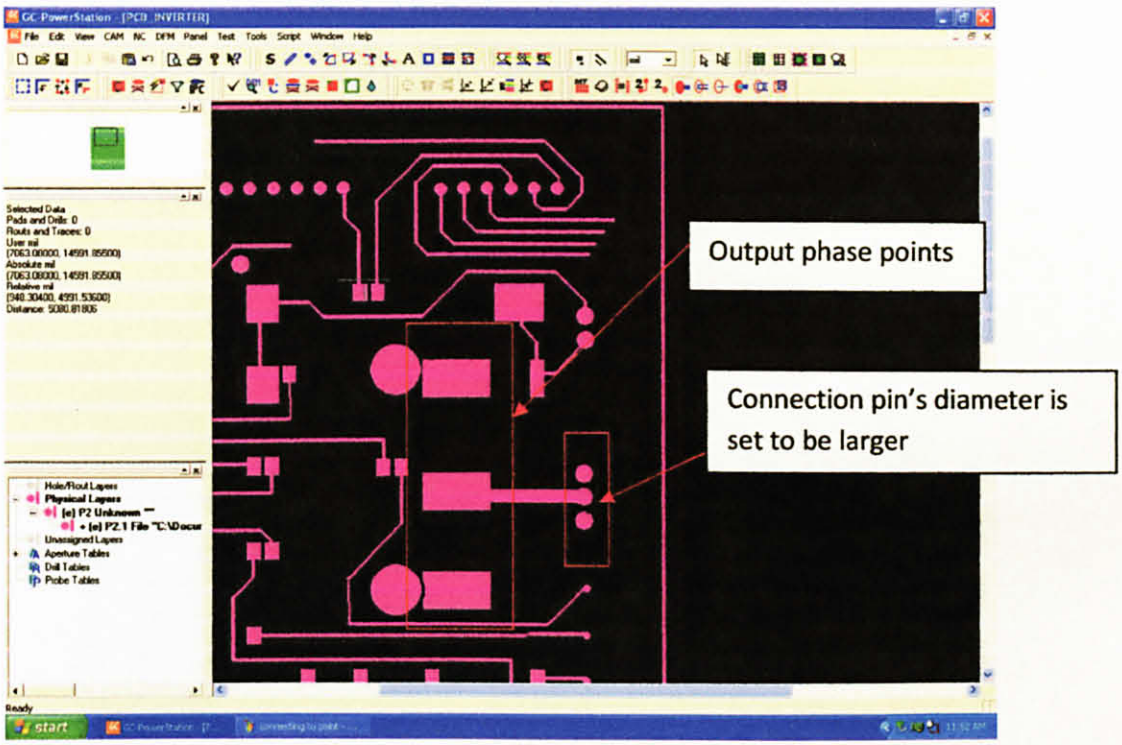


Figure 25: The connection of output phase points

Because of the output phase carry the highest current and voltage on the board, therefore the route of the connection between the connection points was set to the setting as same as Figure 26 below.

Figure 26: Output route line setting

The diameter is set to be 100 mil. This setting will make the route to be able to conduct the higher level of output voltage and current. Then, the completed tracks of the output phase route were done as shown in Figure 27 below.

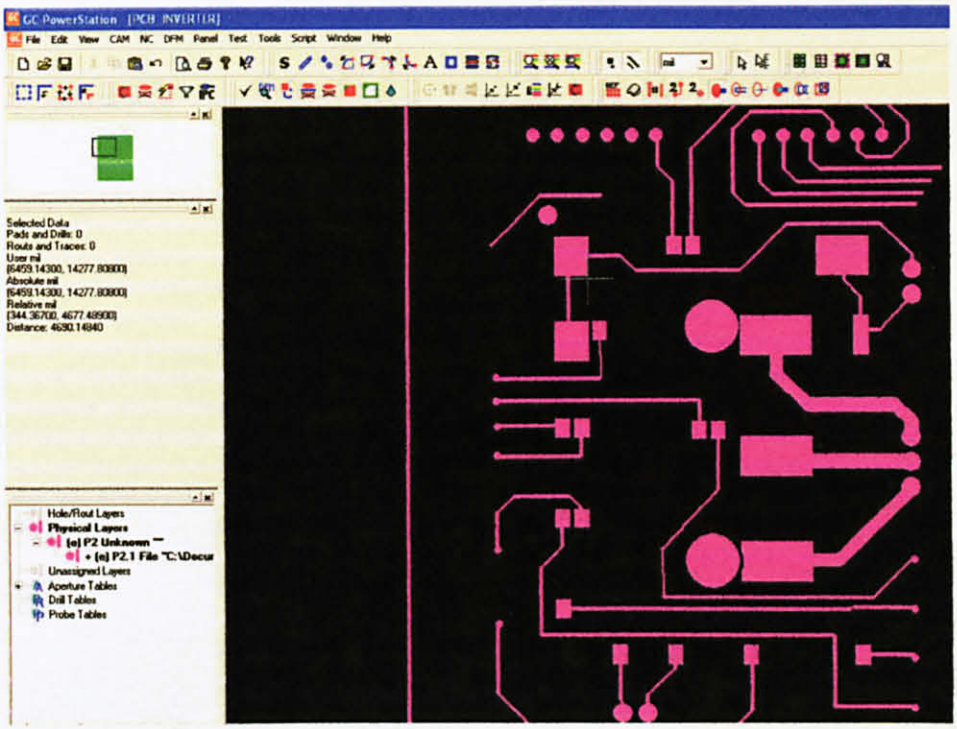


Figure 27: The complete route for output phase connection.

Finally, all the connection points then were connected to the correct points on the PCB layout. Figure 28 below shows the completed design of this project PCB design.

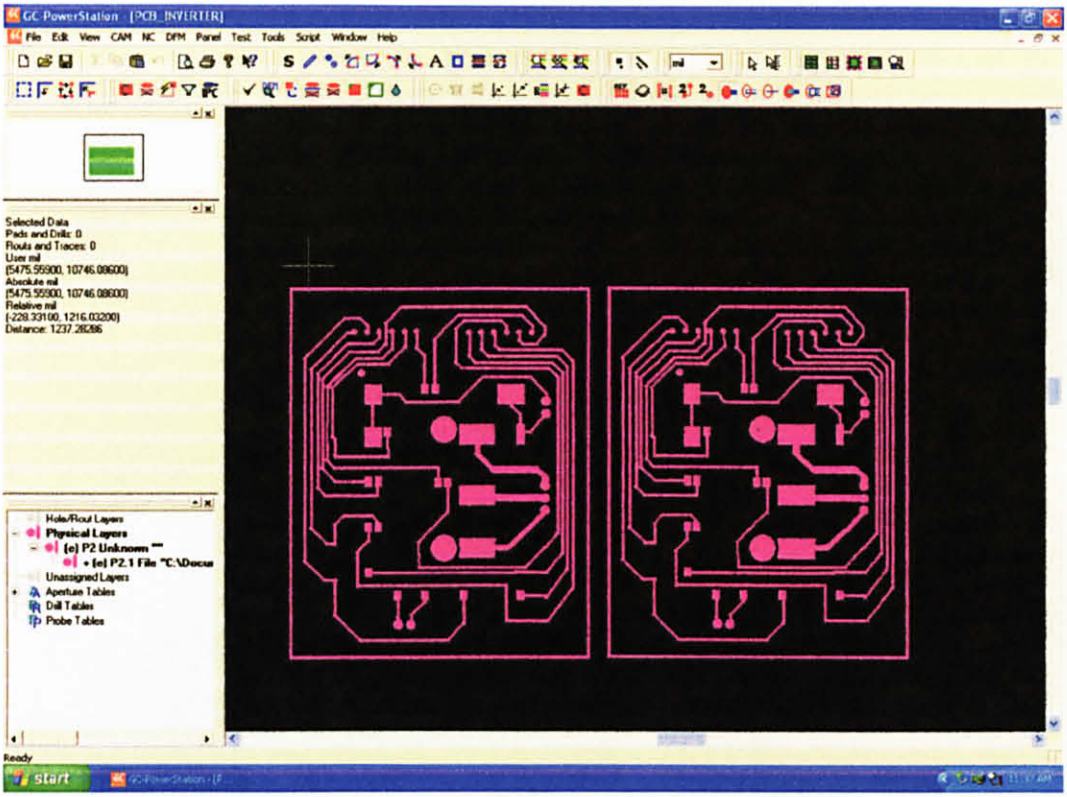


Figure 28: The completed PCB board design

Figure 29 below shows the PCB board that was finally fabricated. This board then will be placed on top of the IGBT inverter and will be screwed with the m4 screw.

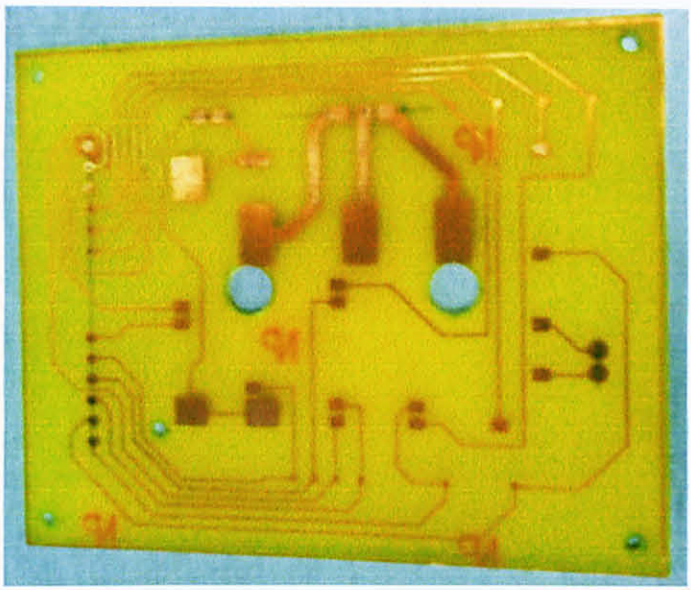


Figure 29: The fabricated PCB board

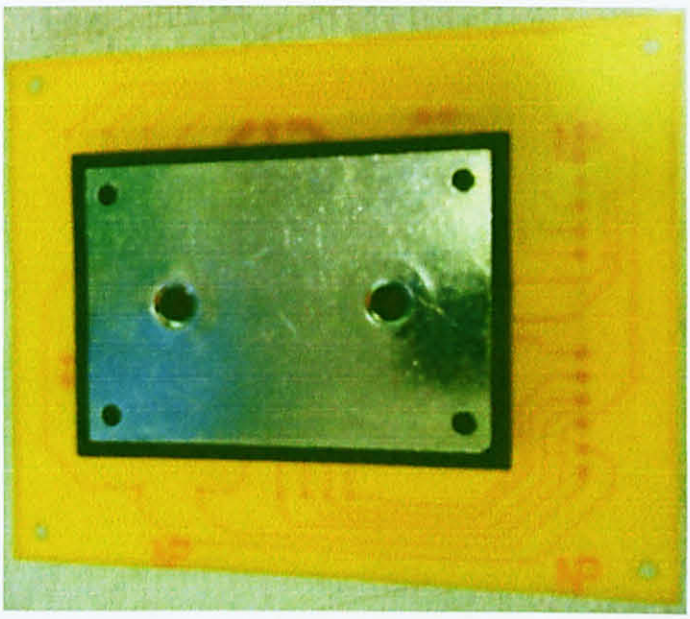


Figure 30: Connecting the IGBT inverter with the PCB board

4.6 Interfacing the Gate Driver and the IGBT Inverter via the PCB board

The next step of this project is the interfacing between the Gate Driver and the IGBT Inverter via the fabricate PCB board. In this phase, all of the connections between the hardware were make sure to be correct before proceeding with the next phase.

Figure 31 below shows the initial setup of this project hardware.

Figure 31: Side View of hardware initial setup

Figure 32: Front View of hardware initial setup

CHAPTER 5

CONCLUSION AND RECOMMENDATION

5.1 Conclusion

This project needs a very careful study and consistent works. There will be many obstacles that need to be handled and overcome in completing this project. However with the guidance from the supervisor, this project can be completed successfully as scheduled. Implementing knowledge from the class will be different from the knowledge gain from the hands-on experience.

In this project, the testing part cannot be implementing yet. This is due to the fact of time limitation of this project. However, the author had managed to get a clear view of this project's process and procedure involves in completing this project. The author also had managed to complete the important steps involved in this project which was the initial setup of the gate driver and the IGBT inverter which can help other semester student to continue the next stages.

5.2 Recommendation

For this semester, the author has to work very hard in order to complete this FYP project on schedule. However, flexibility is important for author to proceed with any modification to accommodate improvement for the problem encountered. For improvement of this project, the author suggests that:

- ✓ **Exposure To The Product's Data Sheet**

  Student should be familiarizing with the product's data sheet. From this product's data sheet or product's manual, a lot of information about the product can be found such as the operating conditions, electrical characteristics and the schematic diagram.

- ✓ **Meeting With Supervisor**

  From the meeting, the author will have opportunity to ask and get advices from the supervisor. This will help author a lot in completing this project successfully according to the schedule.

- ✓ **Neater Design**

  The author plans to install the housing part for the device. This will prevent it from dust and exposed it to the potential hazard.

REFERENCES

[1] Synchronous motor by http://en.wikipedia.org/wiki/Synchronous_motor

[2] IGBT Basic by http://en.wikipedia.org/wiki/Insulatedgate_bipolar_transistor#18/12/2009 3:47:18 PM

[3] IGBT description http://ocw.mit.edu/NR/rdonlyres/Electrical-Engineering-and-Computer-Science/6-012Fall-2009/781BD339-C575-45EF-A21F-F5E4C48D8E32/0/MIT6_012F09_lec14_inverter.pdf

[4] IGBT Basic: http://www.powerdesignersusa.com/InfoWeb/design_center/articles/IGBTs/igbts.shtm

[5] IGBT gate driver by: http://www.rell.com/resources/RellDocuments/SYS_25/Microsemi-Tutorial-IGBT-APT0201.pdf

[6] Inverter by 6.012 -Microelectronic Devices and Circuits – Fall 2009

[7] Inverter design www.discovercircuits.com/C/co-dctoac.htm

[8] SkiiP_39AC12T4V1_101209 Datasheet

[9] SKHI_23_12R_101209 Datasheet

APPENDICES

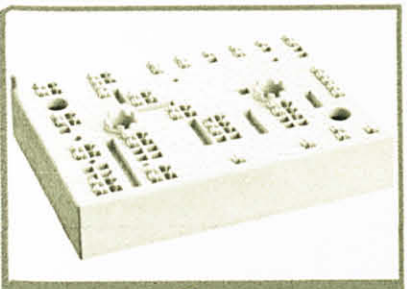
APPENDIX: Gantt chart

No.	Detail/Week	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
1	Component Purchasing and Researching															EXAM WEEK		
2	Submission of Progress Report 1																	
3	PCB Designing and Fabrication																	
4	Submission of Progress Report 2																	
5	Poster Exhibition (ElectrEx)																	
6	Submission of Draft Report																	
7	Submission of Dissertation (softbound)																	
8	Oral Presentation																	
9	Submission of Project Dissertation (Hardbound)																	

Progress

Suggested milestone

SKiiP 39AC12T4V1



MiniSKiiP®3

3-phase bridge inverter

SKiiP 39AC12T4V1

Features

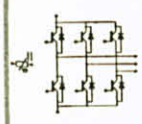
- Trench 4 IGBT´s
- Robust and soft freewheeling diodes in CAL technology
- Highly reliable spring contacts for electrical connections
- UL recognised file no. E63532

Typical Applications

- Inverter up to 50 kVA
- Typical motor power 30 kW

Remarks

- V_{CEsat} , V_F= chip level value
- Case temp. limited to T_C = 125°C max. (for baseplateless modules $T_C = T_S$)
- product rel. results valid for $T_j \leq 150$ (recomm. T_{op} = -40 ... +150°C)
- For short circuit: Soft R_{Goff} recommended



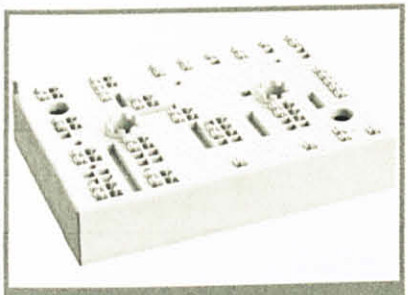
AC

Absolute Maximum Ratings T_s = 25 °C, unless otherwise specified

Symbol	Conditions		Values	Units
IGBT				
V_{CES}	T_j = 25 °C		1200	V
I_C	T_j = 175 °C	T_c = 25 °C	167	A
		T_c = 70 °C	135	A
I_{CRM}	I_{CRM} = 3xI_{Cnom}		450	A
V_{GES}			±20	V
t_{psc}	V_{CC} = 800 V; $V_{GE} \leq$ 15 V; V_{CES} < 1200 V	T_j = 150 °C	10	µs
Inverse Diode				
I_F	T_j = 175 °C	T_c = 25 °C	136	A
		T_c = 70 °C	107	A
I_{FRM}	I_{FRM} = 3xI_{Fnom}		450	A
I_{FSM}	t_p = 10 ms; sin	T_j = 150 °C	900	A
Module				
$I_{t(RMS)}$			160	A
T_{vj}			-40...+175	°C
T_{stg}			-40...+125	°C
V_{isol}	AC, 1 min.		2500	V

Characteristics T_s = 25 °C, unless otherwise specified

Symbol	Conditions		min.	typ.	max.	Units
IGBT						
$V_{GE(th)}$	$V_{GE} = V_{CE}$, I_C = 6 mA		5	5,8	6,5	V
I_{CES}	V_{GE} = V, $V_{CE} = V_{CES}$	T_j = °C				mA
V_{CE0}		T_j = 25 °C		0,8	0,9	V
		T_j = 150 °C		0,7	0,8	V
r_{CE}	V_{GE} = 15 V	T_j = 25°C		6,7	7,3	mΩ
		T_j = 150°C		10	10,7	mΩ
$V_{CE(sat)}$	I_{Cnom} = 150 A, V_{GE} = 15 V	T_j = 25°C$_{chiplev.}$		1,85	2,05	V
		T_j = 150°C$_{chiplev.}$		2,25	2,45	V
C_{ies}	V_{CE} = 25, V_{GE} = 0 V	f = 1 MHz		8,8		nF
C_{oes}				0,58		nF
C_{res}				0,47		nF
Q_G	V_{GE} = -8 ... +15V			850		nC
R_{Gint}	T_j = 25 °C			5		Ω
$t_{d(on)}$	R_{Gon} = 1 Ω	V_{CC} = 600V		165		ns
t_r	di/dt = 2840 A/µs	I_C= 150A		50		ns
E_{on}		T_j = 150 °C		22,5		mJ
$t_{d(off)}$	R_{Goff} = 1 Ω	V_{GE} = ±15V		390		ns
t_f	di/dt = 1880 A/µs			80		ns
E_{off}				14		mJ
$R_{th(j-s)}$	per IGBT			0,33		K/W



MiniSKiiP®3

3-phase bridge inverter

SKiiP 39AC12T4V1

Characteristics						
Symbol	**Conditions**		**min.**	**typ.**	**max.**	**Units**
Inverse Diode						
$V_F = V_{EC}$	I_{Fnom} = 150 A; V_{GE} = 15 V	T_j = 25 °$C_{chiplev.}$		2,15	2,45	V
		T_j = 150 °$C_{chiplev.}$		2,05	2,4	V
V_{F0}		T_j = 25 °C		1,3	1,5	V
		T_j = 150 °C		0,9	1,1	V
r_F		T_j = 25 °C		5,7	6,3	mΩ
		T_j = 150 °C		7,7	8,7	mΩ
I_{RRM}	I_F = 150 A	T_j = 150 °C		188		A
Q_{rr}	di/dt = 4020 A/µs			27		µC
E_{rr}	V_{GE} = ±15V			11,4		mJ
$R_{th(j-s)}$	per diode			0,52		K/W
M_s	to heat sink		2		2,5	Nm
w				97		g
Temperature sensor						
R_{ts}	3%, Tr = 25°C			1000		Ω
R_{ts}	3%, Tr = 100°C			1670		Ω

Features

- Trench 4 IGBT´s
- Robust and soft freewheeling diodes in CAL technology
- Highly reliable spring contacts for electrical connections
- UL recognised file no. E63532

Typical Applications

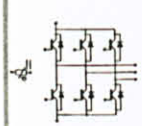
- Inverter up to 50 kVA
- Typical motor power 30 kW

Remarks

- V_{CEsat} , V_F= chip level value
- Case temp. limited to T_C = 125°C max. (for baseplateless modules $T_C = T_S$)
- product rel. results valid for $T_j \leq 150$ (recomm. T_{op} = -40 ... +150°C)
- For short circuit: Soft R_{Goff} recommended

This is an electrostatic discharge sensitive device (ESDS), international standard IEC 60747-1, Chapter IX.

This technical information specifies semiconductor devices but promises no characteristics. No warranty or guarantee expressed or implied is made regarding delivery, performance or suitability.



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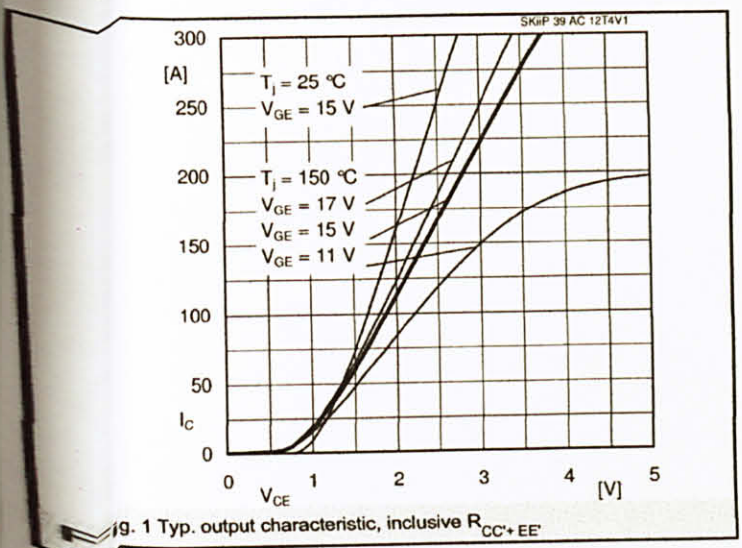


Fig. 1 Typ. output characteristic, inclusive $R_{CC'+EE'}$

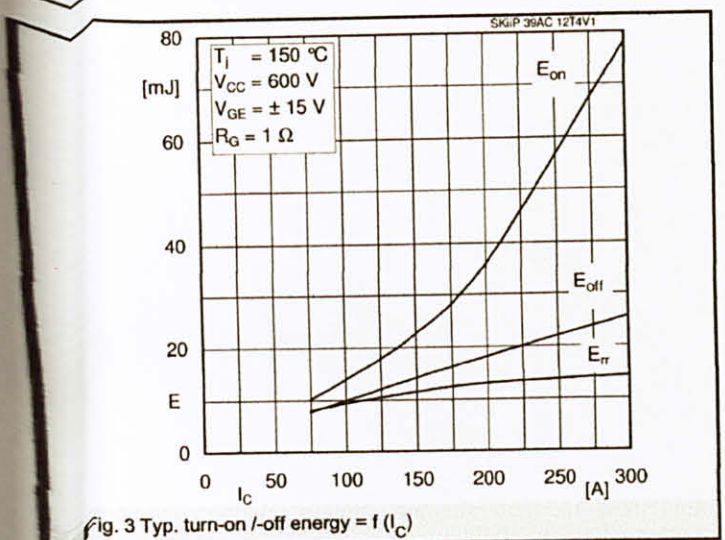


Fig. 3 Typ. turn-on /-off energy = f (I_C)

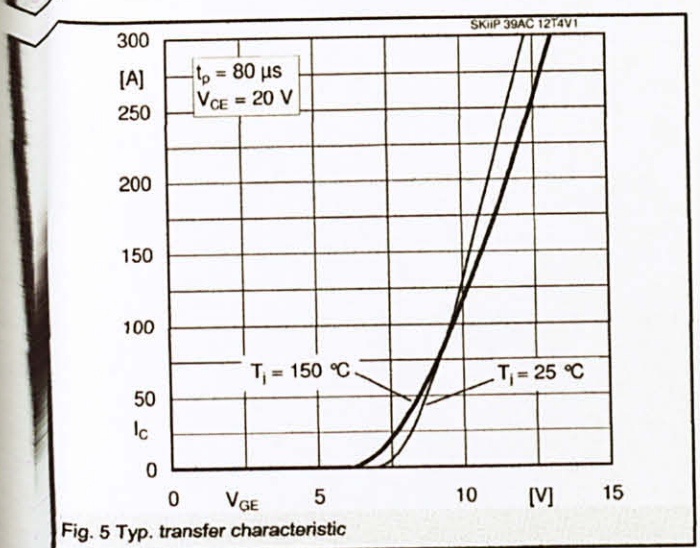


Fig. 5 Typ. transfer characteristic

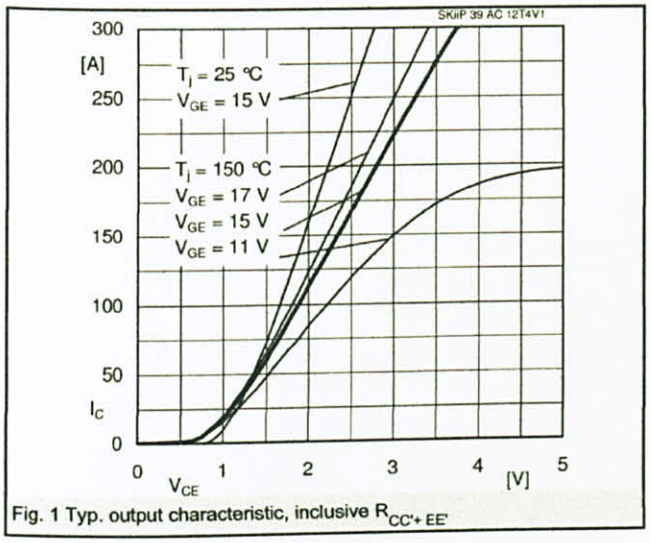


Fig. 1 Typ. output characteristic, inclusive $R_{CC'+EE'}$

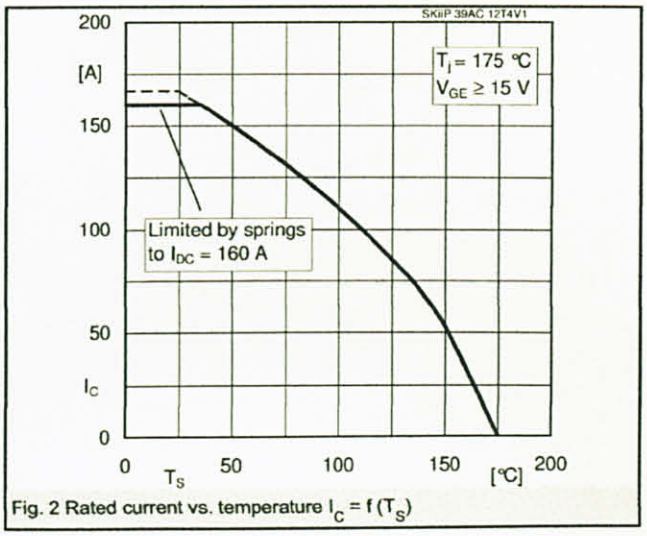


Fig. 2 Rated current vs. temperature $I_C = f(T_S)$

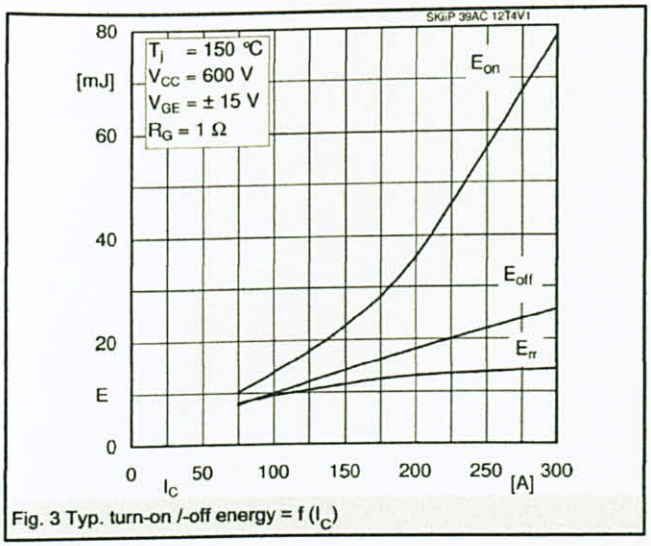


Fig. 3 Typ. turn-on /-off energy = f (I_C)

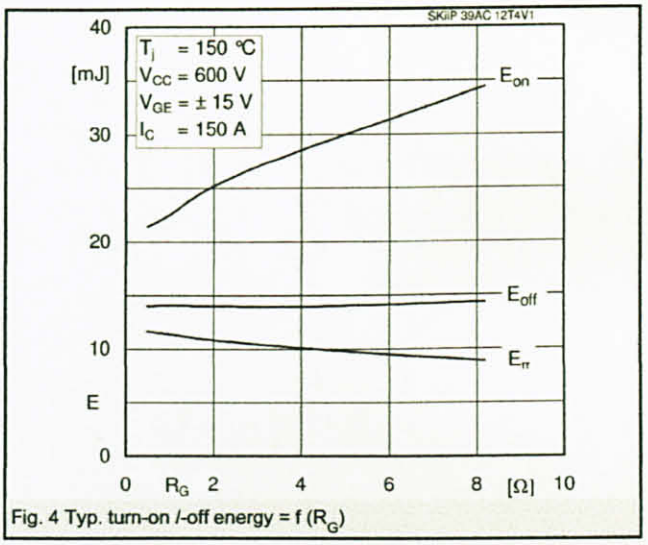


Fig. 4 Typ. turn-on /-off energy = f (R_G)

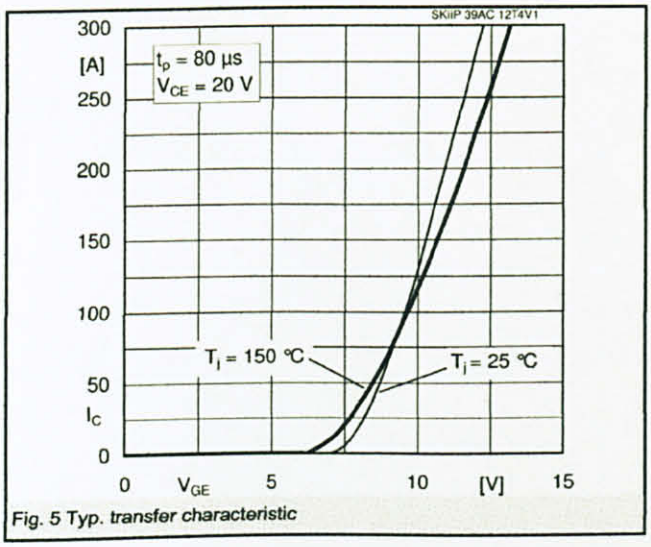


Fig. 5 Typ. transfer characteristic

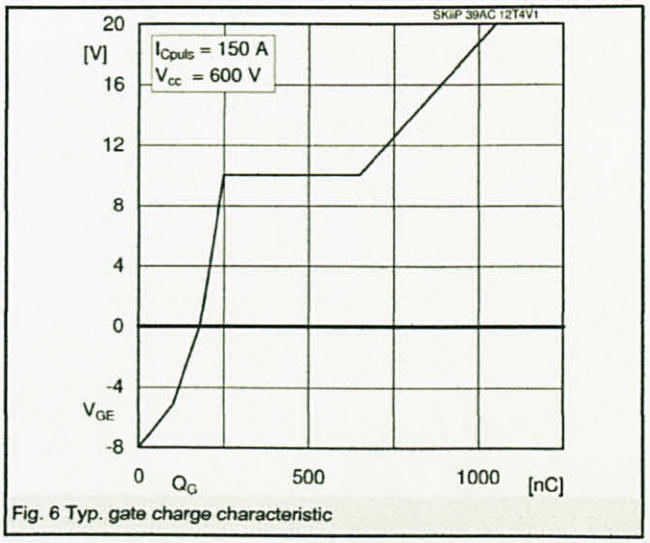


Fig. 6 Typ. gate charge characteristic

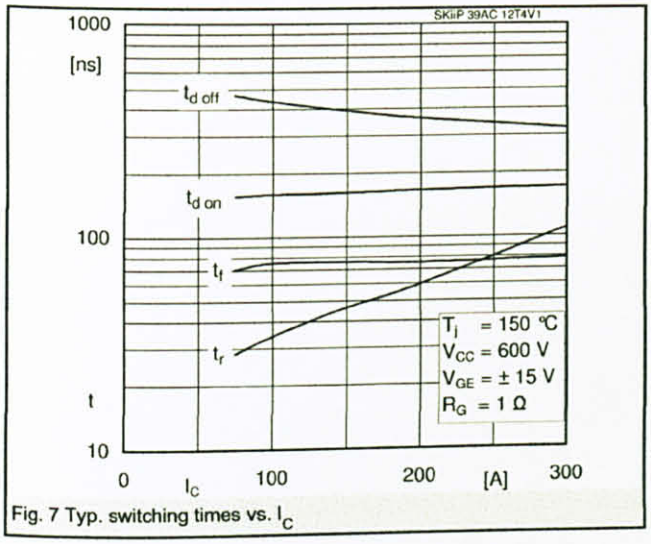


Fig. 7 Typ. switching times vs. I_C

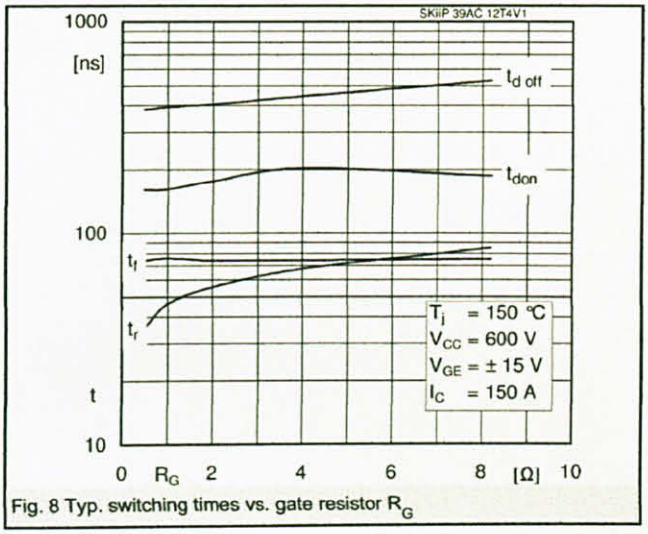


Fig. 8 Typ. switching times vs. gate resistor R_G

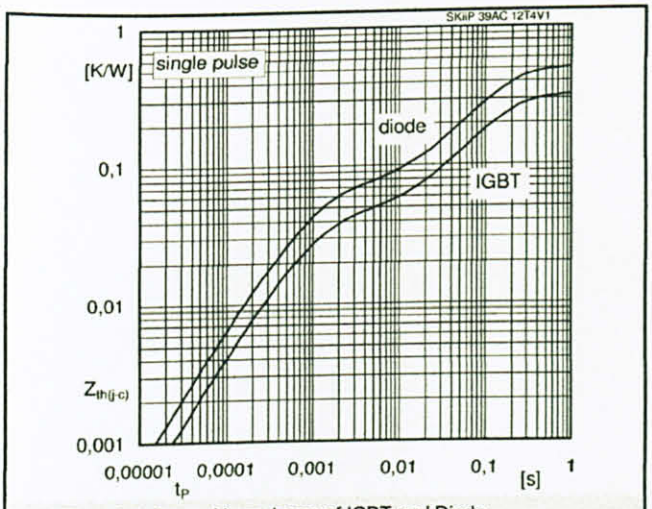


Fig. 9 Transient thermal impedance of IGBT and Diode

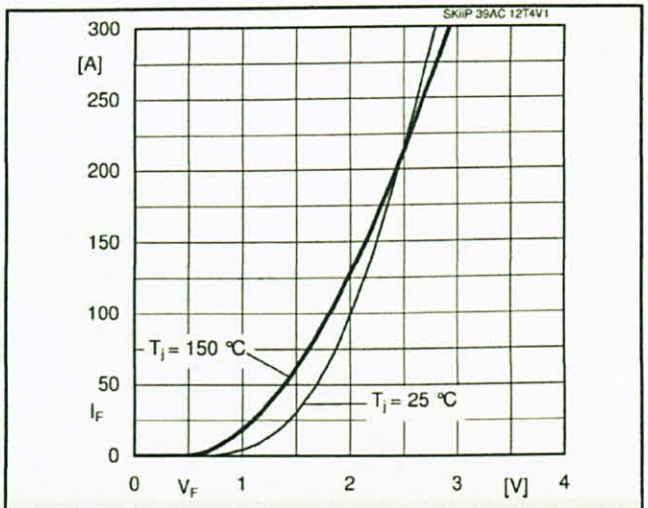


Fig. 10 CAL diode forward characteristic

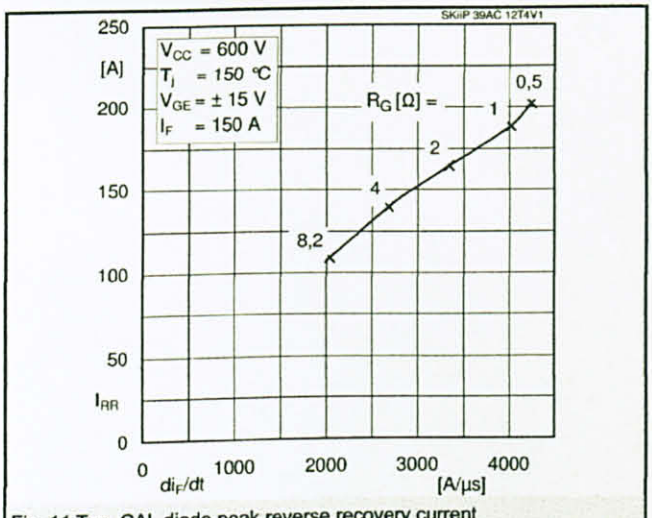


Fig. 11 Typ. CAL diode peak reverse recovery current

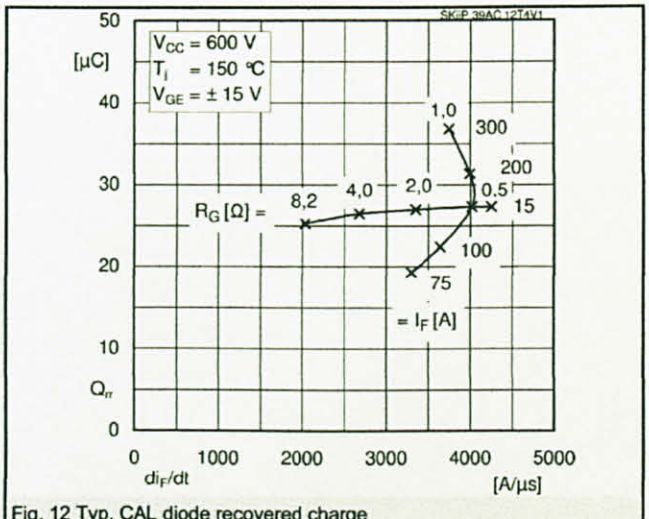
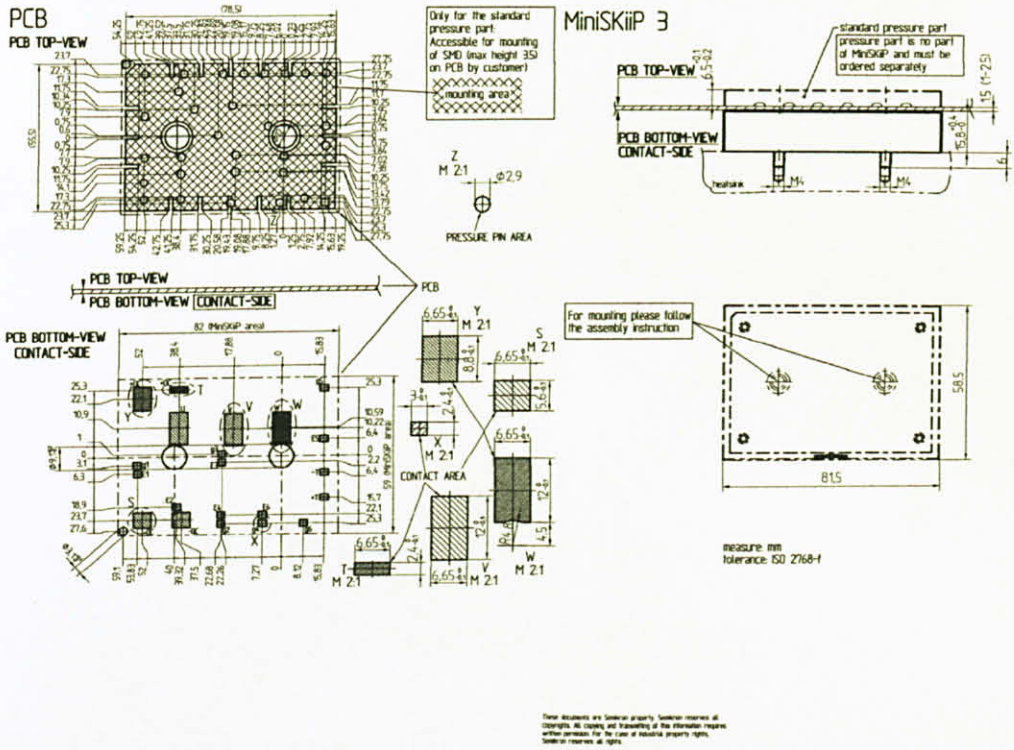


Fig. 12 Typ. CAL diode recovered charge

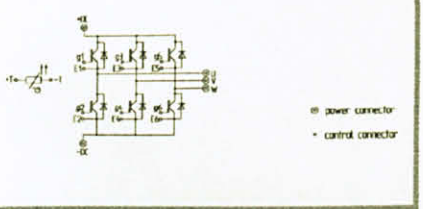
SKiiP 39AC12T4V1

UL recognized file

no. E 63 532

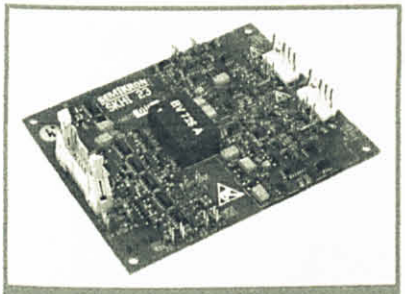


case



pinout

SKHI 23/17 (R) ...



SEMIDRIVER™

Medium Power Double IGBT Driver

SKHI 23/17 (R)

Features

- SKHI 23/17 drives all SEMIKRON IGBTs with V_{CES} up to 1700 V (V_{CE}-monitoring adjusted from factory for 1700 V-IGBT)
- Double driver circuit for medium power IGBTs, also as two independent single drivers
- CMOS / TTL (HCMOS) compatible input buffers
- Short circuit protection by V_{CE} monitoring
- Soft short circuit turn-off
- Isolation due to transformers (no opto couplers)
- Supply undervoltage monitoring (< 13 V)
- Error memory / ouput signal (LOW or HIGH logic)
- Driver interlock top / bottom
- Internal isolated power supply

Typical Applications

- High frequency SMPS
- Half and Full bridges
- Three phase motor inverters
- High power UPS

1) This current value is a function of the output load condition
2) Operating fsw = 0 Hz
3) This value does not consider t_{on} of IGBT and t_{MIN} adjusted by R_{CE} and C_{CE}; see also fig. 14
4) Matched to be used with IGBTs < 100 A; for higher currents, see table 4
5) With R_{CE} = 36 kΩ, C_{CE} = 470 pF; see fig. 6
6) Factory adjusted; other values see table 3

Absolute Maximum Ratings T_a = 25 °C, unless otherwise specified

Symbol	Conditions	Values	Units
V_S	Supply voltage primary	18	V
V_{iH}	Input signal voltage (HIGH) (for 15 V and 5 V input level)	V_S + 0,3	V
$Iout_{PEAK}$	Output peak current	± 8	A
$Iout_{AV}$	Output average current	± 50	mA
V_{CE}	Collector emitter voltage sense	1700	V
dv/dt	Rate of rise and fall of voltage (secondary to primary side)	75	kV/µs
$V_{isol\ IO}$	Isolation test volt. IN-OUT (2 sec. AC)	4000	V
$R_{Gon\ min}$	minimal R_{Gon}	2,7	Ω
$R_{Goff\ min}$	minimal R_{Goff}	2,7	Ω
$Q_{out/pulse}$	charge per pulse	4,8	µC
T_{op}	Operating temperature	- 25 ... + 85	°C
T_{stg}	Storage temperature	- 25 ... + 85	°C

Characteristics T_a = 25 °C, unless otherwise specified

Symbol	Conditions	min.	typ.	max.	Units
V_S	Supply voltage primary	14,4	15,0	15,6	V
I_S	Supply current (max.)		0,32[1]		A
I_{SO}[2]	Supply current primary side (standby)		0,12		A
V_{iT+}	Input threshold voltage (HIGH) min.				
	15 V input level	12,5			V
	for 5 V input level	2,4			V
V_{iT-}	Input threshold voltage (LOW) max.				
	for 15 V input level			3,6	V
	for 5 V input level			0,50	V
$V_{G(on)}$	Turn-on output gate voltage		+ 15		V
$V_{G(off)}$	Turn-off output gate voltage		- 8		V
f	Maximum operating frequency		see fig. 15		
$td(on)_{IO}$	Input-output turn-on propagation time		1,4		µs
$td(off)_{IO}$	Input-output turn-off propagation time		1,4		µs
$t_{d(err)}$	Error input-output propagation time		1,0[3]		µs
t_{TD}	Dead time		10[6]		µs
V_{CEstat}	Reference voltage for V_{CE} monitoring		6,3[5]		V
R_{Gon}	Internal gate resistor for ON signal		22[4]		Ω
R_{Goff}	Internal gate resistor for OFF signal		22[4]		Ω
C_{ps}	Primary to secondary capacitance		12		pF

Block diagramm SKHI 23

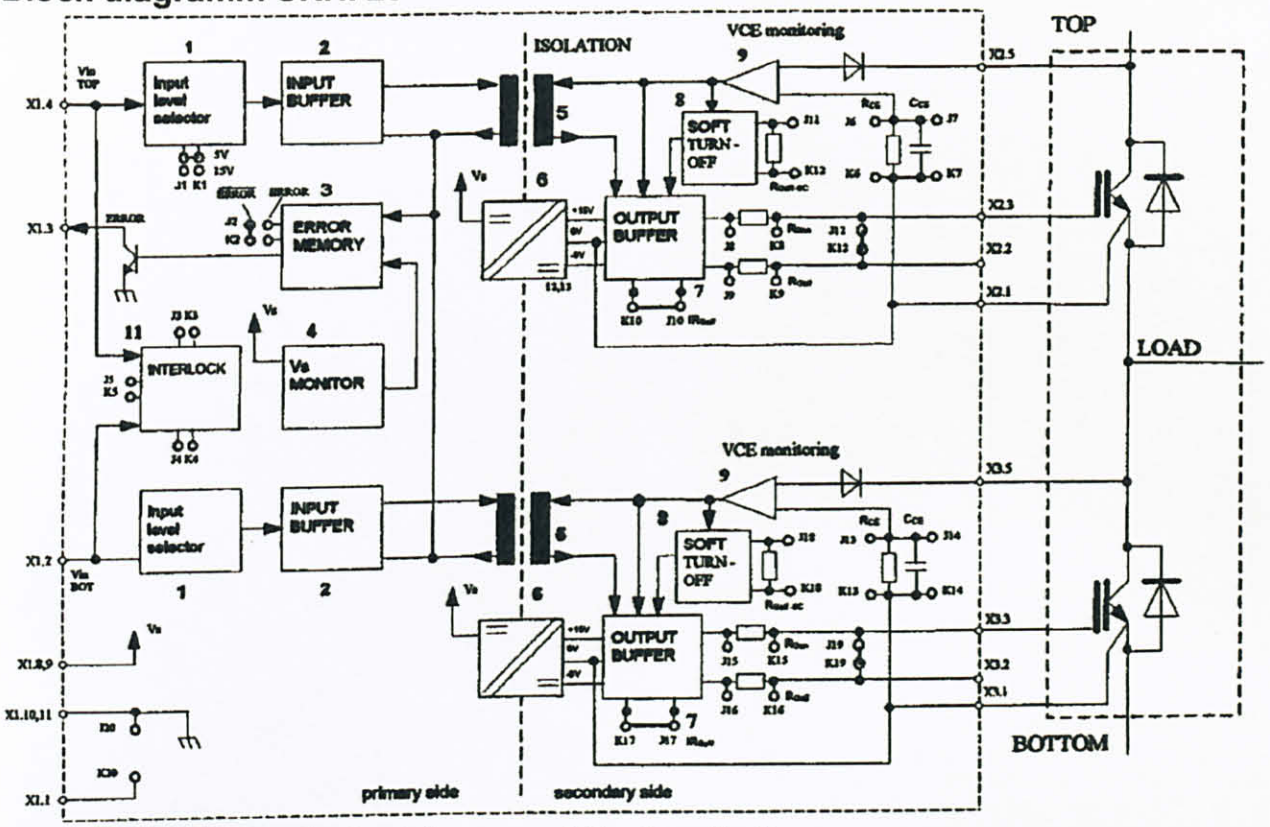
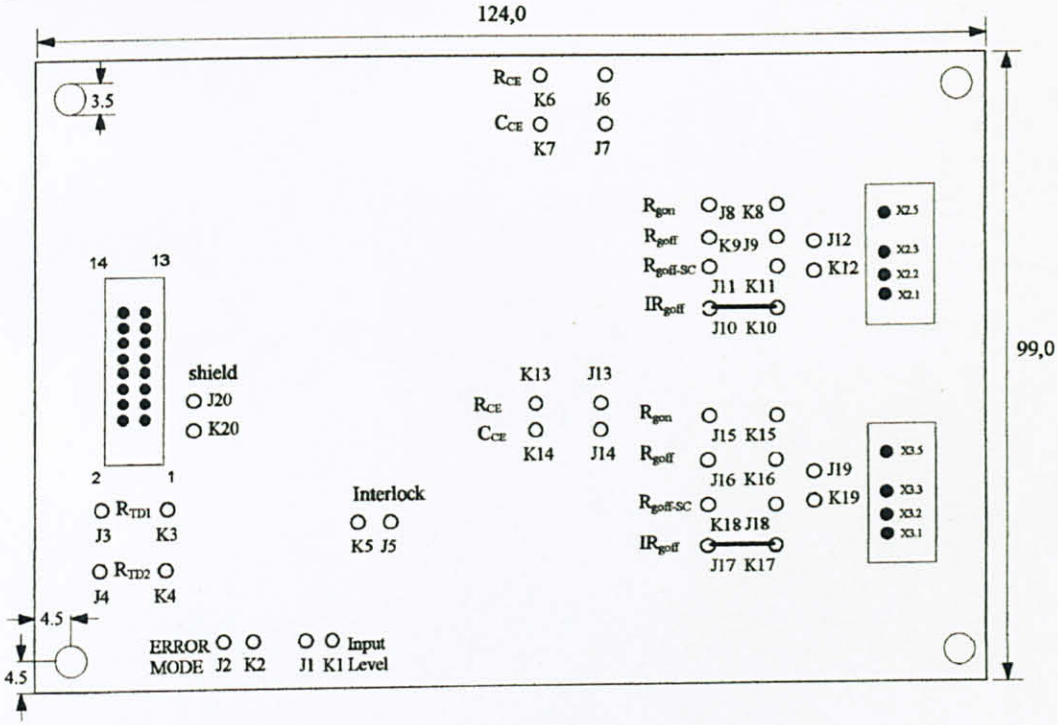


Fig. 1 The numbers refer to the description on page B14 – 45, section B.



Input connector = 14 pin flat cable according to DIN 41651
Output connector = MOLEX 41791 Series (mates with 41695 crimp terminals 7258)

Fig. 2 Dimensions (in mm) and connections of the SKHI 23

SEMIDRIVER™ SKHI 23/12
SEMIDRIVER™ SKHI 23/17

Medium Power Double IGBT Driver

Overview

The new intelligent double IGBT driver, SKHI 23 respectively SKHI 23/17 is a standard driver for all power IGBTs in the market.

SKHI 23/12 drives all IGBTs with V_{CE} up to 1200 V. SKHI 23/17 drives all IGBTs with V_{CE} up to 1700 V. To protect the driver against moisture and dust it is coated with varnish. The adaption of the drivers to the application has been improved by using pins to changing several parameters and functions. The connections to the IGBTs can be made by using only one MOLEX connector with 12 pins or by using 2 separate connectors with 5 pins for each IGBT.

The high power outputs capability was designed to switch high current double or single modules (or paralleled IGBTs). The output buffers have been improved to make it possible to switch up to 200 A IGBT modules at frequencies up to 20 kHz.

A new function has been added to the short circuit protection circuitry (Soft Turn Off), this automatically increases the IGBT turn off time and hence reduces the DC voltage overshoot enabling the use of higher DC-bus voltages. This means an increase in the final output power.

Integrated DC/DC converters with high galvanic isolation (4 kV) ensures that the user is protected from the high voltage (secondary side).

The power supply for the driver may be the same as used in the control board (0/+15 V) without the requirement of isolation. All information that is transmitted between input and output uses ferrite transformers, resulting in high dv/dt immunity (75 kV/µs).

The driver input stages are connected directly to the control board output and due to different control board operating voltages, the input circuit includes a user voltage level selector (+15 V or +5 V). In the following only the designation SKHI 23 is used. This is valid for both driver versions. Any unique features will be marked as SKHI 23/12 (V_{CE} = 1200 V) or SKHI 23/17 (V_{CE} = 1700 V) respectively.

A. Features and Configuration of the Driver

a) A short description is given below. For detailed information, please refer to section B. The following is valid for both channels (TOP and BOTTOM) unless specified.

b) The SKHI 23 has an INPUT LEVEL SELECTOR circuit for two different levels. It is preset for CMOS (15 V) level, but can be changed by the user to HCMOS (5 V) level by solder bridging between pins J1 and K1. For long input cables, we do not recommend the 5 V level due to possible disturbances emitted by the power side.

c) An INTERLOCK circuit prevents the two IGBTs of the half bridge to switch-on at the same time, and a "deadtime" can be adjusted by putting additional resistors between pins J3 and K3 (R_{TD1}) and pins J4 and K4 (R_{TD2}). Therefore it will be possible to reduce the deadtimet t_{TD} (see also table 3).
The interlocking may also be inhibit by solder bridging between pins J5 and K5 to obtain two independent drivers.

d) The ERROR MEMORY blocks the transmission of all turn-on signals to the IGBT if either a short circuit or malfunction of Vs is detected, a signal is sent to the external control board through an open collector transistor. It is preset to "high-logic" but can be set to "low-logic" (ERROR).

e) The V_s MONITOR ensures that V_s actual is not below 13 V.

f) With a FERRITE TRANSFORMER the information between primary and secondary may flow in both directions and high levels of dv/dt and isolation are obtained.

g) A high frequency DC/DC CONVERTER avoids the requirement of external isolated power supplies to obtain the necessary gate voltage. An isolated ferrite transformer in half-bridge configuration supplies the necessary power to the gate of the IGBT. With this feature, we can use the same power supply used in the external control circuit, even if we are using more than one SKHI 23, e.g. in three-phase configurations.

h) Short circuit protection is provided by measuring the collector-emitter voltage with a V_{CE} MONITORING circuit. An additional circuit detects the short circuit after a delay (adjusted with R_{CE} (this value can only be reduced) and C_{CE} (this value can only be increased) and decreases the turn off speed (adjusted by $R_{goff-sc}$) of the IGBT. SOFT TURN-OFF under fault conditions is necessary as it reduces the voltage overshoot and allows for a faster turn off during normal operation.

i) The OUTPUT BUFFER is responsible for providing the correct current to the gate of the IGBT. If these signals do not have sufficient power, the IGBT will not switch properly, and additional losses or even the destruction of the IGBT may occur. According to the application (switching frequency and gate charge of the IGBT) the equivalent value of R_{gon} and the R_{goff} must be matched to the optimum value. This can be done by putting additional parallel resistors R_{gon}, R_{goff} with those already on the board. If only one IGBT is to be used, (instead of paralleled IGBTs) only one cable could be connected between driver and gate by solder bridging between the pins J12 and K12 (TOP) as well as between J19 and K19 (Bottom).

j) Fig. 1 shows a simplified block diagram of the SKHI 23 driver. Some preliminary remarks will help the understanding:

- Stabilised +15 V must be present between pins X1.8,9 (V_s) and X1.10,11 (⊥); an input signal (ON or OFF command to the IGBTs) from the control system is supplied to pins X1.2 and X1.4 (V_{in}) where HIGH=ON and LOW=OFF. The pin X1.1 can be used as a shield for the input signals.
- Pin X2.5 on TOP (and X3.5 on BOT) at secondary side is normally connected to the collector of the IGBTs to monitor V_{CE}, but for initial tests without connecting the IGBT it must be connected to pin X2.1 on TOP (and X3.1 on BOT) to avoid ERROR signal and enable the output signals to be measured.
- The RESET is performed when both input V_{in} signals are zero (TOP = BOT = LOW).
- To monitor the ERROR signal in "high-logic", a pull-up resistor must be provided between pin X1.3 and V_s.
- Table 1 (see page B 14–46) shows the factory adjustment and the different possible adjustments of the pins.

B. Description of the Circuit Block Diagram (Fig. 1)

The circuit in Fig. 1 shows the input on the left and output on the right (primary/secondary).

1. Input level circuit

This circuit was designed to accept two different CMOS logic voltage levels. The standard level is +15 V (factory adjusted) intended for noisy environments or when long connections (l > 50 cm) between the external control circuit and SKHI 23 are used, where noise immunity must be considerate. For lower power, and short connections between control and driver, the TTL-HCMOS level (+5 V) can be selected by solder bridging between J1 and K1, specially useful for signals coming from uP based controllers.

Fig.3 Selecting J1, K1 for 5 V level (TTL-HCMOS)

When connecting the SKHI 23 to a control board using short connections no special attention needs to be taken (Fig. 4a).

Otherwise, if the length is 50 cm or more (we suggest to limit the cable length to about 1 meter), some care must be taken. The TTL level should be avoided and CMOS/ 15 V is to be used instead; flat cable must have the pairs of conductors twisted or be shielded to reduce EMI/RFI susceptibility (Fig. 4b). If a shielded cable is used, it can be connected to pinX1.1 and coupled to 0 V through a capacitor, resistor or by solder bridging between pins J20 and K20.

As the input impedance of the INPUT LEVEL SELECTOR circuit is very high, an internal pull-down resistor keeps the IGBT in OFF state in case the V_{in} connection is interrupted or left non connected.

The following overview is showing the input treshold voltages

V_{IT+} (High)	min	typ	max
15 V	9,5 V	11,0 V	12,5 V
5 V	1,8 V	2,0 V	2,4 V

V_{IT-} (Low)	min	typ	max
15 V	3,6 V	4,2 V	4,8 V
5 V	1,8 V	0,65 V	0,8 V

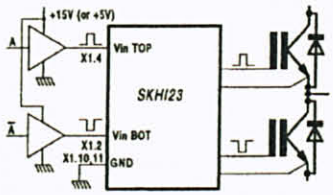


Fig. 4a Connecting the SKHI 23 with short cables

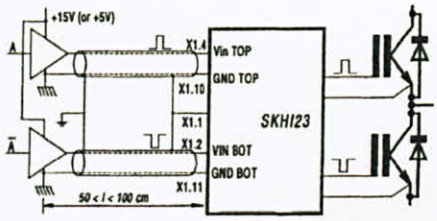


Fig. 4b Connecting the SKHI 23 with long cables

2. Input buffer

This circuit enables and improves the input signal V_{in} to be transferred to the pulse transformer and also prevents spurious signals being transmitted to the secondary side.

3. Error memory and RESET signal

The ERROR memory is triggered only by following events:

- short circuit of IGBTs
- V_s-undervoltage

In case of short circuit, the V_{CE} monitor sends a trigger signal (fault signal) through the pulse transformer to a FLIP-FLOP on the primary side giving the information to an open-collector transistor (pin X1.3), which may be connected to the external control circuit as ERROR message in "high-logic" (or "low-logic" if pins J2 and K2 are bridged). If V_s power supply falls below 13 V for more than 0,5 ms, the FLIP-FLOP is set and pin X1.3 is activated. For "high logic" (factory preset), an external R_p must be connected, preferably in the control main board. In this way the connection between main board and driver is also monitored.

Function	pin description	adjustment by factory		possibilities of functions
input level selector	J1 / K1	not bridged ⇒15V CMOS		soldering bridged ⇒5V HCMOS
error - logic	J2 / K2	not bridged ⇒HIGH-aktiv		soldering bridged ⇒LOW-aktiv
interlock time	J3 / K3 (TOP R_{TD1}) J4 / K4 (BOT R_{TD2})	not equiped ⇒max. t_{TD} = 10 µs		adjustment according table 3
interlock of TOP and BOTTOM	J5 / K5	not bridged ⇒interlock activ		soldering bridged ⇒no interlock
$R_{CE\ TOP}$	J6 / K6	**SKHI 23/12** not equiped ⇒ R_{CE}= 18 kΩ	**SKHI 23/17** not equiped ⇒ R_{CE}= 36 kΩ	adjustment according tab. 4a/b
$C_{CE\ TOP}$	J7 / K7	**SKHI 23/12** not equiped ⇒ C_{CE}= 330 pF	**SKHI 23/17** not equiped ⇒ C_{CE}= 470 pF	adjustment according tab. 4a/b
$R_{gon\ TOP}$	J8 / K8	**SKHI 23/12** not equiped ⇒ R_{gon}= 22 Ω	**SKHI 23/17** not equiped ⇒ R_{gon}= 22 Ω	adjustment according tab. 4a/b
$R_{goff\ TOP}$	J9 / K9	**SKHI 23/12** not equiped ⇒ R_{goff}= 22 Ω	**SKHI 23/17** not equiped ⇒ R_{goff}= 22 Ω	adjustment according tab. 4a/b
$IR_{goff\ TOP}$	J10 / K10	equiped with IR_{goff}= 0 Ω		adjustment according tab. 4a/b
$R_{goffSC\ TOP}$	J11 / K11	equiped with ⇒R_{goffSC}= 22 Ω		
TOP: one IGBT/ paralleled IGBTs	J12 / K12	not bridged ⇒2 cables to gates		soldering bridged ⇒1 cable to gate
$R_{CE\ BOT}$	J13 / K13	**SKHI 23/12** not equiped ⇒ R_{CE}= 18 kΩ	**SKHI 23/17** not equiped ⇒ R_{CE}= 36 kΩ	adjustment according tab. 4a/b
$C_{CE\ BOT}$	J14 / K14	**SKHI 23/12** not equiped ⇒ C_{CE}= 330 pF	**SKHI 23/17** not equiped ⇒ C_{CE}= 470 pF	adjustment according tab. 4a/b
$R_{gon\ BOT}$	J15 / K15	**SKHI 23/12** not equiped ⇒ R_{gon}= 22 Ω	**SKHI 23/17** not equiped ⇒ R_{gon}= 22 Ω	adjustment according tab. 4a/b
$R_{goff\ BOT}$	J16 / K16	**SKHI 23/12** not equiped ⇒ R_{goff}= 22 Ω	**SKHI 23/17** not equiped ⇒ R_{goff}= 22 Ω	adjustment according tab. 4a/b
$IR_{goff\ BOT}$	J17 / K17	equiped with IR_{goff}= 0 Ω		adjustment according tab. 4a/b
$R_{goffSC\ BOT}$	J18 / K18	equiped with ⇒R_{goffSC}= 22 Ω		
BOT: one IGBT/ paralleled IGBTs	J19 / K19	not bridged ⇒2 cables to gates		soldering bridged ⇒1 cable to gate
shield	J20 / K20	not bridged ⇒no screening		soldering bridged ⇒screening to GND

Adjustements for SKHI 23/12

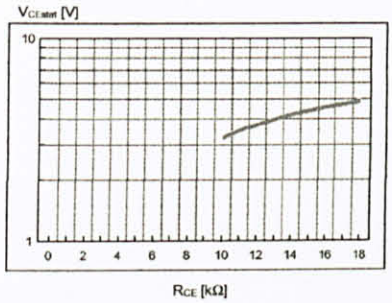


Fig. 7a V_{CEstat} as function of R_{CE}

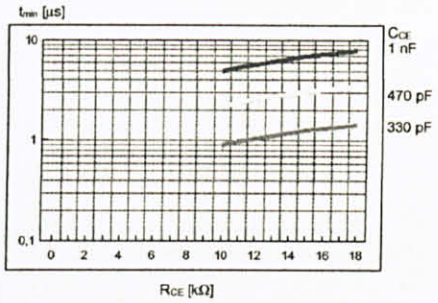


Fig. 7b t_{min} as function of R_{CE} and C_{CE}

Adjustements for SKHI 23/17

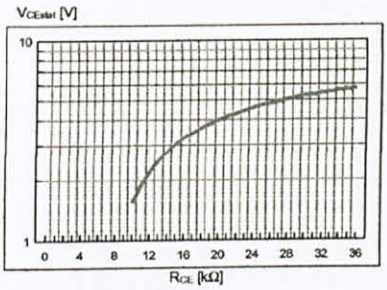


Fig. 7c V_{CEstat} as function of R_{CE}

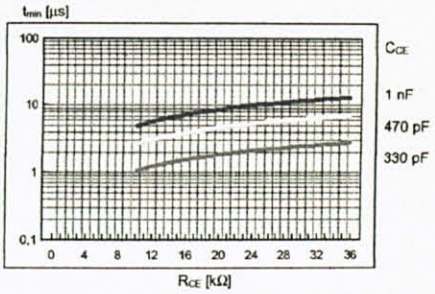


Fig. 7d t_{min} as function of R_{CE} and C_{CE}

The V_{CEstat} must be adjusted to remain above V_{CEsat} in normal operation (the IGBT is already in full saturation).

To avoid a false failure indication when the IGBT just starts to conduct (V_{CEsat} value is still too high) some decay time must be provided for the V_{CEref}. As the V_{CE} signal is internally limited at 10 V, the decay time of V_{CEref} must reach this level after V_{CE} or a failure indication will occur (see Fig.6, curve 1). A t_{min} is defined as function of V_{CEstat} and τ to find out the best choice for R_{CE} and V_{CE} (see Fig.6, curve 2). The time the IGBT come to the 10 V (represented by a "□" in Fig. 6) depends on the IGBT itself and R_{gon} used.

The R_{CE} and C_{CE} values can be found from Fig. 7a and 7b for SKHI 23/12 and from Fig. 7c and 7d for SKHI 23/17 by taking the V_{CEstat} and t_{min} as input values with following remarks:

- $R_{CE} > 10K\Omega$
- $C_{CE} < 2,7nF$

Attention!: If this function is not used, for example during the experimental phase, the V_{CE} MONITORING must be connected with the EMITTER output to avoid possible fault indication and consequent gate signal blocking.

10. R_{gon}, R_{goff}

These two resistors are responsible for the switching speed of each IGBT. As an IGBT has input capacitance (varying during the switching time) which must be charged and discharged, both resistors will dictate what time must be taken to do this. The final value of resistance is difficult to predict, because it depends on many parameters, as follows:

- DC-link voltage
- stray inductance of the circuit
- switching frequency
- type of IGBT

The driver is delivered with two R_g resistors (22 Ω) on the board. This value can be reduced to use the driver with bigger modules or higher frequencies, by putting additional resistors in parallel.

The outputs G_{on} and G_{off} were previewed to connect the driver with more than one IGBT (paralleling). In that case we need both signals ON/OFF separately to connect additional extremal resistors R_{gon} and R_{goff} for each IGBT. If only one IGBT is to be used, we suggest connecting both outputs together by solder bridging between pins J12 and K12 and respectiveley pins J19 and K19 to save on external connection. We also suggest using two restistors for R_{gon} and two resistors for R_{goff} when using low values of resistance, due the high current peak (up to 8 A) which could damage a single resistor.

11. Interlock

The interlock circuit prevents the IGBT turning on before the gate charge of the other IGBT is completely discharged. It should be set to delay time longer than the turn-off time of the IGBT. From the factory: t_{TD} = 10 µs. By putting additional resistors onto the pins J3/K3 ($R_{TD\ TOP}$) and onto the pins J4/K4 ($R_{TD\ BOT}$) the interlock time t_{TD} can be reduced (see table 3).

$R_{TD1} = R_{TD2}$	interlock time t_{TD}
10 kΩ	0,9 µs
22 kΩ	1,8 µs
33 kΩ	2,5 µs
47 kΩ	3,2 µs
68 kΩ	4,0 µs
100 kΩ	5,0 µs
330 kΩ	7,7 µs
not equiped (adjustement by factory)	10 µs

It have to be considered: $R_{TD1} = R_{TD2}$ 10 kΩ
Table 3 adjustement of interlock time

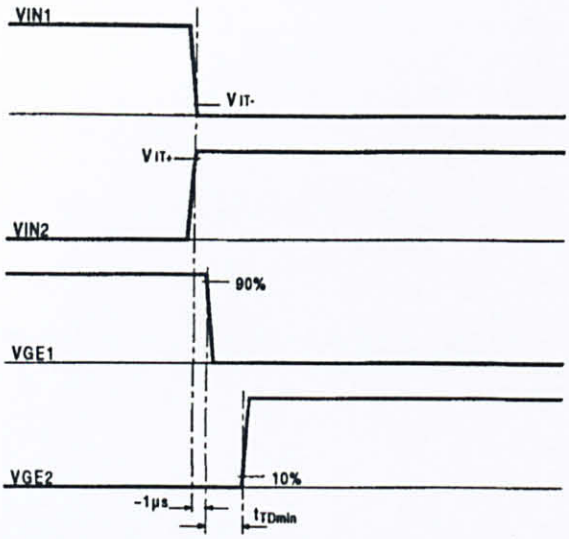


Fig. 8 Interlock function time diagram

C. Operating Procedure

1. One dual IGBT connection

To realize the correct switching and short-circuit monitoring of one IGBT-module some additional components must be used (Fig. 9).

Typical component values: *)

SK-IGBT-Module	R_{Gon} Ω	R_{Goff} Ω	C_{CE} pF	R_{CE} kW	I_{rgoff} Ω
SKM 75GB123D	22	22	330	18	0
SKM 100GB123D	15	15	330	18	0
SKM 145GB123D	12	12	330	18	0
SKM 150GB123D	12	12	330	18	0
SKM 200GB123D	10	10	330	18	0
SKM 300GB123D	8,2	8,2	330	18	0

Table 4a 1200V IGBT@ DC-link< 700V

SK-IGBT-Module	R_{Gon} Ω	R_{Goff} Ω	C_{CE} pF	R_{CE} kW	I_{rgoff} Ω
SKM 75GB123D	15	15	470	36	0
SKM 100GB123D	12	12	470	36	0
SKM 150GB123D	10	10	470	36	0
SKM 200GB123D	8,2	8,2	470	36	0
SKM 300GB123D	6,8	6,8	470	36	0

Table 4b 1700V IGBT@ DC-link< 1000V

*) Only starting values, for final optimization.

The adjustment of R_{goffSC} (factory adjusted R_{goffSC} = 22 Ω) should be done observing the overvoltages at the module in case of short circuit. When having a low inductive DC-link the module can be switched off faster.

The shown values should be considered as standard values for a mechanical/electrical assembly, with acceptable stray inductance level, using only one IGBT per SKHI 23 driver. The final optimised value can be found only by measuring.

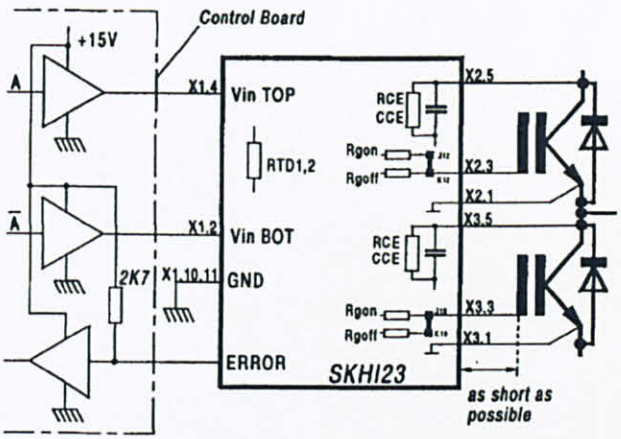


Fig. 9 Preferred dual IGBT-module standard circuit

2. Paralleling IGBTs

The parallel connection is recommended only by using IGBTs with homogeneous structure (IGHT), that have a positive temperature coefficient resulting in a perfect current sharing without any external auxiliary element. Care must be considered to reach an optimized circuit and to obtain the total performance of the IGBT (Fig. 10). The IGBTs must have independent values of R_{gon} and R_{goff}, and an auxiliary emitter resistor R_e as well as an auxiliary collector resistor R_c must also be used. The external resistors R_{gonx}, R_{goffx}, R_{ex} and R_{cx} should be mounted on an additional circuit board near the paralleled modules, and the R_{gon}/R_{goff} should be changed to zero ohms.

The R_{ex} has a value of 0,5 Ω and its function is to avoid the main current to circulate by the auxiliary ermitter what could make the ermitter voltage against ground unbalanced.

The R_{cx} assumes a value of 47 Ω and its function is to create an average of V_{CEsat} in case of short circuit for V_{CE}-monitoring.

The mechanical assembly of the power circuit must be symmetrical and low inductive.

The maximum recommended gate charge is 4,8 µC.

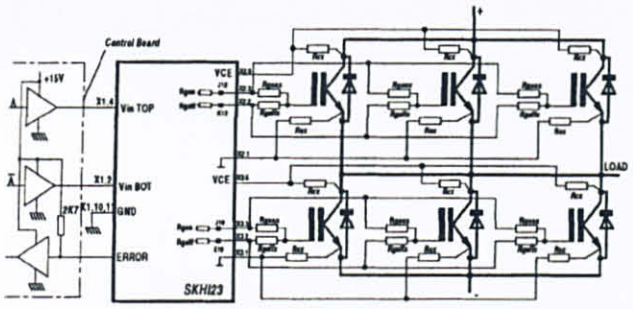


Fig. 10 Preferred circuit for paralleld dual IGBT-modules

D. Signal Waveforms

The following signal waveforms were measured under the conditions below:

- V_S = 15 V
- T_{amb} = 25 °C
- load = SKM75GB120D
- R_{CE} = 18 kΩ
- C_{CE} = 330 pF
- U_{DC} = 600 V
- I_C = 100 A

All results are typical values if not otherwise specified.

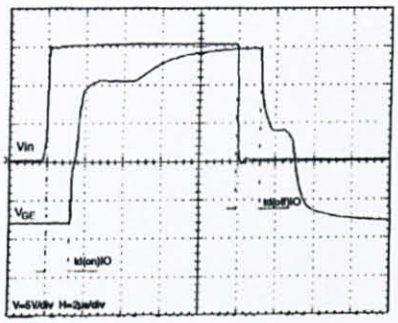


Fig. 11 Input and output voltage propagation time

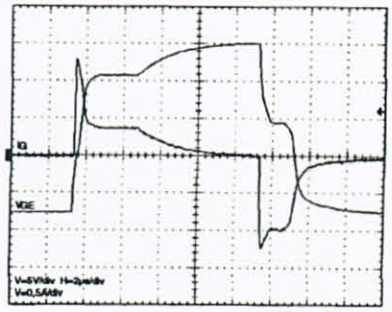


Fig. 12 Output voltage V_{GE} and output current (I_G)

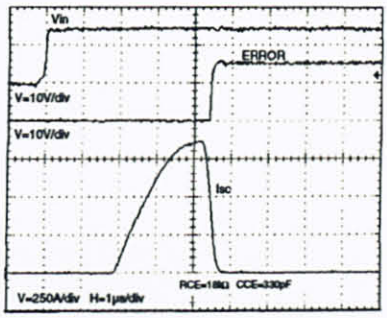


Fig.13 Short circuit and ERROR propagation time worste case (V_{IN} with SC already present)

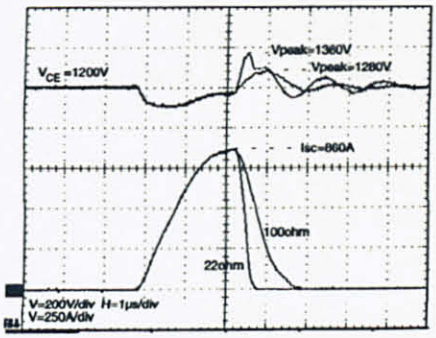


Fig.14 Effect of $R_{goff-SC}$ in short - circuit

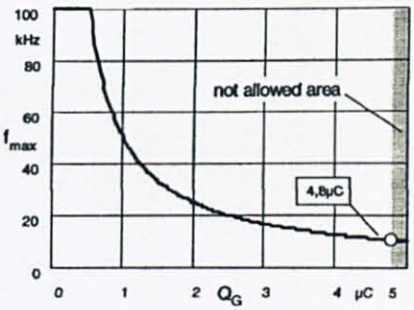


Fig. 15 Maximum operating frequency x gate charge

The limit frequency of SKHI 23 depends on the gate charge connected in its output pins.

If small IGBT modules are used, the frequency could theoretically reach 100 kHz. For bigger modules or even paralleled modules, the maximum frequency must be determinate (Fig. 15). Q_G is the total equivalent gate charge connected to the output of the driver. The maximum allowed value is limited (about 4,8 µC).

E. Application / Handling

1. The CMOS inputs of the driver are extremely sensitive to overvoltage. Voltages higher than (V_S + 0,3 V) or under - 0,3 V may destroy these inputs.

Therefore the following safety requirements are to be observed:

- To make sure that the control signals do not see overvoltages exceeding the above values.
- Protection against static discharges during handling. As long as the hybrid driver is not completely assembled the input terminals must be short circuited. Persons working with CMOS devices should wear a grounded bracelet. Any floor coverings must not be chargeable. For transportation the input terminals must be short circuited using, for example, conductive rubber. Places of work must be grounded. The same safety requirements apply to the IGBTs.

2. The connecting leads between the driver and the power module must be as short as possible, and should be twisted.

3. Any parasitic inductance should be minimized. Overvoltages may be damped by C or RCD snubber networks between the main terminals [3] = C1 (+) and [2] = E2 (-) of the power module.

4. When first operating a newly developed circuit, low collector voltage and load current should be used in the beginning. These values should be increased gradually, observing the turn-off behavior of the free-wheeling diodes and the turn-off voltage spikes across the IGBT by means of an oscilloscope. Also the case temperature of the power module should be monitored. When the circuit works correctly, short circuit tests can be made, starting again with low collector voltage.

5. It is important to feed any ERROR back to the control circuit to switch the equipment off immediately in such events. Repeated turn-on of the IGBT into a short circuit, with a frequency of several kHz, may destroy the device.

For further details ask SEMIKRON