

## **ABSTRACT**

This dissertation presents the finding on the project “**The Effect of Trim and Form Process on the Plated Leads of IC Packages**”. This work was done in collaboration with IDS Electronics Sdn Bhd which is a semiconductor assembly house. One of the highest volume product in IDS is the SOT-23-3L EIAJ IC package. It is of great interest for IDS to study the effect of the trim and form process on the plated lead frame of this package type. The trim and form process is carried out after the electroplating process, thus there is a possibility of the tin plating being compromised by the trim and form steps. The methods of metallography are used extensively in this project from preparation of all the samples until observations and analyses by optical and scanning electron microscopy. Thickness of electroplating at various locations along the plated leads will be made on images obtained via optical microscopy. Chemical composition of the plating will also be made using energy dispersive spectroscopy (EDS). It is found that there are variations of thickness of the plated leads especially at the bend locations of the leads. Some defects were also discovered such as plating peel-off and zero plating thickness. This project lays the groundwork for future work in order to improve the integrity of the plated leads of SOT-23-3L EIAJ package.

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## ABBREVIATIONS

IC	-	Integrated Circuits
SM	-	Surface Mounted
SEM	-	Scanning Electron Microscope
SiC	-	Silica Carbide