RESIST PROTECTION OXIDE TRANSISTOR AS SPIKING NEURON

By

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FINAL PROJECT REPORT

Submitted to Department of Electrical & Electronic Engineering
In Partial Fulfillment of the Requirement
For the Degree
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(Electrical & Electronic Engineering)

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Approved:

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AP. Dr. Tang Tong Boon

Project Supervisor

UNIVERSITI TEKNOLOGI PETRONAS

TRONOH, PERAK

December 2013

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

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Abdul Rasid Mohamed Mydin

ABSTRACT

Neural Network discovered since decade ago, as time goes on better understanding about the biological neural circuit is established. From here, the research focus shifted more to biologically characteristic model such as Spiking Neural Network. This circuit able to mimic biological spiking neural network. With a problem of processing step and noise adaptability, RPO (Resist-Protection-Oxide) transistor been introduced. These transistors contain defect rich RPO film in between gate, drain, and it able to enhance low frequency noise for more than two decade, allowing closer resemblance to the (biological) noisy neuron. Noise will be able to be control by adjusting drain voltage of RPO transistor.

ACKNOWLEDGEMENTS

The authors would like to thanks to Allah S.W.T for HIS blessing and guidance to overcome the challenges and trouble throughout the final year project period, and AP. Dr. Tang Tong Boon for his guidance, tireless even he is not in Malaysia but supporting me straight from Japan in order to complete this project.

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LIST OF FIGURE

1.0 PROJECT BACKGROUND

1.1 Background of study

Spiking neural network is not something new as it has been in discussion since before. This field keeps on rapidly progressing, mostly for medical purposes. Spiking neural network is a circuit that can provide almost same spike as human communication network in the brain. The basic unit in human communication brain part is neuron itself. Neuron is a bit noisy and unreliable computing cell as it will provide unreasonable type of spike. People have applied the concept for a lot of part such as speech, medical division such as cochlear implant, retinal prosthesis and many more. Part by part spiking neural network concept giving a noble solution to the future of the world.

1.2 Problem Statement

Neural circuits have been found since decades ago. Early work neural network in hardware focused on pulse modulated circuit design. As time goes by, better understanding about biological neural circuits is established and the research focus shifted to more biologically characteristic model, i.e. spiking neural network (SNN). While the circuit can mimic actual neuron more faithfully, SNN required extra processing step and simply need to gain the low-frequency noise to the level we want without considering the noise adaptability [9]. Simply mean that using normal SNN method requires having many steps in order to get required result and its doesn't have the controllability.

1.3 Significant of Project

Resist-Protection-Oxide (RPO) introduced recently, which contains defect rich RPO film in between gate and drain of the transistor. RPO transistor able to enhance low frequency noise for more than two decades while considering the noise adaptability. RPO transistor fabricated with standard CMOS size, which is 0.18 µm logic, which without any external mask or process steps. Therefore, it

has potential to scale up the network. If achieved, we can use it for many functions that using neuron as its basic building block, i.e. cochlear implant.

1.4 Objective

The objective of this project is to explore this 'Resist-Protection-Oxide' (RPO) transistor as building block for spiking neural network.

1.5 Scope of study

For current semester, author will focus on following matter:

- Understanding spiking neural network
- Creating simulation of spiking neural network
- Understanding RPO transistor
- Creating SNN using RPO transistor

2.0 LITERATURE REVIEW

2.1 Introduction to Neural Network

Human brain is very complicated; even we as human being also unable to detect the functionality of the brain as it contains ten thousand million basic units, that which is neuron [1]. Interneuron is a connection from output to input for over 100 micron, which the output connected through different regions such as brain, muscle and other from each sensory part to another [1]. Figure 1 shows soma, which is body of neuron and it connected part, which is axon and dendrite. Dendrite is long and not normal like shape of filament, which connected to the soma. On other part on soma, there is axon, which is electrically active and worked as output of neuron; even sometime axon is absent inside of neuron [1].

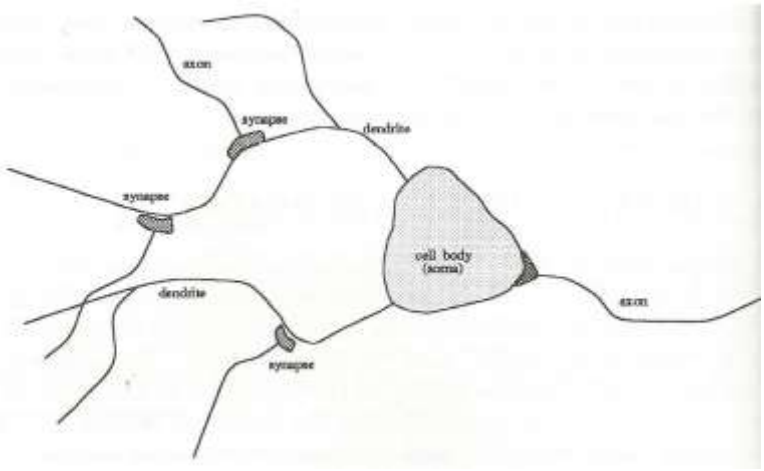


Figure 1: Neural System

2.2 Spiking Neural Network

Since biological neuron spike is very complicated, people hardly explore this field of technology but as time goes by, Spike Neural Network (SNN) becomes popular as a medium to explore and understand the function of brain [2]. SNN is a circuit designed by human to able mimic actual neural network in human biological body. Until now, there is a lot of simulation made in order to explore more on this field. A lot of circuit built to replicate the actual neuron spike. Earlier of research during decade ago, the circuit is complicated but as time goes by the circuit is simplified. By understanding SNN and its characteristic, many application is available scaling into real time system [3]. In term of this design, the range is wide as biological neuron proportionally with neural circuit [3].

According to [4]-[6] stochastic resonance (SR) is a phenomenon that occurs from the noise during the transmission of information. While from [7] SR is a nonlinear phenomenon that occurs during the process of random interference which interference of information can be enhanced in to the scale that can be calculated [7]. Noise playing a unique role in human biological neural system [8], as noise can enhance the human sensory part of function [10]. One of function in neural system is as sensory part, by following this order, SR can be useful to find sensory part in living being as it can detect and enhance the noise transferred from neural system [13]. To use SR, neuromorphic engineer tried to use noise for computation method [14]. Neuromorphic engineering is a method research field where the biological neural system implemented with “Very Large Scale Integration” (VLSI) technologies [15].

2.3 Resist Protection Oxide Transistor

In a neural spike circuit, modifying a standard transistor as a standard biological channel to mimic, which it increase the implementation of building blocks spike node, dendrite and synapses [15]. The process of increasing low frequency can be achieved to have intrinsic noise element in MOSFET area [12]. Proposed octagonal dual-gate transistor that possess extra gate, which functions have scalable noise during operation. In order to achieve a level for SR by enhancing the low signal noise, an extra step needs to perform in order to take care of the adaptability of transistor [9]. In order to fulfil these requirements, [9] also proposed a brand new technology of transistor that called "Resist-Oxide-Protection" (RPO).

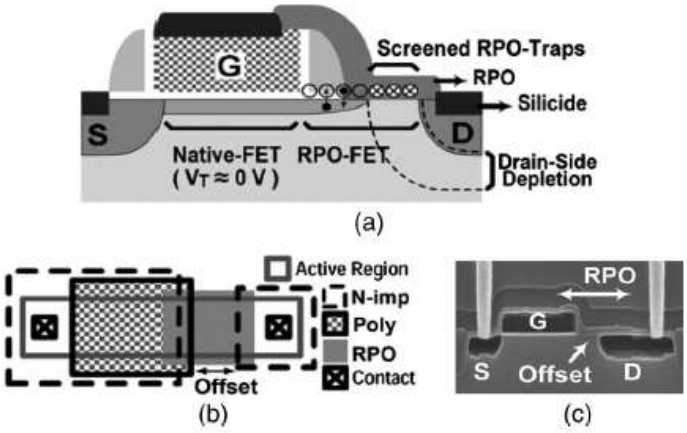


Figure 2 RPO-FET structure. (a) Cross-sectional view. (b) Layout. (c) SEM

This RPO transistor is using a defect-rich RPO film between drain and gate of the MOSFET in order to enhance the weak intrinsic noise [9].Drain part is shifted away from the edge of polygate which resulting offset occur between gate and drain. Defect rich RPO film inserted in the mosfet between gate and drain, which covering offset region. Using this film inside the transistor, drain voltage can generate any level of noise with a basic principle due to the increased detect density [9]. This RPO film covered offset region (screen RPO-trap) able to trap low frequency and enhance the frequency by more than two decade [9].

Drain voltage of RPO transistor able to control the level of offset between gate and drain, which mean it also can control the noise adaptability by controlling the offset [9].

3.0 METHODOLOGY

3.1 Detailed Project Activities

3.1.1 Completing FYP 1

By starting FYP 2, FYP 1 is necessary to be completed. The objective of FYP 1 is pre –requisite to do FYP 2. The basic understanding in FYP 1 used in the simulation in FYP 2.

3.1.2 Simulate Spiking Neural Network Circuit

Based on understanding on SNN during FYP 1, SNN circuit simulated using SPICE. As for this report, SPICE been used is National Instrument Multisim10.1.

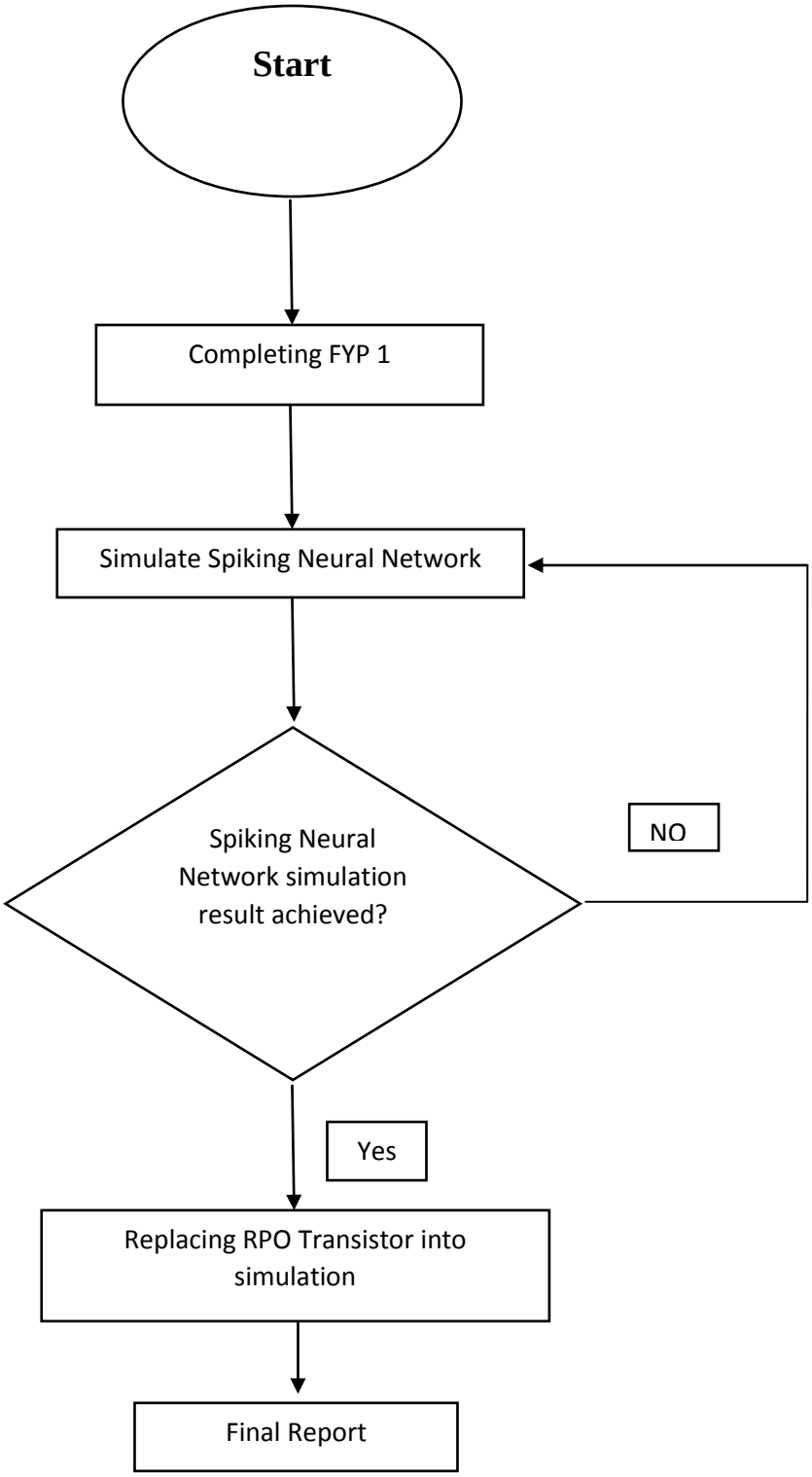
3.1.3 Simulate Spiking Neural Network Circuit using RPO Transistor

By completing SNN simulation, thisp project is proceed to the stage two which is by using RPO transistor. RPO transistor used to replace MOSFET in SNN circuit.

3.1.4 Final Report

By completing FYP 1, after simulating SNN circuit and SNN circuit with RPO transistor, the discussion and result is compiled in FYP final report. From here, a complete FYP final report achieved.

3.2 Research Methodology



3.4 Tools & Starting Simulation

Resist Protection Oxide as Spiking Neuron using a SPICE simulation in order to finish its project. Below is tools been used to finishing the project.

i. National Instrument Multisim 10.1

ii. Asus A55V series : Intel ® Core ™ i3-3110M CPU @ 2.40GHz with 64-bit Operating System

iii. Window 8 Profesional

Below is the method used to starting the simulation of this project.

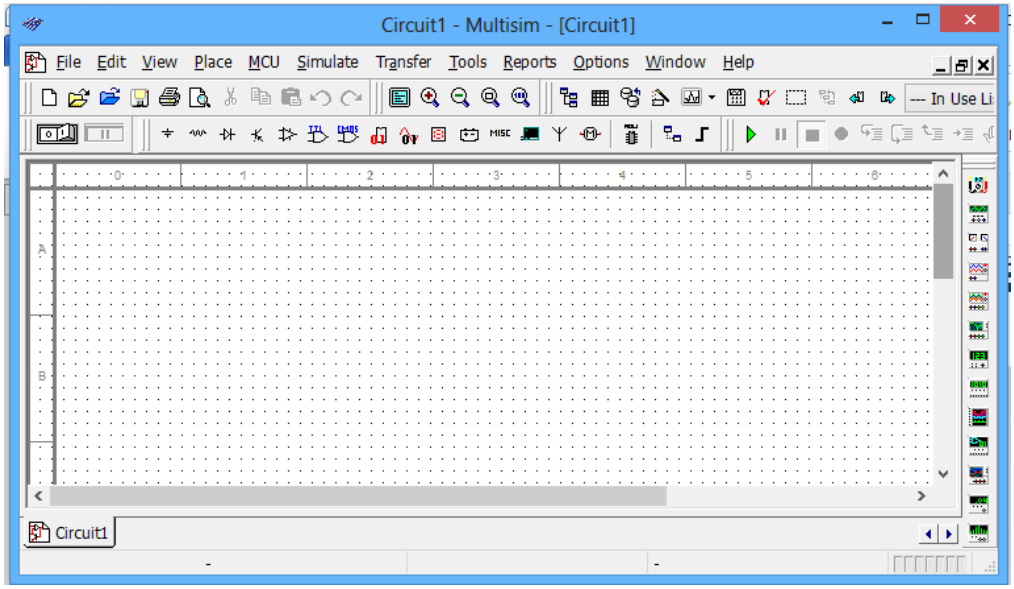


Figure 3 Multisim interface

Figure 3 shows the multisim interface which when double clicked the software it will be open. When open this multisim, there is some space, which allows us to insert an electronic component in it in order to make a complete circuit.

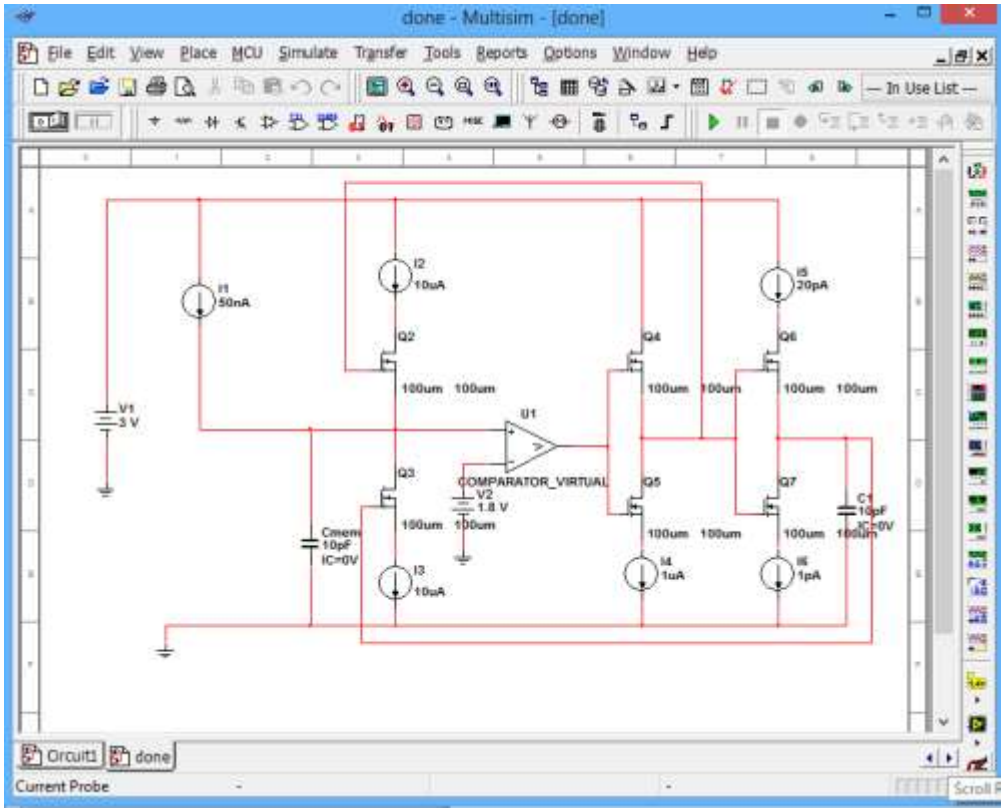


Figure 4 Inserting Electronic Circuit

Figure 4 show, the result when the electronic symbol inserted. The red line shows the wire connecting between each component. The circuit can be expanding, depend on our usage, as there is no limitation to it.

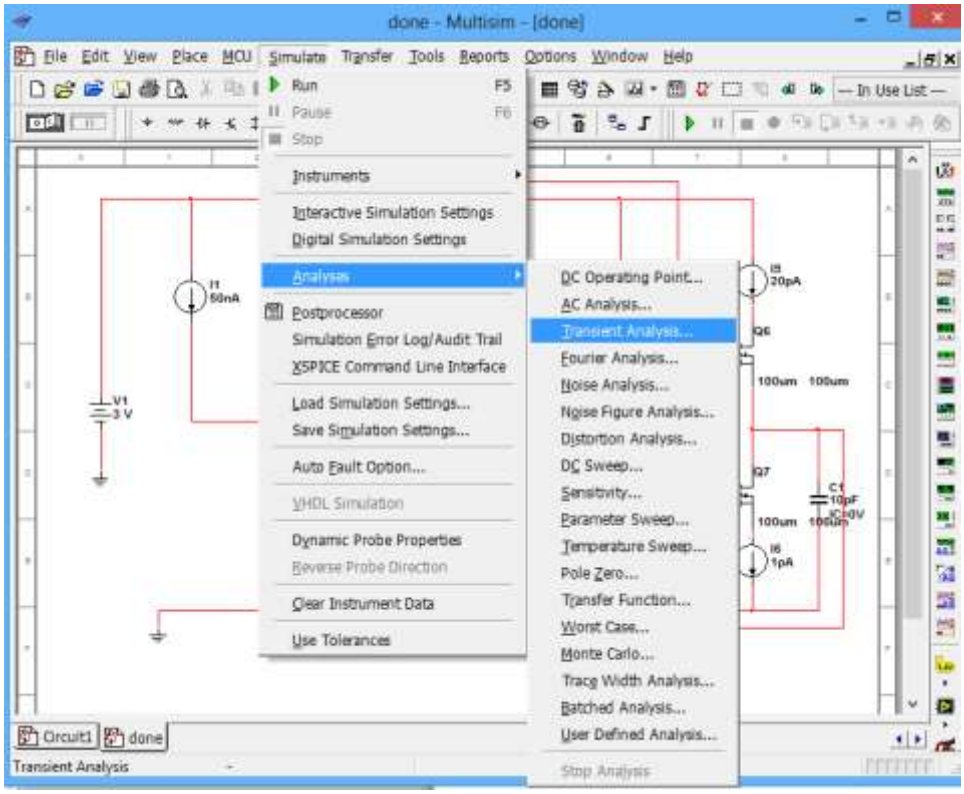


Figure 5 Interface to Transient Analysis

Figure 5 shows how to go to transient analysis, by clicking, simulate, and then go to analysis lastly to transient analysis. Transient analysis is the place for us to get the result Vmem which it calculate using numerical method time based.

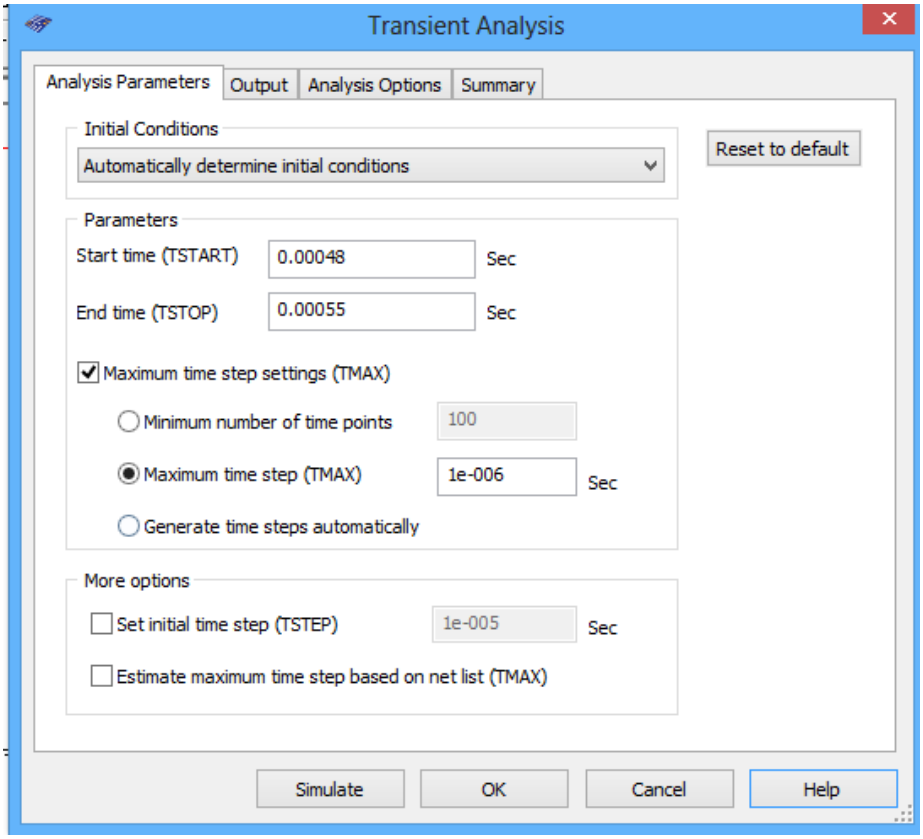


Figure 6 Transient Analysis

Figure 6 shows the transient analysis which indicate Start time (TSTART), End time TSTOP) and maximum time step setting (TMAX). Start time refer to when the simulation want to start, while end time is the time when simulation want to end. While maximum time step setting is the step time we want the simulation to process from start time to end time. Step time playing a main role to simulation to run using numerical method.

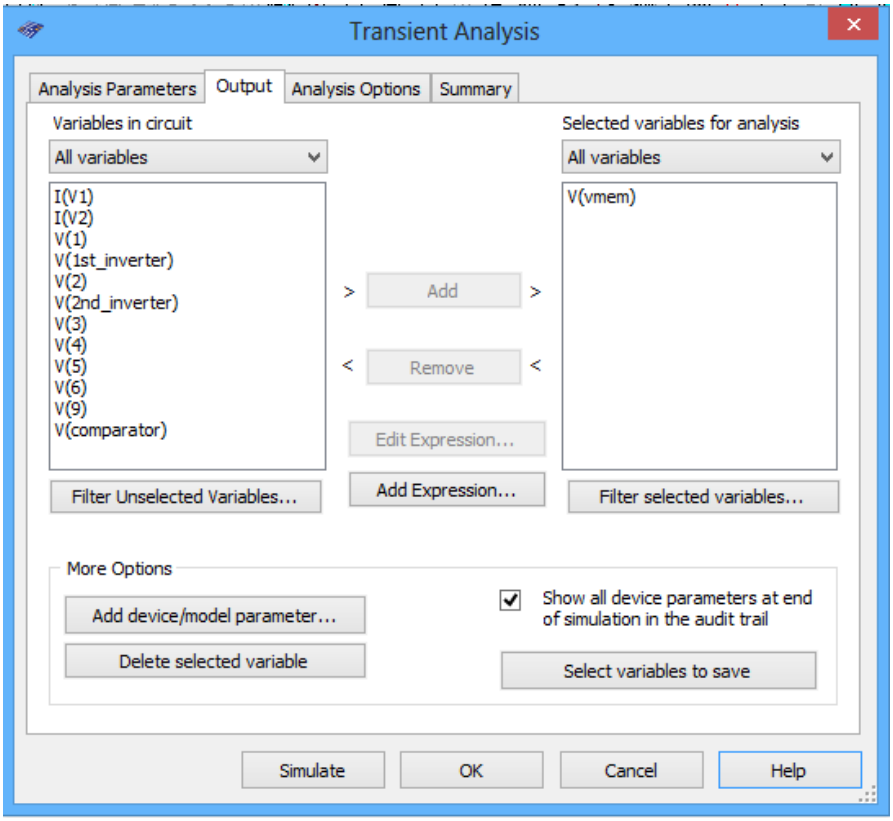


Figure 7 Output

Figure 7 shows the output which what we want to analysis. There is variable in circuit and selected variable for analysis. Variable in circuit is the variable available in circuit which we can measue it voltage or current. Usually those variable is measured from the wire. As for this project, the variable to measure already been labelled as V(1st_inverter), V(2nd_Inverter), V(Comaprator) and V(mem). Vmem is the voltage which we want in this project which is the action potential. Selected variable for analysis is the place we select from variable in circuit to analysis.As for this example, V(mem) is selected, which mean this project want to measure V(mem) variable. Finally,simulate button is click when all step is done which in the end will show the result in graph which in our case will show the spike event.

3.5 Summary of Project Activity Chart

Activities	Week 1	Week 2	Week 3	Week 4	Week 5	Week 6	Week 7	Week 8	Week 9	Week 10	Week 11	Week 12	Week 13	Week 14
Simulate SNN IN SPICE														
Simulate SNN with RPO														
Discussion on Result Obtained														
Final Report														

4.0 RESULT & DISCUSSION

4.1 Theory

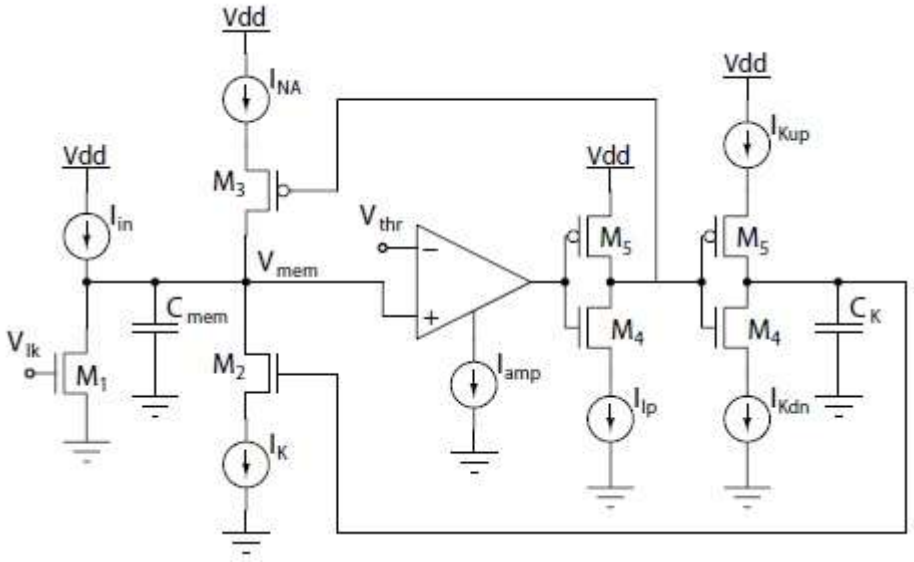


Figure 8 Axon-Hillock Spiking Neural Network

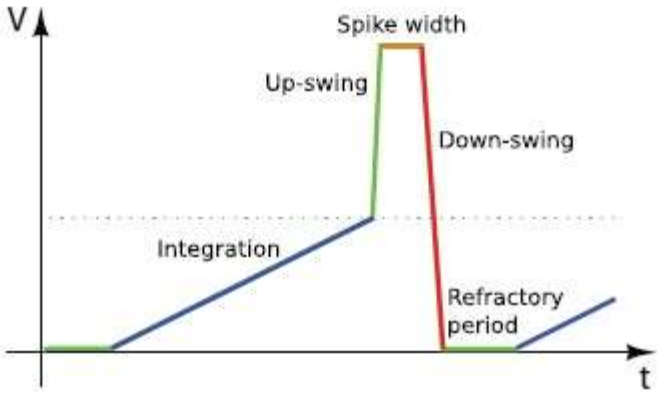


Figure 9 Axon-Hillock Spiking Neural Network spike

Figure 8 shows circuit of Axon-Hillock Spiking Neural Network which been established by Van Schaik [2], [3]. This circuit produces a spike activity when the membrane voltage crosses threshold voltage, which it also depends on the geometry of transistor and VLSI process characteristic. This proposed circuit is

applicable for both setting explicit spiking thresholds and implementing an explicit refractory period. From the figure, we can see that membrane voltage varies with signal conditioning.

Membrane capacitance in the circuit represents membrane of a biological neuron while the gate voltage Vlk of nFET controls membrane leakage current. With the input zero, membrane voltage will be drawn to be in its resting potential by leakage current. Iin, which is excitatory current, add charge to membrane capacitance while inhibitory input removes charge from membrane capacitance. If excitatory current larger than leakage current applied, membrane voltage increases from its resting potential. In the comparator, membrane voltage and threshold voltage compared, if membrane voltage larger than threshold voltage, action potential generated. The output of comparator, which is rise to the positive power supply, will go through inverter and it will go low which it will allowing sodium current to pull membrane potential. Second inverter will allow capacitance Ck to be charged at a speed which controlled by current Ikup. When Ck reached the high limit to allow conduction of nFET of M2, potassium current Ik will discharge the membrane capacitance. Ikup control the spike width, which it delays between opening of the sodium channels and opening of potassium channel inversely proportional to Ikup. Here, membrane voltage will drop lower than threshold voltage, which the output of first inverter is high and it will cut off Ina current. While second inverter will allow Ck to discharge Ikdn. If Ikdn is low, voltage in Ck decrese slowly and as long it stay high enough to allow Ik discharge membrane capacitance it will impossible to stimulate neuron for Iex lower than Ik. Therefore, Ikdn controls refractory period of neuron [3].

4.2 Simulation

Based on above part understanding a Spiking Neural Network Circuit created in PSPICE simulation platform as shown in figure 10.

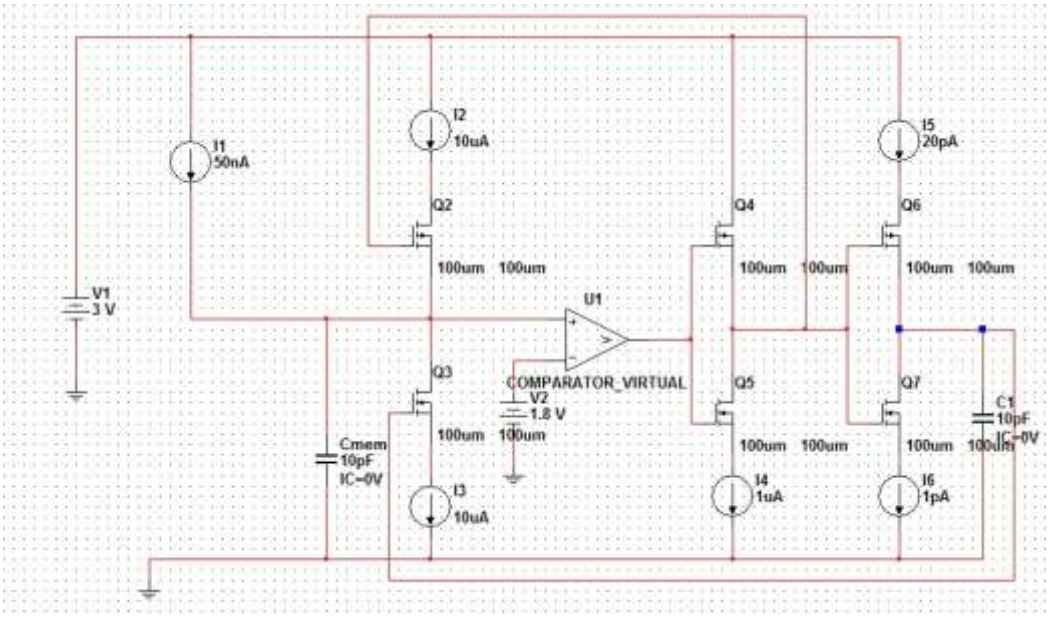


Figure 10 Spiking Neural Network Circuit

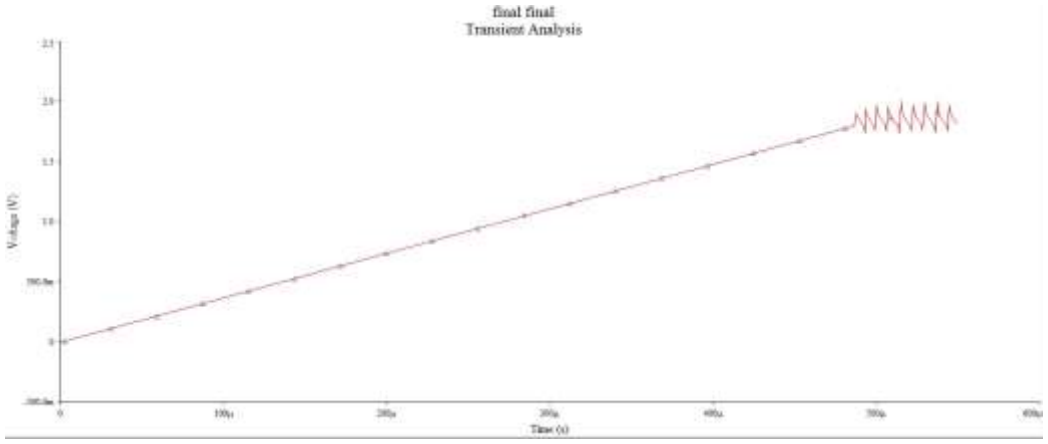


Figure 11 Vmem from 0s

Figure 11 is Vmem from initial condition of 0V from 0s. Vmem rise from 0 to threshold point which is 1.8V. This period is called integration period where when Iin is more than Ilk, action potential will rise from is resting period (ground).

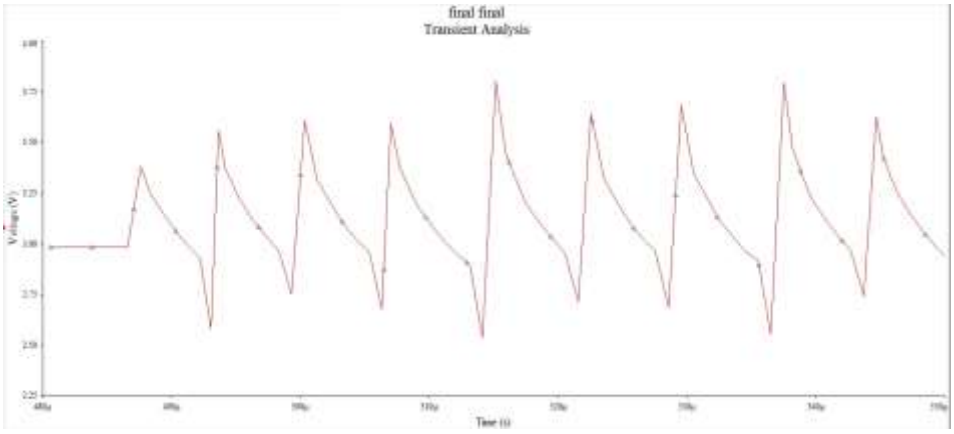


Figure 12 Vmem from 480us

Figure 12 shows Vmem within period from 480us till 550us which is zoomed in from figure 11. From this figure we can see up-swing, down-swing and spike width.

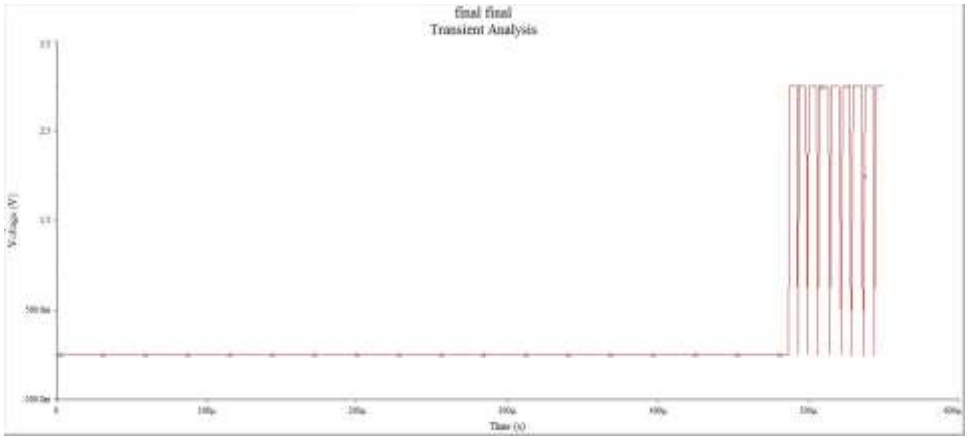


Figure 13 Comparator from 0s

Figure 13 shows the output of comparator which at certain point, comparator show low value where, this value is when Vthr higher than Vmem. Comparator value rises up when Vmem reach 1.8V.

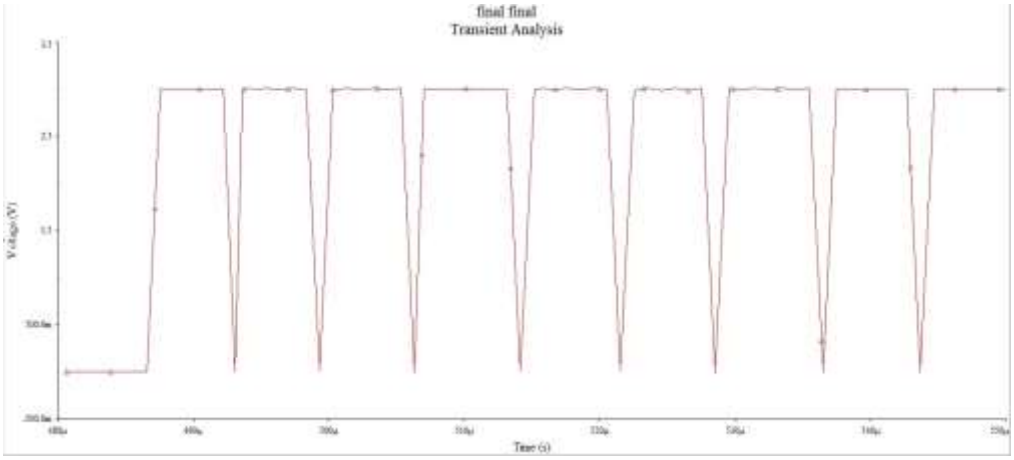


Figure 14 Comparator from 480us

Figure 14 shows comparator as from 480us which shows is rising till certain point it maintain stable and fall down.

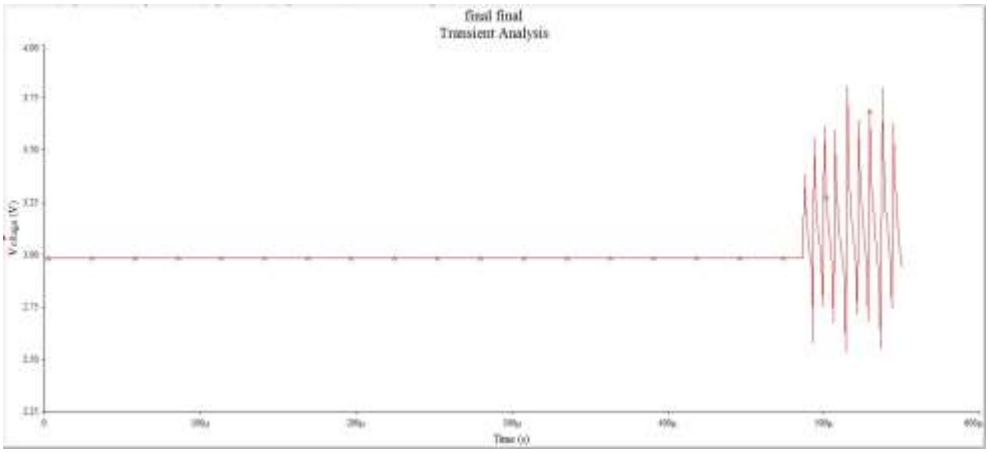


Figure 15 First Inverter from 0s

Figure 15 shows output of inverter, which came from the output of comparator from 0s. The output of inverter shows a constant value until certain point, it start to trigger. Its initial condition is 3V.

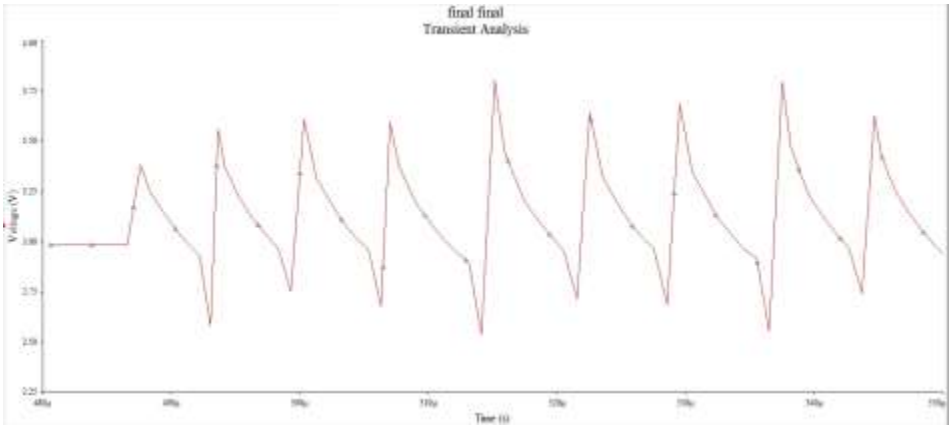


Figure 16 First inverter from 480us

Figure 16 is zoomed version of figure 10. It indicate the rise time and fall time of inverter affect from the result from comparator. If comparator fall, inverter will rise, if comparator rise, inverter rise. This inverter will on Q2 when its fall to able to make up-swing in Vmem.

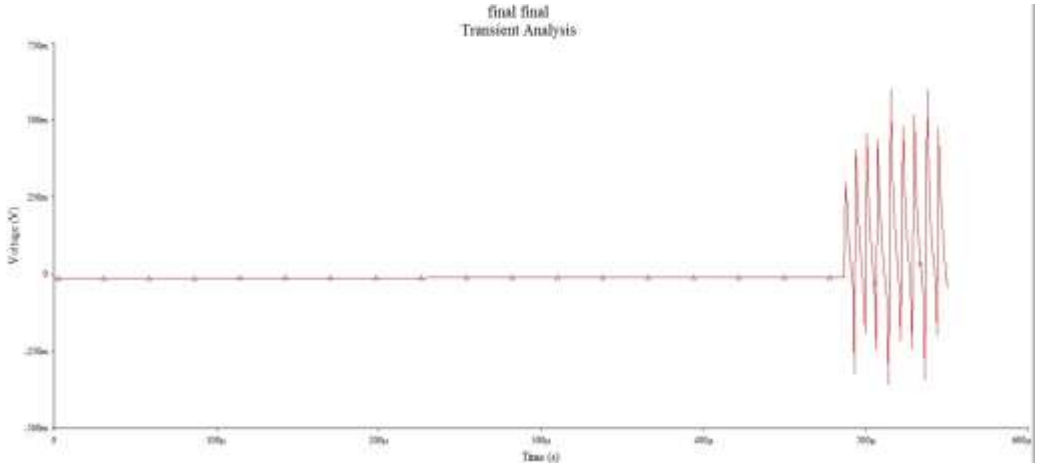


Figure 17 Second inverter from 0s

Figure 17 shows the result on second inverter which after passes through first inverter. Second inverter initial condition is 0V.

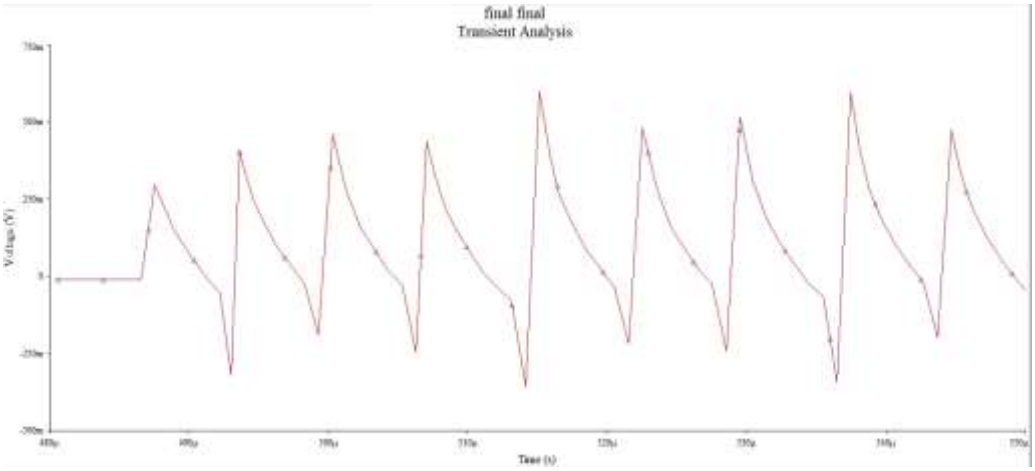


Figure 18 Second Inverter from 480s

Figure 18 shows second inverter in scale of 480us to 550us. As can see in the figure, the capacitor playing main role for this output which to charge and discharge. I5 will charge C1 to rise and I6 is to set the discharge time for capacitor C1.When C1 fully charge, it enable Q3 to on which allow Vmem to go to 1.8V again.

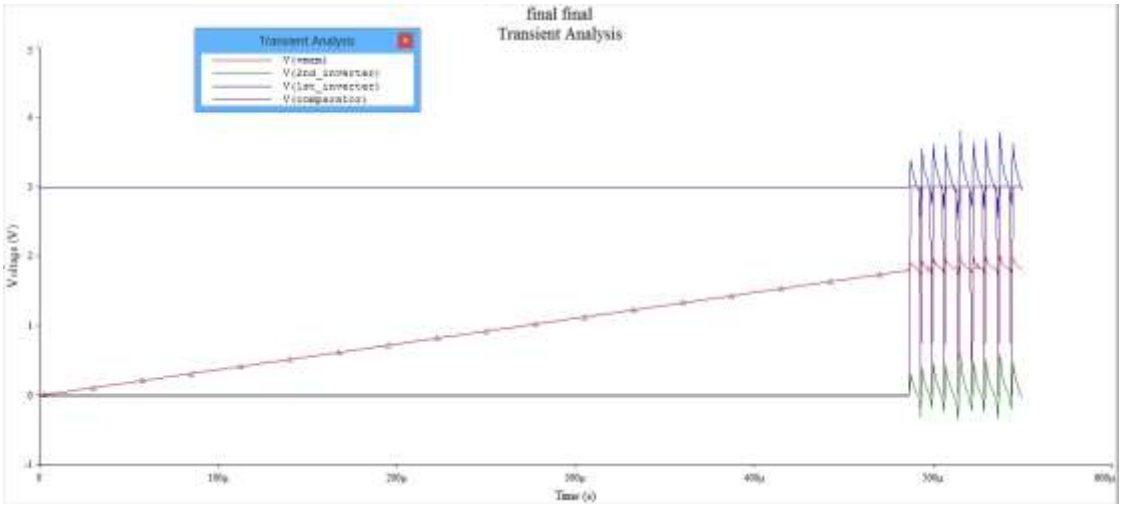


Figure 19 Overall views from 0s

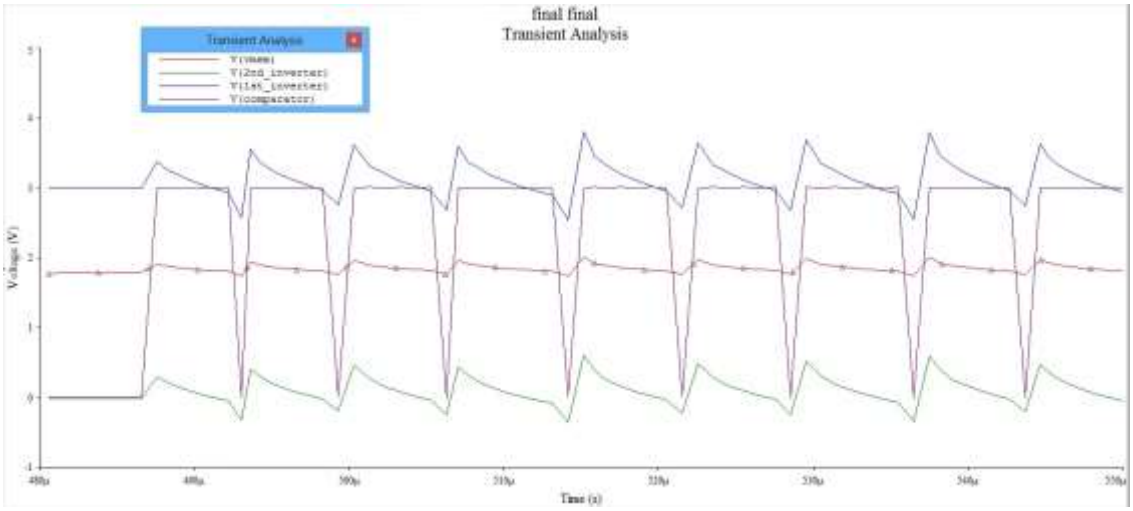


Figure 20 Overall view from 480us

Figure 19 shows overall view, which includes Vmem, voltage at first inverter, voltage at second inverter and output of comparator from 0s. While Figure 20 is the same, result which from 480us for better view. In figure 19 we can see that Vmem rise from its resting period as Iin is inserted. When Vmem equal to Vthr, the comparator output rise up into positive supply which allow first inverter to fall down. The outcome from second inverter will allow Q2 on and allow I2 to pull voltage to Vmem, which create period call “up-swing”. As can see in the figure 20, the charging period of C1 controlling Vmem “spike width” as Longer C1 charge, Vmem spike width will more longer. When the charging of C1 reach high, it will turn Q3 on and allow Vmem to fall to be same as Vthr. Charging time and discharging time of C1 is controlled by adjusting I5,I6 and value of C1.

5.0 CONCLUSION

The purpose of the project is to explore the RPO transistor using Spiking Neural Network circuit. In order to fulfill it, understanding the whole circuit of Spiking Neural Network is a compulsory. This circuit output shows a neuron activities spike for a single neuron. The spike needs to have resting period, integration, up-swing, spike width, down-swing and refractory period. All this activates will occur in membrane voltage of the circuit.

In FYP 2 the studies in FYP 1 used to create simulation of SNN circuit using SPICE simulation platform. Result obtained is not same from expected result and more work to be done. The process to control the spike is a lot as to control single Vmem need to take care of other parameter. To control single step of Vmem need to control other thing such as to control up-swing, need to control output of comparator to reach positive supply by Vmem exceeding vthr. From this output of comparator, need to control first inverter to be fall down as it will be able to turn on Q2, which allow supply to Vmem, and Vmem will rise to up-swing.

6.0 FUTURE WORK

Based on literature review and theory, Spiking Neural Network circuit simulated in SPICE platform. This simulation as currently is not complete and need to do further work out. The outcome needs to obtain as in figure 9 which include integration period, up-swing period, spike width period, down-swing period and refactory period.

By finishing the normal spiking neural network, RPO transistor need to be substitute with nFET and pFET, in order to achieve the objective.

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