Uniformity of Plating Thickness of IC Packages at

Various Locations on its Lead Frame

by

Farah Liyana bt Ab Ghani

Dissertation submitted in partial fulfilment of

the requirements for the

Bachelor of Engineering (Hons)

(Mechanical Engineering)

JUNE 2010

Universiti Teknologi PETRONAS
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CERTIFICATION OF APPROVAL

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Approved by,

_____

(Dr. Azmi Bin Abdul Wahab)

UNIVERSITI TEKNOLOGI PETRONAS

TRONOH,PERAK

JUNE 2010

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

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FARAH LIYANA BINTI AB. GHANI

ABSTRACT

This report outlines a project entitled 'Uniformity of Plating Thickness of IC Packages at Various Locations on its Lead Frame'. The project is conducted with the collaboration of IDS Electronics Sdn Bhd, a company that offers semi conductor assemblies and services. IC package used in this study is SOT-23-3L EIAJ matrix lead frame with tin plating since it is the most critical product in IDS Electronics that frequently having problem during its plating process. Hence, this project aims to measure plating thickness at various locations on its tin plated lead frame and simultaneously acts as continuous quality improvement (CQI) for this particular package. Metallographic technique has been employed entirely throughout this study in order to measure the plating thickness of IC lead frame. The result from this study shows that the average tin plating thickness of SOT-23-3L EIAJ IC package lead frame is 14.976 μm and its standard deviation of 2.458 μm. Plating thickness measured from this random condition plating solution show some variations of thickness but no measurements were found to lie outside the thickness specification range of 7μm to 20μm [Joseph Gauci, 2002]. Variations in surface finish were also apparent depending on location of the lead frame. Outputs of this study may ensure the company to produce better product with high quality on top of plating process can be performed with more practical and cost saving in the future production.

ACKNOWLEDGEMENT

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Finally, I thank my parents, other family members, friends and colleagues for their support and company all through and particularly, during the difficult times towards completion of this study.

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CHAPTER 1

INTRODUCTION

1.1 Background of Study

The study entitled 'Uniformity of Plating Thickness of IC Packages at Various Locations on its Lead Frame' had been conducted with the collaboration of IDS Electronics Sdn Bhd, a company which offers semiconductors assembly and test services. The company located in Bandar Seri Iskandar is manufacturing IC or integrated circuit as the main product. In IDS Electronics, IC is entirely fabricated from the first initial stage of wafer processing until final stage of IC packaging.

IC packaging is the final stage of semiconductor device fabrication comprises of molding, sealing, plating, marking and trims and form processes. The technique employed in this plating process is called electroplating. It is used for depositing a layer of metal over the leads to protect against corrosion and abrasion. Electroplating uses electrical current that passes through an electrolyte containing solution of metal to be plated.

The density of electrical current in electroplating may differ accordingly to the required plating quality which leads to a property called current density. Current density becomes a concern because it strongly influences the deposition rate of the electroplating, plating adherence and plating quality. Besides, current density may also vary over the surface of a part due to geometry design.

1.2 Problem Statement

As a semiconductor assembly company, IDS Electronics is usually looking for methods to improve their services to customers. For one particular product, which is the SOT-23-3L EIAJ package, the company is interested to know the capabilities of their electroplating process, so further refinements and optimizations can be carried

out to improve the process further. Currently, the production of the IC packages is carried out using essentially the same parameters on various solutions and lead frame geometries. Thus, the plating process may not be optimized which may lead to plating quality issues such as thickness and surface finish. In fact, one of the main challenges is to ensure uniform plating with a high deposition rate. Therefore it becomes an important task to investigate the localized effects of the tin-plating process on matrix lead frame for SOT-23-3L IC package. The effects of plating thickness concerned are in terms of thickness, surface finish, and material composition.

1.3 Objectives

The objectives of this study are as follows:

- To measure the tin-plating thickness of IC leads at various locations of lead frame plated.
- To study the uniformity and appearance of plating thickness over the IC leads at various location.
- To verify the elemental composition of tin plating solution and its base metal.

1.4 Scope of Study

The scope of this project is to study the uniformity of plating thickness at various locations on its lead frame. Surface finish and plating composition with respect to the lead frame locations will also be considered. The IC package used in this study is SOT-23-3L EIAJ matrix lead frame with tin electroplating. SOT-23-3L EIAJ has been chosen because it is the highest volume product in IDS Electronics, thus maintaining and improving the quality of this product is desirable.

1.5 Significance of Study

The uniformity of plating thickness of SOT-23-3L EIAJ leads may help IDS Electronics to systematically document the statistics regarding the tin-plating thickness of IC lead frame. Furthermore, it is also imperative to document the composition and surface finish of the tin-plating with respect to the location on its leadframe.

These statistics are important parameters for lowering material and energy consumption as well as minimizing scrap and maximizing productivity. The results which will be obtained at the end of this project may ensure the company to produce better product with high quality. Besides the plating process can be performed in more practical and cost saving in the future production.

CHAPTER 2

LITERATURE REVIEW AND THEORY

2.1 IC Package

IC or integrated circuit is a miniaturized electronic circuit consisting mainly of semiconductor devices while IC package is a container for an integrated circuit. The package contains an IC chip, a piece of silicon on which transistors and diodes embedded and interconnected to function as an electronic circuit. The casing usually provides metal leads which are sturdy enough to electrically and mechanically connect the fragile chip to the circuit board.

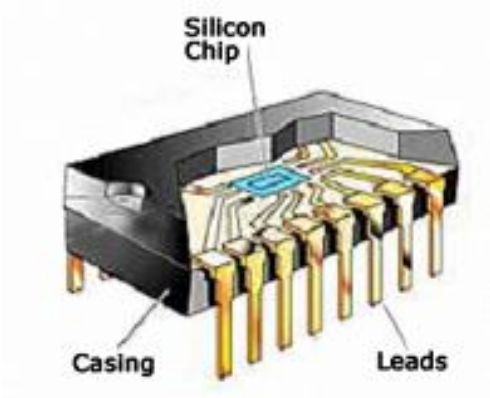


Figure 1: IC Package [Fairchild Semiconductor, 2007]

2.2 IC Fabrication Process

Fabrication of integrated circuit involves many process steps that can be divided into two major parts namely front-end assembly and back-end assembly [Omron Corporation, 2008]. Figure 1 below shows the process steps in both assembly parts.

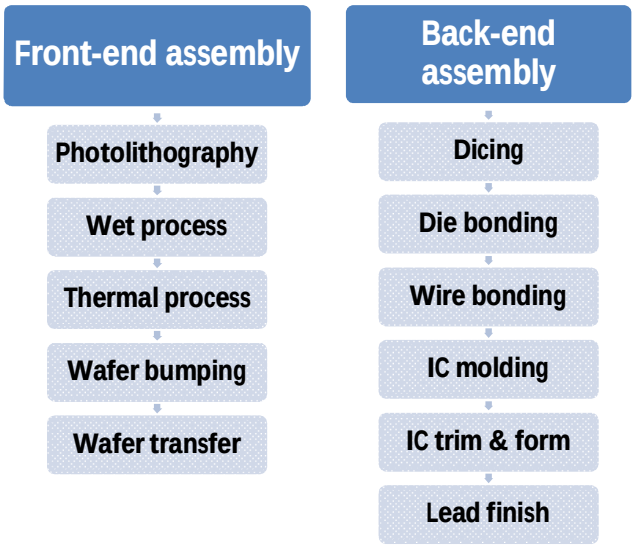


Figure 2: Process steps in IC packaging fabrication

Generally in the front-end assembly, the processes involved are to fabricate the wafer by formation of transistors directly onto the silicon wafer whereas back-end assembly refers to the technology of mounting and interconnecting of devices into the final products.

2.2.1 Front-end assembly

In photolithography process, photo resist film is coated on the surface of a wafer and the circuit patterns are formed on the wafer surface, exposing light through a photo-mask. Later, the wafer surface is developed to remove the photo-resist layer of exposed pattern.

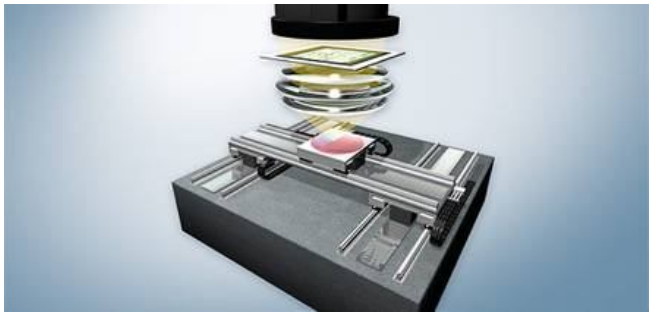


Figure 3: Photolithography process [Omron Corporation, 2008]

In wet process, such as single wafer cleaning, butch cleaning and post CMP cleaning, wafers are cleaned with water or chemicals to remove light contamination, particles and dust. Efficient medium consumption and high throughput is required in wet processes. Later in thermal process, wafers are baked in quartz furnaces to make thin film or to dope the surface. For high thermal-process quality, accurate and fast temperature control is very essential. Further process is wafer-level bumping, a process that creates interconnections between chip and substrate. It is important to ensure the consistency of bump composition as well as height uniformity across the whole wafer.

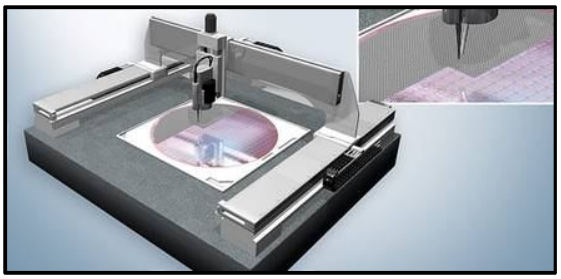


Figure 4: Wafer bumping process [Omron Corporation, 2008]

The final process in front-end assembly stage is wafer transfer. In this process, wafers are transferred to a loadport. EFEMs (Environmental Front End Module) align and transfer wafers from loadports to the wafer station at the various process equipment. At the wafer alignment stage, the orient notch and deviation of the wafer have to be aligned to transfer wafers at the correct position.

2.2.2 Back-end assembly

In back-end assembly, dicing process is performed priory by polishing the undersurface of the wafer. Then it is diced into individual chips by cutting a checkerboard pattern.

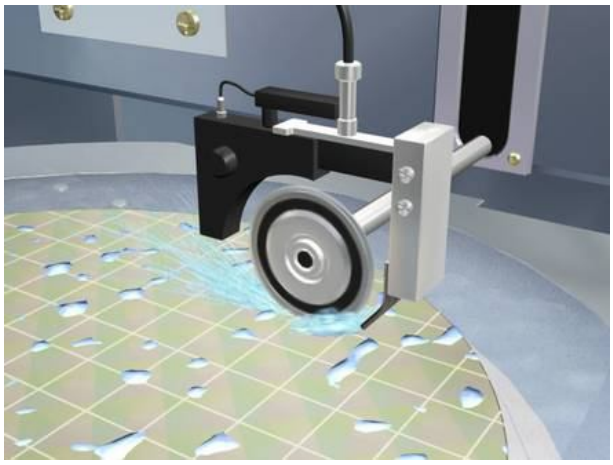


Figure 5: Dicing process [Omron Corporation, 2008]

Diced chips are then connected to lead frames at a die-bonding machine in the die bonding process. Various chips are assembles accurately and quickly in this process and the key in this process is the high productivity and throughput of the machines. The frames and chips are then connected with extremely fine gold wire at a wire bonding machines. For high-quality bonding, it is necessary to ensure the correct position of the die and the transported lead frame. Later, the bonded chip on the lead frame is encased in a synthetic resin or ceramic package in the molding process. Each mold is managed with a unique ID. The molds are heated up to melt the resin. Then, the lead frame is trimmed off and formed into the shape required to mount the IC on a circuit board.

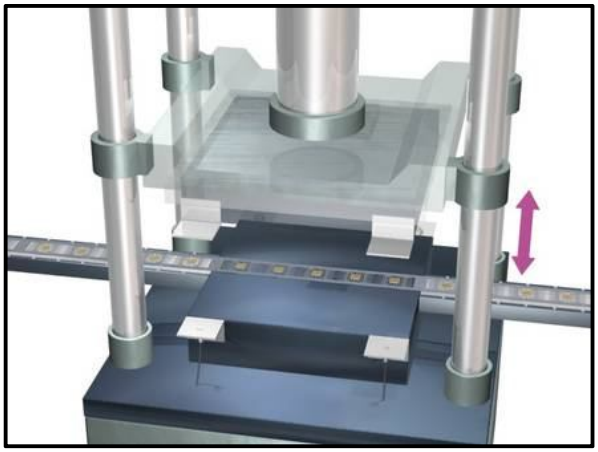


Figure 6: IC molding process [Omron Corporation, 2008]

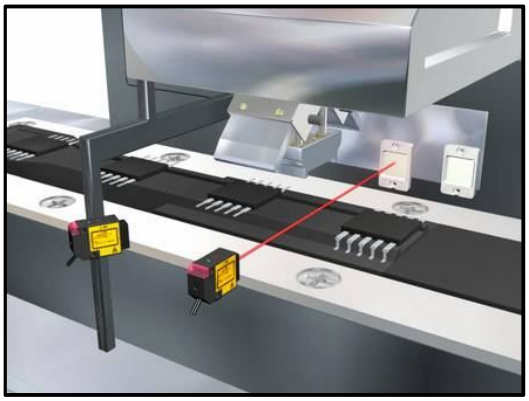


Figure 7: IC trim and from process [Omron Corporation, 2008]

Lead finish is the final process in IC semiconductor fabrication. It is a process of applying a coat metal over the leads of an IC to protect the leads against corrosion and abrasion, to improve the solderability of the leads and to improve the appearance of the leads. This process will be discussed in detail later and it becomes significant to the author since it is the focus area of study in this project.

2.3 SOT-23-3L EIAJ

Semiconductor industry manufactures a very wide variety of IC packages that have different requirement. Package features that are taken into consideration when choosing package type for certain semiconductor application include size, lead count, power dissipation, field operation conditions and cost [Siliconfareast.com, 2008]. In semiconductor industry nowadays, the popular IC packages used are indicated in the following figure.

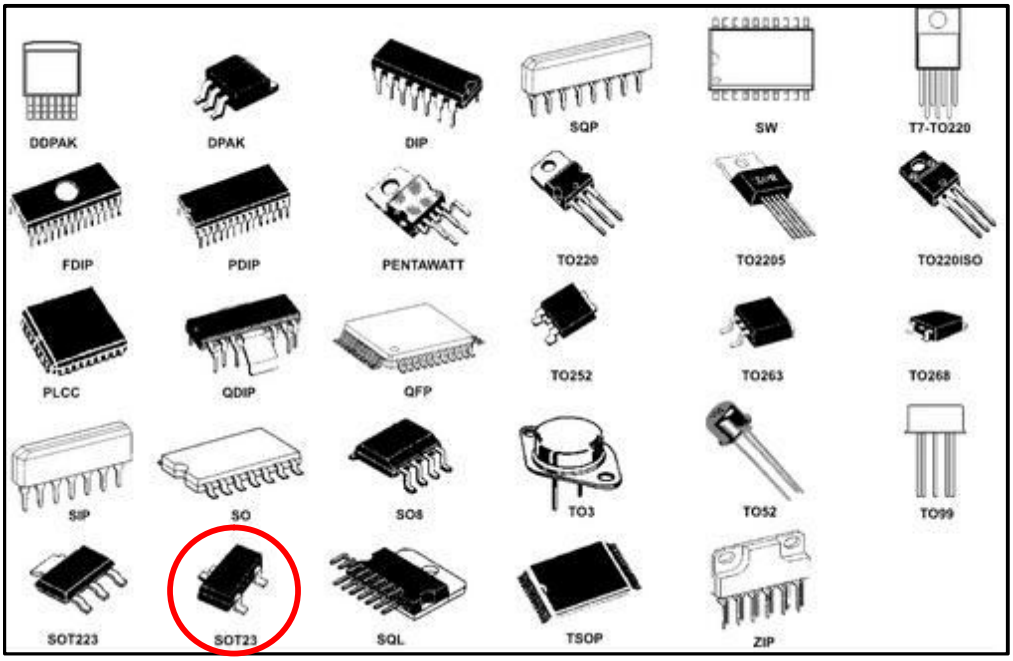


Figure 8: Types of IC packages [Jestine Yong, 2009]

SOT-23-3L EIAJ matrix is one of the IC packaging types which underlying below surface mounted transistor package with three leads. The base material of lead is made up of pure copper (Cu) and electroplated by tin (Sn) material. EIAJ stands for Electronic Industry Association of Japan, an organization for electronics industry standardization, specifically semiconductor integrated circuit. SOT-23-3L EIAJ has been chosen because it is the most critical product in IDS Electronics that frequently having problem during its plating process. Figure of SOT-23-3L EIAJ IC packaging and its specification are shown below.

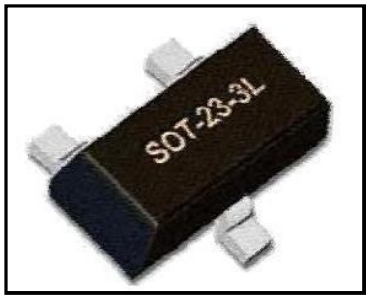


Figure 9: SOT-23-3L IC packaging from IDS Electronics

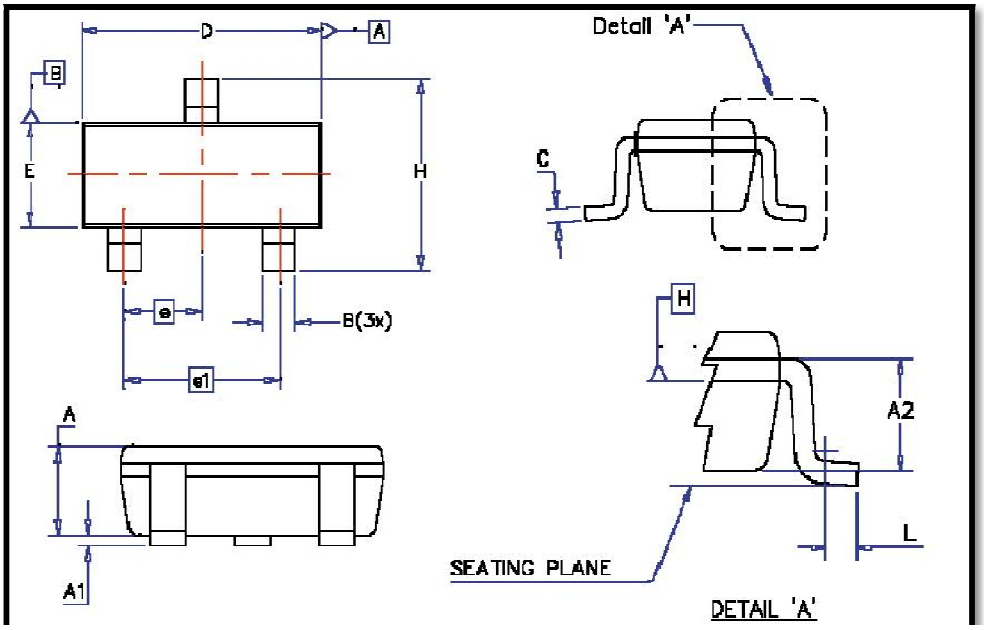


Figure 10: Specification of SOT-23-3L IC packaging from IDS Electronics

Table 1: Specification of SOT-23-3L IC packaging from IDS Electronics

VARIATIONS								
SYMBOL	MILLIMETERS				INCHES			NOTES
	MINIMUM	NOMINAL	MAXIMUM		MINIMUM	NOMINAL	MAXIMUM	
A	0.90	-	1.30		.035	-	.051	
A1	0	-	0.10		0	-	.004	
A2		0.80 REF				.031 REF		
B	0.30	-	0.50		.012	-	.019	4
C	0.10	-	0.35		.004	-	.014	4
D	2.70	-	3.10		.106	-	.122	1,2
E	1.40	-	1.80		.055	-	.071	1,2
H	2.50	-	3.00		.098	-	.118	
e		0.95 BSC				.037 BSC		
e1	1.70	-	2.10		.066	-	.083	
L		MIN 0.2				MIN .008		

2.4 Electroplating Process

A lead frame is a thin layer of metal that connects the wiring from electrical terminals on the semiconductor surface to the larger circuit on circuit boards. It undergoes several stages of plating process to avoid from corrosion and abrasion to the surface. The process used in this plating stage is called electroplating. Electroplating is a process of depositing a coating metal on a surface by passing a current through an electrolyte. The mechanism of this process is illustrated as below.

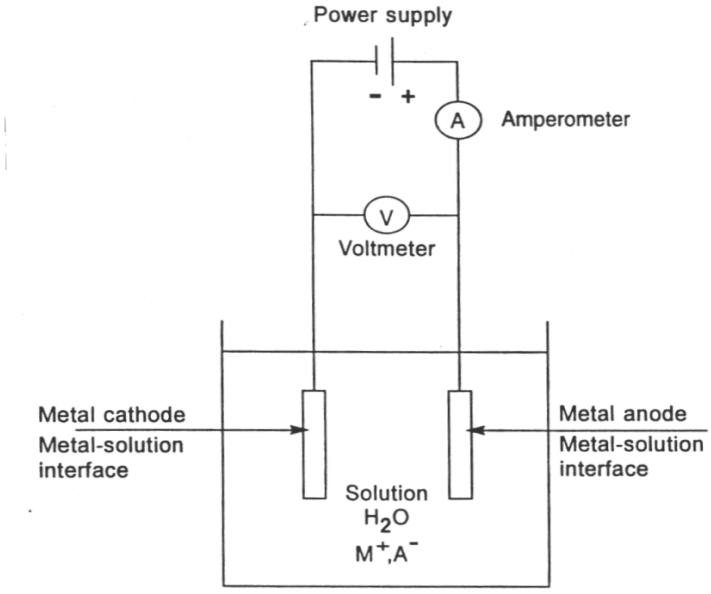


Figure 11: Schematic diagram of an electroplating process [Mordechay Schlesinger, 2002]

An electroplating system has four components: 1) the cathode, which is the surface to be coated; 2) the anode, which is the source of coating metal; 3) the electrolyte, the aqueous medium through which the metal ions from the anode transfer to the cathode; and 4) the power source, which supplies the current needed for the plating process [4].

The electrical current supplied may be varied by controlling the current density in order to achieve a better quality plating thickness. Current density strongly influences the deposition rate of the electroplating, plating adherence and plating

quality. In fact, these factors can also vary over the surface of a part due to geometry design. For example, the outside surface will experience higher current density compared to the inside surface. Theoretically, the higher current density the higher deposition rate will be.

In electroplating of IC lead frames, it will be clear from the foregoing that in its simplest form an electroplating plant consists of degreasing, etching and rinsing tanks, separate plating tanks for each metal to plated, each with appropriate and adequate supply of continuous electric current. The articles to be plated are fastened to wires or suspension jigs, and these are then lifted intro and out of the appropriate tanks in sequence, the times and currents being adjusted at the judgment of the operator. Many electroplating plant are indeed operated in this way. For larger scale operation it is now, however, much more common to mechanize the whole process to a greater or lesser extent. The various tanks are arranged in line a common width and depth, but with length in proportion to the relative time the articles will spend in them. Overhead mechanisms lift the work from tank to tank, and driving chains progress it laterally through the plant.

It will ensure that each article receives the predetermined treatment without human judgment. Temperatures, current, pH values, etc. are automatically controlled and centrally indicated. Such machines are costly to install and maintain, and are uneconomic unless they can be kept fully loaded, but they have high capacity and above all they produce consistent result with a small labor force. This small force is used to supervise, control and inspect the operations and to maintain quality.

Electroplating Substrates

Since copper is the base material of IC lead frame, it is necessary to coat the frame with the higher resistivity material such as nickel, tin or silver to prevent from corrosion and abrasion on the surface. These metal materials are then being electrolytes also known in the industry as baths in the electroplating process. In this case, tin has been used for coating as its properties of solderability and high corrosion resistance. The electrolytes primary constituent is the metal salt of the

metal to be deposited, then in most cases an acid or alkali to promote conduction. In addition, there will be additives to promote the electroplating process or optimize the deposit [Nasser Kanani, 2004].

Table 2 below shows an example of set of bath operating parameters plating substrate used in pure tin plating process as a lead free finish for IC packaging.

Table 2: Bath operating parameters for a pure tin plating process of IC packaging [Joseph Gauci, 2002]

Parameter	**Range**	**Optimum**
Tin(II)	40 – 60 g/l	50 g/l
Total Acid	200 – 300 ml/l	250 ml/l
Temperature	40 – 50 °C	45°C
Additive	50 -110 ml/l	80 ml/l
Antioxidant	5 – 20ml/l	10ml/l
Cathode Current Density	5 – 25 A/dm²	15 A/dm²
Agitation	Vigorous solution coupled with cathode movement	
Anode Current Density	0.1 – 5.0 A/dm²	
Anodes	Tin slabs in titanium baskets	
Deposition Rate	ca. 7.5 microns/minute under optimum conditions	

In this process, the lead frame is plated with the pure tin as their electrolytes primary constituent and acid act as agent to promote conduction. The optimum temperature used in this process is 45°C which is important parameter in determining deposition rate and bath stability. Increase in temperature will result in higher electrolytic conductivity, and because all reaction rates are accelerated, will increase the rate of additives consumption in solutions as well.

In addition to metal salts, electrolytes usually contain various other species like additives for the specific purposes, for example, to increase bath stability, or improve metal distribution, or to optimize the chemical, physical or technological properties of the deposited metal (corrosion resistance, brightness or reflectivity, hardness,

mechanical strength, ductility, internal stress, wear resistance or solderability) [Nasser Kanani, 2004].

Electrolyte and its properties become vital in fabricating dense, uniform and adherent metal plating. Some of the parameters are discussed below.

- **Electrolytic Conductance**

  The conductivity of an electrolyte is a function of the degree of dissociation, the mobility of the individual ions, the temperature (and thus viscosity) and the electrolyte composition. While in principle, the electrolytic conductivity of a solution has no effect on the properties of the deposited metal, in cases where it is too low, certain adverse effects will appear [Nasser Kanani, 2004]. These include:

a) Primary current distribution deteriorates, with the result that disproportionately heavy deposition occurs at leading edges and corners of the work. Generally, the outcome is less uniform metal distribution.
b) Because the resistance is higher, more heat will be generated by the passage of the same current through the electrolyte, the result being increased electrical energy required, and perhaps more cooling of the solution being necessary.

- **Covering Power**

  'Covering power' is a term used to describe to which an electrolyte can cover the entire surface of an object being plated, with reasonably uniform thickness. An electrolyte is said to have good covering power when satisfactory metal deposition extends into the lowest current density range. Covering power usually increases with increasing current density and decreases with increasing temperature [Nasse Kanani, 2004].

- **Macro-throwing Power**

  The term ‘macro-throwing power’ is used to describe the ability of an electrolyte to lie down as nearly as possible, a uniformly thick deposit across the surface of an object. The more this is so, the better the throwing power, and thus it can be used as a predictor for the uniformity of a deposit. It will be clear that good covering power is a pre-requisite for good macro-throwing power [Nasser Kanani, 2004].

- **Micro-throwing Power**

  Micro-throwing power is important for perfectly smooth electroplated surface. This is the extent to which metal electroplating occurs at the base of valleys or cracks. In principle, electroplating at these sites is hindered, but in access of fresh electrolyte and dispersal of exhausted electrolyte is hindered [Nasser Kanani, 2004]. In many cases, it is found that micro-throwing power is inversely related to macro-throwing power. When the one is good, the other is not, and vice versa.

2.5 Uniform Plating Thickness Distribution

One of the techniques on how to maintain the plating thickness distribution based on cell geometry factor is by creating an even current density. The thickness of the local deposit varies with the local time-current product so, as Figure 12 shows, the thickness of plating can only be constant if the cell geometry creates an even current density. [Martin Tarr, 2001]

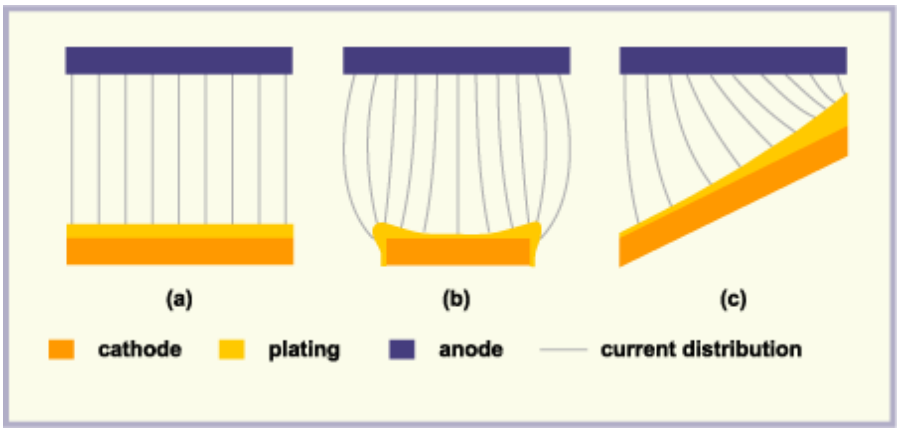


Figure 12: Examples of primary current distribution for three different cathodes [Martin Tarr, 2001]

When plating onto a flat laminate, a sufficiently parallel field can usually be obtained, but plating piece-parts or three-dimensional boards can present more of a challenge. Four general ways of improving the evenness of plating are described below:

- using a 'current screen' of non-conducting material to force the field into specific areas
- placing one or more 'current thieves', electrically connected to the cathode but separate from it, to 'steal' some of the surplus current from regions of high current density
- using a 'bipolar anode', which is a piece of metal (usually of the same material as the main anode) placed in the field between anode and cathode, but connected to neither – being a much better conductor than the electrolyte, the bipolar anode will dissolve at the end closest to the cathode, and metal will be deposited on the other end
- using one or more extra anodes, placed in appropriate positions near the cathode surface.

All these methods need physical modifications to the plating bath. However, for the more usual PCB situation of a flat substrate, a very simple set-up will provide uniform plating, given attention to agitation. However, this uniformity only applies on a macro scale, and there are a number of causes of small-scale variation,

particularly relating to plating down through-holes and vias. Some of these are design-related, and others can be tackled using plating bath additives.

2.6 Metallographic Technique

The purpose of metallographic technique is to perform further processes which are plating thickness measurement and microstructure examination of plated lead frame. The reason is the technique will ease in handling the very tiny sample part to be measured and examined. The surface of metallographic specimen is prepared by various methods of sectioning, mounting, fine grinding, rough polishing and final polishing.

- **Sectioning**

  Sectioning is the initial stage of sample preparation in metallographic by removing a representative area from the parent piece. It can be performed in two different techniques which are precision or abrasive depends on the parts properties. The cut plane should be as near as the desired area and normally the final size of sectioned part is 2 inches or less in diameter.

- **Mounting**

  Mounting is a process of embedding the small pieces of sample in a plastic medium for ease in manipulation and other factors such as:

a) Protect edges during polishing
b) Protect delicate sample
c) Increase life of polishing surface
d) Uniformity that allows for automation
e) Safety

This can be done by two methods, cold or hot mounting. Usually cold mounting is the preferable since it is faster compared to hot mounting besides using no special equipment. A mounted specimen usually has a thickness of about half its diameter, to prevent rocking during grinding and polishing. The edges of the mounted specimen should also be rounded to minimize the damage to grinding and polishing discs. The appropriate samples should be as the following figure.

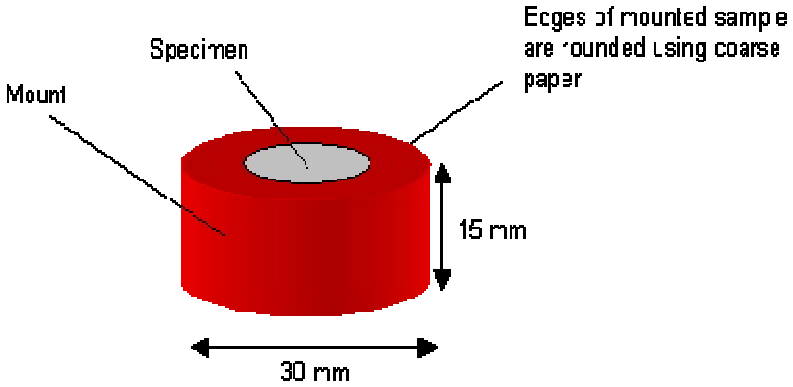


Figure 13: A mounted specimen (shows typical dimensions) [DoITPoMS, University of Cambridge]

- **Fine Grinding**

Fine grinding is a process of removing the damage resulting from sectioning and coarse grinding. Depths limitation can be acquired by proper abrasive size sequencing during this process. Normally the abrasives used in fine grinding are Silicon Carbide, Emery and Aluminum Oxide. Silicone Carbide and Aluminum Oxide materials are available with either a non water proof paper for dry operation or water proof cloth for wet or dry operation. Preference is for wet operation which offers a flushing action to prevent the surface from becoming clogged with removal products. [Cornelius A. Johnson, LECO Corporation].

- **Rough Polishing**

  The significance of rough polishing is a further limitation of the deformation zone produced by fine grinding. This stage may be considered the most important in the entire preparation sequence [Cornelius A. Johnson, LECO Corporation]. Polishing involves the use of abrasives, suspended in a water solution, on a cloth-covered electrically powered wheel. Diamond abrasives provide the best, and most expensive, compounds utilized in polishing; standard sized aluminum oxide powders are applied for general use purposes. Diamond particles retain their shape and size during abrasion and produce a uniform and high rate of material removal with minimal induced surface damage.

- **Final Polishing**

  The final polishing stage serves to remove any deformation zone resulting from rough polishing. A uniformly polished and scratched-free surface must be produced. Any zone produced at this stage should be minimal and generally will be removed during etching [Cornelius A. Johnson, LECO Corporation]. The final polishing stage will be employing polishing suspension such as diamond paste or aluminum oxide particles (most extensively used material) carried out on the polishing cloth. A wide variety of abrasive materials are used for final polishing. The most common are aluminum oxide, chrome oxide, magnesium oxide, silicon dioxide and diamond.

CHAPTER 3

METHODOLOGY

3.1 Project Flow

In completing this project, a number of tasks and methodology have been allocated for the whole two semesters. The project flow is illustrated as the following.

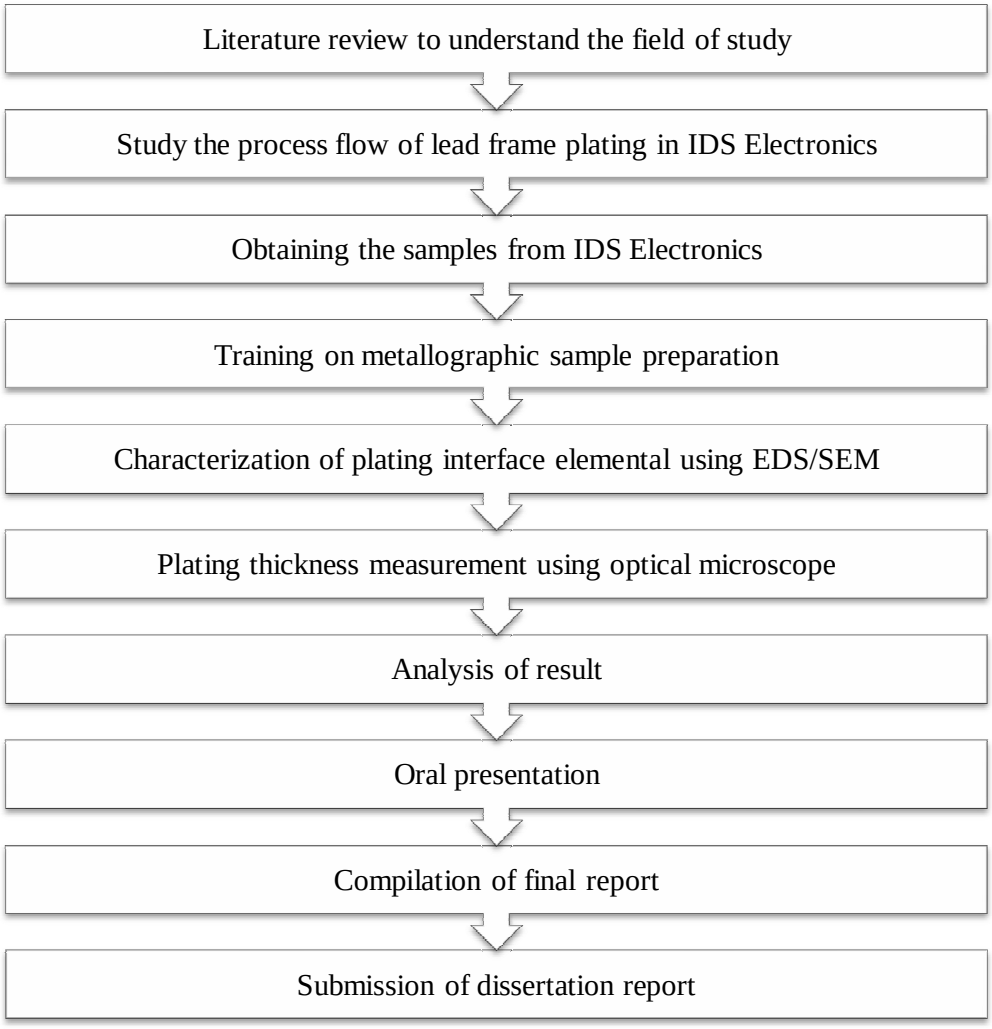


Figure 14: Project flow within two semester studies

The first four steps which are focusing on the theory and literature reviewing and training on metallographic sample preparation have been performed in the first

semester studies while, the remaining steps have been completed during second semester studies by performing plating thickness measurement and result analyses as well as report preparation.

In the first stage, research has been done on the study since this is a real life problem in industry field. In completing this project, research on the IC semiconductor packaging, lead frame electroplating process and metallographic technique have been studied. In fact, studying the process flow of lead frame plating in IDS Electronics had much help for further understanding of the process. The author has visited the company for purpose of obtaining samples and information as well as comprehensive understanding of the issue.

Once the samples obtained, the immediate progression is the training on metallographic sample preparation by using dummy part. The purpose of this training is to ensure that samples can be properly prepared with:

- Flat, free from scratches, stains and other imperfections which tends to damage the surface,
- Section contain all non-metallic inclusions intact,
- No chipping or galling of hard and brittle intermetallic compounds and
- Section must be free from all traces of disturbed metal.

The prepared samples then further used for another two stages which are characterization of plating interface microstructure and plating thickness measurement. These two steps however can be performed using scanning electron microscope or SEM and optical microscope respectively. Finally, all the data and statistics gathered from previous steps have been analyzed and compiled into a document so-called dissertation report.

3.2 Gantt Chart

Project flow in the previous section must be accomplished within the timeline given. In order to ensure this project is successfully completed at the end of this study, a Gantt Chart as Figure 15 has been constructed.

Figure 15: Gantt Chart

3.3 Project Activities

- **Sample Sectioning and Mounting**

In the week twelve, 2009, a sample of dummy lead frame tin-plated for SOT-23-3L package has been obtained form IDS Electronics. This sample is being used for the purpose of metallographic sample preparation training which complies with the project milestone for this semester. The rationale of metallographic

training is to ensure the writer is skilled enough to prepare a number of samples for thickness measurement and microstructure characterization in second semester. Figure 14 below shows the dummy part provided by IDS Electronics.

(a) (b)

Figure 16: (a) A piece of dummy lead frame for SOT-23-3L package (b) A unit of IC is cut from its frame for mounting purpose

Before mounting process, the IC is cut by unit using scissors since copper material is very soft and it is not need precise or abrasive cutter. Then mounting process is performed using Epo-Kwick Epoxy Kit by Buehler provided by university. The steps involved in mounting are as follows:

1) Five (5) parts Epo-Kwick Resin to one (1) part Epo-Kwick Hardener are mixed by weight using a scale.
2) Samples are thoroughly clean and dried before the encapsulation.
3) Sampl-Kup is coated from the inside with Release Agent to ensure easy removal of the mount from the mold.
4) The specimen is placed inside the center of Sampl-Kup with the surface of interest facing down.
5) The mixture is blended thoroughly for approximately 1-1½ minutes until cloudy mixture become clear. Violent stirring must be avoided to prevent air bubbles formation.
6) Once the mixture is clear, it is poured into the Sampl-Kup to near capacity for about ¾ full.
7) The mold is allowed to cure at room temperature for approximately 90 minutes.
8) After curing, the mount is removed from the mounting cup.

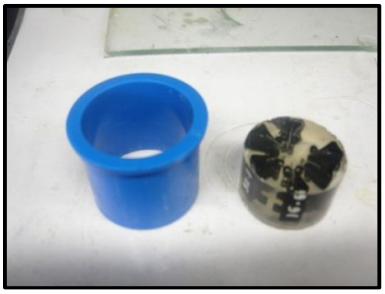
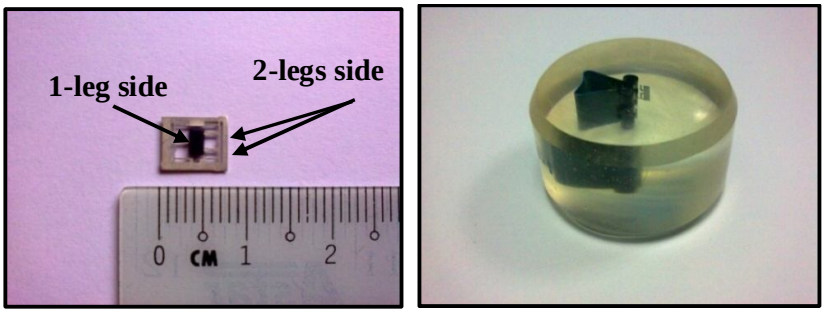


Figure 17: Mounted specimen using Epo-Kwick Epoxy Kit

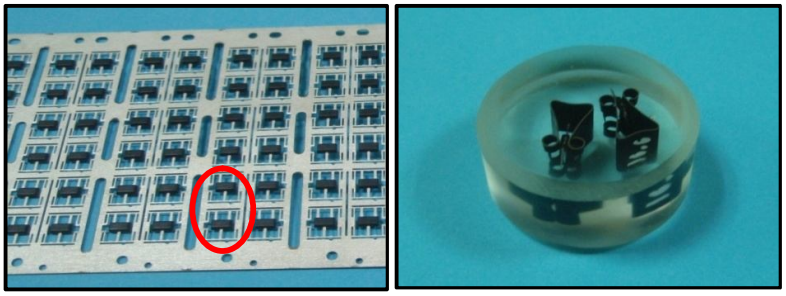
Figure 16 next showing a unit of IC has been cut and mounted using cold mounting. In the picture (b), it can be seen that a paper clip inside the mounting together with IC unit. The reason is paper clip used to hold the sample so that it stands vertically and the 2-leads side will be facing the horizontal plane as the surface of interest.



(a) (b)

Figure 18: (a) A unit of IC cut from its lead frame (b) The mounted IC inside epoxy which the 2-legs side as the surface of interest

In the first week of 2010, a meeting with IDS Electronics was held again in order to obtain the actual sample of IC packages. These samples have been tested and recorded the relevant data. The testing method applied is similar to how the dummy samples have been experimented in the previous semester. The only difference is two IC packages have been mounted together inside a mounting in order to save the material as long as time for metallographic process. The plating thickness is measured optically on three leads adjacent to the package. Therefore, two pieces of ICs have been mounted with 2-leads and 1-lead sides respectively as the surfaces of interest.



(a) (b)

Figure 19: (a) Two adjacent ICs assumed to be plated evenly (b) Two adjacent ICs mounted with 2-leads and 1-lead sides respectively as the surfaces of interest

In order to investigate the consistency of plating thickness over a lead frame IC package, 6 critical spots (4 corners and midsection of the lead frames) have been designated to be tested. Figure 19 below shows the most important areas to study their uniformity thickness as well as plating microstructure. These six spots have been coordinated respectively according to the total number of IC comprises in a piece of lead frame SOT-23-3L package (6 rows and 32 columns). The rows are designated alphabetically with A, B, C, D, E, and F while the columns are denoted numerically from 1 to 32. The detail locations of IC on lead frame are as the following table and figure.

Table 3: Locations and respective row and column of six critical spots adjacent ICs.

Spot	**1**	**2**	**3**	**4**	**5**	**6**
Column	1	16	32	1	16	32
Row	A	F	A	F	A	F
Location	[1,A]	[16,F]	[32,A]	[1,F]	[16,A]	[32,F]

Figure 20: The rows are designated alphabetically with A, B, C, D, E, and F while the columns are denoted numerically from 1 to 32.

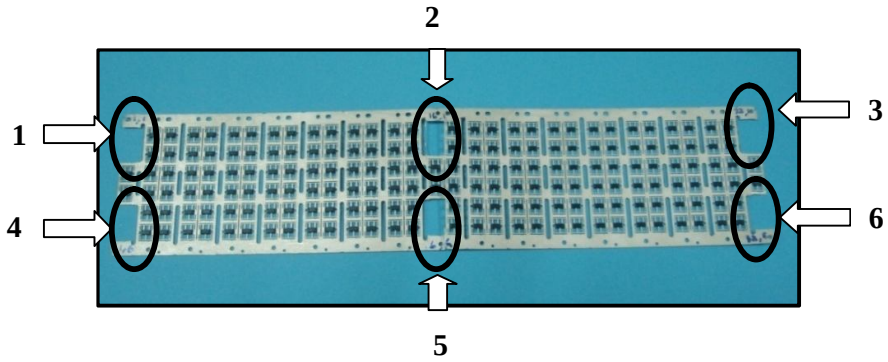


Figure 21: Six spots of IC location on a piece of IC lead frame for SOT-23-3L package.

- **Grinding and Polishing**

After sample has been mounted inside the epoxy, the mount is then ground and polished. Initially, coarse grinding is performed to remove deformation produced during cutting and to provide the initial flat surface for microsample preparation. The process is performed on silicon carbide abrasive disc covered rotating wheels. The size range has been used are 60,180 and 240 grit. Water is used as a coolant to prevent overheating of the specimen and flush away the surface removal products, thus keeping sharp abrasive grain exposed at all times. Figure 15 shows the METASERV 2000 grinder used with the various abrasive papers as in Figure 16.

Figure 22: METASERV 2000 Grinder

Figure 23: Abrasive grinding papers

The next step is to perform fine grinding to remove the zone produced by coarse grinding. Grit sizes that have been used in the process are from 320 and 600 SiC. This will result a shallower deformation depth and thus smoother sample surface.

Further, the most important stage in the entire preparation sequence is the polishing process. In the process, there are two diamond-abrasive sizes have been used, 6 and 3 micron respectively. Diamond particles retain their shape and size during abrasion and produce a uniform and high rate of material removal with minimal induced surface damage. The paste-like diamond abrasive material facilitates convenient charging of the polishing cloth surface and the addition of an extender contributes to even particle distribution over same. The type of cloth used for this stage has an extremely important bearing on the end result. Napless

cloth such as chemotextile materials has been used to hold relief and undercutting at interfaces to a minimum. Figure 17 shows the IMPTECH 302 DVT polishing machine used to polish the sample to a free-scratch surface to be examined under optical microscope in the later stage.

Figure 24: IMPTECH 302 DVT Polishing Machine

During grinding and polishing process, several techniques and tips have been applied to ensure equal material removal over the entire surface. These techniques are implied especially with the manual processing.

a) With manual processing, the sample must be firmly held with the fingers.
b) Finger and wrist joints should remain rigid and shoulder line fixed to aid in even pressure control and produces a planar surface with no faceting.
c) The specimen is rotated 90º between abrasive steps. The purposes are to indicate when the abrasive scratches from the previous step have been removed and to prevent faceting.
d) Since the rotation of the polishing wheel is in counter clock-wise direction, the sample should be moved in a clock-wise direction around the entire polishing surface as in Figure 9. The reason is to avoid: (1) Directional traces, (2) 'Fishtailing' of certain family type inclusions, (3) 'Pull-out' of faces poorly consolidated within a microstructure.

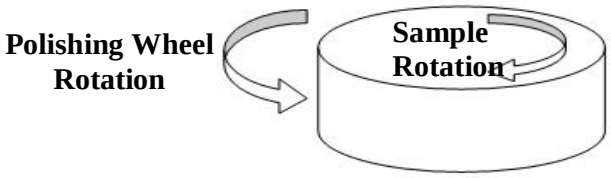


Figure 25: Rotation of polishing wheel and sample rotation.

- **Cleaning**

Cleanliness is one of the most important requisites in sample preparation. Samples have been carefully cleaned between each stage of preparation to prevent contamination by coarser abrasives being carried over to a finer abrasive stage. After rinsing under tap water, the sample is flooded with ethanol and dried in a stream of warm dry air. The specimen must be dried quickly to prevent staining or corrosion.

- **Microscopy**

Microscopy is the technical field of using microscopes to view samples or objects. It is used for viewing polished metal surfaces under high power magnification with a flat and cleaned surface. After the sample preparation have been done, the plating thickness are then measured under optical microscope by employing DinoCapture Software embedded to it. Optical microscope has been used extensively throughout the study from initial inspection to various stages in the analysis.The main objective of microscopy in this study is to measure the thickness of tin plating over the copper material. By using optical microscope, thickness measurement can be performed by using levels of magnification of 100X and 500X.

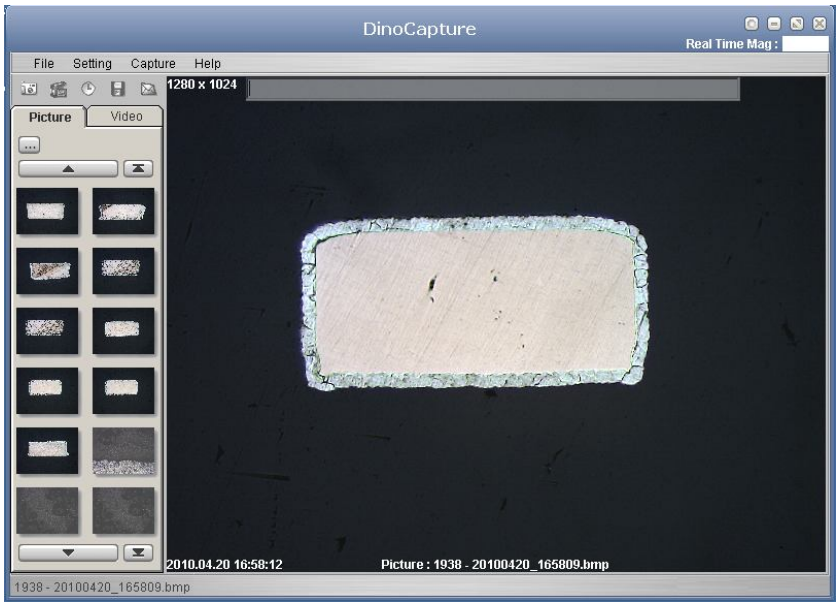


Figure 26: DinoCapture Software embedded to the optical microscope

- **Tools and Equipment Required**

In completing this study, a range of tools and equipment will be used for the optimum result such as:

1) Metallographic sample preparation
    - Scissors for part sectioning since lead frame material is too soft
    - Paper clips to hold the sample in the mounting
    - Epoxy Systems Epo-Kwick Kit for cold mounting process
    - Grinder and polisher for grinding and polishing process
    - Abrasive grinding paper
    - Diamond paste and Aluminum Oxide polishing paste
    - Ethanol for sample drying purposes

Figure 27: Epo-Kwick Epoxy Kit

2) Microscopy examination
    - Optical microscope for thickness measurement
3) Microstructure characterization composition examination
    - EDS/SEM to see and verified the material viewed under optical microscope whether they are pure copper (base material), or pure tin (plating material) or copper-tin intermetallic composition.

Figure 28: Scanning Electron Microscopy machine [Susan Swapp, University of Wyoming]

EDS/SEM also known as EDX or Energy Dispersive X-ray is used to identify the elemental composition of small areas of interest on the sample. During EDS, a sample is exposed to an electron beam inside a scanning electron microscope. These electrons collide with the electrons within the sample, causing some of them to be

knocked out of their orbits. The vacated positions are filled by higher energy electrons which emit X-rays in the process. By analyzing the emitted x-rays, the elemental composition of the sample can be determined. EDS is a powerful tool for microanalysis of elemental constituents.

CHAPTER 4

RESULT AND DISCUSSION

4.1 Result

For each IC lead frame, there are six spots (four corners and midsection of the frames) of plating thickness to be measured. Each spot indicates a unit of IC package with three legs. Plating thickness of IC lead frame is determined by measuring each side of three cross-section legs. The illustration of IC locations on the lead frame and leads position are shown below.

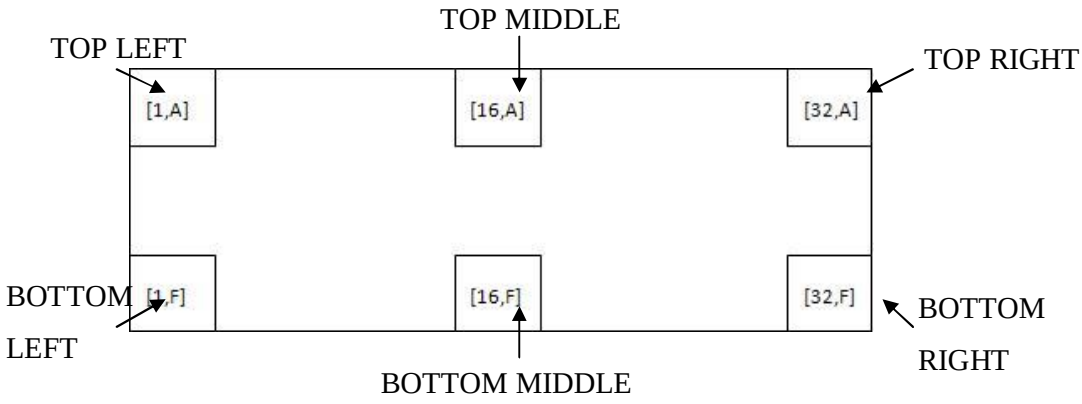


Figure 29: Six spots of IC locations on a lead frame

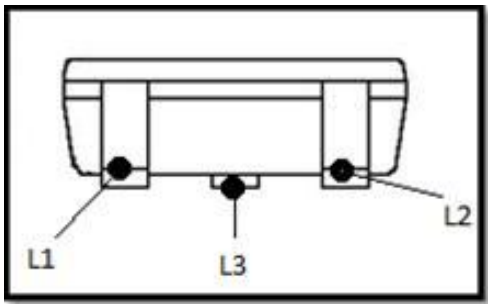


Figure 30: Three IC leads positions

- **Plating Thickness**

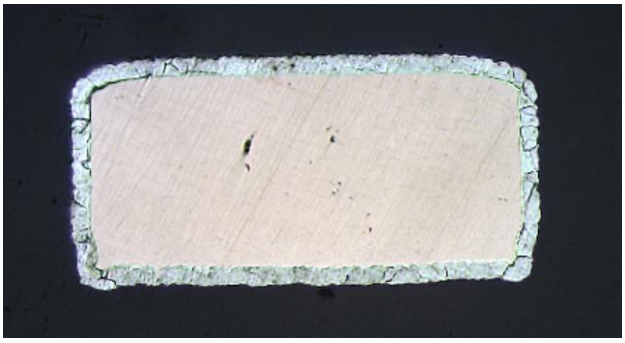


Figure 31: A well distributed plating thickness of an IC lead at 500X magnification

Table 4: Tin plating thickness in over five samples of lead frame

Location \ Sample	Plating thickness in microns (µm)					
	#1	#2	#3	#4	#5	Mean,µ
TOP-LEFT	12.5	14	23.13	16.5	18.33	
TOP-MID	13.25	12	12.8	12.67	12	
TOP-RIGHT	13.33	14.33	15.2	17	18	
BOT-LEFT	13.5	13	20	23.33	16.67	
BOT-MID	14.5	12.5	11.5	10.5	11.5	
BOT-RIGHT	14	14	15.75	16.5	17	
Mean,µ	13.513	13.305	16.397	16.083	15.583	14.976
Sigma,δ	0.625	0.862	4.023	4.011	2.771	2.458

Data obtained from :

Number of lead frames = 5
Number of IC per lead frame = 6
Number of leads per IC = 3
Spots measured on each lead = 8
Total number of data = 720

Table 4 shows the tin plating thickness has been measured over five sets of lead frame samples on the six critical spots. From the table, the mean thickness over these sets is 14.976 µm and its standard deviation of 2.458. However samples three, four and five show a quite large number of thickness compared to others especially on the TOP-LEFT and BOTTOM-LEFT spots. Plus they are also a bit off from the

thickness specification of 7-20 µm [Joseph Gauci, 2002] which are 23.13 µm and 23.33 µm.

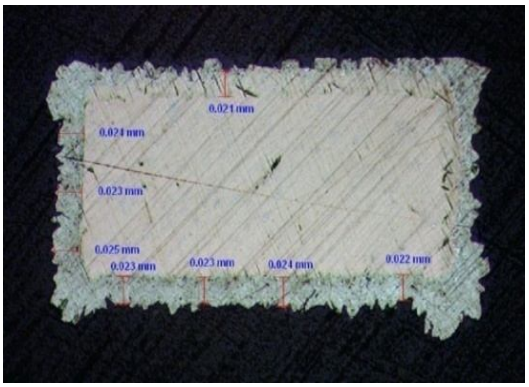


Figure 32: Sample three at TOP-LEFT location with 500X magnification

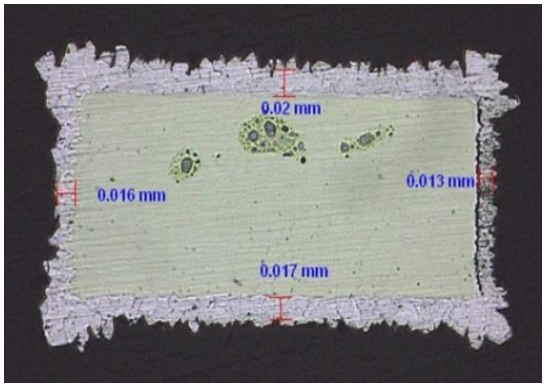


Figure 33: Sample four at TOP-LEFT location with 500X magnification

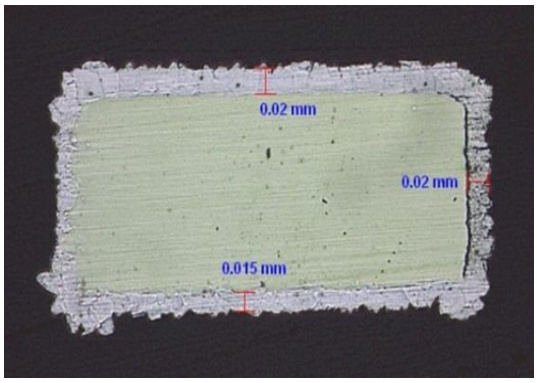


Figure 34: Sample five at TOP-LEFT location with 500X magnification

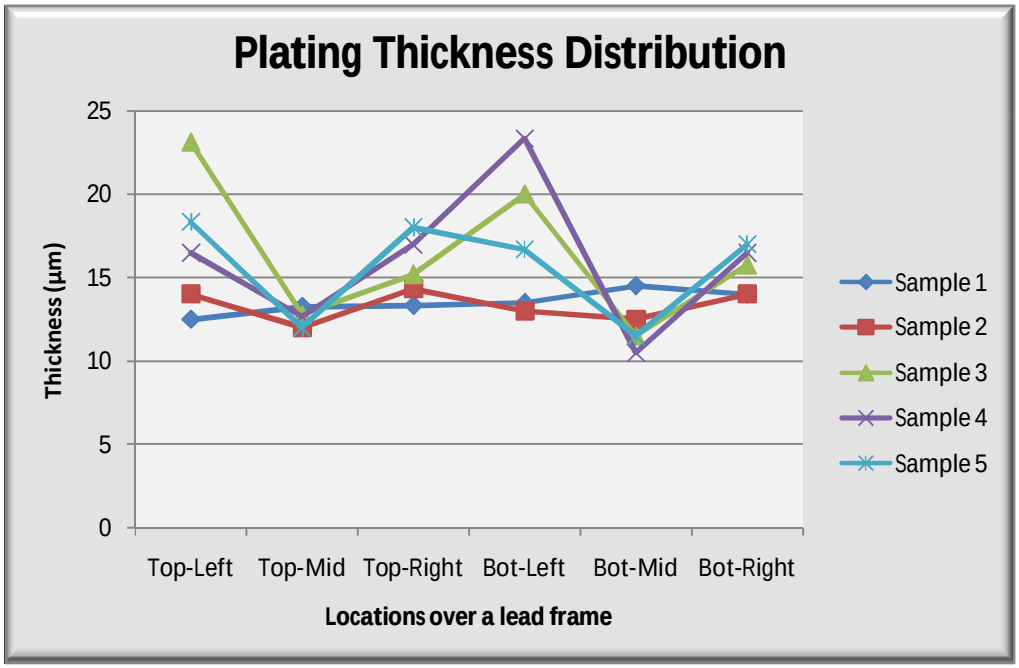


Figure 35: Plating thickness distribution over five sets of lead frame

Graph depicts the plating thickness distribution over a lead-frame in the second level degradation of solution for five samples. The first and second samples show almost uniform distribution as can be seen in Figure 36 with standard deviation < 1.00 while the rests show non uniform plating thickness with standard deviation > 4.00.

There are large variations at the top-left and bottom-left locations where the thickness is higher compared to others but still within the thickness specification range of 7-20 µm. except, only sample three and four are outside the range as in the Figure 37.

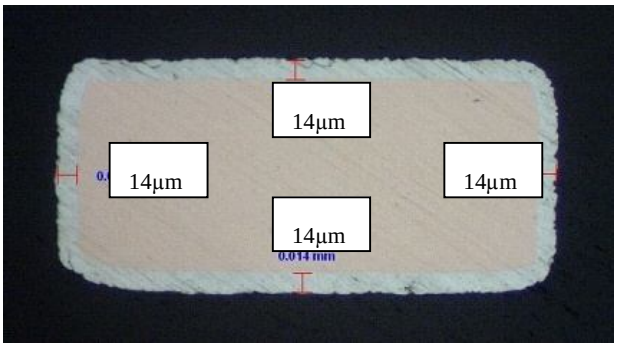


Figure 36: Lead cross section shows plating thickness

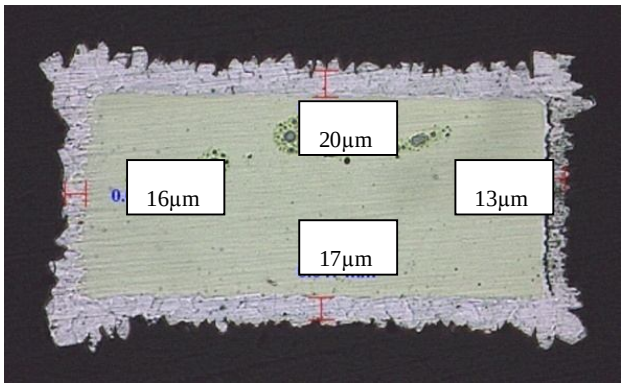


Figure 37: Inferior appearance and non uniform plating thickness

- **Elemental Composition**

The EDS analysis has been performed onto the samples at three spots; base material (Cu), plating material (Sn) and Intermetallic of Cu/Sn. The purpose of this analysis is to determine the elemental composition of these two materials on the sample. Result of EDS analysis can be referred in the following figures.

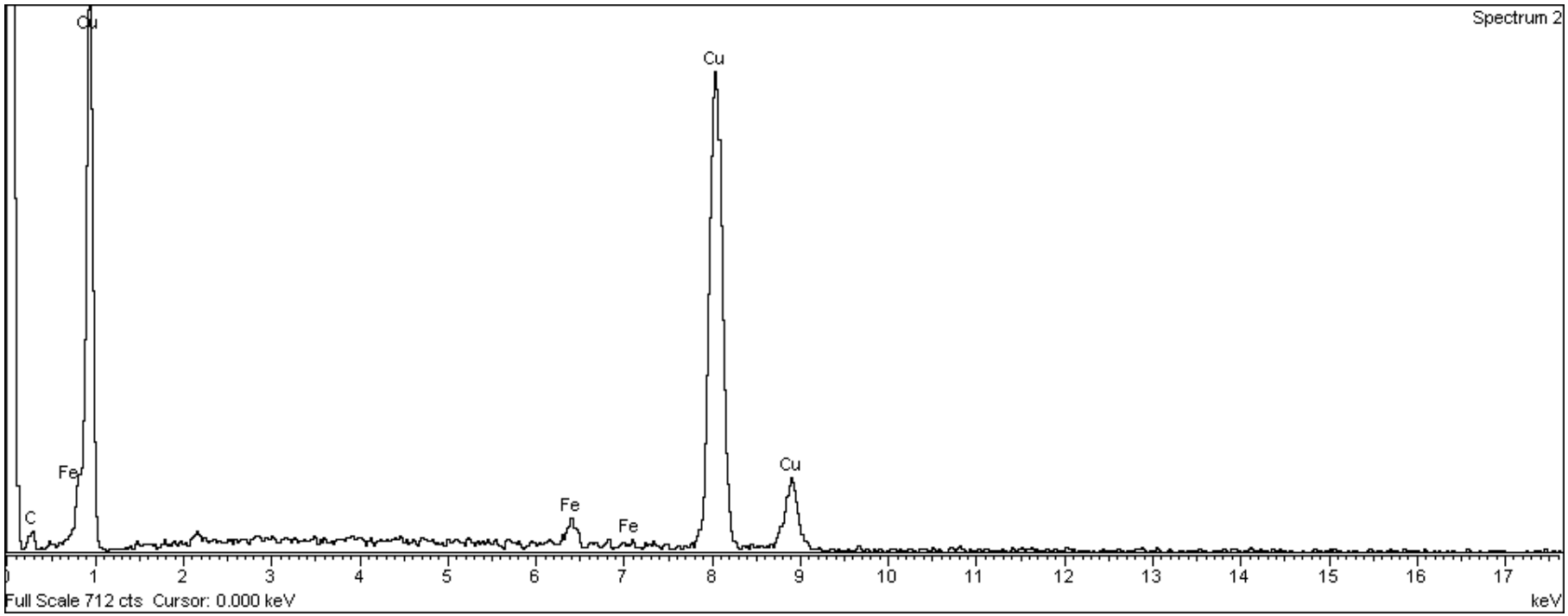


Figure 38: EDS Analysis result for base material, copper (Cu)

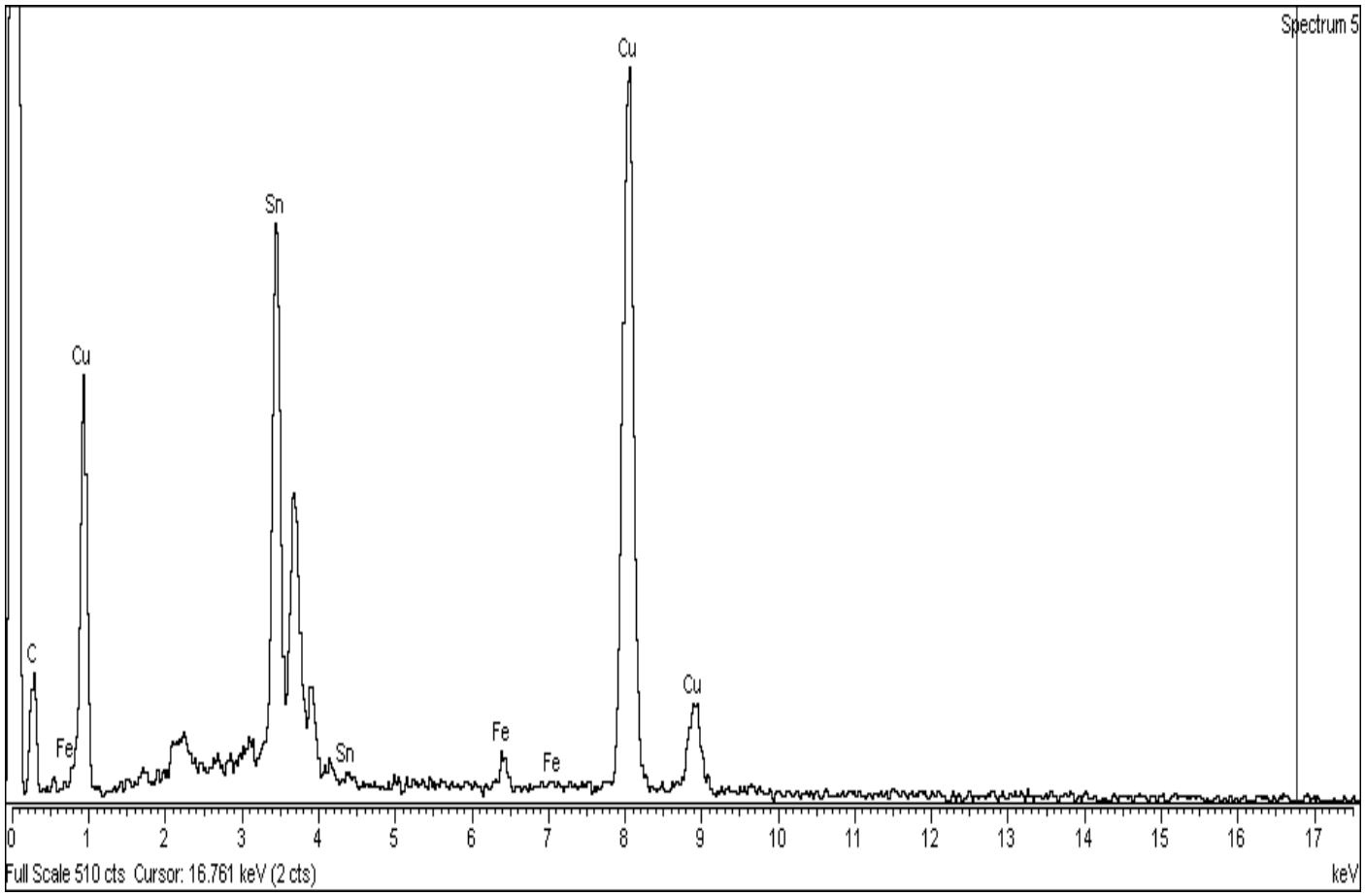


Figure 39: EDS Analysis result for Intermetallic Cu/Sn

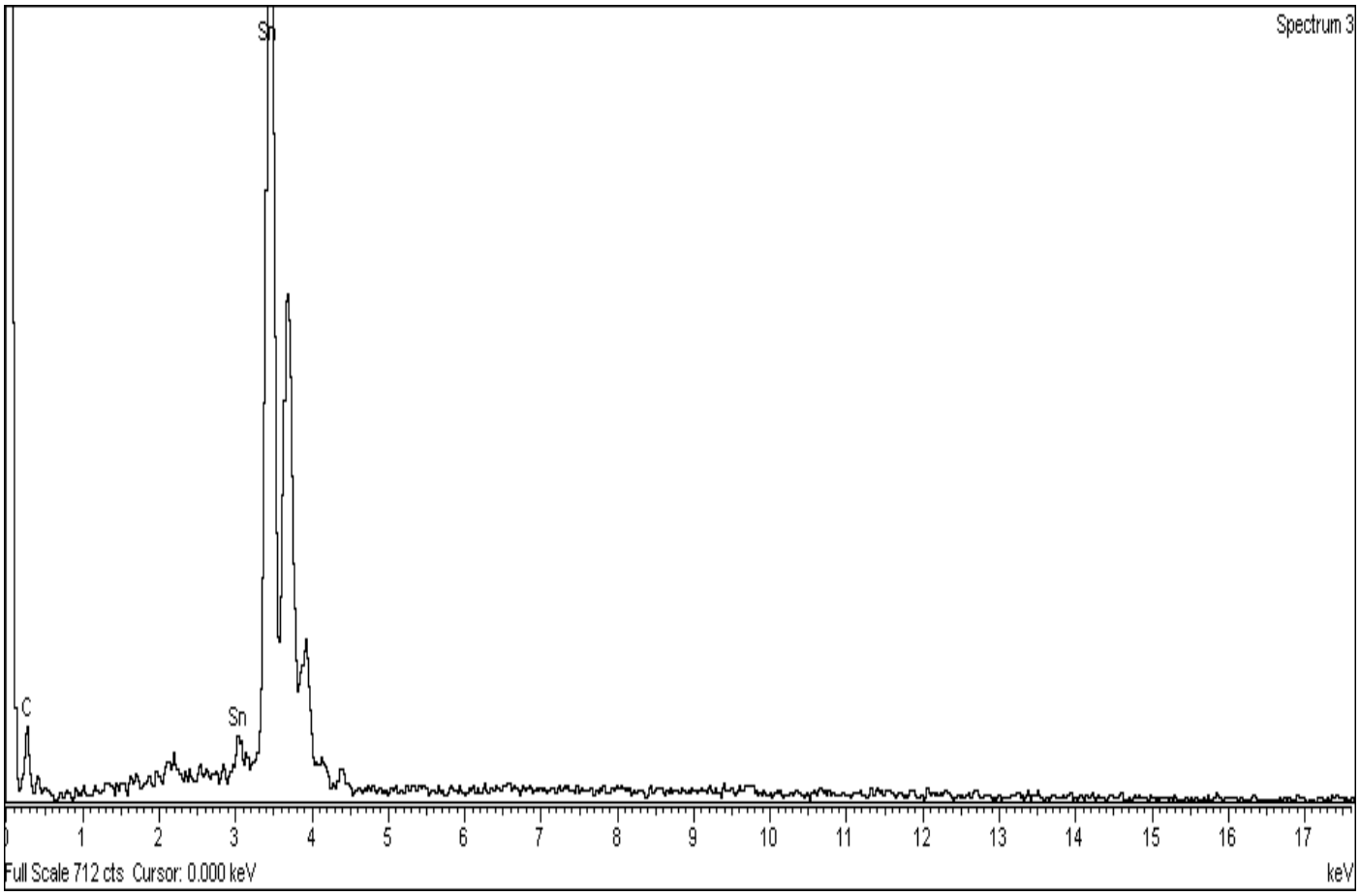


Figure 40: EDS Analysis result for plating material, tin (Sn)

4.2 Discussion

The most challenge in plating process faced by electroplating industry is to obtain a fine uniform plating thickness with the specific requirement. Common lead finish failure attributes are:

- Lead corrosion – corrosion of the leads due to imperfection in the lead finish process
- Poor solderability – insufficient wetting of the solder often caused by contaminants, excess additives, and inadequate plate thickness
- Tin whiskers – formation of very thin extrusions of tin material from the lead finish that can result in electrical shorts between adjacent pins; observed in pure tin plating
- Other lead finish failure attributes – solder dullness, roughness, pitting, tarnishing, inferior appearance, burns [Siliconfareast.com]

Specifically, the potential problems that can occur during plating process are:

- Rough surfaces
- Underplating (Deposit too thin)
- Overplating (Deposit too thick)
- Dimensional tolerance issues
- Inferior appearance

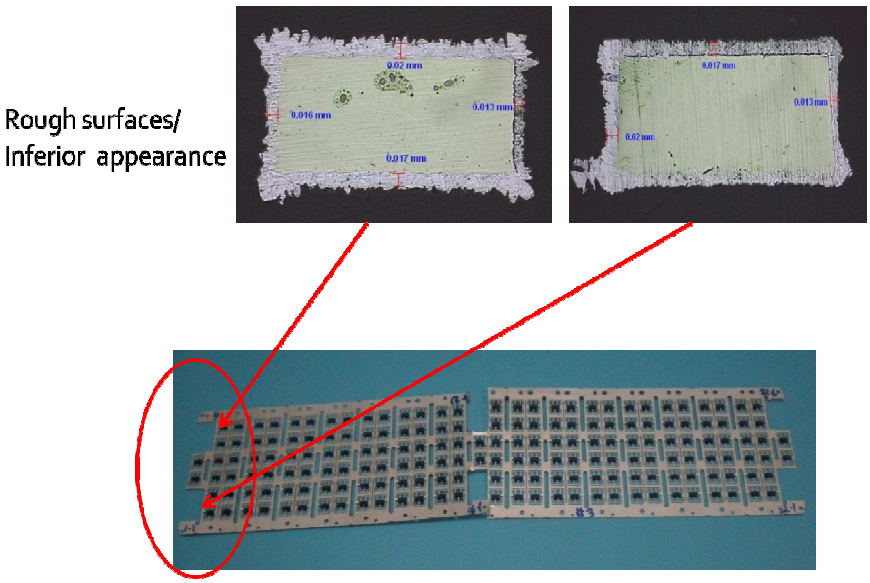


Figure 41: Inferior appearance of IC plating at the left side of SOT-23-3L EIAJ package

The most common causes of this substandard plating are as follows:

- Poor cleaning prior to plating.
- Improper plating solution maintenance.
- A lack of process and/or procedural controls.
- Impure anodes.
- Poor cleaning and drying after plating

CHAPTER 5

CONCLUSIONS AND RECOMMENDATIONS

5.1 Conclusion

From this project, several conclusions can be made by achieving the objective as well as answering the problem statement from the initial stage of this study. They are:

- The average tin plating thickness of SOT-23-3L EIAJ IC package lead frame is 14.976 μm with standard deviation of 2.458 μm.
- Plating thickness measured from this random condition plating solution, resulting variations of distribution and appearance but no measurement found to lie outside the thickness specification range 7-20 μm [Joseph Gauci, 2002].
- The factors influence this result are still unknown and require further investigation by specifying the parameter to be studied such as current density, level of plating solution degradation and plating process geometry. However according to its appearance, it can be said that the most probable cause of this problem is improper solution maintenance performed in the system.
- It was found out through EDS/SEM analysis that the elemental composition of the base material of IC is pure copper (Cu) while the plating material is pure tin (Sn).

5.2 Recommendation

In order to discover the real factors influence plating thickness distribution, a more thorough study should be carried in this project by employing appropriate parameters to be investigated. However, this company might consider a way on how to maintain the plating thickness distribution based on cell geometry factor that have been discussed in the literature review.

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APPENDIX