PROTOTYPE DEVELOPMENT FOR APPLICATION OF A RF ENERGY HARVESTER FOR 2.4GHZ BAND

By

ANDREW MARK ALLOSIAS

(15516)

Dissertation submitted in partial fulfillment of

the requirement for the Bachelor of Engineering (Hon)

Electrical and Electronics Engineering

SEPTEMBER 2014

UNIVERSITI TEKNOLOGI PETRONAS

BANDAR SERI ISKANDAR

31750 TRONOH

PERAK DARUL RIDZUAN

MALAYSIA

DECLARATION OF DISSERTATION

Dissertation Title : PROTOTYPE DEVELOPMENT FOR APPLICATION OF A RF ENERGY HARVESTER FOR 2.4GHZ BAND

I, ANDREW MARK ALLOSIAS (15516) ,

Hereby declare that the dissertation is based on my original work except for quotations and citations which have been duly acknowledge. I also declare that it has not been previously or concurrently submitted for any other degree at UTP or other institutions.

Witnessed by,

_____
(Signature of Author)

Andrew Mark Allosias

Permanent Address:
Block G4-101, Nuri Apartment,
Jalan Bukit Idaman 1,
Bukit Idaman,
68100 Batu Caves,
Selangor

Date : _____

_____
(Signature of Supervisor)

Assoc. Prof. Dr. Rosdiazli B. Ibrahim

Date : _____

CERTIFICATION OF APPROVAL

Prototype Development For Application Of A RF Energy Harvester For 2.4GHz Band

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Andrew Mark Allosias
15516

A project dissertation submitted to the
Electrical and Electronics Engineering Programme
Universiti Teknologi PETRONAS
in partial fulfillment of the requirement for the
BACHELORS OF ENGINEERING (Hons)
(ELECTRICAL AND ELECTRONICS)

Approved by,

_____

AP. DR. Rosdiazli B. Ibrahim

UNIVERSITI TEKNOLOGI PETRONAS
TRONOH,PERAK
September 2014

CERTIFICATION OF ORIGINALITY

This is to certify that i am responsible for the work submitted in this project, that the original work is my own except as specied in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

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ANDREW MARK ALLOSIAS

ACKNOWLEDGEMENTS

First and foremost, i would like to thank Almighty God for by His blessings for providing me with good health along the entire project period.With His grace, i was able to accomplished my final year project on time with promising results and many challenges have been overcomed.

I would like to express my sincere appreciation to my supervisor and co-supervisor, Assoc. Prof. Dr. Rosdiazli B. Ibrahim and Dr. Haris B. Md. Khir from the bottom of my heart for playing the main role of constantly guiding me and providing never ending support. Just as pilgrims depend on the stars the entire journey, their continued guidance has been the compass to my path towards success for this project.

I would also like to the extend my thanks to the knowledgable and cooperative lab technicians and staff of Universiti Teknologi PETRONAS for their dedication and expertise which have been invested in this projects,namely En. Adz Jamros B. Jamali, En. Noor Azwan B. Ahmad, En. Mohd Hasrul Firdaus B. Rostam, En. Muhd Alif Afiq B.Ahmad Rahim. and Ms. Rohayu Bt Roslan. I owe the sucess of the project to them one way or another.

Last but not the least, i would like to pay tribute to my father, Allosias Saminathan, my mother, Philomina Andrews together with my sister, Dr. Jacqueline Ann and extended family. Family are like branches on a tree, we all grow in different directions,yet our roots remain as one. Thanks to all for being a part of this wonderful journey.

ABSTRACT

Radio Frequency Identification is a wireless communication technology which utilizes radio waves to transmit information. This emerging technology has been available for over 50 years yet has only become customary in recent years. For better understanding, the barcode available on groceries items usually serves the same application principle as the RFID. Active or Passive tags are normally associated when dealing with RFID. The major difference of these tags is the presence of an internal battery source. One of the major setbacks in RFID technology is the limitation of the active tag internal battery. Replacement of these batteries usually consumes time and is a hassle. One of the feasible recommendations is to overcome the battery replacement in the RFID tag by harvesting ambient RF waves from surrounding using a RF energy harvester. In the context of this project, the RF energy harvester that is utilized will be a 7-stage Cockroft-Walton rectifier with band pass filters (BPF) and Bessel low pas filter (LPF) integrated on 1.57mm RT/Duroid 5880 (RO5880) laminated thickness operating in 2.45GHz of the transmission medium equivalent to the transmission of the Wi-Fi signal. Since the output energy obtained from the harvester is figuratively low and un-usable. A step –up circuit with charging and storage function will be implemented to produce a more usable energy output. The main component that will be utilized in the proposed design is a power harvesting integrated circuit (IC), LTC 3105. The simulation for the proposed circuit design is done using Linear Technology (LT) Spice Software followed by fabrication of design on to Printed Circuit Board (PCB) using the EAGLE Software. Upon completion of the prototype, the functionality of the prototype was tested under ideal situation where, an output of 5V and 100mA was achieved with a constant supply of 2.45GHz at (-5dBm) which yields and efficiency of 80%.

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LIST OF ABBREVIATIONS

AUX	Auxiliary
BPF	Band Pass Filter
DC	Direct Current
FYP	Final Year Project
IC	Integrated Circuit
LDO	Low Dropout
LPF	Low Pass Filter
MPPC	Maximum Power Point Control
PCB	Printed Circuit Board
RF	Radio Frequency
RFID	Radio Frequency Indentification
SMD	Surface Mount Devices
V	Voltage

CHAPTER 1

INTRODUCTION

In the advancement of technologies, more ways of transmitting and receiving information wirelessly is emerging. This communication technologies was present for along time but has only came to light in recent years. One of this technologies is, Radio Frequency Identification (RFID). This technology does not need physical connection or the involvement of contacts for storage and reading of data entrusted in an RFID tag. RFID technology communication utilizes the Radio Frequency (RF) waves which normally only focuses on a selected bandwidth from the wide range of RF waves.

There are two types of tags, commonly related to RFID,which are, Active and Passive tags. The major difference between these two tags is the presence of an internal battery source made available in the Active RFID tags. The major setback for this tags are the replacement of the internal battery. Therefore, a much feasible solution towards the limitation of the on-board battery was to intergrate an RF Energy Harvester with the existing Active RFID tags. Since there is still small amount of energy in scattering RF waves, by using an RF energy harvester, these signal powers or strengths can be transformed into electrical power and thus charge the internal battery on-board the Active RFID tag.

By using the concept idea, this project will look into the development of a prototype for the application of a Radio Frequency (RF) Energy Harvester. The Energy Harvester will operate at RF bandwidth range of 2.4 – 2.48GHz. The ideology of energy harvesting is made practical by the device by harvesting ambient RF waves of the selected bandwidth from the surrounding to produce electrical power. The RF energy harvester type that is utilized in this project would be the 7-stage Cockroft-Walton Rectifier.The power obtained may be figuratively small, generally in millivolts and would not be sufficient to source low power applications.

The main scope of this project is focused on the utilization of the power that is produced by the 7-stage Cockroft-Walton Rectifier. The project will pursue the basis of stepping – up the output power to ensure the harvester output power is more usable by most applications while charging and storage function of the usable output power will also be made present. The suggested idea meant by making the output power more usable, would be powering up a Zigbee module. The extracted power from the harvester would presentably be in Direct Current (DC) form. The prototype will mainly consist of a stepping –up circuit with charging and storage functions, by using results obtained from the 7-stage Cockroft-Walton as its design parameters.

1.1 Background Study

The RF energy harverster that is utilized for this project uses a Cockroft-Walton voltage multiplier topology integrated with a Band Pass Filter (BPF) and a Bessel Low Pass Filter (LPF). The Cockroft-Walton topology is also often referred as the Villard voltage doubler. The Cockroft-Walton rectifier is mainly made up of Schottky diodes and Capacitors. Therefore the appropriate type of Schottky diode and capacitance value are crucial for the RF energy harvester. Figure 1.1 shows an example of the 7-stage Cockroft-Walton scheme.

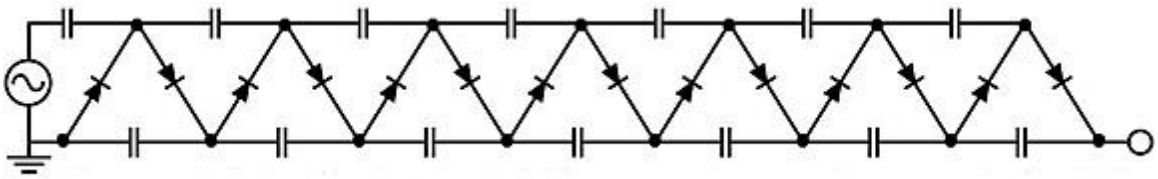


Figure 1.1: Half-wave Cockroft- Walton Voltage Multiplier Topology.

The output power obtained from the energy harvester is then channeled into a circuitry which provides stepping-up with charging and storage function. This is based on the output from the RF energy harvester, where the output is considerably small in DC power and not entirely stable. Therefore, it is proposed to utilize LTC3105 IC. The IC will stabilize the output power from the RF energy harvester in order to provide a smooth charging process to the super capacitor. The output rating from the super capacitor will be based on the low power application that will be using the stored energy. The capacitor that is used in the project is rated at 0.1F (Farad), 25V. A lower rating capacitor is used to demonstrate that the capacitor is being charged at a shorter time period.

1.2 Problem Statement

The problem with RF energy harvesting at 2.4-2.48GHz bandwidth is that the signal characteristics of the RF wave is unstable and un-continuous. Therefore, the output from the RF energy harvester is also disrupted and cannot supply a steady output. The stability of the signal solely depends on the availability of Wi-Fi signals.

Ambient RF wave at 2.4-2.48GHz also have weak signal strength. The signal strength measure in a UTP laboratory recorded between the ranges of -48dBm to -63dBm. This will result in the output of the RF energy harvester to be in millivolt range because the harvesting energy power is small. The efficiency of the power conversion depends also on the Wi-Fi signal strength captured and converted.

No storage capability is also problem with regards to this project. Energy which has successfully converted is not stored would be put to waste. For its stored, it could be used at any period of time.

1.3 Objectives

The objective of the project is to implement the output from the RF energy harvester by developing step-up circuit with charging and storage function. To this moment, the objectives of this project are summarized as follows:

- To investigate and design a step-up circuit with charging and storing function that is merged with the RF energy harvester circuit to efficiently source a low-power application.
- To develop and fabricate the storing and charging circuit with step-up function on Printed Circuit Board (PCB)
- To perform field testing and analyze the performance of the propose design.

1.4 Scope of study

Project investigation will mainly cover design optimization for the step-up circuit with charging and storage function incorporating a super capacitor in the context of utilization of harvested power from the RF energy harvester.

It will focus mainly on improving and altering the designed circuit for the best utilization of output energy obtained from the RF energy harvester. Antenna design and rectifying circuit are beyond the scope of this project

The proposed design will be fabricated on PCB with surface mounted devices to produce a working prototype that will serve as confirmation for the simulation performance work. Circuit design will be carried out in LT-Spice software prior to the fabrication of the layout design on the PCB using the Eagle software.

CHAPTER 2

LITERATURE REVIEW

The basic block diagram for the RF energy harvesting system is shown in Figure 2.1. As shown, it has three main subsystems, which are the RF Harvester Circuit, Circuit Integration and Output Application. The detection of the RF signal wave, energy conversion and the DC output obtained are covered in the RF Harvester Circuit subsystem. While the Circuit Integration subsystem, includes the design and usage of the LTC3105 IC together with a super capacitor. Finally the Output Application subsystem, a Zigbee module is considered to be tested with the completed prototype.

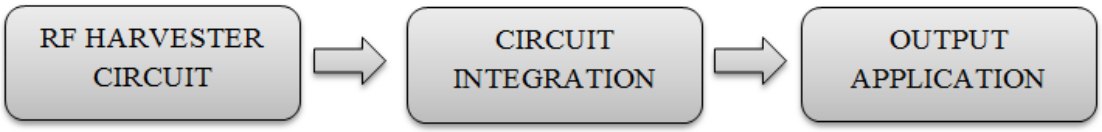


Figure 2.1: Basic block diagram for RF Energy Harvesting System.

2.1 RF Energy Harvester

RF energy harvesting utilizes low power energy and can be considered as a part of renewable energy for it does not bring damage [1]. RF energy harvesting has resolved the challenges once faced by wireless devices and low power integrated circuits. The common challenge was the onboard battery for the wireless or low powered devices had a short life span and replacing or maintaining it often was costly and time consuming according to E.M. Cooney and S. Kim [2][3]. Therefore, with the presence of RF energy harvester, the wireless devices and low power circuits are able to self-sustain by using ambient frequencies to source power which is proven by S. S. B. Hong et al [5][6].

A RF energy harvester contains a rectenna system to convert the ambient RF sources into DC power. The conventional rectenna system consists of usually, an antenna, RF to DC rectifying circuit and DC Filters [6][7]. Basic and conventional rectenna architecture is shown in the Figure 2.2. Channeling and capturing the most amounts of RF transmission signal power is the sole function of the antenna. While, the RF to DC rectification circuit converts the RF energy into DC power supply. There are various reasons to the use of DC filter. It is primarily used for smoothening of the DC output. Suppression of the higher frequency harmonics has also been one of the capabilities of filters in order to maximize output.

Figure 2.2: Block diagram from Rectenna Architecture.

The topology used for the RF to DC rectification here is a 7-stage Cockroft-Walton Voltage Multiplier. There are also other topologies associated with rectification, which are Greinacher and Dickson configurations with the utilization of schottky diodes. But according to H. Yan et al. [21], the results obtained using the Dickson and Cockroft-Walton topologies are relatively similar.

J. P Curty et al. [22] found out that a higher DC voltage can be achieved using the Greinacher topology which usually needs multiple stages. The drawback of the topology is excessive cascading might produce lower output voltage due to the accumulation of parasitic capacitances at high frequency.

The DC Filters that were used for the project is a band pass filter (BPF) and Bessel low pass filter (LPF) on 1.57mm RT/Duroid 5880 (RO5880) laminated thickness. The operations were carried out on 2.45GHz of the transmission medium, which equivalents to the transmission of Wi-Fi signal [5]. The 7-stage Cockroft-Walton Printed Circuit Boards (PCB) (RO5880) laminate parameters can be seen in the table below.

Table 2.1: RO5880 laminate parameters

Description	Parameters
Substrate Thickness	1.57mm
Relative Dielectric Constant	2.2
Relative Permeability	1
Dielectric Loss Tangent,	0.0009
Conductor Conductivity	$5.8x10^7$ S/m
Conductor Thickness	17.5µm

The 7-stage Cockroft-Walton Rectifier with BPF and LPF is tested and the results obtained are as follows.

Table 2.2: The result of the 7 stage Rectifier + BPF + LPF (S. S. B. Hong et al., 2014)

Frequency (GHz)	7-Stage Rectifier + BPF +LPF		
	Lower input power, (dBm)	DC Output Voltage,(V)	Efficiency, η(%)
2.40	-1	1.71	0.37
2.45	-7	1.63	1.33
2.48	-20	1.54	23.72

There are few other parameters that should be considered in achieving the output voltage of the rectifier. Such as, type of antenna and transmitting / receiving RF signal strength. These parameters might affect the output voltage from the rectifier.

2.2 Circuit Integration

Circuit Integration consists of 3 components as well, which are, the Step up Converter, Charging Circuit and Storage Circuit. The output that is obtained from the RF energy harvester is already in DC and the power is very small also inconsistent. The inconsistency or the fluctuation of the output is caused by the availability of the Wi-Fi signal and also the efficiency of the antenna to detect the Wi-Fi signal.

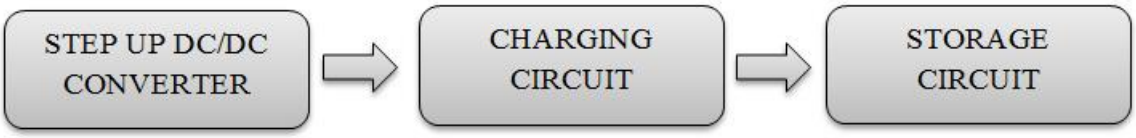


Figure 2.3: The Circuit Integration Block diagram.

Once the output of the RF harvester is obtained, the output is then stepped up using a DC to DC converter. The multiplied or stepped up output is used to charge a super capacitor. The super capacitor is charged until it reaches maximum capacity. Once the super capacitor discharges at a constant rate or in other words, when the power is used to source an output application. The super capacitor power will start to deplete which will activate the charging system again.

2.2.1 Step up DC/DC Converter

The LTC 3105 IC provides function of stepping up the output voltage with a relatively low input voltage. The IC is capable of producing two output supply voltage known as Low Dropout (V_{LDO}) output and Boost output (V_{OUT}). Both output voltage can be adjusted to desired value by the manipulation of a simple voltage divider using resistors. The minimum input voltage need to start up the IC is 225mV which a Boost output and LDO output of 5.1V and 3.1V is able to be achieved.

The IC is a surface mount device (SMD) with size of 3mm X 3mm X 0.75mm. The figure below show the configuration of the IC while the function of each pin can be obtained in the Appendix I attached.

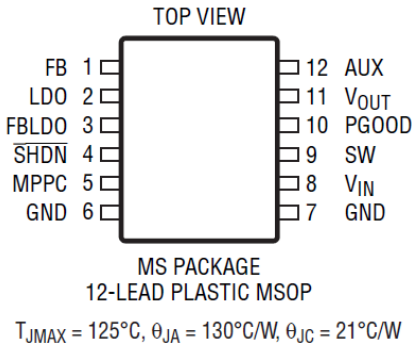


Figure 2.4: Pin Configuration of LTC3105 MS Package.

Compared to the selected step up DC/DC converter, there are many method and circuitry present to achieve this function.

1. Charge Pumps

Charge pumps were used in K. C. Wei et al [8] to overcome the use of external voltage regulator by utilizing the supply voltage to generate higher DC voltage. Charge pumps can be implemented into the RFID technology due to the suitability of the charge pumps characteristics of application, which is, low power consumption, high efficiency of energy and low current driving supply [9].

The main components of the charge pumps consist of diodes, nMOS and pumping capacitors, for it is a capacitor based circuit [8][9], where the voltage gain plays an important role when voltage is pumped up stage by stage. The voltage gain has a relationship with voltage loss in the circuit which is affected by the nMOS threshold voltage [9][10], and together with parasitic capacitors influences the pumping efficiency [10].

It is found that improved four stage charge pumped circuits [11] recorded minimum parasitic capacitance, with pump capacitors valued at 0.1pF producing 5.95V from 1.8V input voltage supply at pumping clock frequency 20MHz, ideal for low voltage devices [8].

2. DC-DC converters (Buck- Boost Topology)

Another method which is common referred to charging circuit is DC - DC Converter. The converter used in C. Karnjanapiboon et al [13][15] had incorporated the Buck –Boost topology. In [13], the converter was used on 4 batteries connected in series to implement balance charging. The circuit consisted of switches, diode and inductors [14]. Minimization of operating voltage rating of active switches and diodes are one of the benefits of the converter [13].

The DC converter used in [15] served two main purposes, which is, ensuring high voltage during charging and to maximize power extraction from the photovoltaic cells by manipulating the On/Off switching duty cycle [16]. In both research, implementing DC-DC converter as to charging circuit was related to requirement of additional volume and cost due to component rated high voltage [13][15],which arises concerns on conduction loss [13]. If a super capacitor is utilized in charging circuit and its starts charging from an empty state, the inrush current can cause the circuit charging current to be lowered.

2.2.2 Charging and Storage circuit

The charging circuit and storage circuit are commonly tied together though having separate block diagrams. The charging circuit is the second step in the circuit integration. The circuit utilizes output power from the Step up DC/DC converter to charge the storage devices, typically a super capacitor.

The storage circuit for this project is defined as a device or equipment that is able to reserve a certain quantity of energy by utilizing the charging circuit. Once charged, the energy can be used at any given time up until the energy in the device completely depleted and can be only used once again upon charging the device [18].

The most common storage device or equipment used for energy is the super capacitor, which is also known as ultra-capacitor. Super capacitors have ultimately long life cycles which allow them to charge and discharge nearly unlimited number of times and are one of the reasons of preference [15].

Two scenarios usually faced by super capacitors are Inrush Current and Cold Booting [15]. Inrush current is when the super capacitor is nearly empty and reduces the charging current. Besides that, cold booting is the pointless operation and depletion of the super capacitor due to stored energy not being over the usable threshold voltage.

2.3 Output Application

The suggested output application of this project would be sourcing of a Zigbee module. The output power from the super capacitor will be determined to suit the input power rating of the Zigbee module. The particular Zigbee module model is XBee Series 2 OEM RF Module, which requires and input voltage and current of 3.3 V and 40 mA. The other characteristics of the Zigbee module is available in the datasheet are attached in the Appendix II.

CHAPTER 3

METHODOLOGY

3.1 Experimental Work

The figure below shows the flow chart for the entire project from Final Year Project (FYP) I to FYP II. The detailed description of each step is explained in the Research Activities section. The entire project is separated into three phase which is the Initial Phase, Simulation Phase and Fabrication Phase.

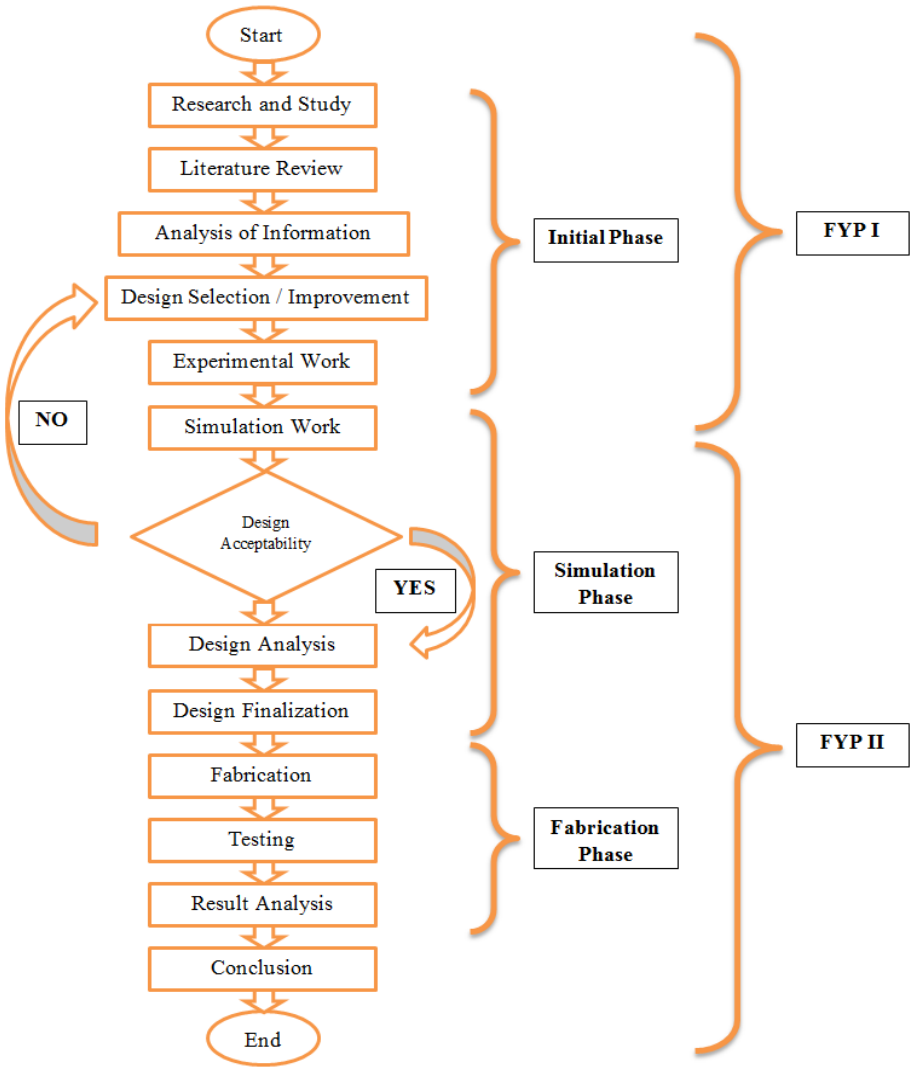


Figure 3.1 Process Flow for Experimental Work

3.1.1 Initial Phase

In this phase, the output results data from the 7-stage Cockroft-Walton rectifier is collected. The input of the 7-stage Cockroft-Walton was connected to Agilent RF Signal Generator and the output was connected to a 1 MΩ load together with Tektronix Mixed Domain Oscilloscope (MDO3014). The set up can be seen in the figure below.

Figure 3.2: Agilent RF Signal Generator.

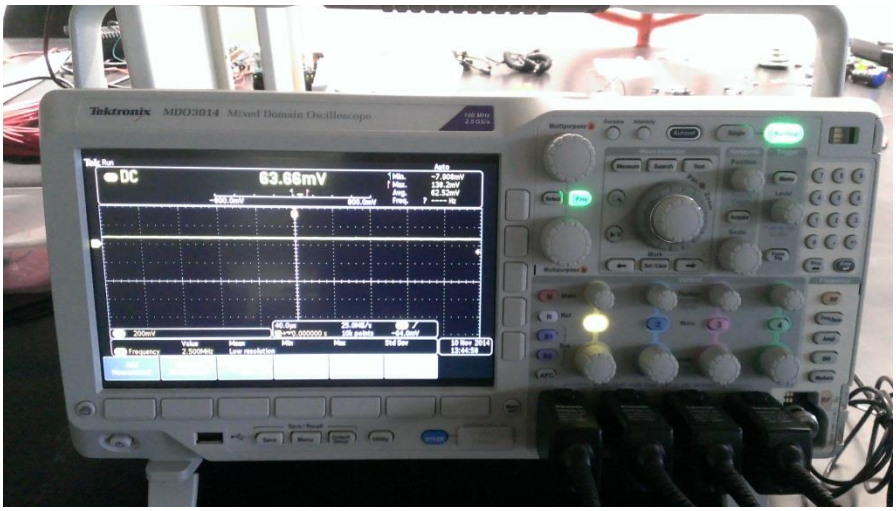


Figure 3.3: Tektronix Mixed Domain Oscilloscope (MDO3014)

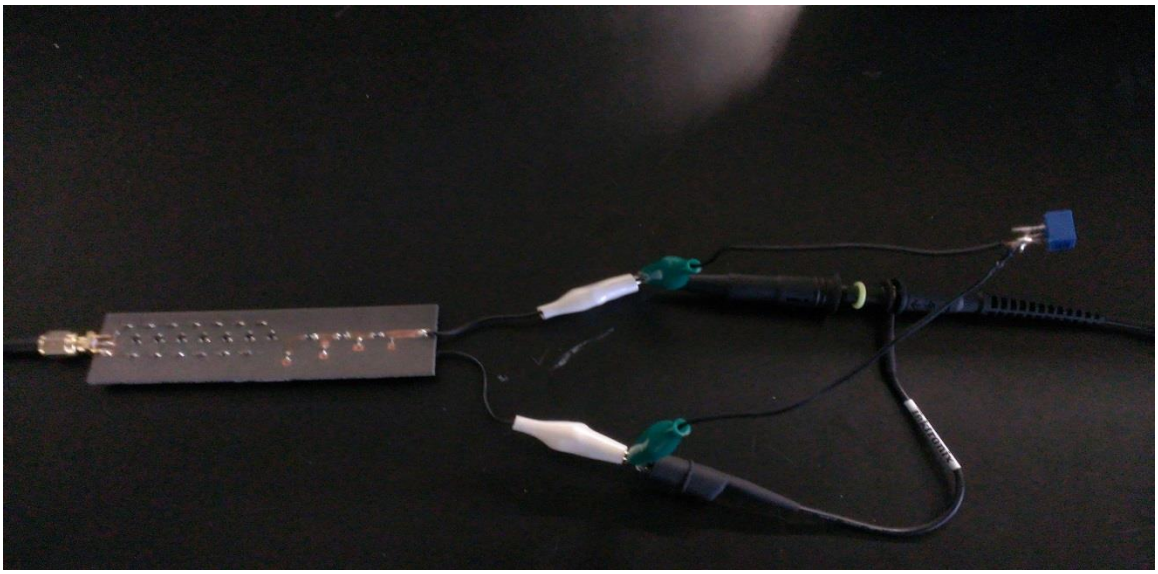


Figure 3.4: The 7-stage Cockroft-Walton Set Up.

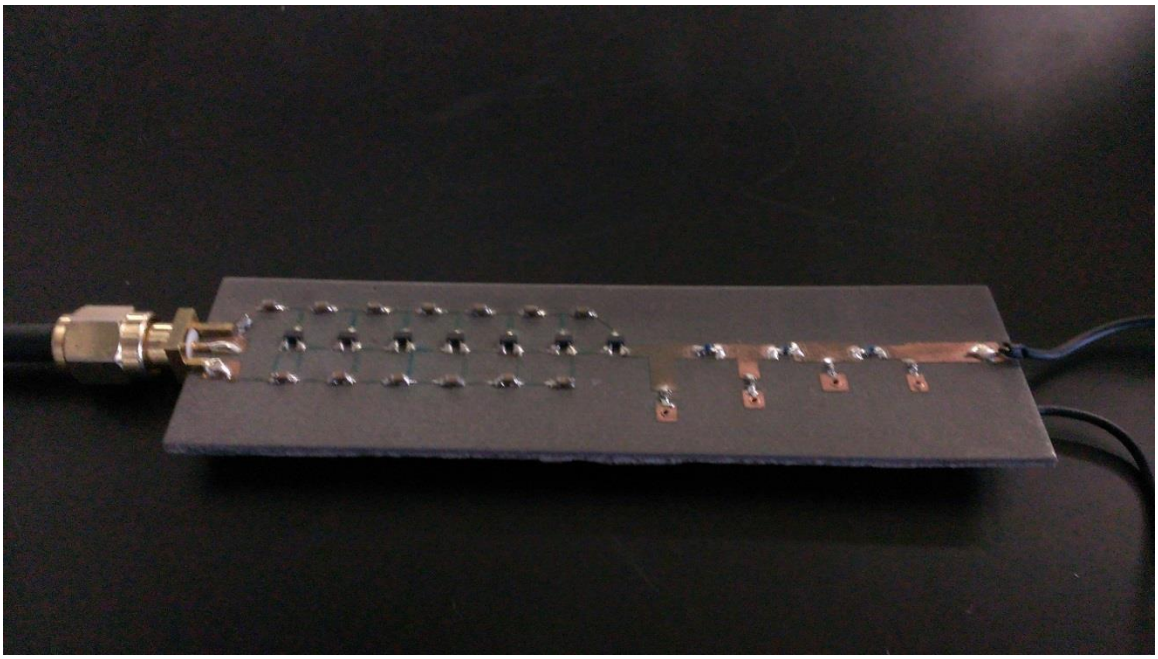


Figure 3.5: 7-stage Cockroft-Walton Rectifier.

A close up view of the 7-stage Cockroft-Walton can be seen in figure 3.4. Once the 7-stage Cockroft-Walton rectifier was set up accordingly, the rectifier was tested with 3 different input RF signals (2.4GHz, 2.45GHz and 2.48GHz) with various dBm ranging from 0dBm to -30dBm together with various load resistance. The results was observed and recorded.

During testing, it was noticed that an Insertion Loss has occurred. The RF signal generator was set at -10dBm but the value that was recorded on the Oscilloscope was -12dBm. Therefore, upon carrying out with the testing, the insertion loss was taken in account and is assumed at the range of 0dBm to 5 dBm. The figures below show the Insertion Loss and the connection method that was used to measure.

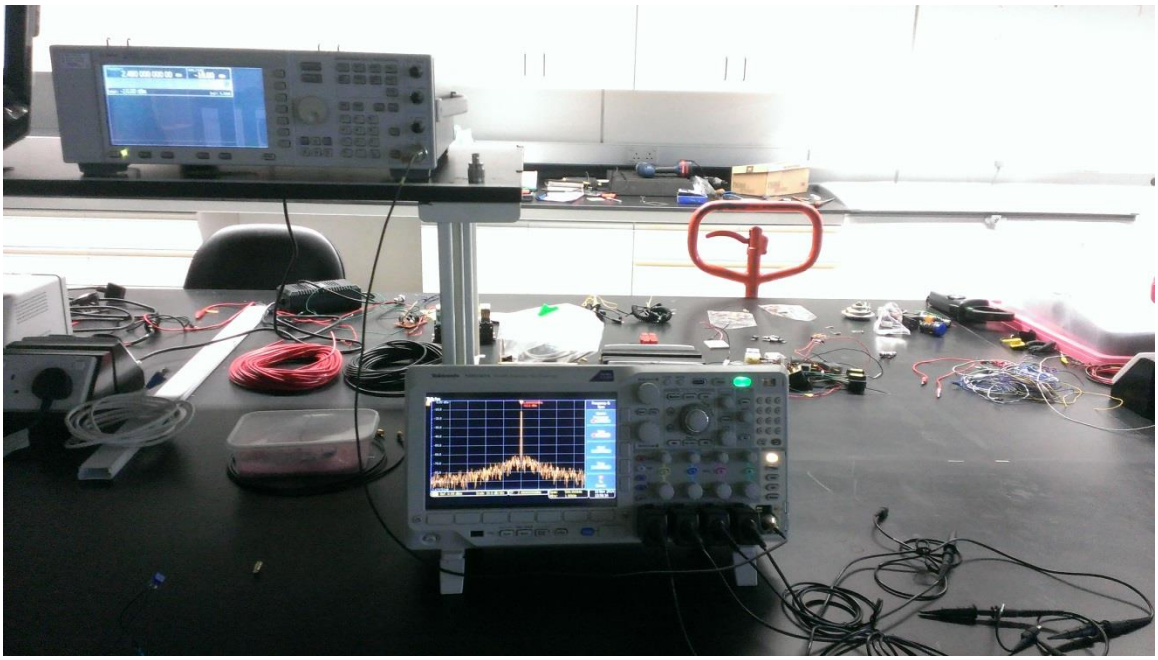


Figure 3.6: The Set Up to Measure Insertion Loss.

Figure 3.7: Input signal from RF Signal Generator with -10dBm.

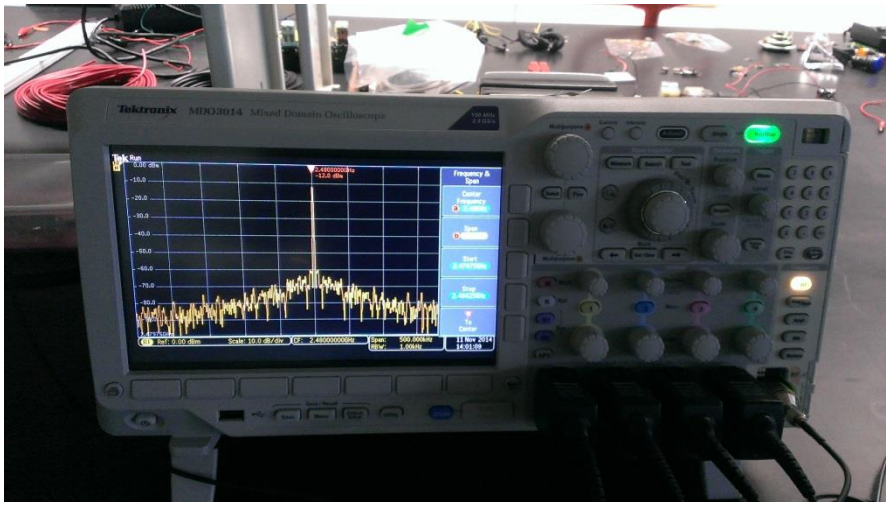


Figure 3.8: Oscilloscope indicating an input signal with -12dBm.

3.1.2 Simulation Phase

The most crucial part to the project would be design on the Step up DC/DC converter. The LTC 3105 that will be utilized in this project has the ability of produce an output voltage up to 5V DC with a lowest minimum input voltage of 225mV DC, which would be ideal since the output from the 7-stage Cockroft-Walton (RF Harvester) is figuratively low.

The IC has 12 pins which each have its own functions. Therefore, to better understand the IC, the pins functions are attached in the Appendix V. By understanding the pin functions and basic configuration and requirement needed, an initial circuitry was designed and tested using the LT Spice software. In the initial circuit the V_{OUT} voltage divider was fixed to produce an output of 4.95V and LDO pin was channel to GND, therefore resulting in a nominal output of 2.2V that will be available on the LDO. This is one of the uniqueness that is made available by the IC.

The selections of value for the component were based on the initial requirement of the IC. The minimum inductor rating needed for the Boost conversion to take place is 10µH. Therefore the exact value is used in the proposed design. Few fixed capacitors values are required as well by the IC to perform the stepping up function, which are, C_1,C_2,C_5.The value for the capacitors are C_1-10µF,C_2-1µF,C_5-33pF.While C3- 4.7µF was added to give a more smooth LDO regulated output and was found that any greater value didn't not have sufficient smoothing effect. C_6-1µF is added into the V_{OUT} to provide a more stable output by reducing the effect of low frequency disturbance. Figure below shows the initial Design of the Step-Up DC/DC converter.

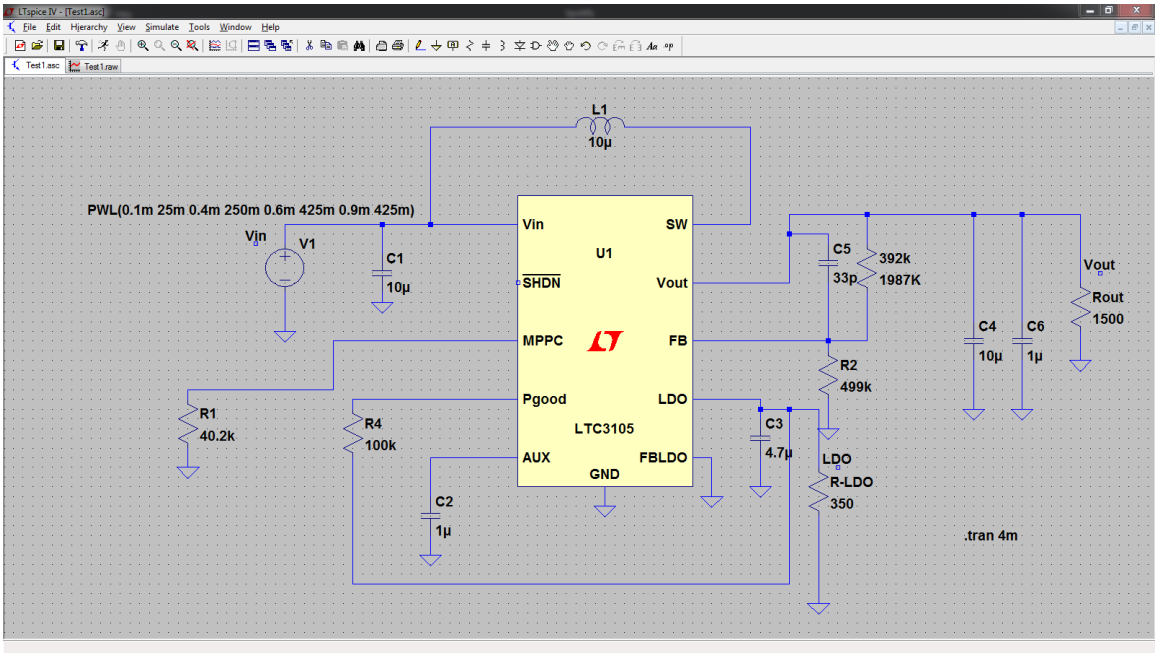


Figure 3.9: Initial Design of the Step up DC/DC Converter.

After further testing, the design was further improved to provide the function of variable output. This is to provide the circuit the ability to cater to its usage. Generally, the power needed to source a Zigbee module would be 3.3V, relatively lower than the power needed to charge a super capacitor circuit.

To provide a more variable range at the output, a voltage divider connection is implemented to the design. The values of the resistors are selected with requirement of the IC, which was to be in or above the kilo-ohm range. Smaller resistance value might cause the design to get heated up quickly and damage the components. The values or the resistors at the MPPC are determined by a normal Ohm's Law. Since there is an internal source of 10µA, the values of the resistors were determined by the maximum power point control (MPPC) wanted. Example if the MPPC is to be set at 402mV, dividing the value with the internal source would result in the resistance value desired, which in this case is 40.2kΩ. Using the same method, a variable MPPC is designed, and the values of resistance are R1-40.2kΩ, R3-200Ω, and R5-402kΩ.

The value of resistance at output is also based on voltage divider and the requirement of the IC. Since the unregulated voltage is able to produce 5V and the LDO regulated output

is able to produce 3V. To provide a variable voltage at the output a voltage divider calculation is utilize. The resistance value is determined by division to get the desired output. For example, if R9 is selected, the division will result as below,

$$\frac{R2 + R11 + R9}{R2 + R11 + R9 + R12}(5V) = \frac{2049k}{4649k}(5V) = 0.44(5V) = 2.2V$$

Therefore 2.2V is obtained at the unregulated output. The values of the resistance can be altered to provide a different ratio for the voltage divider, thus providing a variable at the unregulated output. The process is similar for the regulated output. Therefore the value of resistance that are selected in the design are R7-549kΩ, R8-274kΩ, R9-1.1MΩ, R10-1.1MΩ, R11-450kΩ, R12-2.6MΩ. Figure below show the improved design of the step-up DC/DC converter.

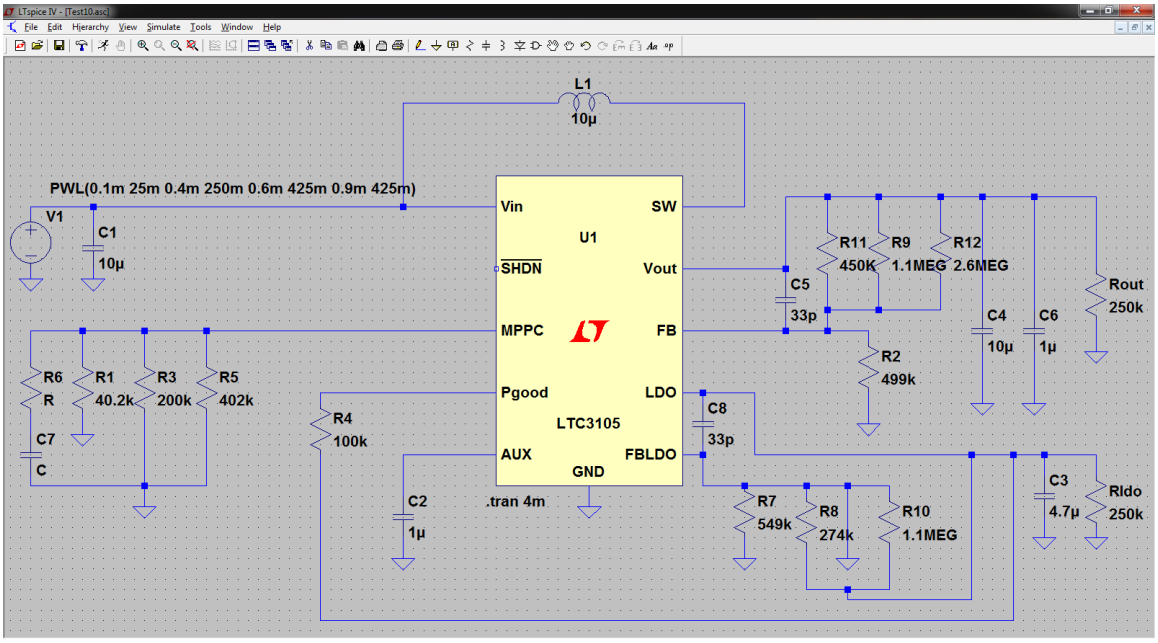


Figure 3.10: Improved Design of the Step up DC/DC Converter.

The improved design utilized a voltage divider function to provide variation to its V_{OUT}, V_{LDO} and MPPC. All the resistors of the voltage divider are connected in the same output path to achieve and variable output. But in practical design for the fabrication of the circuit using Eagle software, the resistance of the voltage divider will be connected to a header pin and by using a pin head, the sought after voltage is selected. The result were obtained and recorded.

3.1.3 Fabrication Phase

Once the simulation design was satisfactory, the exact similar circuit was design using the Eagle 7.1 software. But before the circuit was design, certain specification was needed to be selected and modified to suit the capability of the PCB fabrication available in UTP. The specification can be seen in the figure below.

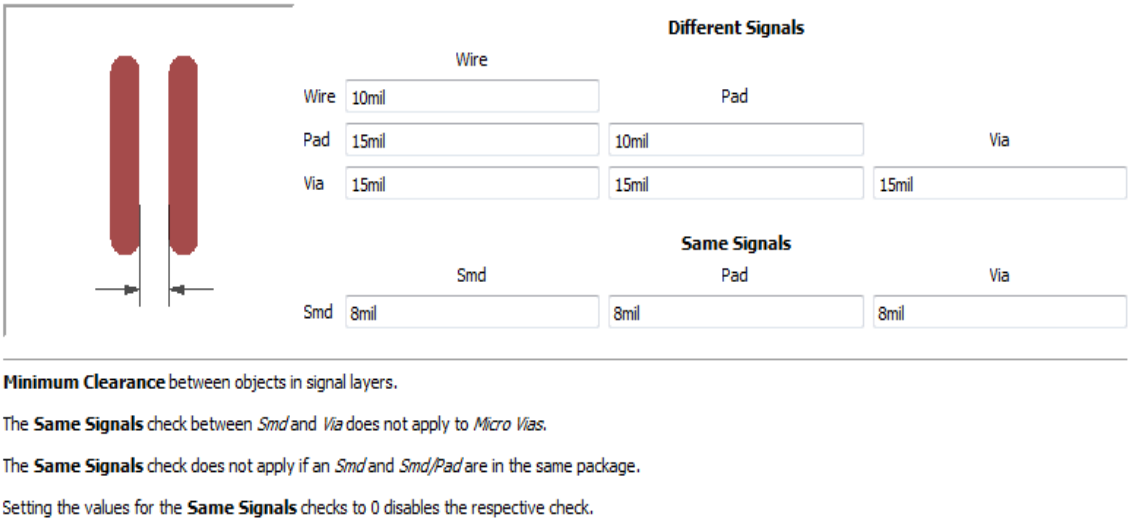


Figure 3.11: Eagle 7.1 Software Design Specification.

Once the design specification was modified, designing of the schematic in the Eagle software was done. As mentioned, the voltage divider is connected via header pins which will only enable one selection of the variable output at a certain given time. The schematic of the design on the Eagle Software can be seen in the figure below.

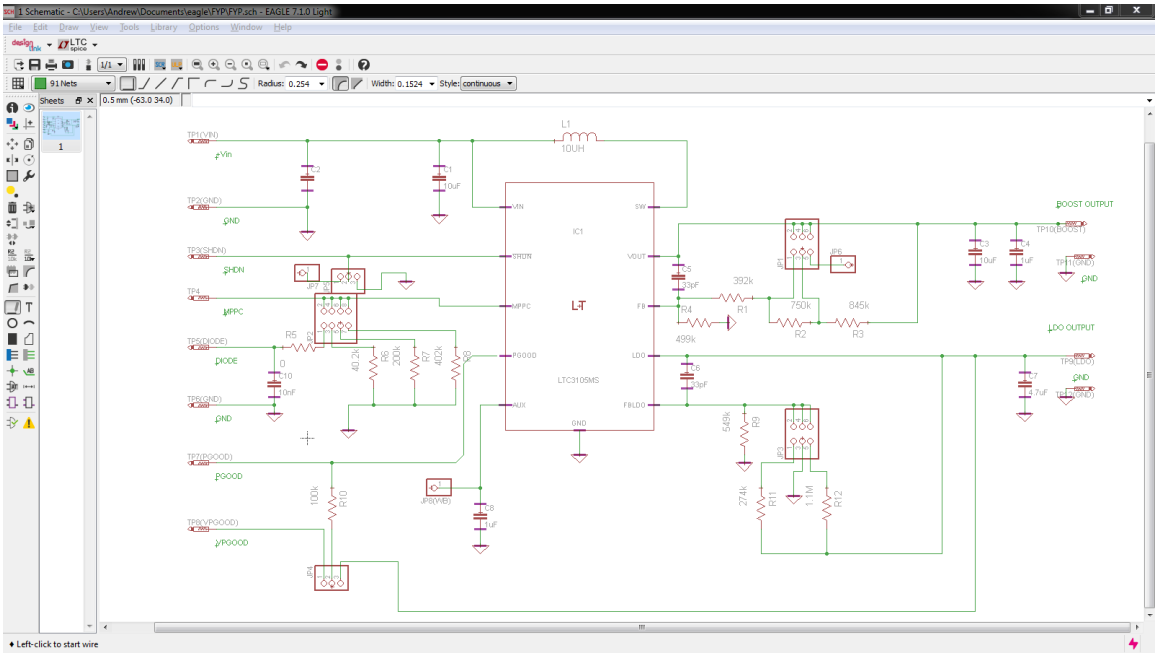


Figure 3.12: Design Schematic on Eagle Software.

A major obstacle that emerged upon designing was that the PCB fabrication requirement of the LTC3105 IC. This is because the minimum clearance requirement of the wire to wire and wire to pad is 10 mil.

1 mil is equivalent to 0.254mm and the clearance needed for wire to wire and wire to pad if the design of the LTC3105 IC was to be implemented on the PCB is the maximum of 6 mil. Therefore, the only solution is to replace the IC pin function with a single header pin where, the IC will be soldered to an SMD adapter and the output of the adapter will be soldered to the single header pins representing the IC pins. The picture below shows the finalized schematic design on the Eagle 7.1 software.

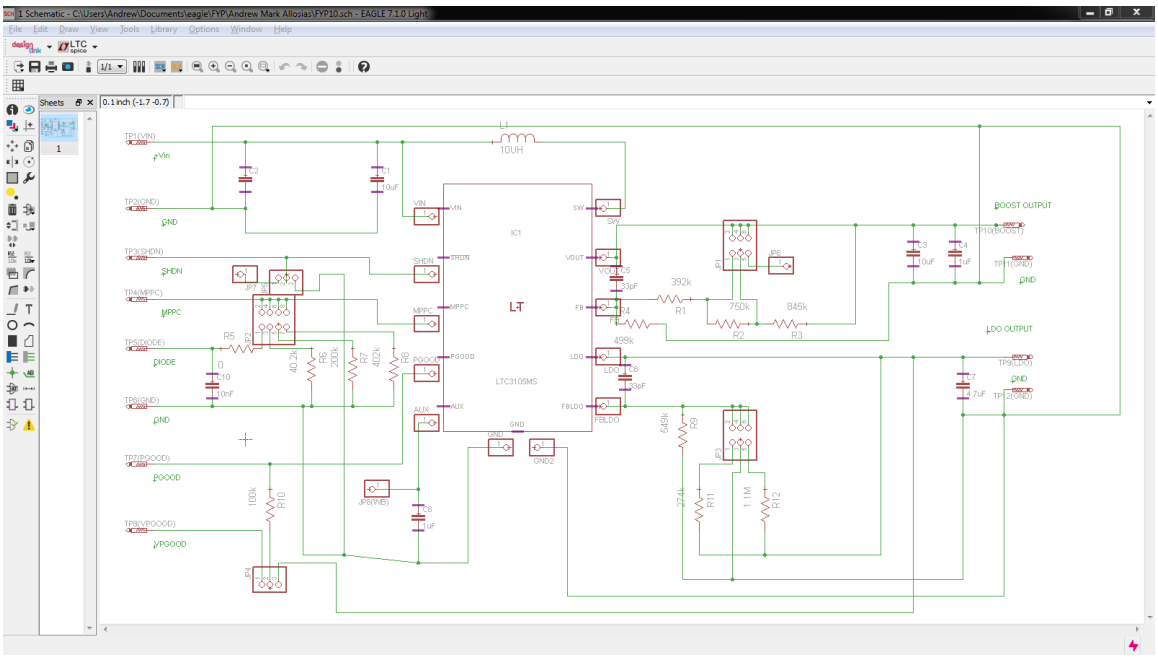


Figure 3.13: The Finalized Schematic Design on the Eagle Software.

3.2 Research Activities

Table 3.1: Research Activities.

No.	Project Activities	Explanation
1.	Literature Review	Research on the step-up circuit with charging and storage function and the various designs methods used in prototyping it. Understanding all related terms while referring to research papers, journals, technical reports and conference papers during this period.
2..	Analysis of Information	Deciding which information is necessary and vital to the project. The problem statement and objectives of the project is outline together with narrowing down the scope of study towards integrating circuit design.
3..	Design Selection and Improvement	Confirming on the design approach that will be taken for the project. Improving the design if necessary.
4.	Experimental Work	Collecting all data information of the design approach as well as doing calculation required. Obtaining parameters required for the software simulation.
5.	Simulation	Simulation of project is done using LT-Spice software based on the requirement.
6.	Fabrication	Based on the software simulation, the proposed design will be fabricated onto the PCB with specific specification using Eagle 7.1 Software.
7.	Testing	Putting the integrating fabricated on the PCB on a field test and collecting results.
8.	Result Analysis	Checking if the actual results and simulation results are as expected or have a recognizable pattern. Minor improvement is done if needed.

3.3 Key Milestones

Table 3.2: Key Milestones for FYP I.

No.	Item \week	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	Submission of FYP Title Selection Form														
2	Literature Review														
3	Design Selection														
4	Submission of Extended Proposal														
5	Proposal Defense														
6	Simulation / Calculation														
7	Submission of Interim Draft Report														
8	Submission of Interim Final Report														

Table 3.3: Key Milestones for FYP II.

No.	Item \week	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	Simulation and Calculation														
2	Design Analysis														
3	Submission of Progress Report														
4	Fabrication														
5	Pre-Sedex														
6	Field Testing														
7	Submission of Draft Final Report														
8	Result Analysis														
9	Submission of Dissertation (Soft Bound)														
10	Project Viva														
11	Submission of Project Dissertation (Hard Bound)														

CHAPTER 4

RESULTS AND DISCUSSION

4.1 Experimental Work

4.1.1 Initial Phase Results

7-stage Cockroft-Walton rectifier was tested with three different input RF signals, which are 2.4GHz, 2.45GHz and 2.48GHz. Several strength of power (dBm) was applied to all of the input RF signals together with various load resistance. The load resistances tested were 100kΩ, 250kΩ, 500kΩ, 750kΩ and 1MΩ. The results of can be seen in tables below.

Table 4.1: Results from 7-Stage Cockroft-Walton rectifier with 100kΩ Load resistance.

Load : 100KΩ

No.		2.4 GHz		2.45GHz		2.48GHz	
		V_{out}	I_{out}	V_{out}	I_{out}	V_{out}	I_{out}
1.	0 dBm	1.264 V	12.64 µA	2.224 V	22.24 µA	2.633 V	26.33 µA
2.	-5 dBm	232.2 mV	2.322 µA	913.7 mV	9.137 µA	1.114 V	11.14 µA
3.	-10 dBm	15.5 mV	0.155 µA	280.6 mV	2.806 µA	243.6 mV	2.436 µA
4.	-15 dBm	1.54 mV	15.4 nA	43.05 mV	0.4305 µA	20.99 mV	0.2099 µA
5.	-20 dBm	**-1.227 mV**	**-12.27 nA**	4.467 mV	44.67 nA	**-1.182 mV**	**-11.82 nA**
6.	-25 dBm	**-2.411 mV**	**-24.11 nA**	**-671.5 µV**	**-6.715 nA**	**-1.14 mV**	**-11.4 nA**
7.	-30 dBm	**-2.010 mV**	**-20.1 nA**	**-1.873 mV**	**-18.73 nA**	**-2.273 mV**	**-22.73 nA**

Table 4.2: Results from 7-Stage Cockroft-Walton rectifier with 250kΩ Load resistance.

Load : 250KΩ

No.		2.4 GHz		2.45GHz		2.48GHz	
		V_{out}	I_{out}	V_{out}	I_{out}	V_{out}	I_{out}
1.	0 dBm	1.471 V	5.884 µA	2.794 V	11.176 µA	3.735 V	14.94 µA
2.	-5 dBm	336.4 mV	1.3456 µA	1.236 V	4.944 µA	1.815 V	7.26 µA
3.	-10 dBm	44.08 mV	0.1763 µA	43.4 mV	0.174 µA	500.5 mV	2.002 µA
4.	-15 dBm	5.96 mV	23.84 µA	87.65 mV	0.3506 µA	49.35 mV	0.197 µA
5.	-20 dBm	**- 777.5 µV**	**-3.11 nA**	12.56 mV	50.24 nA	5.723 mV	22.89 nA
6.	-25 dBm	**-2.158 mV**	**-8.632 nA**	675.7 µV	2.703 nA	**-374.6 µV**	**-1.4984 nA**
7.	-30 dBm	**-2.330 mV**	**-9.32 nA**	**-1.892 mV**	**-7.568 nA**	**-1.247 mV**	**-4.988 nA**

Table 4.3: Results from 7-Stage Cockroft-Walton rectifier with 500kΩ Load resistance.

Load : 500KΩ

No.		2.4 GHz		2.45GHz		2.48GHz	
		V_{out}	I_{out}	V_{out}	I_{out}	V_{out}	I_{out}
1.	0 dBm	1.691 V	3.382 µA	3.116 V	6.232 µA	4.305 V	8.61 µA
2.	-5 dBm	464.6 mV	0.929 µA	1.442 V	2.884 µA	2.286 V	4.572 µA
3.	-10 dBm	78.36 mV	0.157 µA	568.7 mV	1.137 µA5	809.4 mV	1.618 µA
4.	-15 dBm	14.10 mV	28.2 nA	144.6 mV	0.289 µA	95.52 mV	0.1911 µA
5.	-20 dBm	2.332 mV	4.664 nA	27.35 mV	54.7 nA	13.26 mV	26.52 nA
6.	-25 dBm	**-726.4 µV**	**-1.453 nA**	5.523 mV	11.05 nA	1.423 mV	2.846 nA
7.	-30 dBm	**-1.552 mV**	**-3.044 nA**	**-140.6 µV**	**-0.281 nA**	**-1.110 mV**	**-2.22 nA**

Table 4.4: Results from 7-Stage Cockroft-Walton rectifier with 750kΩ Load resistance.

Load : 750KΩ

No.		2.4 GHz		2.45GHz		2.48GHz	
		V_{out}	I_{out}	V_{out}	I_{out}	V_{out}	I_{out}
1.	0 dBm	1.803 V	2.404 µA	3.289 V	4.385 µA	4.596 V	6.128 µA
2.	-5 dBm	536.6 mV	0.7155 µA	1.564 V	2.086 µA	2.509 V	3.345 µA
3.	-10 dBm	106.2 mV	0.1416 µA	652.9 mV	0.8705 µA	1.02 V	1.36 µA
4.	-15 dBm	21.58 mV	28.773 nA	189.3 mV	0.2524 µA	138.1 mV	0.1841 µA
5.	-20 dBm	4.62 mV	6.16 nA	40.57 mV	54.094 nA	22.35 mV	29.8 nA
6.	-25 dBm	375.6 µV	0.501 nA	9.54 mV	12.72 nA	3.725 mV	4.967 nA
7.	-30 dBm	**-975.6 µV**	**-1.301 nA**	1.356 mV	1.808 nA	**-181.5 µV**	**-0.242 nA**

Table 4.5: Results from 7-Stage Cockroft-Walton rectifier with 1MΩ Load resistance.

Load: 1 MΩ

No.		2.4 GHz		2.45GHz		2.48GHz	
		V_{out}	I_{out}	V_{out}	I_{out}	V_{out}	I_{out}
1.	0 dBm	1.914 V	1.914 µA	3.351 V	3.351 µA	4.696 V	4.696 µA
2.	-5 dBm	604.5 mV	0.6045 µA	1.595 mV	1.595 µA	2.605 V	2.605 µA
3.	-10 dBm	132.3 mV	0.1323 µA	675.2 mV	0.6752 µA	1.143 V	1.143 µA
4.	-15 dBm	28.75 mV	28.75 nA	192.0 mV	192.0 nA	174.0 mV	174.0 nA
5.	-20 dBm	6.475 mV	6.475 nA	49.87 mV	49.87 nA	27.09 mV	27.09 nA
6.	-25 dBm	590.3 µV	0.5903 nA	11.45 mV	11.45 nA	5.127 mV	5.127 nA
7.	-30 dBm	**-1.207 mV**	**-1.207 nA**	1.606 mV	1.606 nA	123.5 µV	123.5 pA

By observing all the results, it can be said the average voltage obtained from the RF energy harvester being tested at three different RF input bandwidths, at difference signal strength and at different loads is at millivolt range. This voltage range is unable to source any application or devices. Therefore a Step-Up DC/DC converter is essential to make

the output energy obtained from the 7-Stage Cockroft-Walton rectifier more usable by other application and devices.

4.1.2 Simulation Phase Results

The results from the initial design simulation using LT Spice software can be found in the figure below.

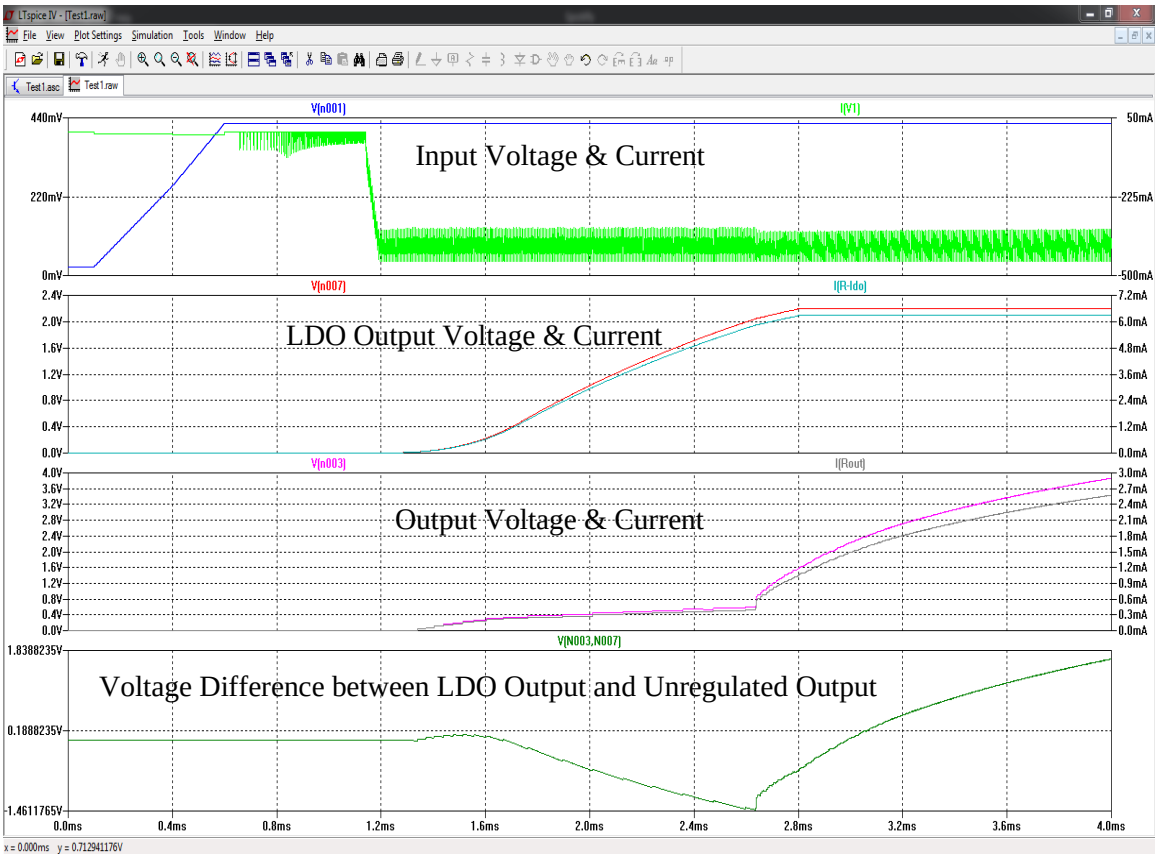


Figure 4.1: Overall Simulation results obtained from Initial Design Schematics.

It can be seen that with the initial basic design of the schematic the voltage for LDO and V_{OUT} is as expected. The output obtained from the LDO is 2.2V for the LDO pin is connected to ground which produces its nominal voltage of 2.2V. The V_{OUT} obtained is recorded at 3.8V. For a better view of the results obtained, the Input supply, the LDO voltage and the V_{OUT} is shown in figures below.

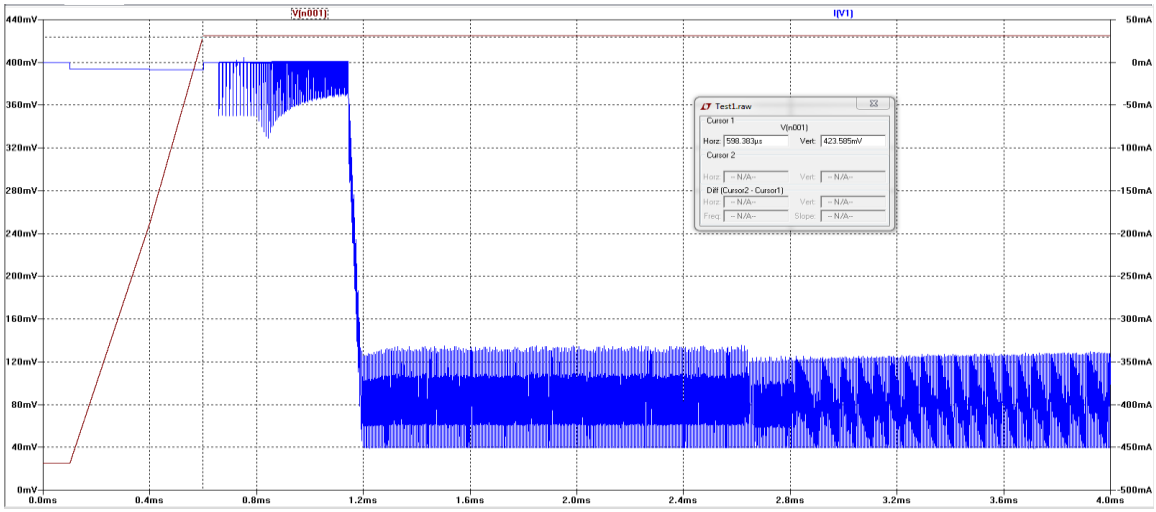


Figure 4.2: Input Voltage Supply for the Simulation.

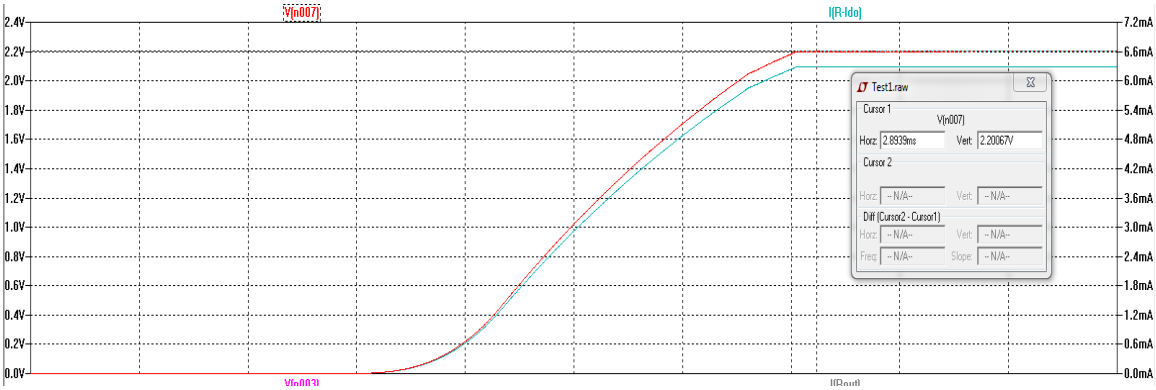


Figure 4.3: LDO Output Voltage for the Simulation.

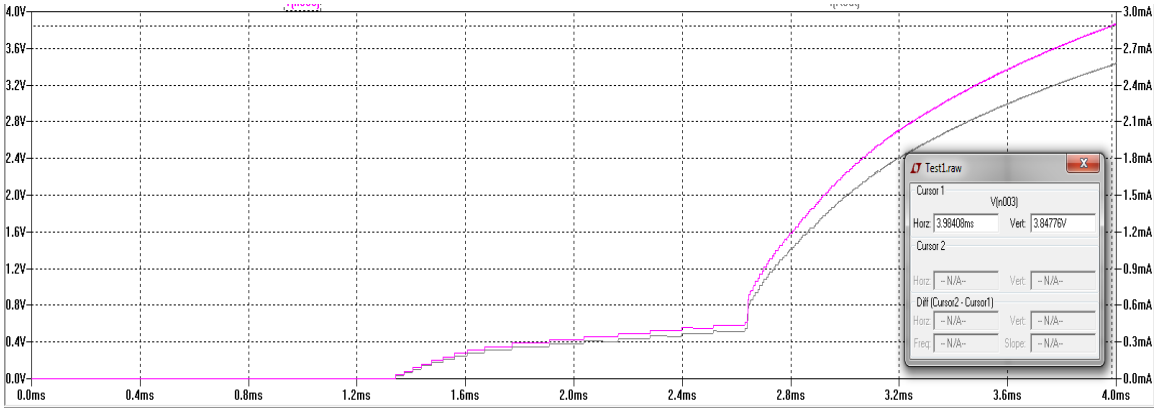


Figure 4.4: V_{OUT} for the Simulation.

After the schematic was further improved with basic voltage dividers to provide the circuit with variable output characteristic, the circuit was tested and results are shown below. The input voltage supplied is similar to the initial basic design.

The MPPC is set to 260mV to fully cater to the output from the 7-Stage Cockroft-Walton rectifier which is low in output. It can be seen that V_{AUX} rises until the circuit enters normal operations where V_{AUX} remains constant and V_{LDO} starts to increase.

The capacitor in AUX starts to discharge as to increase the V_{LDO}. Once V_{LDO} has reached its preset output, V_{AUX} is fed to V_{OUT} to start increasing where V_{AUX} drops lower before remain constant again. At the same time, once V_{OUT} is increasing, C_{OUT} is also discharging until V_{OUT} reaches its preset output. Therefore the unregulated output at 4.9V and LDO output of 3.3V is able to be obtained through simulation. The figures below shows the results.

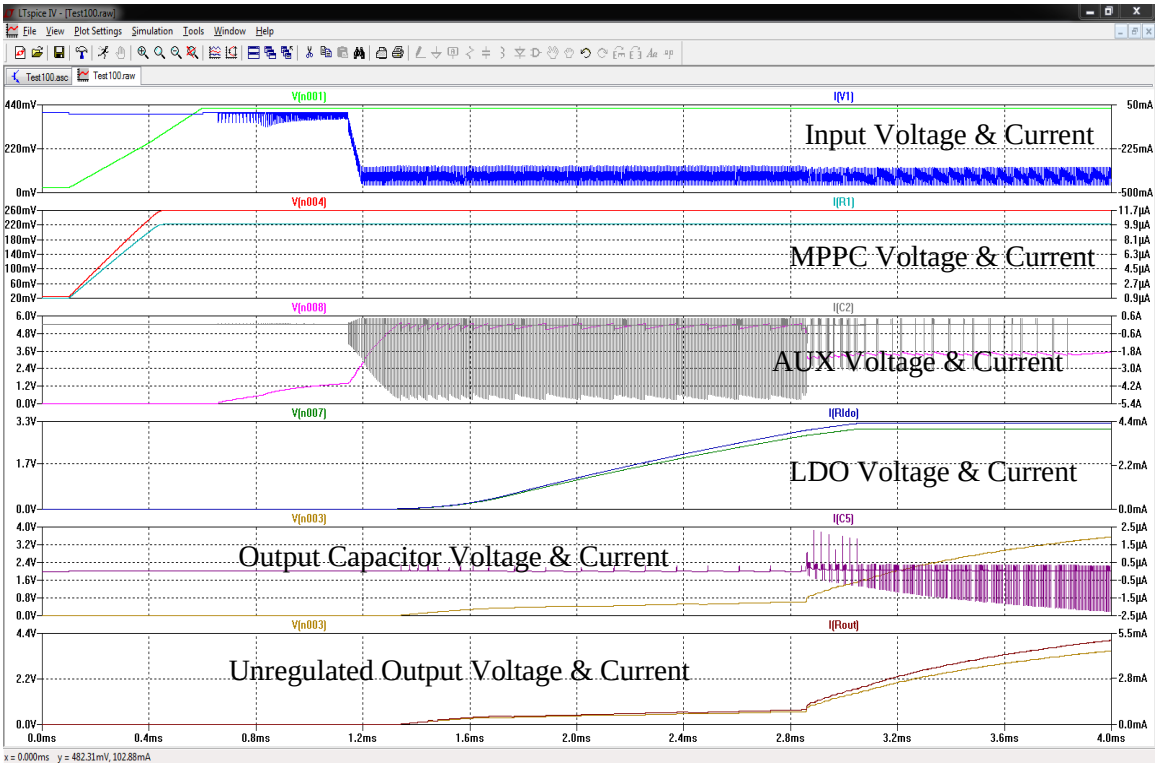


Figure 4.5: Overall Simulation results obtained from Improved Design Schematics.

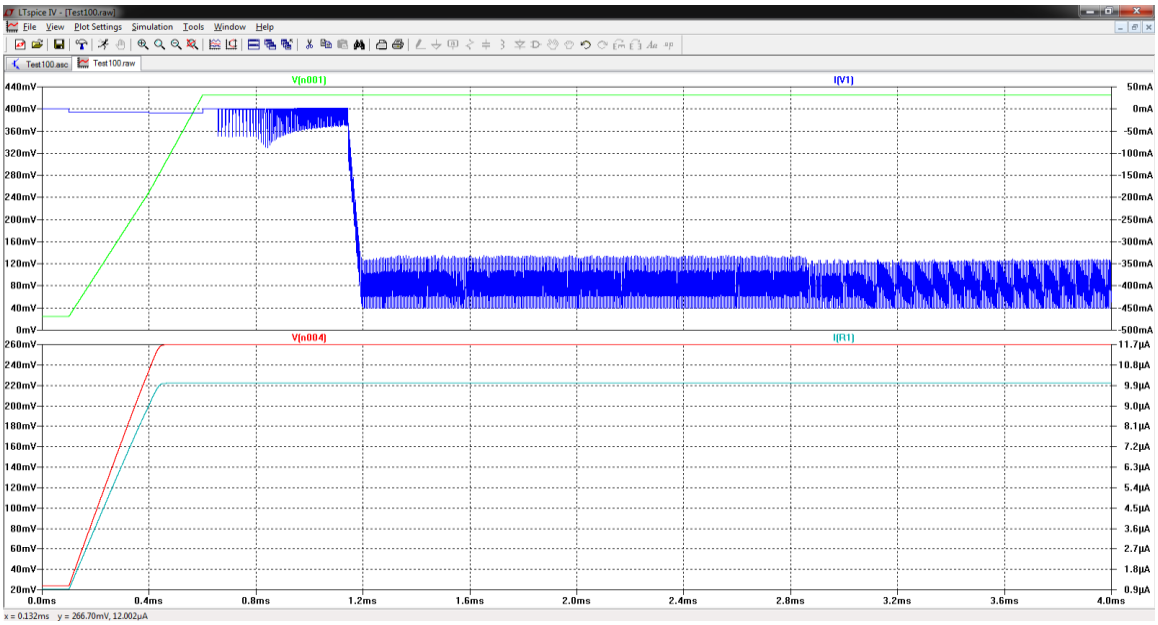


Figure 4.6: Input Voltage Supply and MPPC for the Improved Design Simulation.

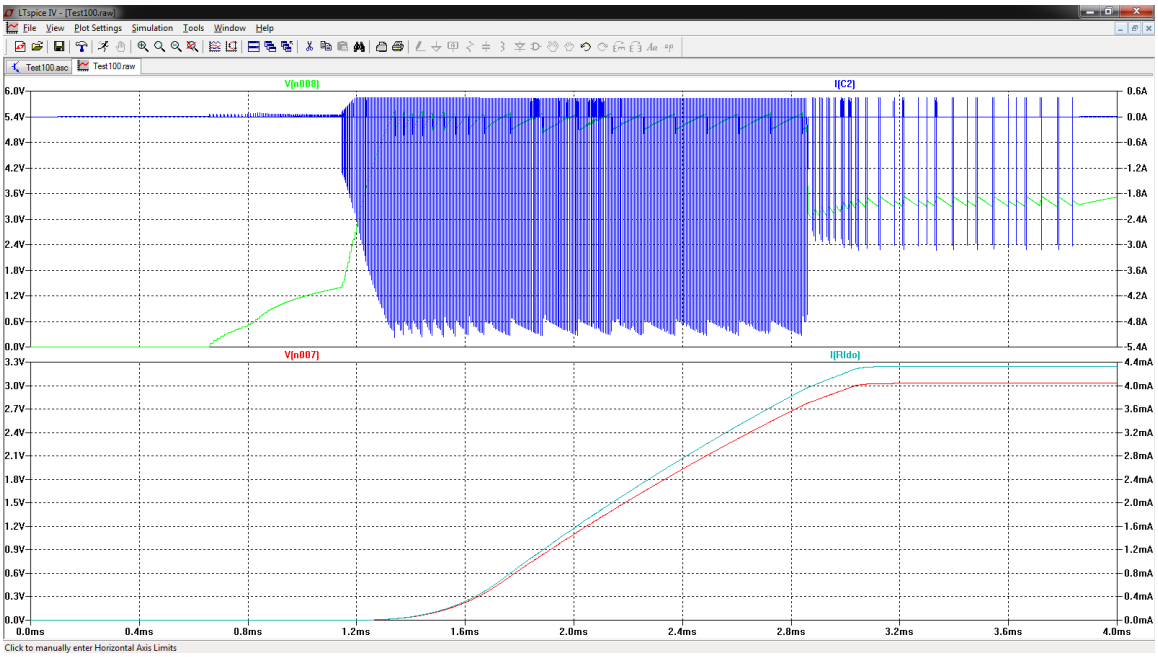


Figure 4.7: AUX and V_{LDO} output for the Improved Design Simulation.

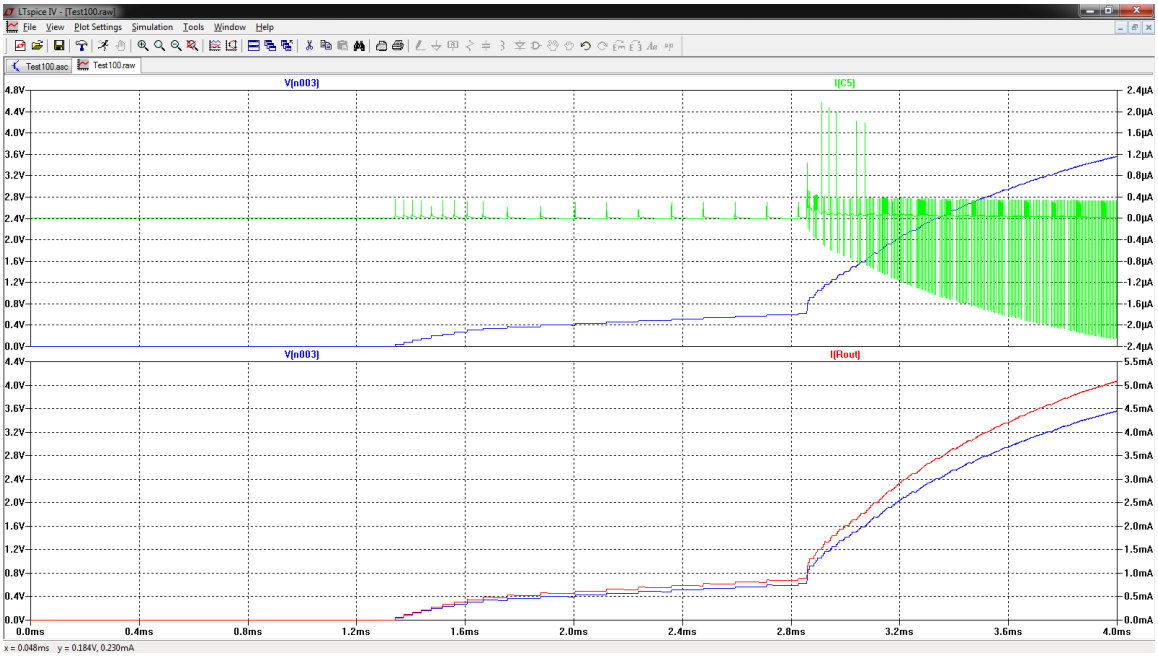


Figure 4.8: C_{OUT} and V_{OUT} output for the Improved Design Simulation.

For the bill of materials used for the initial and improved design schematics are included in Appendix III and Appendix IV.

4.1.3 Fabrication Phase Results

Based on the initial design schematic, the design was switched to board. The board schematic is fabricated and the SMD components are soldered on once the fabrication is completed. Figure 4.9 show the initial design schematic switched to board. This would be the circuit layout that will be printed on to the PCB.

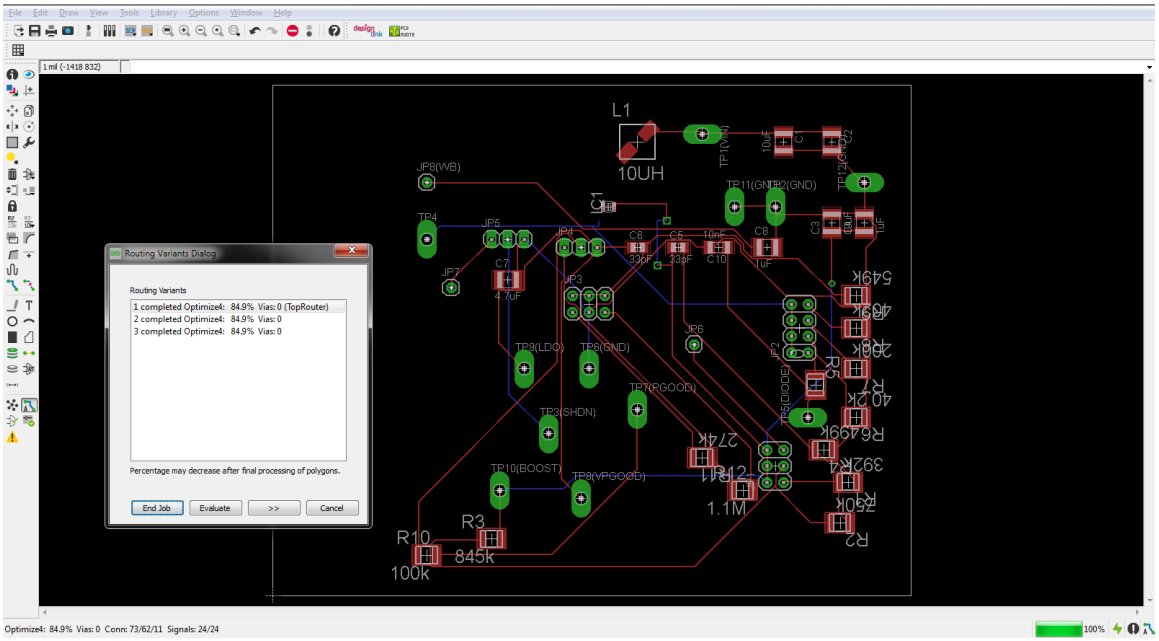


Figure 4.9: Initial Design Board Schematic.

It can be seen that, the connections from the IC is the cause of the problem as the minimum track clearance does not comply with the UTP fabrication requirement as mentioned in the previously. Hence the design was modified to enable to get the TopRouter to 100% routing. The figure below shows the modified design board schematic. The IC representation has been replaced with single pin heads and the TopRouter and the results showed 100%.

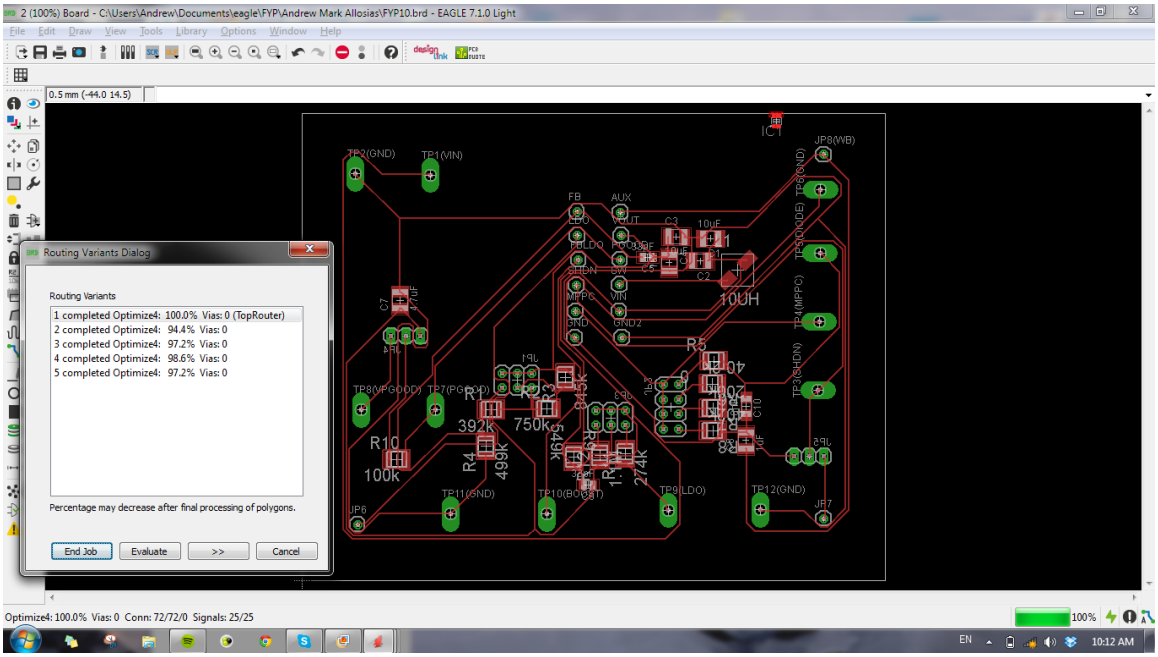


Figure 4.10: Improved Eagle Software Board Schematic.

4.2 Field Testing Results

Once the design has been fabricated on the PCB and the SMD are soldered. Field testing has been carried out on the prototype. The figure below shows the completed prototype. Regarding the design for the prototype, many spaces on the PCB can be saved if the double sided PCB is fabricated. Some of the components require double sidedness, such as the test turret and the pin head as well.

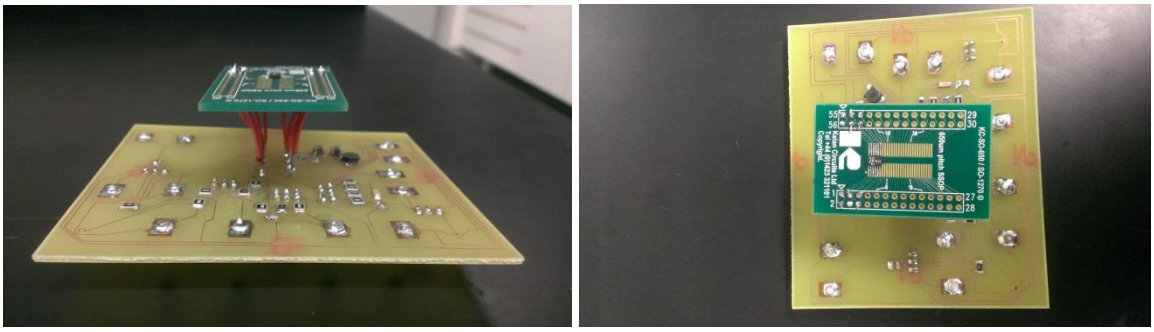


Figure 4.11: Top and Side View of Prototype.

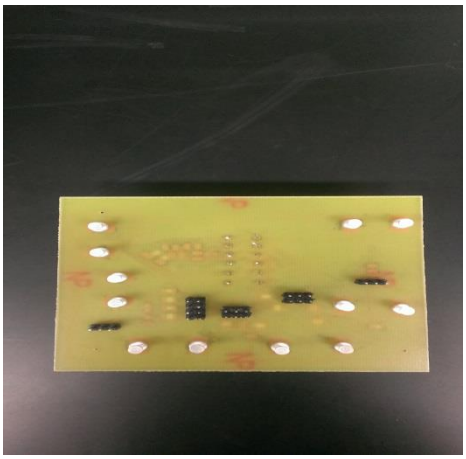


Figure 4.12: Back View of Prototype.

The prototype was tested under ideal condition where the input was fed up a DC power Supply and the output of both the regulated output and the unregulated output was measured using an oscilloscope under no load. A variable resistor was used on the voltage divider configuration to test the current that is able to obtain from the outputs. A total efficiency of 80% is able to achieve when a 500Ω and a 50Ω resistors are placed on the LDO regulated output and unregulated output respectively. The current that can be

achieved by the LDO regulated output is 6mA and 100mA at the unregulated output by setting the outputs at 3V and 5V. The prototype was fed with a supply of 2.5V at 0.25A. Note has to be taken that, the efficiency of the prototype under ideal situation increase with the input voltage supply. The calculations for the efficiency obtained are as follows;

$$Input\ power\ = P_{in}\ = (2.5V\ \times 0.25A) = 0.625W$$

$$Output\ Power(LDO) = P_{LDO} = (3V\ \times 6mA) = 0.018W$$

$$Output\ Power\ (Unregulated) = P_{OUT} = (5V \times 100mA) = 0.5W$$

$$Efficiency = \eta = \frac{P_{LDO} + P_{OUT}}{P_{in}} \times 100\% = \frac{0.018W + 0.5W}{0.625W} \times 100\%$$

$$Efficiency = \eta = 82.88\% \cong 80\%$$

The super capacitor is not soldered directly to the step-up circuit for the purpose of safety. The super capacitor rating of 10F, 2.5V was fully charged after 6-7 hours and was connected to a Zigbee module. The energy in the super capacitor is able to successfully source the Zigbee module until the energy in the super capacitor is depleted. The power is depleted much faster is there is constant transmission of information by the Zigbee module. The time the Zigbee module is source by the super capacitor until the super capacitor is fully depleted varies depending on the usage of the Zigbee module.

CHAPTER 5

CONCLUSION AND RECOMMENDATION

5.1 Conclusion

This projects presents a solution to the existing 7-Stage Cockroft-Walton Rectifier. Since the existing rectifiers output is generally in millivolt range and is unable to source most application and devices, the Step-up circuit with Charging and Storage function was the solution. The prototype of the step-up circuit with charging and storage function was able to provide and output voltage of 5V, 100mA with an input voltage as low as 400mV from the RF energy harvester. It was also able to provide variable output voltages by utilizing the voltage divider configuration in the prototype. The prototype is also able to source a Zigbee module successfully and tested under ideal condition, yields an efficiency of 80%. The promising field testing results validates the results obtained by simulation. For the purpose of safety, the charging and storage function of the circuit, which is a super capacitor is implemented using a Veraboard and is separated from the prototype. This is done to ensure that the step up circuit and charging circuit can be dis-attached for safety and for modification purpose if required. All objectives of the project are achieved upon completion of the working prototype and serves as a benchmark for further improvement in this field.

5.2 Recommendation

While the proposed circuit is able to be implemented into the system, there are other power harvesting IC which are able to harvest energy from a much lower energy to provide a usable output energy. LTC3109 is one of those IC. This is able to produce output energy of 5V with and input voltage as low as 20mV. This IC is suggested for progressive works under this project for its unique capability of stepping up output voltage.

It is also recommended that different types of RF energy harvesting topology are used together with this prototype. The prototype utilized a 7-Stage Cockroft-Walton topology provided promising results perhaps will do the same with other voltage multiplier topologies.

A circuit integrator is also recommended for future work. It will allow the prototype to select the highest output obtained from a variety of input sources to be stepped up, charged and stored. For example, having two 7-Stage Cockroft-Walton connected to the Prototype. Therefore, making it the output more reliable and constant

REFERENCE

[1] Technovelgy LLC, "What is RFID," Available: http://www.technovelgy.com/ct/technology-article.asp, Accessed on June. 19,2014.

[2] E.M. Cooney,*RFID.* Indiana, NY:Thomson and Delmar Learning,2006.

[3] S. Kim, "RF Energy Harvesting technique for Wirelessly Powered Devices," *IEEE MTT-S International Microwave Workshop Series*,1-2, Aug. 2011.

[4] T. B. Lim, N. M. Lee and B. K. Poh,"Feasibility study on Ambient RF Energy Harvesting for Wireless Sensor Network," *IEEE Microwave Workshop Series on RF and Wireless Technologies for Biomedical and Healthcare Applications*, 1-3, Dec.2013.

[5] S. S. B. Hong et al.,"Wifi energy harvester for low power RFID Application," *Progress In Electromagnetics Research C*, Vol. 40, 69–81, 2013.

[6] S. Scorcioni et al.,"An Intergrated RF Energy Harvester for UHF Wireless Powering Application," *IEEE Wireless Power Transfer (WPT)*, 92-95, May 2013.

[7] M. Dini et al.,"A Fully-Autonomous Integrated RF Energy Harvesting System for Wearable Application"*IEEE Microwave Conference (EuMC)*, 987-990, Oct. 2013.

[8] K. C. Wei, M. B. I. Reaz, M. S. Amin, J. Jalil and L. F. Rahman, "Design of a low Voltage Charge Pump Circuit for RFID tag", *IEEE 10th International Conference on Semiconductor Electronics (ICSE)*, pp:466 – 469, 19-21 Sept. 2012.

[9] J.F Dickson, "On-Chip high voltage generation in nMOS integrated circuits using an improved voltage multiplier technique", *IEEE Journal of Solid-State Circuits*, vol. 11, no.3, pp:374-378, Jun 1976

[10] W. Henru and C. Yuhua, "A charge pump circuit design based on a 0.35um BCD technology for high voltage driver applications", *Proceedings of the 9th International Conference on Solid-State and Integrated-Circuit Technology (ICSICT)*, pp.2035, 30-23 Oct. 2008.

[11] J. Shin; I.Y. Chung; Y. J. Park; Hong and S. Min, "A new charge pump without degradation in threshold voltage due to body effect [memory applications]", *IEEE Journal of Solid-State Circuits*, vol. 35, no. 8, pp:1227- 1230, Aug. 2000.

[12] L.D. Sheng, Z. Cheng, Z. Fan, Deng Min, "Embedded EEPROM Memory Achieving Lower Power New design of EEPROM memory for RFID tag IC", *Circuits and Devices Magazine, IEEE,* vol.22, no.6, pp:53-59, Nov.-Dec. 2006.

[13] C. Karnjanapiboon, Y. Rungruengphalanggul, and I. Booiyaroonate, "The Low Stress Voltage Balance Charging Circuit For Series Connected Batteries Based on Buck – Boost Topology", *Proceedings of the 2003 International Symposium on Circuits and Systems (ISCAS), IEEE,* vol.3, pp:284-287,2003.

[14] Yao C.Hsieh, Chin S.Moo and I S. Tsai, "Balance Charging Circuit For Charge Equalization", *IEEE Proceedings of the Power Conversion Conference*, vol.3, pp.1338-1141,2002.

[15] S. Kim, K.-S. No. and P. H. Chou, "Design and Performance Analysis of Supercapacitor Charging Circuits for Wireless Sensor Nodes", *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol.1,no.3, pp:391-402,2011.

[16] C. Park and P. Chou, "AmbiMax: Efficient, autonomous energy harvesting system for multiple-supply wireless sensor nodes," in *Proc. 3rd Annu. IEEE Commun. Soc. Conf. Sensor, Mesh, Ad Hoc Commun. Networks (SECON),* pp. 168–177, 2006.

[17] J. Timmer. (2007,Sept 5). Supercapacitor "battery" could lead to instant charging, long charge life. [Online]. Available: http://arstechnica.com/science/2007/09/supercapacitor-battery-could-lead-to-instant-charging-long-charge-life/

[18] I.Buchmann. (2014). Supercapacitor.[Online]. Available: http://batteryuniversity.com/learn/article/whats_the_role_of_the_supercapacitor

[19] V. Jaseem, (2013, April). 12v Battery Charger Circuit with Auto Cut off. [Online]. Available:http://www.circuitsgallery.com/2013/04/automatic-battery-charger-controller.html

[20] D. Mohankumar, (2008). Fast Charger with Auto Cut Off. [Online]. Available: http://www.electroschematics.com/5614/fast-charger-with-auto-cut-off/

[21] H. Yan, J. G. Macias Montero, A. Akhnoukh, L. C. N. de Vreede, and J. N. Burghartz, "An integration scheme for RF power harvesting," in *Proc. 8th Ann. Workshop Semiconductor Advances for Future Electonics and Sensors*, Veldhoven, the Netherlands, pp. 64–66, 2005.

[22] J. P. Curty, M. Declercq, C. Dehollain, and N. Joehl, "Rectifier building blocks," in *Design and Optimization of Passive UHF RFID Systems*, New York: Springer, ch. 2, pp. 6-8, 2010.

[23] E. W. T. Ngai, K. K. L. Moon, F. J. Riggins, and C. Y. Yi, "RFID research: An academic literature review (1995-2005) and future research directions," Int. J. Production Economics, vol. 112, pp. 510–520, 2008.

[24] M. Pi˜nuela, P. D. Mitcheson, and S. Lucyszyn, "Ambient RF energy harvesting in urban and semi-urban environments," *IEEE Trans. Microw*. Theory Tech., vol. 61, no. 7, pp. 2715–2726, Jul. 2013.

[25] Y. H. Suh and K. Chang, "A high-efficiency dual-frequency rectenna for 2.45- and 5.8-GHz wireless power transmission," *IEEE Trans. Microw. Theory Tech*., vol. 50, no. 7, pp. 1784–1789, Jul. 2002.

[26] H. Takhedmit, L. Cirio, B. Merabet, B. Allard, F. Costa, C. Vollaire, and O. Picon, "Efficient 2.45 GHz rectenna design including harmonic rejecting rectifier device," *IET Electron. Lett.*, vol. 46, no. 12, Jun. 2010.

[27] B. Merabet, H. Takhedmit, B. Allard, L. Cirio, F. Costa, O. Picon, and C. Vollaire, "Low-cost converter for harvesting of microwave electromagnetic energy," presented at *IEEE Energy Conversion Congress and Exposition, (ECCE 2009)*, San Jose, California, pp. 2592-2599, Sep. 20-24, 2009.

[28] H. Hong, X. Cai, X. Shi, and X. Zhu, "Demonstration of a highly efficient RF energy harvester for Wi-Fi signals," presented at *Int. Conf. on Microwave and Millimeter Wave Technology, (ICMMT 2012)*, Shenzhen, China, pp. 1-4, May 5-8, 2012.

[29] V. Marian, C. Menudier, M. Thevenot, C. Vollaire, and B. A. J. Verdier, "Efficient design of rectifying antennas for low power detection," in *IEEE Microwave Symposium Digest (MTT 2011)*, Baltimore, MD, pp. 1–4, 2011.

[30] S. Dearborn, "Develop affordable mixed-signal battery-charger designs," [Online]. Available: http://electronicdesign.com/energy/ develop-affordable-mixed-signal-battery-charger-designs, 2006.

[31] R. Akl, D. Tummala, and X. Li, "Indoor propagation modeling at 2.4GHz for IEEE 802.11 networks," in *6th IASTED Int. Multi-Conf. on Wireless and Optical Communications*, Banff, AB, 2006, pp. 510–515.

[32] Y. Kim and S. Lim, "A highly efficient rectenna using harmonic rejection capability," *J. Korean Inst. Electromagn. Eng. Sci*., vol. 11, no. 4, pp. 257–261, Dec. 2011.

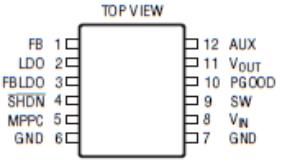
ABSOLUTE MAXIMUM RATINGS (Note 1)

SW Voltage
- DC ..... –0.3V to 6V
- Pulsed (<100ns) ..... –1V to 7V

Voltage, All Other Pins ..... –0.3V to 6V
Operating Junction Temperature Range (Note 2) ..... –40°C to 85°C
Maximum Junction Temperature (Note 4) ..... 125°C
Storage Temperature ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.)
- MS Package ..... 300°C

PIN CONFIGURATION

DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W, θ_{JC} = 3°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB



MS PACKAGE
12-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 130°C/W, θ_{JC} = 21°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3105EDD#PBF	LTC3105EDD#TRPBF	LFQC	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC3105EMS#PBF	LTC3105EMS#TRPBF	3105	12-Lead Plastic MSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

Appendix I: LTC3105 Datasheet

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{AUX} = V_{OUT} = 3.3V, V_{LDO} = 2.2V, V_{IN} = 0.6V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Step-Up Converter						
Input Operating Voltage		●	0.225		5	V
Input Start-Up Voltage	(Note 5) T_J = 0°C to 85°C (Note 5)	●		0.25	0.4 0.36	V V
Output Voltage Adjust Range		●	1.5		5.25	V
Feedback Voltage (FB Pin)		●	0.984	1.004	1.024	V
V_{OUT} I_Q in Operation	V_{FB} = 1.10V			24		µA
V_{OUT} I_Q in Shutdown	$\overline{SHDN}$ = 0V			10		µA
MPPC Pin Output Current	V_{MPPC} = 0.6V		9.72	10	10.28	µA
$\overline{SHDN}$ Input Logic High Voltage		●	1.1			V
$\overline{SHDN}$ Input Logic Low Voltage		●			0.3	V
N-Channel SW Pin Leakage Current	V_{IN} = V_{SW} = 5V, $V_{\overline{SHDN}}$ = 0V			1	10	µA
P-Channel SW Pin Leakage Current	V_{IN} = V_{SW} = 0V, V_{OUT} = V_{AUX} = 5.25V			1	10	µA
N-Channel On-Resistance: SW to GND				0.5		Ω
P-Channel On-Resistance: SW to V_{OUT}				0.5		Ω
Peak Current Limit	V_{FB} = 0.90V, V_{MPPC} = 0.4V (Note 3)		0.4	0.5		A
Valley Current Limit	V_{FB} = 0.90V, V_{MPPC} = 0.4V (Note 3)		0.275	0.35		A
PGOOD Threshold (% of Feedback Voltage)	V_{OUT} Falling		85	90	95	%
LDO Regulator						
LDO Output Adjust Range	External Feedback Network, V_{AUX} > V_{LDO}	●	1.4		5	V
LDO Output Voltage	V_{FBLDO} = 0V	●	2.148	2.2	2.236	V
Feedback Voltage (FBLDO Pin)	External Feedback Network	●	0.984	1.004	1.024	V
Load Regulation	I_{LDO} = 1mA to 6mA			0.40		%
Line Regulation	V_{AUX} = 2.5V to 5V			0.15		%
Dropout Voltage	I_{LDO} = 6mA, V_{OUT} = V_{AUX} = 2.2V			105		mV
LDO Current Limit	V_{LDO} 0.5V Below Regulation Voltage	●	6	12		mA
LDO Reverse-Blocking Leakage Current	V_{IN} = V_{AUX} = V_{OUT} = 0V, $V_{\overline{SHDN}}$ = 0V			1		µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3105 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3105E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 85°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: Current measurements are performed when the LTC3105 is not switching. The current limit values measured in operation will be somewhat higher due to the propagation delay of the comparators.

Note 4: This IC includes over temperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 5: The LTC3105 has been optimized for use with high impedance power sources such as photovoltaic cells and thermoelectric generators. The input start-up voltage is measured using an input voltage source with a series resistance of approximately 200mΩ and MPPC enabled. Use of the LTC3105 with lower resistance voltage sources or with MPPC disabled may result in a higher input start-up voltage.

Specification	XBee Series 2
Performance	
Indoor/Urban Range	up to 133 ft. (40 m)
Outdoor RF line-of-sight Range	up to 400 ft. (120 m)
Transmit Power Output (software selectable)	2mW (+3dBm)
RF Data Rate	250,000 bps
Serial Interface Data Rate (software selectable)	1200 - 230400 bps (non-standard baud rates also supported)
Receiver Sensitivity	-95 dBm (1% packet error rate)
Power Requirements	
Supply Voltage	2.8 – 3.4 V
Operating Current (Transmit)	40mA (@ 3.3 V)
Operating Current (Receive)	40mA (@ 3.3 V)
Power-down Current	< 1 uA @ 25°C
General	
Operating Frequency Band	ISM 2.4 GHz
Dimensions	0.960" x 1.087" (2.438cm x 2.761cm)
Operating Temperature	-40 to 85° C (industrial)
Antenna Options	Integrated Whip, Chip, RPSMA, or U.FL Connector
Networking & Security	
Supported Network Topologies	Point-to-point, Point-to-multipoint, Peer-to-peer & Mesh
Number of Channels (software selectable)	16 Direct Sequence Channels
Addressing Options	PAN ID and Addresses, Cluster IDs and Endpoints (optional)
Agency Approvals	
United States (FCC Part 15.247)	Pending
Industry Canada (IC)	Pending
Europe (CE)	Pending

Appendix II: XBee Series 2 OEM RF Module Datasheet

--- Bill of Materials ---

Ref.	Mfg.	Part No.	Description
C1	--	--	capacitor, 10µF
C2	--	--	capacitor, 1µF
C3	--	--	capacitor, 4.7µF
C4	--	--	capacitor, 10µF
C5	--	--	capacitor, 33pF
C6	--	--	capacitor, 1µF
L1	--	--	inductor, 10µH
R1	--	--	resistor, 40.2K
R2	--	--	resistor, 499K
R4	--	--	resistor, 100K
R9	--	--	resistor, 1.987M, 1%, 0.1W
Rload	--	--	resistor, 1.25K
Rload2	--	--	resistor, 350
U1	Linear Technology	LTC3105	integrated circuit

Appendix III: Bill of Materials for Initial Design Schematics on LT Spice Software.

--- Bill of Materials ---

Ref.	Mfg.	Part No.	Description
C1	--	--	capacitor, 10µF
C2	--	--	capacitor, 1µF
C3	--	--	capacitor, 4.7µF
C4	--	--	capacitor, 10µF
C5	--	--	capacitor, 33pF
C6	--	--	capacitor, 1µF
C7	--	--	capacitor, 10nF
C8	--	--	capacitor, 33pF
L1	--	--	inductor, 10µH
R1	--	--	resistor, 40.2K
R2	--	--	resistor, 499K
R3	--	--	resistor, 200K
R4	--	--	resistor, 100K
R5	--	--	resistor, 402K
R6	--	--	resistor, 0
R7	--	--	resistor, 549K
R8	--	--	resistor, 274K
R9	--	--	resistor, 1.987M, 1%, 0.1W
R10	--	--	resistor, 1.1M
Rldo	--	--	resistor, 250K
Rout	--	--	resistor, 250K
U1	Linear Technology	LTC3105	integrated circuit

Appendix IV: Bill of Materials for Improved Design Schematics on LT Spice Software.

NO	PIN	FUNCTION
1.	FB (Pin 1)	This pin is the Feedback Input for the step-up converter. If the resistors of the voltage divider for V_{OUT} is connected to this pin. An output between 1.5V to 5.25V can be adjusted.
2.	LDO (Pin 2)	This pin is the Low Dropout (LDO) Regulator Output. Normally a capacitor valued at 4.7µF or greater is connected between the LDO and Ground (GND) pin.
3.	FBLDO (Pin 3)	FBLDO (Pin 3): This pin is the LDO Feedback Input. If the resistors of the voltage divider for LDO is connected to this pin. An output between 1.5V to 3.1V can be adjusted. Otherwise connecting the FBLDO pin to GND will configure the output voltage from the LDO to be set at 2.2V which is nominal.
4.	SHDN (Pin 4)	SHDN (Pin 4): This pin is the Logic Control Shutdown Input. The converter is normally has a 2MΩ pull up resistor when SHDN is in open. For the converter to enter normal operation, the SHDN pin should be driven and floated.
5.	MPPC (Pin 5)	This pin is the Maximum Power Point Control Input Set Point. The resistors of the voltage divider are connected from this pin to the ground to program the activation point for the MPPC loop. MPPC can be directly connected to ground to disable MPPC function.
6.	GND (Pin 6, 7)	This is the Ground pin for the converter. The GND connections should be soldered to the Printed Circuit Boards (PCB) ground using the lowest impedance path possible.
7.	VIN (Pin 8)	This is the Input Supply pin for the IC. A decoupling capacitor is still connected between the pin and ground to lessen the voltage fluctuations obtained from the 7-stage Cockroft-Walton rectifier.

8.	SW (Pin 9)	This is the Switch Pin for the IC. An inductor is connected between the pin and VIN. Safety should be taken during the designing of the PCB to make sure the PCB trace length is relatively short to reduce Electromagnetic Interference.
9.	PGOOD (Pin 10)	This is the Power Good Indicator for the converter and is an open drain output. The pull-down is disabled when the VOUT has achieved voltage defined by the feedback divider on the FB pin, during Shutdown or Start-Up mode.
10.	VOUT (Pin 11)	This is the Converter Step-Up Output. A 10µF or larger capacitor is connected between this pin to the GND to function as an output filter capacitor.
11.	AUX (Pin 12)	This is the Auxiliary Voltage for the converter. This pin is used by the start-up circuitry to generate a voltage rail to power the internal circuitry until the main output reaches regulation. AUX pin is also internally connected together to VOUT once VOUT exceeds VAUX

APPENDIX V: LTC3105 Pin Function.