BACKEND DESIGN OF WIDEBAND LOW NOISE AMPLIFIER USING 130 NM RF CMOS TECHNOLOGY

by

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ABSTRACT

Low Noise Amplifier (LNA) is widely applied nowadays for amplify very weak signals usually captured by antenna with reduced noise due to the gain of the LNA. Thus the main concern in this paper is in designing an LNA for ultra-wideband which cover frequency ranging from 3.1 GHz to 10.6 GHz. The design of the circuit is implemented using the 130 nm complementary metal-oxide semiconductor (CMOS) technology. Comparative studies have been done between inductive degeneration and common gate configuration with special consideration in terms of the corresponding noise figure. The backend designs of LNA are more likely focusing on the post layout simulation based in the three steps, i.e. design rule check (drc), layout –vs-schematic (lvs) and parasitic extraction (pex). The parameters attained will include s-parameter, linearity, noise and power consumption. The results show that careful consideration of the arrangement in the layout could have significant effects in total for the circuit. Further modification is suggested such as by using other different type of elements and arrangement for further improvement on the parasitic extraction and completion of project until fabrication so comparative studies between simulation and the fabricated can be executed.

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CHAPTER 1
INTRODUCTION

1.1 Project Background

In this modernized era, the development of wireless communication technology is in a rapid state due to overwhelming demand for high speed data communication. Thus, in order to fulfill this increasing demand in bandwidth technology for commercial applications called ultra-wide band (UWB) is proposed since 2002. It has been adopted from the used for radar, sensing and military communication application for over the past 20 years. One of the salient properties of UWB is the ability to penetrate through buildings due to very high frequency. In addition to that, UWB also applied in aviation section as it is being used to sense obstacles and thus lead to the collision avoidance system. In February 2002, the Federal Communication Commission (FCC) issued a ruling that the UWB should be used for data communication as well as for radar and safety applications.

There are other wireless systems that can cause interference to the UWB systems. One of them is the Global Positioning System (GPS) with its "sub-noise floor" power density signal. Thus, this leads to an approval from the FCC to a low frequency bound for UWB commercial to be at 3.1 GHz. This requirement can be observed from the spectral mask shown in Figure 1. Note that, at 1.6 GHz, PSD is less than -85 dBm/MHz. However, mobile phone providers and airline industries also urged the FCC to prohibit the use of UWB technology below 6 GHz.

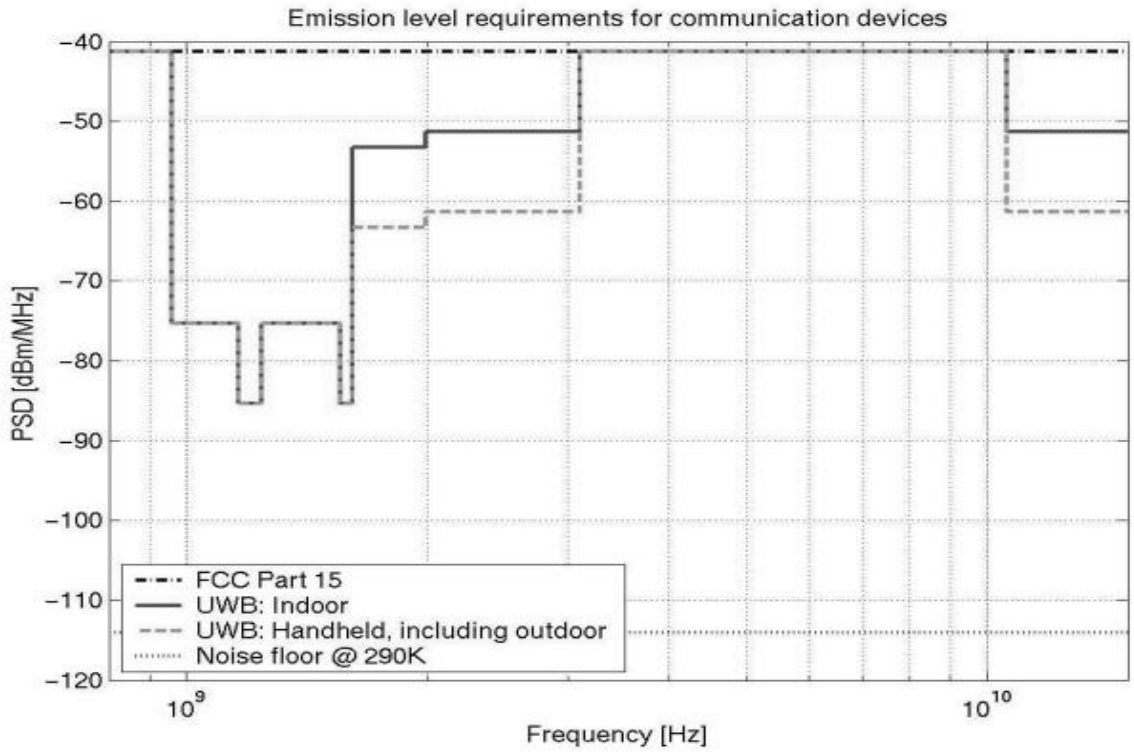

Figure 1: UWB Spectrum Mask

As a result, a PSD in the -40 dBm/MHz represents a compromise to other existing technologies. FCC also defines that the -10 dB bandwidths of a UWB signal to be greater than 25 % of the center frequency or greater than 1.5 GHz. Furthermore, with the recent adopted proposal, new regulation with regard to the use of UWB without license for handheld wireless communication is defined to be between 3.1 GHz and 10.6 GHz.

Therefore, a higher communication speed can be achieved using the UWB systems so that the data can be transmitted through radio channel faster than the traditional narrowband transceivers which only provide a short range and very low power connection with much more bandwidth. Recently, Bluetooth 3.0 even adopted UWB architecture to increase the data rate.

In implementing wireless UWB receiver, low noise amplifier (LNA) is the most critical block in providing a considerable gain and minimizing the noise. As the first block that receives the signal from the antenna to amplify the received signal to within the bandwidth of interest. Thus, the LNA is a very significant as its performance can affect the sensitivity and noise parameters of the overall receiver. It is a very challenging to design RF front/back-end receiver due to wideband requirements needed. Thus, it necessitates in obtaining wideband input matching to a

50-Ω antenna, good linearity and low power consumption. Furthermore, gain flatness over the entire frequency range of interest is desirable since variations in the flatness of the amplifier's gain can cause distortion of signals. Other than that, loads of inductors are available and analyses to be used in acquiring the most suitable technique to be applied in the circuit.

1.2 Problem Statement

Wideband requirement poses a wideband impedance matching as opposed to LC tuning for narrowband LNA. Hence, the input impedance needs to be matched to the characteristics impedance of the antenna, typically at 50-Ω. To ensure wideband matching from 3.1 GHz to 10.6 GHz, Bevaliacqua and Niknejad proposed 3rd order Chebyshev filter at the input on inductive degeneration LNA. However, this proposal results in the use of 5 inductors, causing for the form factor to increase. To reduce it, center-tap-inductor (CTI) will be used to alleviate the area consumed in the design.

Noise for wideband system has always been greater than the narrowband system due to wide coverage of the frequency range. To alleviate the noise over a wide frequency range, the narrowband inductive degeneration LNA that is widely utilized in narrowband can be adopted. There is one report by Shekhar *et.al* who proposed the use of common gate topology to design UWB LNA exhibiting low noise figure. Therefore there is a need to investigate the choice of LNA topology in relation noise characteristics for wideband LNA.

1.3 Scope of Study and Objective

- To compare noise parameter between inductive degeneration and common gate configuration.
- To implement wideband LNA that exhibits bandwidth of 7.5 GHz with operating frequency of 3.1 to 10.6 GHz.
- To optimize various types of inductors to be used in the design.

In general the scope of this project is to design a complete layout design by making study comparison on types of circuit configuration to be used in the layout design.

CHAPTER 2
LITERATURE REVIEW

The major challenges of a wideband LNA design can be summarized in terms of S-parameters and NF as follows:

1. Forward gain degradation (decreases in S_{21}) which necessitates some techniques to compensate the gain roll-off.

2. Frequency variations of S_{11} and S_{22}.

3. Increase in $|S_{12}|$ which will reduce the forward gain and increase the possibility of oscillation and instability.

4. NF degradation at high frequencies.

To address these challenges in the design of a wideband LNA, several topologies and circuit techniques have been proposed in the literature. This project will discuss the popular wideband architectures and briefly discuss their advantages and disadvantages. Other than that this project will reviews the fundamental of noise figure, stability and linearity involved. Moreover, the study of different behavior topologies would determine the overall performance of wideband LNA system.

In February 2002, ultra-wideband (UWB) could be used for data communication technology as it can transmit high data rate over a wide spectrum of frequency range with very low power and can be commercialized. The wideband LNA servers as an important building block for the UWB receiver as depicted in Figure 2. Hence, the design of a LNA is the most challenging part because it should provide constant gain for the input signal through the entire bandwidth, which is 3.1 GHz to 10.6 GHz for UWB receiver. In this work, it is difficult to implement a good wideband input matching and wideband output response in order to keep the overall receiver noise figure as low as possible. In most applications, definitely technology scaling helps improve frequency but degrade performance in term of large noise, low output impedance, poor output swing and dynamic range. Therefore, it is desirable to obtain flat response over ultra-wide frequency range, good input matching to a 50-Ω antenna, good linearity, and low power consumption. In this chapter, the design of a

low noise amplifier (LNA) using a 0.13-mm CMOS technology for the receiver path of a UWB system is discussed.

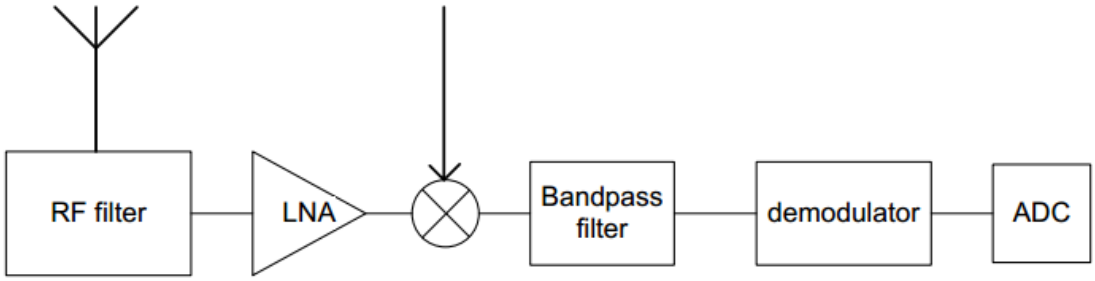

Figure 2: The Block Diagram of a simplified RF receiver

For the case of studying the effects of common gate configuration and inductive source degeneration, they are two differently configured circuits with different properties.

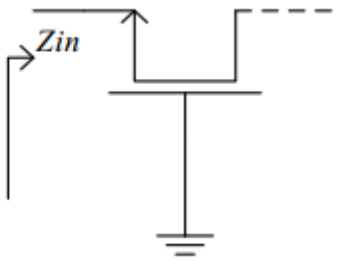

Figure 3: The Schematic of Common Gate Configuration

A common gate configuration circuit will gives a reasonable NF value (Idora, 2014). With an addition, by doing a proper biasing and sizing of the LNA will result in equivalent impedance matching to the resistance which is the R, 50-Ω (Adhyaru, 2007). Other than that, the common gate configuration has an advantage towards wideband LNA input matching design as it is independently on its own regardless of the frequency but only up to a certain frequency range. (Idora, 2014)

The major setback for the common gate configuration is that it has a large noise factor, even though the calculated noise figure is in the tolerable value but due to external noise sources such as gate induced noise and substrate noise. The performance will degrade with due time. (Idora, 2014)

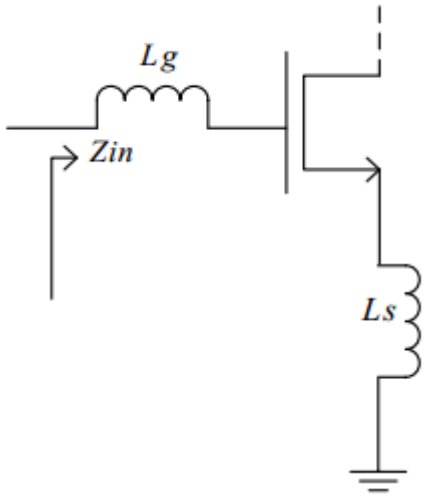

Figure 4: Schematic of Inductive Source Degeneration Circuit

As shown in figure 4, this is a schematic for inductive source degeneration circuit. It is widely adopted in the industry as this topology has a significant feature which to give fixed input impedance without degrading the noise performance of the amplifier (Idora, 2014). This is due to input impedance of the topology that is directly proportional to the inductance value. Thus resulting in the noise is not affected by the value of the resistive term as a pure reactance is noiseless, (Idora, 2014). Furthermore, the inductive source degeneration has very good input matching and can be achieved by varying the value of the inductor $L_s and\ L_g$

Table 1: Comparison between Common Gate Configuration and Inductive Source Degeneration

Common Gate Configuration	Criteria	Inductive Source Degeneration
- Gives reasonable Noise Figure - Easy impedance matching with proper biasing - Independently regardless of the frequency	Advantages	- Has fixed input impedance without degrading the noise performance - Noise not affected by value of the resistive term - Very good input matching
- Has a large noise factor - Performance degraded with time	Disadvantages	- Requires alteration of few inductors for input matching

In addition, as per layout design, multiple types of inductors can be chosen to be used the circuit. But one stands out among the rest is the center-tapped inductors. The main reason for this is that, by using center-tapped inductors they lead to saving in chip area due to the mutual magnetic coupling, (Niknejad, 2000). Furthermore, by applying center-tapped inductors, they will lead to higher *Q* values due to the savings of area and lastly, the parasitic coupling will not occur in them, (Niknejad, 2000).Below shows an example of center tapped inductor extracted from Niknejad's research paper.

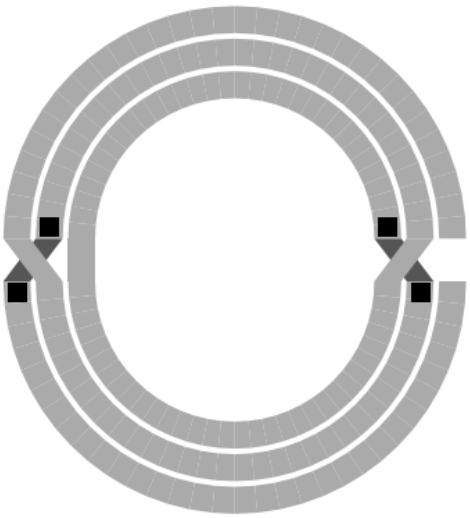

Figure 5: Example of Spiral Center Tapped Inductor with R = 125 µm and metal width W = 14.5 µm

CHAPTER 3
METHODOLOGY

3.1 Introduction

This chapter presents on the proposed wideband low noise amplifier (LNA) according to the result of the comparison done between two common topology used in wideband LNA. The LNA is identified as the critical block because it amplifies the received signal from the antenna to a desirable range of frequency. The main goal for this project is to design a most preferable and compact RF circuit using the fabrication software which is cadence.

3.2 Design flow chart

The design flow shown in Figure 5 represents the design procedure of Ultra-Wideband (UWB) low-noise amplifier (LNA). This flowchart is showing the process in detail to achieve the main goal of this project. Firstly, the comparative studies between common gate configuration and inductive source degeneration circuit have been done. Thus the appropriate method in designing the low-noise amplifier has been chosen that is the inductive source degeneration.

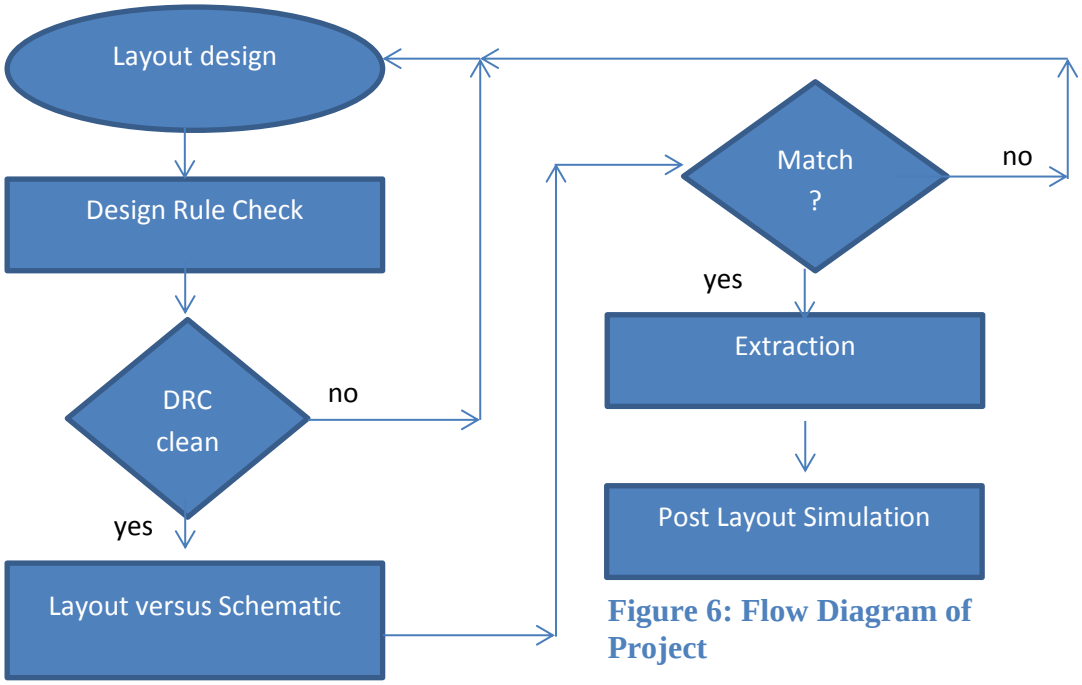

Figure 6: Flow Diagram of Project

Layout Design

Layout design is the process of where the user design the layout for the circuit according to the specification or the plan that has been reviewed

Design Rule Check (DRC)

Design Rule Check is the process of in which it determines whether the physical layout of microchip proposed satisfies a series of recommended parameters called Design Rules. The design rules are set or provided by semiconductor manufacturers to enable the designer to verify the correctness of their design circuit.

Layout versus Schematic

Layout versus Schematic is the process in which the program determines the particular integrated circuit layout is the same as the original schematic or circuit diagram of the design.

Extraction

Extraction to be exact is the parasitic extraction in which it is a process of calculation of the parasitic effects in both the designed devices and the required wiring interconnects of an electronic circuit.

Post Layout Simulation

Post Layout Simulation is the process where to get an idea of how the designed layout would work out. Other than that, the procedure is identical to that for simulating from the schematic view.

3.3 Layout Design from the Schematic

From the given schematic design, we have to extract the data to replicate the same component but in the layout design using Cadence. From the component selection, we have to alter few criteria to achieve the specified specification from the proposed circuit. The criteria to be altered are most likely to be the width size, core size, and number of coils to achieve to the respected configuration. In addition to that, there are also the specifications of resistor and capacitors to be used. Furthermore, there are also transistors specification that needed to be fulfilled and following the

industrial requirements. Especially the width and length for the transistors to match up for the following the circuit configurations

Table 2: List of Transistors and Sizing

Transistors	Sizing (µm)
M_1	100
M_2	40
M_3	200
M_4	200

Table 3: List of Elements with their specifications

Parameters	Values
L_1	2.31 nH
C_1	400 fF
R_1	8 Ω
L_2	1.455 nH
C_2	635 fF
R_2	5 Ω
L_g	1.6 nH
C_{gs1}	400 fF
R_g	272 Ω
C_p	5.53 fF
L_3	40 nH
R_3	138 Ω
L_4	18 nH
R_4	62.21 Ω
L	3.9 nH
R	13.5 Ω
C	68 pF

CHAPTER 4
RESULTS AND DISCUSSION

4.1 Introduction

The results of the project comprises of two parts namely:

- Schematic Design
- Layout Design

Schematic Design

From the previous research and study, we have come up with a suitable circuit to be used which is as follow

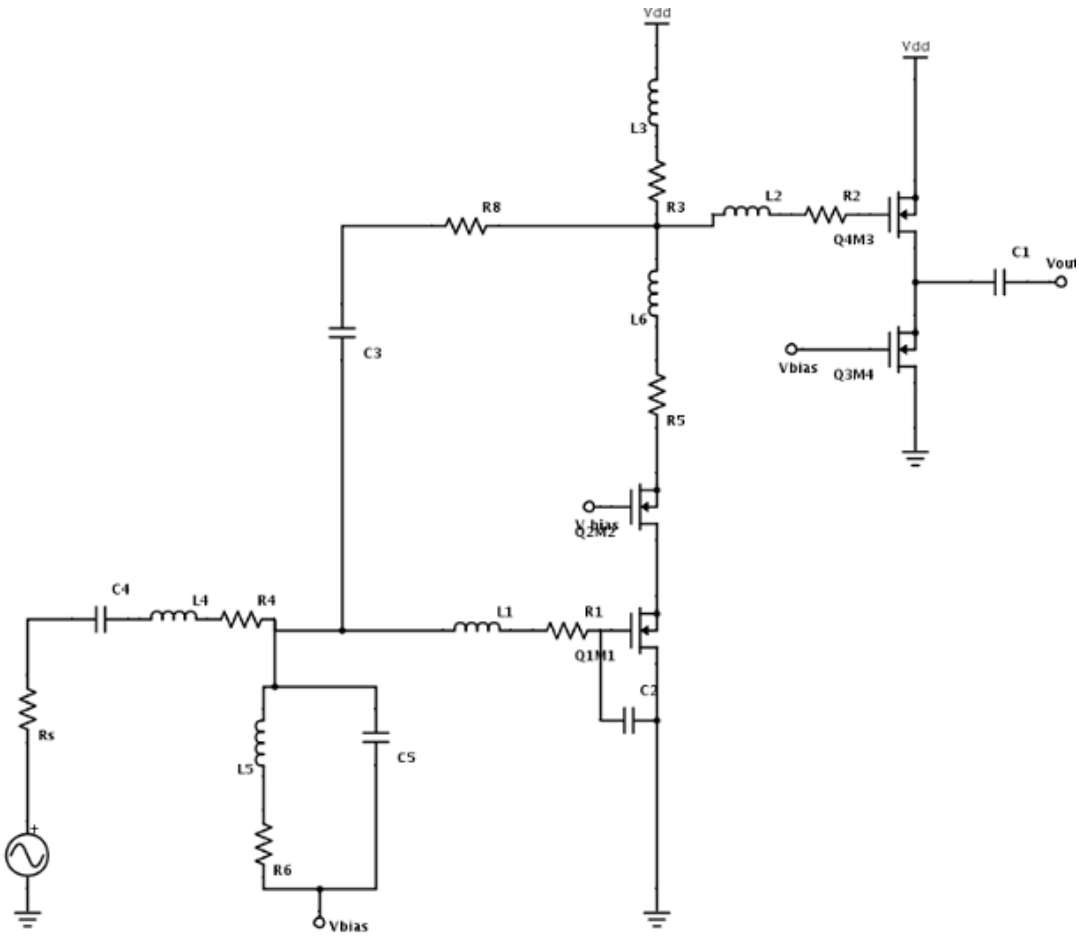

Figure 7: Circuit Design for Project

From the schematic, we can see that there are 5 inductors to be drawn and connected in the layout. And there are 4 in total for the number of MOSFET which their sizes will effects on the outcome of the simulation.

Table 4: Actual Sizing for transistors in the layout design

Transistors	Sizing (µm)
M_1	100
M_2	40
M_3	160
M_4	160

From the given table, some of the sizing of the transistors is not similar to the preplanned in the schematic design as there is a maximum sizing for the transistors which have already been set by the industry. These settings are set so that they will not differ from other designs in the other industries during the testing time.

CHAPTER 5
CONCLUSION

Cadence software requires a lot of understanding to be used to come up with the required proposed design, especially regarding the arrangements of components and the path to be constructed. Other than that, the Cadence software is used for the confirmation of the layout design whether it fulfils the industrial requirement besides being use for the simulation part only. Even though the project is yet to achieve the final stage of post layout simulation and the fabrication of the circuit for testing, a lot of few steps are in needed to improve the layout of the circuit design.

Recommendation for future work:

- Completion of project - Finish the project until the fabrication of the project so the comparison between the simulation of the circuit and the actual fabricated circuit can be executed.
- Modification of Model – Further modification by using different types of inductors and also the different arrangements of equipment in the circuit could lead to improvement of the circuit design.

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