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DEVELOPMENT OF FAST SWITCHING AND DATA ACQUISITION CIRCUIT FOR IN HOUSE ECT SYSTEM

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DEVELOPMENT OF FAST SWITCHING AND DATA ACQUISITION CIRCUIT FOR IN HOUSE ECT SYSTEM

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Abstract

Electrical Capacitance tomography, or ECT, is the technology to generate visual representation of flow's different phases using the distribution of electrical permittivity [1].

In this project, an enhanced design of data collection and switching circuit which aims to improve the in-house ECT system, especially to implement an automatic switching circuit, and increase the data collection rates.

The proposed design uses short analogue signals routes by implementing a local ADC module for every data collection circuit. Furthermore, this design has adheres to universal communication standards and can be integrated in most of nowadays technologies. Furthermore, it implements an on-board reprogrammable microcontroller. Therefore, the design enjoys high portability and can be re-configured to meet various ECT system requirements for different applications with minimum hardware adjustments.

The main focus of this project is to improve the performance of the in-house ECT system by improving the data collection circuitry to incorporate an automatic switching module that is able to switch operation of the electrode modules between four modes namely, Excitation, Detection, floating and grounding. As well as, increasing the data collection data rate by enabling parallel detection operations.

A Printed circuit board have been designed by KiCad software, and has been produced and validated. In addition, the programming logic has been developed in C language, and it has been implemented in a Microchip PIC 8bits microcontroller using Mplab IDE and XC8 C compiler.

Acknowledgement

I would like to take this opportunity to express my gratitude and appreciation towards anyone or any entity that assisted me in completing this project. I would like to specifically thank AP Ir Dr Idris Ismail, who was my supervisor for this project and did not save any effort to provide me all the advice and guidance that I needed.

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CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

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Mohammed Nasser Hussein Al-ademi

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Chapter1: Introduction

1.1 Background study

ECT technology is a non-intrusive and non-destructive imaging technique that seeks to visually present the distribution of different materials flows inside enclosed vessels or pipes, by sensing the electric permittivity contrast of the flowing materials [2] .

A typical ECT system consists of set of electrode ,usually between 8 to 16, symmetrically mounted inside or outside of the examined vessel, as shown in Figure 1 [3]. One scanning cycle is initiated by applying an excitation sine wave to one electrode while measuring the generated voltage on the rest of the electrodes. In order to construct one frame of image, a number of scanning signals equals to the number of electrodes is required, in each cycle the excitation signal is applied to different electrode with measurements are taken from other electrodes. In any giving scanning cycle the electrode to which the excitation signal is applied to is called excitation electrode, while the rest of the electrodes are referred to as detection electrodes.

A typical ECT system has a main shortcomings slow scanning rates, which hinders the ability for real time visual presentations. This project presents an improved ECT data collection circuitry which enables parallel scanning operation, which theoretically should decrease the time required to scan an entire ECT frame to the time required to scan one electrode.

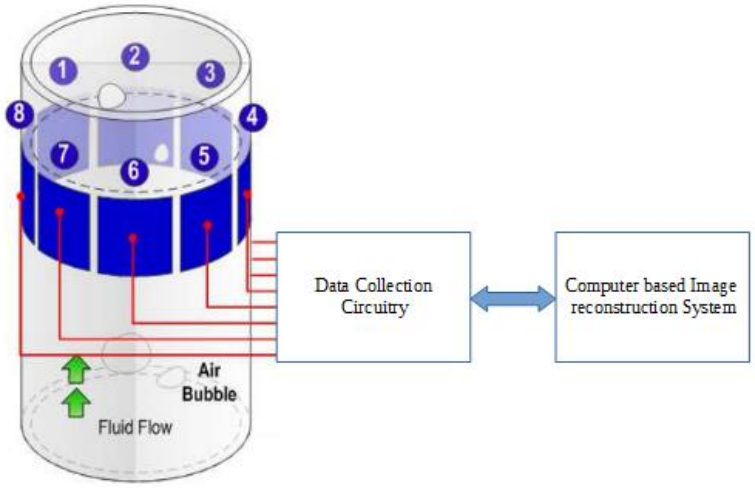


Figure 1: Illustration of ECT System

1.2 Problem Statement

The in house ECT module, designed by Mr.Abang Nizammudin as a final year project, suffers from two main Problems,

- The switching module of the system performs only one reading cycle automatically, and requires human interaction to commence the next reading cycle.
- However to achieve real time visualization, the scanning rate of entire frame should be greater than 20 frames per second.

1.3 Objectives and Scope of Study

The main objective of this project is to produce a modified design of data collection circuitry which would manage the operation of two electrodes as shown in Figure 2. The circuitry is expected to perform the following functionalities:

- Switching operation mode of its associated electrodes into one of four modes which are Excitation, Detection, Grounding and Floating,
- Measuring Capacitance of an electrode by utilizing Capacitance to Voltage Converter circuitry.
- Converting the obtained analogy value to a digital value using an Analogue to Digital Converter, and calculate the actual measured capacitance using a local Microcontroller, and
- Sending the measured capacitance using proper communication protocol to a central computer based image reconstruction system.

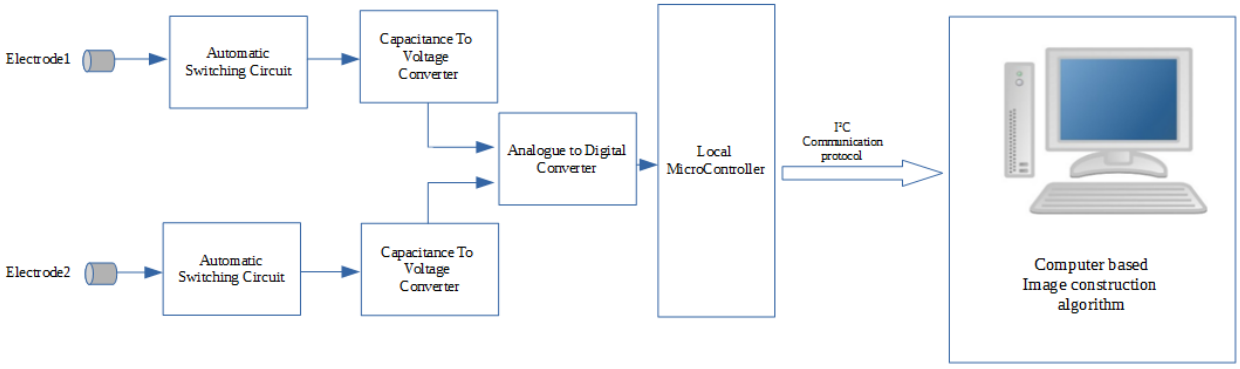


Figure 2: Simplified View of Data Collection Circuitry

Chapter 2: Literature review

The development of ECT Technologies has been involving since the 1980s with early modules of 8 electrodes modules [4]. More recent developments are heading in two different directions. On one hand, there is new ECT systems which are able to construct 3 dimensional visualisations of the measured flow phases such as the system reported by Winkler [5] ,on the other hand different systems combine more than one tomography technologies such as ECT and ERT , or ECT and ultrasonic tomography. A good Example of such systems is described by Hoyle [6].

The main drive behind the rapid development of ECT systems, is the Non-intrusive and Non-invasive nature of the technique which, makes it advantageous over many other tomography techniques. Furthermore, ECT requires no direct contact between the sensor and the flow being measured, which greatly simplifies maintenance process. Furthermore, ECT imposes no change nor any disturbance to the flow being explored[7]. Unlike Electrical Resistance Tomography, ECT does not require an electrically conductive medium to operate which makes it a perfect candidate in hydrocarbon industries such as oil and gas industries.

Development of in house system is very crucial for future research and development in UTP. In this chapter, the reader is introduced to the main components in a typical ECT system, with brief description of each module and common technologies used in designing the component.

2.1 ECT sensor module

Figure 3 illustrates across sectional illustration of a typical ECT sensor. The sensor mainly consists of 4 distinctive parts. Outer most part is a metallic shield which is connected to ground potential to cancel the effect of stray capacitances between the measuring electrodes and to provide a protection layer against outer environment disturbances that may affect the measurement process. The next layer is an electrically isolating layer which isolates the measuring electrodes from the outer screen and from each other.

Measuring electrodes come below the isolating layer, typically an ECT sensor will have 8, 12, or 16 measuring electrodes mounted outside the wall of the vessel. The sensor shown in *Figure 3* have 12 electrodes. The initial step to capture one cycle of data is to excite electrode 1 with excitation signal and measure the capacitance measurement from the electrodes 2 to 12. After that electrode 1 is put to an idle state and electrode 2 is excited. This time capacitance measurements are taken from the electrodes 3 to 12. This cycle is repeated until electrode 11 is excited where only one capacitance measurement is obtained from electrode 12.[8]

In a 12 electrode sensor module the total number of capacitance measurements is 66. In

General the numbers of measurements corresponds to the number of electrodes by the formula

.

$$\frac{N \times (N-1)}{2} \qquad \text{Equation 1}$$

Where N is the number of electrodes

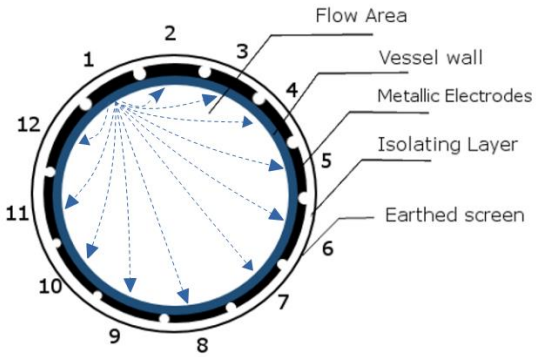


Figure 3 : ECT Sensor Module

2.2 Signal conditioning module

Signal conditioning module is responsible for capturing the capacitance measuring coming from the sensor module. Furthermore, the signal conditioning module is where the first stage of filtration and amplification is applied to the captured signal.

In order to achieve best performance possible, there are two main challenges the circuitry of this module is expected to fully overcome. Namely stray capacitance and standalone capacitance.

2.2.1 Stray Capacitance

Stray capacitances are introduced by wires, environment or electronic parts simply due to their approximation to each other. Stray capacitance forms an unavoidable and undesirable source of noise. Furthermore, due to its variety of sources, stray capacitance tend to have random values which are very hard to predict.

Since in ECT applications the capacitance to be measured is usually very small, and stray capacitances could add up to reach tens of pF, it is very difficult to detect the desirable capacitance mixed with random and large values of stray capacitances. Therefore, it is very crucial to design a capacitance to voltage conversion circuit that eliminates the effects of stray capacitances before any performing any measurement.

2.2.2 Standalone capacitances

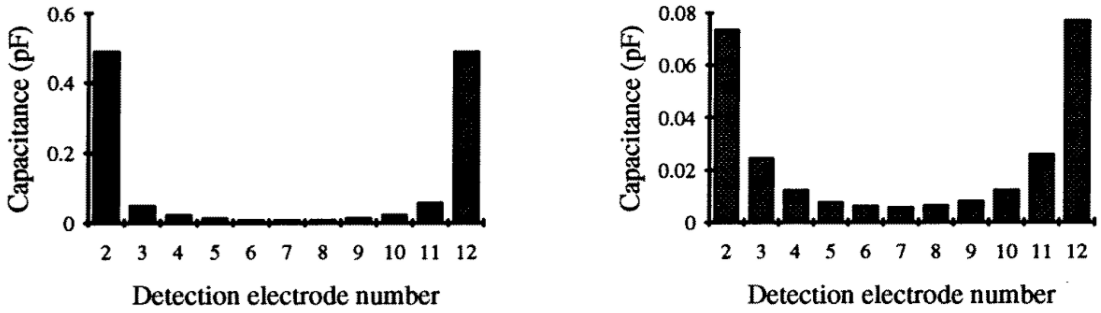


Figure 4: Capacitance measurements for a 12-electrode ECT sensor [4]

Figure 4 demonstrates typical capacitance measurements of 12 electrode sensor. The graph in the left is measurements taken with the pipe is filled with low permittivity material such as air. On the right the same measurements were taken when the same pipe was filled with a material which has relatively higher permittivity permittivity.[9]

The figure illustrate the wide range of capacitance values present in typical one cycle ECT system where values of low might range between 6.7 pF and 0.489 pF. Furthermore, the difference of measurement between low and high permittivity mediums very small (in the range of 76.9 and 5.47 fF.[9]

The wide range of measured capacitance values requires big bandwidth signal processing. Furthermore, for the very small difference in measurements in different mediums to be detected the quantization process of the analogue to digital conversion must be of a very high resolution or a variable amplification methods should be adopted. [9]

2.3 Capacitance to Voltage Conversion circuits

The Capacitance to Voltage Conversion circuit is responsible for producing a voltage signal that is proportional to the detected capacitance value, as well as, deleting the effects of stray capacitance. For this project two circuit configurations were considered, Charge/discharge circuits, and alternating voltage excitation circuits.

2.3.1 Differential Charge / discharge capacitance measurements circuits

The Charge Discharge circuits employs a square excitation wave to charge the sensors blades and measure the resulting capacitance before discharging the sensor preparing for the next reading [10]

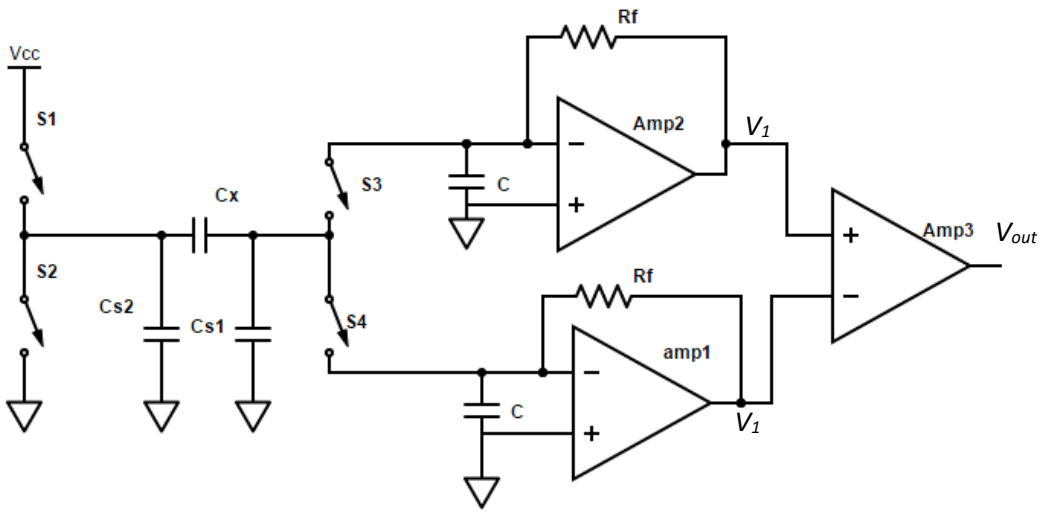


Figure 5: Charge / discharge capacitance Measurement circuit

Figure 5 shows a typical configuration of Charge/Discharge circuits. The stray capacitance is presented as C_{s1} and C_{s2}, C_x stands for the unknown capacitance. On the right of the figure is the excitation signal produced by rapid operation of the switches S_1 and S_2.

Each measurement cycle composes of two stages; charging and discharging. In charging stage, switches 1 and 4 are closed to form path for the current to flow from V_C through the unknown capacitance C_x to operational amplifier 1. In turn operational amplifier 1 converts this current to voltage proportional to the value of Cx, according to the equation,

$$V_1 = -F\ Vc\ C_x\ R_f - E_1 \qquad \text{Equation 2}$$

Where F is the switching frequency

Cx is the unknown capacitance

R_F is the value of the feedback resistance

E operational amplifier offset

In the discharging stage switch 2 and switch 3 are closed while switch 1 and 4 are opened. In this configuration charge stored in Cx discharges; charge in the left side flow to ground potential while charge in the right side draws current from operational amplifier generating voltage equals to the following,

$$V_2 = F \ \ Cx \ \ R_f - E_2 \qquad \text{Equation 3}$$

Where E_2 is the offset value of operational amplifier 2

The two resulting voltages are then challenged to a differential amplifier which subtracts both voltages and generates the output voltage

$$V_{out} = K\ (V_2 - V_1) \qquad \text{Equation 4}$$

$$V_{out} = 2\ K R_f C_x - K(E_1 - E_2)$$

This configuration enjoys two advantages; the sensitivity of the circuit is amplified by a factor of 2 and operational amplifier offsets E1 and E2 reduce, ideally cancel, the effect of each other. The second advantage is that, the leakage capacitances, C_{s1} and $C_{s2,}$ do not affect the measurement process. C_{s1} is alternatively driven by the voltage source *Vc* in the charging half and connected to ground in the discharging half, hence C_{s1} does not produce current flowing through C_x. In the case of C_{s2} , the leakage capacitance is always connected to the ground potential.

On the other hand, The coupling capacitance of the switches introduces large random noise to the system. As shown in *Figure 4* the capacitance change is less than 0.1 pF where Cmose Switches typical coupling capacitance could reach as high as 0.5 pF. Furthermore, this approach involves many steps to complete one measuring cycle , which is time consuming and not desirable in real time applications.

2.3.2 Alternating voltage Capacitance to Voltage Converter

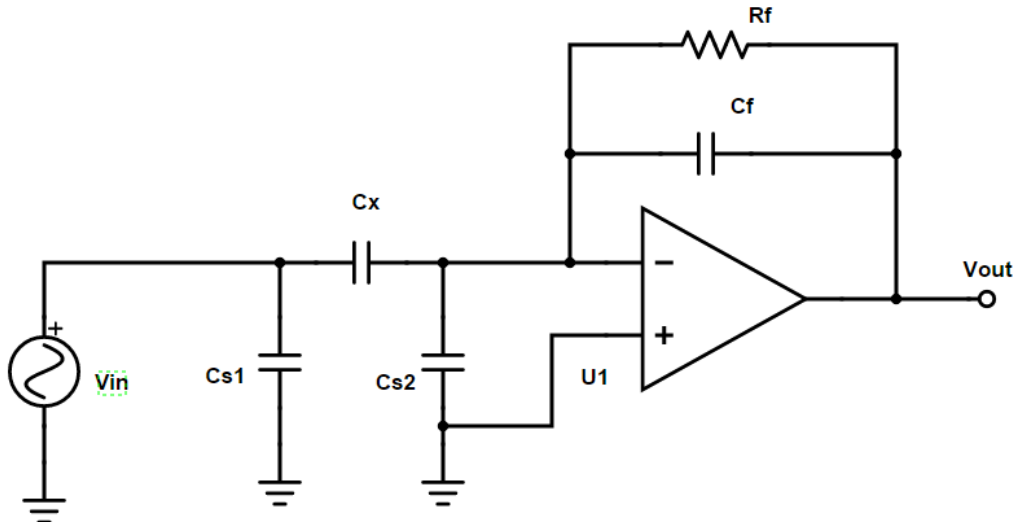


Figure 6: AV based measuring circuit

Figure 6 presents a basic capacitance to voltage converter circuit which incorporates an Alternating voltage excitation signals.

In this approach an excitation sine signal of alternating voltage is applied to one of the electrodes of C_x to produce a current that is challenged to the operational amplifier which in turn produces an alternating voltage proportional to C_x value according to the equation.[9]

$$V_{out} = \frac{j\, R_f\, C_x\, \omega}{1 + jR_f C_f \omega} \times V_{in} \qquad \text{Equation 5}$$

Where

$\omega = 2\pi F$,

R_f the feedback resistance,

and C_f is feedback capacitance respectively,

C_x is the capacitance to be measured, and

F is the frequency of the excitation signal This circuit configuration , though more complex in circuit design and measuring algorithm, provides more robust response with more accurate results than the Charge / discharge capacitance measurements circuits.

2.4 Switching Module

Every electrode in the system is going to be directly attached to a switching module, which would be responsible to control the electrode operating mode through four modes, 1) Detection, 2) Excitation, 3) Grounding and 4) Floating. An Electrode in the excitation mode is connected to the excitation source, and transmits the excitation sine signal to the rest of the electrodes. Whereas, an electrode in Detection mode, is connected to the capacitance to voltage conversion circuit. Electrodes in Ground and Float modes, are in idle state and not connected to either the excitation signal or the capacitance to voltage conversion circuit.

The switching, module is expected to be flexible, to accommodate various requirements and settings such as different number of electrodes and adjust the system operation and switching process accordingly. Furthermore, the multiple channels should be set to operating modes at the same time, for faster acquisition time.

In conventional switching configuration shown on Figure 7, the added stray capacitance is very severe, when sitch 1 and switch 4 are closed to measure the unknown capacitance C_x, the open switches 2 and 3 present parallel stray capacitance , as shown in Figure 7, and effectively distort the resulting circuit before the measurement process start. To cancel this noise capacitance an improved switching will be adopted in this project which will be discussed in the next chapter.

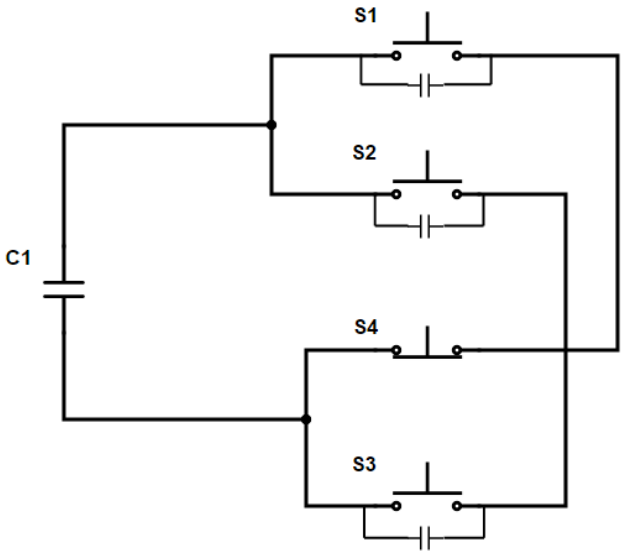


Figure 7: Traditional Switching configuration

2.5 Communication protocols

The most common low end communication protocols are the inter integrated circuit communication protocol, or I²C, designed by Philips ,and the Serial Peripheral Interface protocol , or SPI designed for Motorola. Both protocols are well-suited for communications between integrated circuits, and digital modules .

The SPI bus is a synchronous serial communication interface specification used for short distance communications. SPI devices communicate in full duplex mode using a master-slave architecture with a single master. The master device originates the frame for reading and writing. Multiple slave devices are supported through selection with individual slave select (SS) lines. Although SPI is simpler and easier to implement than I^2C, it requires an independent wire for every slave the master is attached to which might make it very cumbersome to implement in this project.

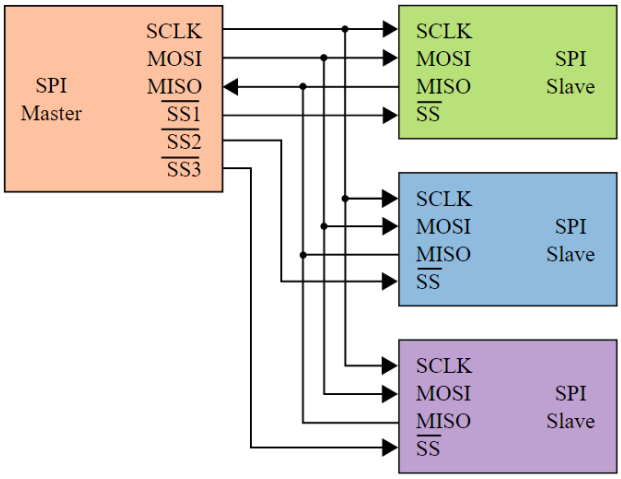


Figure 8: SPI bus Illustration

The I²C protocol uses only two bidirectional wires, Serial Data Line (SDA) and Serial Clock Line (SCL). The I²C reference design has a 7-bit or a 10-bit (depending on the device used) address space. Common I²C bus speeds are the 100 kbit/s standard mode and the 10 kbit/s low-speed mode, but arbitrarily low clock frequencies are also allowed.[11]

Chapter 3: Project Development and Methodology

There are two major sections that needs to be developed in order to produce a complete data acquisition card to achieve the objectives of this project, namely, the hardware development section, which aims to produce a fully functional model of the data acquisition card, and a software development section which focuses on development of the logical steps to control the switching operation, amplification operation, filter operations, as well as interface the data acquisition card with a master controller.

A flow chart in Figure 9 shows the step by step procedure in order to develop the whole system.

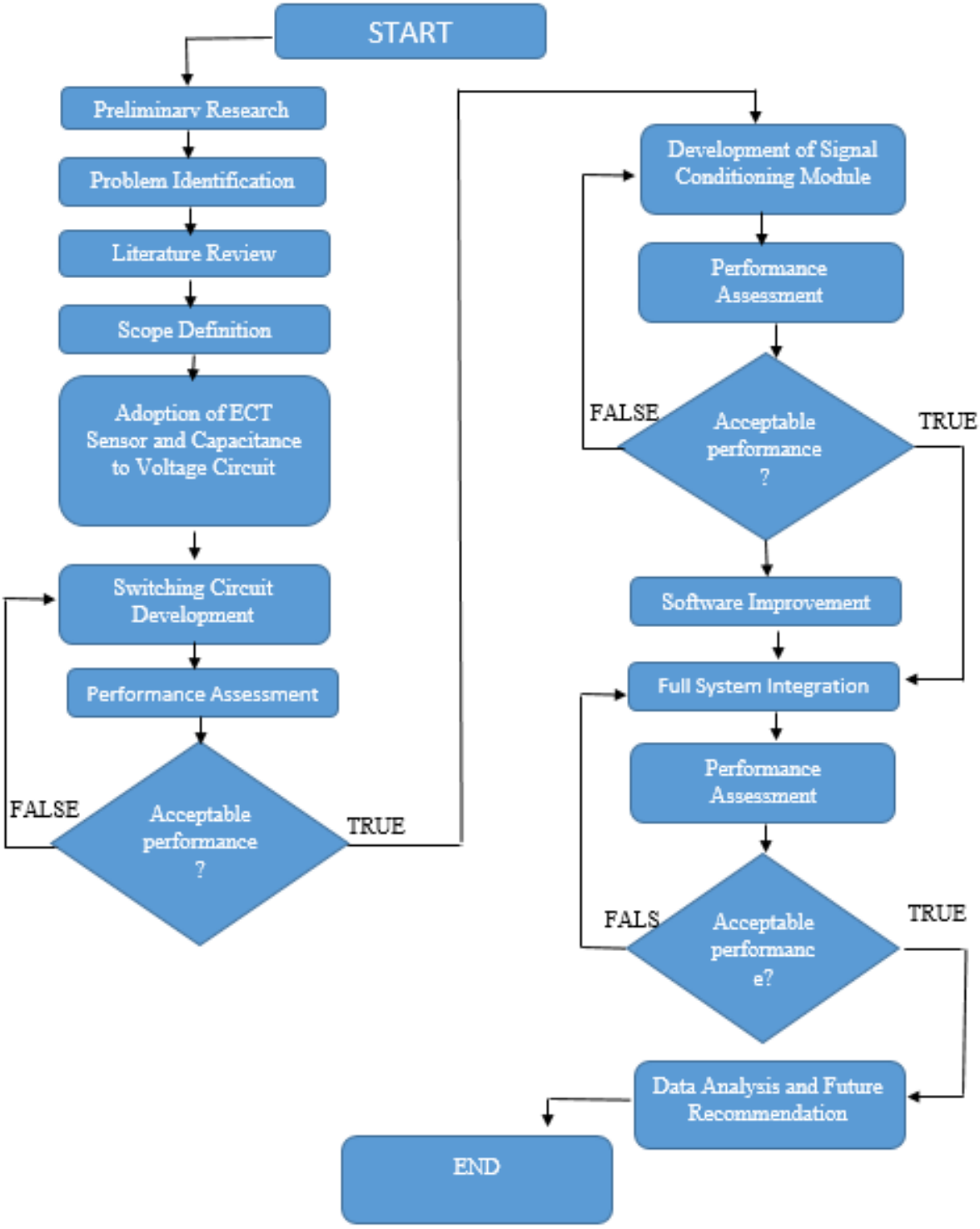


Figure 9: Project Development Flow Chart

3.1 Hardware Development

The final product of this project is a printed circuit board that consists of components ,

- A Capacitance to Voltage Converter,
- Signal conditioning module which apply several arithmetic and filtration operations to the generated signal, an analogue to digital Converter,
- a switching circuitry which controls the operational mode of the attached electrodes and,

In this chapter a detailed descriptions of each component , its functionality and relationship to other components is thoroughly discussed

3.1.1 Capacitance to Voltage Converter

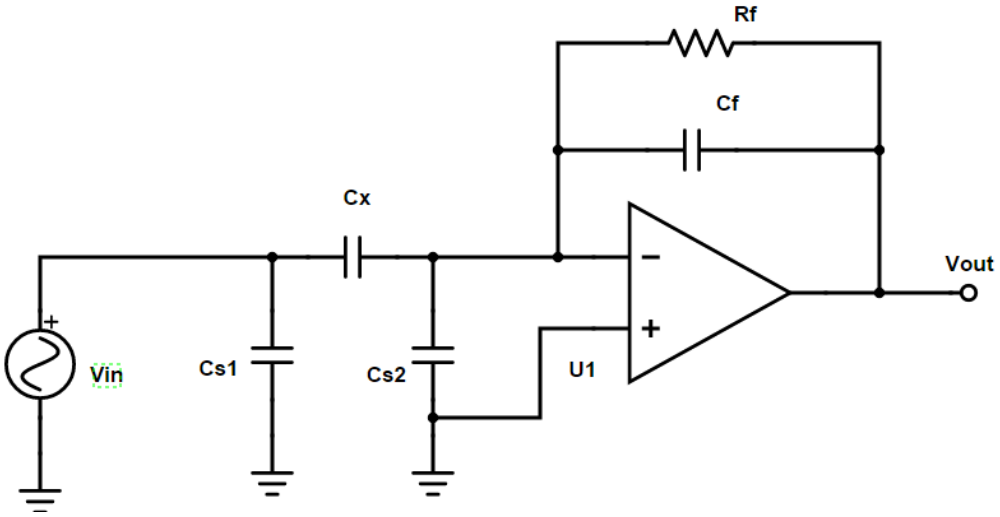


Figure 10: An AV based Capacitance to Voltage converter

For the Capacitance Voltage Converter, an AV based circuit is adopted, as shown in Figure 10. *Cs1* and *Cs2* represent the stray capacitance, $C_x$represents the measured capacitance , C_f and R_f are the feedback capacitance and feedback resistance respectively. Vin stands for sine wave alternating voltage.

In this approach an excitation sine signal of alternating voltage is applied to one of the electrodes of C_x to produce a current that is challenged to the operational amplifier which in

turn produces an alternating voltage proportional to C_x value according to the equation Equation 6 .

$$V_o = \frac{j\, R_f\, C_x\ 2\pi\, f}{1 + jR_f\, C_f 2\, \pi\, f} \times V_{in}$$ Equation 6

Where R_f and C_f are the feedback resistance and feedback capacitance respectively and C_x is the capacitance to be measured. f is the frequency of the excitation signal

If the equation

$$\left|R_f\, C_f\, j\omega\right| \gg 1$$ Equation 7

is satisfied then the value of the produced voltage becomes,

$$V_o = -\frac{C_x}{C_f} \times V_{in}$$ Equation 8

Which implies that the generated voltage signal is directly proportional to the value of C_x, and insensitive to the excitation wave frequency.

As shown in Figure *10* the leakage capacitance Cs1 is directly driven by the voltage source Vexcite and hence does not produce any current that flows through C_x. The same neutrality is observed for Cs2 which is connected to virtual ground by the operational amplifier.

To analyse the system's dynamics the transfer function of the above voltage to capacitance converter is

$$G(s) = \frac{Vo}{Vin} = \frac{S\, C_x\, R_f}{S\, C_f\, R_f + 1} = \frac{C_x}{C_f}\left(\frac{1}{S\, C_f\, R_f + 1} - 1\right)$$ Equation 9

Which is a first order system with time constant K of $\frac{C_x}{C_f}$, can be rewritten as,

$$G(s) = \frac{K}{\tau s + 1} - K$$ Equation 10

When a step voltage is applied to the system,

$$V_o = \frac{1}{s}\left(\frac{K}{\tau s + 1} - K\right)$$ Equation 11

Using reverse Laplace operation,

$$V_o = -K\, e^{\frac{t}{\tau}}$$ Equation 12

The response time of the system is defined as the time elapsed between the time when the unity step voltage is applied and the time when the steady state error is lower than a given value. For the C/V converter, if this given value is selected to be 0.1%, the response time can be calculated as

$$t = 6.9\,\tau$$ Equation 13

Equation 13 implies that the shorter the time constant, the faster the time the system requires to reach its stable state.

For an ECT system, the capacitance to be measured is between 10−11 and 10−14 μF [12], in general. According to Equation 8, if the feedback capacitance is selected to be a few pF, the output voltage would be in a suitable range for an analogue to digital converter To satisfy , the feedback resistance should be large, which leads to a long response time. Therefore, a trade-off must be made between selection of the feedback resistance and the response time. In general, to obtain a good real-time performance of the converter, the response time should be short enough. Here, the response time is set to 1 μs at the frequency of 100 kHz, i.e., one-tenth of one signal period,

$$\tau < \frac{1}{69f}$$ Equation 14

If Equation 10 works, the response time is shorter than 1 μs. However, Equation 6 cannot be simplified as Equation 7 , in this case. Then Equation 6 should be used to calculate the output voltage. According to Equation 6, if the excitation frequency is fixed, the measured voltage is still proportional to the capacitance.

To ensure the measurement accuracy of the circuit acceptable in awide measurement range the sensitivity of the capacitance to voltage converter should be high. The sensitivity is

$$S = \frac{V_o}{C_x}$$ Equation 15

Where Vo is the modulus value of $Vo(t)$. Substituting Equation 6 into Equation 15

$$S = \left| -\frac{\omega\, R_f\, Vi(t)}{j\,\omega\, C_f R_f + 1} \right| = \frac{\omega\, R_f\, Vi}{\sqrt{(\omega\, C_f R_f)^2 + 1}}$$ Equation 16

The output signal of the capacitance to voltage converter should be lower than the analog input range of ADC, which is usually 5V for this project . Assuming that the maximum capacitance to be measured is 6 pF, the sensitivity of the capacitance to voltage converter should be 0.33 Vp−p/pF. If the excitation frequency is 300 kHz and the amplitude of excitation voltage is 16 Vp−p, Equation . (11) becomes

$$0.33 = \frac{2\,\pi\, \times 300\,000\, R_f\, \times 16}{\sqrt{(2\,\pi\, \times 300\,000\, C_f\, R_f)^2 + 1}}$$ Equation 17

To satisfy the conditions on Equation 14 the feedback resistance and capacitance can be determined to be

$R_f \leq 33.2$ kΩ,

$C_f \geq 4.4$ pF.

If the feedback resistance and capacitance are 33 kΩ and 4.4 pF, the sensitivity and response time of the C/V converter would be 0.33 Vp−p/pF and 1 μs, respectively.

3.1.2 Signal Conditioning module

The main functionality of the signal conditioning module is to get the generated signal from the capacitance to voltage converter and apply sequential arithmetic and filtration operation on it in the analogue domain before outputting the result to analogue digital converter. As shown in Figure 11, each Data acquisition board will have two signal conditioning modules to accommodate two electrodes.

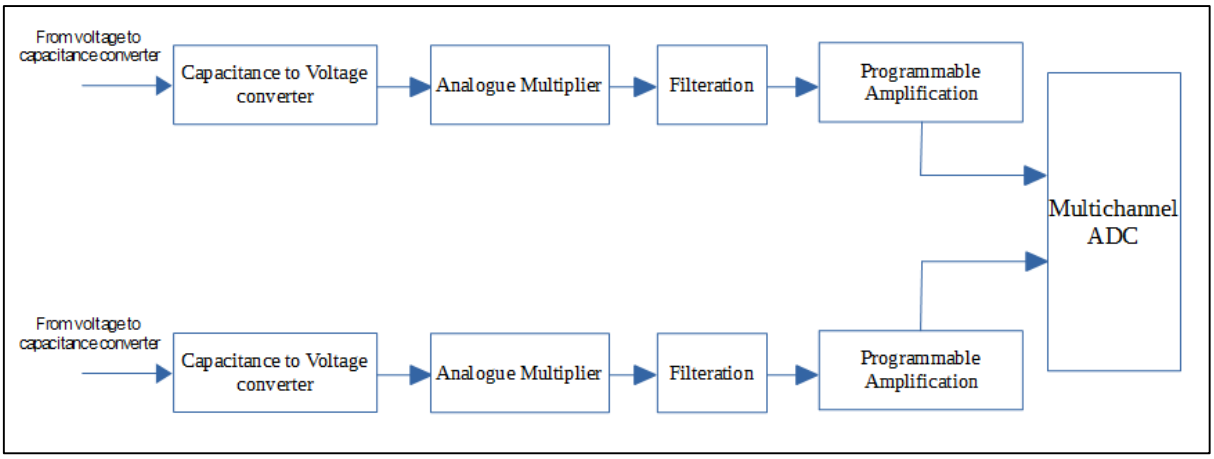


Figure 11: Signal Conditioning module

3.1.3 T-shaped Switching Configurations

Because the system is expected to measure very small change in capacitance, the stray capacitance discussed produced by tranditional switching circuits must be eliminated. To eliminate the stray capacitance a different switching configuration is adopted where every switch is substituted by 3 switches connected in T shampe. As shown on Figure 12, When switch1 and switch 2 are open switch 3 is closed ensuring that any stray capacitance is grounded and effectively eliminated.

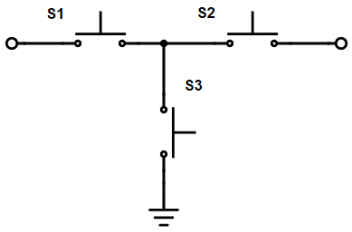
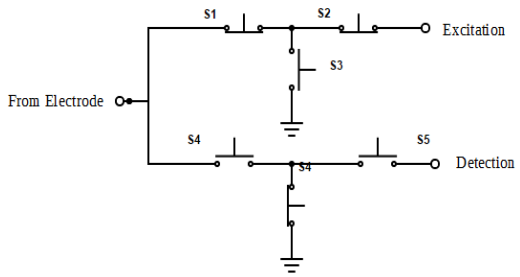
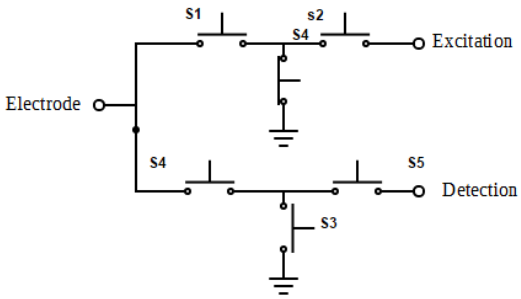
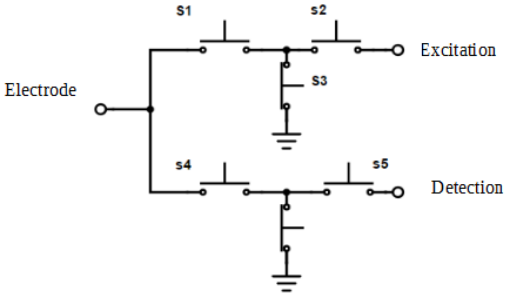
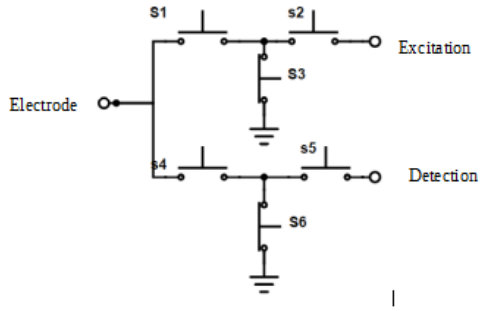


Figure 12: T-shaped Switching Configuration [13]

Table 1:Electrodes Operating Modes

 Excitation Mode	 Detection Mode
 Ground Mode	 Float Mode

3.1.4 Multiplication Stage

If *Equation 6* can be expressed in time domain it would equal to,

$$V_{o1}(t) = -\frac{\omega C_x R_f}{1+(\omega C_f R_f)^2}\left[\frac{1}{\omega C_f R_f}\exp\left(-\frac{t}{C_f R_f}\right) - \sin(\omega t) + \omega C_f R_f \cos(\omega t)\right] \quad \text{Equation 18}$$

The wave form of V_{01} is shown in *Figure 13: Vo1 graph in Time Domain*

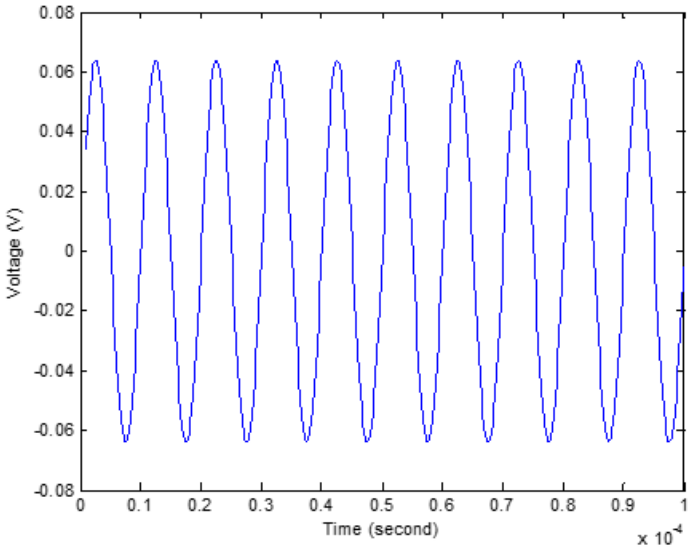


Figure 13: Vo1 graph in Time Domain

When the V_{O1} signal is multiplied by a sine signal, $V_i = \cos(\omega t + \alpha)$, the resulting signal

equals to

$$V_{02} = -\frac{\omega\, C_x\, R_f}{1 + \left(\omega\, C_f\, R_f\right)^2} + \frac{1}{2}\left[\sin(2\omega t + \alpha) - \sin(\alpha)\right] \qquad \text{Equation 19}$$

where α is the phase difference between the input signal V_i and the demodulation signal *Figure 14*shows the waveform of V_{o2}.

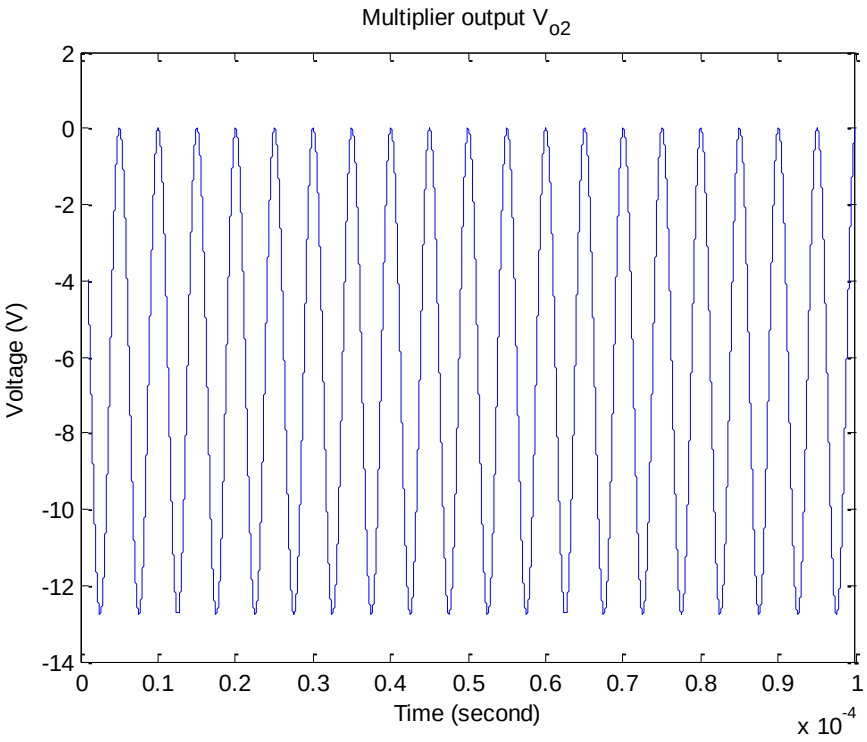


Figure 14: Multiplication Product wave shows the waveform of V_{O2}

3.1.5 Filtering stage

The target is to acquire the Dc component from Vo2 which holds the value of Cx , the Dc component equation is,

$$V_{o3} = -\frac{1}{2}\frac{C_x}{C_f}\left[\cos(\alpha) + \frac{1}{\omega C_f R_f}\sin(\alpha)\right]V_i \qquad \text{Equation 20}$$

In order to get the Dc component in the Vo2 , the signal is ran through fourth order Butterworth filter with cut off frequency of 5.1 kHz and transfer function as follows,

$$H = \left(\frac{1}{-\omega^2 C_1 C_2 R_1 R_2 + j\omega C_1 (R_1 + R_2) + 1}\right)^2 \qquad \text{Equation21}$$

With $C_1 = 10\ nF$, $C_2 = 22nF$ *and* $R_1 = R_2 = 1k\Omega$, the circuit diagram of the filter is shown in figure Figure 15 .

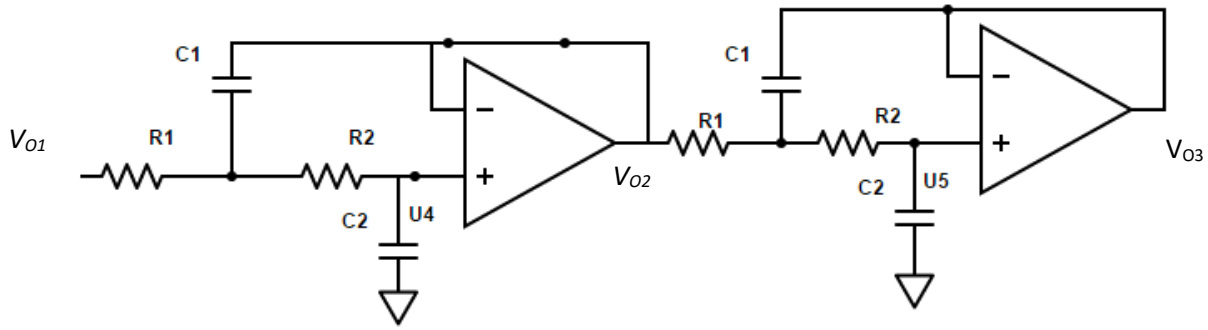


Figure 15: Butterworth Low pass Filter

3.2 Software Development

The final software version implemented in this project is expected to accomplish the following tasks,

- Receiving commands from a central controller and delivering results using I^2C communication protocol.
- Controlling the operational modes of the attached electrodes, by controlling the switching circuit
- Controlling the amplification of the resulting signal to ensure the signal is within the best range of the analogue to digital component, and
- Convert the resulting signal to digital value using an analog to digital converter.

In this chapter a detailed descriptions of each task, and its relationship to other components is thoroughly discussed

3.2.1 Local controlling

Every data acquisition card module incorporate a slave microcontroller that manages the operation of the two electrodes attached to the card, using the switching module, controls the amplification value of the programmable amplifier and reads the analogue value and of the electrodes.

The slave controller is controlled by a master controller that resides in an independent processing unit. The two controllers communicate using I^2C protocol.

Due to the low processing power require for this project , and the relatively slow computing rates expected the Microchip PIC18F452 microcontroller is used in the final model, which is a Low powered Low cost 8 bit microcontroller with programmable flash memory and 10 bits built in analogue to digital converter.

3.2.2 Programmable Amplification

As shown in Figure 16*Figure 16*, the resulting voltage readings of the filtration process varies greatly, where adjacent electrodes results in reading of as high as 3.8V, further apart readings results in readings in range below 1v. Hence to amplify low readings with selective amplification factor, a Programmable Amplifier is used before the digitizing process. The amplifier used was the AD526 was used, with amplification factors of 1,2,4,8 and 16. The results are shown in.

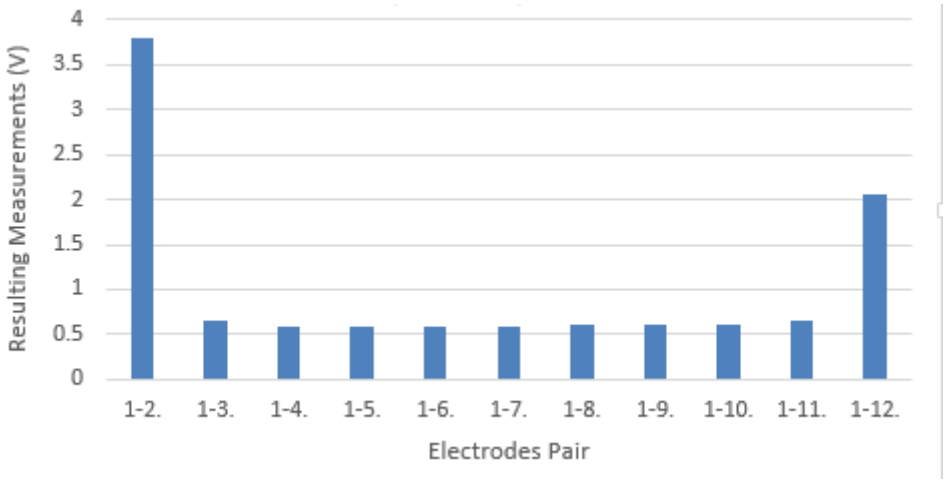


Figure 16: ADC Readings before programmable Amplifier

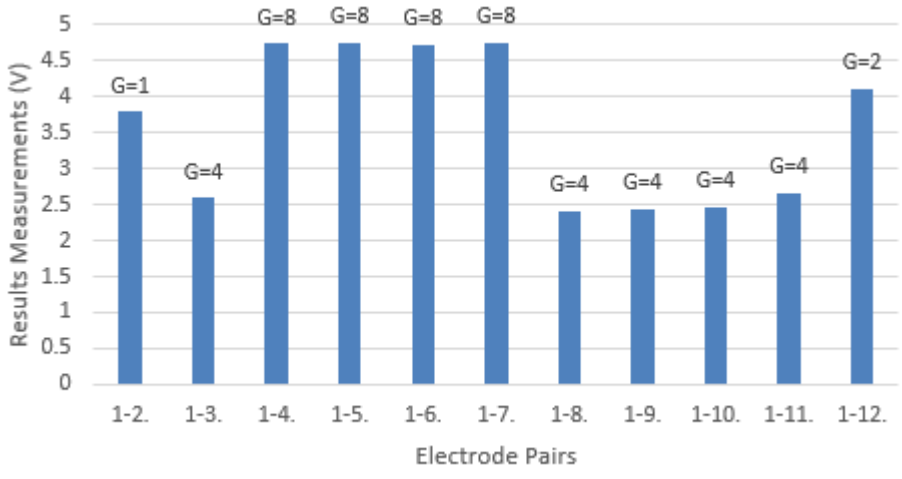


Figure 17:ADC Readings After Programmable Amplifier

3.2.3 Data Normalization

In order to gain the dynamic phase distribution inside the monitored pipe the ECT system should compare the obtained raw measurements with measurements obtained in two extreme cases, the first case is when the measured pipe is fulfilled with the lower electrical permittivity material, and the second case is when it is fulfilled with the material with the higher electrical permittivity. Suppose the corresponding capacitance values measured in these cases are C_a and C_b ,respectively, and the current measurement is C the normalized capacitance can be expressed as,

$$\varphi = \frac{C - C_b}{C_a - C}$$ *Equation 22*

3.2.4 Analog to Digital Conversion stage

For simplicity the ADC module used in this project is a built module inside the Microcontroller, the ADC has 10 bits resolution with the reference voltage is at 5 volts the minimum detected voltage change is 4.8 mV. The minimum sampling time required by this module is 225 us.

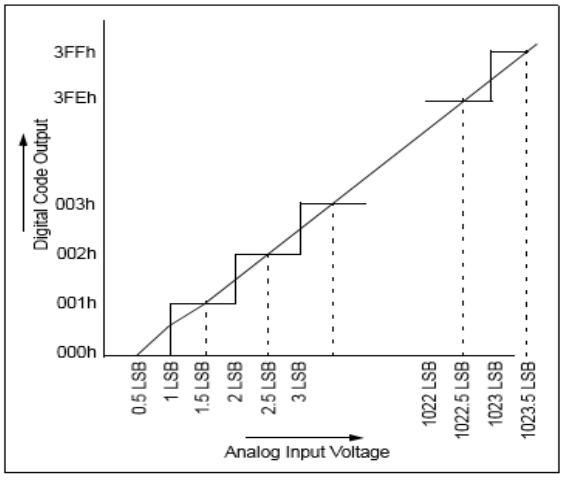


Figure 18: ADC Transfer Function

However the expected values are very small in ,maximum of 200 mv, and hence the programmable amplifier AD526 was incorporated with multiplication factors of 2, 4,

8, and 16 .The transfer function of the ADC module is shown in Figure 18*: ADC Transfer Function*.

3.2.5 Communication protocols I²C

The Inter-Integrated Circuit™ (I²C™) is a multi-master, multi-slave, single-ended, serial computer bus invented by Philips Semiconductor. I²C uses only two bidirectional open-drain lines, Serial Data Line (SDA) and Serial Clock Line (SCL), pulled up with resistors, as shown in Figure 19*: I2C communication Protocol*

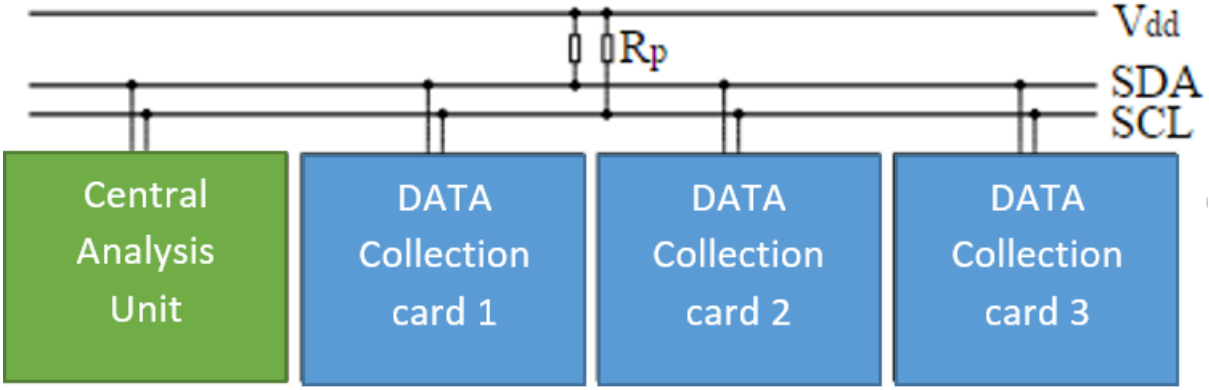


Figure 19: I²C communication Protocol

With transfer rates of 100kb/s, 400 kb/s, or 1Mb/s, and maximum attached devices of over 100, The I2C protocol is ideal for ECT systems, and matches all the requirements needed for smooth scanning and data transmitting operations. Furthermore, the availability of the shelf I2C modules, makes it a perfect candidate for time constrained project like this one.[14]

Chapter 4: Results and Discussion

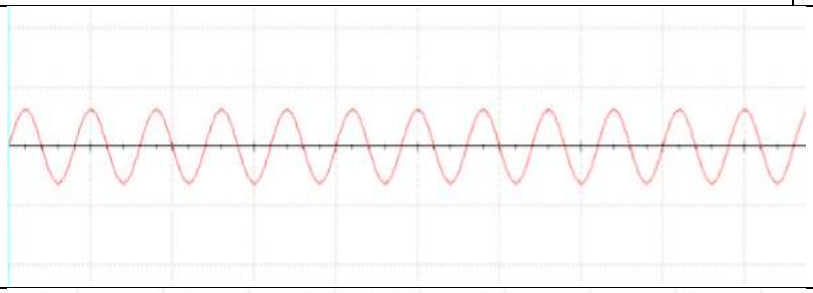
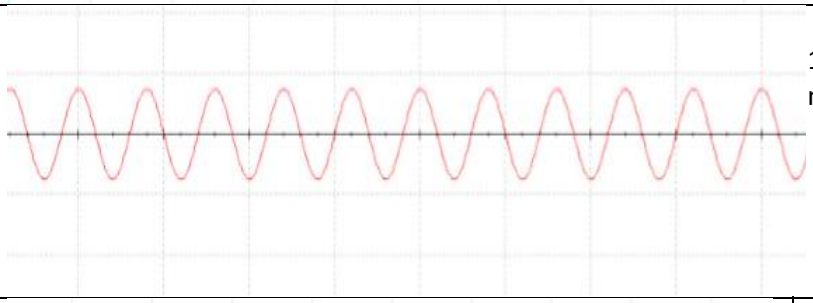
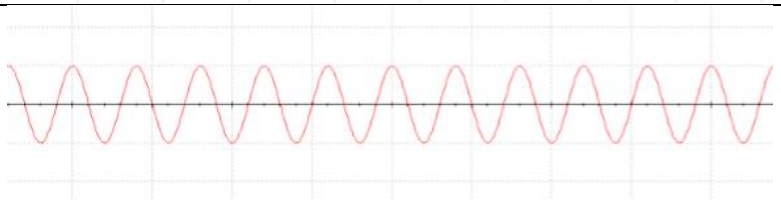
4.1 Capacitance to Voltage Conversion Circuit

The essential working strategy of the capacitance to Voltage circuit is to apply an exciting sine wave AV signal to one sensor's electrodes , the excited electrode, to

generate a distorted AV Signal on the rest of the electrodes. The distorted signal then undergoes signal conditioning process.

To obtain the waveforms in Table 2, a 100 KHZ, 16 Volts peak to peak excitation signal is used.

Table 2: Capacitance to Voltage Result Converter

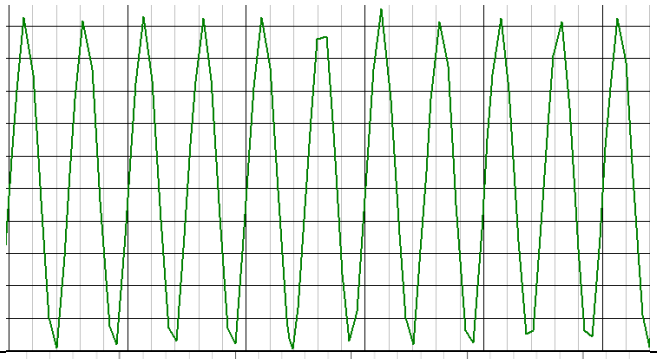
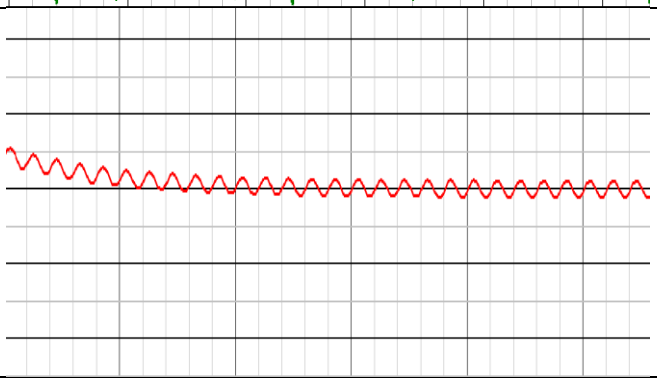
Capacitance Used	Simulation results	Simulated results
1pF		500 mv/dev
2pF		100 mV/dev
3.9pF		100 mV/dev

4.2 Signal Conditioning Module

The resulted signal from the Capacitance to voltage conversion process is multiplied with the original excitation signal to produce two components , a high frequency Sine signal and a direct voltage signal. Those two components are subjected to a low pass filter to get rid of the high frequency component. The resulting direct voltage signal has

a magnitude proportional to the capacitance value between the excited electrode and the measured electrode. In Table 3, the different signals are illustrated,

Table 3:Signal Conditioning Resulting signal

Signal Description	Signal	Scaling factors
Resulting signal after multiplication		50 mV/dev
Resulting Signal After filtration and Amplification		50 mV/dev

4.3 Analogue to Digital Conversion

After obtaining the Direct Voltage signal, signal is passed to a programmable amplifier which tries to keep the DV value in the as high as possible , but not higher than the maximum input Voltage to the Analog to Digital converter which is 5 Volts. After the a achieving the best DV value possible the signal is passed to an analogue to digital converter , ADC, which is responsible to sample the DV signal and present it in the digital domain

Both modules, the programmable amplifier and the ADC are controlled by an on board microcontroller. In Addition the microcontroller controls the switching circuits, and communicate with central analysis unit.

4.4 Final Product

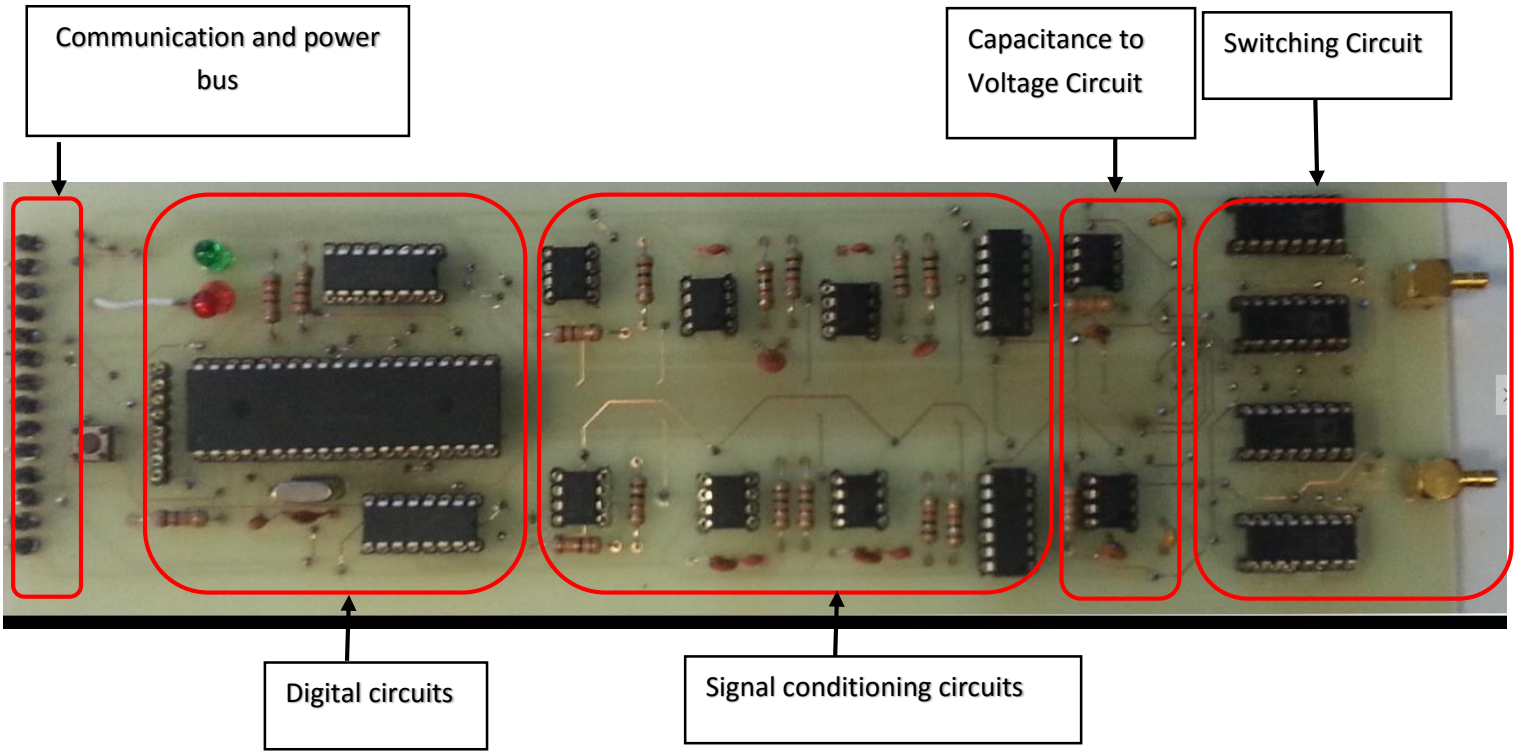


Figure 20: Final Model

Chapter 5: Conclusion

In this project the main objectives was dedicated to develop a robust, and portable data collection card for in-house ECT system. A model with complete functionality was produced and experimentally tested.

To achieve the main objective of this project which is to have automatic and fast data rates. Unlike conventional data collection card where all control and sampling operations are handle by central analysis unit, the final product of this project incorporates complete digital system with local controller to handle the switching , amplification and digitizing operations. This feature enables parallel operation of a system with more than one data collection card and hence greatly increase the sampling rate of the system.

To ensure easier integration with any central analysis unit, in any generic ECT system, the final design adheres to the I2C communication protocol. Through which the Data Collection Card receives commands from the Central controller to perform set of tasks, or enables the central controller to read the ADC value.

The data collection card was built with later improvements and modifications considered. All major components are connected with detachable slots which simplifies any future hardware modifications. Furthermore, a local on board programming module is installed, which gives easy access for any software development to the local controller, As well as indicator LEDs for debugging purposes.

In this project one of the main parts of the in-house ECT system was developed. However, In order to produce a complete in-house ECT system, a central controlling unit has to be designed. Moreover, the ECT Image generating algorithms should be developed. Furthermore, the designed data collection card can be further improved by incorporating components with higher resolution and faster processing times with lower internal noise.

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APPENDIX A – Gantt Chart and Key Milestone

FYP 1 Gantt Chart

Item / Week	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Title Selection	■	■												
Preliminary research			■	■										
Scope Definition			■	■										
Literature Reviews				■	■	■	■	■	■	■	■	■	■	■
Submission Extended Proposal						*								
Proposal Defence									*					
Elementary Designs and models of sensor and measuring circuit simulations						■	■	■	■					
Switching Module development									■	■	■	■		
Primary design Assessment										■	■	■		
Submission of Interim Draft Report													*	■
Submission of Interim Report													■	*

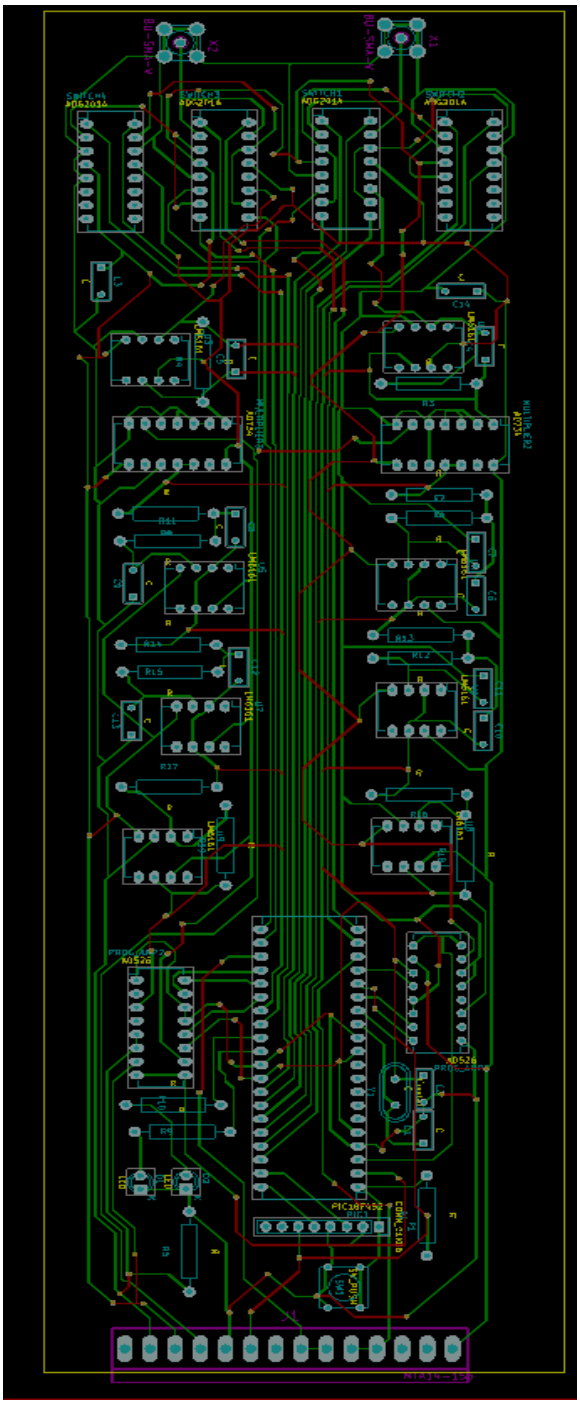
* key Milestones

FYP2 Gantt Chart

Item / Week	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Designing the PCB of the system	■	■	■	■	■									
Developing the Software of the data acquisition module					■	■	■	■	■					
Submission of Progress Report							*							
Design Assessment and evaluation							■	■	■	■				
Tuning and optimising of developed model						■	■	■	■	■	■	■		
Result analysis and outcome presentations							■	■	■	■	■	■		
Testing model under disturbance									■	■	■	■		
Submission of Draft Final Report											*			
Further tuning and optimization of the model									■	■	■	■		
Submission of Dissertation												*		
Viva													*	
Submission of Project Dissertation (Hard Bound)														*

* key Milestones

APPENDIX B – PCB LAY OUT DESIGN



APPENDIX C- Code for local controller

```
#define _XTAL_FREQ        12000000
#define slave_address     0x18

#define read_electrode_1      1
#define read_electrode_2      2

//commands difinitions
#define excite_switch_1       3
#define excite_switch_2       4
#define detect_switch_1       5
#define detect_switch_2       6
#define float_switch_1        7
#define float_switch_2        8
#define ground_switch_1       9
#define ground_switch_2       10

//I2c vars
unsigned short recieved ;
volatile unsigned char send[] = {0,0};
unsigned char i2c_counter =0;          //  counter for counting elements sent to I2C
volatile unsigned char i2c_command =0;

// functions protocols
void delay();
void init_adc(void);
void init_i2c(void);
void i2c_isr(void);

void switch_excite(unsigned char s);
void switch_detect(unsigned char s);
void switch_ground(unsigned char s);
void switch_float(unsigned char s);
unsigned int adc_read (unsigned char channel);

void interrupt high_isr(void)          // High priority interrupt
{
  if (PIR1bits.SSPIF && PIE1bits.SSPIE) {      // Check for SSP interrupt
    i2c_isr();          // It is an SSP interrupt, call the SSP ISR
    PIR1bits.SSPIF = 0;  // Clear the interrupt flag
  }
}

void main(void) {
  TRISD =0x00;                 // LED PINS SET TO OUTPUT and switch2
  TRISB = TRISB &0xC0;          // for switch2
  LATDbits.LATD6 = 1;
  LATDbits.LATD7 = 0;

  init_adc();
  init_i2c();

  INTCONbits.PEIE = 1;   // PERIPHERRAL INTERRUPT ENABLED
  RCONbits.IPEN   = 1;   // INTERRUPT PRIORITY ENABLED
  INTCONbits.GIE = 1;    // GLOBAL INTERRUPT ENABLED

  unsigned int result=0 ;
  while(1){
    switch (i2c_command){
      case read_electrode_1:
        result = adc_read(0);
        send[0] = result & 0xFF;
```

```
    send[1] = (result>>8) & 0xFF;
    LATDbits.LATD7 = ~LATDbits.LATD7;      // indicate any operation by flashing an LED
    i2c_command = 0;
    break;
  case read_electrode_2:
    result = adc_read(1);
    send[0] = result & 0xFF;
    send[1] = (result>>8) & 0xFF;
    LATDbits.LATD7 = ~LATDbits.LATD7;      // indicate any operation by flashing an LED
    i2c_command = 0;
    break;
  case excite_switch_1:
    switch_excite(0);
    LATDbits.LATD7 = ~LATDbits.LATD7;      // indicate any operation by flashing an LED
    send[0] = 1;
    send[1] = 1;                           // acknowledgement signal
    i2c_command = 0;
    break;
  case excite_switch_2:
     switch_excite(1);
    LATDbits.LATD7 = ~LATDbits.LATD7;      // indicate any operation by flashing an LED
    send[0] = 1;
    send[1] = 1;                           // acknowledgement signal
    i2c_command = 0;
    break;
  case detect_switch_1:
    switch_detect(0);
    LATDbits.LATD7 = ~LATDbits.LATD7;      // indicate any operation by flashing an LED
    send[0] = 1;
    send[1] = 1;                           // acknowledgement signal
    i2c_command = 0;
    break;
  case detect_switch_2:
    switch_detect(1);
    LATDbits.LATD7 = ~LATDbits.LATD7;      // indicate any operation by flashing an LED
    send[0] = 1;
    send[1] = 1;                           // acknowledgement signal
    i2c_command = 0;
    break;
  case float_switch_1:
    switch_float(0);
    LATDbits.LATD7 = ~LATDbits.LATD7;      // indicate any operation by flashing an LED
    send[0] = 1;
    send[1] = 1;                           // acknowledgement signal
    i2c_command = 0;
    break;
  case float_switch_2:
    switch_float(1);
    LATDbits.LATD7 = ~LATDbits.LATD7;      // indicate any operation by flashing an LED
    send[0] = 1;
    send[1] = 1;                           // acknowledgement signal
    i2c_command = 0;
    break;
  case ground_switch_1:
    switch_ground(0);
    LATDbits.LATD7 = ~LATDbits.LATD7;      // indicate any operation by flashing an LED
    send[0] = 1;
    send[1] = 1;                           // acknowledgement signal
    i2c_command = 0;
    break;
  case ground_switch_2:
    switch_ground(1);
    LATDbits.LATD7 = ~LATDbits.LATD7;      // indicate any operation by flashing an LED
    send[0] = 1;
    send[1] = 1;                           // acknowledgement signal
```

```
            i2c_command = 0;
            break;
          default:
            send[0] = 0;
            send[1] = 0;                    // acknowledgement signal
            i2c_command = 0;
            break;
      }
    }
    return;
}
unsigned int  adc_read(unsigned char channel){
    if(channel >1) return 0;
    else{
       ADCON0bits.CHS = channel;
       ADCON0bits.ADON = 1;       //switch ADC module on
       ADCON0bits.GODONE = 1;     //start conversion
       while(ADCON0bits.GODONE);  // wait till conversion is done
       ADCON0bits.ADON = 0 ;      //switch ADC module off
    }
}
void switch_excite(unsigned char s){
    if (s==0) LATB = 0b00011100;
    else if(s==1)LATD = 0b00011100;
}
void switch_detect(unsigned char s){
    if (s==0) LATB = 0b00100011;
    else if(s==1)LATD = 0b00100011;

}
void switch_ground(unsigned char s){
    if (s==0) LATB = 0b00011010;
    else if(s==1)LATD = 0b00011010;

}
void switch_float(unsigned char s){
    if (s==0) LATB = 0b00011011;
    else if(s==1)LATD = 0b00011011;
}
void delay(){
    int i,j;
    for(i=0;i<500;i++){

       for(j=0;j<100;j++);
    }
    return;
}

void init_adc(void){
    //SET R REGISTER TO INPUTS
    TRISA = 0xFF;
    //FOSC/16
    // INITIALLY SELECTING CHANNEL 0
    // TURNING THE MODULE OFF FOR NOW
    ADCON0 = 0b01000000;
    // RIGHT JUSTIFIED
    //  FOSC/16
    // ONLY AD0 AND AD1 ARE ANALOGUE INPUTS
    ADCON1 = 0b01001101;
}
void init_i2c(void){
    TRISC |=0x18;          // rc3 and rc4 inputs

    SSPADD = slave_address;
```

```
   SSPCON1 = 0x36;      // SSPEN: Synchronous Serial Port Enable bit - Enables the serial port and configures the SDA and SCL pins as the
serial port pins
                        // CKP: SCK Release Control bit            - Release clock
                        // SSPM3:SSPM0: SSP Mode Select bits       - 0110 = I2C Slave mode, 7-bit address
   SSPCON2=0x01;        // DISABLE GENERAL CALL ENABLE BIT
   SSPSTAT=0x00;
   PIE1bits.SSPIE = 1;          // Enable SSP interrupt
   IPR1bits.SSPIP = 0x01;       // Set SSP interrupt priority to high
   PIR1bits.SSPIF = 0;

}


// This is the actual SSP ISR
void i2c_isr(void) {
   unsigned char temp , discard ;
   unsigned char size = sizeof(send)/sizeof(send[0]);
   temp = SSPSTAT & 0x2d;
   if ((temp ^ 0x09) == 0x00) {          // write request, last byte was address
      i2c_command = SSPBUF ;            //commmand coming

   } else if ((temp ^ 0x29) == 0x00) {    // write request, last byte was data
      i2c_command = SSPBUF ;            //command coming

   } else if ((temp ^ 0x0c) == 0x00) {    // read request, last byte was address == SEND MESSAGE FROM THE BEGINNING
      i2c_counter = 0;                   // reset the counter
      SSPCON1bits.WCOL = 0;             //wait for the sspbuf register finishes
      discard = SSPBUF;                 //clear the buffer
      SSPBUF = send[i2c_counter++];         //Send the first element of the message and increase the counter

      while(!SSPSTATbits.BF);           // hold on till the buffer is empty
      if (SSPSTATbits.BF) discard = SSPBUF; // just to ensure no collision happens, empty the buffer

   } else if ((temp ^ 0x2c) == 0x00) {    // read request , last byte was data
      if (SSPSTATbits.BF) discard = SSPBUF;    // Clear BF
      SSPCON1bits.WCOL = 0;
      if(i2c_counter >= size)i2c_counter = 0;       // ensure the counter did not go over the message limit
      SSPBUF = send[i2c_counter++];
   } else {                             // slave logic reset by NACK from master
      discard = SSPBUF ;
   }
   SSPCON1bits.CKP = 1;                 // release the clock line
}
```