Development of Novel Multilevel Inverter with Reduced Power Switches

by

DEVENTERAN A/L KUMARAN

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Dissertation submitted in partial fulfilment of
the requirement for the
Bachelor of Engineering (Hons)
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Universiti Teknologi PETRONAS,
32610, Bandar Seri Iskandar,
Perak

CERTIFICATION OF APPROVAL

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Approved by,

_____

(Dr. Ramani Kannan)

UNIVERSITI TEKNOLOGI PETRONAS
BANDAR SERI ISKANDAR, PERAK
JANUARY 2016

CERTIFICATION OF ORIGINALTY

This is to certify that I am responsible for the work submitted in this project, that the original work is own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

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(DEVENTERAN A/L KUMARAN)

ABSTRACT

In recent days the usage of multilevel inverters became very essential and crucial especially on high power consuming sites. The advantages on the modularity, failure management, reliability and the waveform with less harmonic distortion at the output made the multilevel inverter to gain more attention in the current industry. Even though, multilevel inverters serving the industry with more significant advantages however they do have drawbacks such the usage of high number of power switches in their circuit and this leads to high manufacturing cost and also increase the complexity of the circuit structure. In this paper a new 9 level multilevel inverter topology has been analyzed. The proposed topology has considered factors such as reducing the power switches, reducing the total harmonic distortion and reducing the complexity of the structure. The performance quality of the proposed topology has analyzed in terms of THD and switching trust and compared with existing conventional inverters using carrier based pulse width modulation techniques. The proposed has developed using single source and double source inverter unit. The MATLAB simulation has done for the proposed topology and a sinusoidal output waveform has produced.

ACKNOWLEDGEMENT

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CHAPTER 1

INTRODUCTION

1.1 Background Study

The demand for the electrical appliances has increased over the years. Technology has played a major part in inventing new electronic appliances to support the demands equally. However every electronic appliances differ in terms of the power consumption because some are meant to use alternating current and some will be using direct current. Small scale power generators usually will produce dc current and AC is a common power used to run electrical appliances. At times there will be situations to use AC appliance having dc source like small scale generators. In this case the direct current has to be converted into alternating current.

Power inverters are the device used for converting the direct current into alternating current. Inverter uses some switches and circuit connections to produce alternating current at any expected voltage and frequency. In industries the usage of high power appliances has increased over years. So some equipment uses medium voltage and some uses high voltages. It is challenging to connect switch directly to medium voltage equipment and multilevel inverter created to achieve high power rating. The combination of few lower level DC sources in input produces the desired AC voltage as output in multilevel inverter.

Multilevel inverter has its own advantages compare to conventional inverters. Less stress on motor can prevent the damages towards them due to the capability of

producing common mode voltage by multilevel inverter. Multilevel inverters also can make use the input current with reduced distortion. Moreover, multilevel inverters can operate at both high and low switching frequencies. Lower switching frequency will improve the efficiency due to its less switching losses. The demand for multilevel inverters also improved due to its reduced harmonic distortion without using any filter circuit.

Various techniques on control and modulation with new topologies have been discussed to improve the performance of multilevel inverters. Aspects such as current looping, voltage capability of the circuits, circuit complexity, number of switches used, dc sources and hybrid topologies has been discussed. The combination of conventional topologies or any new topologies can be said as Hybrid topology. Using the hybrid topology the efficiency and switching losses and be improved. The modulation techniques in hybrid topologies useful in the usage of switching frequencies according to the voltage levels. The hybrid modulation techniques also improve the strength of the high power applications.

Diode clamped multilevel inverter, flying capacitors multilevel inverter and cascaded H-bridge multilevel inverters are the commonly used inverters. In diode clamped inverter, it uses one DC source and capacitors connected parallel to the source which equally distributes the DC voltages. Diode clamped inverters normally will be used in higher voltage applications due to its equal distribution of a single dc source into several dc inputs using the capacitors. However the diode clamped inverter has disadvantages where it needs more diodes and uses external circuit for capacitor balancing. Flying capacitor inverter uses a clamping capacitor and large storage capacitors needed. At the same time it is very hard to maintain the voltage of each capacitors.

Among these topologies H-bridge multilevel inverter is one of the well-known topology. Cascaded H-bridge multilevel inverter uses switches and also diodes in its circuit structure. Compare to other topologies H-bridge multilevel inverters don’t use any

diodes and capacitors for clamping purposes. The output wave produced is almost sinusoidal in nature without using any filter. However the efficiency of the H-bridge multilevel inverter can be improved even more reducing the harmonic distortion level. The power switches usage is high in H-bridge inverters. The increase in the number of power switches also makes the circuit structure to become more complex.

1.2 Problem Statements

The component usage is increases as the level of the H-Bridge multilevel inverter increase. Increase in component such as power switches causes the high switching losses and circuit structure to be more complex. The usage of more power switches increase the overall cost of the inverter. The switching stress and also control complexity causes the production of harmonics.

1.3 Objectives

There are number of objectives need to be achieved by end of this project. The objectives are:

- Reduce the harmonics produced by the switching trust and control complexity.
- Reduce the number of power switches usage to reduce the switching losses.
- Reduce the circuit complexity of the H-bridge multilevel inverter.
- Reduce the overall production cost of the inverter due the high usage of power switches.

1.4 Scope of study

The scope of study of the project is about the designing a new topology for cascaded H-bridge multilevel inverter to reduce the harmonic distortion and power switches used. The literature review of the project includes the number of switches, switching angle, harmonic distortion, modulation techniques, cost and complexity of the proposed design topology. Simulation software such as MATLAB, LOGISIM and MULTISIM can be used to design the theoretical circuit topology of the inverter and also to get the output waveforms. Different switching combinations will examined to get the expected voltage at every inverter cells. The modulation techniques will be examined to control the harmonics produced.

CHAPTER 2

LITERATURE REVIEW

In the research study of reducing power switches and harmonic distortion of multilevel inverters several research papers were studied and reviewed to understand about the scope of H-bridge multilevel inverters. The literature study covers topics such as number of switches used in a topology, circuit structure, modulation techniques and load used in H-bridge multilevel inverters.

2.1 Multi Source Multilevel Inverter

Approximately more than 20 years ago the idea of using multiple small voltage source to perform power conversion was patented. This approach has been a great start to reduce the number of switches as the inverter level increases. Moreover, this multilevel inverter attempt having some advantages such as reduced switching losses, improved electromagnetic capability and increased voltage capability. Basically In multilevel inverters an array of power semiconductors which is called as switches with voltage sources produces voltages with stepped waveforms at the output. The fast switching of DC signal produces the multiple levels which is staircase wave which is similar to a sine wave. H bridge multilevel inverters is the common type of inverters which uses separate DC sources.

2.1.1 Cascaded H-bridge Multilevel Inverter

In [1] a seven level H-bridge multilevel inverter with only seven switches has proposed. The author has explained about the Fundamental switching scheme and selective Harmonic Elimination to handle the total harmonic distortion. Appropriate switching angle and Selective Harmonic Elimination Stepped Waveform (SHESW) is used to reduce harmonics. The (SHESW) technique can generate output waveform without using any filter. The author has explained about the powering mode, freewheeling mode and regenerating mode.

The attenuation of the switching component is called modulation. Fundamental switching frequency and high switching frequency PWM decides the pulse width modulation controls. Carrier based PWM techniques are widely being used due to its simple implementations. Sinusoidal PWM, third harmonic injection PWM and space vector PWM are the major carrier based techniques being used for conventional inverters. Sinusoidal PWM are the mostly used carrier technique in industrial applications [2]. Both phase shifted and level shifted modulation can be used for cascaded H-bridge inverters. Harmonic distortion differs compare to both the modulation. Alternate phase opposition disposition (APOD), Phase opposition disposition (POD) and phase disposition are under phase shifted modulation. Phase disposition method reduces more harmonic distortion [3].

The paper [4] explains about the working principle of symmetric, asymmetric and cascade switched diode multilevel inverter. The algorithm for output voltage values, number of levels and number of power switches needed for the inverter design has discussed. The design flexibility and optimization of inverter has achieved through the suggested topology. There is also an algorithm has been in discussed in [5] to generate minimum THD level for selected voltages with optimum switching angles.

Total harmonic distortion concept has discussed well in [6] for cascade multilevel inverters for industrial applications. From the studies on the paper it is known that the

harmonic distortion level depends on the switching angles of the inverters. Equations has been shown on calculating the switching angles and the harmonic distortion level has been discussed for 7, 11 and 15 level inverters. THD levels were compared with the output voltages and simulations outputs were present with increase and decrease in voltages.

A number of research papers were read to know about the load connections of the multilevel inverter. A 5 level H-bridge multilevel inverter topology with induction motor as load created and compared with conventional multilevel inverter. The total harmonic distortion produced in the voltage and current of the proposed topology is lower compare conventional inverter [7]. Another topology in [8] has used RL load and design the structure with less switches, harmonic distortion and lower EMI. In [9] a topology had discussed with R load, RL load and R load with filter. From the results it is proven that the harmonic distortion reduces as the level of inverter increases using all the loads mention above. Compare to the 3 loads R load with filter produces less THD and R load produces most THD [10].

2.1.2 Hybrid H-bridge Multilevel Inverter

The combination of conventional or new topologies can be said as hybrid. A hybrid topology has discussed to increase the output voltage level with reduced harmonic distortion and low order harmonics in [11]. The author has developed a topology with greatest number of level and reduced switching losses due to the highest DC link voltage with lower switching frequency. The equations to generate the output levels for hybrid model were explained. The switching combination were explained to generate output voltage at every level. It is also explained about the state with DC link voltage with least number of commutation which reduces the switching losses and this state also contains low and high frequency components such IGBT and IGCT.

2.1.3 New Hybrid H-bridge Multilevel Inverter

A new H-bridge multilevel inverter with a concept called New Hybrid has been discussed in [12]. Basically this topology is meant for electrical vehicle and hybrid electrical vehicle. This cascaded topology has been developed by Selective Harmonic Elimination Pulse Width Modulation method. The DC link voltages for the stages has the link of $3^{S-1}V$ and the number of level can be calculated using the formula 3S. The S mentioned above is equal to the number of stages.

2.2 Reduced Number of Switches

In [13] [14] a new topology has proposed to reduce the number of switches. The proposed topology uses 3 DC sources and 6 switches. Sine wave generated using the multi carrier PWM technique [15]. The proposed topology was compared with conventional seven level seven switch MLI and seven level six switch MLI. The author has discussed about alternative phase opposition disposition (APOD) and Inverter Phase Disposition (IPD). In the results the modulation technique used has reduced the harmonic distortion in the proposed topology compare to conventional seven level topologies.

To reduce the complexity and the cost of the inverter a new topology has discussed in [16] [17]. The complexity and cost reduces as the number of power switches reduces [18]. A new algorithm called Bee algorithm used to find the equations which can be used to identify the switching angle [19] . The results from simulation shows 97.2% efficiency and harmonic distortion below 3%. The designed topology also uses less number of power switches, diodes, and DC voltages and also driver circuits compare to conventional topologies [20].

A new symmetric multilevel inverter topology with less number of switches and also a good stepped sinusoidal output has discussed in [21]. The high switching frequency and low frequency and the voltage levels has been discussed [22]. The author has explained about the Single source sub multilevel inverter and double source sub

multilevel inverter. The equations for the number of levels and the number of IGBT's to be used also stated. The required number of single and double sources varies with the number of DC sources and the equations for the odd and even number has explained well. Having the simulation results and comparing with the other existing topologies this inverter which is the combination of the multi-stepped dc-dc converter and the H-bridge inverter uses less number of switches and also the THD level is reduced.

2.2.1 Single Source Unit

The connection of single voltage source in series with a switch and in parallel with another switch is considered as Single Source Sub Multilevel Inverter. The topology discussed in [23] can be separated into level generator unit and polarity changer. In [24] a new inverter topology discussed which uses only a single DC source. Normal cascade structure uses n number of sources for 2n + 1 levels. Whereas in the structure discussed by using the single source unit and remaining n-1 DC sources being capacitors. From this topology using single source unit the voltage of the capacitors can be controlled and can achieve specified modulation index and also the harmonics can reduced from the output waveform. In [25] the performance and technical aspects of cascaded multilevel inverters were discussed. New topology suggested using single source unit and its advantages such as less number of components, reliability of the proposed structure, reduced switching frequency and electromagnetic interference and removed third harmonics has been discussed.

2.2.2 Double Source Unit

In [26] series connection of sub-multilevel inverter is proposed and the number of switches, standing voltages on the switches and number of dc voltage sources has been analyzed. The topology has approached in both symmetrical and asymmetrical conditions and the simulations outputs has shown. The equations has been developed for the number of switches, levels of the inverter and the number of dc sources to be used [26] [21]. Comparison has made between varieties of dc voltage sources which is an important

parameter to determine the cost of the proposed topology. On the simulation site various modulation techniques has been introduced such as sinusoidal pulse width modulation (SPWM) [27] [28], space vector PWM [15] [29], selective harmonic distortion [30], hybrid modulation [31], hysteresis modulation and fundamental frequency switching.

2.3 Summary

On overall in literature studies the evolution of multilevel inverter that cascaded h-bridge inverter, hybrid h-bridge inverter and new hybrid h-bridge inverter has been discussed. To overcome the drawbacks of conventional inverters many topologies has developed and discussed on cascaded multilevel inverter. Hybrid was developed from the cascaded and it involves the combination of same topology or different topology. However the drawback of hybrid topology where the voltage rating varies for the power switches. The switch reduction also has been discussed to reduce the complexity of the inverter. The single source and double source unit has elaborated and a new better performing topology has developed in this paper.

CHAPTER 3

METHODOLOGY

3.1 Modelling and Operation of Single and Double Source Unit

The modelling and operation of the single and double source unit will be discussed. The basic structure and mathematical expressions will be shown for number of voltage levels (N_{level}), number of switches (N_{switch}) and number of DC voltages (n).

3.2 Modelling of Proposed Topology

In FIGURE 3.1 the voltage source V_1 is connected in series with switch S_1 and parallel with switch P_1. S_1 is considered as voltage adder switch and P_1 is considered voltage subtraction switch. This is classified as single source unit. In FIGURE 3.2 the switch S_1 is connected in series with the dc sources V_1 and V_2 and switch P_1 connected in parallel with both the dc sources. This configuration is referred as double source unit.

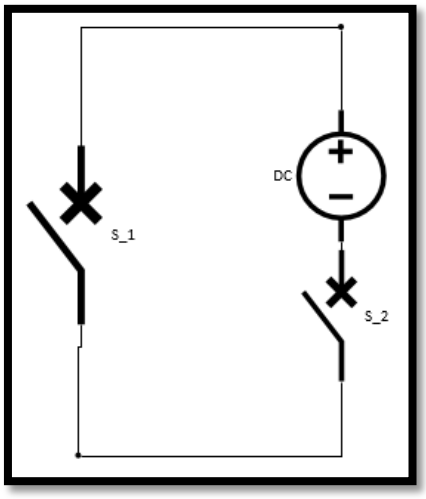

FIGURE 3.1 Single source unit

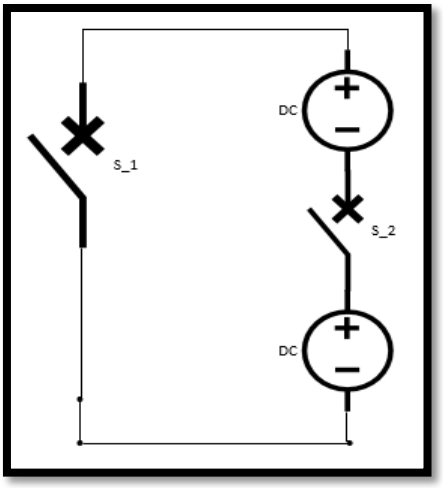

FIGURE 3.2 Double source unit

The number of level

N_{Level} = 2n + 1, n = number of DC sources (1)

Number of switches

$$N_{switch} = \frac{N_{Level}+7}{2} \quad (2)$$

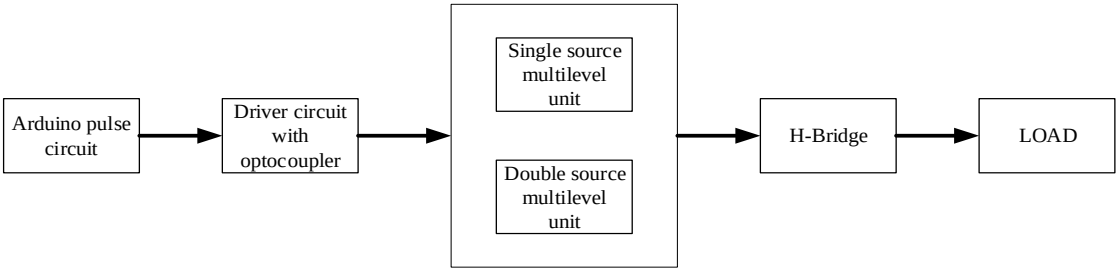

FIGURE 3.3 Proposed topology representation

FIGURE 3.3 shows the overall block diagram of proposed 9 level multilevel inverter. Arduino pulse circuit is connected with driver circuit. Driver circuit developed using optocoupler. Single source sub multilevel inverter (SSSMLI) and double source sub multilevel inverter (DSSMLI) will be connected in series and the circuit called as level generator. The level generator circuit is connected with an H-bridge circuit with a load is called as polarity changer.

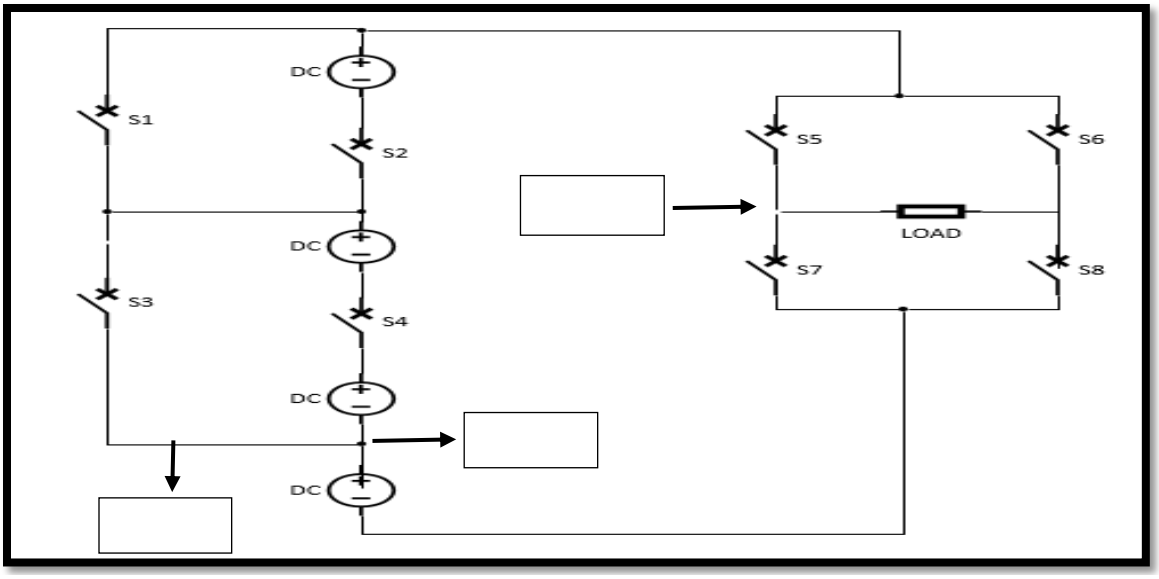

FIGURE 3.4 Circuit diagram of proposed topology

The circuit diagram shown in FIGURE 3.4 illustrates the circuit structure of proposed topology. The labelling S1, S2, S3, S4, S5, S6, S7, S8 denotes the switches used in the structure. While conducting the experimental set up all the switches tested separately to prevent from using any damaged switch. Switch S1 and S3 connected on leg one of the circuit. On the leg 2 switch S2 and S4 connected with 4 6 Volt DC sources. The output of leg 1 and 2 connected to H-bridge circuit which has switch S5, S6, S7, S8 and a load.

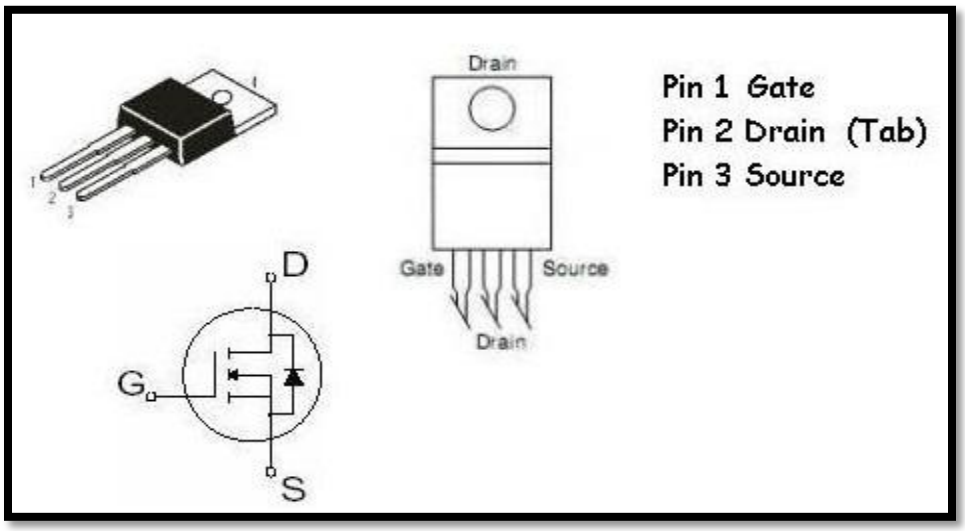

FIGURE 3.5 MOSFET IRF540-N

Basically MOSFET has 3 legs where gate, drain and source. IRF540-N is a forward biased MOSFET. Positive connections will be made at the Drain leg and negative connections will be made at source leg of the MOSFET. The gate leg of the MOSFET will be connected to pulse generator to trigger the MOSFET. The V_{GS} can be supplied up to 33V maximum and V_{GS} can be supplied up to ± 20V. In this project in overall 8 witches need to be used and each switches causes about RM 3.50.

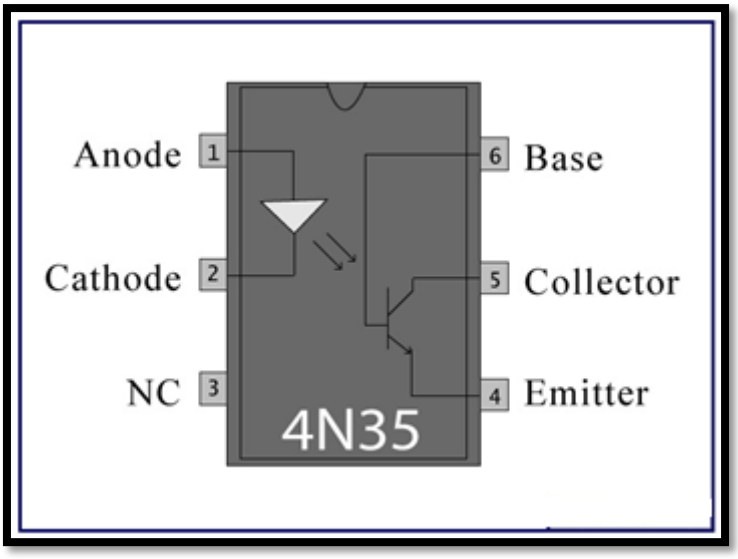

FIGURE 3.6 Optocoupler IC configuration

Optocoupler is the component that used to transfer electrical signal between two isolated circuits by using light. Optocoupler also prevents the system from being damaged by high voltages. In this proposed topology 8 switches will be used. Switching pulse will be generated from Arduino microcontroller and will be connected to all the switches. There is an isolation needed since switching pulse signal will be transmitted from Arduino to main circuit. The optocoupler IC choose for the project is 4N35. It comes with 6 pin. First pin is Anode. The pulse signal from Arduino pin will be connected to the Anode. Cathode pin will be connected to ground of Arduino. 1K Ohm resistor will be connected to positive pin of 9V battery and will be connected to the collector pin of the optocoupler. The negative pin of 9 volt battery will be connected to the Emitter pin of the optocoupler. Gate pin of the MOSFET switch will be connected to

collector of the optocoupler. From Emitter of the optocoupler will be connected to the source of the MOSFET switch.

3.3 Modulation Technique

3.3.1 Pulse Width Modulation Technique

Pulse width modulation signals are continuing pulse with constant frequency and magnitude with various pulse width. The modulating signal decides the magnitude of the pulse. The turning on and off of Power Electronic components such as transistors can be controlled by triggering the gate. The frequency of the PWM signal must be higher than the modulating signal. PWM technique is used in inverters to give a steady output. Pulse Width Modulation has its own advantages such less power dissipation and easily can be implemented and controlled. Moreover, it is compatible with current type microcontroller such Arduino and can generate output voltage without using any additional components and PWM technique helps to reduce lower order harmonics or even can be eliminated and the higher order harmonics can be filtered easily. However PWM technique has its drawbacks as well. The integrated circuit cost is higher for PWM. The complexity of the circuit increase as well. The performance of the circuitry is affected by the radio frequency interference and electromagnetic interference. The continuous and rapid succession of switches can be considered to an impulse.

3.3.2 Sinusoidal Pulse Width Modulation Technique

Sinusoidal pulse width modulation are widely being used in industries. The gate signal can be generated by making comparison between reference sinusoidal signal and triangular carrier wave. The sinusoidal pulse width modulation technique has advantages such as low switching losses, output with less harmonics and easy to implement. There are different type of sinusoidal pulse width modulation method exist and all the methods uses level shifted or phase shifted triangular signals. It uses reference signal which is single sine wave to generate gate signals for respective switches. The intersection of sine

wave with different triangular signals will generate the gate signal. SPWM is not able to produce line to line output voltage as high as the line supply. In order to get a sinusoidal PWM as the output, every small pulsed need to be considered in the modulation where the small pulses can contribute to inverter losses.

3.3.3 Nearest level control

Nearest level control is modulation technique for phase voltage. Nearest level control method differs from other carrier based modulation techniques where this method will not be using any triangular carrier wave whereby it will be calculating the switching states and duty cycle of the converters directly. So the significant difference of this nearest level control method has the advantage of more flexibility and easier implementation when dealing converters with high number of level. Furthermore, the nearest level control method will approximates the reference voltage by two nearest voltage levels instead of one and reduces the harmonics. Nearest level control method more suitable to be used in multiphase multilevel inverter due to its phase voltage modulation approach.

3.4 Tools Required

TABLE 3.1 Tools and Components

Tools	Explanation
Bread board	Using the board for making the connections of the witches.
MOSFET switches	The switch type will be used for the project prototyping.
DC power supply	The voltage source supply for the circuit connection
Oscilloscope	Will be using it to moniter the output wafeform
Multimeter	Will be used for checking current, voltage and component values on the breadboard.
Arduino Uno	Used to give pulse to the MOSFET switches from MATLAB simulation
MATLAB software	Used in doing the simulation work for the proposed topology.

3.5 Gantt Chart

TABLE 3.2 Gantt chart of Project Process

	FYP 1 WEEK													
Activites	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
Selection of Project Topic														
Study on Inverters														
Study on multilevel inverters and its operation														
Analyse the H-bridge inverter operations														
Study on modulation techniques														
Simulation on MATLAB														

	FYP 2 WEEK													
Activites	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
Analyze the simulation results														
Bread board connections for the simulation														
Collection of results														
Validation and Performance Evaluation														
Analysis and discussion of results														
Technical Report														

CHAPTER 4

RESULTS AND DISCUSSION

4.1 Simulation of Single and Double Source Unit Multilevel Inverter

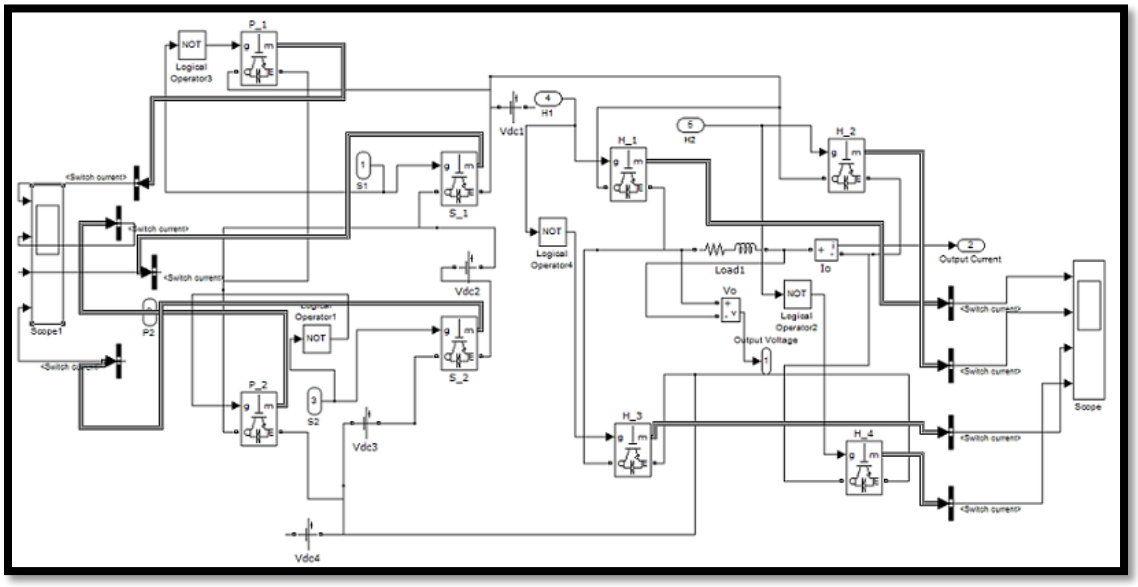

FIGURE 4.1 Simulation circuit for proposed 9 level single and double source unit inverter

FIGURE 4.1 shows the simulation circuit done for the proposed topology. The simulation is done using MATLAB Simulink. 8 MOSFET switches selected from Simulink library and used to simulate the output of proposed topology. 4 main signals used to generate the switching pulse for all the switches. Signal one is directly given to trigger switch S_1. Using not gate, signal one inverted and given to switch P_1. Signal 2

given to the switch S_2. Signal 2 inverted and given to switch P_2. Signal 3 and signal 4 used at the h-bridge side. Signal 3 and inverted signal 3 used to trigger switch H_1 and H_3. The signal 4 used to trigger switch H_2 and H_4.

4.1.1 Output Waveform

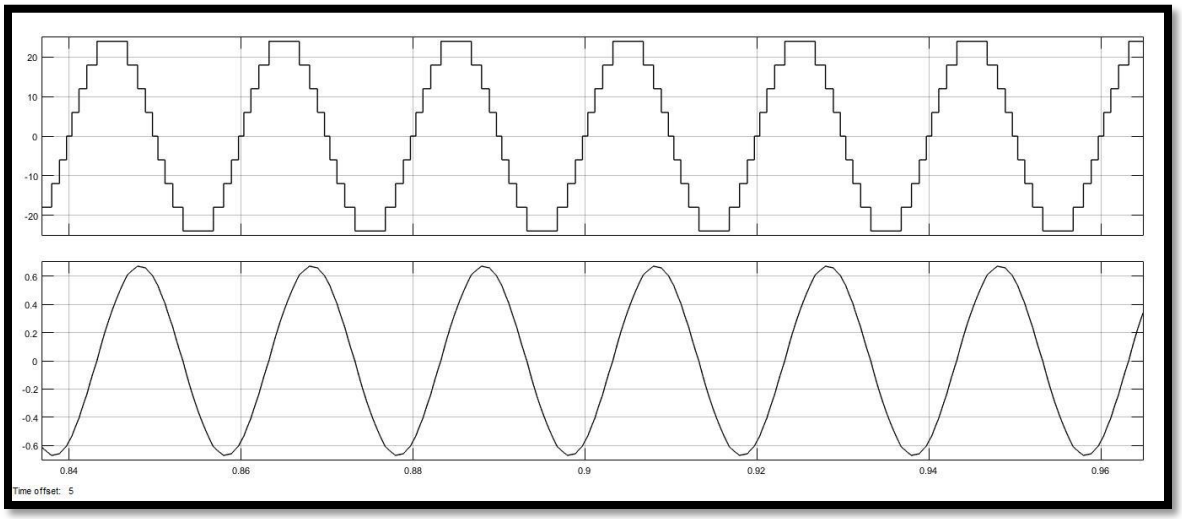

FIGURE 4.2 Simulation output waveform of proposed 9 level single and double source unit inverter

FIGURE 4.2 shows the output waveform that has taken for the simulation work done for the suggested topology. The simulation output shows the 9 level step voltage waveform of the proposed topology. Since 4 six Volt DC sources used the peak to peak voltage positive 24 to negative 24. Load connected on the circuit and the sinusoidal output waveform is generated.

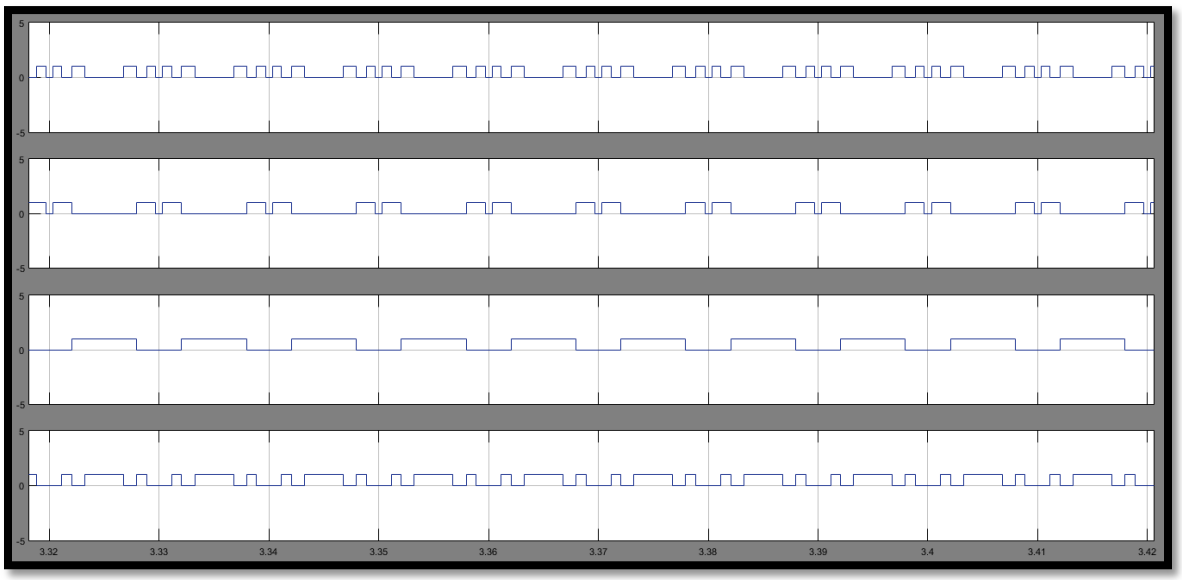

FIGURE 4.3 Voltage across level generator switches

FIGURE 4.4 Current through level generator switches

4.1.2 Total Harmonic Distortion

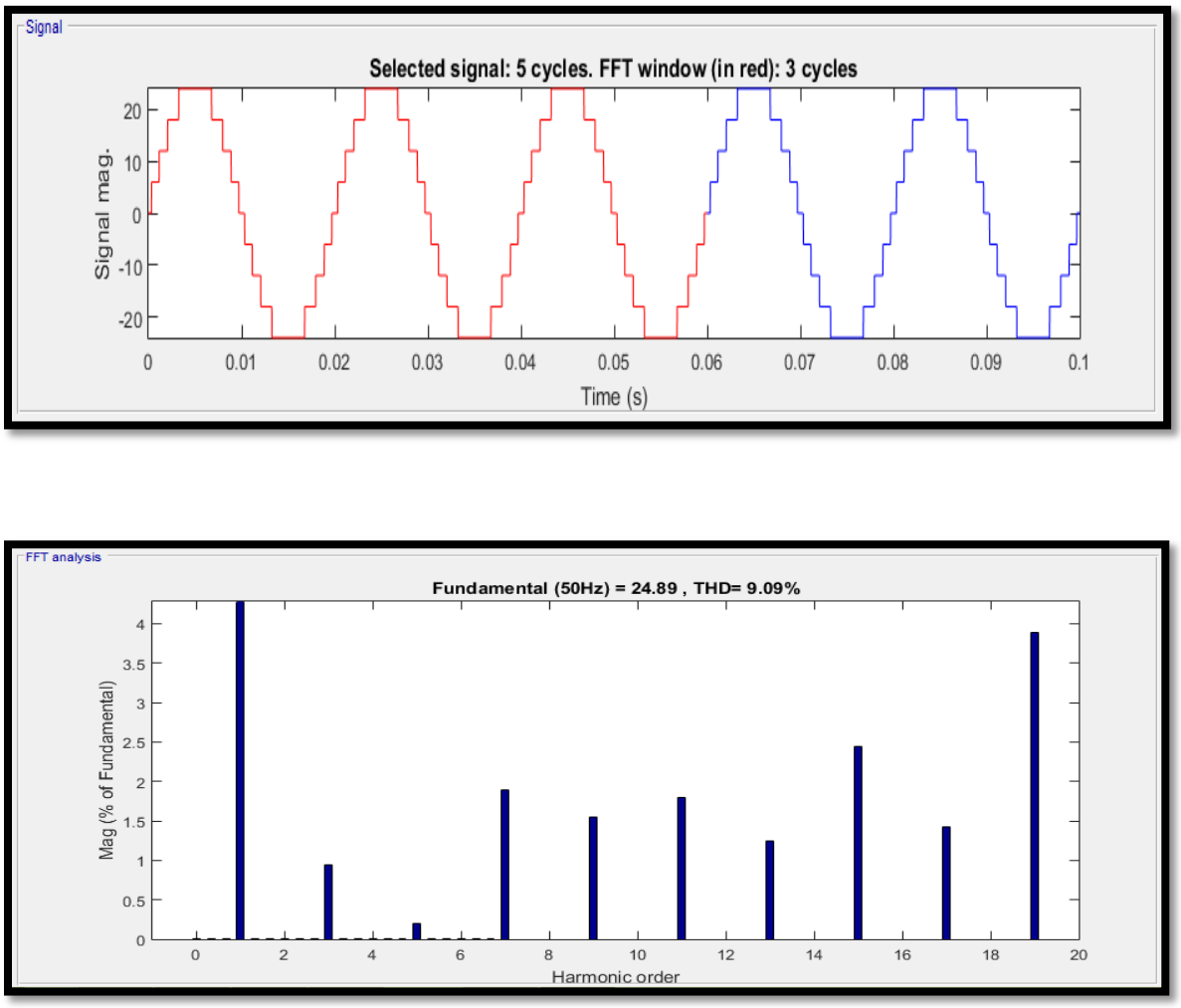

FIGURE 4.5 Simulation of voltage waveform and THD value calculation

As the level of the inverter increase the harmonic distortion will decrease. The harmonic distortion of proposed topology has been compared with [8] [7] [13]. The harmonic distortion value in the proposed topology is lower.

4.1.3 Comparison with other topologies

A comparison has been made with other topologies to show the number of switches used in proposed topology is lesser. The topologies in [13] [17] [32] generate

2n+1 levels for n number of dc source with equal magnitude. The number of switches varies for every topology and it has shown in the comparison chart below. In [27] has used the combination of unidirectional and bidirectional switches. The bidirectional switch usage recquires power diodes and also might increase power electronic component. In [32] this structure generate stepped waveform using n number of dc sources with a multi dc link capacitor. Increase in the number of power diodes and dc link capacitors might cause failure problems and protection steps need to be taken to prevent the diodes and capacitors from being damaged. Power dissipiation and blocking voltages nee to be considered when using more number of power diodes in the circuit structure. Capacitors has to be monitored very frequently where the probability of the capacitors to fail in converters are high. The proposed topology uses only 8 switches which is the lowest compare to other topologies. The cost for the number of MOSFETS used, number of DC source used and number of driver circuit used for every MOSFET is need to counted on overall cost of the proposed topology. The overall cost for the proposed topology is lesser compare to the [32] [17] due to the number of switches used in the proposed topology is lesser compare to the other topologies.

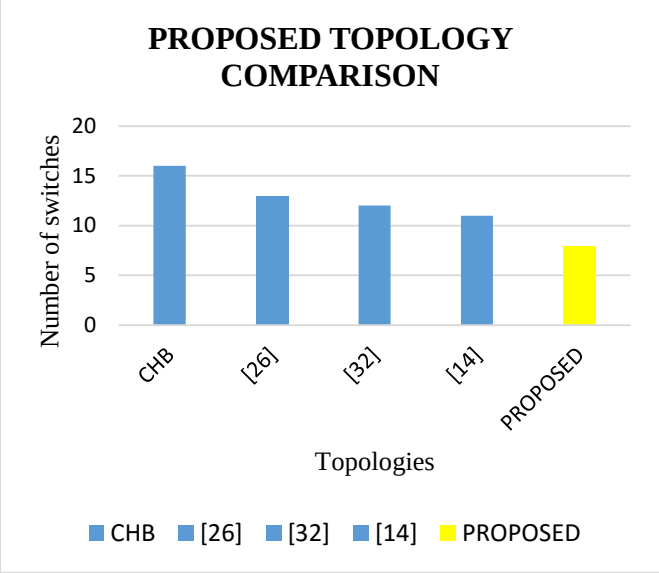

FIGURE 4.6 Comparison of number of switches of proposed topology with other topologies

TABLE 4.1 Perfomance analysis of proposed topology

R (Ω)	L (mH)	V_{rms} (V)	I_{rms} (A)	THD (V) %	P_{in} (W)	P_{out} (W)	η (%)
55	100	14.35	0.28	9.09	33.13	28.82	87.01
60	100	14.35	0.24	9.09	31.09	27.51	88.45
75	100	14.35	0.18	9.09	25.86	23.85	92.21
90	100	14.35	0.15	9.09	22.09	20.83	94.29
100	100	14.35	0.14	9.09	20.05	19.14	95.45

The perfomance of the proposed topology has been analysed with different resistance, inductance. The inductance valaue kept constant and the resistance value increased. The efficiency value calculated using the formula (P_{out} / P_{in}) * 100. As the resistance value increased with the constant iductance the efficiency of the topology increases.

4.2 Experimental Set up Results

The H-bridge connection has done in a breadboard and the output waveform has been captured from ossiloscope.

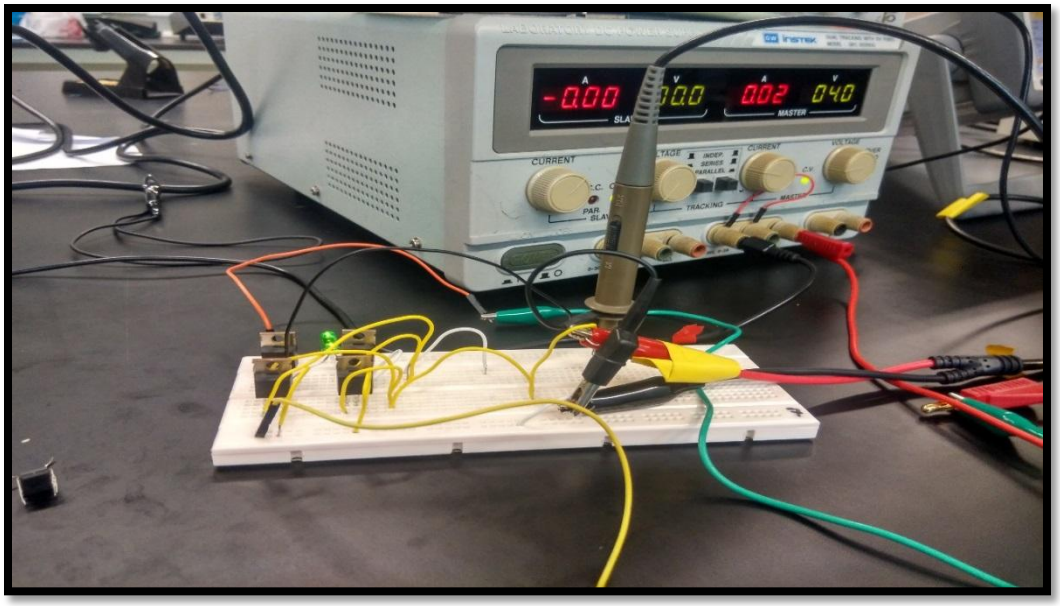

FIGURE 4.7 H-bridge connection

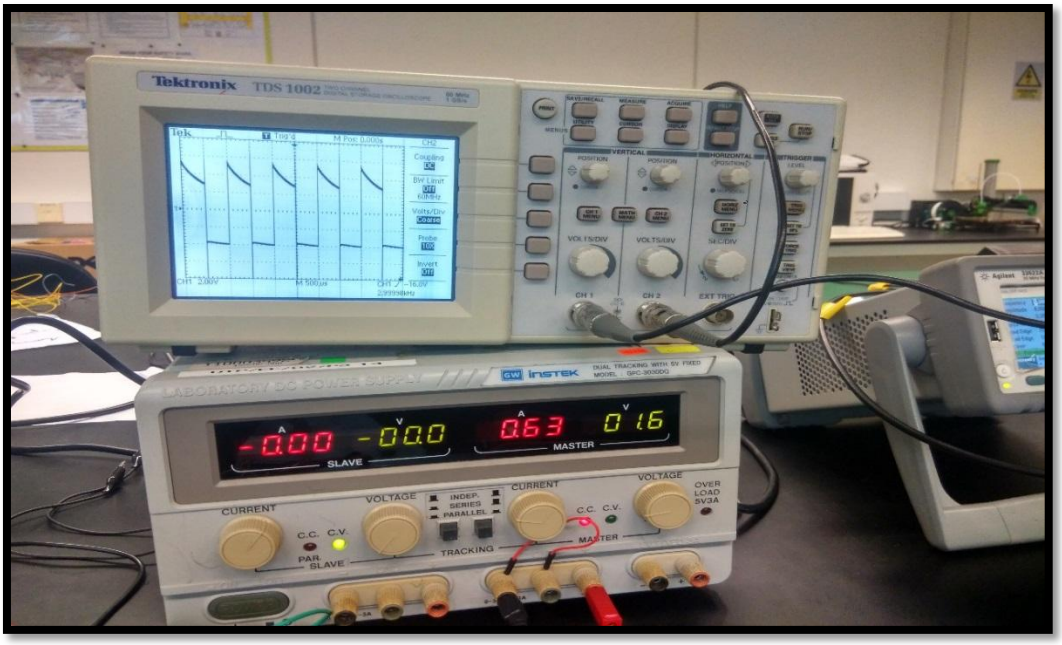

FIGURE 4.8 Square wave form output for H-bridge connection.

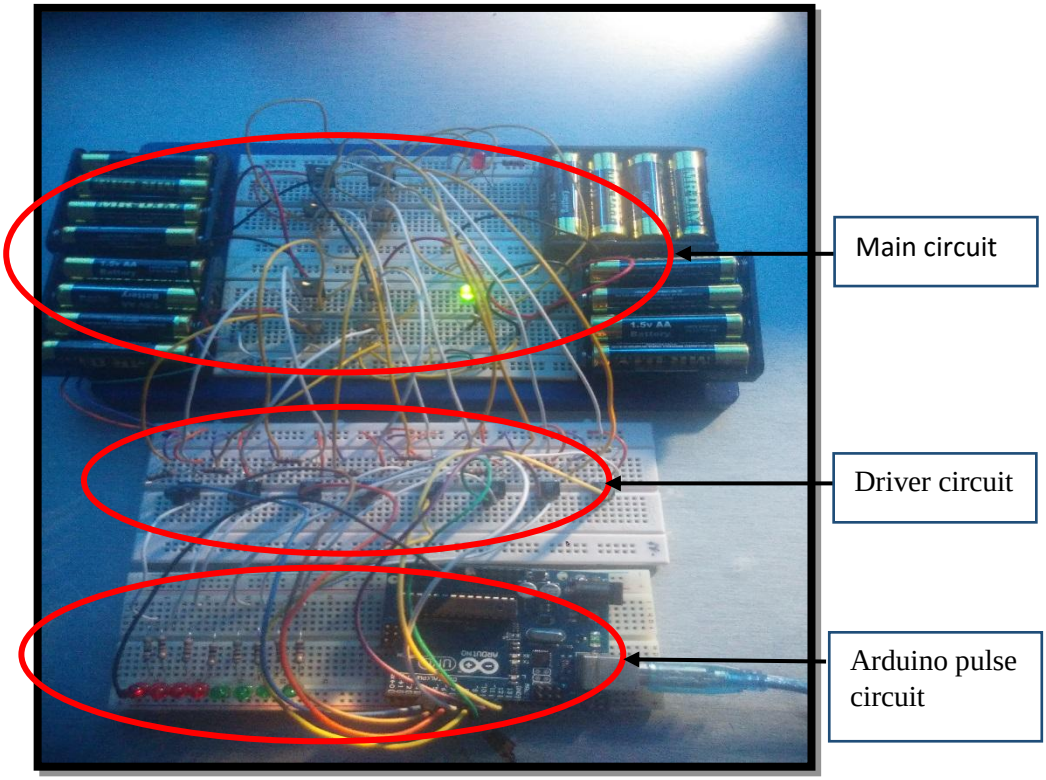

FIGURE 4.9 Experimental set up of proposed topology

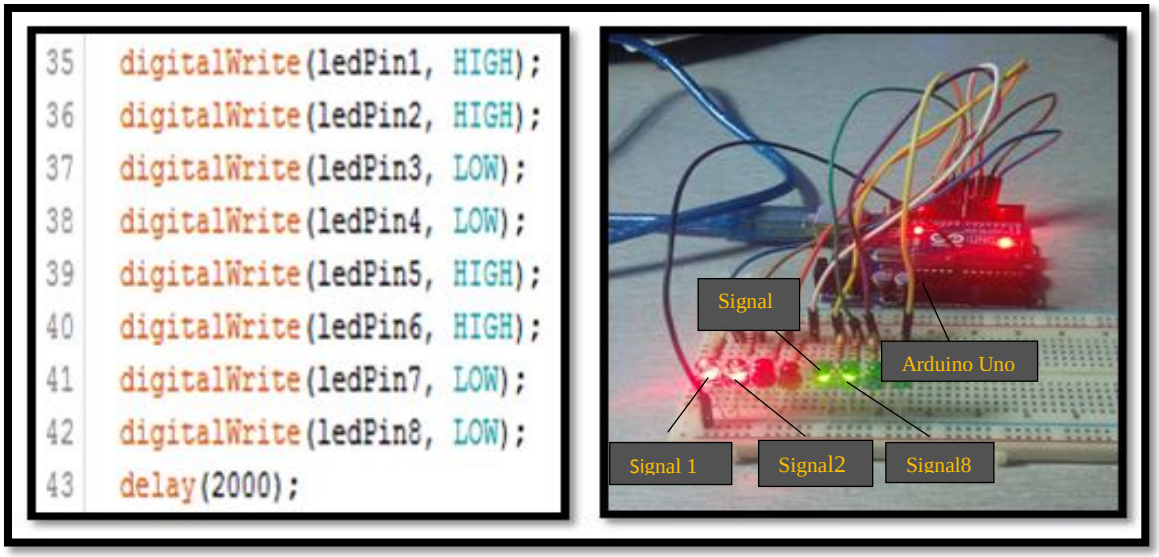

FIGURE 4.10 Arduino pulse for 6V.

FIGURE 4.10 shows the pulse generation signal for positive 6 voltage from Arduino board. LED's used to indicate the signal generation from the arduino board. The signal 1 and signal 2 will be connected to switch 1 and switch 3. Signal 5 will be connected to switch 5 and signal 8 will be given to switch 8 at the H-bridge.

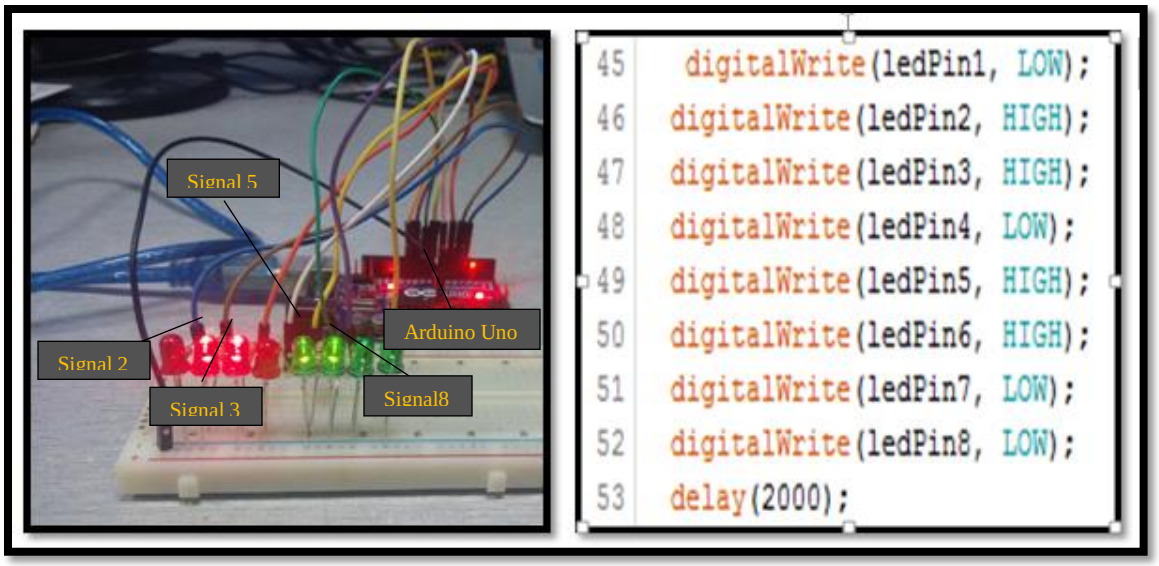

FIGURE 4.11 Arduino pulse for 12 Volt.

FIGURE 4.11 shows the switching pulse to generate 12 Volt. The signal 2 and 3 will be given to the switch 2 and 3 on the level generator side. The signal 5 and 8 ensures the output generation for the positive cycle by triggering the switch 5 and 8.

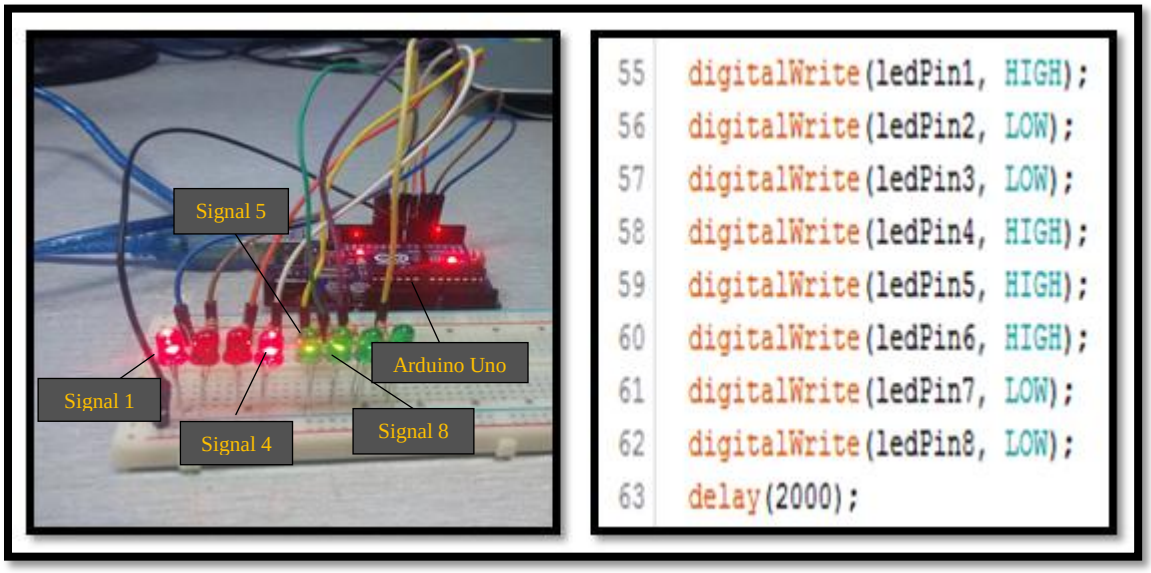

FIGURE 4.12 Arduino pulse for 18 Volt

The signal 1 and signal 4 shown in FIGURE 4.12 will be given to switch 1 and switch 4. The signal 5 and 8 ensures the output generation for the positive cycle by triggering the switch 5 and 8.

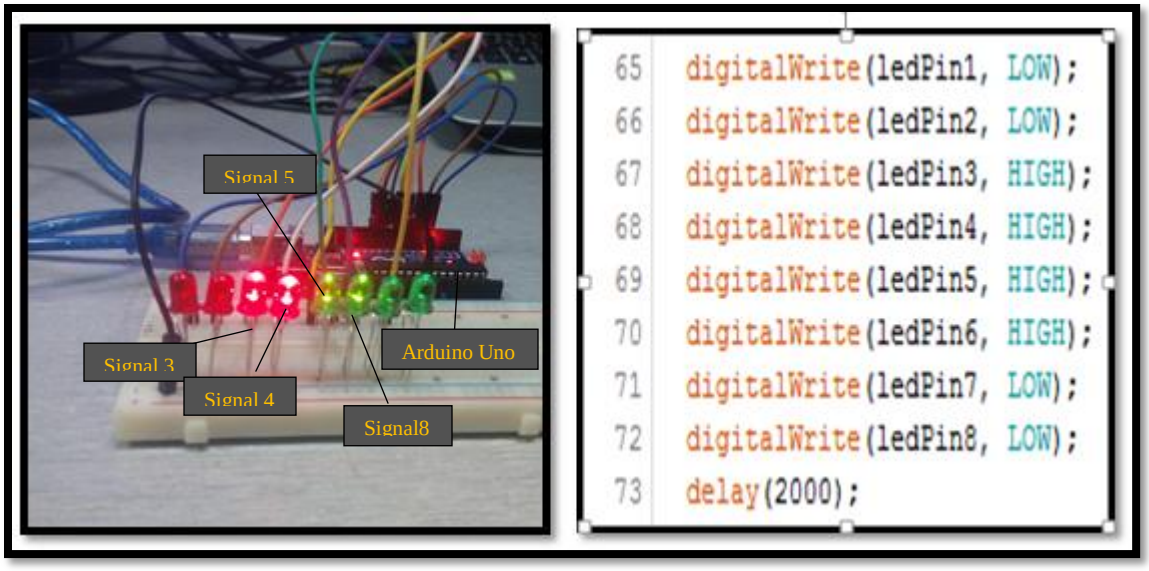

FIGURE 4.13 Arduino pulse for 24 Volt

The signal 3 and signal 4 shown in FIGURE 4.13 will be given to switch 3 and switch 4. The signal 5 and 8 ensures the output generation for the positive cycle by triggering the switch 5 and 8.

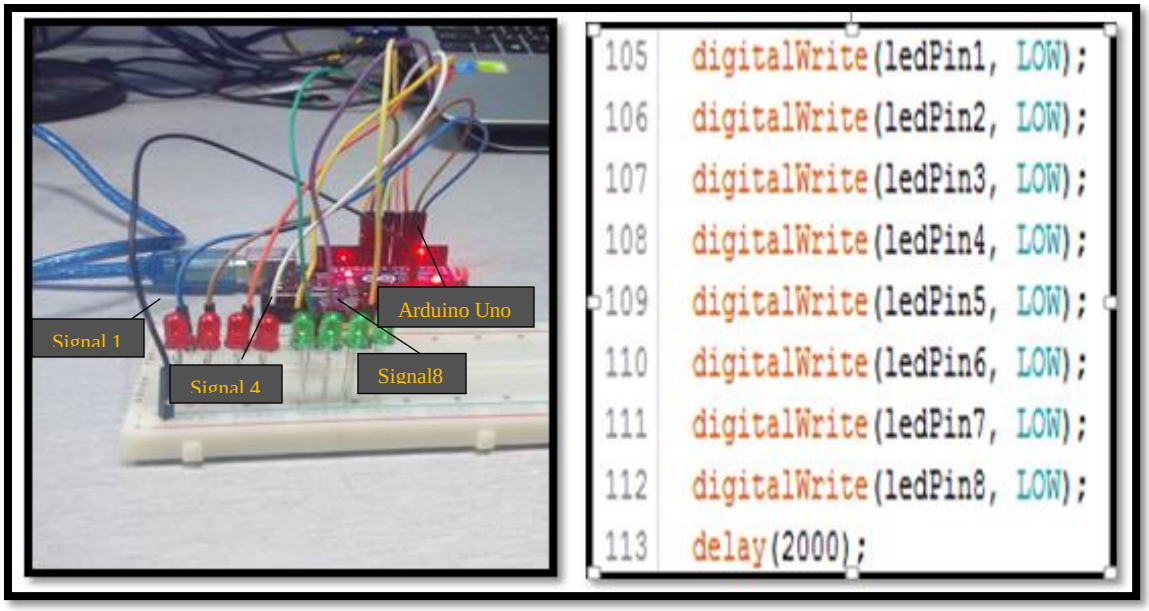

FIGURE 4.14 Arduino pulse for 0 Volt.

For 0 volt there will be no pulse will be generated and given to any switches. All the Arduino pin declared to be in low state in the coding as shown in FIGURE 4.14.

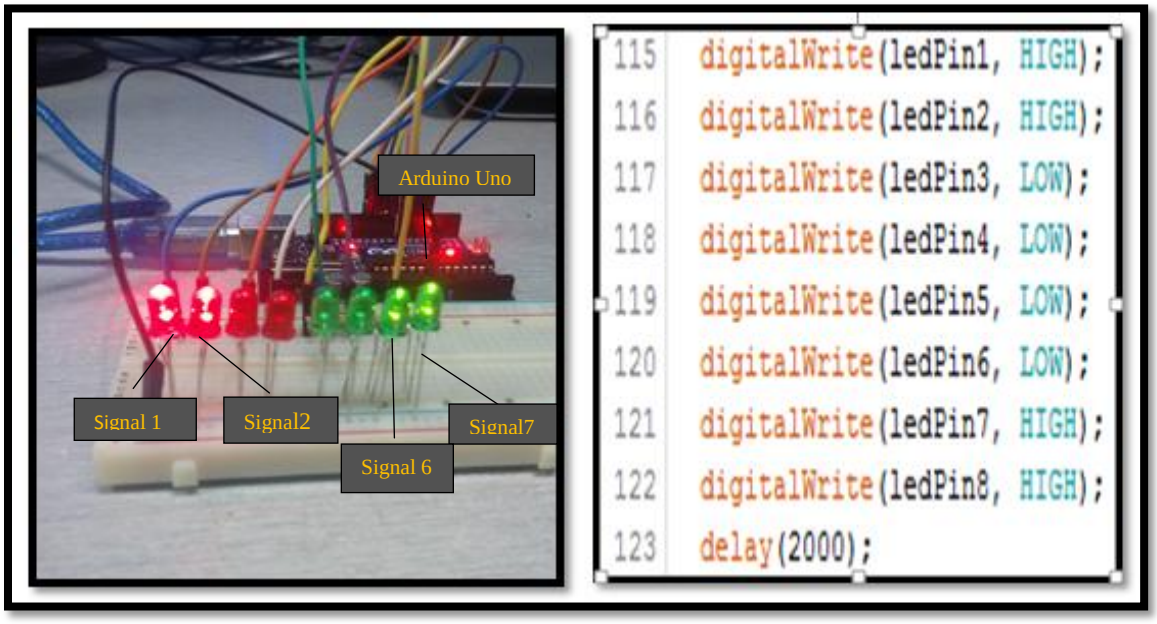

FIGURE 4.15 Arduino pulse for -6V.

FIGURE 4.15 shows the pulse generation signal for negative 6 voltage from Arduino board. LED's used to indicate the signal generation from the arduino board. The signal 1 and signal 2 will be connected to switch 1 and switch 3. Signal 6 will be connected to switch 6 and signal 7 will be given to switch 7 at the H-bridge.

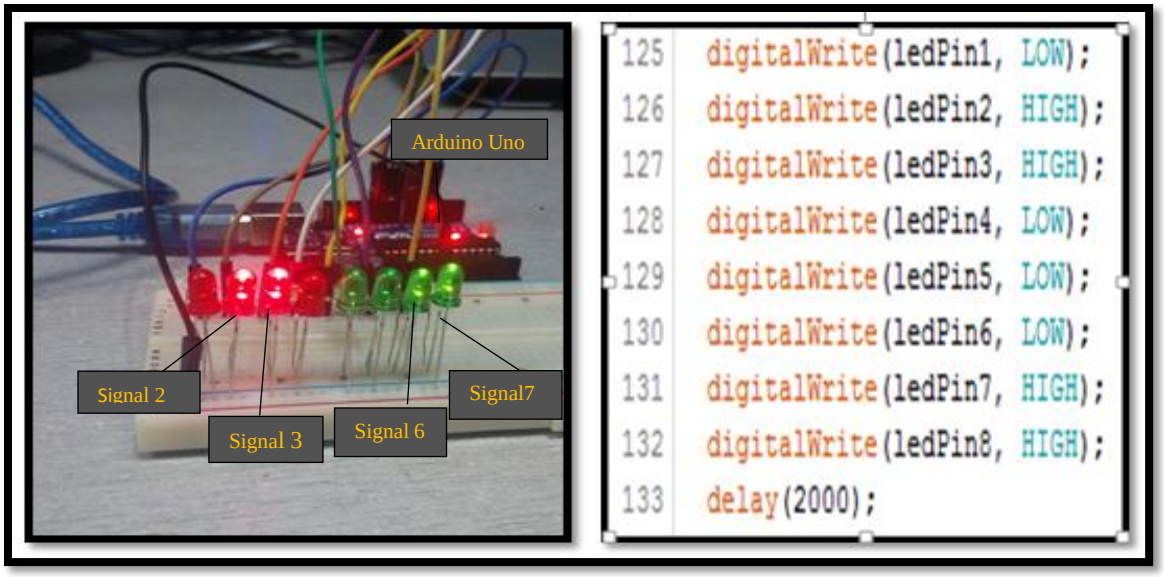

FIGURE 4.16 Arduino pulse for -12 Volt.

FIGURE 4.16 shows the switching pulse to generate -12 Volt. The signal 2 and 3 will be given to the switch 2 and 3 on the level generator side. The signal 6 and 7 ensures the output generation for the positive cycle by triggering the switch 6 and 7.

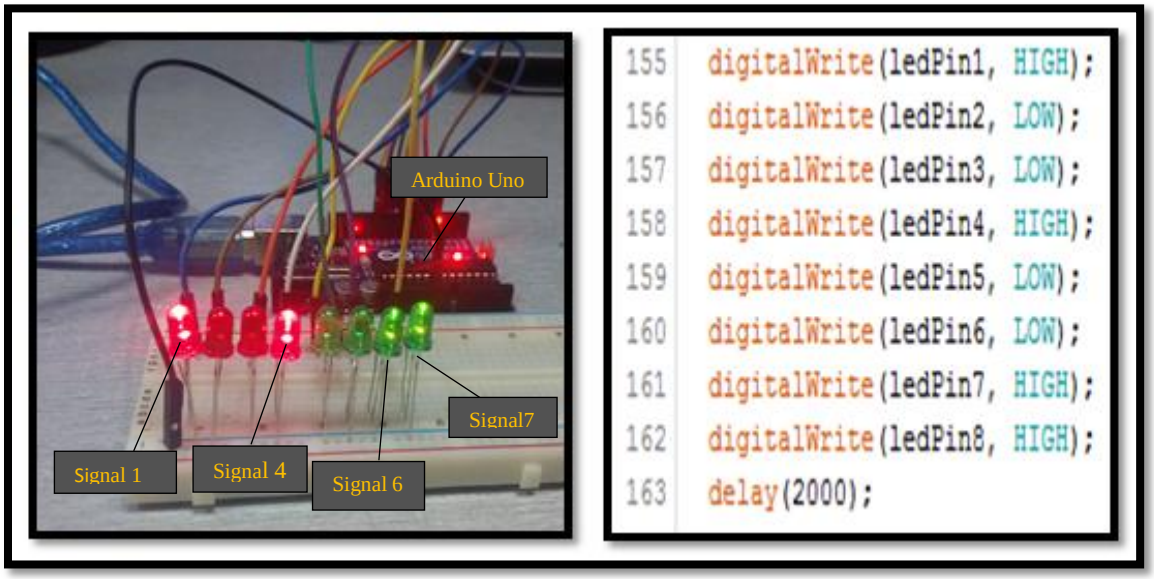

FIGURE 4.17 Arduino pulse for -18 Volt.

The signal 1 and signal 4 shown in FIGURE 4.17 will be given to switch 1 and switch 4. The signal 6 and 7 ensures the output generation for the positive cycle by triggering the switch 6 and 7.

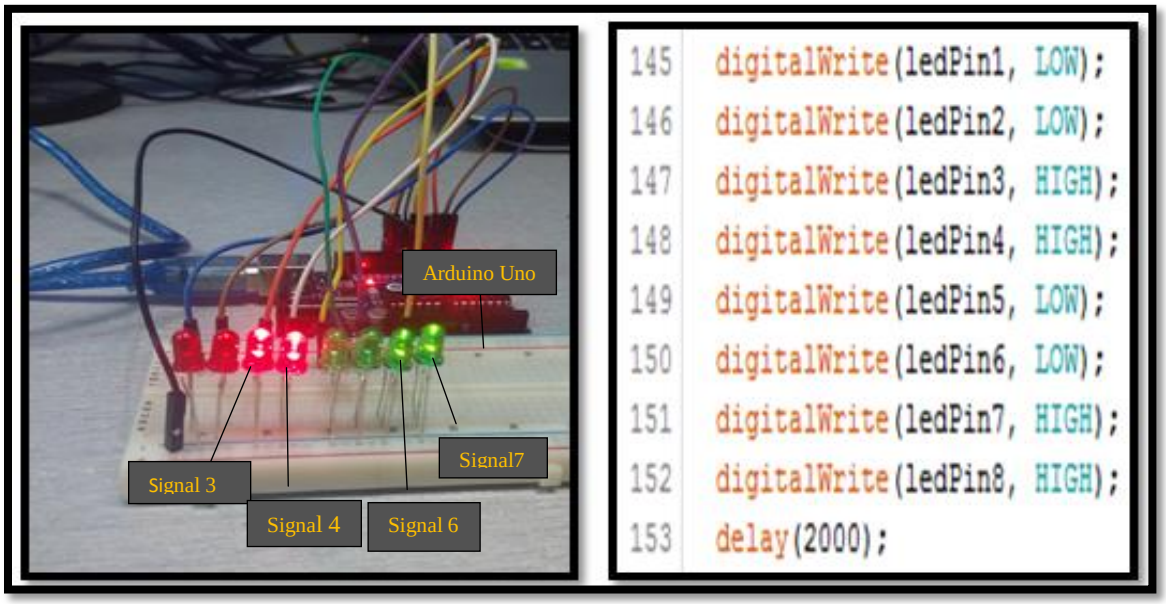

FIGURE 4.18 Arduino pulse for -24 Volt.

The signal 3 and signal 4 shown in FIGURE 4.18 will be given to switch 3 and switch 4. The signal 6 and 7 ensures the output generation for the positive cycle by triggering the switch 6 and 7.

CHAPTER 5

CONCLUSION AND RECOMMENDATION

As per the Gantt chart the literature study on different topologies of multilevel inverter has done. Multilevel inverters are widely being used in power industries and proposing a new topology with increased efficiency and reduced cost is merely going to be a very useful innovation. The introduction towards current existing multilevel inverter topologies with advantages and disadvantages has been discussed and analyzed. A new inverter topology based on single source and double source sub multilevel inverter has been discussed and has shown that the topology produces 2n+1 of levels with n number of dc sources. To show the performance of the topology simulation has done in MATLAB/Simulink and the output waveforms has been discussed in the report. On overall, the number of power switches used has been reduced in the proposed topology. The FFT analysis has been done and the THD level produced for the proposed topology is lower compare to other topologies. The complexity of the circuit and manufacturing cost reduces as the number of power switches reduced. Improved efficiency and reduced THD value is the major advantage of the proposed topology and it is more reliable to use in medium power applications. This project even can be enhanced to be used in high power applications by cascading the proposed topology. Apart from that in this project 6 volt batteries are used as separate dc sources. This can be improved with some renewable energy sources such as PV arrays. The proposed topology can be enhanced by implementing with different type of loads such as nonlinear and motors.

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APPENDICES

```
int ledPin1 = 4;

int ledPin2= 5;

int ledPin3 = 6;

int ledPin4 = 7;

int ledPin5 = 8;

int ledPin6 = 9;

int ledPin7 = 10;

int ledPin8 = 11;



void setup()

{

  pinMode(ledPin1, OUTPUT);

  pinMode(ledPin2, OUTPUT);

  pinMode(ledPin3, OUTPUT);

  pinMode(ledPin4, OUTPUT);

  pinMode(ledPin5, OUTPUT);

  pinMode(ledPin6, OUTPUT);

  pinMode(ledPin7, OUTPUT);
```

```
  pinMode(ledPin8, OUTPUT);
}

void loop()
{
  digitalWrite(ledPin1, LOW);
  digitalWrite(ledPin2, LOW);
  digitalWrite(ledPin3, LOW);
  digitalWrite(ledPin4, LOW);
  digitalWrite(ledPin5, LOW);
  digitalWrite(ledPin6, LOW);
  digitalWrite(ledPin7, LOW);
  digitalWrite(ledPin8, LOW);
  delay(2000);

  digitalWrite(ledPin1, HIGH);
  digitalWrite(ledPin2, HIGH);
  digitalWrite(ledPin3, LOW);
  digitalWrite(ledPin4, LOW);
  digitalWrite(ledPin5, HIGH);
  digitalWrite(ledPin6, HIGH);
  digitalWrite(ledPin7, LOW);
  digitalWrite(ledPin8, LOW);
```

```
delay(2000);

 digitalWrite(ledPin1, LOW);
digitalWrite(ledPin2, HIGH);
digitalWrite(ledPin3, HIGH);
digitalWrite(ledPin4, LOW);
digitalWrite(ledPin5, HIGH);
digitalWrite(ledPin6, HIGH);
digitalWrite(ledPin7, LOW);
digitalWrite(ledPin8, LOW);
delay(2000);

digitalWrite(ledPin1, HIGH);
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digitalWrite(ledPin5, HIGH);
digitalWrite(ledPin6, HIGH);
digitalWrite(ledPin7, LOW);
digitalWrite(ledPin8, LOW);
delay(2000);

digitalWrite(ledPin1, LOW);
```

```
digitalWrite(ledPin2, LOW);
digitalWrite(ledPin3, HIGH);
digitalWrite(ledPin4, HIGH);
digitalWrite(ledPin5, HIGH);
digitalWrite(ledPin6, HIGH);
digitalWrite(ledPin7, LOW);
digitalWrite(ledPin8, LOW);
delay(2000);

digitalWrite(ledPin1, HIGH);
digitalWrite(ledPin2, LOW);
digitalWrite(ledPin3, LOW);
digitalWrite(ledPin4, HIGH);
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digitalWrite(ledPin7, LOW);
digitalWrite(ledPin8, LOW);
delay(2000);

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digitalWrite(ledPin3, HIGH);
digitalWrite(ledPin4, LOW);
```

```
digitalWrite(ledPin5, HIGH);
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delay(2000);

digitalWrite(ledPin1, HIGH);
digitalWrite(ledPin2, HIGH);
digitalWrite(ledPin3, LOW);
digitalWrite(ledPin4, LOW);
digitalWrite(ledPin5, HIGH);
digitalWrite(ledPin6, HIGH);
digitalWrite(ledPin7, LOW);
digitalWrite(ledPin8, LOW);
delay(2000);

digitalWrite(ledPin1, LOW);
digitalWrite(ledPin2, LOW);
digitalWrite(ledPin3, LOW);
digitalWrite(ledPin4, LOW);
digitalWrite(ledPin5, LOW);
digitalWrite(ledPin6, LOW);
digitalWrite(ledPin7, LOW);
```

```
digitalWrite(ledPin8, LOW);
delay(2000);

digitalWrite(ledPin1, HIGH);
digitalWrite(ledPin2, HIGH);
digitalWrite(ledPin3, LOW);
digitalWrite(ledPin4, LOW);
digitalWrite(ledPin5, LOW);
digitalWrite(ledPin6, LOW);
digitalWrite(ledPin7, HIGH);
digitalWrite(ledPin8, HIGH);
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digitalWrite(ledPin1, LOW);
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digitalWrite(ledPin8, HIGH);
delay(2000);
```

```
digitalWrite(ledPin1, HIGH);
digitalWrite(ledPin2, LOW);
digitalWrite(ledPin3, LOW);
digitalWrite(ledPin4, HIGH);
digitalWrite(ledPin5, LOW);
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digitalWrite(ledPin8, HIGH);
delay(2000);

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digitalWrite(ledPin2, LOW);
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digitalWrite(ledPin5, LOW);
digitalWrite(ledPin6, LOW);
digitalWrite(ledPin7, HIGH);
digitalWrite(ledPin8, HIGH);
delay(2000);

digitalWrite(ledPin1, HIGH);
digitalWrite(ledPin2, LOW);
digitalWrite(ledPin3, LOW);
```

```
digitalWrite(ledPin4, HIGH);
digitalWrite(ledPin5, LOW);
digitalWrite(ledPin6, LOW);
digitalWrite(ledPin7, HIGH);
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digitalWrite(ledPin5, LOW);
digitalWrite(ledPin6, LOW);
digitalWrite(ledPin7, HIGH);
digitalWrite(ledPin8, HIGH);
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digitalWrite(ledPin2, HIGH);
digitalWrite(ledPin3, LOW);
digitalWrite(ledPin4, LOW);
digitalWrite(ledPin5, LOW);
digitalWrite(ledPin6, LOW);
```

```
  digitalWrite(ledPin7, HIGH);
  digitalWrite(ledPin8, HIGH);
  delay(2000);


}
```