Prediction of Peak Junction Temperature of Semiconductor Devices: A Simulation Study

by

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16053

Dissertation submitted in partial fulfillment of
the requirements for the
Bachelor of Engineering (Hons)
(Electrical & Electronics)

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CERTIFICATION OF APPROVAL

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Approved by,

_____
(Dr. Mohana Sundaram Muthuvalu)

UNIVERSITI TEKNOLOGI PETRONAS

SERI ISKANDAR, PERAK

January 2016

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

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NOR ATIQAH BINTI MOHD SUHAIMI

ABSTRACT

Thermal effects have become increasingly important as devices get smaller on-chip. Components temperature on Printed Circuit Board (PCB) will increase due to the thermal interaction between the components, thus, effects its performance. The concern on reliability and performance of the semiconductor devices is one of the main things that the designers should take into account. Due to this problem, thermal control system can be used in order to achieve high performance of electronic system. In this project, it will focus on discretizing two-dimensional heat conduction equation using numerical approach to predict the peak junction temperature of semiconductor devices. The numerical approach will be divided into two main stages. For the first stage, Backward Time, Centered Space (BTCS) finite difference is used to discretize two-dimensional heat conduction equation. Next, presented models will leads to a linear system that is solved by using Gauss-Seidel (GS) and Successive Over Relaxation (SOR) iterative methods. The material, Silicon (Si) will be tested under the adiabatic condition where it allows testing the performance of the die with no heat transfer with the surroundings. Based on numerical results obtained, it clearly shows that the application of SOR method reduce the number of iterations and computational time compared to GS method. Both methods give same maximum temperature and these temperatures are comparable with the result obtained by using *pdepe* tool.

ACKNOWLEDGEMENT

It would not have been possible to write this dissertation without the assistance and support of so many people whose names may not all enumerated.

First of all I would like to be grateful to Allah S.W.T for giving me chance to gain knowledge and give me strength to finish this final year project.

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Lastly, I want to express my gratefulness to my family and friends for their continuous support, either morally, financially and physically which driven me to complete this project.

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ABBREVIATIONS AND NOMENCLATURES

ASM	Academy of Science Malaysia
MOSTI	Ministry of Science, Technology and Innovation
IC	Integrated Circuit
PCB	Printed Circuit Board
IR	Infrared
FDM	Finite-Difference Method
BTCS	Backward Time, Centered Space
FEM	Finite Element Method
BEM	Boundary Element Method
IEM	Integral Equation Method
PDE	Partial Differential Equation
GS	Gauss-Seidel
SOR	Successive Over Relaxation
T	Temperature Distribution
K_x	Thermal Conductivity in *x*-direction
K_y	Thermal Conductivity in *y*-direction
ρ	Material Density
c_p	Specific Heat Capacity
x	*x*-axis
y	*y*-axis
t	Time
L	Length of the die size
Δx	Step size in *x*-axis
Δy	Step size in *y*-axis
Δt	Step size in *t*

CHAPTER 1

INTRODUCTION

1.1 Background of Study

Academy of Science Malaysia (ASM) is a legal body built up by an Act of Parliament in 1995 and placed under the Ministry of Science, Technology and Innovation (MOSTI). ASM believes that the Science, Engineering and Technology industries can contribute enormously to the future advancement of Malaysia. So that, ASM conduct a Flagship Study entitled "The Mega Science Agenda – Malaysia 2050" on 2009. As part of the Mega Science 2050 Agenda, one of the main sectors that had been identified for second stage implementation (2014-2015) is Mega Science 2.0: Electrical and Electronics Sector. In this sector, it focuses on Malaysia's cooperation in the compound semiconductor industry. This industry will keep on developing due to high demand on high power applications, smartphones and the telecommunication industries [1].

High power is usually encountered in a power device application and it is important to make power devices reliable for their intended application. In order to achieve this goal, reliability and performance must be considered. For semiconductors devices, the basic nature of the hardware is they will leave no room for failure. It is a designer's job to properly designed semiconductor devices, so that it will increase the life expectancy of the equipment. Careful processing also will ensure that each device meets the designed specification [2].

The reliability and performance of semiconductor devices depend on their resistance to stresses applied to the devices. Stress factors affecting the device reliability includes

mechanical stress, electrical stress, thermal stress, environmental stress, and external stress. If a device has a specifically weak structure part, the weak part may extremely react to the stress applied to the device, and such an extreme reaction may results serious failures [3]. Junction temperature is the highest operating temperature of semiconductor device. In order to determine the reliability and performance of semiconductor devices, junction temperature is a very important parameter that must be measured, especially to determine power devices reliability [4].

Generally, semiconductor devices such as Integrated Circuit (IC) will be installed onto a Printed Circuit Board (PCB). PCB is a board that has lines and pads that electrically connect the various connectors and components to each other (refer Figure 1.1). Figure 1.2 shows IC die mounted on PCB illustration and epoxy is used as component body.

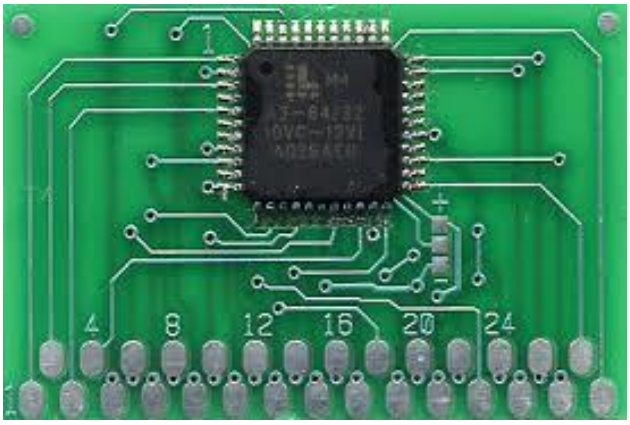

FIGURE 1.1 Printed Circuit Board (PCB) (source: [5])

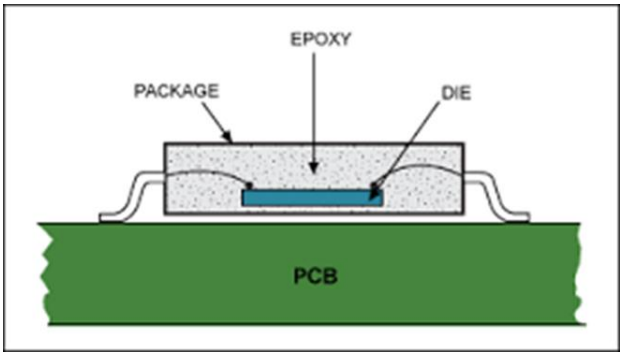

FIGURE 1.2 Silicon die mounted on PCB (source: [6])

1.2 Problem Statement

Nowadays, with the trends towards devices miniaturization combine with system reliability and performance increasing demand, thermal consideration has become a very important aspect in electronic packaging design [7]. Most researchers perceive heat management as the critical problem, as it may cause the devices to degrade permanently or even fail. Therefore, consideration has to be taken regarding the maximum operating junction temperature of the semiconductor devices in order to determine the reliability of semiconductor, thus, preventing thermal failure and extending electronic package life time. Current semiconductor temperature monitoring tools is by using temperature sensor. However, in this study, mathematical modeling is used to predict IC junction temperature so that it can monitor the temperature of semiconductor. Two-dimensional heat conduction equation will be used to predict IC junction temperature as shown below

$$\frac{\partial}{\partial x}\left(K_x \frac{\partial T}{\partial x}\right)+\frac{\partial}{\partial y}\left(K_y \frac{\partial T}{\partial y}\right)=\rho c \frac{\partial T}{\partial t}. \tag{1}$$

For constant thermal conductivity, the equation is shown below

$$K\left(\frac{\partial^2 T}{\partial x^2}+\frac{\partial^2 T}{\partial y^2}\right)=\rho c \frac{\partial T}{\partial t} \tag{2}$$

where T, K_x and K_y represent temperature distribution, thermal conductivity in the *x*-direction and thermal conductivity in the *y*-direction, respectively. Meanwhile, ρ and c represent silicon mass density and specific heat respectively [8].

The equations (1) and (2) satisfy the following boundary equation

$$T(L,t)=T_{in}, \quad t>0 \tag{3}$$

where L and T_{in} are thickness of vertical power device and input temperature respectively [9].

1.3 Objectives of Study

The main objectives of this study are:

1) To develop the algorithm of thermal modeling by solving the governing heat conduction equation by using numerical techniques.
2) To validate the performance of GS and SOR methods in solving the governing heat conduction equation.
3) To validate the results of peak junction temperature based on GS and SOR methods compared with *pdepe* tool.

1.4 Scope of Study

In this study, numerical techniques and *pdepe* tool in MATLAB R2013 will be used to predict IC peak junction temperature. Steady state thermal characteristic is analyzed by discretizing the governing two-dimensional heat conduction equation via Finite-Difference Method (FDM) scheme i.e Backward Time, Centered Space. The equation will be addressed under adiabatic condition where the heat generated and the heat transferred in will be neglected. The heat conduction equation also satisfies boundary condition (i.e. equation (3)) and initial condition (room temperature). After discretization, it will lead to a linear system. Thereafter, GS and SOR methods will be applied to obtain the peak junction temperature of semiconductor devices on PCB. Material properties used in this project is Silicon (Si) which is most commonly used material in die fabrication.

CHAPTER 2

LITERATURE REVIEW

2.1 Thermal Analysis

System designers and board designers need to design their PCBs to handle the heat produced due to power utilization in the ICs. When a device is running, it utilizes electrical energy that is converted into heat. A good understanding of thermal resistance and its implication on power dissipation and heat generation is necessary. This knowledge allows designers to determine the requirements of PCB layout and system requirement. Therefore, it can prevent both overheating of the board and catastrophic IC failure ([2], [10], [11]).

The peak junction temperature (T_{JPEAK}) is the highest temperature on the semiconductor devices due to power dissipation internal applied to the devices. Usually, T_{JPEAK} depends on the reliability of the die used in the manufacturing process. In [10] and [11], the following equation is used to determine the junction temperature, T_J and peak junction temperature, T_{JPEAK}

$$T_J = T_A + \theta_{JA} P_D \tag{4}$$

$$T_{JPEAK} = T_A + \theta_{JA} P_{DMAX} \tag{5}$$

where T_A, θ_{JA}, P_D and P_{DMAX} represent ambient temperature, thermal resistance, power dissipation and maximum power dissipation respectively.

As shown in Figure 2.1, the junction temperature is the hottest temperature on the IC due to its power dissipation during operation.

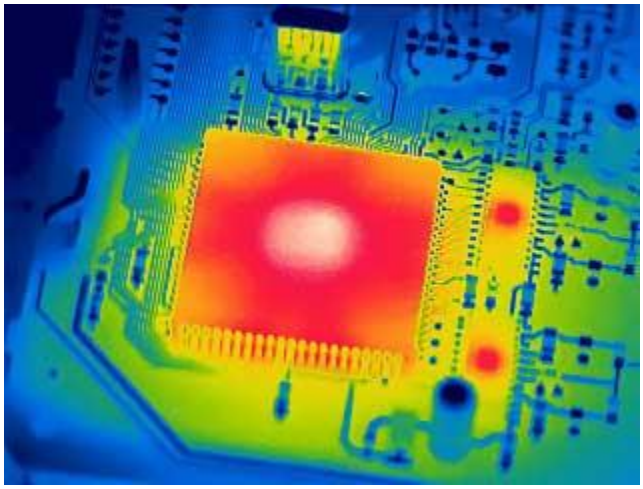

FIGURE 2.1 IC Die Temperature using IR Camera (source: [12])

There are three accurate methods to determine the junction temperature of a component during operation in a real system [12]

1) Measure the silicon die temperature on the component itself,
2) Measure the component's case temperature, and
3) Measure the board temperature which the components are attached.

Figure 2.2 provides the measurement of thermal parameters on the IC die. Meanwhile, Figure 2.3 and Figure 2.4 provide measurement of the case temperature and board temperature.

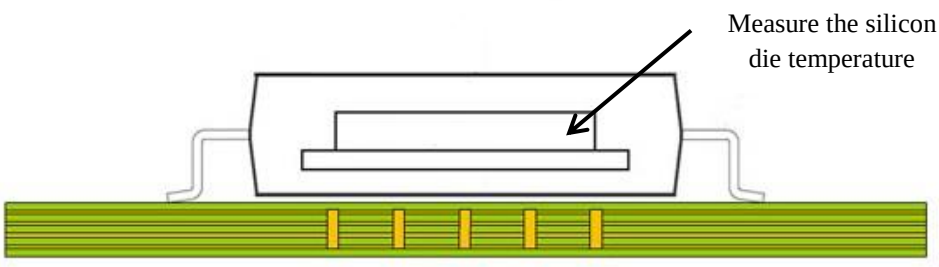

FIGURE 2.2 Location of IC die temperature measurement points (source: [12])

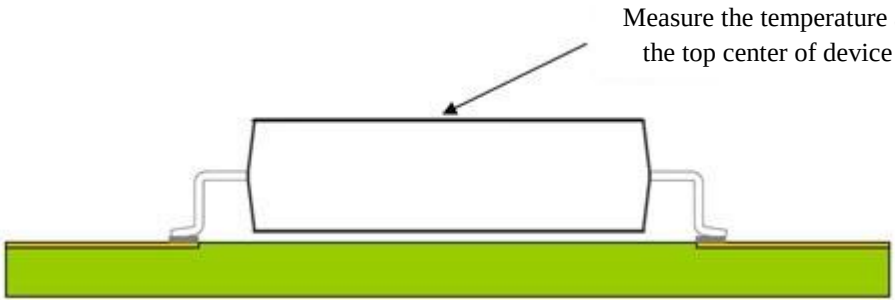

FIGURE 2.3 Location of case temperature measurement points (source: [12])

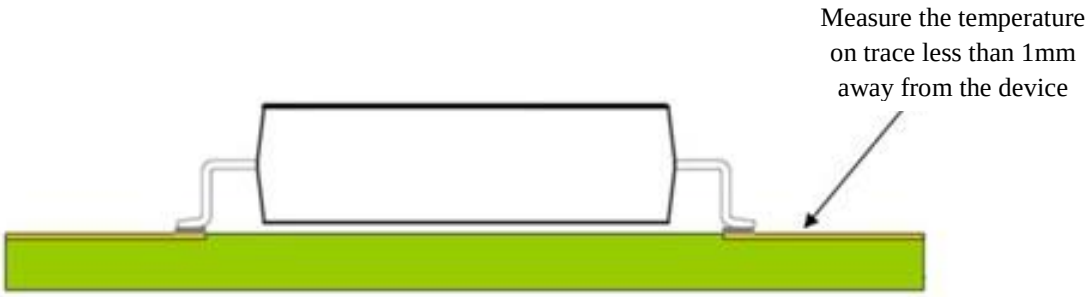

FIGURE 2.4 Location of board temperature measurement points (source: [12])

There is two type of thermal analysis that is commonly used which are steady state (static) and dynamic state (unsteady state). In [17], steady state analysis define the temperature profile, thermal conductivity profile and given power. Meanwhile, dynamic state defines the temperature profile with an initial temperature, thermal conductivity profile and heat capacity.

2.2 Monitoring Tools

Every process step in silicon die fabrication depends on the measurement and control of die temperature. As die sizes increase, the cost of each die grows and the value of high quality in-process temperature monitoring becomes critical. Inadequate control of die temperature during processing reduces fabrication yields and directly translates to lost revenues [19]. Current semiconductor temperature monitoring tools is by using temperature sensor. The most popular temperature sensors used today are the

Thermocouple, Resistive Temperature Device (RTD), Thermistor, and the newest technology, the Integrated Silicon Based Sensors. Each of these sensor technologies cater to specific temperature ranges and environmental conditions. The sensor's temperature range, ruggedness, and sensitivity are just a few characteristics that are used to determine whether or not the device will satisfy the requirements of the application [20]. Nevertheless, all of these sensors are real-time temperature monitoring tools. The sensor can only detect the temperature at actual time during which a process occurs. However, by using mathematical modeling, the temperature at real time and after certain time can be estimated.

2.3 Mathematical Modeling

The mathematical modeling can be used to determine the peak junction temperature. Different researcher has their own thermal modeling techniques to determine the junction temperature of semiconductor devices on PCB. Ghaffar *et al*. [9] assumed that the silicon thermal characteristic to be independent of temperature. So, the proposed model of thermal system is governed by one dimensional parabolic differential equation as shown below

$$K\frac{\partial^2 T}{\partial x^2} = \rho c\frac{\partial T}{\partial t}\ ,\ 0 < x < L\ ,\ t > 0 \tag{6}$$

where T, K, ρ, c and L represent temperature distribution, thermal conductivity, mass density, specific heat material and thickness of vertical device respectively.

Meanwhile, the equation (7) represents initial condition and equations (8) and (9) represent boundary condition respectively

$$T(x,0) = 300.15K \tag{7}$$

$$SK\frac{\partial T}{\partial x}\bigg|_{x=0} = -P_{in} \tag{8}$$

and

$$T(L,t) = T_{in}, \quad t > 0 \tag{9}$$

where S, T_{in} and P_{in} represent semiconductor area, input temperature and input power.

According to Hefner *et al*. [18], three-dimensional heat diffusion equation for isotropic materials is needed for electrothermal simulation. The thermal model can be written as

$$\nabla.(k(T)\nabla T) = \rho c\frac{\partial T}{\partial t} \tag{10}$$

where the thermal conductivity is given by

$$k(T) = 1.5486.(300/T)^{4/3} \tag{11}$$

2.4 Numerical Methods

To solve equation (2) numerically, several methods can be used such as Finite Element Method (FEM), Finite-Difference Method (FDM), Boundary Element Method (BEM) and Integral Equation Method (IEM). Sapatnekar *et al.* [13] and Alias *et al*. [14] both proposed a thermal simulation algorithm for multilayer full chip system by using Boundary Element Method (BEM). The Green Function, which is an important underlying concept under BEM, describes the temperature distribution in the chip. In [15], it gives idea about Integral Equation Method (IEM) which is using Volterra-Fredholm integral equation. Usually, IEM is used to determine the voltage gradient distribution and electro-insulation systems.

Meanwhile, Ammous *et al*. [16] presented a comparison between FEM and FDM thermal models. It shows the effect of the boundary condition at heat source. These thermal models produce a large temperature error because the discretized heat equation

does not fulfill the boundary equation. So, it is very important to properly determine the initial and boundary equation. According to Ghaffar *et al*. [9], FDM is the most commonly used method to design the discretization of partial differential equations (PDE) of heat transfer. FDM is usually designed in the form of one or two dimensional along the Cartesian plane. Figure 2.5 shows the meshes on the *x-y* plane.

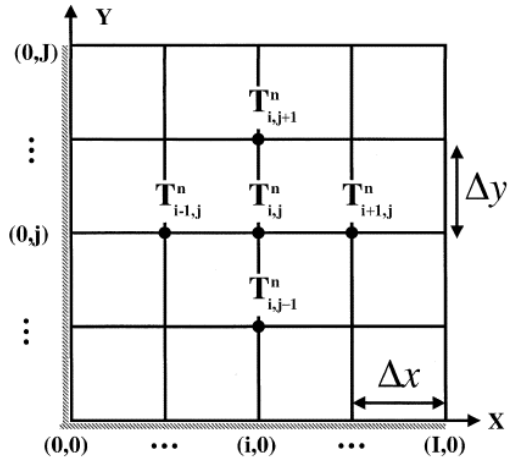

FIGURE 2.5 Meshes on the *x-y* plane.

In order to solve the linear system equation obtained from the FDM, iterative methods such as Jacobi, GS and SOR is used. These iterative methods are beneficial in solving large sparse system. However, iterative methods are not always applicable but they are still ideal to be used for FDM [21].

CHAPTER 3

METHODOLOGY

Figure 3.1 shows the process flow for this project.

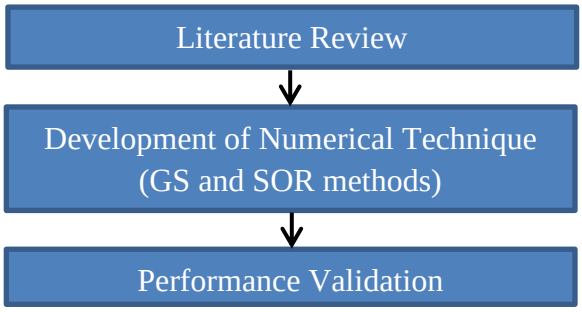

FIGURE 3.1 Project flow chart

This project started through identifies the current problem and determines the objectives. By gathering all the information from different researchers' publication such as scientific journals, books, and technical papers, a deeper understanding on peak junction temperature and thermal analysis is achieved.

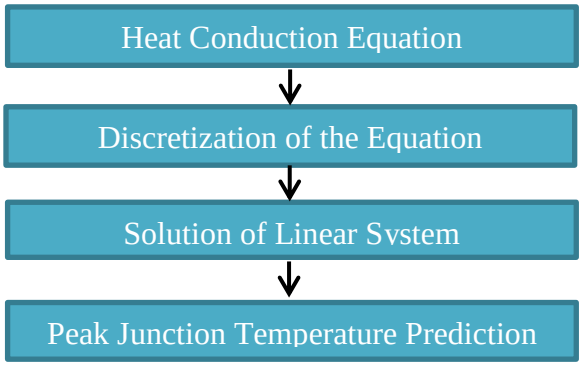

FIGURE 3.2 Development of numerical technique

Figure 3.2 shows the flow of development of numerical techniques. First phase is to understand the derivation of the heat conduction equation. The next phase is to integrate the heat conduction equation into silicon die thermal system. In this phase, FDM will be applied to the governing heat conduction equation of silicon die thermal system. Thereafter, in order to determine the peak junction temperature, GS and SOR methods will be used to solve the resulting linear system. After determine the peak junction temperature from both numerical techniques, a comparison will be performed.

As mention earlier, FDM implicit scheme i.e. Backward Time, Centered Space (BTCS) will be applied to discretize the equation (2).

The BTCS scheme is as shown below

$$\frac{\partial T}{\partial t} = \frac{T_{i,j}^{(k+1)} - T_{i,j}^{(k)}}{\Delta t} \ , \tag{12}$$

$$\frac{\partial^2 T}{\partial x^2} = \frac{T_{i+1,j}^{(k+1)} - 2T_{i,j}^{(k+1)} + T_{i-1,j}^{(k+1)}}{(\Delta x)^2} \tag{13}$$

and

$$\frac{\partial^2 T}{\partial y^2} = \frac{T_{i+1,j}^{(k+1)} - 2T_{i,j}^{(k+1)} + T_{i-1,j}^{(k+1)}}{(\Delta y)^2} \ . \tag{14}$$

By applying formulas (12), (13) and (14) to equation (2), it will results to

$$\frac{T_{i,j}^{(k+1)} - T_{i,j}^{(k)}}{\Delta t} = \frac{k}{\rho c_p}\left[\frac{T_{i+1,j}^{(k+1)} - 2T_{i,j}^{(k+1)} + T_{i-1,j}^{(k+1)}}{(\Delta x)^2} + \frac{T_{i+1,j}^{(k+1)} - 2T_{i,j}^{(k+1)} + T_{i-1,j}^{(k+1)}}{(\Delta y)^2}\right] + \frac{G_{i,j}^{(k)}}{\rho c_p} \ . \tag{15}$$

Now, let $(\Delta x)^2 = (\Delta x)^2 = h^2$, $\alpha = 1 + \frac{4\Delta t k}{\rho c_p h^2}$ and $\lambda = \frac{\Delta t k}{\rho c_p h^2}$, equation (15) can be rewrite as

$$\alpha T_{i,j}^{(k+1)} = \lambda\left(T_{i+1,j}^{(k+1)} + T_{i-1,j}^{(k+1)} + T_{i+1,j}^{(k+1)} + T_{i-1,j}^{(k+1)}\right) + T_{i,j}^{(k)} + \frac{\Delta t}{\rho c_p} G_{i,j}^{(k)} . \tag{16}$$

Generally, equation (16) can be represented in matrix form as below

$$AT = c\,. \tag{17}$$

Then, the resulting linear system (17) will be solved by using GS and SOR methods. The formula of GS is

$$T^{(k+1)} = \left(D - L\right)^{-1}\left(UT^{(k)} + c\right). \tag{18}$$

Meanwhile, the formula of SOR is

$$T^{(k+1)} = (1-\omega)T^{(k)} + \omega\left(D - L\right)^{-1}\left(UT^{(k)} + c\right) \tag{19}$$

where D, $-L$ and $-U$ represent the diagonal, strictly lower triangular, strictly upper triangular of matrix A, respectively. The convergence criterion formula for both GS and SOR methods is

$$\left\|T^{(k+1)} - T^{(k)}\right\| < \varepsilon\,. \tag{20}$$

CHAPTER 4

RESULTS AND DISCUSSION

In this chapter, the results obtained from the tests performed by using GS and SOR iteration method will be discussed. The numerical technique have been conducted for steady state and different mesh grid sizes which are 16×16, 32×32, 64×64, 128×128 and 256×256. For GS and SOR methods, it is important to define the initial and boundary conditions properly as it will affect the results. For initial condition (i.e. t = 0), it is assumed to be the room temperature which is $20°\text{C}$. Meanwhile, for boundary equation (refer to equation (3)), it determine the value at $x=0$, $x=L$, $y=0$ and $y=L$. The model length, L is set to 2cm. Table 4.1 below shows the properties of silicon that has been used in this project.

TABLE 4.1 Properties of Silicon [17]

Properties	**SI Units**	**Values**
Thermal Conductivity, k	$w/cm°\text{C}$	1.3
Thermal Density, ρ	g/cm^3	2.33
Specific Heat Capacity, c_p	$J/g°\text{C}$	0.7

For the numerical simulations, parameters such as the number of iterations (k), computational time in seconds (Total time) and maximum temperature ($T_{\max}$) are recorded. The optimal value of ω for SOR method is chosen within ±0.1 by a trial and error process. All the simulations are performed on a personal computer with Intel®

Core™ 2 Duo processor T6400 (2.0 GHz, 800 MHz PSB, 2 MB L2 Cache) and 2.0 GB RAM, and the programs are compiled by using MATLAB. In addition, numerical results of the GS method and built-in function in MATLAB, *pdepe* are also included in order to validate the performance of the SOR method. In this study, the convergence criterion for GS and SOR methods is $\varepsilon = 10^{-10}$ and only case of steady state is considered.

Comparison of numerical results is presented in Table 4.2. The graphs in Figure 4.1 to Figure 4.5 illustrating the temperature profile by using GS method and the graphs in Figure 4.6 to Figure 4.10 presenting the temperature profile by using SOR method. Meanwhile, Figure 4.11 to Figure 4.14 represent the temperature profile by using *pdepe* function.

.

TABLE 4.2 Comparison of numerical results

Grid size	Iteration method	k	Total time	T_{max}
16×16	GS	452	2.270	30.17
	SOR ($\omega = 1.7$)	58	0.184	30.17
	pdepe	-	-	29.39
32×32	GS	1664	18.257	30.19
	SOR ($\omega = 1.8$)	146	1.081	30.19
	pdepe	-	-	29.80
64×64	GS	6076	287.447	30.20
	SOR ($\omega = 1.9$)	241	7.722	30.20
	pdepe	-	-	30.00
128×128	GS	21986	3429.41	30.20
	SOR ($\omega = 1.9$)	1109	181.571	30.20
	pdepe	-	-	30.10
256×256	GS	78702	47260.527	30.20
	SOR ($\omega = 1.9$)	4103	2190.073	30.20
	pdepe	-	-	30.15

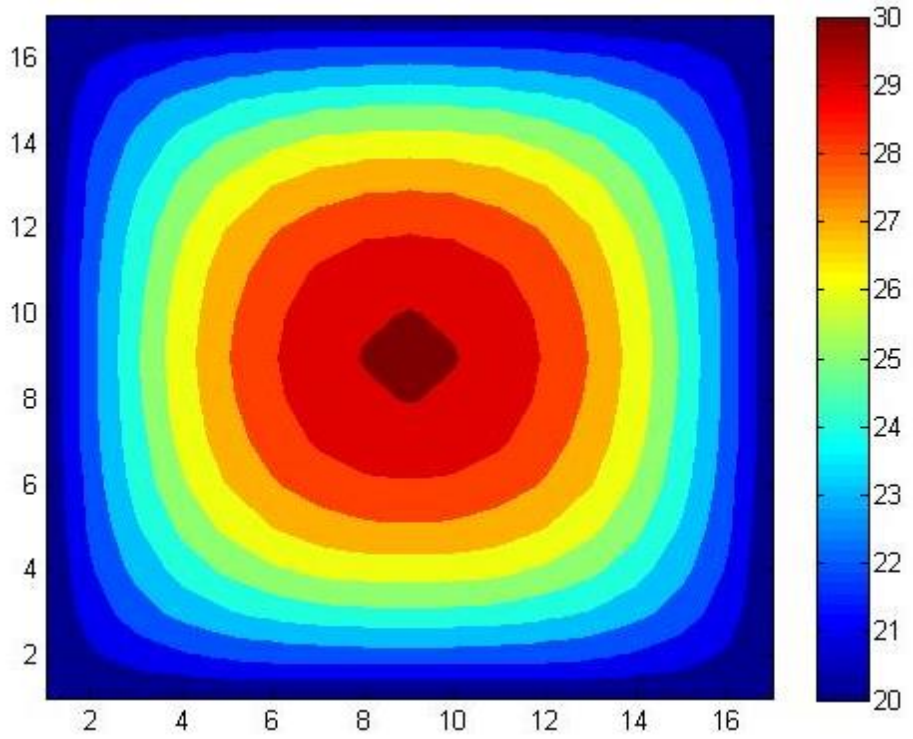

FIGURE 4.1 Temperature profile by using GS method for grid size of 16×16

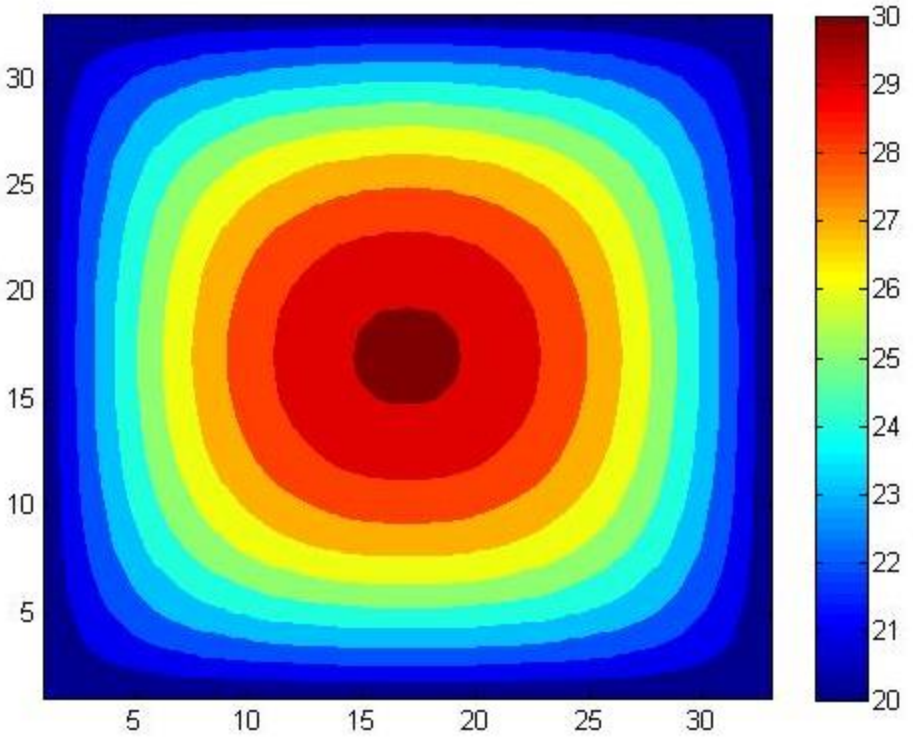

FIGURE 4.2 Temperature profile by using GS method for grid size of 32×32

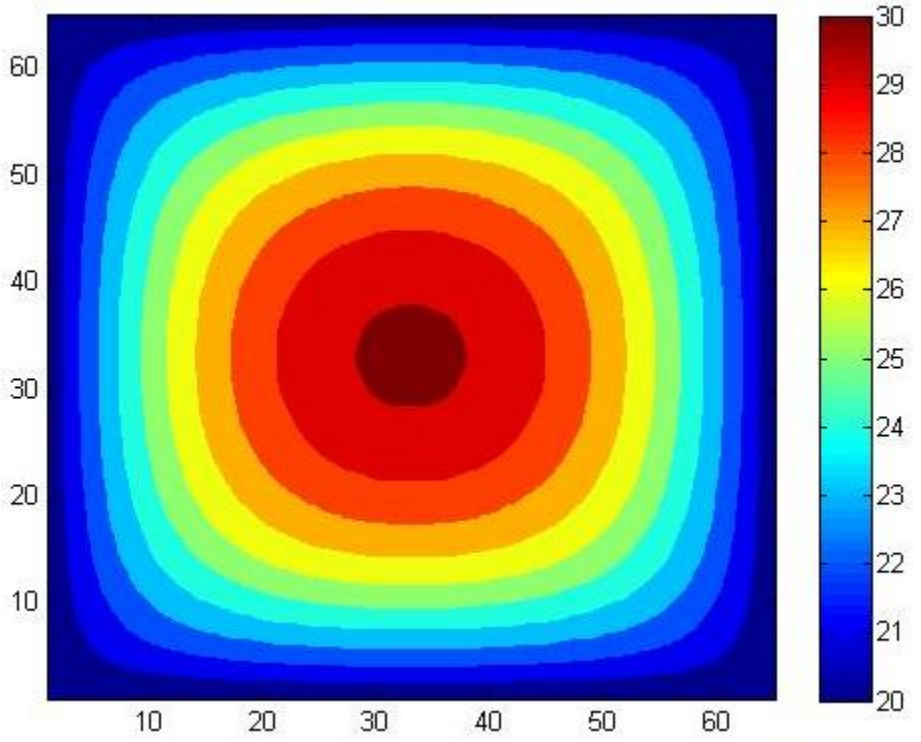

FIGURE 4.3 Temperature profile by using GS method for grid size of 64×64

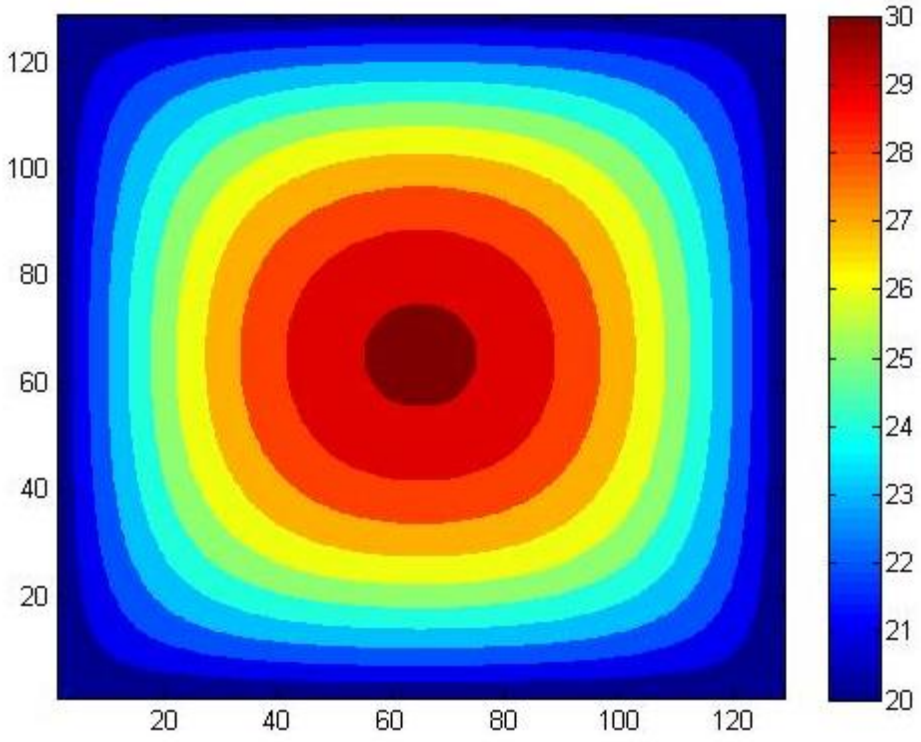

FIGURE 4.4 Temperature profile by using GS method for grid size of 128×128

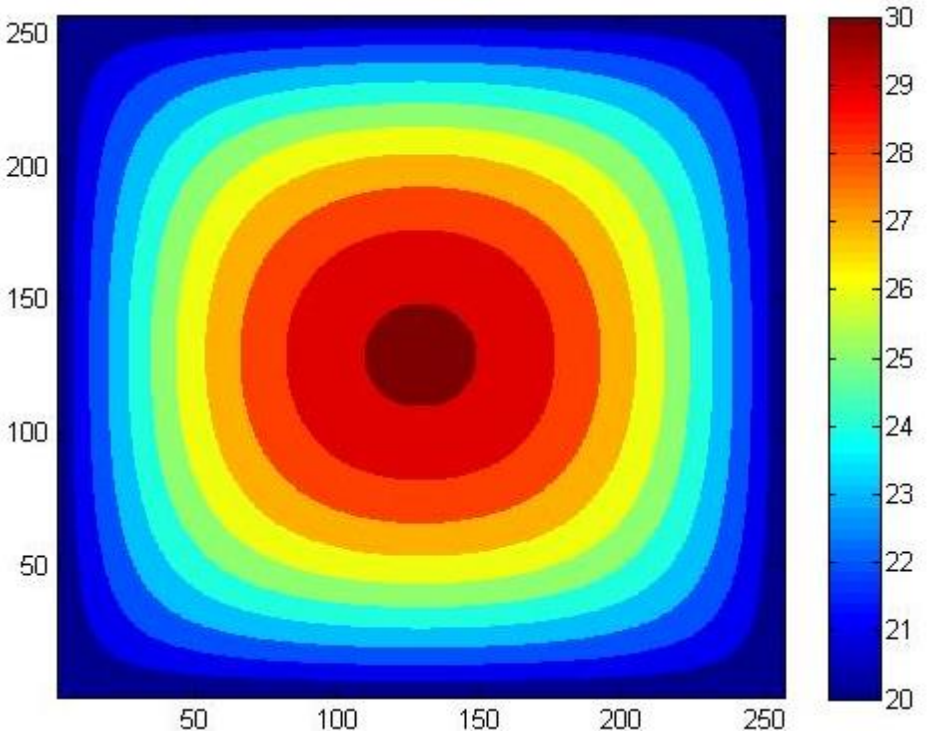

FIGURE 4.5 Temperature profile by using GS method for grid size of 256×256

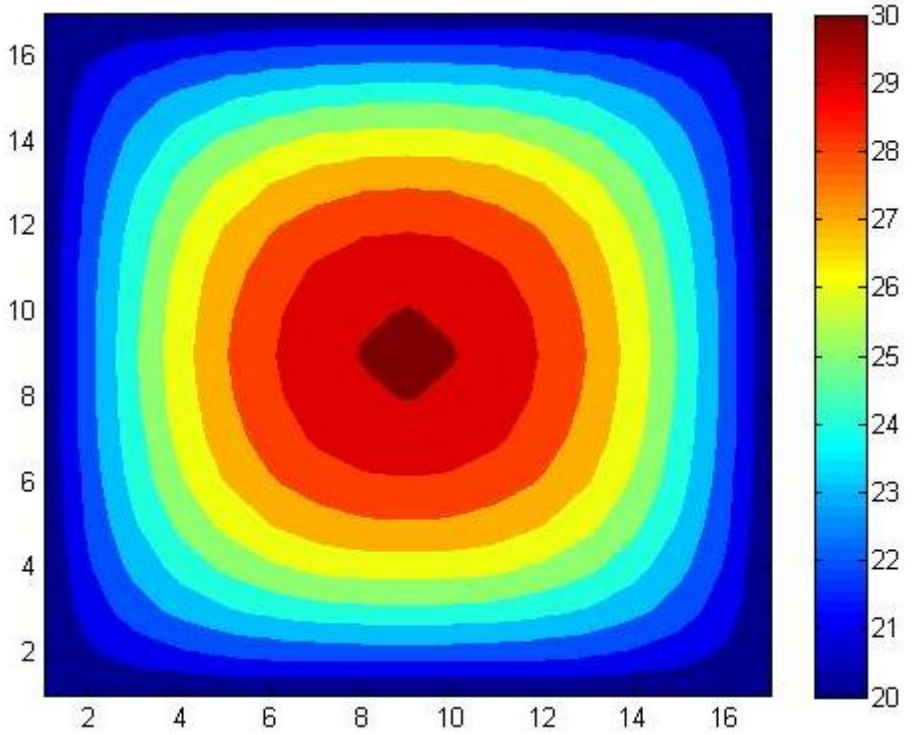

FIGURE 4.6 Temperature profile by using SOR method for grid size of 16×16

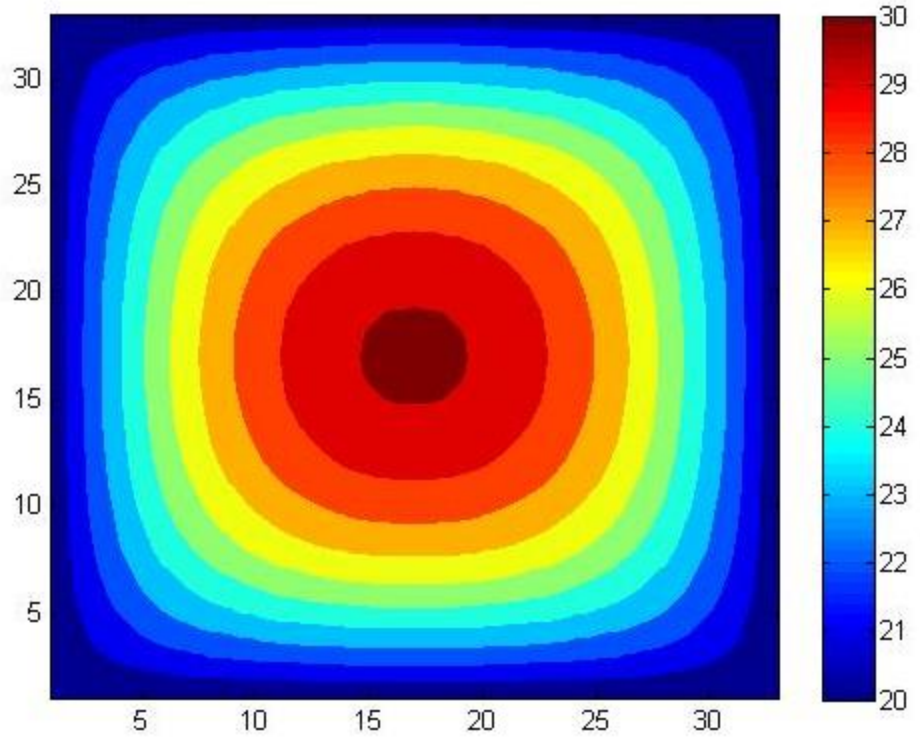

FIGURE 4.7 Temperature profile by using SOR method for grid size of 32×32

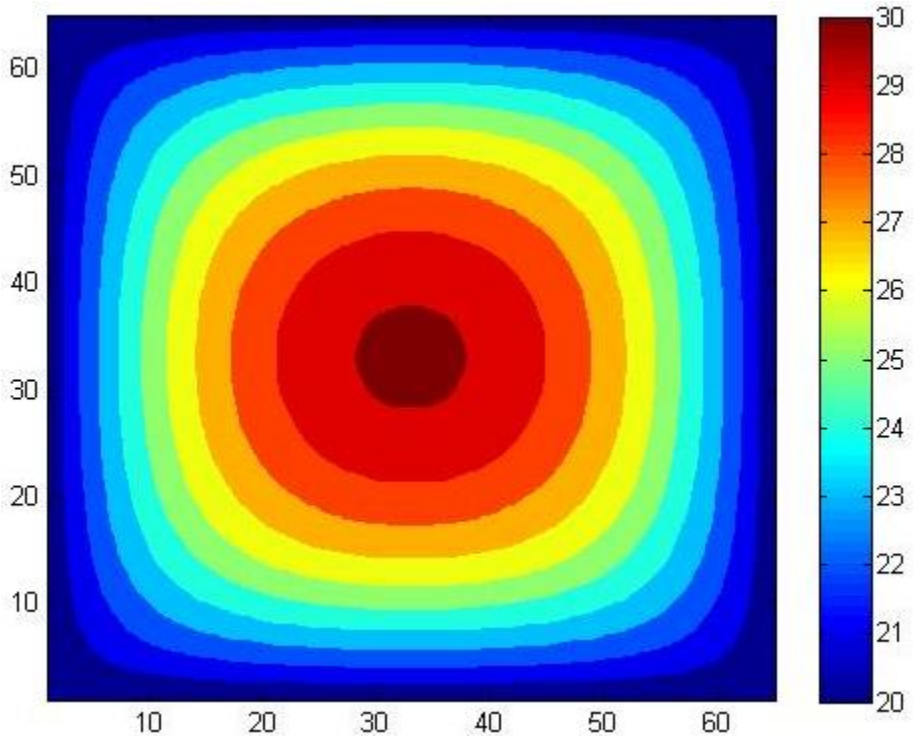

FIGURE 4.8 Temperature profile by using SOR method for grid size of 64×64

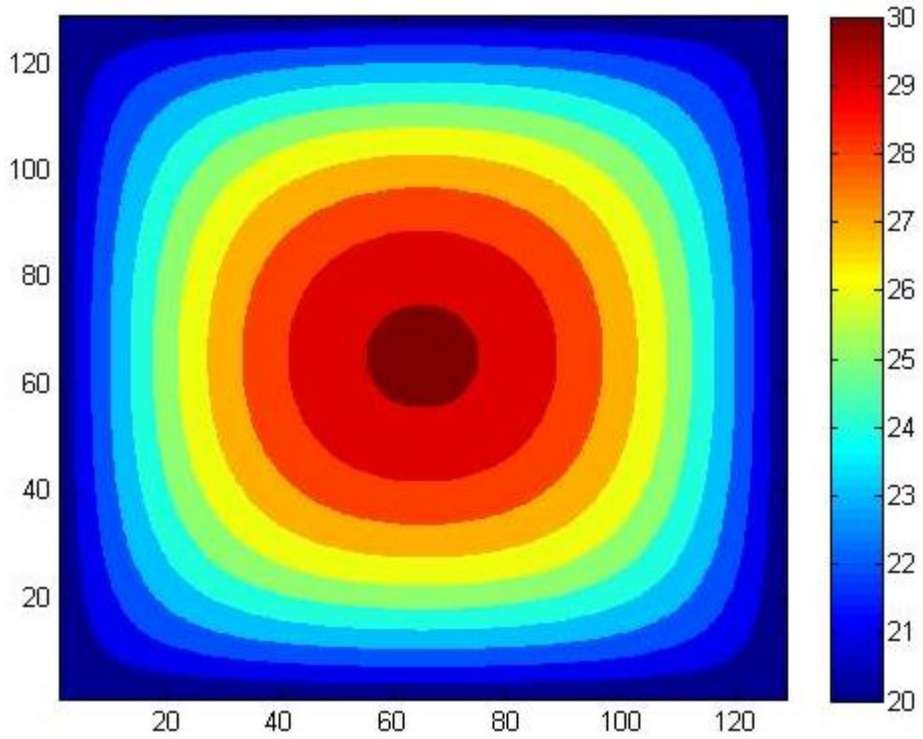

FIGURE 4.9 Temperature profile by using SOR method for grid size of 128×128

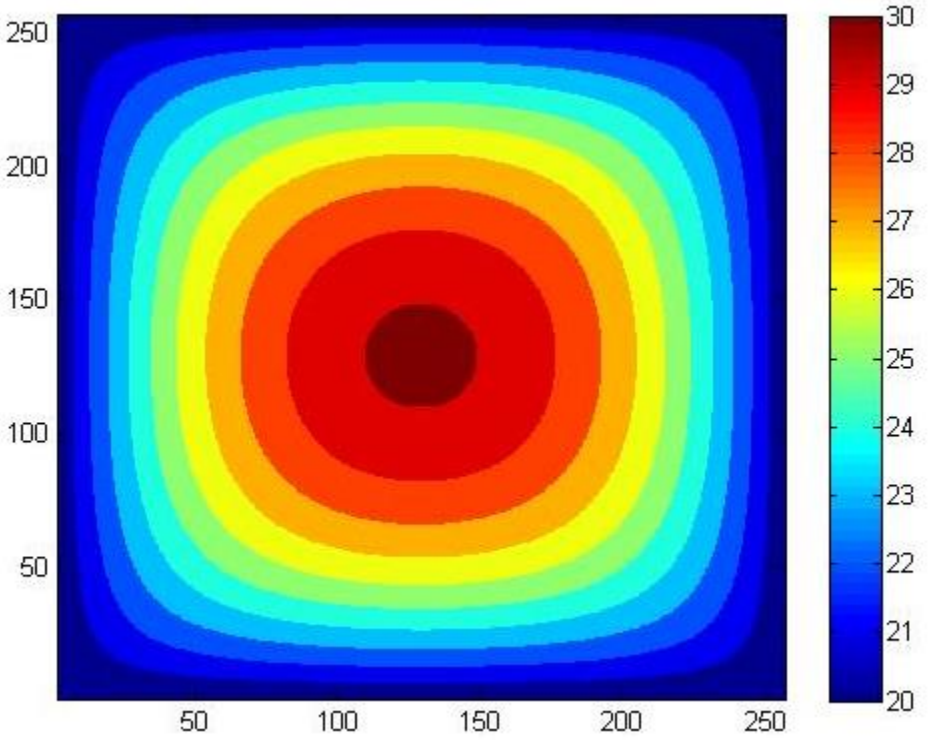

FIGURE 4.10 Temperature profile by using SOR method for grid size of 256×256

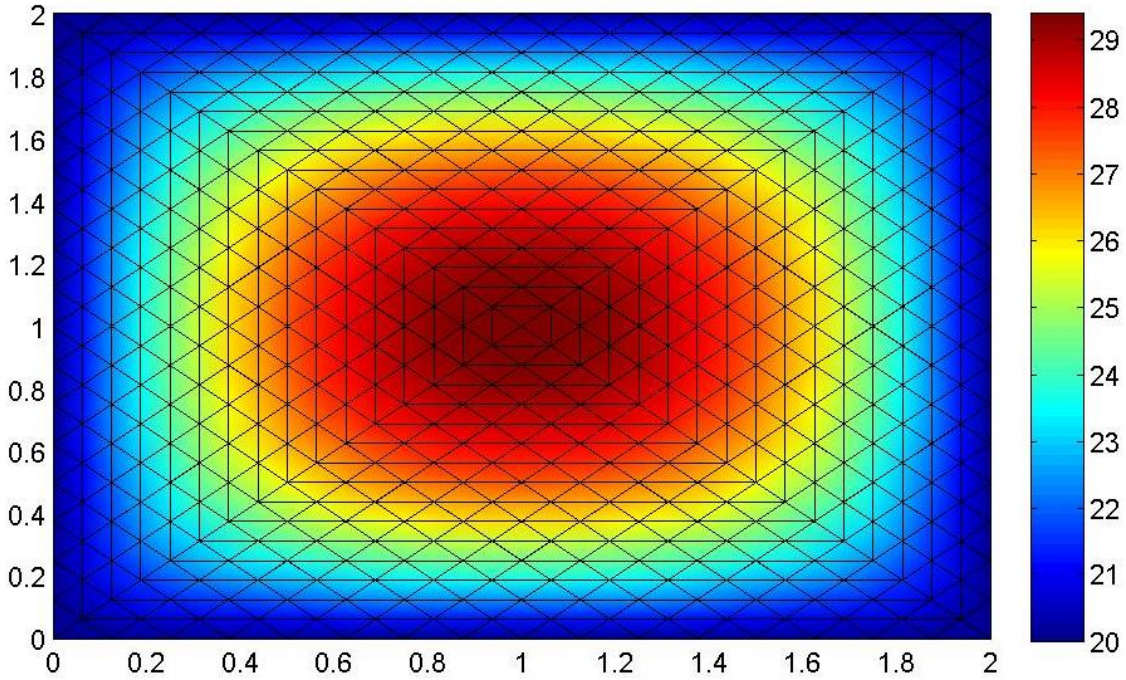

FIGURE 4.11 Temperature profile by using *pdepe* for grid size of 16×16

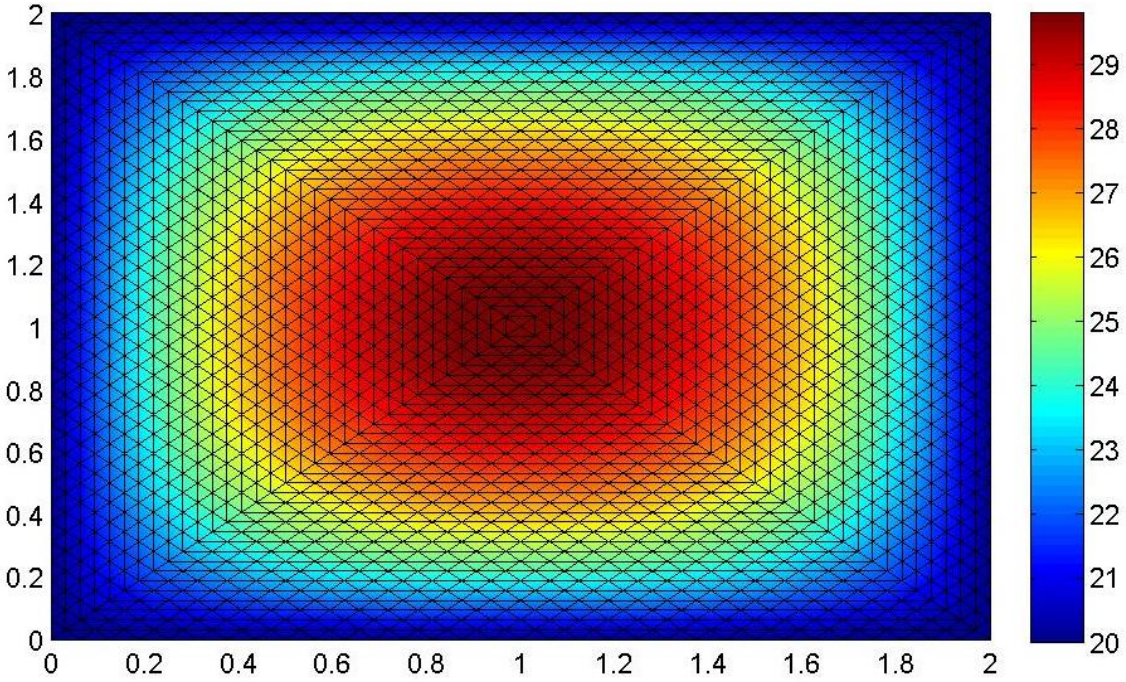

FIGURE 4.12 Temperature profile by using *pdepe* for grid size of 32×32

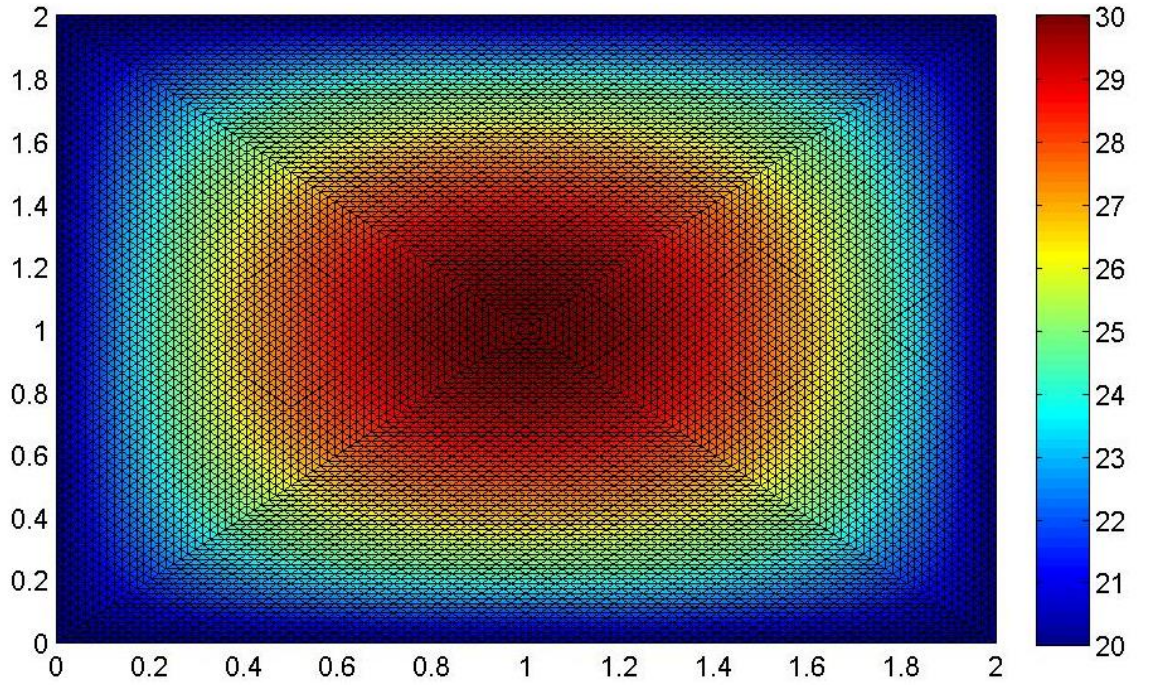

FIGURE 4.13 Temperature profile by using *pdepe* for grid size of 64×64

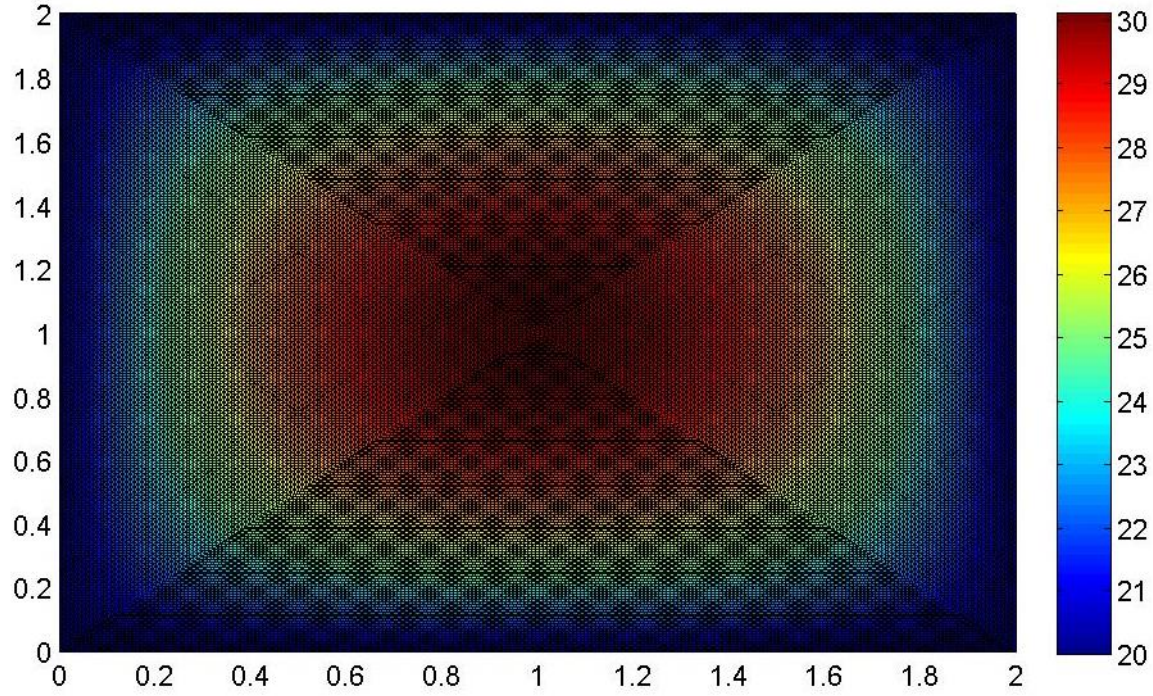

FIGURE 4.14 Temperature profile by using *pdepe* for grid size of 128×128

From the comparison of numerical results in Table 4.2, it is observed that both GS and SOR methods give same maximum temperature. Meanwhile, for *pdepe*, the maximum temperature is comparable with GS and SOR methods result. Based on the numerical results obtained, it clearly shows that an application of the SOR method reduced the number of iterations and computational time compared to GS method. Range of percentage of reduction in term of number of iteration is in between 87.17% to 96.03%. Meanwhile, in term of computational time, the percentage of reduction is in between 91.89% to 97.33%. From Figures 4.1 until 4.14, it can be observed that the maximum temperature is located at the center of the silicon die.

CHAPTER 5

CONCLUSION AND RECOMMENDATIONS

As a conclusion, this study is concerned with peak junction temperature of semiconductor devices on Printed Circuit Board (PCB). This study also focused on the implementation of heat conduction equation in solving thermal systems. The equation will be solved under adiabatic condition where the heat generated and the heat transferred in will be neglected. The numerical method used to discretize the governing equation is by using FDM. As a result from the discretization, a linear system will be solved using GS and SOR methods. For comparison analysis, results from both numerical techniques will be analyzed and the parameters such as number of iteration, maximum temperature and total time were recorded.

Based on numerical results obtained, it apparently show that the application of SOR method reduce the number of iterations and computational time compared to GS method. After performing this case study, it can be concluded SOR method is more preferable compared to GS method in determining the peak junction temperature of semiconductor devices.

For future recommendation, the study can be extended by solving the two-dimensional heat conduction equation in dynamic state (unsteady state). Besides that, thermal analysis on three-dimensional model can also be considered. Also, for more advanced study, monitoring tool or system for prediction peak junction temperature can be developed.

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