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DEVELOPMENT OF GRAPHENE BASED FIELD EFFECT TRANSISTOR (FET)

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JANUARY 2017

CERTIFICATION OF APPROVAL

Development of Graphene Based Field Effect Transistor (FET)

By

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18365

A project dissertation submitted to the

Electrical and Electronics Engineering Program

Universiti Teknologi PETRONAS

In partial fulfilment of the requirement for the

BACHELOR OF ENGINEERING (Hons)

(ELECTICAL & ELECTRONICS)

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CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

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1.0 ABSTRACT

The electronic and electrical properties of graphene have great potential for electronic devices in future. Researchers and engineers exploiting the benefit of graphene to be replaced or integrated together with current electronic device and semiconductor, thus allow more smaller and faster electronic. It could be material that could break Moore's Law limitation that predicts in 2021 the semiconductor fabrication feature size of electronic devices such as short channel length and width will stop shrinking. In this report, the fabricate and characterize graphene in FET (became Graphene based Field Effect Transistor, GFET) on silicon wafer are demonstrated. There were two design of GFET which is with Al_2O_3 material and SiO_2 uses as insulator to separate drain, source and gate by using atomic layer deposition (ALD) technique. By using all maximum capability of facilities in UTP, I will be able to fabricate (GFET) and characterized the properties.

2.0 INTRODUCTION

2.1 Background of FET

For the 50 years, we are shrinking the size of transistor and increase its number. However new method need to be explored because it cannot be forever shrink to the size of atom. In 1965 transistor shrinking is double every year that could fit onto a chip, and in 1975 adjusted the number of transistor double every 18months. "A FET (Field Effect Transistor) consists of a gate, a channel region which is source and drain electrodes, and a barrier gap for channel separate [1][7]". The conventional FET operation works as control of the channel conductivity. FET should be responses quickly to change of voltage, at gate. Short channel is one of requirement to make the switching channel fast. Unfortunately, FETs tend to be short circuit if the gate are to close and caused also by degradation of electrostatic such as threshold-voltage roll-off, drain-induced barrier lowering, and impaired drain-current saturation. As mentioned in scaling theory FET will be robust against short-channel effects. The gate-controlled region and the barrier is thin. The interesting in here is having one atom layer thick of graphene as transistor. Single-layer graphene is a purely two-dimensional material with lattice consist of hexagon shape with C atom on each corner.

2.2 Problem Statement

"In 1965, Intel co-founder Gordon Moore stated that the number of transistors per area on IC had doubled every year based on his observation which known as today as Moore's Law [1]". Although the law has slowed, the law redefined to the numbers of transistor has since doubled approximately every 18 months. Because Moore's law growth plot look like exponential growth, it definitely can't be continue forever. It must be limitation of it physical. The Moore's Laws make the IC and computer chip become smaller, efficient and cheaper at a same transistor count. Eventually, the conflict come later which is the heat can't escape well because cooling the transistors not enough energy compare to what the energy passes through. Experts show that computers should reach physical limits of Moore's law sometime in the 2020s. We are now 4 years toward 2020 should think and research other way of fabrication of transistor. Achieving of doubling transistor and shrinking become slower. Furthermore, shrinking size of transistor cause the degradation

of electrostatic and other problem such as short channel effect. By apply a graphene layer between gate at D-S, a short-channel effects can be reduced and lower the resistance of the GFET.

3.0 OBJECTIVES AND SCOPE OF STUDY

In this project, the graphene grown in various method to fabricate graphene-based transistors. The fabrication includes preparation of substrate graphene, fabricate electrode of drain, gate and sources. The method of fabrication is quite complicated, so that the simple way, high quality and affordable need be researching more and explored. The project objectives are:

i. To fabricate graphene based FET on Si wafer.
ii. To study and plot the I-V transfer characteristic of the GFET.

From all the objectives listed, at the end of the day. Student must be able to demonstrate a graphene FET with its current-voltage transfer characteristics, fabrication of GFET electrode, and transfer graphene to silicon wafer.

4.0 LITERATURE REVIEWS

4.1 Properties of graphene

A graphene layer exists in two dimension purely unlike most material exist in 3 dimension in nature It form of hexagons shape with equal length with a carbon atom at every corner of the hexagons. This material reported around one and half decade ago without the discover of graphene name but in 2004 Manchester group have found interest in graphene for the use of electronic devices. "A few method approach in grown graphene some of it famous are mechanical exfoliation, growth on metals and subsequent graphene transfers to insulating substrates and thermal decomposition of SiC (also known as epitaxial graphene) [1],[2]". Exfoliation is one of popular method of grown graphene in laboratory, however not for electronics industry. While the other two method have bright future in producing wafer-scale graphene. Common practice of semiconductor processing techniques in fabrication is metallization, lithography and etching. This technique applied to the graphene after has been prepared. Here discussed the important characteristic of graphene which is the bandgap, and charge transport.

4.1.1 Bandgap

The bandgap tenability is key of change the characteristic of graphene from metal to semi conductive properties. The shape of valence and conduction bands are cone and meet at the K points of the Brillouin zone. However, it has zero bandgap which cause the properties always on act like a metal and can't switch off and not suitable for logic application like a transistor. Thus, the band structure need to modified. However, there is a few methods to open or trim the bandgap. One of it by constraining large-area graphene in single dimension and shape like a nanoribbon. Second is applying strain to graphene so that biasing the bilayer graphene. "The difference of nanoribbons and edge geometries [1] and functionalization together with doping have been eliminated from giving any effect to bandgap [2] by disarray of modest edge". For devices with custom field-effect, only edges that have well-designation and taper or thin nanoribbons are required and this gives great issue with the current equipment to process semiconductor. It is also important to note that a nanoribbon that has wider bandgap may increase in its parabolic conduction

band and valence. Even though lately, uniform width and less-rough edge of nanoribbons have been produced by 'unfastening' process of carbon nanotube, a nanoribbon which is perfect may be still not good enough towards electronics implementation. "According to theoretical experiments, bandgap size depends on perpendicular area strength [3,4]". "While if electrical force is put on bilayer, the bandgap will open and the K-point band will follow the shape of Mexican hat [3,4]". "Few results proposed that the big-field of epitaxial graphene single layer is zero [5,6]". Its transfer characteristic suggests no bandgap as it reflects zero switch off. While epitaxial bi-layer graphene shows regular band-gap. In conclusion, even though there are many ways to disclose graphene bandgap, it may be difficult or do not suit for real implementation. For example, strain has been proposed to open the large graphene area.

4.1.2 Mobility

One of the advantages of graphene in FET is it have high carrier mobility at room temperature. The mobility for exfoliated graphene is depend on the carbon or silicon face of the SiC. Although this two-type reported have high mobility, it is easier to grow on single-layer or bilayer which make it suitable for uses of electronic application. "In early graphene MOS structures, the mobility was affected by the use of a top-gate dielectric [7, 8]". "However, in study of the recent demonstration, the mobility in top-gated graphene MOS channels and the observation of similar mobility before and after top gate formation show that high-mobility graphene MOS channels can be made with a proper choice of the gate dielectric and optimization of the deposition process [9], [10]". The numbers of mobility are awesome but it requires closer inspection. "A general trend for conventional semiconductors is that the electron mobility decreases as the bandgap increases, and a similar trend has been predicted for carbon nanotubes (CNTs) [11], 12]." The expected of graphene nanoribbon mobility should be lower than in silicon (in bulk) and no higher than silicon channel in standard MOS device. The graphene offered high mobility than convectional MOS that increase the speed of the switching, but it is difficult to switch off devices.

4.1.3 GFET structure

The G-FET structure are usually form from the traditional FET structured with integrated of graphene on top of a layer in FET structure. Below are few structure that have been practiced in most FET. I was select the C option (top gate/top contact) with graphene on top of the semiconductor. This structure give the best and easy structure layer to fabricate because only work with one single side of the semiconductor (Si).

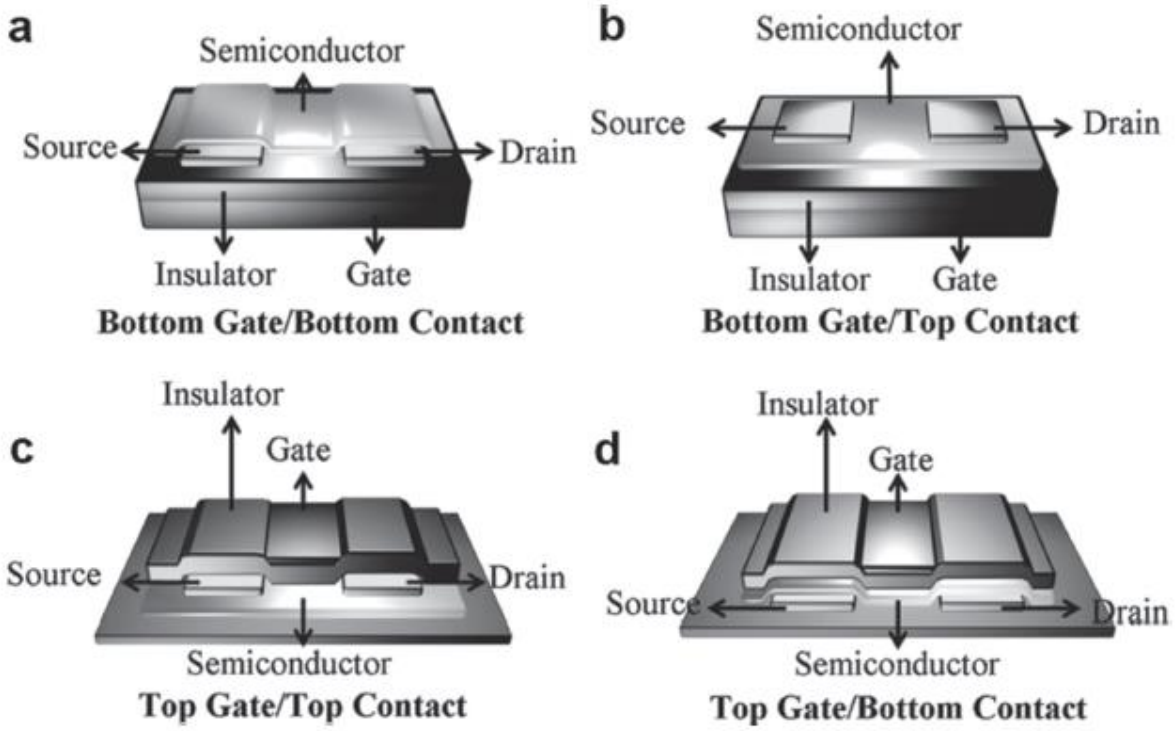


Figure 1: Design structure of FET

4.1.4 Method growth graphene

Below the comparison of growth graphene using different methods with their advantages and disadvantages. The consideration of method usually cost, quality of graphene and practically mass produce.

Method	Advantages	Disadvantages
Mechanical exfoliation	Highest quality of electrical properties	size, thickness and location are uncontrollable
Epitaxial Growth on Silicon Carbide Single Crystal	Practical larger scale, single atomic	High temperature, high cost
Chemical Vapour Deposition (CVD)	Most promising, inexpensive and feasible method for single layer. Practical for large application	Gaseous by-products of the process are usually very toxic
Self-Assembly of Soluble graphene	Practical larger scale, single atomic and cheaper	Quality of graphene (oxygen functional group left)

Table 1: method of growth graphene and their advantages and disadvantages

4.1.5 Circuit Characterization

Measurement of I-V characteristic. Based on theory of properties grapheme. The graph of measurement should be as shown as below

1. Drain current VS Gate voltage

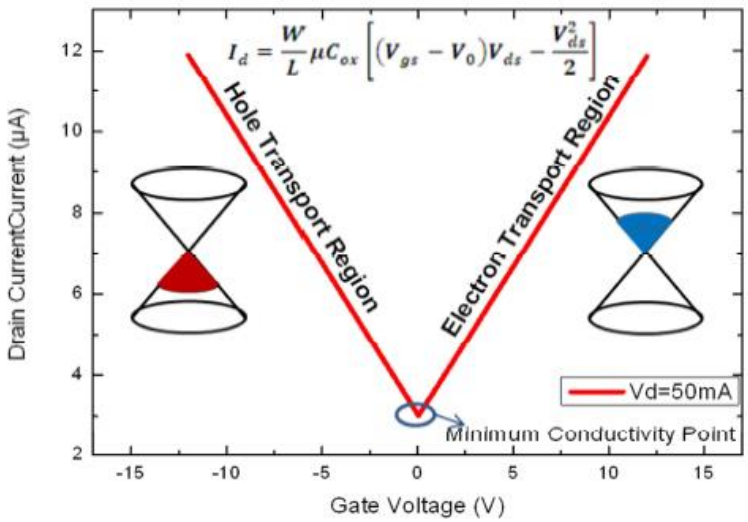


Figure 2: The drain current is modulated almost symmetrically with back gate voltage All graphs are ideal case of simulation.

2. Drain current versus Source-Drain Voltage

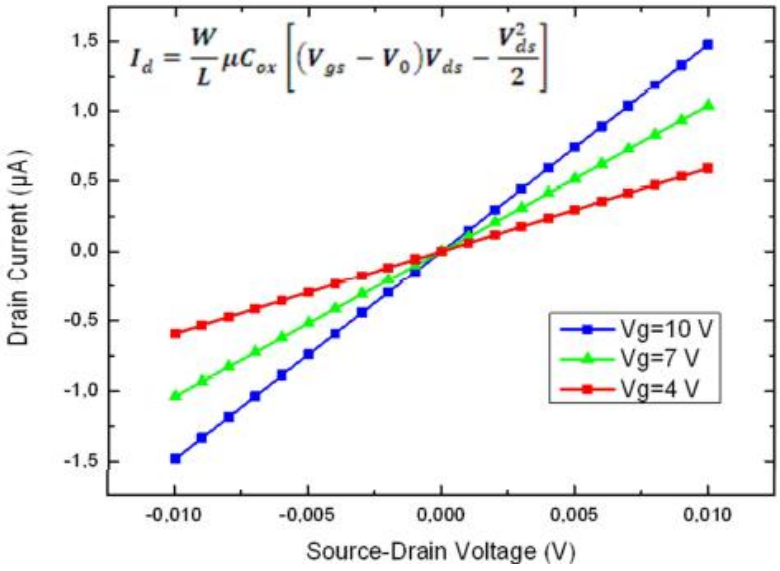


Figure 3: The drain current linearly increases with source-drain voltage

4.2 Critical Analysis

In this project focused were fabrication of graphene FET that will replace conventional MOSFET. CPU is the hottest part in computer that usually running around 45 °C to 115 °C. Some research claim that by applying layer of graphene it reduces the CPU temperature average in 13 °C and attribute for more life span of electronic. Furthermore, graphene makes an electronic device possible to be thin and can be integrated with any surface like paper and human. It has great advantages not also in microprocessor but also in radio instrument, sensing application and medical.

4.3 Survey of literature reviews

no	Authors	Methods	Details	Advantages/Disadvantages
1	Wang, Ouyang, Li, Guo,2 Dai1 (2008)	Plasma etching	Graphene Nanoribbon FET at room temperature with 10nm fabrication	comparable in performance to small diameter carbon nanotube devices challenging of fabricate under 20nm using plasma
2	Schwierz (2010)		bilayer pseudospin FET GFET in logic and RF applications. Scaled more short for the channel which impact higher speed	still at early stage compare to CNT
3	Vaziri (2011)	Mechanical exfoliation	single layer dual gate GFET	Various contact and design arrangement graphene gate tested, clear instruction involve high cost and equipment limitation
4	Xia,Farmer, Lin, Avouris (2010)	E-beam lithography	dual layer, dual gate, FET with high on off current ratio	Potential in digital electronics, pseudospintronics, terahertz technology, and infrared nanophotonics

Table 2: A few surveys from research papers published

5.0 METHODOLOGY/PROJECT WORK

5.1 Flow Chart of Project Work

The process flow chart of the project as below. It may change according the problems and future experimental. The total progress is in FYP 1 and FYP 2 project.

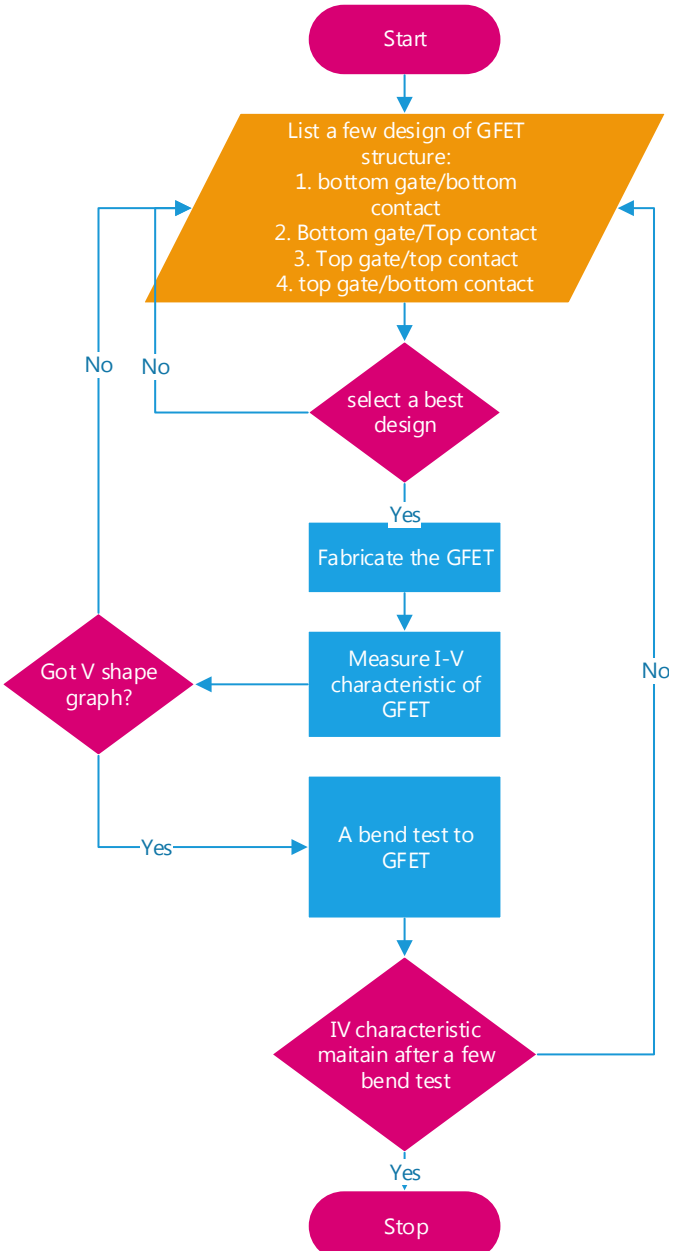


Figure 4: Flowchart process of fabrication GFET

Based on the flowchart, the GFET design was selected from a few of design of GFET and composition. If it is good design, then proceed with fabrication of GFET. Then the GFET will characterized, if the result as expected a few other physical tests done and measure again the GFET should be pass. If not, it repeat back to the selection of best GFET design.

5.2 Equipment and material

EQUIPMENT	MATERIAL	SOFTWARE
Graphene CVD	Cooper Film	Sketchme Up
Magnetron sputtering	PMMA	LTpsice
Agilent B1500A	Iron Chloride	
Spin Coater	Acetone	
	Silicon wafer	
	Gold	
	Al2O3	
	Aluminum plate Titanium	

Table 3: A list of equipment, materials and software

5.3 Process of fabrication Option A

There were 2 structure with different design and different oxide layer (dielectric material). First option A is using Al_2O_3 and option B is using Silicon dioxide. Option A was fabricating in UTP while Option B is fabricating at Adtec, Taiping. Both fabricated with different method.

5.3.1 Cutting/cleaving silicon wafer

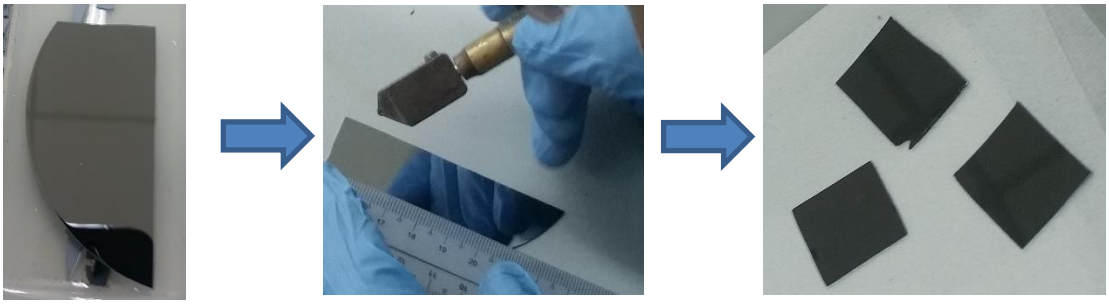


Figure 6: Cutting/cleaving process of silicon wafer

Cutting/cleaving the silicon wafer into desire size of device using glass scribers. The silicon wafer is cutting into size of 2cm x 2cm. After scribe the silicon wafer is place into different height of place at a line of break. Press the tow side equally to break the wafer into a piece.

5.3.2 Cleaning Silicon wafer

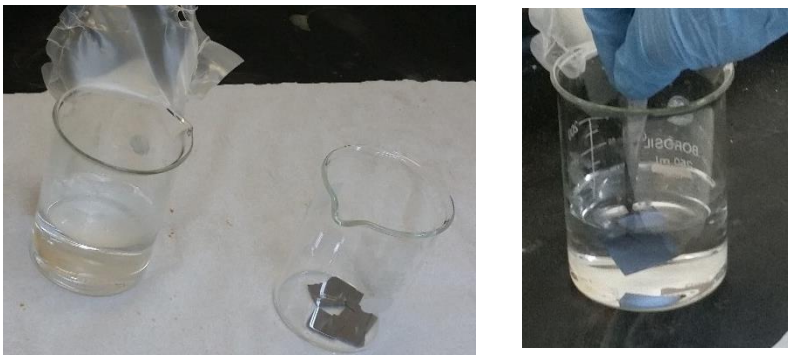


Figure 7: Cleaning of silicon wafer using HCl

Silicon wafer need to be clean to increase impurity of silicon by removing any contaminate or residue inorganic or organic on surface on silicon pieces. There are a few methods can be select in cleaning silicon but often used wet cleaning technique by using solvent clean (example: acid) followed by distilled water to rinse.

In semiconductor industry, the cleaning of contamination on the surface of wafer is become critical especially when the device in more smaller and smaller. This cause the defect density (depend on cleanness) which affect to the yield on the silicon wafer. Cleaning wafer techniques that remove contaminant particle will decrease the defect density. However, the small particles tend to have strong electrostatic forces which give difficulty in removing them between particles and substrates. For about three-decade process of cleaning wafer remain unchanged except what has changed is its implementation with optimized equipment: from simple immersion to centrifugal spraying, megasonic cleaning and ultrasonic techniques. The objective of wafer cleaning is the reduce unwanted particle and chemical impurities from the silicon surface without damaging or change the substrate surface. The cleaning of wafer is very crucial because it affected the device performance and reliability of device later for the semiconductor devices.

5.3.3 Growth silicon dioxide

Figure 8: Silicon insert the reaction chamber

Oxidation is a process by which a metal or semiconductor is converted to an oxide. The objective of this step is to growth (SiO_2) on top of silicon. The chemical reaction between oxygen and silicon to generate SiO_2 is usually driven by a high-heat environment; however, silicon dioxide also form in room temperature with approximate of 1nm thick in normal environment air. In order to grow thicker oxides in a controlled environment, several methods can be implemented to grow silicon dioxide which is thermal oxidation, Plasma Enhanced Chemical Vapor Deposition (PECVD), and Nitric Acid Oxidation of Silicon (NAOS). I used thermal oxidation which one equipment availability in the nanotechnology lab.

Thermal oxidation can be divided into two which is wet oxidation and dry oxidation. I prefer using dry oxidation which is using molecular oxygen the main oxidant. Dry oxidation is more controllable than wet oxidation. The reaction take placed:

$$\mathrm{Si} + \mathrm{O_2} \rightarrow \mathrm{SiO_2},$$

Usually thermal oxidation performed at high temperature within range of 800 ^{o}C - 1200 ^{o}C. Thus, resulting in a High Temperature Oxide (HTO) layer. “Silicon dioxide layers are mainly used as high quality insulators or masks for ion implantation and the ability to form high quality silicon dioxide is the main reason why silicon is still the dominating material for IC fabrication [6]”

Temperature is the parameter in control the growth silicon dioxide thickness. It may go varies depend on the hydrostatic pressure in the reaction chamber. In addition, the crystal orientation of the silicon wafer also affected.

Figure 9: Reaction Chamber to growth silicon dioxide

Figure 10: Flow control of oxygen.

Before start oxidation, the argon gas is flow into the chamber to pump out all the unnecessary air that have. Than after that oxygen will flow. This is necessary so that silicone don't react with other gas except oxygen. Argon gas used because it is inert gas which don't react to other elements. During dry oxidation, the wafer is placed in a pure oxygen gas (O_2) and heat up to desire temperature. The silicon on their surface will react with oxygen and become Silicon dioxide.

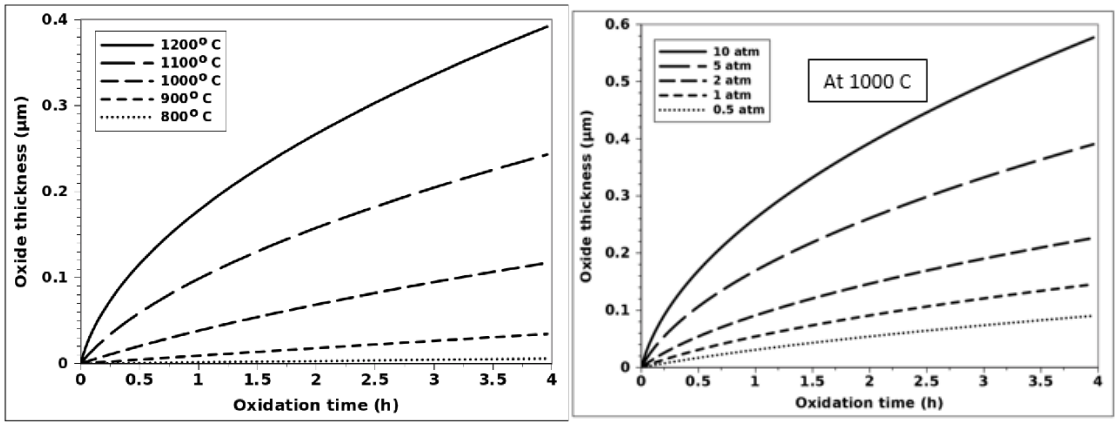


Figure 11: a) graph grow of oxide thickness versus time

b) Dry oxidation affected by the pressure which give faster rate of growth.

Oxide thickness versus oxidation time for dry (O_2). Figure shows the oxide thickness versus time for dry oxidation. By using lower temperature, the growth thickness is more controllable, however consume more time. In this project, I will growth approximate around 90nm to 100nm of silicon dioxide layer. Dry oxidation has more better quality oxide layer than wet oxidation. Commonly this method used to growth silicon dioxide lower than 100nm or a second step of oxidation (after wet oxidation). The purpose of second step is for improves the quality of oxide layer of the top tick part of oxide.

As mention earlier, hydrostatic pressure also effect the thermal grown oxides in both dry and wet oxidation. The oxidation thickness was also affected by the pressure of the oxygen the reaction chamber. The advantages of increased pressure are being able to achieved faster growth rate at lower temperature . By reducing the temperature, it causes less impurities and minimal movement of the junction during multiple subsequent oxidation steps required for complex IC device manufacturing. Further study by Katz and Kimerling stated that oxides that growth in high pressure enhanced more performance by reduced stacking fault.

5.3.4 Growth graphene

In literature review I have list a few methods of grow graphene and their advantages, disadvantage, suitability, cost and quality of graphene layer produces. With bias of equipment that available, I choose of growth graphene using Chemical Vapor Deposition (CVD). In simply word CVD is one of technique to deposit a substance onto substrate by using gaseous reactant. It combines the gas molecules in reaction chamber and heated. Detail explanation information below.

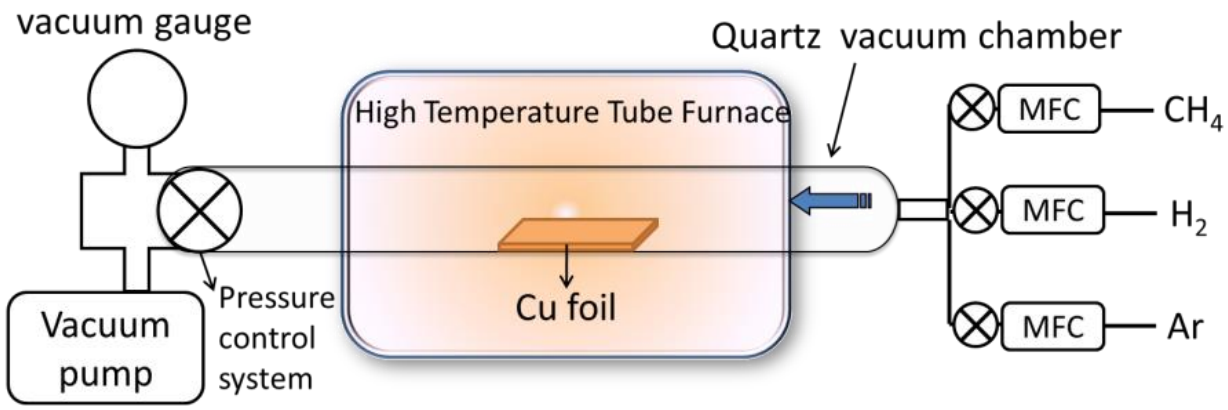


Figure 12: Illustration of growth graphene on copper foil

CVD is one of promising technique that produce high quality graphene with controllable thickness. In this case, copper foil is used because it has low solubility of carbon. The furnace is heat up with decomposition of methane gas in diluted hydrogen with temperature on the surface of copper at 1000^{o}C. The common practice is copper foil heat up until 1000^{o}C with hydrogen for 30 minutes. Than small rate of flow for the methane come later with 30 minutes' time as the carbon source gas. Then the copper is cooled down until room temperature. The graphene growth is robust and transparent.

Figure 13: cooper foil insert into CVD machine and Graphene growth on copper foil

5.3.5 Transfer Mechanism Graphene

Graphene on cooper need to be etch and transfer to our desire substrate example in my case is silicon dioxide. A few methods of transition have been demonstrated such as polymeric foils (polyethylene terephthalate (PET)). The objective is to let the graphene membrane free and to be scooped by substrate. The copper first spin-coat with a top layer of polymeric layer example in this case I use poly (methyl methacrylate) (PMMA). This layer is used to provide support for the membrane later in duration of transfer so that the graphene is not break or tear out. The copper then will etch away by Using iron chloride ($FeCl_3$) solution. The copper will dissolve into solution and only left graphene membrane on top of the solution layer. Graphene now can be scoped into subtracted.

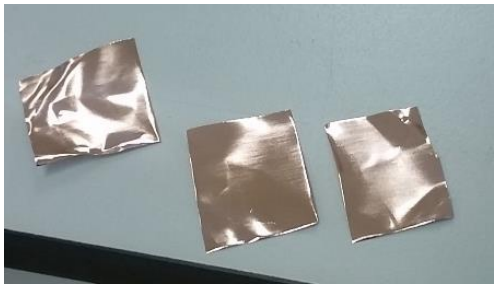


Figure 14: Copper foil cut into a few pieces of desired size.

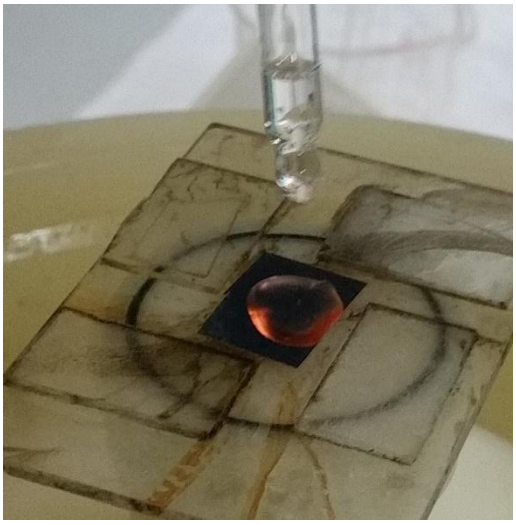


Figure 15: PMMA layer on top of cooper for support of graphene when etched.

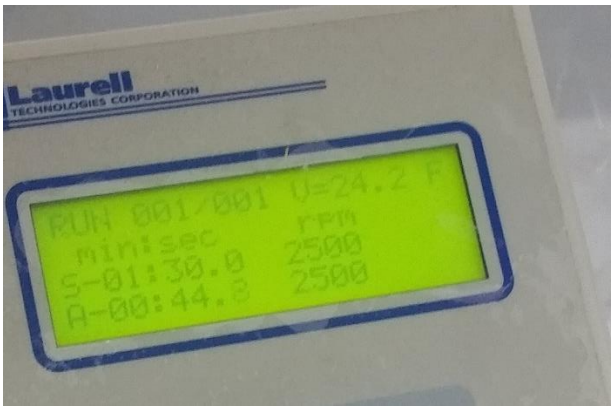


Figure 16: The sample then spin coated with above setting.

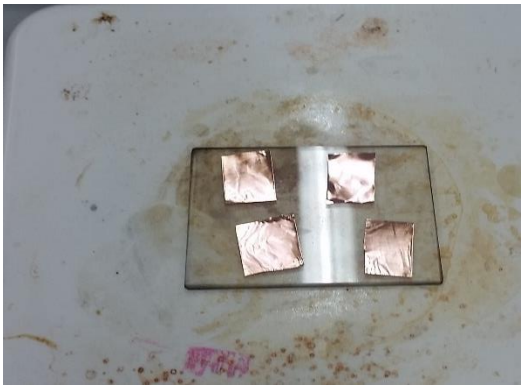


Figure 17: The copper then heated up with 90C

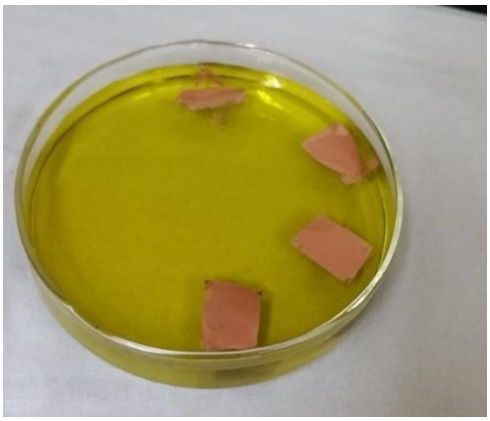


Figure 18: Etched cooper in solution iron chloride

Figure 19: Silicon dioxide after scoped with graphene.

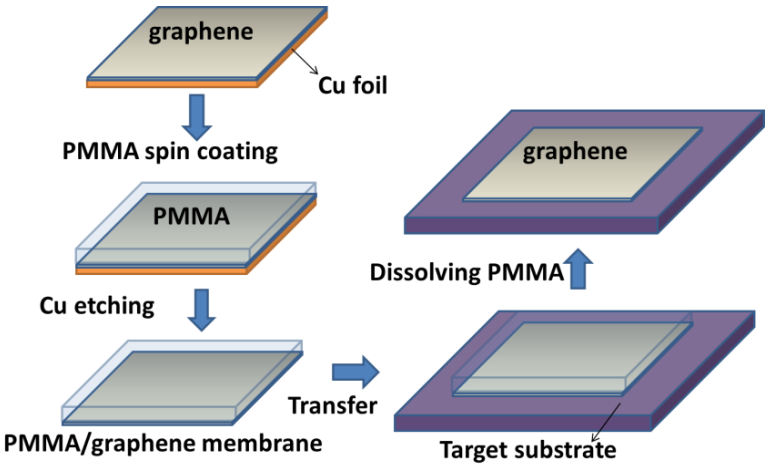


Figure 20: Illustration of transfer

All this method left a few impurities to that graphene. In way of scooped, the graphene may defect structurally, crack, wrinkles and ripples. The PMMA layer is hard to be remove then the graphene membrane quality is drop which will affect yield, uniformity, and performance. Further process need to be done such as PMMA heating, substrate treatment and chloroform cleaning to return back the quality of graphene and natural properties.

5.3.6 Sputtering Electrode

Sputter deposition is a physical vapor deposition (PVD) method of thin film deposition by sputtering it onto substrate. In this case, I was using magnetron sputtering which one of PVD technology in PVD coating technology. The idea is shot out atom from the element in front of gun sputtered. The ion beam will be shot the element in atom and deposit in top of substrate. In order to select which area/region to be select for sputter. Unwanted area need to be closed on top of substrate.

Illustration of sputtering illustrate below. The thickness of deposited masking is depended on type and plasma density.

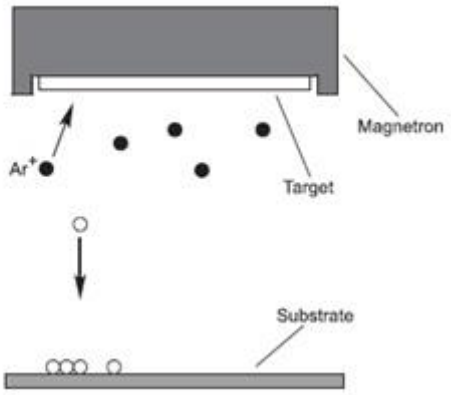


Figure 21: Magnetron sputtering illustration of shooting target atom to substrate.

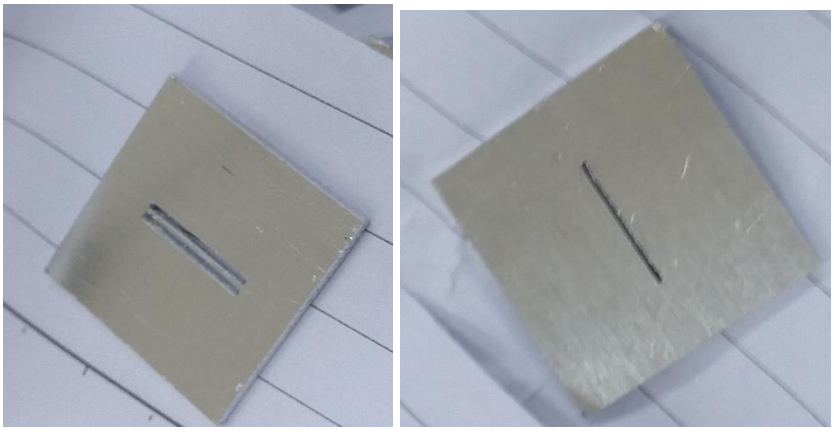


Figure 22: Masking used to make electrode. The exposed area will deposit the target onto substrate.

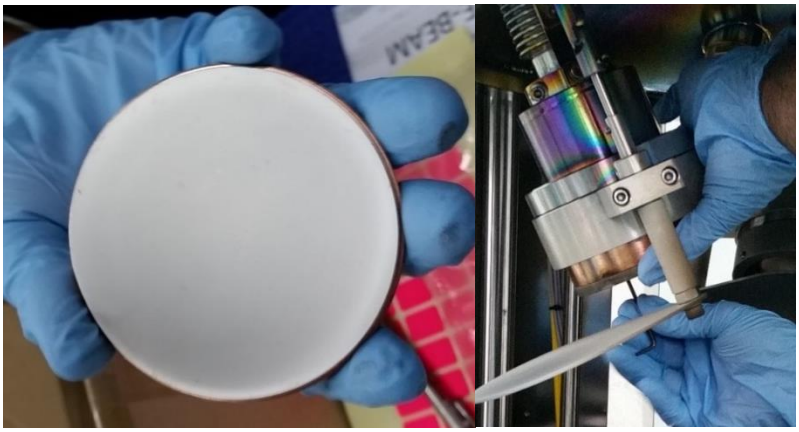


Figure 23: Target element that being installed in front of sputter gun.

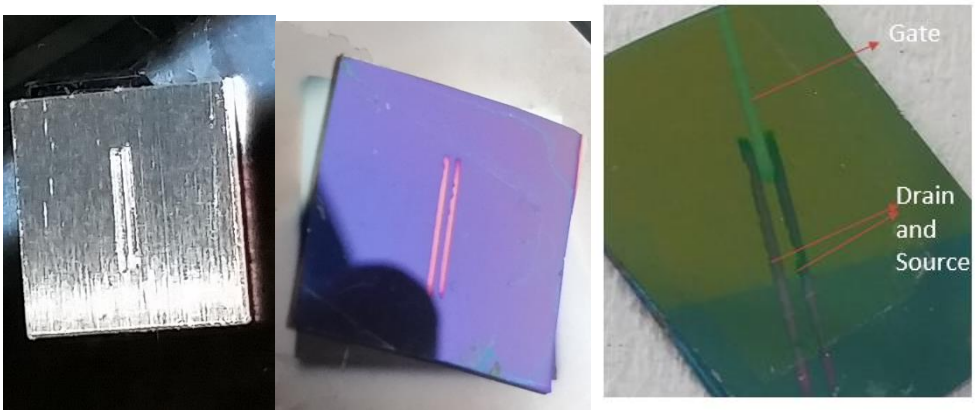


Figure 24: Drain and Sources electrode deposit in top silicon dioxide and graphene using cooper target.

Final form G-FET with gate in the middle and D-S side by side. The layer between electrode is deposited using Aluminum Oxide for 12 minutes and 3minutes for coppers electrode. Different thickness achieved base on variation of time. Process flow of option 1 process flow show in tabular form can be referred in appendix.

5.4 Process fabrication of Option B

Unlike option A, the resources are only used that available only in UTP. Because UTP don't have a few machine examples for lithography this fabrication was done at Adtech Taiping. A process of concept on how the process can be done can be referred in appendix.

Most of process done were exact same as the previous option A but only a few change of design and using photolithography methods for etching the oxide layer. Another different is oxide layer insulator in this design is silicon dioxide which have dielectric constant 4.2.

The main fabrication step is divided into 5 step: (process flow in appendix with pictures)

- Wet oxidation
- Diffusion process
- Formation of gate oxide
- Graphene Transfer and Lift-off
- Contact electrode deposition and lift-off

In this test, the wafer specification used as below:

- Wafer grade: Test
- Native Dopant: Phosphorous (n-type)
- Resistivity: 7.0 – 10.5 ohm-cm
- Sheet Res: 109.2k ohm/sq
- Native Oxide: 130.7nm
- Orientation: 1 0 0

Final form in 3D illustration of GFET

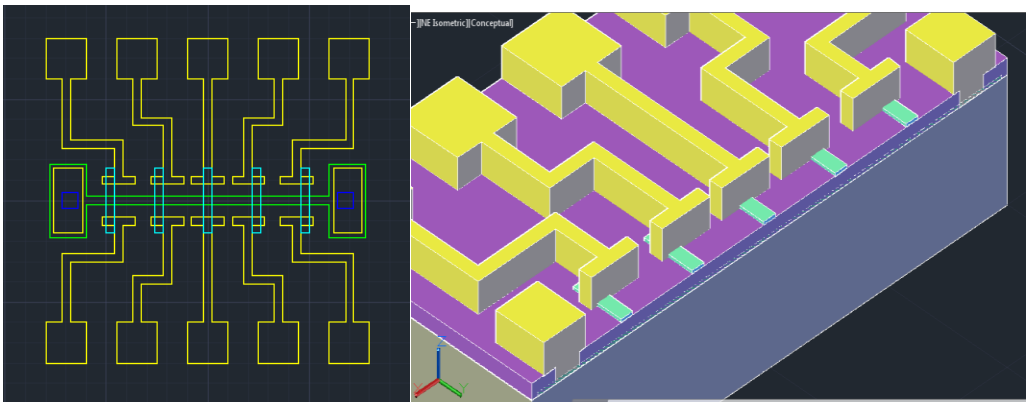


Figure 25: schematic of device

Actual device under microscope with 5 channel with channel length of 50um (mark in red line)

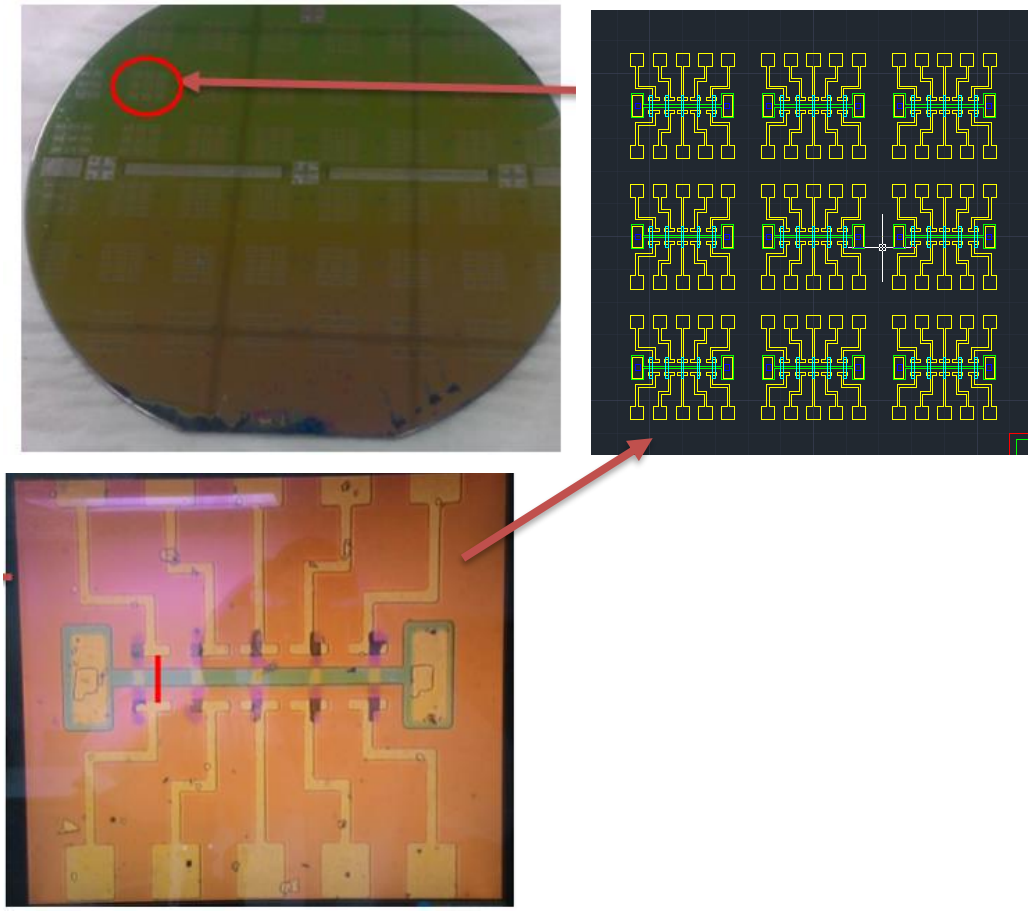


Figure 26: Actual devices

5.5 Measurement and Circuit Configuration for Characterization of G-FET

Setup of the circuit as shown below.

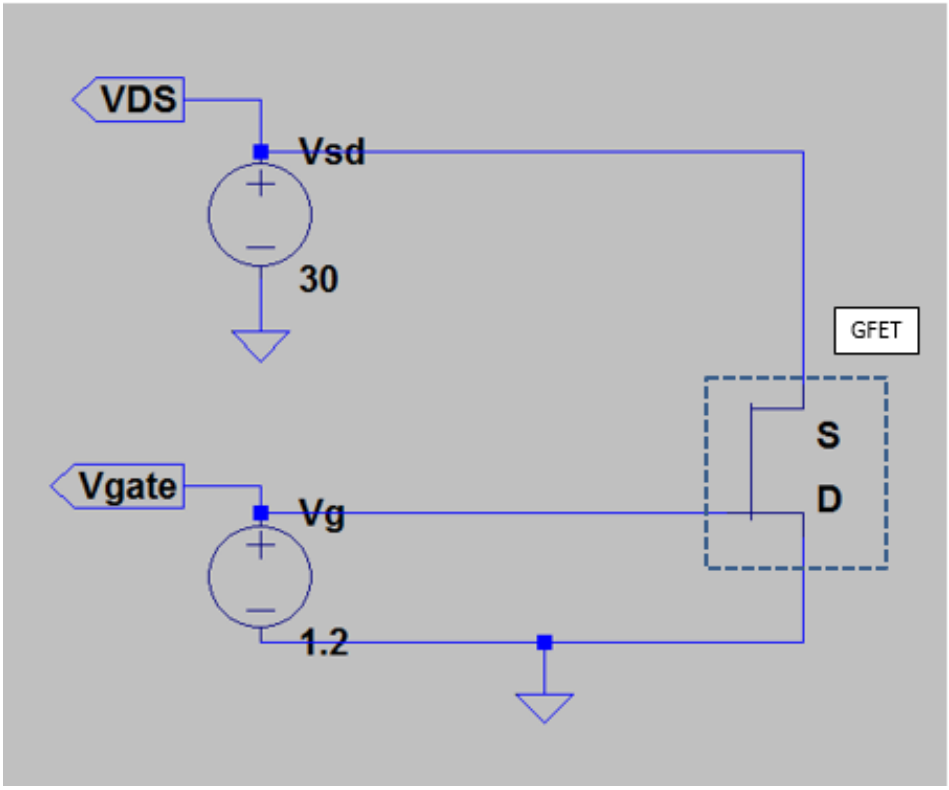
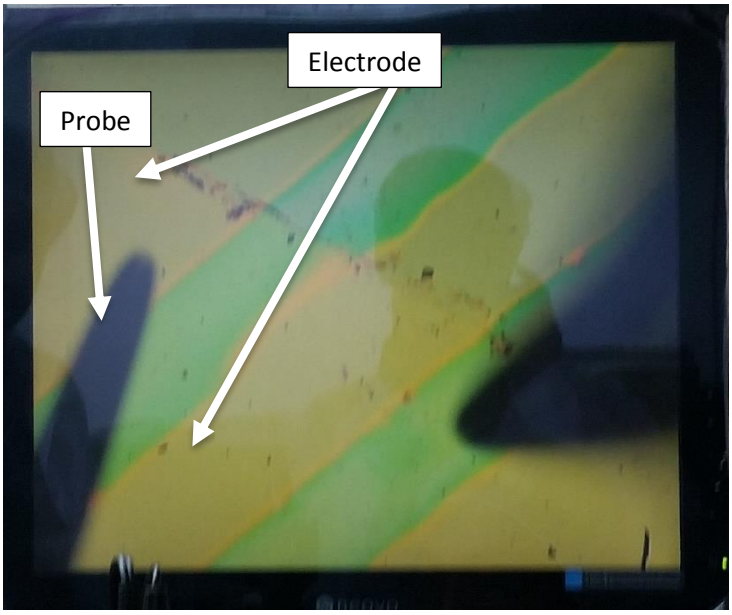


Figure 27: The setup circuit connected to bench power supply to variable the voltage supply.

The Vg will various from -10 to +10V and the current from source to drain is measured with increment of 0.1V of every gate voltage.

Figure 28: Measuring G-FET characteristic used Agilent B1500A



Figured 29: Touched probe to electrode of G-FET under microscope

6.0 RESULT AND DISCUSSION

6.1 Raman Spectroscopy

In order to confirm there was a single layer graphene flake used, Raman spectroscopy was applied. The electrical measurement was done by standard shielded probe station and Keithly 4200-SCS analyzer for characterization of fabricated devices. Raman spectroscopy is one of the famous method that provides fast and reliable tool to determine the single-layer, multilayer graphene or graphite. Raman spectroscopy is considered a key tool for identification and characterization in graphene research [14]. By using Raman spectroscopy, the graphene layer and their quality can be studied. For confirmation of single layer graphene flake, Raman spectroscopy with Horiba LabRAM used as the channel in GFET.

The test conducted under room temperature with laser sources of Argon. The laser aimed to the silicon with graphene on top. The result shown in figure below. The resulted from the spectrum show that a single 2d peak at 2700cm^{-1}. It confirms and show that the single layer graphene in this channel.

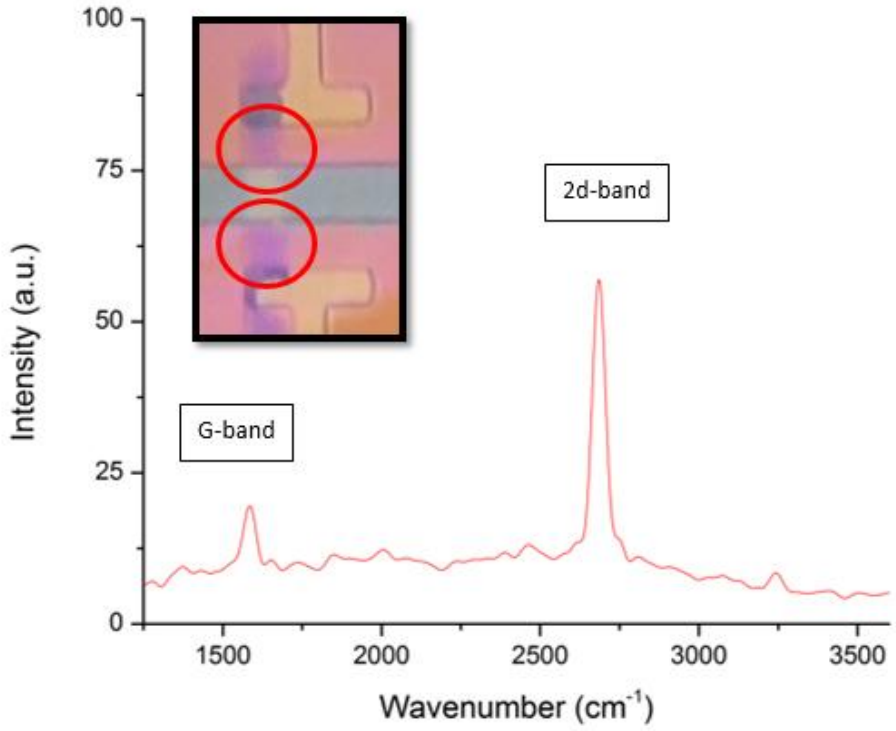


Figure 30: Raman shift spectrum of 2d band graphene flake single layer confirm on circle picture

6.2 Option A result and discussion

After a few fabrications and failed, the result of GFET of I-V characteristic failed and not shown as expected. Below a few pictures that show the GFET is short circuit. In this design insulator used Al_2O_3 with dielectric constant 11.54.

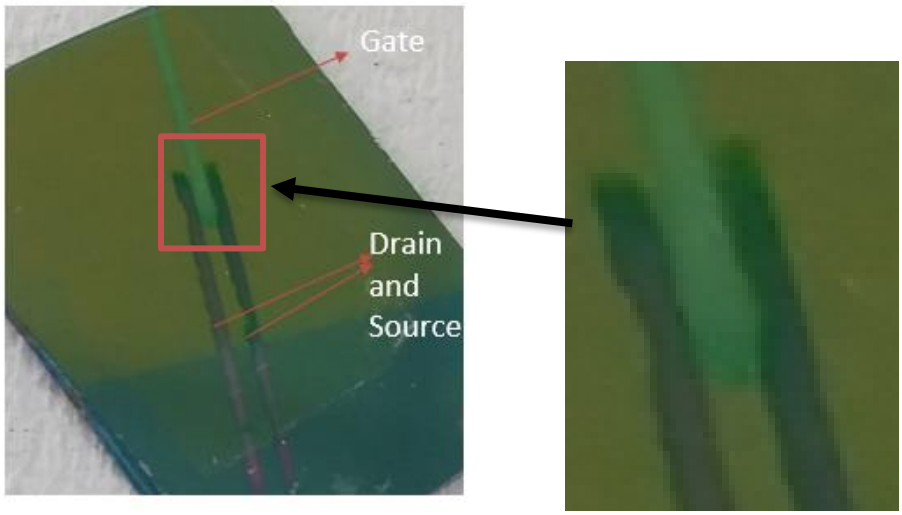


Figure 31: The gate and D-S electrode have small effect region for electromagnetic field effect

Based a few analyses and expected failure, the GFET probably don't have enough (too small area) for the FET to act as field effect to switch on the FET. Another factor is miss align the gate electrode placement. This cause the only a few parts of graphene only activated.

Figure 32: miss align electrode

-

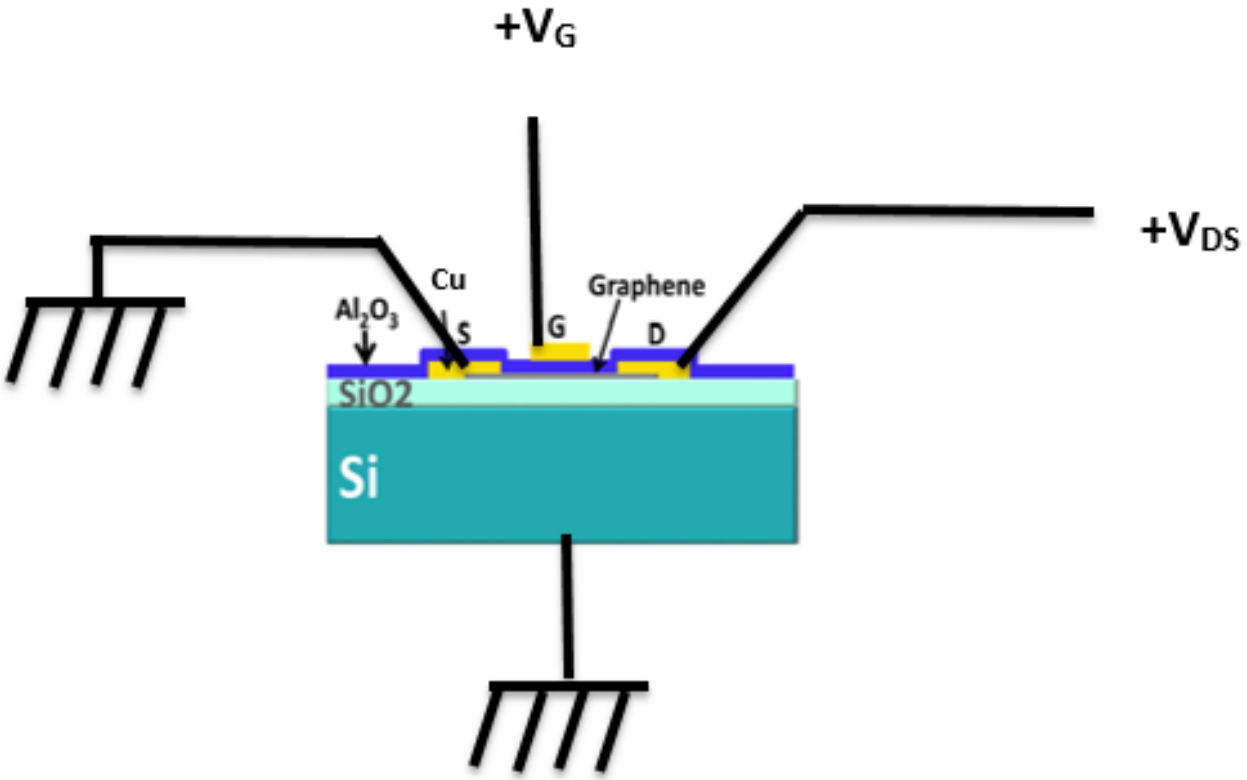


Figure 32: Circuit constructed for GFET test.

The hard mask was design is 500um width for all electrode. Due to alignment factor, the gate electrode will not place exactly between drain and source electrode. Only a few regions that overlap with gate will only activated the graphene to conduction band.

Another factor is material for electrode. As proposed early the electrode is using gold which have lower resistance and ohmic contact. However the cost matter make it impossible to buy the gold sputter target.

6.3 Option B result and discussion

The option B used SiO_2 as the insulator of dielectric between gate and drain-source. The GFET then measure with same setup circuit and parameter of previous GFET. The graph shown as figure below.

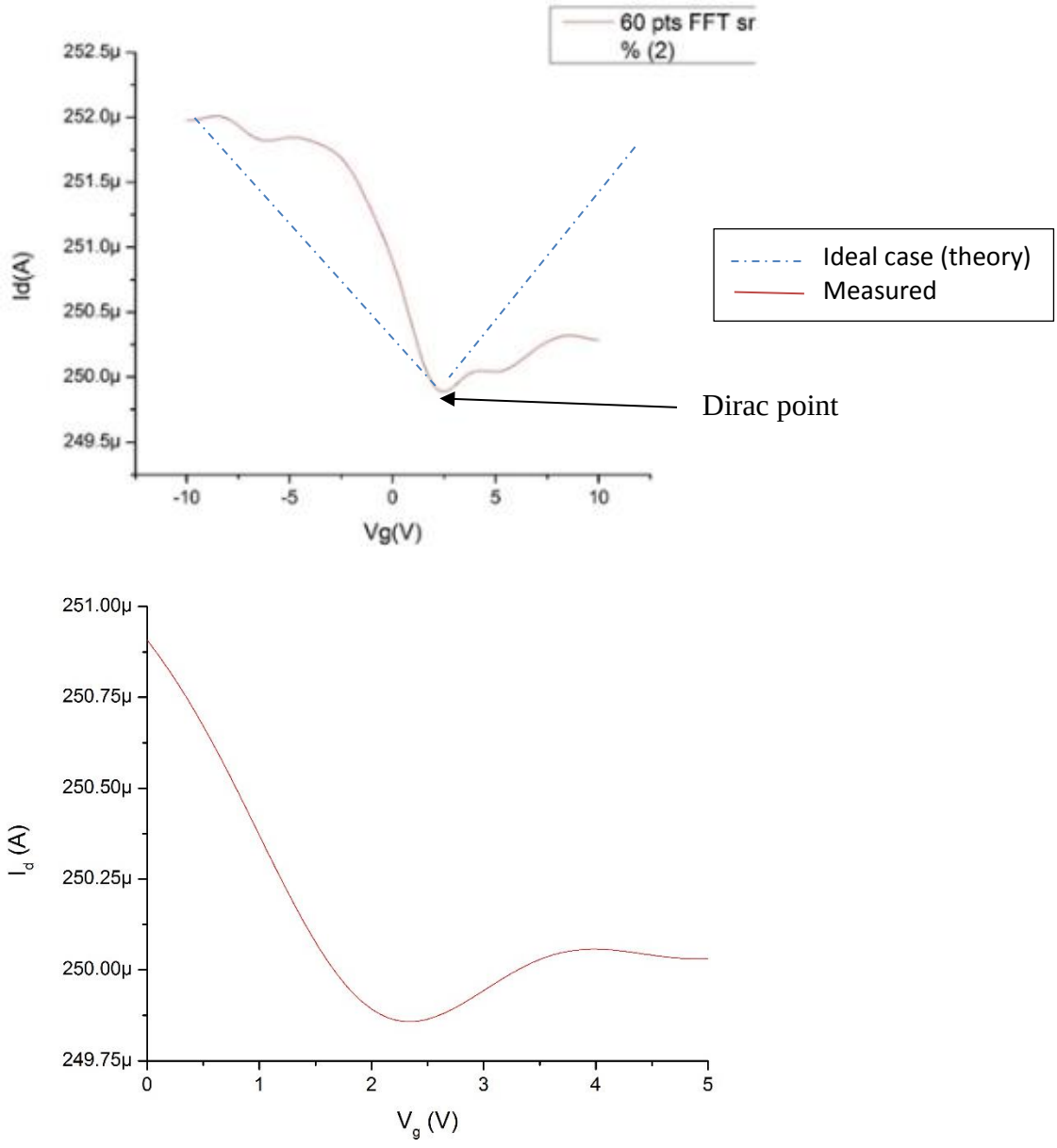


Figure 33: The drain current modulated almost symmetrical to the gate voltage.

The drain current modulated almost symmetrical to the gate voltage with the shifted amount of offset 2.5V. In ideal case, the Dirac point should fall at 0V. However, a

few factors such as wrinkle during graphene scoop and ununiform of growth silicon dioxide could affect the shifting of Dirac point. The "V"- shape curved show the characteristic of the GFET transport ambipolar behavior. The result of outcome from the GFET is ideal when (Vds<Vgs-V0). Due to the gapless property of graphene, GFET tend to exhibit ambipolar behavior at region of charge carriers change from electron to holes or otherwise at a minimum conductivity. This point called a Dirac neutrality point. (the point where the bottom point of shape of "V"). The ideal shape of V may infect by the structure and device fabrication GFET due to impurities during fabrication and other factor as well. Unlike other material that exist in 3D, graphene consists only a single layer of atom. Intrinsic graphene is a semimetal (semiconductor which have zero band gap). the E-k relation is linear for low energies near the six corners of the two-dimensional hexagonal Brillouin zone, leading to zero effective mass for electrons and holes (can be referred to figure 34 about hole and electron conduction which met at only one point).

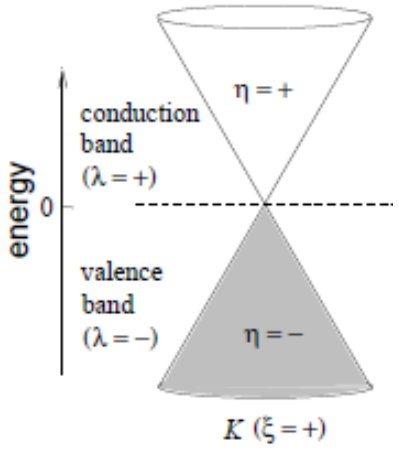


Figure 34: conduction band and valence band met at only one point.

In a century, a few models of formula to simulated the current voltage characteristic have been proposed. For example, the model below (1-2), describe the drain current components which have constant charge carrier mobility.

$$I_d = \frac{W}{L}\mu C_{ox}\left[(V_{gs} - V_0)V_{ds} - \frac{V_{ds}^2}{2}\right] \qquad (1\text{-}2)$$

This equation practically used same as convectional MOSFET except for V_0 which is the Dirac neutrality point. Due to inhomogeneity and thermal excitations there must be minimum conductivity point (took as transport model) much larger than the universal minimum conductivity.

The Vgmin shifts from device to device, indicating that the fabrication process cannot achieve consistency. Probably because graphene doesn't not shear off properly and Lift-off method introduces unwanted localized stresses, forming cracks and wrinkles as see in the following picture. Gate electrode isn't consistent as well, as I have investigated by conducting fixed voltage on random sites and getting slightly different currents from point to point. There's a whole lot of fluctuations. Probably due to poor connections and perhaps expired measurement tip.

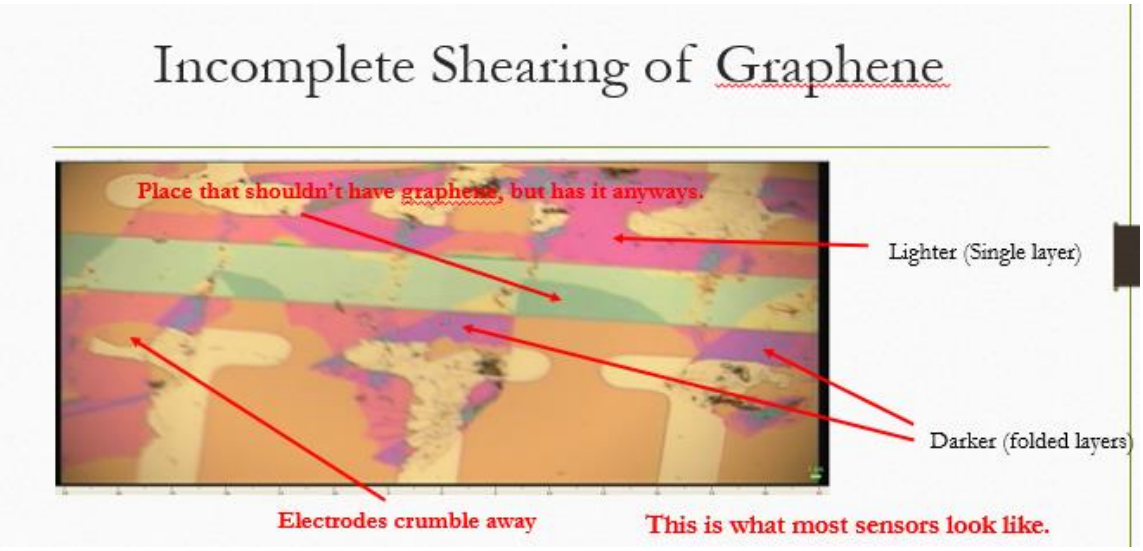


Figure 35: Failure on some FET factor due to incomplete shearing of graphene.

7.0 FUTURE WORK

One of suggestion if hard mask need mask aligner so that the device and mask are in align especially for gate electrode.

Connections of Agilent probes aren't properly secured. Will need female to female adapter to make that work. Each cost $28.95. We need four to make proper connection directly to the SMUs. Plus, delivery and that would be about $300, which means RM1300. (Kind of expensive.). By the way, I've searched all the places that I can think off in UTP but there's none.

Bad Wafer. The wafer used is test grade. It shouldn't affect much, but we never know. Prime wafer costs about >RM300 a piece though.

Poor device design. My gate should be properly degenerated via Phosphorous doping, but at high voltage, it suffers leakage as illustrated in the following graph. My graphene is really not that properly etched. Lift off method really isn't that good on graphene. There's a lot of debris and contaminations. Cleanroom & RIE should prove to be useful but we don't have that.

Non-ohmic contact between graphene and metal contact. Using gold might solve the problem but one piece for magnetron sputtering is RM5000. So, not solvable at the moment.

In future, the fabricated transistor will be test on transparent and flexible surface. Then the circuit will be go through a few bend tests and remeasure. The properties of device/ FET must be able to maintain after a few tests.

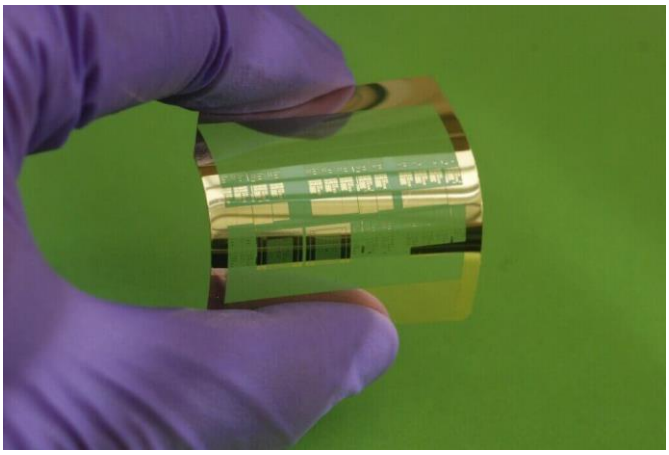


Figure 36: Transistor on flexible and transparent surface material

8.0 GANTT CHART

The total duration of FYP 1 and II is 7 month. The experiment will be conducted after week 7. Below the Gantt Chart for whole FYP.

ACTIVITIES	WEEK																												
	1	2	3	4	5	6	7	8	9	10	11	12	13	**14**	1	2	3	4	5	6	7	8	9	10	11	12	13	**14**	**15**
	SEM 1														**SEM 2**														
Selection of Project Title																													
Identifying Objectives and Scope of Study																													
Preparing Project Ganttchart, Key Milestone, Process																													
Discussion on Fundamental Knowledge																													
Literature Review																													
Collecting Data Material																													
Listing a few of GFET design																													
Lab booking																													
Submit design hardmask for fabrication																													
Submission of Extended Proposal																													
Dicussion on GFET design and material used																													
Proposal Defence and Progress Evaluation																													
Finalise GFET to be used and material available																													
Drafting Interim Report																													
Submit Interim Report (to SV)																													
Submit Interim Report (to Examiner)																													
Fabricating the GFET from silicon wafer																													
Growth graphene and transfer																													
Refabricate GFET after a few fail																													
Analysing Data and characterization																													
Progress Report Submission for reviewing by SV																													
Submit Progress Report																													
Poster Preparation																													
Pre-Sedex																													
Submit Draft Final Report																													
Technical Paper Writing																													
Submit Technical Paper for reviewing by SV																													
Submit Technical Paper to Examiner																													
Dissertation Writing																													
Dissertation submission (softbound)																													
Viva																													
Submit (hardbound)																													

Table 3: Gantt Chart table for FYP II

WEEK	W2	W3	W4	W5	W6	W7	W8	W9	W10	W11	W12	W13	W14
ACTIONS													
Identify parts that need help (fabrication)													
Find people/sources that can help to solve (Salleh/Dr.Vira/ Hoe Chee etc)													
Hard mask redesign and submit to block 16													
Fabricate GFET													
Graphene gorwth and transfer													
Refabricate GFET													
Characterization of GFET													

Table 4: implementation plan on FYP II

9.0 PROJECT KEY MILESTONES

The following table shows the key milestones of this project:

No.	**Activity**	**Complete in**
1	Progress Report submission	Done
2	PRE-SEDEX	Done
3	Draft Report	Done
4	Final Report and Technical Paper	Done
5	VIVA	Week 15

Table 5: Key milestone of FYP II

10.0 CONCLUSION AND RECOMMENDATION

A graphene-based FET is fabricated successfully by employing layer-by-layer techniques. The graphene is synthesized using CVD technique followed by transfer onto Si wafer. The metal is deposited on the graphene by using sputter deposition with masking plate. Moore's Law is hitting the wall and silicon fabrication in transistor is no longer valid due to the shrinking physical size limitation. Shortly after discover of graphene, this material explored to be used in many applications. Due to it exceptional limitation in a few properties, GFET has a great potential in future in replace of convectional MOSFET. However, to grow and development of graphene is quite challenges. The biggest challenges are fabricating well-controlled graphene for device manufacture. At this moment, CVD process is the best technique to solve this problem.

11.0 REFERENCES

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94, 0786802 (2005).
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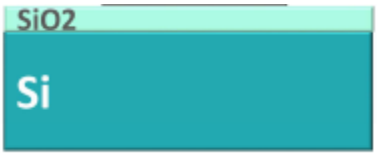
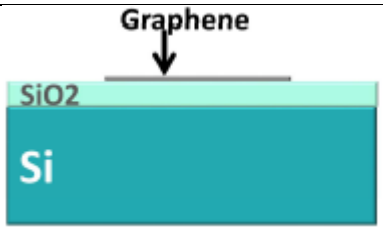
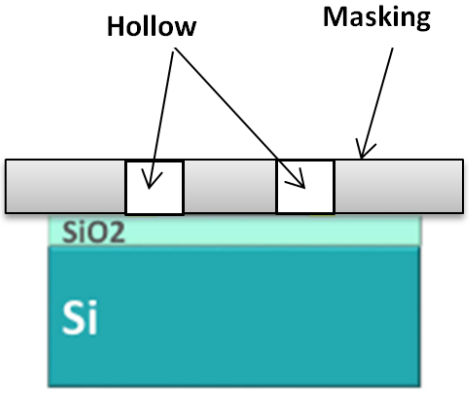
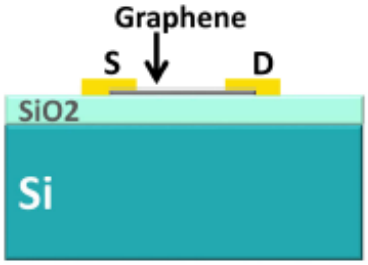
12.0 APPENDICES

Process flow for option A procedure

Step	Procedure	Image
1	Grow silicon dioxide on silicon wafer. Thermal oxidation of silicon performed at a temperature between 800 and 1200 °C. Use either water vapor or oxygen molecular for oxidation. $Si + O_2 \rightarrow SiO_2$ **Grow thickness: 90nm-100nm**	
2	Transfer graphene.	
3	Place D-S mask on top of silicon. Deposit electrode (gold) for drain and sources using PVD **Coppers thickness: ~80nm**	 

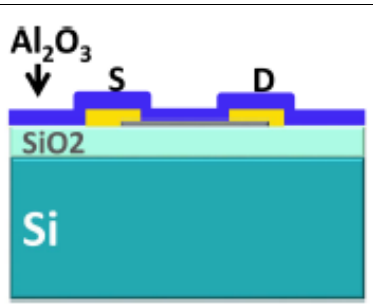
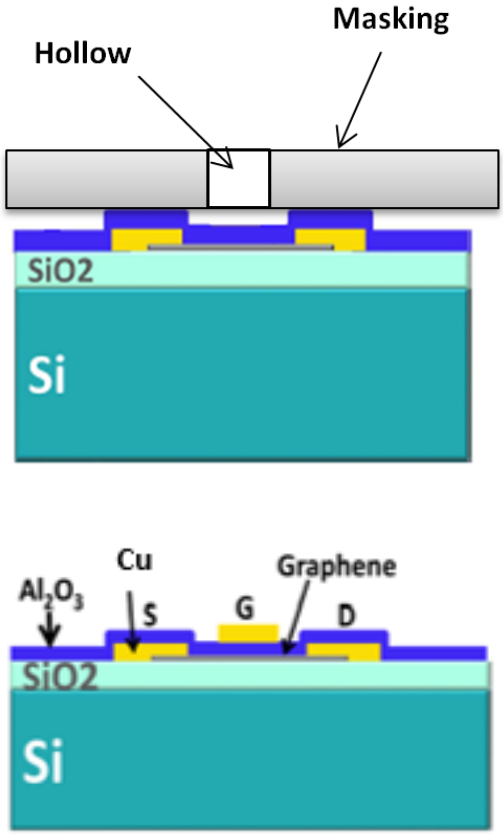
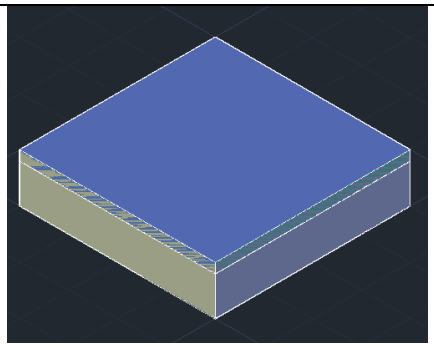
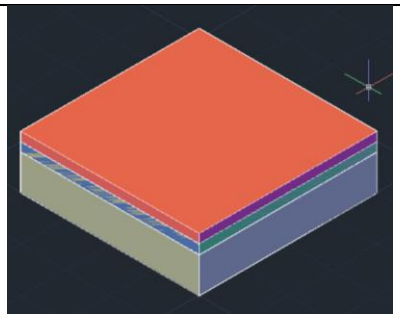
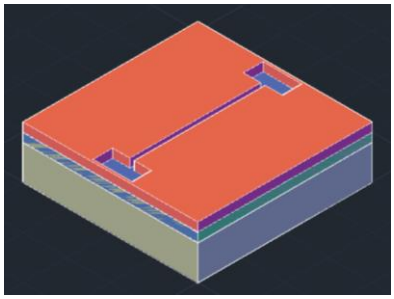
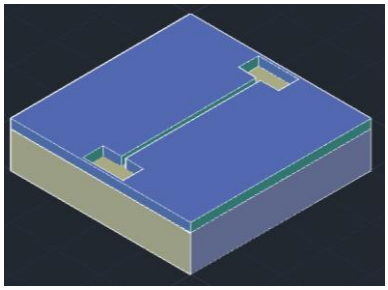
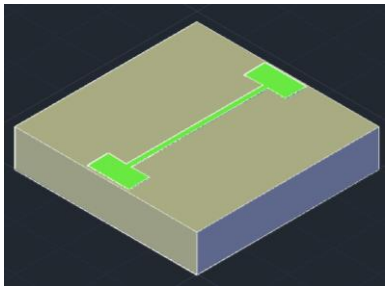
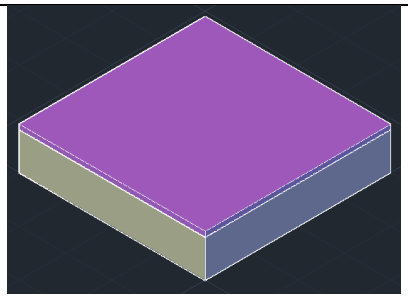
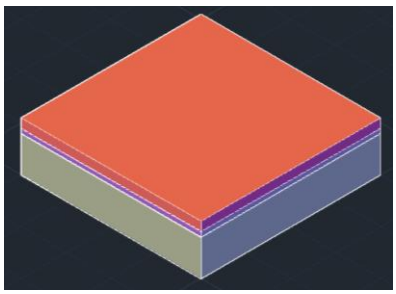
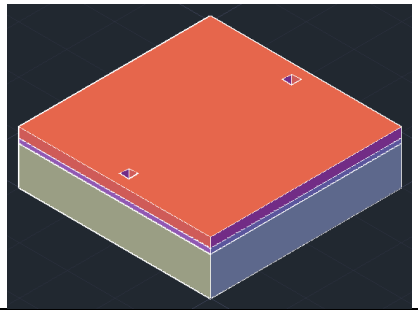
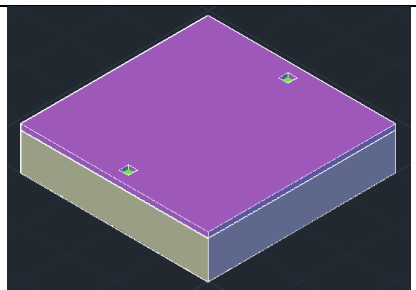
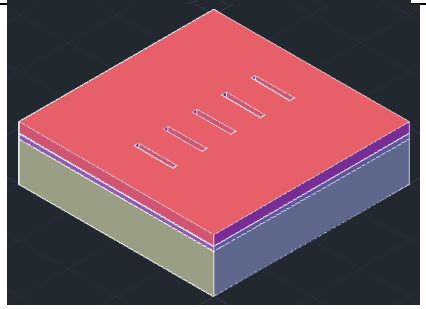
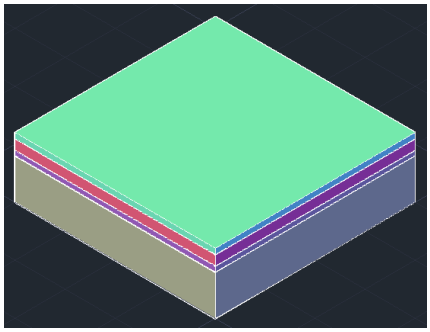
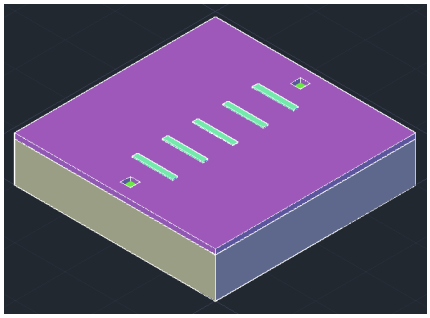
4	Al2O3 deposit using PVD All the area is exposed except the end of electrode that need be tap later as contact point **Al2O3 thickness: ~50nm**	
5	Deposit electrode gate The unwanted area is cover by aluminium plate. **Coppers thickness: ~80nm**	

Table 3: Process step and picture of fabrication

Process flow for fabrication option B

Step	Procedure	Image
1	Wet oxidation • BOE to remove native oxide & cleaned with DI water. • Wafer inserted into furnace tube at 700C under 400sccm N_2 environment. • Temperature ramped up to 1000C and 400sccm O_2 is introduced. • Oxidation process is 1 hour. • Oxide thickness = 387.8nm.	
2	Photolithography (Gate)	  

3	Diffusion process • Wafer placed in diffusion furnace at 700C under 400sccm N_2 environment • Furnace ramped up to 1000C with Phosphorous Chloride (n-type doping) source approx. 5mm from the wafer. (N_2 flow rate remains unchanged) Diffusion process is 2 hours	 *(Green : highly doped region)*
4	Formation of gate oxide (Dry Oxidation) • Wafer is inserted into oxidation furnace at 700C under 400sccm N_2 environment • Temperature is ramped up to 1000C. • 450sccm O_2 is introduced into the furnace • Process of oxidation is 45 minutes • Gate oxide thickness = 124.4nm	
5.	Photolithography (Gate Window) • Gate window is formed to allow direct contact of metal on the gate electrode.	 

		
6.	Graphene Transfer and Lift-off • Photolithography is done to pattern out the desired channel dimensions. • Graphene is transferred on top of the photoresist and baked for proper adhesion. • The substrate is immersed into acetone for 2 hours to remove the PR, PMMA and excess graphene *(red : photoresist ; grey : silicon ; purple : gate oxide ; turquoise : graphene)*	  
7.	Contact electrode deposition and lift-off • Photolithography is done to pattern the desired electrode dimensions • Nickel is sputtered onto the substrate. • The substrate is immersed into acetone to remove the photoresist and excess metal *(red : photoresist ; purple : gate oxide ; grey : silicon ; yellow : nickel)*