LIST OF PUBLICATION

The research work in this thesis was presented and published in official proceedings of rigorously referred conferences through the following research papers:


APPENDIX A

DAC BURN-IN PLAN

The burn-in board matrix is customized specifically to stress the DAC circuit. The original intent of building the burn-in board was to use for a specific product sample but for this special experiment, the emphasis is on stressing the DAC circuit. Trace impedance of all channels is controlled to allow operation of the signals operating at 10 MHz, low frequency. The output monitor signal (DAC out) is to be brought out to the burn-in board edge connector for the BI socket through a 100 ohm series resistor. The purpose is to facilitate the debug of DAC burn-in.

This special DAC BI is structurally exercised with DAC power supply at elevated voltage of 4.6V (VCC DAC). Other power supplies which are not to the interest of this experiment are core power supplies at 1.6V (VCC Core) and I/O power supplies at 2.5V (VCC I/O) The reference voltages are set to 1/2 VTT, 1/2 VDD, or 2/3 VCC depending on the interfaces. A dedicated burn-in system supply is used for the 4.6V source. A resistor divider is used to acquire proper reference source. The BI frequency under BI mode is 10 MHz. Each of the product samples is laid to support single voltage supply requirement.

A series of inexpensive discrete components is mounted on a burn-in board (BIB) to stimulate, and monitor a new on-die burn-in stress mode for DAC. This is to make each burn-in board a self-contained independent stress module. To accomplish this; the Design-For-Test (DFT) mode is entered using a strapped pull-up resistor to a power plane in conjunction with toggling the input signals. The on-burn-in board circuits will include two signals, which will be tapped off of a crystal using an RC time constant to supply input stimulus to a discrete 16-bit shift register, this will provide 900 phase shifted clocks to the device. These clocks will vary the sample product’s operational frequency and junction temperature. Monitoring will use blinking Light Emitting Diodes (LED), which will give a visual reference that the DAC burn-in mode is operating properly.
BI testing is enabled when the video DAC is programmed for the triangle pattern mode with a special DAC input pin. The way the pin works is tracked by its bit from 0 to bit 2.

With this test mode activated, the video DAC internal 8-bit up/down counter is enabled and produces a triangular input data pattern (ramp 00 to FF and then ramp FF to 00 hex and repeat) that is muxed to the inputs of all three DAC channels.

This provides full-toggle coverage of the video DAC for burn-in testing. As the 8-bit counter reaches its terminal count value, either FF or 00 hex, a status signal from the video DAC embedded block transitions.

A special indicator signal will be the key to indicate the status bit intended for end of burn-in testing.

There are two flavors for executing this DAC test mode, the burn-in mode which also requires the PLL to be turned off and placed in the 1X bypass mode, and the mode which is the default DAC burn-in test mode that depends on the PLLs.

DAC burn-in is activated by setting test selects and strobing test enable when hardware test mode has been activated.

Once activated the following test mode conditions are applied:

- All clocks are ungated. (open)
- All scan-out buffers and the burn-in monitor output buffer are enabled.
- The Linear Feedback Shift Register (LFSR) monitor buffer is enabled. LFSR is a shift register whose input bit is a linear function of its previous state.
- The remaining buffers are tristated.
- The pull-ups and pull-downs are turned off.
- All clamps are turned off.
The tri-state buses are grounded. This mode is not cumulative. Figure A.1 shows a high level DAC specific BI block diagram.