

FINAL EXAMINATION MAY 2024 SEMESTER

COURSE :

TEB1024 - COMPUTER SYSTEMS

DATE

1 AUGUST 2024 (THURSDAY)

TIME

9:00 AM - 12:00 NOON (3 HOURS)

INSTRUCTIONS TO CANDIDATES

- 1. Answer ALL questions in the Answer Booklet.
- 2. Begin **EACH** answer on a new page in the Answer Booklet.
- 3. Indicate clearly answers that are cancelled, if any.
- Where applicable, show clearly steps taken in arriving at the solutions and indicate ALL assumptions, if any.
- 5. **DO NOT** open this Question Booklet until instructed.

Note

- i. There are **SIX** (6) pages in this Question Booklet including the cover page
- ii. DOUBLE-SIDED Question Booklet.

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a. Illustrate the elements involved in an Input-Process-Output (IPO) model.

[2 marks]

b. Describe the role of Storage component in an IPO model of a computer system.

[4 marks]

 Consider the digital circuit diagram shown in FIGURE Q1 where A, B, C are the inputs and Q is the output.

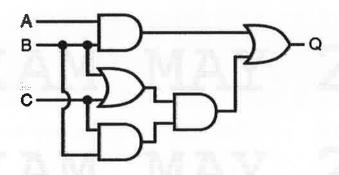


FIGURE Q1

Write the Boolean expression of Q.

[3 marks]

ii. Construct a complete Truth Table for the output, Q.

[7 marks]

d. State and verify the **TWO** (2) DeMorgan's theorems by means of Truth Tables.

[4 marks]

2. a. i. Explain **ONE** (1) benefit of 1's complement number compared with sign-and-magnitude representation.

[2 marks]

ii. Explain ONE (1) benefit of 2's complement number compared with 1's complement number representation.

[2 marks]

b. Complete the addition of the two-signed decimal numbers, -23 and -104
 by using a 10-bit 1's complement representation.

[8 marks]

- c. A computer system operated using decimal digits. The system stored a floating-point number in a format of SEEMMMMM in excess-60. The sign is 1 for a positive number and 2 for a negative number. Based on the system specifications:
 - i. Compute the floating-point representation for the decimal number,-0.00002234657.

[2 marks]

ii. Complete the addition of the two floating-point numbers 26054321 and 25811223. Check your answer using the decimal number representation.

6 marks

 a. Discuss the concept of CPU registers in a modern computer with regards to the relevant components of Little Man Computer (LMC) model.

[6 marks]

b. Draw a flowchart that describes the steps in which LMC follows to fetch and execute a branch instruction.

[4 marks]

c. i. Describe the memory characteristics of the Von Neumann architecture.

[4 marks]

ii. Write an LMC program that finds a positive difference of two numbers.

[6 marks]

4. a. Differentiate between batch and interactive systems in terms of response time and how data enters the system.

[4 marks]

b. Explain TWO (2) issues in a relocatable dynamic partition system.

[4 marks]

c. Discuss ONE (1) issue in memory sharing within a computer system.

[4 marks]

- d. A job with four pages, namely A, B, C, and D is to be processed by a system that has only three available page frames. The job pages would be swapped into the page frames in the order: A, B, A, C, D, A, B, A, C, D, C. Using appropriate diagrams, determine how many page faults will occur if the following policies are used:
 - i. First In First Out (FIFO).

[4 marks]

ii. Least Recently Used (LRU).

[4 marks]

5. a. Explain the key responsibilities of Job and Process Schedulers by using a sketch of a state transition diagram.

[4 marks]

b. Differentiate between preemptive and non-preemptive scheduling policies.

[4 marks]

c. TABLE Q5 presents a list of jobs in a queue.

TABLE Q5

Arrival Time	0	1	2	3
Job	: A	В	С	D
CPU Cycle (ms)	7	4	2	5

Compute the average turnaround time of the jobs in TABLE Q5 using the following algorithms.

i. Shortest Remaining Time (SRT).

[4 marks]

ii. Shortest Job Next (SJN).

[4 marks]

d. Conclude your answers from part (c)(i) and part (c)(ii) in terms of the average turnaround time.

[4 marks]

- END OF PAPER -