UNIVERSITI
TEKNOLOGI
PETRONAS

FINAL EXAMINATION
JANUARY 2025 SEMESTER

COURSE	**:**	**EDB2033/EEB2013/EFB2013 - ANALOGUE ELECTRONICS/ANALOGUE ELECTRONICS I**
DATE	**:**	**17 APRIL 2025 (THURSDAY)**
TIME	**:**	**9.00 AM - 12.00 NOON (3 HOURS)**

INSTRUCTIONS TO CANDIDATES

1. Answer **ALL** questions in the Answer Booklet.
2. Begin **EACH** answer on a new page in the Answer Booklet.
3. Indicate clearly answers that are cancelled, if any.
4. Where applicable, show clearly steps taken in arriving at the solutions and indicate **ALL** assumptions, if any.
5. **DO NOT** open this Question Booklet until instructed.

Note :

i. There are **EIGHT (8)** pages in this Question Booklet including the cover page and appendix.

ii. **DOUBLE-SIDED** Question Booklet.

iii. **Graph paper and semilog papers will be provided.**

1. a. Consider the circuit shown in **FIGURE Q1a**. From the DC power source, V_{IN} of 40 V supplying to the circuit, identify voltages, V_{O1}, V_{O2} and currents, I_{IN} and I_{O2}. Both diodes are of Silicon (Si) type.

[8 marks]

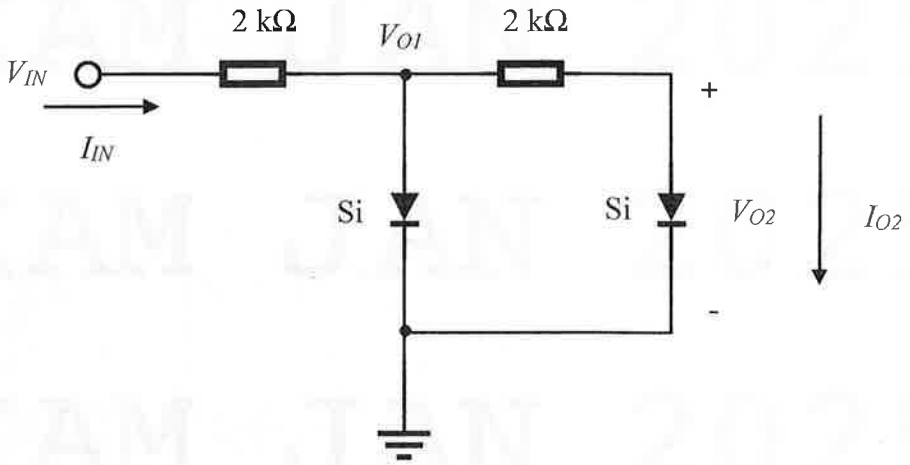

FIGURE Q1a

b. For the circuit shown in **FIGURE Q1b**, there are two separate independent DC sources connected in series with the diodes. Illustrate the current, $I(t)$ and output voltage, $V_O(t)$ for the AC input, $V_{IN}(t)=20\sin(\omega t)$ V.

[12 marks]

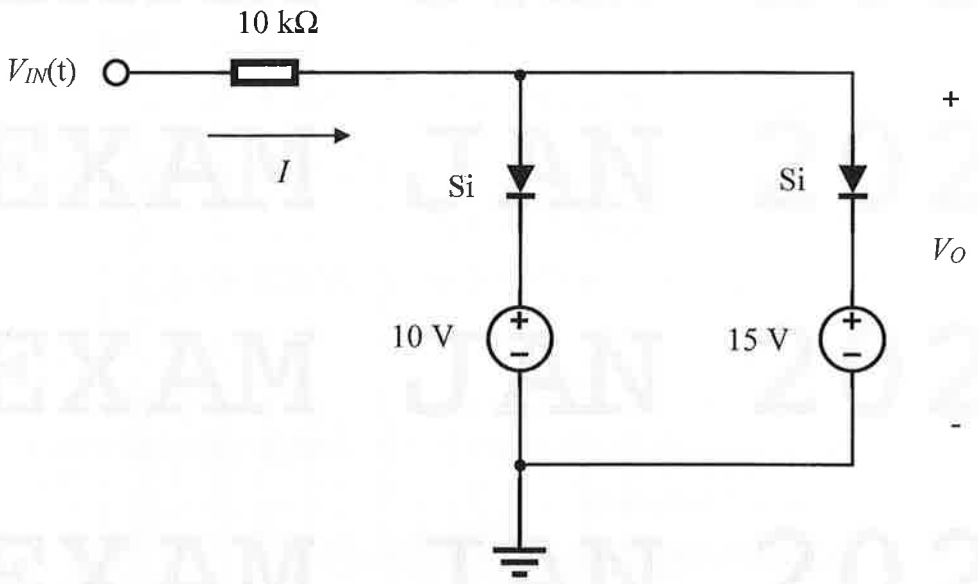

FIGURE Q1b

c. One of the roles using zener diode is to regulate the output voltage level. From the circuit configuration shown in **FIGURE Q1c**, estimate source resistor, R_S and voltage across zener diode, V_Z in order to regulate load voltage, V_L at 20 V for a load current, I_L, not exceeding 1 A.

[5 marks]

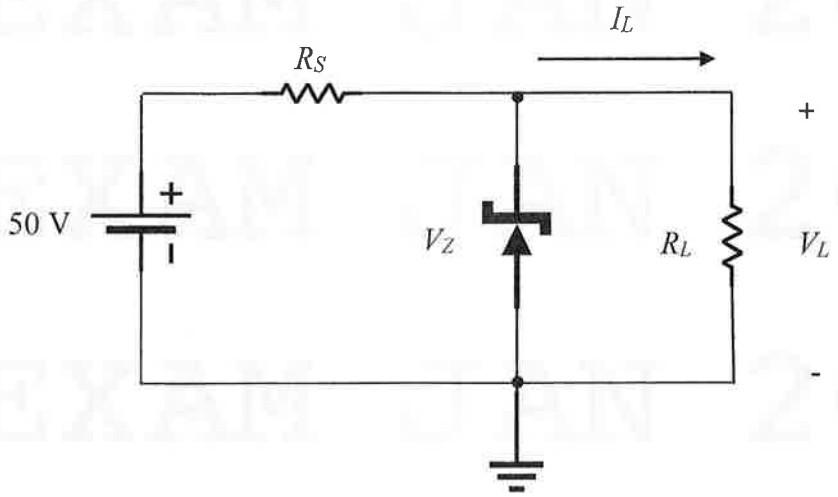

FIGURE Q1c

2. The emitter-stabilized Bipolar Junction Transistor (BJT) circuit is given in **FIGURE Q2**. In the preliminary design stage, there are several technical issues to be rectified. Engineers need to understand the role of each component's parameter and its value used in the circuit. If parameter values are wrongly chosen, the circuit operation will be affected.

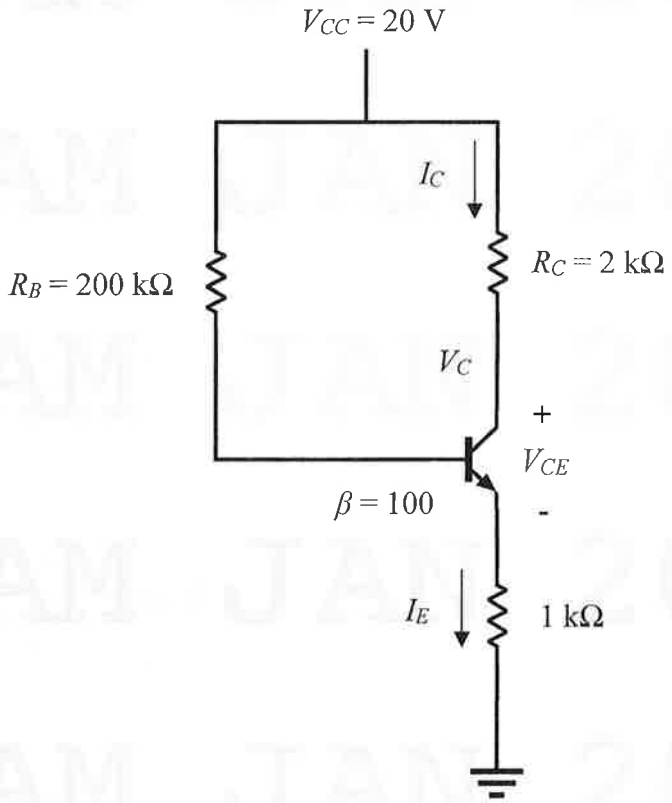

FIGURE Q2

Therefore, based on specific parameter condition, determine and justify analytically the following cases. Compare answers using original values in **FIGURE Q2**.

a. The collector voltage, V_C if base resistor, R_B is doubled.

[5 marks]

b. The base current, I_B if β is reduced to half.

[5 marks]

c. The saturation current, $I_{C,sat}$ if β is doubled.

[5 marks]

d. The collector-emitter voltage, V_{CE} if input DC, V_{CC} is reduced to half.

[10 marks]

3. Designing a network in frequency-based application may compromise output voltage gain if it is not carefully configured. **FIGURE Q3** shows a network using a D-MOS as a switch. By reviewing this network,

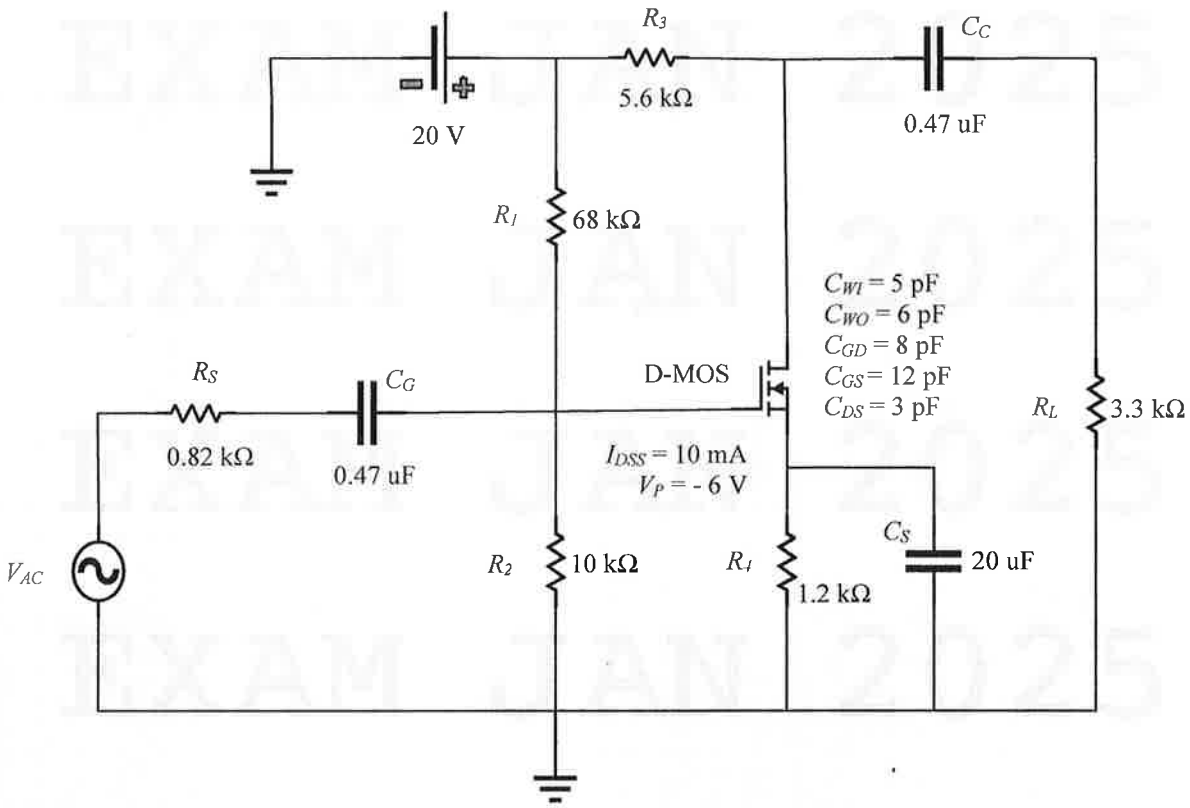

FIGURE Q3

a. predict the Q-point value using the graphical method,

[8 marks]

b. evaluate both cut-off frequencies at low and high frequency levels, and

[12 marks]

c. construct the bode-plot and show both cut-off frequencies on the semi log paper.

[5 marks]

APPENDIX

NPN BJT

$\beta_{RE} \geq 10R_2$	$r_e = \frac{26m}{I_E}$
$A_V = -\frac{(R_L \| R_C)}{r_e}$	$\frac{V_I}{V_S} = \frac{R_{IN}}{(R_{IN} + R_S)}$
$A_{VS,MID} = \frac{V_O}{V_I} x \frac{V_I}{V_S}$	$f_{LS} = \frac{1}{[2\pi(R_S + R_{IN})C_S]}$
$f_{LC} = \frac{1}{[2\pi(R_D + R_L)C_C]}$	$R_S{}' = R_S \| R_1 \| R_2$
$R_e = R_E \| [\left(\frac{R_S{}'}{\beta}\right) + r_e]$	$f_{LE} = \frac{1}{[2\pi R_e C_E]}$
$R_{TH1} = R_S \| R_1 \| R_2 \| R_{IN}$	$C_I = C_{WI} + C_{BE} + (1 - A_{VS,MID})C_{BC}$
$f_{HI} = \frac{1}{[2\pi R_{TH1} C_I]}$	$R_{TH2} = R_C \| R_L$
$C_O = C_{WO} + C_{CE} + (1 - \frac{1}{A_{VS,MID}})C_{BC}$	$f_{HO} = \frac{1}{[2\pi R_{TH2} C_O]}$