SIGNAL INTEGRITY ANALYSIS FOR HIGH SPEED DIGITAL CIRCUIT

ENDA TING MEI SHANG

ELECTRICAL & ELECTRONICS ENGINEERING
UNIVERSITI TEKNOLOGI PETRONAS

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Signal Integrity Analysis for High Speed Digital Circuit

by

Erica Ting Mei Shang

Dissertation submitted in partial fulfilment of
the requirements for the
Bachelor of Engineering (Hons)
(Electrical & Electronics Engineering)

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Universiti Teknologi PETRONAS
Bandar Seri Iskandar
31750 Tronoh
Perak Darul Ridzuan

CERTIFICATION OF APPROVAL

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Approved by,

(Mr. Patrick Sebastian)
Project Supervisor

UNIVERSITI TEKNOLOGI PETRONAS

TRONOH, PERAK

June 2009

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

(ERICA TING MEI SHANG)

ABSRACT

This dissertation report marks the commencement of the Final Year Project (FYP) titled Signal Integrity Analysis for High Speed Digital Circuit. This project is a study on various signal integrity (SI) issues that could possibly come into play on Printed Circuit Boards (PCBs). This project is conducted to analyze and grasp a better understanding on the nature of the problem, how the problem is manifested in circuits and what design solutions can be employed to minimize its effects. Such a study is not something new but is definitely getting more crucial as the vast improvement in chip fabrication technology leads to logic families operating at a much higher speed, resulting to a faster rise time which will worsen the noise phenomena, i.e. reflection, crosstalk, and power system stability during component switching. Several causes to signal integrity issues on the printed circuit boards are analyzed and both proper and improper circuit design techniques are implemented on the Advanced Design System (ADS) software for data collection and analysis. Deliverables at the end this project would be the simulation results to support the study, whereby several simulations are conducted to demonstrate and verify the theoretical study of signal integrity issues. Besides that, the designs will then be fabricated on a two-layer microstrip board and tested on the Digital Communication Analyzer (DCA) to obtain more practical results. A project Gantt chart is attached in the appendix to illustrate the work flow and anticipated progress.

ACKNOWLEDGEMENT

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I would also like to thank Regina, who has greatly helped me in this project when needed. And finally I would like to thank my friends and family for the support they have given me.

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LIST OF ABBREVIATIONS

IC	Integrated Circuit
PCB	Printed Circuit Board
EMI	Electromagnetic Interference
SSN	Simultaneous Switching Noise
I/O	Input/Output
ADS	Advanced Design System
DCA	Digital Communication Analyzer
SNR	Signal-to-Noise Ratio

CHAPTER 1
INTRODUCTION

1.1 Background of Study

Technology trends toward higher speed and density devices pushed the package performance to its limits. Advances in high performance microprocessors and broadband Internet access require high performance packaging structures for reliable high-speed data transmission. This necessitates the fabrication of interconnects and packages to support fast varying and broadband signals without degrading the signal integrity to unacceptable levels. In our new high-speed world, where the packaging and interconnect are no longer electrically transparent to the signals, a new methodology for designing a product right the first time is needed.

While the chip design and fabrication technology have evolved, the fabrication of interconnects package design has lagged, limiting the system performance [1]. Namely, the number of devices in a single IC scales with the square of the chip size over device size ratio, while standard interconnection, being placed on the die boundary, scales linearly towards the same parameter. With this, we face an interconnection bottleneck, thus, in the realm of high-speed digital design, signal integrity is one of the most important factors to be considered when designing and integrating packages together [2].

The term signal integrity addresses two concerns in the electrical design aspects – timing and quality of signal [1]. The context of quality here refers to the level of signal distortion. Signal distortion occurs when the waveform of interest changes its shape [3]. Thus, the goal of signal integrity analysis is to ensure reliable high-speed data transmission [6]. The way to solve signal integrity problems is to first understand their origin and then apply all the tools in our toolbox to find and verify the optimum solution.

With an efficient design and simulation process, many of the trade-offs between the expected performance and the ultimate cost can be evaluated early in the design cycle, where the time, risk, and cost savings will have the biggest impact.

Signal integrity is a major concern for engineers doing high-data-rate designs such as Infiniband, PCI Express, RapidIO, and 10 Gigabit Ethernet. Increasingly fast circuits with high clock speeds are in demand, and meeting this requirement is a constant challenge for every digital designer. High-frequency analogue effects such as reflection, cross talk, ground bounce, and propagation delays through interconnects adversely affect signal quality and timing performance. A table of speed of currently used operating logic families is attached in **APPENDIX A**.

1.2 Problem Statement

In the realm of high-speed digital design, signal integrity has become a critical issue, and is posing increasing challenges to design engineers. With modern digital electronic systems pushing beyond the 1-GHz barrier, packaging and board designers must now balance signal integrity and electrical performance with these other concerns. However, due to improper designs of high speed PCB, various signal integrity issues arise, which results to distortion in transmitted signals.

1.3 Objectives

At the end of this project, it is expected to achieve the following:

- To understand the nature of signal integrity problems.
- To verify theoretical study by running simulations.
- To conduct experiments on real 2-layer PCBs to support theoretical study and simulation results.
- To propose proper design solutions to minimize the effects of signal integrity.

1.4 Scope of Study

In general, the first part of this project encompasses the following scopes of study:

- The package of interest – Printed Circuit Boards (PCBs).
- Transmission line structure of interest – Microstrip line structure.
- Types of signal integrity issues – Reflection and crosstalk.

CHAPTER 2
LITERATURE REVIEW

2.1 Transmission Lines

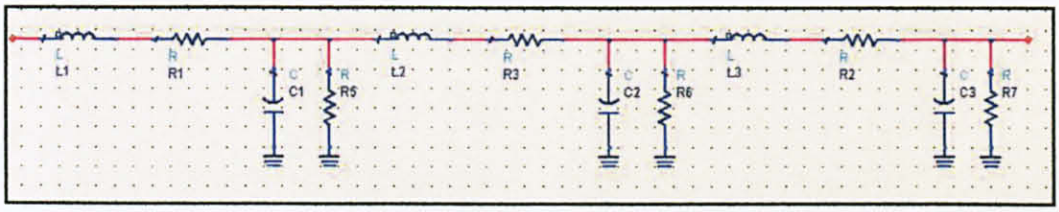


Figure 1: Multiple-cell models [2]

The multiple-cell models are attached in Figure 1. Each cell models a piece of PCB track; as the length of this piece diminishes and the number of cells increases, the model approximation improves. For an infinite number of very small cells, the sequence turns into a distributed parameter model or transmission line [6]. The transmission line is a distributed parameter model for the interconnection. The parameters of the transmission line are the R, L, C, G values for unit length.

A transmission line is lossless when the series resistance and parallel conductance are zero ohms (Ω) and susceptance (S), respectively. No power is dissipated in a lossless transmission line which brings this to the fact that such lines are ideal and make very good approximation for coaxial cable and copper wires, and of course, PCB tracks. However, in practice, no transmission lines are ideal [6].

Figure 2: Types of transmission line structures used in PCBs [2]

A transmission line uses some physical configuration of metal and/or dielectrics to direct a signal along the desired path. There are several types of transmission lines such as stripline, microstrip line, wire pair, radial transmission line, shown in Figure 2. However, the two most commonly used transmission lines are stripline and microstrip line whereby the former, which is attached in **APPENDIX B**, is a transmission line with the traces in the inner layer with which the presence of both top and bottom shields provide good isolation from other signals on the PCB [16] while the latter, the microstrip line structure, also attached in **APPENDIX B**, consists of a conducting strip separated from a ground plane by a dielectric layer known as the substrate [16].

The stripline environment will not be considered because the transmission line of structure in this project is the microstrip line structure.

This microstrip line family structure can be further broken down into several different configurations whereby the most useful configurations for designers are embedded microstrip line, covered microstripline, and microstrip line, all which are attached in **APPENDIX C**. Embedded microstrip line is the situation encountered when the microstrip line is covered with solder mask or a thin layer of epoxy [16] while a covered microstrip line is a transitional structure somewhere between microstrip line and stripline [16]. When an electrically close shield covers, the circuit designers will want to analyze it as a covered microstrip line.

The simplest configuration, the microstrip line which is the main focus in this project, simplifies the stripline by removing the upper ground planes. It is probably the most popular planar transmission line because of its ease of fabrication and the ready availability of the signals for probing and circuit connections [16]. Its disadvantage over stripline is that some of the energy transmitted may be coupled into space or adjacent traces. Despite its disadvantages, the microstrip line appears to be the most commonly used transmission line on PCBs and this feeds to the whole purpose and objective of this project – to study the root causes of signal integrity problems and to address these problems on a high speed PCB.

2.2 Signal Integrity (SI)

Signal integrity is the ability of a signal to generate correct responses in a circuit. A signal with good signal integrity has digital levels at required voltage levels at required times. signal integrity has 2 components that are interlinked – Voltage accuracy of the waveform and timing of arrival of switching edges at the input, whereby the waveform voltage accuracy is affected by impedance matches, ground bounce and coupling and so on while the timing of arrival of switching edges is affected by propagation delay variations in ICs, travel time on wires, and variation in edge rates of ICs [3].

2.3 Typical Signal Integrity Problems

Signal integrity becomes a problem when the rise time decreases to the point where parasitic inductance and capacitances on the board begin to result in noise signals which is dependent on the circuit specifics [5]. Some symptoms that might accompany signal integrity problems include:

- Design fails compliance testing.
- Design worked but fails later on after changing IC supplier or board fabricator.
- Design is sensitive to power supply and temperature variations.
- Design works in the lab but is intermittent in the field.

Circuit board materials also play a role in signal integrity issues. Factors like board thickness are obvious but the importance of other parameters such as relative dielectric coefficient, which will rise if fabrication parameters are not maintained, is often overlooked [4]. However, the common signal integrity problems on PCBs fall into 2 areas, which are related to rise time or frequency harmonics – Crosstalk and reflection noise.

There are two more problems that contribute to signal waveform distortions – Power/ground system stability and Electromagnetic Interference (EMI) but both these problems will not be studied in this project.

2.4 Signal Integrity Issues in Designs

The vast improvement in chip fabrication technology leads to logic families operating at much higher speed. Faster rise time worsens the noise phenomena – Crosstalk and reflection noise.

2.4.1 Crosstalk Noise

a. Overview

Leakage of a signal from one conductor to another is called crosstalk, and it can be induced through two coupling mechanisms: capacitive and inductive. Crosstalk, which is caused by electromagnetic (EM) coupling between transmission lines in parallel, is the interaction between signals on two different electrical traces, causing noise to pick up on adjacent quiet traces that may lead to false logic switching [1]. It will also impact the timing on the active lines if multiple lines are switching simultaneously.

The trace creating crosstalk is called an aggressor, and the one receiving it is called a victim. Often, a net is both an aggressor and a victim. The amount of crosstalk is related to the signal rise time, spacing between the lines, and how long these lines run parallel to each other [5].

b. Capacitive Crosstalk

All conductors have a certain degree of capacitance between them. And when sufficiently close, the capacitance will be able to couple energy from one line to another. The capacitance allows displacement current to cross the gap and into the victim line.

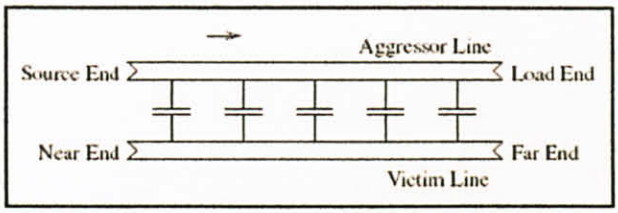


Figure 3: Circuit modelling of capacitive coupling [17]

Once the victim line develops some crosstalk signals, it can create crosstalk back onto the aggressor line, upsetting the signal on the aggressor line. The coupling is said to be strong when this secondary crosstalk (on the aggressor line) is strong.

The aggressor and forward waveforms on the victim trace travel towards the load and the far end, respectively. The aggressor edge adds to the victim pulse, which will grow in magnitude at each increment on the lines. There is an overlap and the pulse travels unchanged to the near end because the aggressor and backward waveforms on the victim trace travel in opposite directions. However, since these pulses are generated continuously, when the last pulse generated at the far end propagates back to the near end, the backward crosstalk grows quickly and at least double the magnitude can be seen at the near end [17].

In summary, capacitive crosstalk results in a weaker signal at the far end and a stronger signal at the near end [6]. The near-end noise grows in width while the far end signal grows in amplitude with longer lines. The crosstalk noise is positive for low-to-high transitions, negative for high-to-low for near end crosstalk and vice versa.

c. Inductive Crosstalk

Crosstalk voltage is generated on the victim line due to the changes in the current on the aggressor line, caused by the closed loops formed by two signal lines are coupled by mutual inductance. In contrast to the capacitive case, where current is injected into the victim line, the net change in current is zero; the aggressor line can only drive current on the victim line [17]. Thus, the forward and backward crosstalk has opposite polarities.

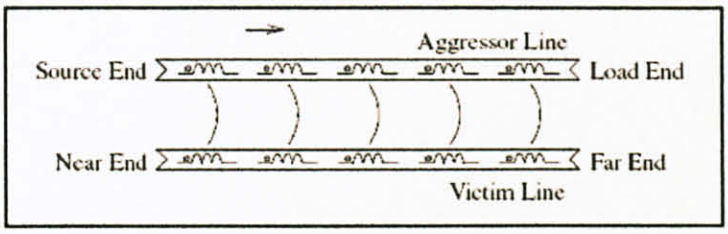


Figure 4: Circuit modelling of inductive coupling [17]

The forward noise, together with the aggressor wave, picks up amplitude continuously. The backward noise only picks up noise for half the edge rate since it and the aggressor travel in opposite directions. A positive backward pulse is produced on the aggressor line, when given a low-to-high transition and a negative forward pulse is produced on the victim line, while a high-to-low transition reverses the signs.

In summary, inductive crosstalk is very similar to the capacitive crosstalk: a weak signal at the far end and a strong signal at the near end [17], except that forward inductive and capacitive crosstalk have opposite signs.

d. Forward and Backward Crosstalk

Capacitively coupled crosstalk signal flows in the same direction as the driven current but inductively coupled crosstalk flows in the opposite direction. Capacitively and inductively coupled crosstalk tend to reinforce themselves in the backward direction, creating components flowing in the reverse direction and cancel each other in the forward direction [5]. The aggressor signal on the active line puts on four noise signals:

- Crosstalk caused by capacitive coupling
  - (1) which propagates towards the termination: Forward Capacitive (FC).
  - (2) which propagates towards the driver: Backward Capacitive (BC).
- Crosstalk caused by inductive coupling
  - (3) which propagates towards the termination: Forward Inductive (FL).
  - (4) which propagates towards the driver: Backward Inductive (BL).

The total crosstalk moving towards the termination end in the same direction of the aggressor signal is the forward crosstalk, which is the sum of terms 1 and 3 above. And since they have the same polarity, the forward crosstalk is always positive for the aggresor signal. The total crosstalk moving towards the driver end, in the opposite direction of the aggressor signal is the backward crosstalk, which is the sum of terms 2 and 4 above and since they have opposite polarity, the actual polarity of backward crosstalk depends on the prevalence of capacitive (2) or inductive (4) term.

The typical crosstalk behaviour is that coupling to neighbours is both inductive and capacitive, with capacitive crosstalk often dominating, while coupling to farther lines is mostly inductive. The signal traces may meet most of the criteria for good crosstalk, especially in terms of separation between adjacent traces. However, since return signal wants to travel directly underneath the traces and during this path, the returns are very close together so even if the traces do not crosstalk with each other, the returns might.

2.4.2 Reflection Noise

a. Overview

The reflection coefficient describes the fraction of the voltage that reflects back to the source. In addition, there is a transmission coefficient that describes the fraction of the incident voltage that is transmitted through the interface into the second region. This property of signals to reflect whenever the instantaneous impedance changes are the source of all signal-quality problems related to signal propagation on one net.

Reflections can be controlled when traces are constructed to represent transmission lines. However if no proper control is done, reflections will still occur and the cause to this issue might be impedance discontinuity and improper termination techniques [2]. Even if a circuit board is designed with controlled-impedance interconnects, there is still the opportunity for a signal to see an impedance discontinuity from the following features – The ends of the line, vias between signal layers, corners, stubs, branches in traces, gaps in the return path, crossovers.

For there to be impedance control and therefore control over reflections, the impedance of the trace must be constant over its entire length. On PCBs, the return signal would want to return directly underneath the trace. This is shown in Figure 5:

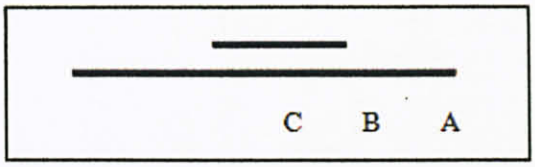


Figure 5: Signal trace (top) and ground plane (bottom)

Assume current is flowing down the trace and the return current is flowing back along the plane at point A. The return current will boost the primary current. However, for the case where if the current flows back at point B, the boost will be stronger since the distance between the current and its return path will be shorter. The point of lowest impedance will be where the boost is the strongest, which is at point C since the return current is directly under the trace. In general, the return signal will be on the closest plane to the signal trace, which is referred to as the reference plane. This is important in the context of reflection because it has implications over control of reflections [1].

In high-speed systems, reflection noise increases time delay and produces overshoot, undershoot and ringing [1]. The root cause of reflection noise is impedance discontinuity along the transmission path. Whenever a signal sees an impedance change, there will be a reflection. Reflections can have a serious impact on signal quality. Predicting the impact on the signals from the discontinuities and engineering acceptable design alternatives is an important part of signal integrity engineering.

b. Characteristic Impedance

When a signal flows along a transmission line matched with impedance values other than its characteristic impedance, impedance values along the line are inconsistent and reflections will occur [1]. The characteristic impedance of a transmission line is defined by its geometry and the dielectric coefficient of the material surrounding the line. Any change

in the geometry or in the dielectric coefficient will cause a change in the characteristic impedance, which will cause reflection.

The reflection magnitude is determined by reflection coefficient, ρ, with RL denoting the terminating, or load resistor.

$$\rho = \frac{RL - Zo}{RL + Zo}$$

The value of the reflection coefficient ranges between -1 and 1 whereby ρ = -1 for a shorted (improper termination) trace and ρ = 1 for an open (improper termination) trace. A reflection coefficient value of zero means the trace is perfectly terminated.

c. Discontinuity

There is also an impedance aspect to discontinuities that is important. Any forms of discontinuities are unterminated sections radiating away from a controlled impedance trace. When a trace is routed over planes with perforations at different locations, crossing a gap, having branches (stubs), or passing the proximity of another trace, impedance discontinuity will occur and reflection can be observed [1].

Stubs are a very common form of discontinuity use on PCBs, which are short trace segments that extend, unterminated, from a controlled impedance main trace.

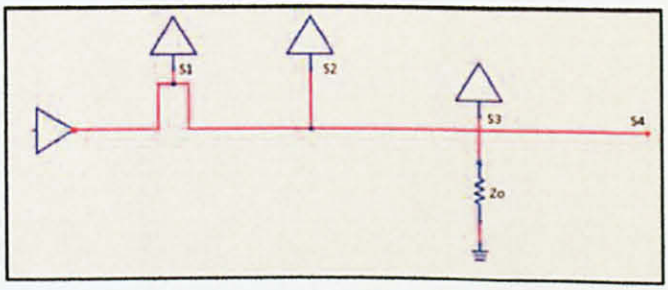


Figure 6: Various stubs designs [1]

The stubs shown, S1 and S3 are the commonly used stubs. The stub design which should be avoided in high speed designs is stub S2. This stub resembles an antenna that extends out of a cell phone. One reason why such long stubs should be avoided – resulting signals can reflect from the far and unterminated end of the stub and cause significant impedance discontinuity and damaging reflections. As the stub length increases, the ringing period increases and the ringing amplitude takes longer to settle. Stub S4, which might have been created when a trace was rerouted and a short segment from the original route was not removed is particularly harmful.

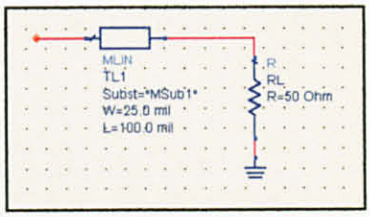
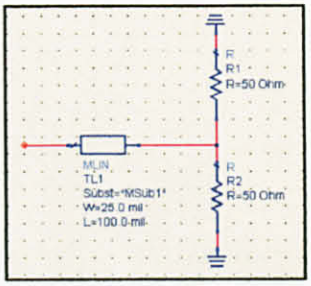
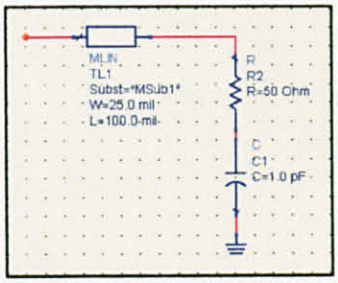
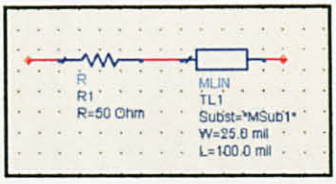
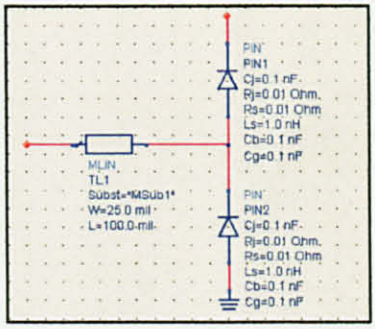
In general, stubs create two principal opportunities for loss of signal quality. First, the branch in the line creates an impedance discontinuity by placing the two lines in parallel. Second, reflections from the unmatched terminations will return to the branching point and reflect again, causing multiple reflections. It is difficult to conclude that this particular stub will or will not create a problem since not all stubs create signal integrity problems but they generally will, so it is best to minimize them.

d. Termination

When a signal reaches the receiving end of a transmission line, if the load is not matched with the characteristic impedance, reflection will occur [1]. The termination technique of interest in this project is the parallel termination – single resistor equal to the characteristic impedance of the line (RL = Zo) is attached to the end of the line. The energy flowing down the trace is absorbed by the terminating resistor and there is no reflection.

There are several commonly used termination techniques:

Table 1: Termination techniques

Termination Technique	Circuit Representation
Parallel	
Thevenin	
AC Termination	
Series	
Diode	

Parallel termination has several advantages – resistor value is easy to determine, easy to construct and performs well with distributed loads. However, it has one drawback – It provides DC path to ground, allows continuous DC current flow and causes significant power dissipation, if many terminating resistors exist in a circuit.

e. Bends

In complex and compact PCBs, microstrip line connections require non-straight paths. The most common way is to route the microstrip line 90° from its original course with mitered corners to retain reasonable return loss. An abrupt 90° un-mitred bend in a microstrip will cause a significant portion of the signal on the strip to be reflected back towards its source, with only part of the signal transmitted on around the bend.

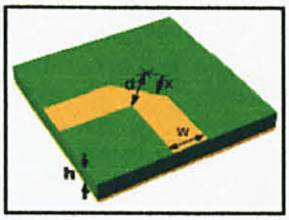


Figure 7: Microstrip 90° mitred bend [15]

The percentage mitre, M is the cut-away fraction of the diagonal between the inner and outer corners of an un-mitred bend. A smaller value of M indicates a smaller cut-away fraction of the diagonal between the inner and outer corners of an un-mitred bend, and vice versa. A good fit for optimum percentage mitre is given by:

$$M = 100\frac{x}{d}\% = (52 + 65e^{-\frac{2\pi W}{3h}})\ \% \text{ [4]}$$

whereby W is the width of the signal trace and h denotes the height of the substrate (Refer Figure 7). The formula above is subject to fraction of W over h to be at least 0.25 and the relative dielectric constant, ε_r to be at most 25, although it is independent of ε_r. Note that the value of the percentage mitre, M cannot exceed 0.9, or 90%.

CHAPTER 3
METHODOLOGY

3.1 Procedure Identification

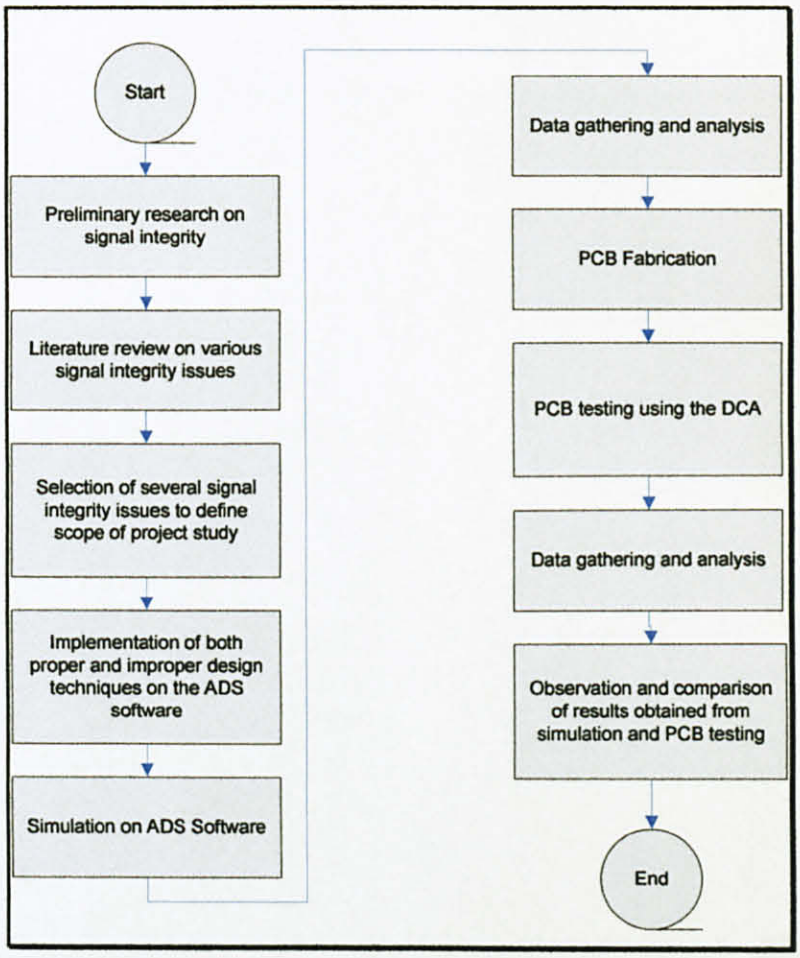


Figure 8: Progress flow chart

3.2 Tools

3.2.1 Software

a. Advanced Design System (ADS)

The Advanced Design System (ADS) software is an electronic design automation software system which offers complete design integrations to designers of various devices i.e. cellular and portable phones, pagers and wireless networks. In this project, the ADS is used to implement proper and improper design techniques on microstrip lines for simulation purposes, PCB fabrication as well as data collection and analysis.

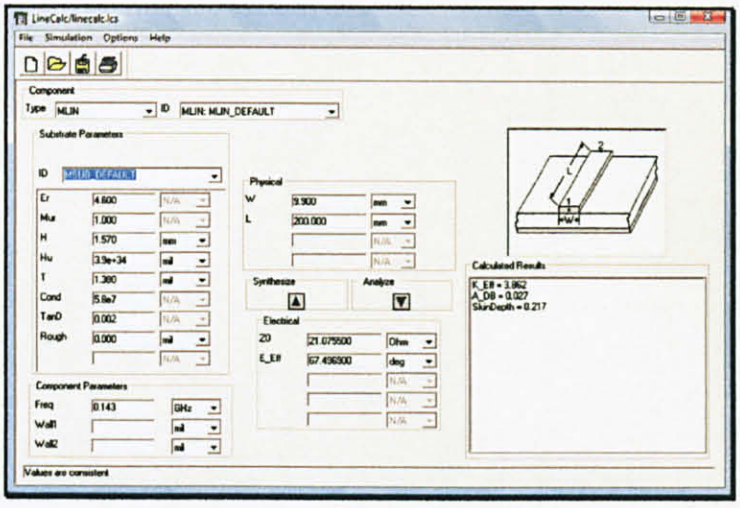


Figure 9: A printscreen of the LineCalc application window on the ADS

A feature in ADS, LineCalc is used to calculate the characteristic impedance of a line, which in this case is the microstrip line, given the necessary parameters such as relative dielectric constant ε_r, height of substrate H, width W and length L of microstrip line and so on.

3.2.2 *Hardware*

a. Digital Communication Analyzer (DCA)

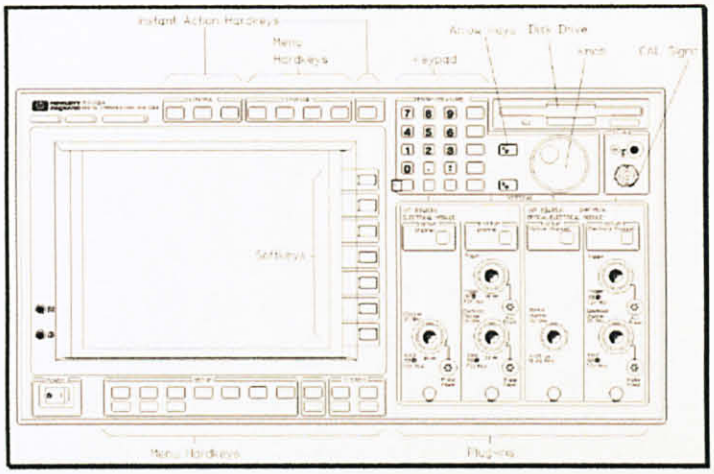


Figure 10: An image representation of the HP 83480A Digital Communications Analyzer

The DCA used in this project is the HP 83480A digital communications analyzer, an instrument for characterizing high-speed digital waveforms. In this project, the signal of interest to be observed from the DCA is the eye diagram, an oscilloscope display of a digital signal, repetitively sampled to get a representation of the signal behaviour.

b. Altera Stratix II GX Transceiver Signal Integrity Development Board

The Altera Stratix II GX Transceiver Signal Integrity Development Board is used in collaboration with the DCA. In order to be able to view and analyze the resulting output signals from the experimented PCBs on the DCA, an input signal is needed, which is generated by this development board. Figure 11 shows an image representation of the Stratix II GX Transceiver Signal Integrity Development Board while Figure 12 shows a printscreen of the control panel, which functions to control the generated signal.

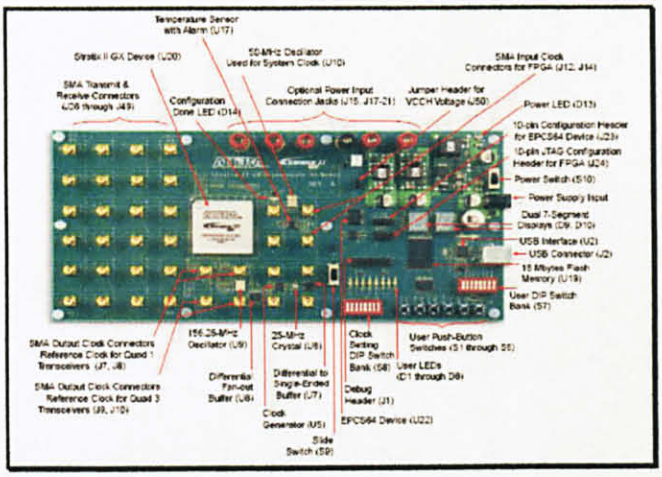


Figure 11: Stratix II GX Transceiver Signal Integrity Development Board [19]

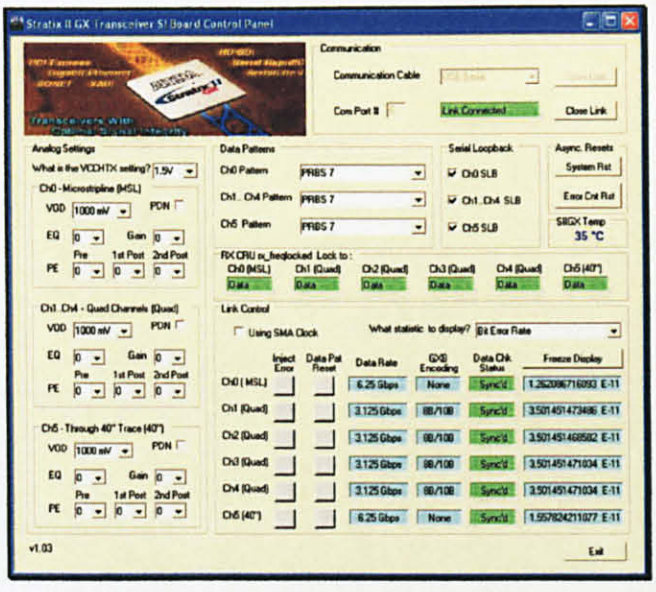


Figure 12: A printscreen of the control panel

c. PCB (FR4 substrate)

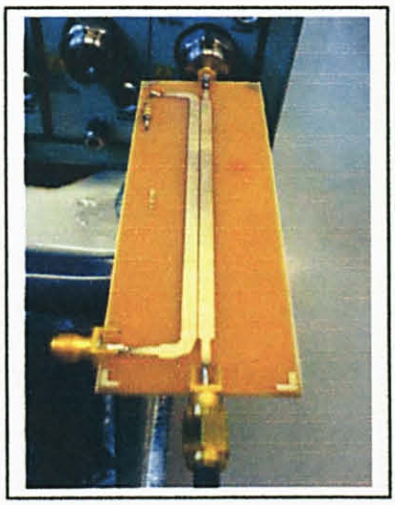


Figure 13: A fabricated microstrip line on a PCB

FR-4, or Flame Retardant 4, is a type of material used for making a PCB. FR-4, manufactured as an insulator, describes the board substrate. The type of PCB of interest in this project is a board with FR-4 as its insulator accompanied by copper layers on both sides of it. The following marks the approximate specifications of a PCB with FR-4 as its insulator:

Height of board, H = 60 mils
Relative dielectric constant, Er = 4.5
Relative permeability, Mur = 1
Conductor conductivity, Cond = 5.8 E +07 S/m
Cover height, Hu = 3.9 E +034 mils
Conductor thickness, T = 0 mils
Loss tangent, TanD = 0.015
Conductor surface roughness, Rough = 0 mils

CHAPTER 4
RESULTS AND DISCUSSION

Since the signal of interest to be observed from the DCA is the eye diagram, it is best to examine the characteristics of an eye diagram first before examining the resulting signal waveforms obtained.

The eye diagram is a performance indicator in digital systems. It gives a quick assessment on the quality of a signal. The signal of interest is continuously superimposed upon each other within a specified display range and the result becomes an "eye shape". The periodicity of the signal is shown in a time fashion by plotting the signal in a serial manner and wrapping it around when a zero crossing is detected.

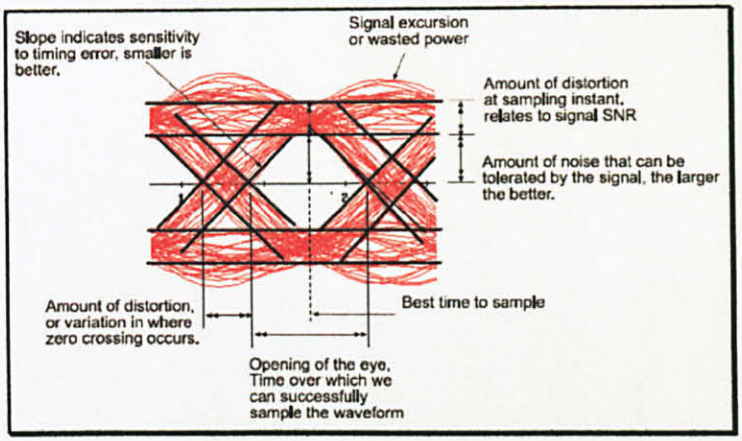


Figure 14: The representation of the eye diagram

The resulting eye diagram provides us with a great deal of information about the received signal performance, namely:

- Eye height – This measurement defines the margin over noise. A larger eye opening indicates a better signal quality with minimal noise.
- Eye width – This measurement defines the time interval over which the received signal can be sampled without error. As the signal noise is minimized, the eye width is larger.
- Zero crossing level – This measurement defines the amount of distortion or variation in the signal. A narrow width indicates that the amount of distortion/variation is minimal.
- Horizontal band – This measurement represents the signal variation at the sampling time, which is directly related to the SNR of the signal. A narrow band indicates a high SNR value.

4.1 Ideal Microstrip Line

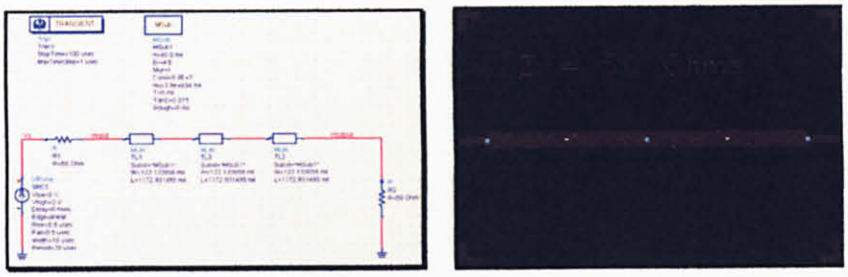


Figure 15: Circuit schematic and design layout of an ideal line

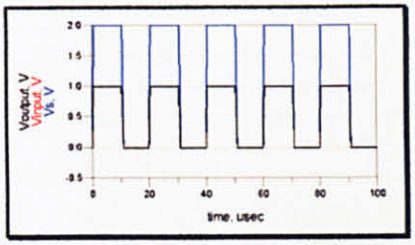


Figure 16: Time domain plot of voltage nodes of an ideal line

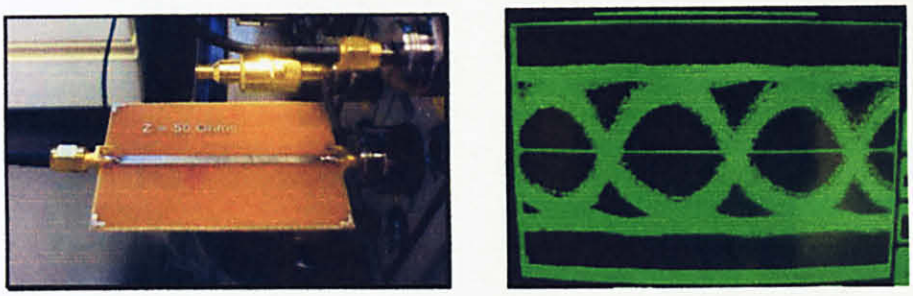


Figure 17: PCB testing on an ideal microstrip line and the resulting waveform

From Figure 17, it is observed the signal quality along the ideal line is considerably good. The eye height and width are large, showing a clear eye opening, the horizontal band is narrow, indicating that the SNR of the signal is high while the zero crossing level is narrow as well, indicating that the signal suffers from minimal signal variations/distortion.

There is a certain percentage of noise and distortion in the resulting signal though, which is most likely contributed from the connectors and cables used. As for the remaining testing work conducted on different designs of microstrip lines, it is assumed that there will be a slight noise and distortion contributed from the cables and connectors.

4.2 Crosstalk

4.2.1 Simulation Work

a. Design Issues

There are three factors that affect the magnitude of the crosstalk noise signal:

- The degree of coupling that exists between the aggressor and victim traces.
- The distance over which that coupling occurs.
- The effectiveness of any traces terminations that might exist.

Coupling

The degree of coupling is affected by the separation between traces, S and the length of coupled lines, L. Crosstalk effects can be reduced if the separation between traces, D is maximized accordingly and if the coupling length is reduced.

Distance

Crosstalk amplitude is low for short coupling regions because it is too short for crosstalk to build up. The magnitude of crosstalk builds as the length of the coupling region increases, up to a critical length where crosstalk amplitude will level out and stay constant.

Terminations

For a coupled pair of traces, for the victim trace to be terminated in its characteristic impedance, backward crosstalk pulse will be absorbed by the terminating resistor and will not reflect forward. This concept will be applied in crosstalk modelling to avoid reflection from occurring.

b. Simulation on ADS

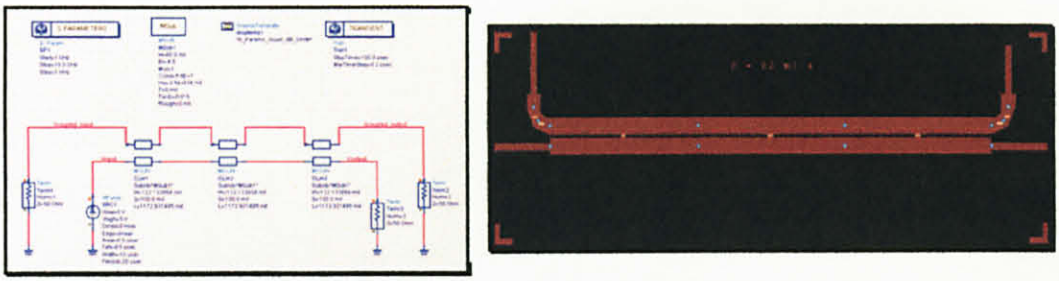


Figure 18: Circuit schematic and design layout to model crosstalk

To model only crosstalk effects, traces are properly terminated with their characteristic impedance, Zo = 50 Ω to avoid reflections effects.

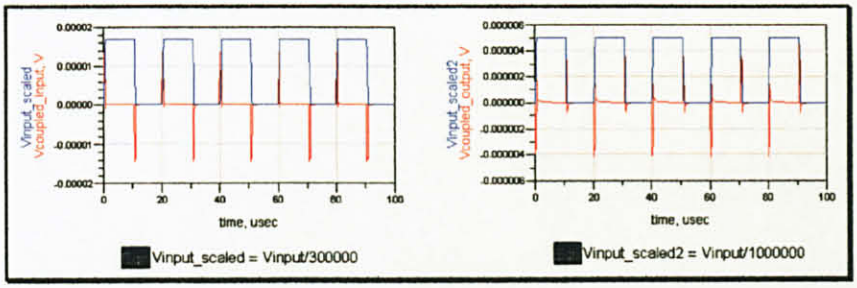


Figure 19: Time domain plot of voltage nodes – S = 100 mils and L = 3519 mils

Vcoupled_input = ±10 μV

Vcoupled_output = ±4 μV

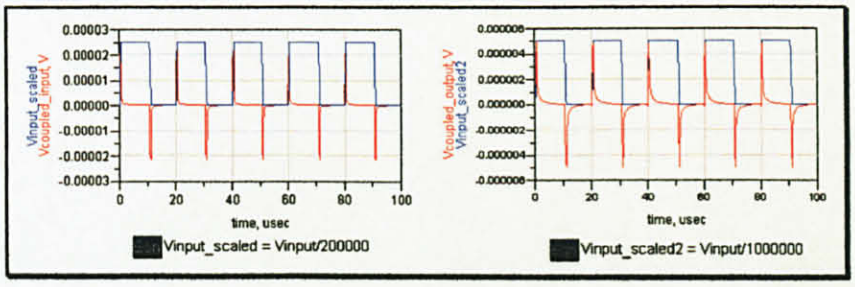


Figure 20: Time domain plot of voltage nodes – S = 20 mils and L = 3519 mils

Vcoupled_input = ±20 μV

Vcoupled_output = ±5 μV

When separation, S between the coupled microstrip lines is decreased (from 100 mils to 20 mils in separation), crosstalk amplitude builds up.

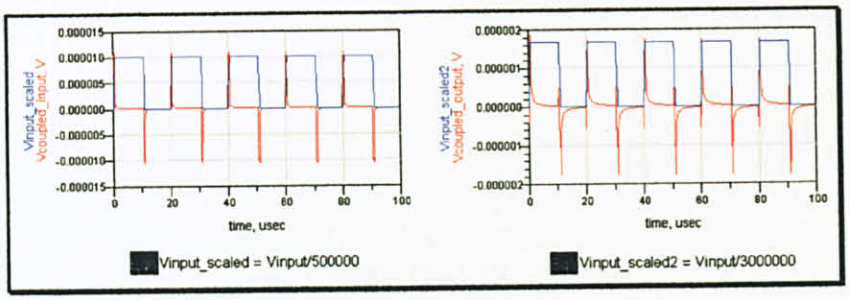


Figure 21: Time domain plot of voltage nodes – S = 20 mils and L = 1173 mils

$$V_{coupled\_input} = \pm 11\ \mu V$$

$$V_{coupled\_output} = \pm 2\ \mu V$$

When the length, L of the microstrip line is decreased (from 3519 mils to 1173 mils in length), crosstalk amplitude decreases as well. This supports the theory stated earlier – crosstalk amplitude builds up as the magnitude of the coupling region increases.

Discussion

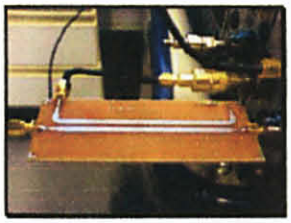
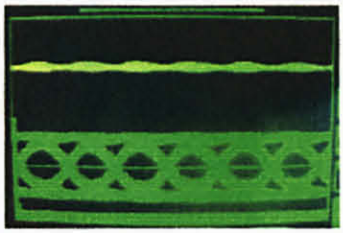
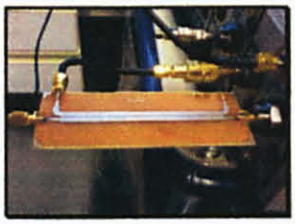
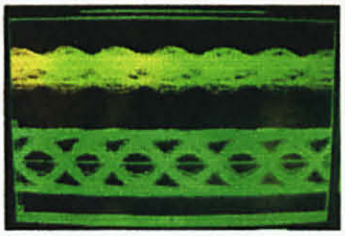
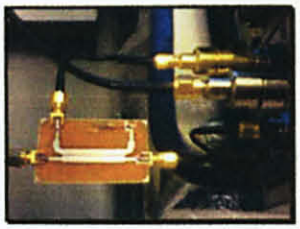
From the simulation results above, crosstalk effect appeared in the form of spikes. Although the crosstalk amplitudes are in microvolts (μV), the impact of these spikes on the signal is significant in real time PCBs. Also, the simulation results support the theory: There will be minimal far end crosstalk since the backward crosstalk is absorbed by the terminating resistor and is not reflected forward.

It can also be seen from the results above that, crosstalk noise is positive for low-to-high transitions and negative for high-to-low for near end crosstalk, and it is negative for high-to-low transitions, positive for low-to-high transitions for far end crosstalk.

In summary, crosstalk amplitude builds up when the magnitude of coupling region increases or when the traces are placed closer to each other.

4.2.2 PCB Testing on the DCA

Table 2: Crosstalk – Results from PCB testing

PCB design	Received Signal	Discussion
Coupled microstrip lines:  S = 100 mils L = 3519 mils	Upper waveform – Signal along the victim line  Lower waveform – Signal along the active line	- The victim line without any input source picks up minimal signal from adjacent active line. - The signal along the active line is slightly distorted due to crosstalk effect contributed by the minimal signal along the victim line.
Coupled microstrip lines:  S = 20 mils L = 3519 mils	Upper waveform – Signal along the victim line  Lower waveform – Signal along the active line	- The signal picked up by the victim line (due to crosstalk) is much higher compared to the previous board design. - With a larger signal along the victim line, the signal along the active line shows more distortion due to crosstalk effect contributed by the signal along the victim line.
Coupled microstrip lines:  S = 20 mils L = 1173 mils	Upper waveform – Signal along the victim line  Lower waveform – Signal along the active line	- With the magnitude of coupling region decreased from 3519 mils to 1173 mils, the degree of crosstalk has decreased. - The signal along the victim line has decreased while the signal along the active line suffers minimal distortion.

4.2.3 Reducing Crosstalk

It is impossible to eliminate crosstalk noise on a PCB altogether. Thus, in order to reduce crosstalk effect on the resulting signals, there are several general design features to follow, which include:

- Keeping coupled lengths short.
- Maximize separation between coupled lines accordingly.
  NOTE: There is no one particular formula which gives the best distance between coupled lines, nor there is any which gives the optimum length to reduce crosstalk effect. However, it is advisable to not design traces as close as 8 mils or less, or design coupled lines to be more than 4000 mils in length.
- Avoid sharing return pins in packages and connectors.

4.3 Reflection

4.3.1 Simulation Work

a. Design Issues

One important criterion to control reflections in a transmission line – To terminate the transmission lines in their characteristic impedance, Zo. The three major designs that affect reflections are trace bends, improper impedance matching and the existence of discontinuities along a signal trace.

Bends

Trace bends are very common in PCB designs. With such route contributing to reflection issues, the better design would be to route the microstrip line 90° from its original course with mitered corners to retain reasonable return loss.

Impedance Matching

Recall that the characteristic impedance of a transmission line, Zo is defined by the geometry of the trace (width W and length L) whereby any changes in any, especially the width, will cause a change in the Zo of the line [1]. A transmission, if not matched, or terminated with its characteristic impedance, may lead to reflection issues.

Discontinuity along a Signal Trace

Any form of discontinuities are unterminated sections radiating away from a controlled impedance trace where signals reflect from the far and unterminated end of the trace and this results in an impedance discontinuity and damaging reflections [1]. Stubs, a form of a discontinuity, will be used in reflection modelling on the ADS.

b. Simulation on ADS

Impedance mismatch – Microstrip line with different line widths

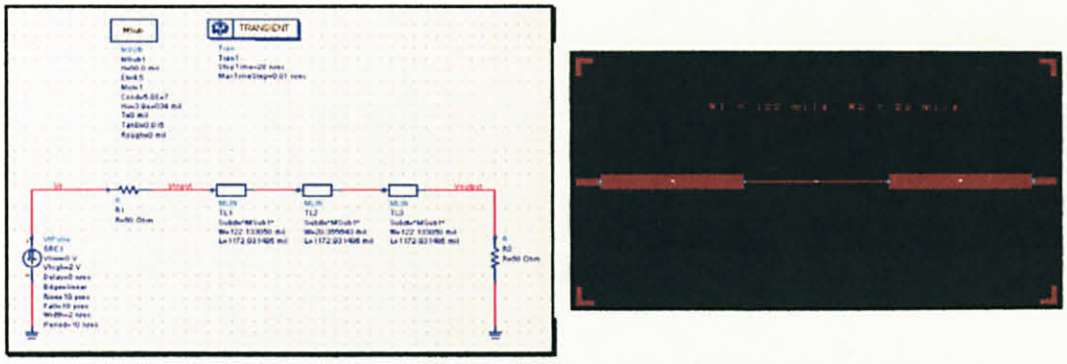


Figure 22: Circuit schematic and design layout used to model impedance mismatch

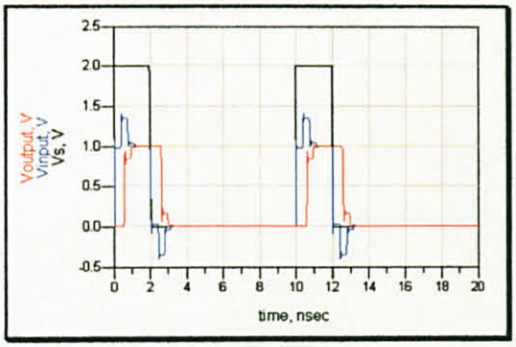


Figure 23: Time domain plot of voltage nodes – W_1 = 122 mils and W_2 = 20 mils

In the simulation conducted, W_2 is of a smaller width as compared to W_1, thus the signals, when travelling from source to load (W_1 to W_2 to W_1, as shown in Figure 22) will be reflected back to the source. This explains the signal amplitude variation seen at port Vinput and Voutput in Figure 23, whereby for a certain period the signal amplitude at Vinput is seen to be slightly higher than the signal amplitude at Voutput, which is due to the contribution of the reflected signals.

When a signal flows along a transmission line matched with impedance values other than its characteristic impedance, impedance values along the line are inconsistent and reflections will occur.

Improper impedance termination

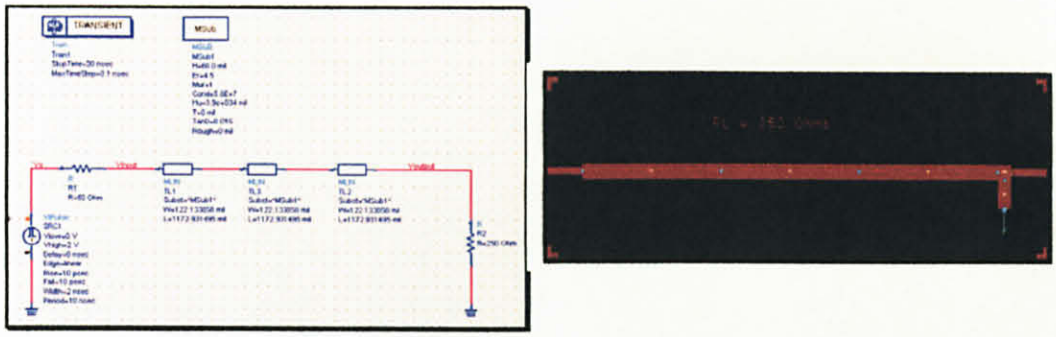


Figure 24: Circuit schematic and design layout to model reflection – Improper line impedance matching

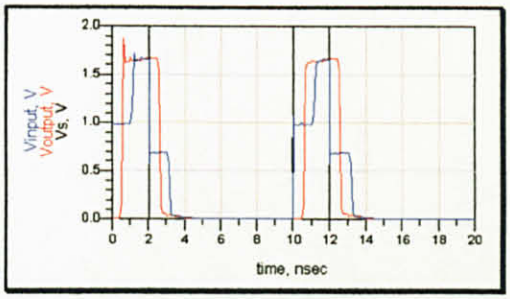


Figure 25: Time domain plot of voltage nodes with termination resistor, RL = 250 Ω

There are several termination techniques i.e. series, parallel and Thevenin termination. The termination technique used is parallel termination. The simulation conducted consists of a microstrip line with its characteristic impedance set to 50 Ω being terminated with a 250 Ω resistor. Signal variation is, again seen at Vinput and Voutput nodes (refer Figure 25). This is due to reflection whereby signals are reflected from the improper termination end of the line. As have noted, the root cause of reflection noise is the impedance discontinuity along the signal transmission path. In other words, whenever a signal sees an impedance change, there will be reflection. In this case, reflection is shown in simulation that when a signal reaches the receiving end of a transmission line, if the load is not matched with the characteristic impedance, Zo, signal reflection occurs [1].

Stubs

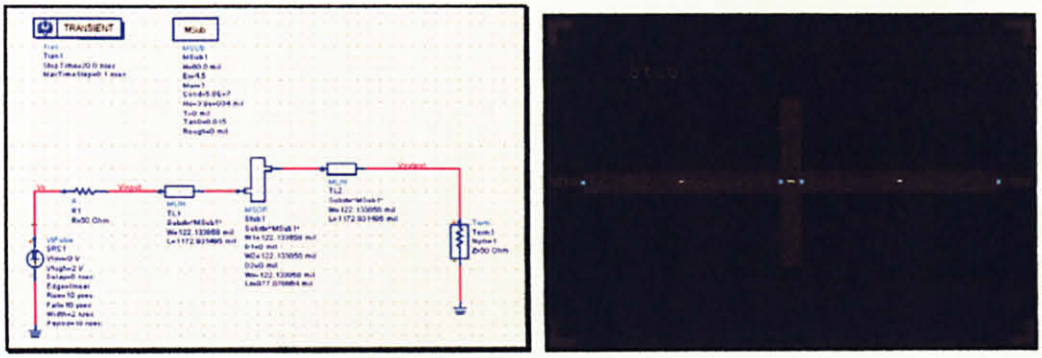


Figure 26: Circuit schematic and design layout to model reflection – Discontinuity (stub)

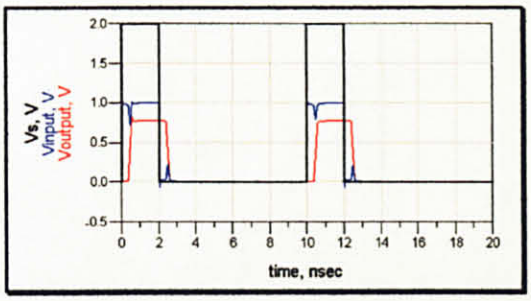


Figure 27: Time domain plot of voltage nodes with the existence of a stub along the microstrip line.

From the simulation conducted, the existence of stubs, which are one of the many causes that leads to impedance discontinuity along a signal trace, affects the quality of the signal flow. Stubs are best avoided in designing circuits on PCBs because the resulting signals reflect from the unterminated end of the stub and cause significant impedance discontinuity and damaging reflections.

Microstrip line 90° bends

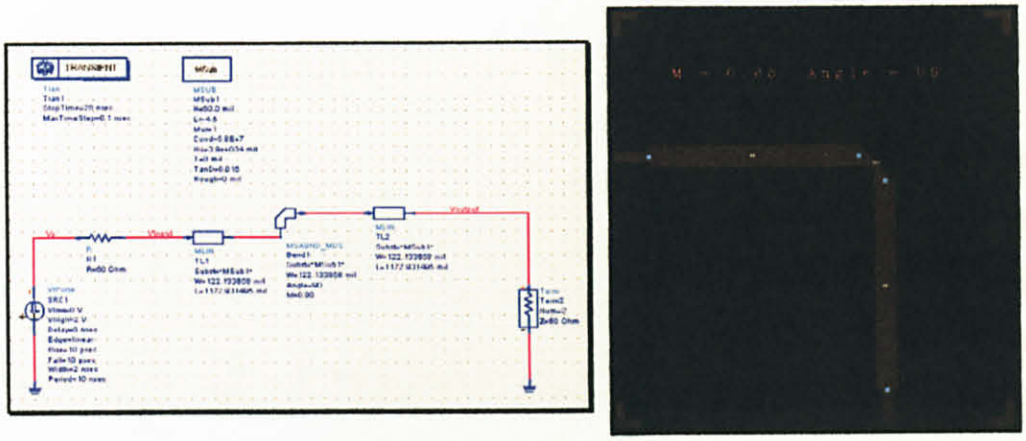


Figure 28: Circuit schematic and design layout to model reflection – 90° bend.

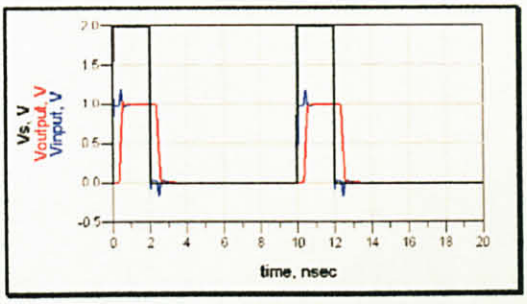


Figure 29: Time domain plot of voltage nodes with angle of bend = 90° and M = 0.85.

Figure 29 shows the time domain plot of voltage nodes with percentage mitre M = 0.85, whereby with 85% of the corner cut away, the resulting output signal experiences slight spikes/glitch, due to reflection of the signal along the line. To obtain a good fit for optimum percentage mitre, the following formula is utilized. In this simulation, h = 60 mils while W = 122 mils.

$$M = (52 + 65e^{-\frac{87W}{60h}})\% = (52 + 65e^{-\frac{87(122\,mil)}{60(1.27\,mil)}})\% = 56\% \text{ or } 0.56$$

From this, the percentage mitre is equivalent to 0.56, given the height of the substrate equivalent to 60 mils and width of microstrip line to be approximately 122 mils.

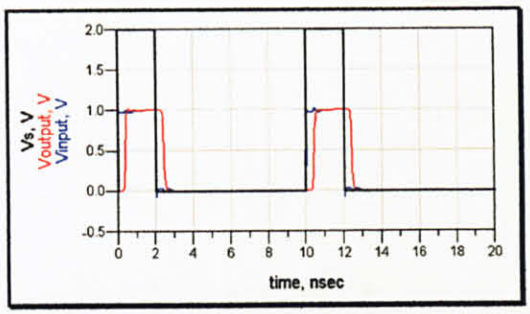


Figure 30: Time domain plot of voltage nodes with angle of bend = 90° and M = 0.56.

Figure 30 shows the time domain plot of voltage nodes with an optimum percentage mitre. From the observations made, it is apparent that the value of M influences the degree of reflection. For the case where the microstrip line is routed 45° from its original course, mitered corners are no longer required, as shown in the simulation conducted below.

Microstrip line 45° bends

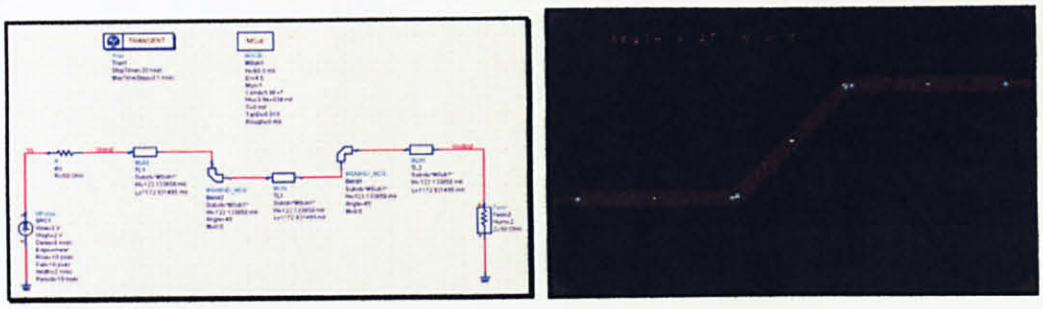


Figure 31: Circuit schematic and design layout to model reflection – 45° bend.

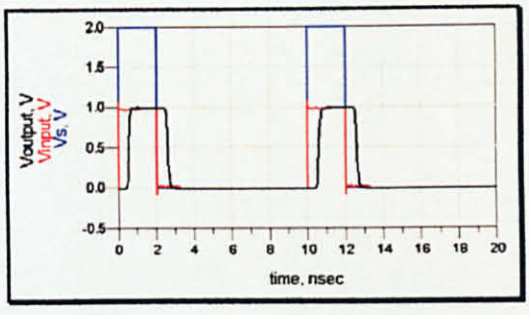
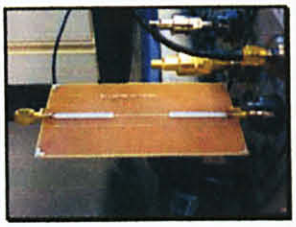
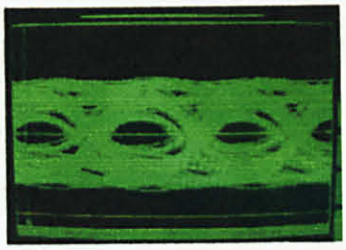
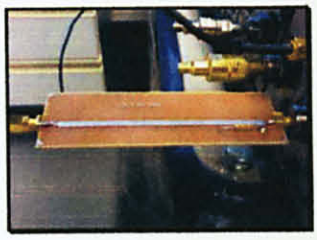
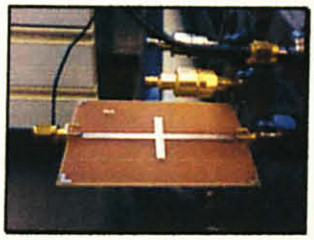
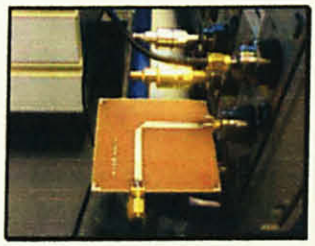


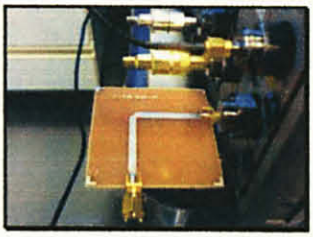
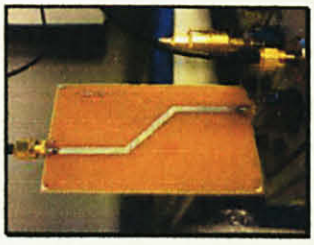
Figure 32: Time domain plot of voltage nodes with angle of bend = 45° and M = 0.

4.3.2 PCB Testing on the DCA

Table 3: Reflection – Results from PCB testing

PCB design	Received signal	Discussion
Impedance mismatch: Microstrip line with different widths  W_1 = 122 mils W_2 = 20 mils	**Horizontal band** – Thick, indicating that the SNR of the signal is low. **Eye height** – Low, indicating a noisy signal.  **Eye width** – Narrow. **Zero crossing level** – Thick, indicating high signal distortion/variation.	- The resulting eye diagram observed suffers greatly from noise and signal distortion. - A microstrip line with different line widths has different line impedance. A line with a change in its impedance will lead to reflection issue.
Improper impedance termination  Zo of line = 50Ω Z_L = 250Ω	**Horizontal band** – Thick, indicating that the SNR of the signal is low. **Eye height** – Low, indicating a noisy signal.  **Eye width** – Narrow. **Zero crossing level** – Thick, indicating high signal distortion/variation.	- The resulting eye diagram observed suffers greatly from noise and signal distortion. - A microstrip line, if not matched with its characteristic impedance, signal reflection will occur and affect the resulting output signal.

PCB design	Received signal	Discussion
Stub 	**Horizontal band** – Thick, indicating that the SNR of the signal is low. **Eye height** – Undefined, indicating the amount of noise is high.  **Eye width** – Undefined. **Zero crossing level** – Undefined, showing that the signal suffers greatly from signal variation/distortion.	- The signal along the line suffers from reflection, whereby the resulting eye diagram is observed to be noisy and distorted. - Stubs are best avoided for signals reflected from the unterminated end of the stub could cause reflection.
Microstrip line 90° bend  Percent mitre, M = 0.85	**Horizontal band** – Thick, indicating that the SNR of the signal is low. **Eye height** – Low, indicating a noisy signal.  **Eye width** – Smaller than the eye width of the ideal line. **Zero crossing level** – Thick, indicating high signal distortion/variation.	- The received signal suffers from reflection, whereby signal along the line is distorted and noisy. - A large portion of the transmitted signal is reflected back due to the sharp turn along the line.

PCB design	Received signal	Discussion
Microstrip line 90° bend  Percent mitre, M = 0.56	**Horizontal band** – Considerably thick, indicating that the SNR of the signal is lower. **Eye height** – Higher, as compared to the previous eye diagram, indicating a less noisy signal.  **Eye width** – Wider, as compared to the previous eye diagram. **Zero crossing level** – Narrower, as compared to the previous eye diagram.	- When a good fit for optimum percentage mitre is applied onto the design, the resulting signal shows some improvement. - The received signal is observed to be less noisy and distorted.
Microstrip line 45° bend  Percent mitre, M = 0	**Horizontal band** – Thinner as compared to the previous eye diagram. **Eye height** – High, indicating a less noisy signal.  **Eye width** – Approximately similar to the previous eye diagram. **Zero crossing level** – Thick, high distortion/variation.	- Another design to mitigate signal integrity issue would be to route the microstrip line 45° from its original course, with no mitred corners required. - The received signal is observed to be less noisy and distorted.

4.3.3 Reducing Reflection

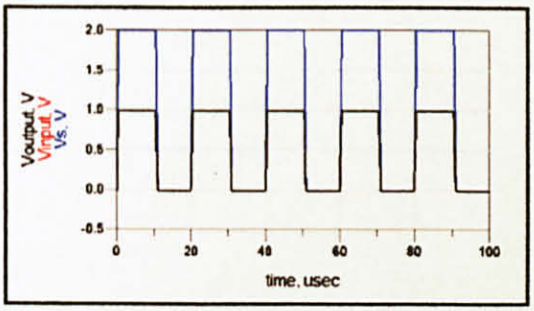
In practical applications, it is impossible to eliminate reflection noise on a PCB. It can only be reduced. Two important criterions to control reflections in a transmission line are to first, keep the line impedance constant until termination end and secondly, terminate the lines with their respective characteristic impedance, Zo. The general design features that will help reduce reflection include:

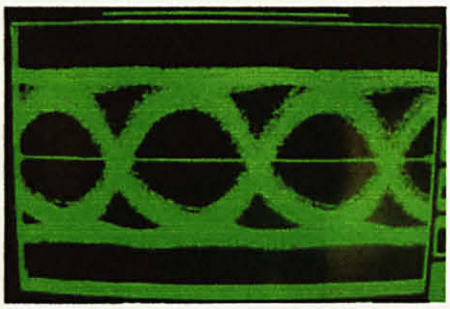
- Matching and terminating a transmission line with its characteristic impedance value, Zo.
- Applying a good fit for optimum percentage mitre in routing microstrip lines 90° from its original course.
- Keeping stubs length short is their existence is necessary.
- Making use of stickups that place traces as close as possible to their reference planes (for the signal return paths).

In summary,

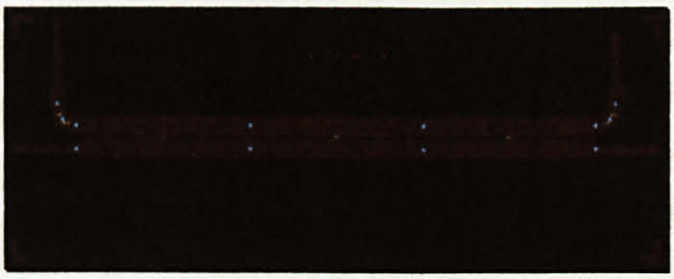
Table 3: Summary on results obtained

IDEAL MICROSTRIP LINE

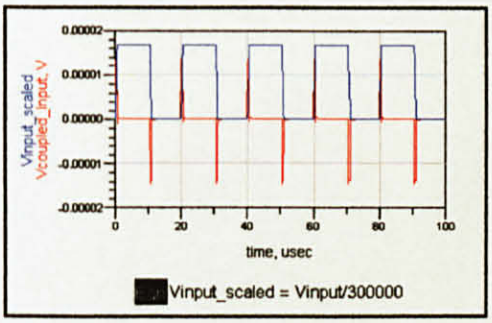


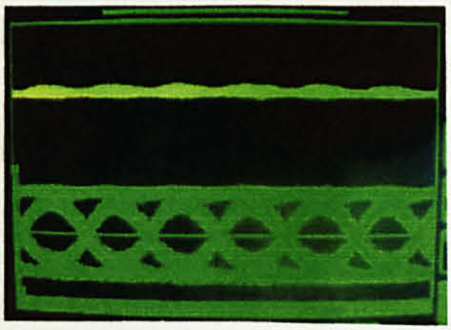


CROSSTALK

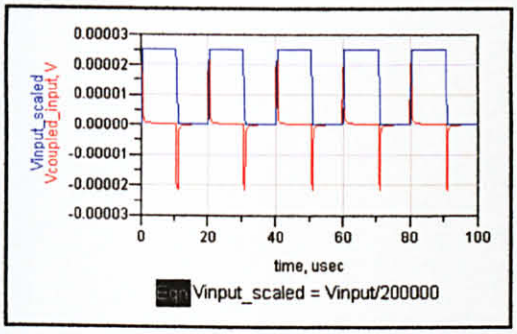


S = 100 mils, L=3519 mils

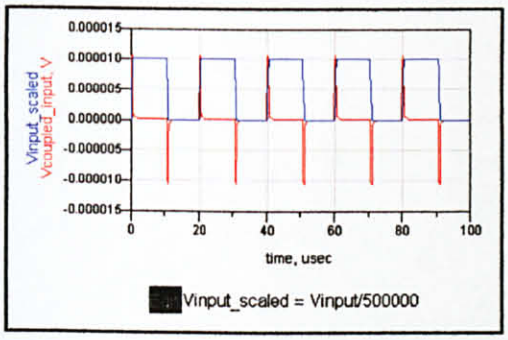


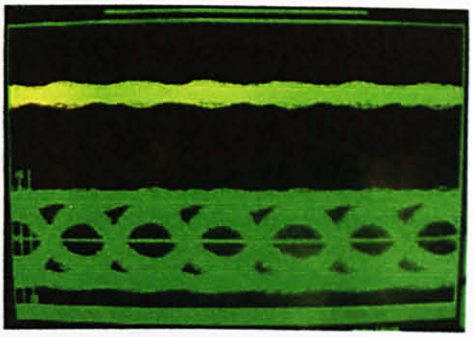


S = 20 mils, L = 3519 mils



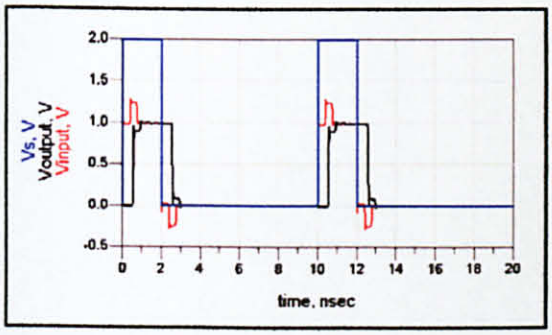
S = 40 mils, L = 1173 mils

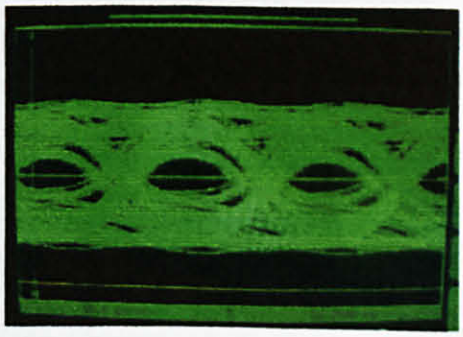




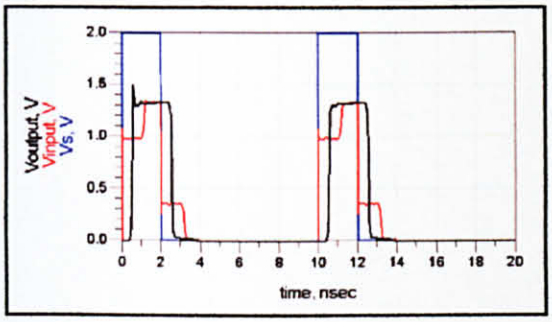
REFLECTION

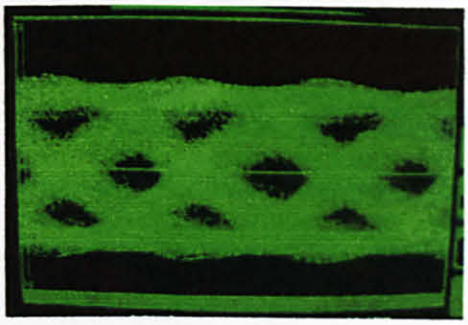
Impedance mismatch – Microstrip line with different line widths



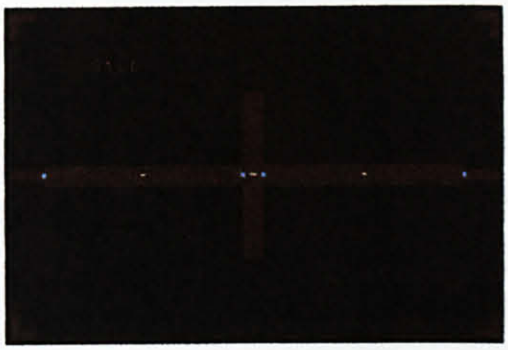


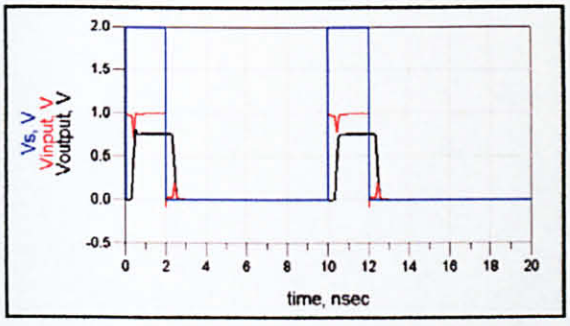
Improper impedance termination

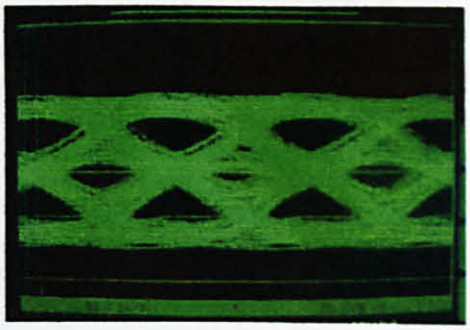




Stubs

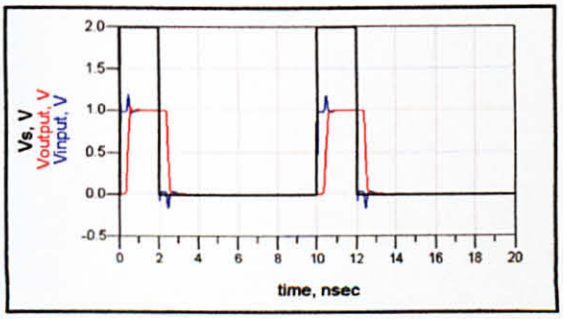




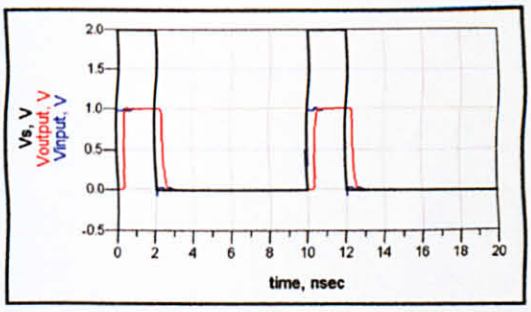


Microstrip line 90° bends

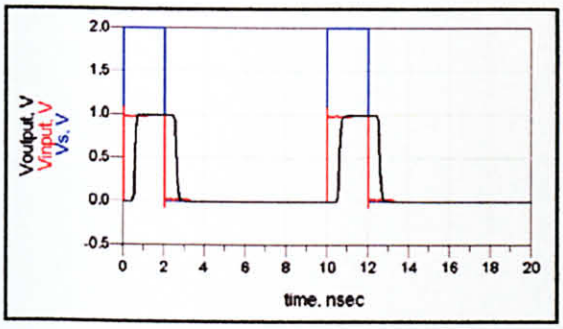
Percent mitred, M = 0.85



Percent mitred, M = 0.56



Microstrip line 45° bends



CHAPTER 5
CONCLUSION AND RECOMMENDATIONS

5.1 Conclusion

The purpose of this study is to add to the pool of knowledge relating to signal integrity on PCBs, and to contribute to the understanding of how different signal integrity issues can affect the signal performance in a PCB. The project is kicked off by conducting various study and literature research to grasp the nature of two signal integrity issues of interest – crosstalk and reflection, occurring on PCBs. A series of simulations is then conducted to verify theoretical claims. As for the second half of this project, work is focused on designing real 2-layer microstrip design layouts for fabrication and testing. Results obtained from both simulation and testing work are then observed, compared and discussed. Recommendations on proper design techniques to minimize the effect of both crosstalk and reflection effects are then made. The objectives of this project have been accomplished.

5.2 Recommendations

If meaningful results are achieved, this investigation could contribute to the progression of knowledge in the field of signal integrity, and on a larger scale this knowledge could be used to improve the effectiveness of designs on PCBs. It is hoped that this research can contribute to the critical issues being dealt with in the industry of microprocessors performances and broadband networks.

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APPENDICES

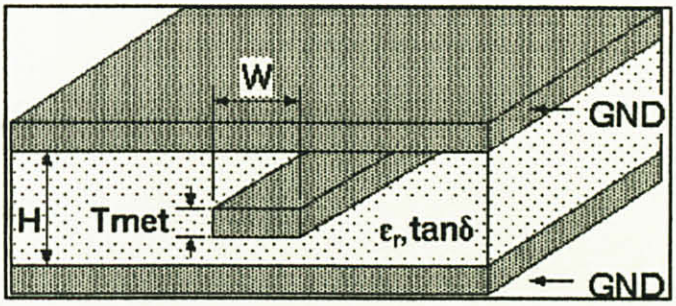
APPENDIX A

Speed of currently used operating logic families [1].

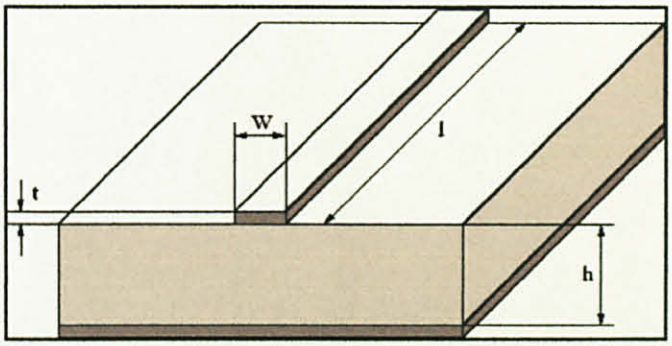
Logic type	Typical edge speed (nSEC)	Transition electrical length in FR-4 (inches)	Critical length in inches
STANDARD TTL	5.0	29.0	14.5
ASTTL	1.9	10.9	5.45
FTTL	1.2	6.9	3.45
10K ECL	2.5	14.4	7.2
BTL	1.0	5.8	3.9
CMOS/DS	1.5	9.0	4.5
LVDS	0.3	1.73	0.86
100K ECL	0.5	2.88	1.44
GA AS 106	0.3	1.73	0.86
GTL+(PENTPRO)	0.3	1.73	0.86

APPENDIX B

Stripline and microstrip line structures [8].



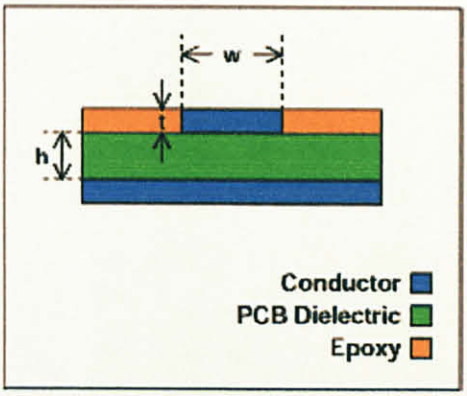
Stripline structure



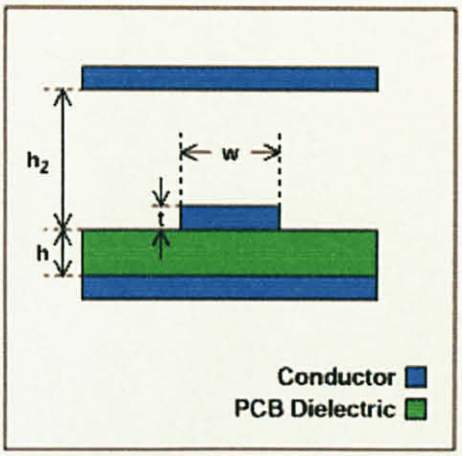
Microstrip line structure

APPENDIX C

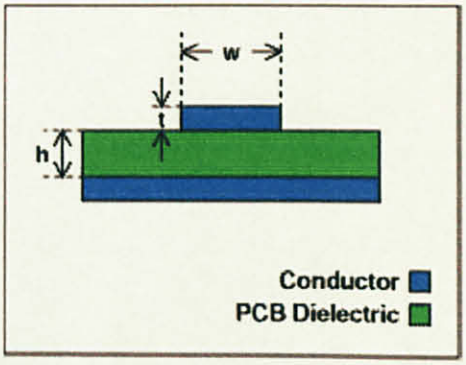
Microstrip line family structures [16].



Embedded microstrip line



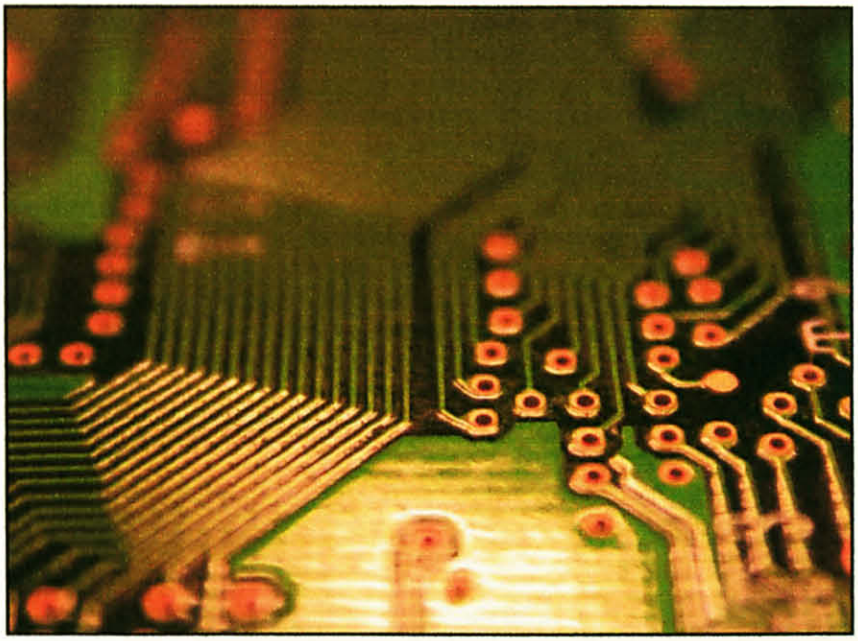
Covered microstrip line



Microstrip line

APPENDIX D

The existence of vias and angles of bend along the trace on a PCB [18].



APPENDICES

Appendix E: Gantt Chart

No.	Detail / Week	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	Review FYP 1 simulation work	■									Mid-Semester Break				
2	Self-study on NA, DCA, SI development board, etc		■	■											
3	Hands-on learning on those hardware		■	■											
4	Design and fabrication of ideal trace on a PCB			■	■	■									
5	PCB testing using NA and DCA					■									
6	Data gathering and analysis					■	■								
7	Design and fabrication of PCBs to model SI issues					■	■	■							
8	PCBs testing using NA and DCA						■	■							
9	Data gathering and analysis							■	■						
10	Comparison of practical results to simulation work							■	■	■					
11	Discussion								■	■					
12	Poster Exhibition											■			
13	Submission of Dissertation (soft bound)												■		
14	Oral Presentation													■	
15	Submission of Project Dissertation (Hard Bound)														■