DESIGN OF LOW NOISE AMPLIFIER (LNA) IN CMOS PROCESS TECHNOLOGY

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By

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CERTIFICATION OF APPROVAL

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Approved:

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Project Supervisor

UNIVERSITI TEKNOLOGI PETRONAS
TRONOH, PERAK

June 2009

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

Nur Fadzlina Binti Tasirin

ABSTRACT

This report describes the design and simulation of low noise amplifier (LNA) using AMI06 CMOS process technology. LNA is an amplifier used in communication systems to amplify a very weak input signal while reducing the amount of noise. The core method in designing LNA is to choose the most suitable topology and operating frequency that fit the design requirements. The design proceeds with the calculation of the LNA parameters which are source inductor drain inductor, gate inductor, width of the transistors, bias resistors and block capacitors. Global Positioning System (GPS) and Ultra Wideband (UWB) LNAs have been successfully designed and simulated using Cadence Spectra RFIC Design Software. Simulation results showed that the GPS LNA can amplify weak input signal at frequency range from 1.0 to 1.8 GHz. The LNA obtained gain from 21.348 dB to 25.513 dB. This LNA has achieved noise figure less than 2.518 dB and the power consumption is 16.5mW. For the UWB LNA the frequency range is from 3.1 to 5 GHz which covers the lower band of Ultra Wideband (UWB) technology. The UWB LNA achieved gain from 21.348 dB to 25.513 dB with noise figure less than 3.280 dB.

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CHAPTER 1

INTRODUCTION

1.1 Background of Study

There are many wireless devices that integrate multiple applications for example phone, navigator and web browser on a single chip. There are varieties of standards for each application such as global positioning system (GPS), global system for mobile communication (GSM) and Ultra Wideband (UWB) system. Because of many wireless communication standards the need for multi-standard transceiver arises. The radio frequency (RF) front-end of such receiver has to cover wide range of different operating frequencies. To achieve this objective, wideband performance of receiver front-end is desired. Low-noise amplifier (LNA) is the basic block of receiver system hence the architecture of LNA is important to fulfill this goal.

LNA is an amplifier used in communication systems to amplify very weak received signals captured by an antenna. The principle of LNA is to amplify the received signal to an acceptable level and at the same time minimizing the noise. By using LNA, the noise of all the subsequent stages of a receiver will be reduced by the gain of the LNA but the noise of the LNA itself is injected back directly into the received signal. Therefore, it is necessary for LNA to amplify the desired signal while ensuring the added noise as low as possible in order to recover the signal in the later stages of the system.

1.2 Problem Statement

There are many problems involving noises in electronic devices and communication systems. In communication systems, any signal other than the desired signal is called noise [1]. In wireless and high frequency communication system, a receiver will be facing noise problems caused by air propagation, electron movement and interfering signals, as a result the antenna will pick up weak receive signals. For that reason, LNA has been developed to enhance the weak receive signal.

The first block is the most critical block of the receiver system because total noise figure in the overall system is mainly dominated by the noise figure at the first amplifying stage which is LNA. The noises in transistors also contribute extra noise to LNA and there are three major noises in transistors are shot noise, thermal noise and flicker noise. Shot noise related to the junction diodes, thermal noise generated in the resistive channel and flicker noise generated by the surface traps between the silicon and the gate oxide [2].

A LNA design involves many considerations relating to gain, noise figure, frequency, linearity and impedance matching networks. Therefore, LNA design gives significant challenges and problems to obtain the suitable result that fulfill the design requirements.

1.3 Objective and Scope of Study

The objective of this project is to study various design aspects and procedures of LNA. Analysis of the LNA topologies that is suitable for a wideband LNA and the effect of different parameters such as operating frequency and width of transistors are presented. The results of this study are used to design and simulate wideband LNA in AMI06 CMOS process technology. The wideband LNA will be designed using Cadence

Spectra RFIC design software. In general, the LNA should have a low Noise Figure (NF), high gain and low power in agreement where it needed to be used. The design procedure of this wideband LNA can be used for many applications such as UWB and multi-standards transceivers. In this project the wideband LNA was designed to operate in lower band frequency of UWB systems which are 3.1GHz to 5.0GHz. This project is related to analogue electronics circuit design, noise, and wireless communication systems.

CHAPTER 2

LITERATURE REVIEW

2.1 CMOS Process Technology

One of the most popular MOSFET (Metal Oxide Semiconductor Field Effect Transistor) technologies available today is complementary metal oxide semiconductor (CMOS) technology; this technology can used both PMOS and NMOS transistors in a circuit. CMOS technology is widely used for interface integrated circuit design and has advantages over other technologies in term of potential cost, high noise immunity and low static power consumption [3]. As this advantage has grown and become more important, CMOS process has been chosen in majority of modern integrated circuit manufacturers. CMOS process technologies are differentiated by the minimum channel length of the transistor such as 0.35μm, 0.18μm and 0.13μm. This project used AMI06 CMOS process technology with the minimum length of 0.6μm for the transistor. The recent amplifier design using AMI06 CMOS technology is 0.5-5.5 GHz wideband amplifier [4].

2.2 Ultra Wideband (UWB)

UWB is wireless technology that capable of transmitting data over a wide radio range with high data rates in a low power system. UWB has many applications such as navigation systems, radio receiver and nowadays there are also researches for medical

imaging [5] and storage device [6]. Ultra wideband radio not only can carry a huge amount of data over a distance up to 230 feet but it also can carry signals through obstacles that tend to reflect signals at more limited bandwidths and a higher power [7]. The frequency band for UWB systems is 3.1GHz to 10.6GHz. The lower band of UWB is from 3.1 GHz to 5 GHz while the upper band is 5 GHz to 10.6 GHz [2]. The low power transmission is the key characteristic of the UWB system but slow progress in UWB standards development, high cost of initial implementations and performance much lower than expected are some of the reasons for the limited success of UWB in consumer products, which caused several UWB vendors to cease operations during 2008 and 2009 [8].

2.3 Noise Figure

Amplifier will amplify the input signal as well as the input noise with the same amount, at the same time the physical noise sources in the transistor will also propagate toward the output signal and this producing additional noise at the output. As a result it will degrade the signal to noise ratio (SNR) at the output. Noise factor and noise figure is used to measure the degradation of the SNR [1]. The formulas of noise factor (F) and noise figure (NF) are shown below [1]:

$$\text{Noise factor (F)} = \text{SNR input} / \text{SNR output} \tag{2.1}$$

$$\text{Noise Figure (NF)} = 10 \log (F) \tag{2.2}$$

In radio frequency (RF) communication receiver, noise figure is one alternatives of characterizing the receiver sensitivity [3]. Noise figure of LNA gives the biggest contribution of the receiver's total noise figure since LNA is at the receiver front-ends block. The formula of total noise figure (NFtot) is given in equation (2.3) [3]:

$$NF_{tot} = NF_1 + \frac{NF_2}{A_1} + \frac{NF_3}{A_1 A_2} + \frac{NF_4}{A_1 A_2 A_3} + ... \quad (2.3)$$

2.4 Gain

In an amplifier, gain is a measure of the ability to increase the power or amplitude of a signal [9]. It is usually defined as the mean ratio of the signal output of a system to the signal input of the same system [3]. There are many blocks in receiver system and each block will contribute noise to the signal (as shown in Figure 1). The total noise figure of the receiver depends on noise figure of each blocks and gain of previous stages. This can be seen in total noise figure (NFtot) formula in equation (2.3) where A is the gain and NF is the noise figure.

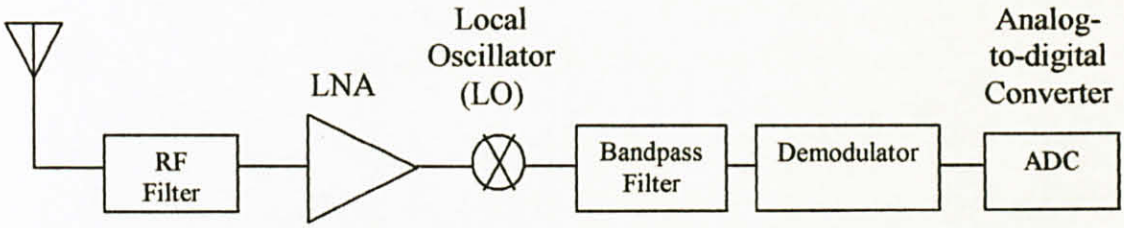


Figure 1: Block diagram of a simplified RF receiver [3]

LNA is the first block in the receiver excluding the antenna; therefore it is the most important block in determining the noise figure of the overall receiver. This lead to the fact that the low noise figure and high gain of the LNA is essential in the receiver design in order to reduce the total noise figure of the overall system.

2.5 Impedance Matching

The loss in transmission line is called characteristic impedance. Whilst the resistance of the output circuit that usually consisting of resistor, capacitor and inductor is called load impedance. When the signal propagates from the transmission line to the output circuit the signal will be reflected back if the characteristics impedance does not match with the load impedance. Impedance matching is used to maximize the power transfer to the load and minimize reflections from the load. Impedance matching is widely used for large bandwidth. It is very difficult to realize impedance matching over a large bandwidth because the imaginary part of the impedance depends on frequency [3]. In radio-frequency (RF) systems, a common value for source and load impedances is 50Ω, so in order to deliver the maximum power from the antenna to the LNA, 50Ω source matching impedance is required at the input port of the LNA. The reason of applying this impedance matching in LNA is to avoid reflection over the transmission line feeding the LNA and to minimize the noise figure of the circuit [3].

Matching networks can be implemented using lumped elements such as resistors, capacitors, inductors and transistors or distributed element which is transmission line. Designers usually choose to implement the network using lumped elements because in modern integrated circuit the lumped elements can be used for wide frequency bandwidth [1].

2.6 Topologies

Two common topologies of CMOS LNA that are widely used in design are common gate and common source with inductively source degeneration.

2.6.1 Common Gate

Common gate topology provides a wide band input matching that is insensitive to input parasitic and the return loss can be degraded at high frequency band by the input parasitic. The disadvantages of this topology is low power gain and difficult in realizing the input-output matching. Since it enables of producing low noise at high frequency band the common gate configuration is widely used for wide band applications. Nevertheless a careful consideration is needed for the input parasitic because it is the major factor of limiting high frequency amplifier performance [10]. Figure 2 shows common gate LNA.

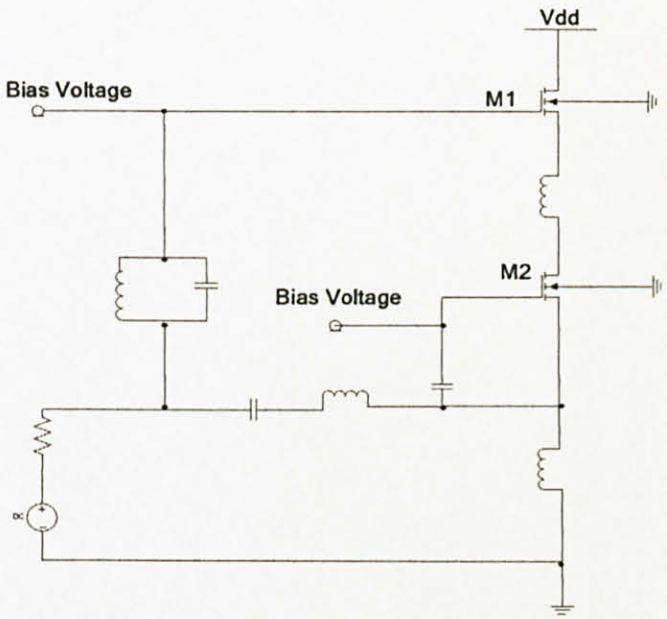


Figure 2: Common Gate LNA Topology [9]

2.6.2 Common Source (CS) with Inductively Source Degeneration

To overcome the increasing noise figure caused by resistor in LNA, inductor is used to replace the resistor and to match the input impedance. Small signal model of an inductively degenerated LNA is shown in Figure 3. This topology is very good in terms of noise figure and power consumption that is why many applications in industry had used this topology but it only suitable for narrowband applications. However in the last few years, due to low power consumption and the low noise figure capabilities of inductively degenerated LNAs; have motivated others to develop a new methodology for broadband applications [3] by exploiting gate-drain capacitor, C_{gd} and choosing output impedance appropriately allows the circuit to be broad banded [11].

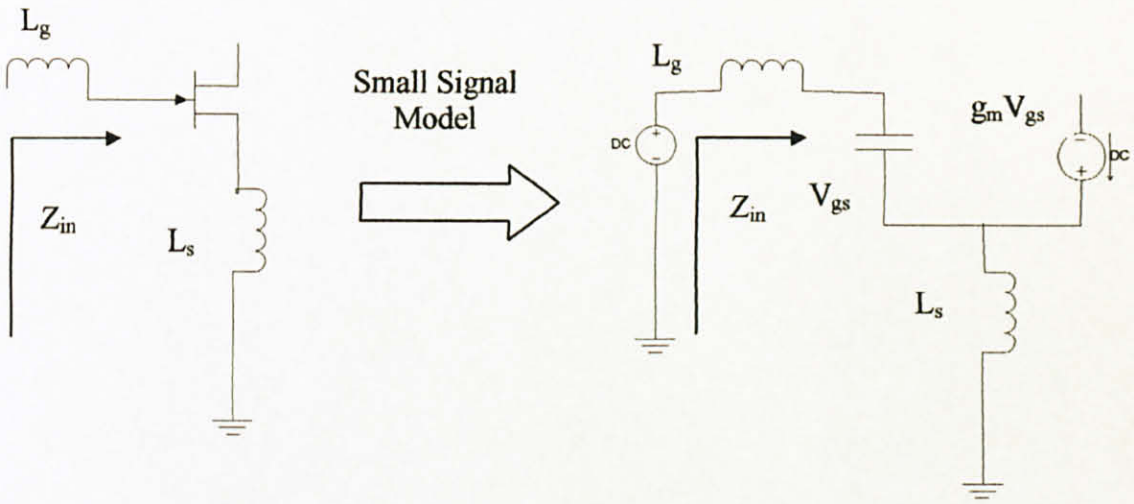
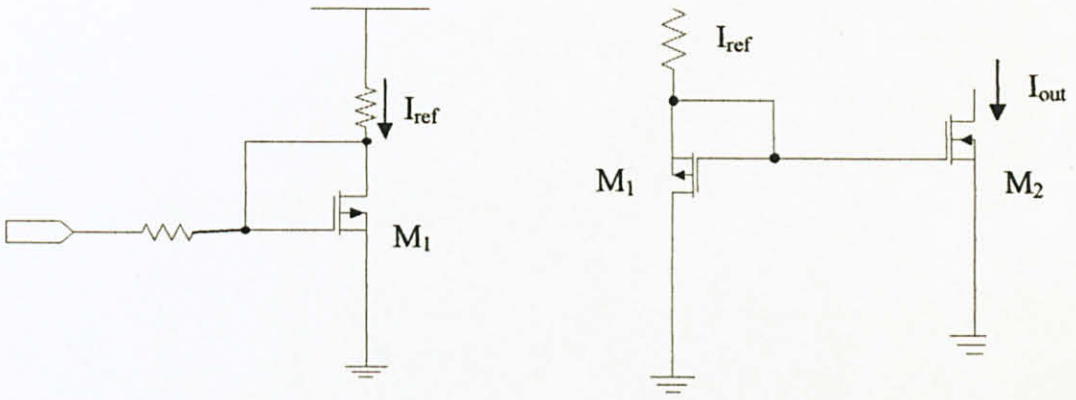


Figure 3: Small signal model of an inductively source degeneration LNA

2.7 Current Mirrors

Current mirrors as shown in Figure 4 (a) and (b) is used in analog circuit. The main function is to provide bias currents and act as active loads to circuits [12].



(a) Diode connected device (b) Basic current mirrors

Figure 4: Current Mirrors circuits

The advantage of current mirror is that it allows copying of the exact current with less dependence on process and temperature [12]. The ratio of output current, I_{out} and reference current can be controlled by changing the size (W/L) of transistor. The equation that relates I_{out} to I_{ref} is given in equation (2.4):

$$I_{out} = I_{ref}\left(\frac{\frac{W_{M2}}{L_{M2}}}{\frac{W_{M1}}{L_{M1}}}\right) \tag{2.4}$$

CHAPTER 3

METHODOLOGY

3.1 Research and Design Consideration

For this project, understanding the basic knowledge and the problems related to LNA were essential because it would lead to the LNA design criteria and requirements. The research is carried out through the internet and library to collect and review the related papers, books, and all related information on the LNA design. The flow chart of the project is shown in Figure 5. In this project a Common Source (CS) with Inductively Source Degeneration topology has been chosen because its enables to produce a low noise figure, high gain and low power consumption which are mandatory requirements for many of today's wireless receivers. The design of LNA circuit topology (as shown in Figure 6) parameters is described in section 3.2.

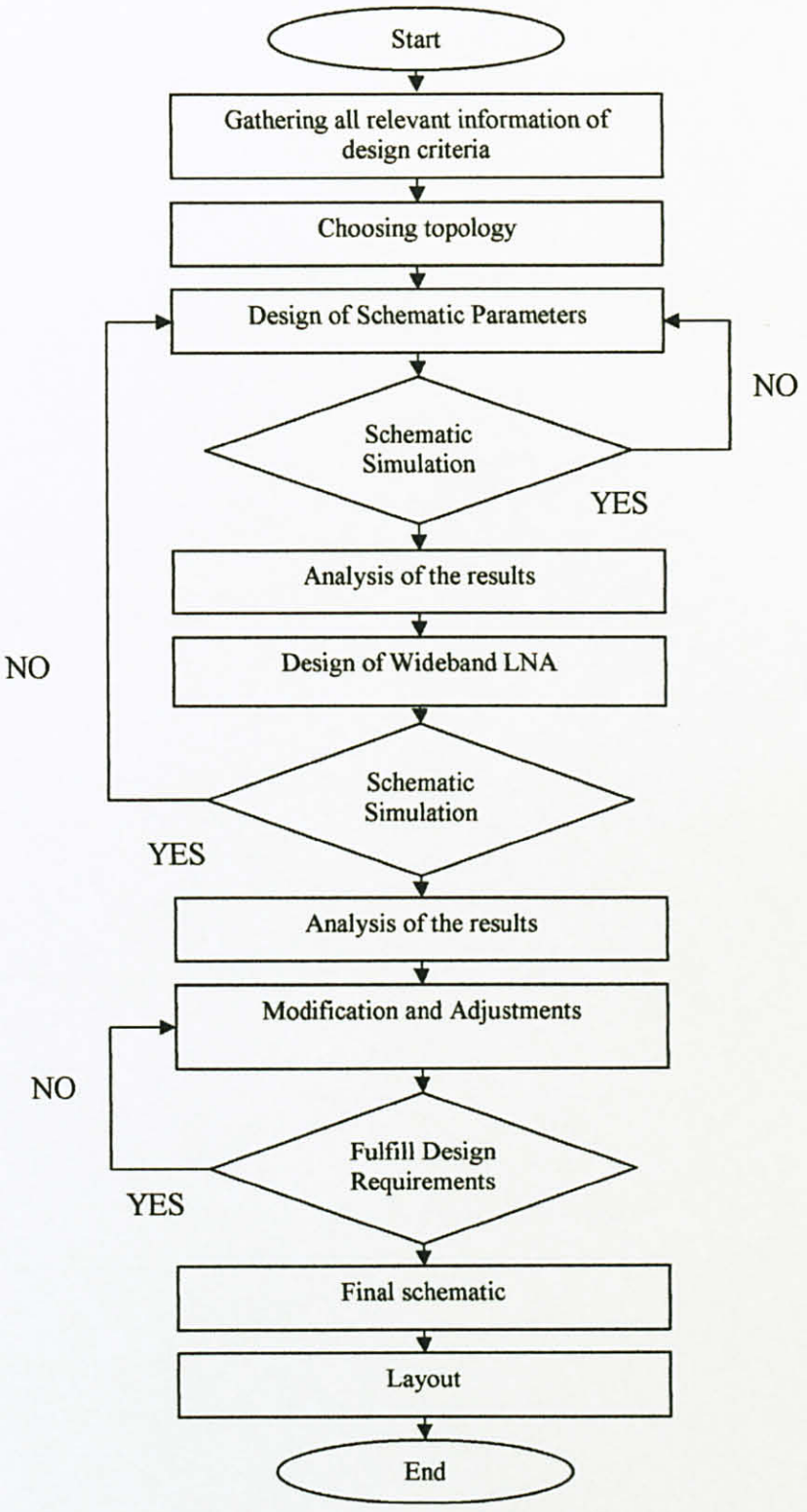


Figure 5: Flow chart of the project

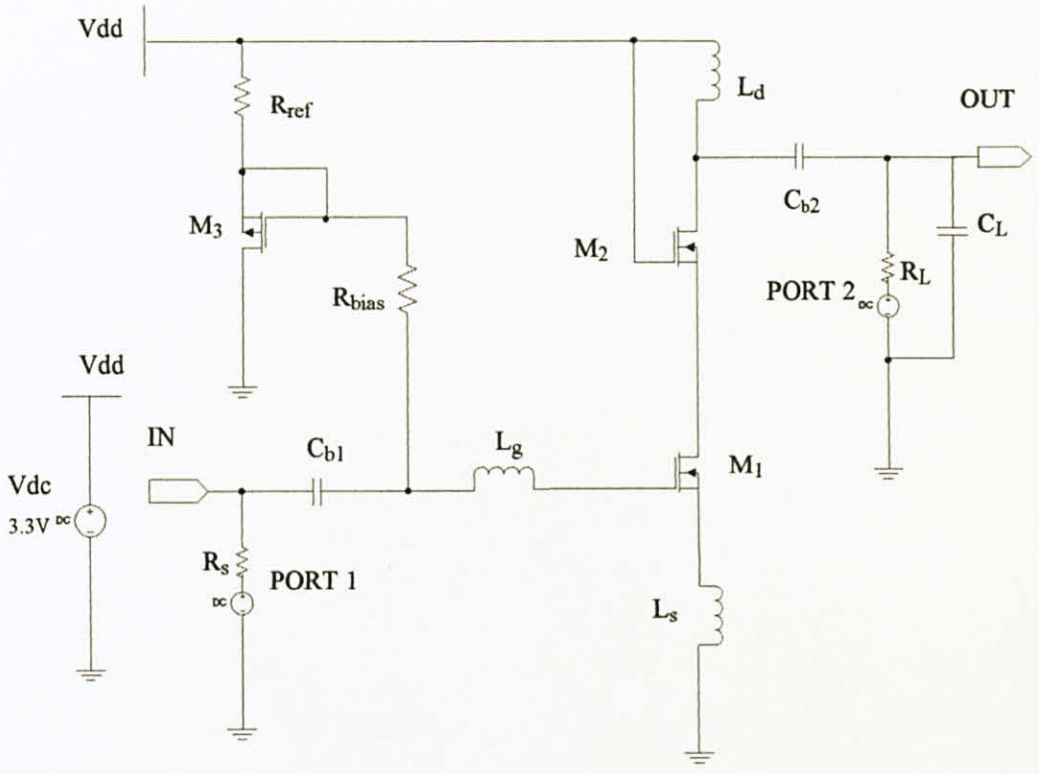


Figure 6: Common Source (CS) with Inductively Source Degeneration topology

3.2 Design of Schematic Parameters

Step 1

For this project, the LNAs are designed and simulated using Cadence Spectre RF IC design software in AMI06 CMOS process technology. The parameters of this technology are given in the Appendix A. The value of 50 Ω is chosen for input and output impedance, (R_s and R_L) because most of the receiver systems require 50 Ω inputs and outputs impedance matching for proper operation.

The technology parameters that needed for the calculation are as follows:

$t_{ox} = 1.41 \times 10^{-8}$m

$\mu_n = 533.695\ cm^2/Vs$

$L_{eff} = 0.6\mu m$

$\varepsilon_{ox} = 3.45 \times 10^{11}$

$$C_{ox} = \frac{\varepsilon_{ox}}{\tau_{ox}} = \frac{3.45 \times 10^{11}}{1.41 \times 10^{-8} m} = 2.447 mF / \mu m \tag{3.1}$$

$$k_n = \mu_n C_{ox} = 533.695 cm^2 / Vs \times 2.447 mF / \mu m = 130.595 \mu A / V^2 \tag{3.2}$$

Step 2

For simplicity, the value of C_{gd}, r_g and r_o have been ignored [13]. Equation (3.3) was used to calculate the width of transistors M_1 and M_2. For this LNA, the width of M_2 is chosen to be equal to the width of M_1 for easy calculation purpose and to simplify the layout design.

$$W_{M1} = \frac{1}{3\omega_o L_{eff} C_{ox} R_s} \tag{3.3}$$

$W_{M1} = W_{M2}$

Step 3

The gate source capacitance, C_{gs}, transconductance of the transistor, g_m and transit frequency, ω_t was then calculated from the following equations in order to find the value of source inductor, L_s [13]:

$$C_{gs} = \frac{2}{3} WLC_{ox} \tag{3.4}$$

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_{out}} \tag{3.5}$$

$$\omega_t = \frac{g_m}{C_{gs}} \tag{3.6}$$

$$L_s = \frac{R_s}{\omega_t} \tag{3.7}$$

Step 4

In order to achieve low power consumption for the LNA, the value of reference current, I_{ref} for the current mirror is chosen to be 1mA. This value is chosen for easy calculation purpose and 1mA is a low value for current. The formula for the reference current, I_{ref} is given in equation (3.8) [14]:

$$I_{ref} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_t)^2 \tag{3.8}$$

In order to get a reference current of 1mA, a reference resistor, R_{ref} is placed at the drain of the biasing transistor, M_3 (as shown in Figure 6) the value of R_{ref} is determined by equation (3.11) [14].

$V_t = 0.7088V$ (see Appendix A)

$$V_{eff} = V_{gs} - V_t = \frac{g_m L}{\mu_n C_{ox} W} \tag{3.9}$$

$$V_{gs} = V_{eff} + V_t \tag{3.10}$$

$$R_{ref} = \frac{V_{dd} - V_{gs}}{I_{ref}} \tag{3.11}$$

Where,

V_t = Threshold voltage (V)

V_{eff} = Voltage efficiency (V)

V_{gs} = Gate-source voltage (V)

V_{dd} = Drain to drain voltage (V)

The bias resistor, R_{bias} is placed at the gates of the current mirror transistors to provide Radio Frequency (RF) isolation between the current mirror and the driver stage of the LNA [14]. The value is chosen large enough so that its equivalent noise current is small enough to be ignored.

$R_{ref} = R_{bias}$

Step 5

Biasing transistor, M_3 forms a current mirror with M_1. So, the width of M_3 must be smaller than M_1 to minimize power overload by the biasing circuit.

Referring to equation (2.4), the drain current, I_{out} of the LNA is a function of reference current, I_{ref}, transistor width and length parameters. Its value was set to 5mA by scaling the current mirror according to the equation (2.4) [14]. Then, the power consumption of the LNA was calculated by the formula below:

Voltage supply = 3.3V

Power consumption, P = VI (3.12)

To complete the biasing, direct current (dc) blocking capacitor, C_b must be present to prevent upsetting the gate source bias of M_1. The value of C_b should have negligible reactance at the signal frequency. The suitable value for C_b must be larger than 10pF [15]. For this design the value of 10pF was chosen for blocking capacitor, C_b.

Step 6

From the equations below the value of the gate inductor, L_g can be calculated [13]:

$$L_g + L_s = \frac{1}{C_{gs}\omega_o^2} \tag{3.13}$$

$$L_g = \frac{1}{C_{gs}\omega_o^2} - L_s \tag{3.14}$$

Step 7

Drain inductor, L_d value of 10nH was chosen for both LNAs. 10nH had been chosen because from the analysis that had been performed for different values of drain inductor, L_d, the results showed that when the value was less than 10nH the schematic of UWB LNA cannot amplify and when the value was higher than 10nH the value of noise figure will increase. The required value of load capacitor, C_L at the operating frequencies of 1.575GHz and 4GHz was calculated by the equation below [15]:

Angular frequency, $\omega_o = 2\pi f$ (3.15)

$$C_L = \frac{1}{L_d \omega_o^2} \tag{3.16}$$

3.3 Calculation of Noise Figure

In order to analyze the performance of LNA, comparisons between the theoretical expectation and simulation result of the noise figure, NF is required. The minimum noise figure, NF_{min} was calculated by equation (3.17) [13]:

$$NF_{min} = 1 + 2.4\frac{\gamma}{\alpha}\frac{\omega_o}{\omega_t} \tag{3.17}$$

For AMI06 CMOS process technology, the value of body coefficient, γ cannot be recognized so in this calculation the value of γ was assumed to be the same with 0.35μm CMOS process technology, namely, $\gamma = 2$.

3.4 Analysis of the LNA Performance

To check whether the circuit of LNA can act as an amplifier or not; an operating frequency of 1.575GHz has been chosen for this analysis. This was due to the fact that global positioning systems operate at a frequency of 1.575426GHz which is approximates to 1.575GHz [15]. The input voltage values for this amplification were 200mV, 80mV and 1mV. The values of 200mV and 80mV are chosen since many wireless products use these values as an input voltage [16] whereas, an input voltage of 1mV is to investigate if the LNA could amplify a very weak signal. Then, the results of gain, noise figure and power consumption of this LNA are analyzed for modification purpose in order to design wideband LNA that has high gain, low noise figure and low power consumption. To fulfill this design requirement; the performance of the wideband LNA had been analyzed by varying the values of operating frequencies, f_o, drain and load inductor (L_d and L_L) as well as output current, I_{out}. The result of the analysis is shown in Table 3 and the calculation for minimum noise figure for GPS and UWB LNA is given in Appendix B.

3.5 Analysis of the Frequency Range

In order o design a wideband LNA that can operate in lower band frequency of UWB system, the analysis of the frequency range of the LNA is carried out using four different operating frequencies. From the calculation, it has been discovered that the width of the transistor is inversely proportional to the operating frequency. The frequency gets higher when the width of the transistor became lower. Because of this fact, the frequency range of the LNA has been analyzed using three different width values for each operating frequency. Table 1 shows the result of the analysis.

Table 1: Data of frequency range at 1.576GHz, 3.5GHz, 4GHz and 4.5GHz

Operating Frequency, f_o	Width	Low Frequency, f_L	High Frequency, f_H
1.576GHz	454μm	1.0GHz	1.8GHz
	227μm	1.2GHz	2.2GHz
	113.5μm	1.5GHz	2.9GHz
3.5GHz	206.49μm	2.6GHz	3.6GHz
	103.245μm	3.3GHz	4.4GHz
	51.6225μm	Not Amplify	
4GHz	181.63μm	3.1GHz	4.1GHz
	90.815μm	3.8GHz	5.0GHz
	45.4075μm	Not Amplify	
4.5GHz	160.59μm	3.6GHz	4.7GHz
	80.295μm	4.4GHz	5.7GHz
	40.1475μm	Not Amplify	

From this analysis, it can be seen that by lowering the width of the transistor the frequency (f_L and f_H) of the LNA become higher but the frequency band of the LNA is still narrow which is approximately 1GHz. In order to improve the bandwidth of the LNA, shunt peaking load is used at the drain of the cascode transistor, M_2 as shown in Figure 10. For common source amplifier, its gain is proportional to g_mR_L. When a capacitive load, C_L is added, the gain will decrease as the frequency increase because the capacitor's impedance diminishes. However the addition of an inductance (L_L) provides an impedance component that increases with increasing frequency (it introduces a zero contrast with a simple RC case) [17]. The value of L_L is chosen large enough so that it does not deteriorate the impedance matching at high frequencies [3]. This helps to offset the decreasing impedance of the capacitance, leaving net impedance roughly constant over a broader frequency range than that original RC network [17]. Figure 7 shows the model of a shunt peaked circuit.

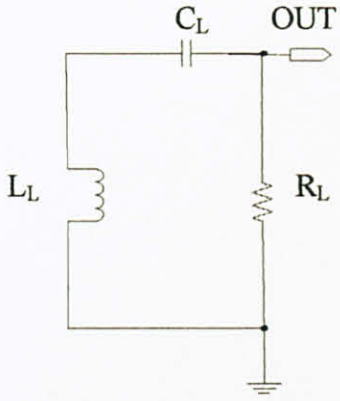


Figure 7: Model of the shunt peaked circuit

3.6 Design of Layout

Layout is the next step of this project after successfully simulated the schematic of the UWB LNA. There are two process that can be chosen in completing the layout, namely automatic layout process and manual layout process. In automatic layout process the transistors are generated automatically, they are created exactly according to the parameters in the schematic but this will build extremely large gate widths transistors [14]. However, the automatic layout process may save time by creating the transistors for the user since to build each transistor would have been extremely times consuming. With manual layout, the transistor will be build from scratch, using the LSW (Layer Selection Window) to select the appropriate materials for each layer.

For this project, the automatic layout process was initially selected since the manual layout technique would have been extremely time consuming. However, a disadvantage of the automatic layout was discovered. Although the automatic layout technique does save time by creating the transistors for the user but it does not build the transistors in a space efficient manner. The transistors widths used in the UWB LNA circuit topology were very large namely, 110μm, 45μm and 40μm. A single large transistor layout is not a good idea. Generally for (p-type Metal Oxide Semiconductor) PMOS transistor the width must be less than 50μm and for (n-type Metal Oxide

Semiconductor) NMOS transistor the width must be less than 30μm [18]. When the transistors were generated automatically, they were created exactly according to the parameters mentioned in section 4.2, resulting in transistors with extremely large size. Since the automatic tool did not optimize the design area; manual layout technique was chosen for the UWB LNA layout design.

With manual layout, the width and length parameters could be adjusted by placing multiple transistors in series; the width was split into smaller units known as fingers. The use of fingers allowed for smaller devices to be used, which optimized the total area occupied by the UWB LNA circuit. To design transistor width of 110μm, four transistors of 27.5μm /0.6μm are used. For width of 40μm and 36.3μm, two transistors of 20μm /0.6μm and 18.15μm /0.6μm are used. The widths of the transistors are chosen to be less than 30μm because the UWB LNA circuit topology used NMOS transistors. With fingers, the correct width of the transistor is still achieved, but with more compact design [14]. In this project only layout of UWB LNA transistors will be design due to the time constraint since to do layout for other components need more research and analysis. The layout of the cascade transistors M_1 and M_2 is shown in Figure 8 whilst Figure 9 illustrates the layout of connection between the common drain transistor and current mirror bias to the cascade transistors M_1 and M_2. Then, the layout will be verified by the Design Rule Check (DRC) in order to check if there has any error in the layout. The result of DRC is given in Appendix C.

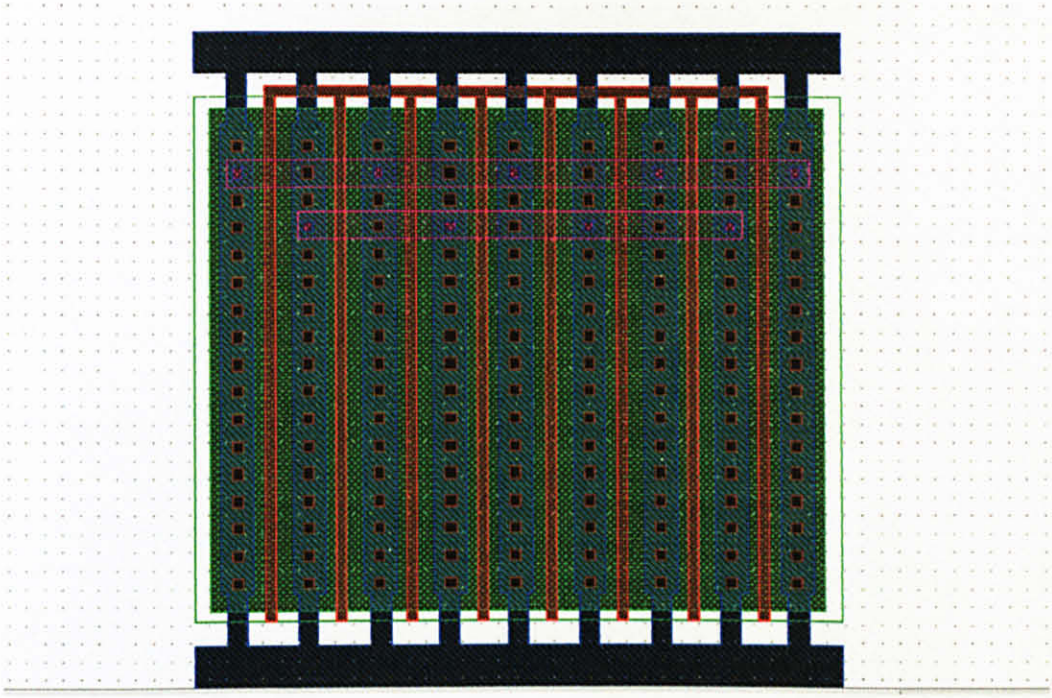


Figure 8: Layout of the cascade transistors M_1 and M_2

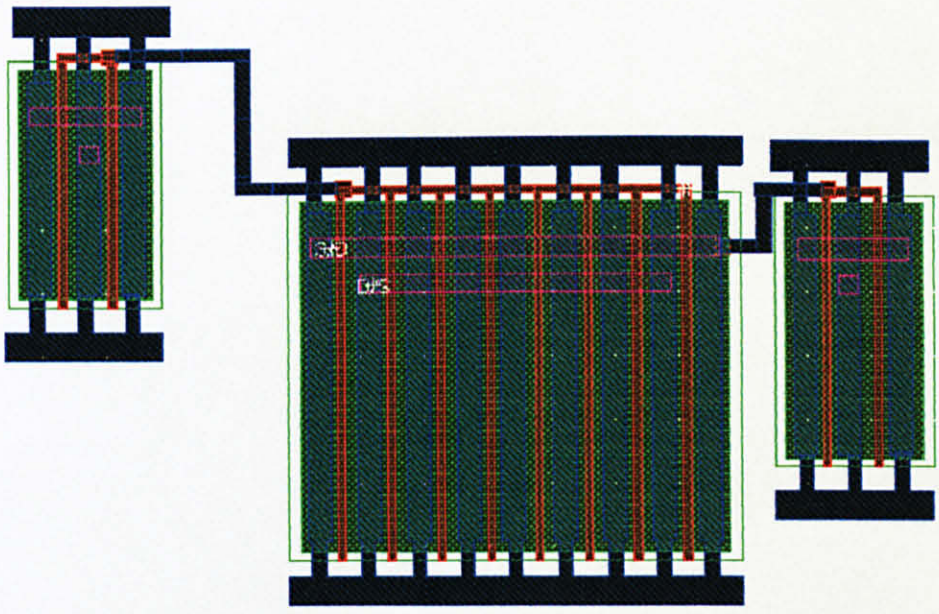


Figure 9: Layout of LNA transistors

CHAPTER 4

RESULT AND DISCUSSION

4.1 Result of the Global Positioning System (GPS) LNA

For the first LNA design, the operating frequency of GPS which is 1.575GHz is chosen as the operating frequency. In order to analyze and simulate the LNA circuit topology, 3.3V voltage supply and two-port network are used. Two-port network is used for impedance matching purposes. The complete schematic of the LNA is shown in Figure 10 and the performance of the LNA is summarized in Table 2.

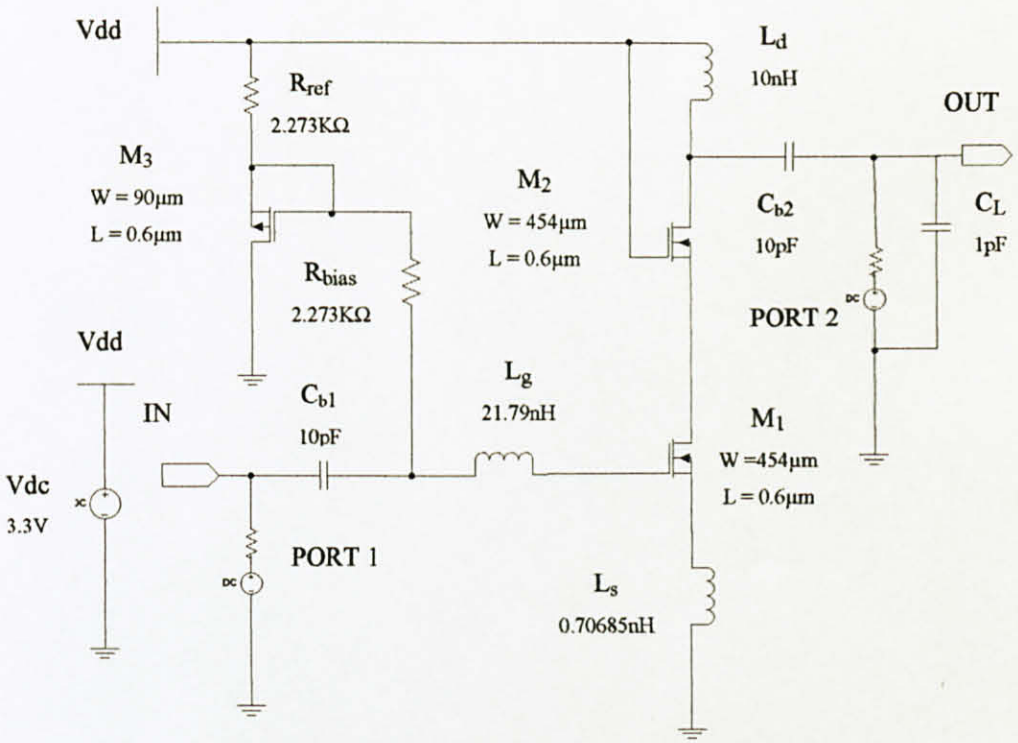


Figure 10: Complete circuit of GPS LNA

Table 2: Summary of GPS LNA performance

Features	Calculation	Simulation
Frequency	1.575GHz	1 – 1.8GHz
Noise Figure, NF	1.678dB	$\leq$ 2.518dB
Gain	-	21.348 - 25.513dB
Power	16.5mW	-

As expected, the calculation and simulation values of the noise figure are slightly different due to the value of γ that cannot be recognized. Even though, the simulated value is higher than the calculated one, it is still low and acceptable since the calculated value is the minimum and not the maximum noise figure of the LNA. From Table 2 it shows that the frequency range of GPS LNA is narrow, so it can not be used for wideband LNA. Modification of the schematic must be done in order to develop wideband LNA.

4.2 Result of the Ultra Wideband (UWB) LNA

The second LNA was designed to operate in the frequency range of 3.1 – 5 GHz, which covers the lower frequency band of UWB systems. The schematic of this LNA is similar to the first LNA, except that the common drain amplifier is added at the load of the LNA to act as a source follower. A shunt peaking load is used at the drain of the cascode transistor to improve the bandwidth of the LNA as can be seen in Figure 11. The analysis of the LNA performance is summarized in Table 3.

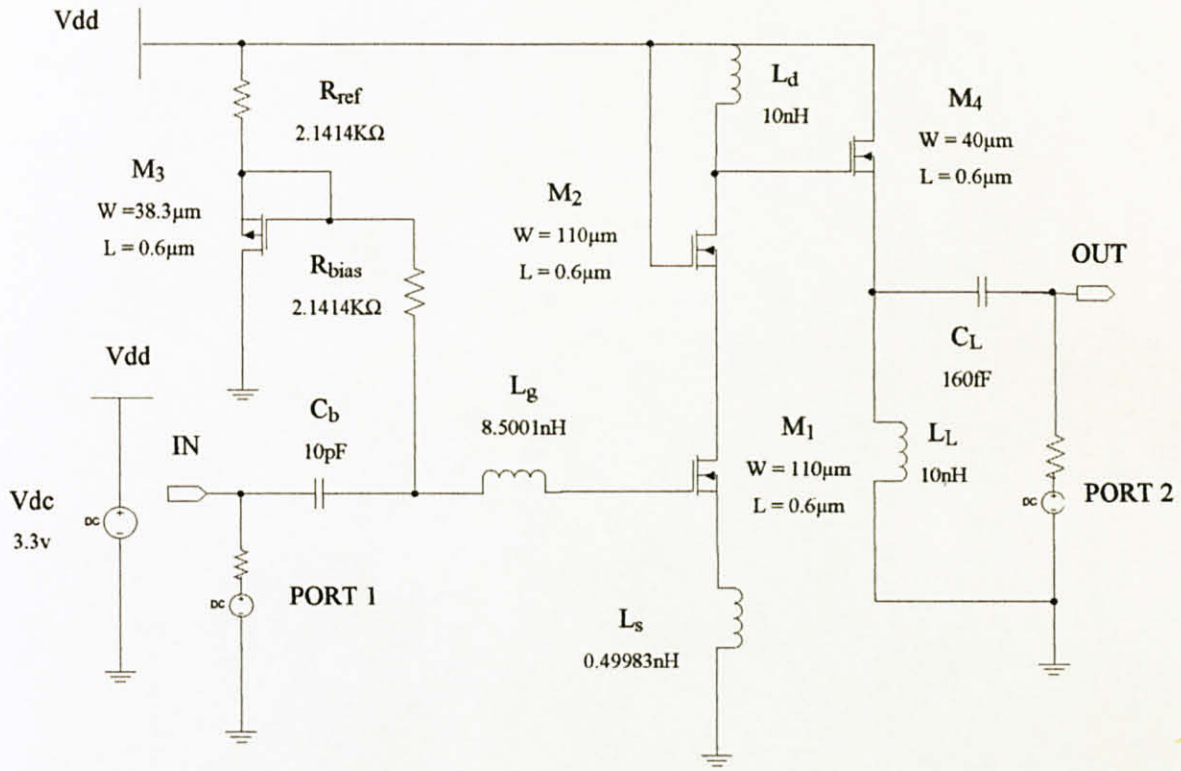


Figure 11: Complete circuit of UWB LNA.

Table 3: Data of noise figure and gain at 4.5GHz, 4GHz and 3.5GHz

Operating Frequency, f_o (GHz)	I_{out} (mA)	Width (μm)	L_d L_L (nH)	Frequency Range (GHz)	Noise Figure, NF (dB)	Gain (dB)
4.5	4	160.59	5	Not amplify		
4.5	4	160.59	10	3.5 – 5.5	1.465 – 7.061	2.1652 – 13.083
4.5	4	130	10	3.4 – 5.6	1.341 – 7.432	2.0608 – 12.675
4.5	4	120	10	3.5 – 5.8	1.294 – 6.742	2.1633 – 12.49
4.5	4	110	10	3.7 – 6.1	1.237 – 7.494	2.2655 – 12.163
4.5	4	160.59	15	3.0 – 5.0	2.338 – 8.031	3.5484 – 13.825
4.5	4	130	15	3.2 – 5.5	1.813 – 7.178	3.6241 – 13.119
4.5	4	120	15	3.4 – 5.6	1.736 – 7.289	3.7979 – 12.887
4.5	4	110	15	3.6 – 5.9	1.656 – 8.87	3.9498 – 12.572
3.5	4	206.49	5	3.5 – 4.5	Small bandwidth not acceptable	
3.5	4	206.49	10	2.5 - 4.5	1.731 – 9.128	12.462 – 18.748
3.5	4	160	10	2.8 – 4.6	1.837 – 7.812	13.48 – 17.361
3.5	4	130	10	3.1 – 4.8	1.993 – 7.453	12.818 – 16.159
3.5	4	120	10	3.2 – 5.0	1.985 – 7.795	12.411 – 15.772
3.5	4	110	10	3.4 – 5.2	2.038 – 8.075	11.999 – 15.11
3.5	4	206.49	15	2.3 – 4.1	1.235 – 9.263	2.4505 – 19.607
3.5	4	160	15	2.4 – 4.5	1.298 – 8.498	4.8639 – 18.946
3.5	4	130	15	2.7 – 5.0	1.278 – 9.577	3.1704 – 17.538
3.5	4	120	15	2.8 – 5.2	1.287 – 9.927	3.7419 – 17.084
3.5	4	110	15	2.8 – 5.4	1.312 – 10.02	2.7419 – 17.02
4	4	181.63	10	2.5 – 5.0	4.387 - 8.04	1.392 - 6.489
4	4	160	10	2.7 – 5.1	1.167 – 8.595	2.287 - 6.789
4	4	130	10	2.9 – 5.3	1.406 – 7.14	2.223 - 6.66
4	4	120	10	3.0 – 5.5	2.362 – 10.14	1.929 - 6.449
4	4	110	10	3.2 – 5.6	2.0112-13.64	-5.223 - 6.389
4	5	181.63	10	2.6 – 4.7	≤3.698	19.362 - 24.657
4	5	160	10	2.9 – 4.9	≤3.445	19.532 - 24.784
4	5	130	10	2.9 – 5.1	≤3.579	19.115 - 24.331
4	5	120	10	3.0 – 5.2	≤3.337	20.346 - 24.513
4	5	110	10	3.1 – 5.3	≤3.280	20.312 – 25.238

The data from Table 3 shows that the most suitable value for L_L and L_d is 10nH. When the values of L_L and L_d are not the same, the UWB LNA could only amplify at a very weak signal which was less than 10mV. Three different output drain current, I_{out} values have been chosen in order to see whether the noise figure and gain of the UWB LNA could be improved. From Table 3 it shows that the noise figure and gain of the UWB LNA were improved by increasing the drain current, I_{out} value. When the drain current, I_{out} value get higher the noise figure values of the LNA get lower. This is due to the fact that the value of transit frequency, ω_t hence low noise figure on expense power consumption. From this analysis, operating frequency, f_o of 4GHz, drain current, I_{out} value of 5mA and transistors width of 110μm for M_1 and M_2 were chosen for the UWB LNA of this project.

4.2.1 Result of Output Voltage

Figure 12, Figure 13 and Figure 14 show the amplification of the output voltage signals at three different input voltage signals. As shown in Figure 12, Figure 13 and Figure 14 the lower amplitude signal in red color is the input signal; whilst the higher amplitude signal in blue color is the output signal. The voltage differences between the input and output voltage signals have shown that the UWB LNA can amplify weak input signals at different input voltages and frequencies. Even tough the amplitude of input and output signal is high for this project but it acceptable because different UWB applications require different amplitude value. Example; UWB system for application that consists of reflector need amplitude of output voltage higher than 100 kV and for UWB system with an electromagnetic field pulse requires amplitude of more than 5 kV/m and a rise time of less than 500 ps [4].

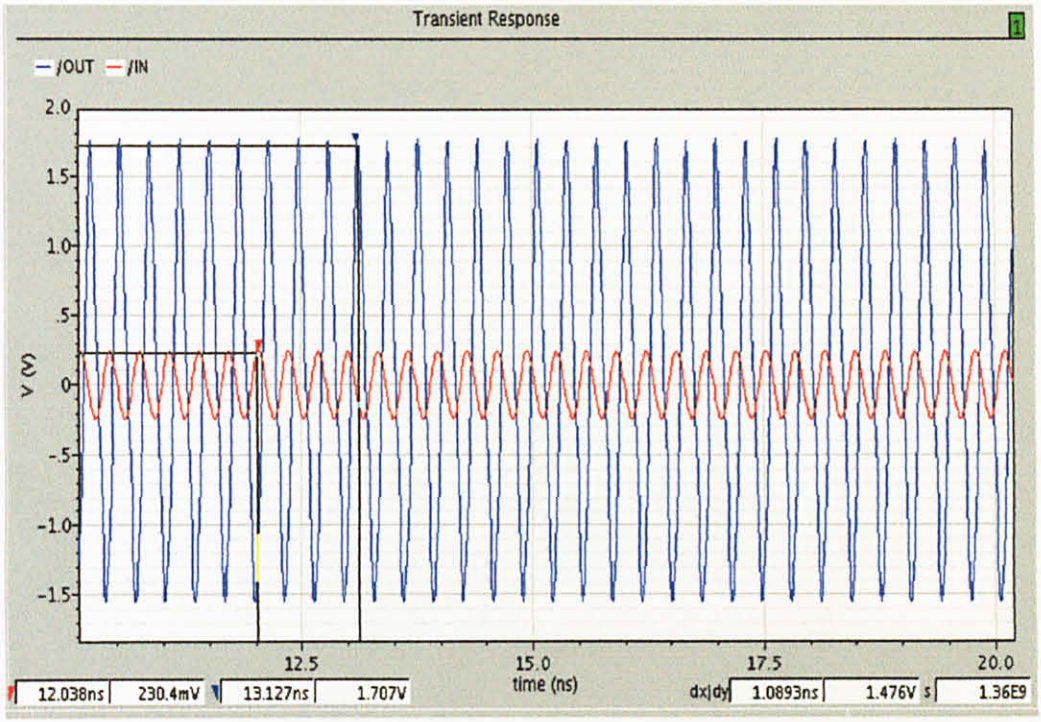


Figure 12: The amplification of 200mV input voltage at 3.1GHz

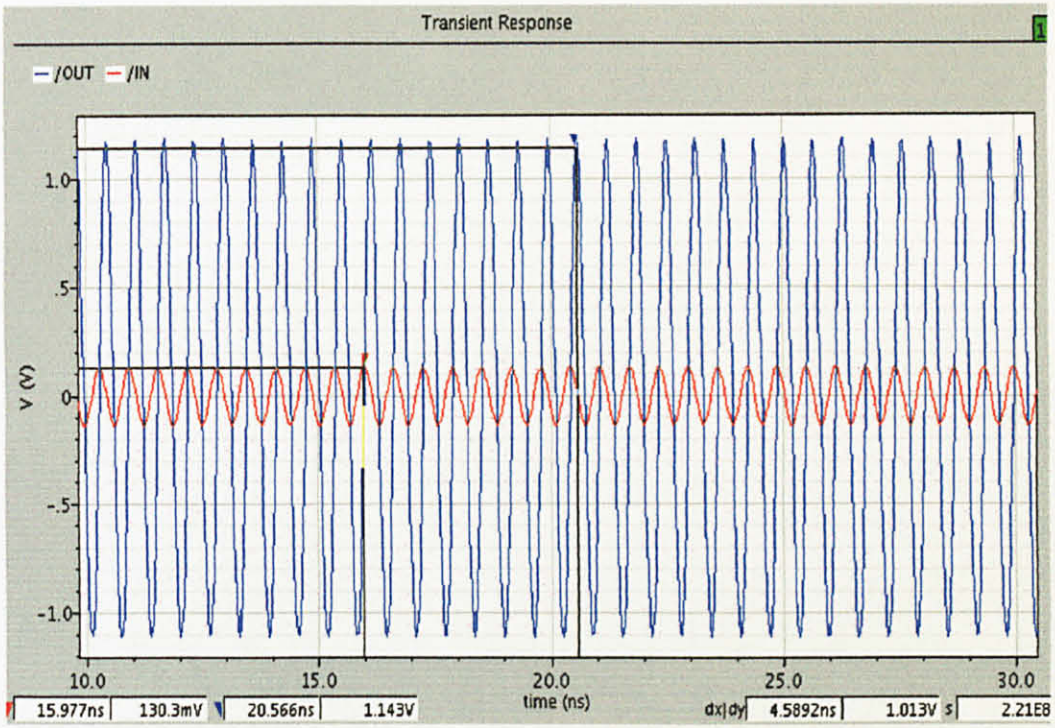


Figure 13: The amplification of 80mV input voltage at 4GHz

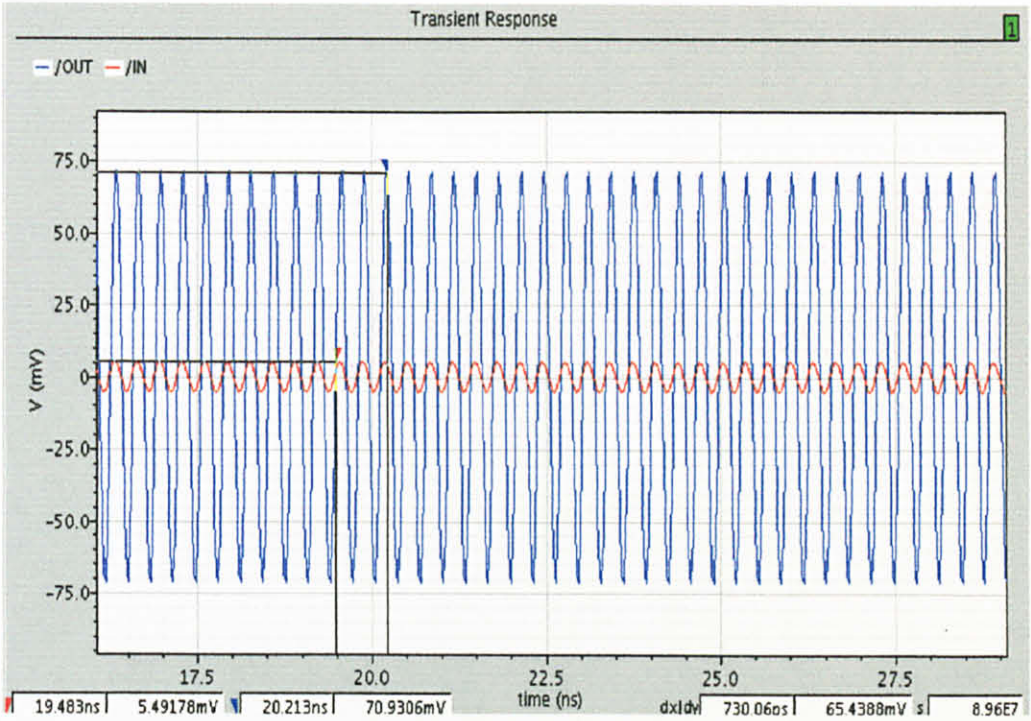


Figure 14: The amplification of 1mV input voltage at 5GHz

4.2.2 Result of Noise Figure (NF) and Gain

Figure 15 and Figure 16 illustrate the simulated performance of noise figure and gain of the UWB LNA. In Figure 15, it can be seen that the LNA achieved noise figures less than 3.28dB. Whilst Figure 16 shows that the gain of the UWB LNA was in the range of 20.312 – 25.238dB. The performance of the Ultra Wideband (UWB) LNA is summarized in Table 4.

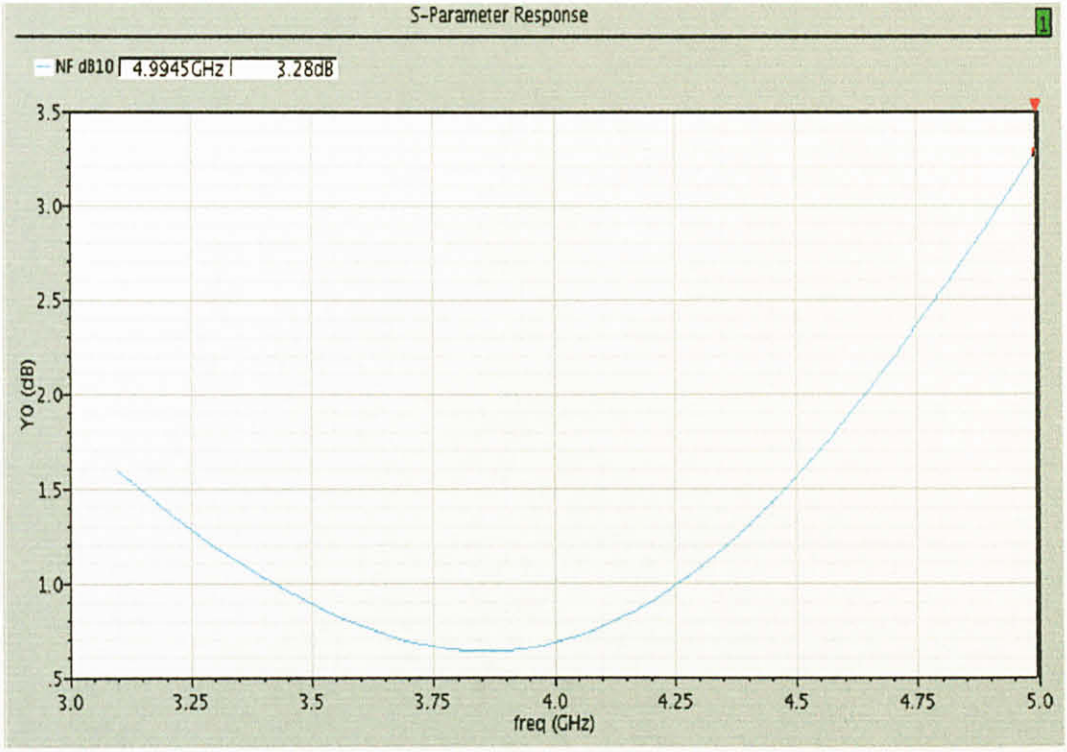


Figure 15: Result of noise figure at frequency of 3.1 - 5GHz

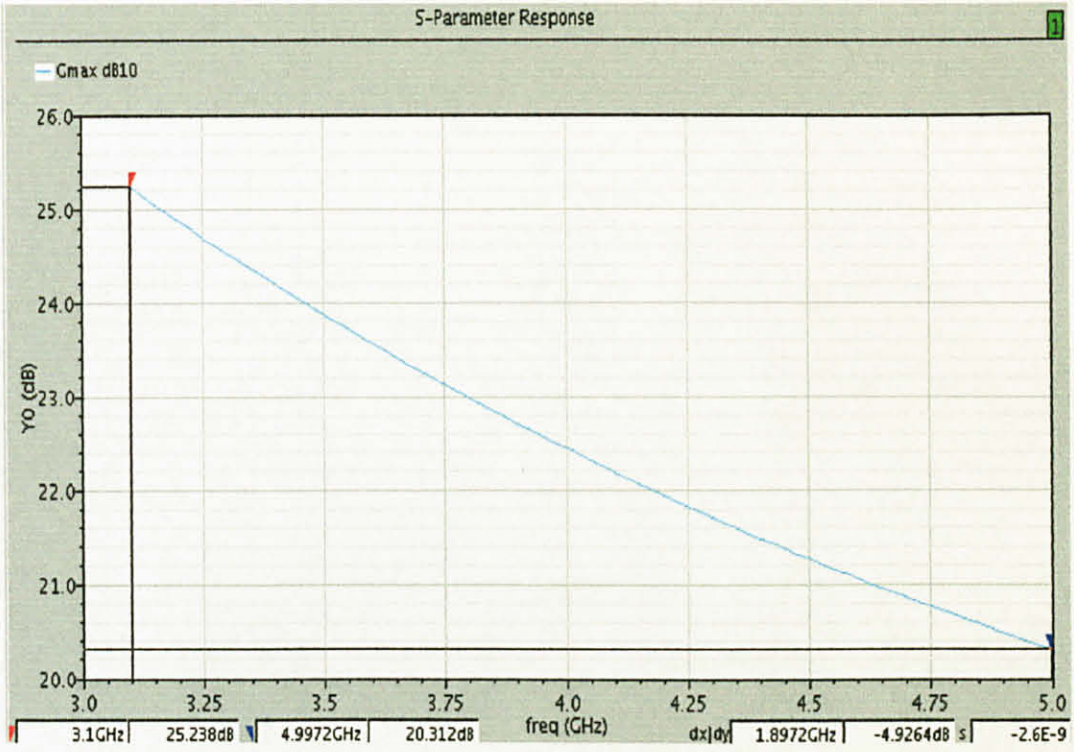


Figure 16: Result of gain at frequency of 3.1 – 5.0GHz

Table 4: Summary of UWB LNA performance

Features	Calculation	Simulation
Frequency	4GHz	3.1 – 5.0GHz
Noise Figure, NF	2.072dB	$\leq$ 3.280dB
Gain	-	20.312 – 25.238dB

The simulated noise figure of the UWB LNA is low and acceptable. This is true since when compared to the calculated value the simulated minimum noise figure of the UWB LNA is lower as can be seen in Figure 15. The power consumption of this LNA can not be verified because Cadence Spectre can not generate the result but due to the low value of the drain current, I_{out} it can be assumed that the power consumption of the LNA is low. Moreover the requirement for maximum total requirement for UWB system is 100mW and 250mW [19]. Table 4 shows that the frequency range of UWB LNA covers the lower band frequency of UWB system. Thus the objective of this project to develop wideband LNA has been achieved.

CHAPTER 5

CONCLUSION AND RECOMMENDATION

5.1 Conclusion

By taking into account the simulation results of both LNAs, the objectives of this project were achieved. The important parameters in this design are the width of the transistors and the operating frequency of the LNA. From these parameters, the values of resistors, inductors and capacitors involved are calculated. By using current mirror and low bias current (I_{ref}) the total power consumed by the LNA is reduced.

The use of Cadence Spectre RFIC design software facilitated the analysis of the LNAs performances. It also allowed for comparisons between theoretical expectation and simulated results. With Cadence Spectre facilitated, it proves that the design method of this project can be applied for designing any wideband LNA in CMOS process technology.

Although the LNA design is the primary focus of the project, a deeper understanding of the UWB systems is also developed. Through interaction and discussion with the project supervisor, a better insight into design work and the application of engineering principles is gained.

5.2 Recommendations

Impedance matching and the linearity performance of the LNA are not priories in the development of the LNA. The linearity of the LNA requires further investigation to clarify the effects to frequency variation of the LNA. Applying a proper method for impedance matching; it can be achieved by two methods which are by calculation and using suitable software that has network analyzer tool. Research and study the different matching networks in more detail in order to develop more flexible wideband LNA design that can fulfill the required gain and noise figure.

In designing LNA, layout is important aspect that can be developed. Research and study in designing layout of all types of components such as resistor, capacitor and inductor are important in RF IC design. Once the layout of all LNA components is completed and all errors have been successfully removed, the next step is making sure that the layout has been implemented according to the original design schematic. Layout is essential facet in developing LNA because LNA can not be fabricated into chip without it.

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APPENDICES

Appendix A

Parameters of AMI06 CMOS Process Technology

```
N8BN SPICE BSIM3 VERSION 3.1 (HSPICE Level 49) PARAM
* Level 11 for Cadence Spectre
* DATE: Jan 25/99
* LOT: n8bn                    WAF: 04
* Temperature_parameters=Default
.MODEL ami06N NMOS ( LEVEL =11 &
VERSION=3.1 &
TNOM=27 &
TOX=1.41E-8 &
XJ=1.5E-7 &
NCH=1.7E17 &
VTH0=0.7086 &
K1=0.8354582 &
K2= 0.000431 &
K3=4 .4405818 &
K3B= 14 &
W0=6.480766E-7 &
NLX=1E-10 &
DVT0W=0 &
DVT1W=5.3E6 &
DVT2W=-0.032 &
DVT0=3.6139113 &
DVT1=0.3795745 &
DVT2=-0.1399976 &
U0=533.0053445 &
UA=7.55802E-10 &
UB=1.181167E-18 &
UC=2.582756E-11 &
VSAT=1.300981E5 &
A0=0.5292985 &
AGS=0.1463715 &
B0=1.283336E-6 &
B1=1.408099E-6 &
KETA=-0.0173166 &
A1=0 &
A2=1 &
RDSW=2 268366E3 &
PRWG=-1E-3 &
PRWB=6.320549E-5 &
WR=1 &
WINT=2.043512E-7 &
LINT=3.034496E-8 &
XL=0 &
XW=0 &
DWG= 1.446149E 0 &
DWB=2.07754E-8 &
VOFF= 0.137226 &
NFACTOR=1.2880596 &
CIT=0 &
CDSC=1.506004E-4 &
CDSCD=0 &
CDSCB=0 &
CIT=0 &
CDSC=1.506004E-4 &
CDSCD=0 &
CDSCB=0 &
ETA0=3.815372E-4 &
ETAB=-1.029173E-3 &
DSUB=2.173055E-4 &
PCLM=0.6171774 &
PDIBLC1=0.185386 &
PDIBLC2=3.475187E-3 &
PDIBLCB=-1E-3 &
DROUT=0.4037723 &
PSCBE1=5.998012E9 &
PSCBE2=3.700030E 0 &
PVAG=0.012927 &
DELTA=0.01 &
MOBMOD=1 &
PRT=0 &
UTE= 1.5 &
KT1=-0.11 &
KT1L=0 &
KT2=0.022 &
UA1=4.31E-9 &
UB1=-7.61E-18 &
UC1=-5.6E-11 &
AT=3.3E4 &
WL=0 &
WLN=1 &
WW=0 &
WWN=1 &
WWL=0 &
LL=0 &
LLN=1 &
LW=0 &
LWN=1 &
LWL=0 &
CAPMOD=2 &
XPART=0.4 &
CGDO=1.99E-10 &
CGSO=1.99E-10 &
CGBO=0 &
CJ=4.233802E-4 &
PB=0.9899238 &
MJ=0.4495859 &
CJSW=3.025032E 10 &
PBSW=0.1082555 &
MJSW=0.1083613 &
PVTH0=0.0212852 &
PRDSW=-16.1543703 &
PK2=0.0253000 &
WKETA=0.0188655 &
LKETA=0.0204955
```

Appendix B

Calculation for Minimum Noise Figure, NF_{min}

$$NF_{\min} = 1 + 2.4\frac{\gamma}{\alpha}\frac{\omega_o}{\omega_t}$$

$$\alpha = \frac{g_m}{g_{do}}$$

$$g_{do} = \mu n C_{ox}\frac{W}{L}(V_{gs} - V_t)$$

$$\gamma = 2$$

α = ratio of g_m and g_{do}

γ = Body-effect coefficient

Global Positioning System (GPS) LNA

$g_{do} = 0.031424$

$\alpha = 1.00357$

$$\frac{\gamma}{\alpha} = 1.99929$$

$$\frac{\omega_o}{\omega_t} = 0.14137$$

$NF_{min} = 1+2.4(1.99929)(0.14137) = 1.678dB$

Ultra Wideband (UWB) LNA

$g_{do} = 0.01988$

$\alpha = 1.0009$

$$\frac{\gamma}{\alpha} = 1.9982$$

$$\frac{\omega_o}{\omega_t} = 0.22353$$

$NF_{min} = 1+2.4(1.9982)(0.14137) = 2.072dB$

Appendix C

Layout Design Rule Check Result