EFFECTS OF CHANNEL LENGTH VARIATION ON TRANSCONDUCTANCE N-CHANNEL MOSFET

By

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DISSERTATION REPORT

Submitted to the Electrical & Electronics Engineering Programme

in Partial Fulfilment of the Requirements for the Degree

Bachelor of Engineering (Hon.)

Electrical & Electronic Engineering

Universiti Teknologi PETRONAS

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CERTIFICATION OF APPROVAL

Effects of Channel-Length Modulation on Transconductance

N-Channel MOSFET

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A project dissertation submitted to the

Electrical & Electronic Engineering Programme

Universiti Teknologi PETRONAS

in partial fulfillment of the requirement for the

BACHELOR OF ENGINEERING (Hons)

(ELECTRICAL & ELECTRONIC ENGINEERING)

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TRONOH, PERAK

May 2012

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

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ABSTRACT

Improvement in MOSFET size has been done throughout the years since the development of first MOSFET. However, there are some reliability issues regarding the channel-length of MOSFET. There is a need to identify the causes of these issues, in order to help the designer improve MOSFET design further. Thus, in this project, research will be done to study the effect of channel-length variation on MOSFET transconductance property. The background of the project will include problem statement to justify the study, objectives, scope of study, relevance and feasibility study. Literature review of MOSFET will cover aspects such as the effects of channel-length variation, threshold voltages shift and also transconductance. An in depth research will attempt to determine a method suitable to be performed in this project. The methodology for this project will be discussed further.

ACKNOWLEDGMENT

First and foremost, praise to Allah the Almighty for his guidance and giving me strength to finish my Final Year Project in two semesters. I do not think I would make it this far without Him. I believe everything has been planned carefully by Him, as the best of planners is Allah (Quran, 8-30).

My next appreciation is special made for Universiti Teknologi PETRONAS (UTP), my university because willing to accept me as a student for 5 years and giving me such opportunity where I might not get it somewhere else. It is my pleasure to be a student of this university due to the opportunity, exposure to the working life, experience in doing our own projects with such big responsibility and the trust given. I am among the luckiest person among my friends where I can get a lot of knowledge during my internship period as compared to student from other university.

Of course, my Final Year life in UTP would not be so convenient without the guidance of my supervisor, Dr. Zainal Arif Burhanudin. I am so thankful to get him as my supervisor because he is the one who gives us a lot of trust and responsibility doing our works as part of his team. I also want to appoint my appreciation to my colleagues in the team, Jufri Hazlan, Laili Nadia, Asmah and Atiqah. During my hard time doing the project, they are always there for me. They have thought me the values of friendship and teamwork. All knowledge they gave me is so meaningful. Lastly, I want to thank my beloved family and friends for giving me such a big support from the start of my internship up until the end. They were the one who always there beside me and help me out in every way they could in the times of trouble.

NOMENCLATURES

$V_{GS} = Gate\ to\ source\ voltage$

$I_{DS} = Drain\ to\ Source\ Current$

$\mathrm{C_D} = Differential\ Capacitance\ of\ the\ Semiconductor\ Depletion\ Layer$

$\mathrm{C_{it}} = Equivalent\ Capacitance\ for\ the\ Interface\ Traps$

$\mathrm{C_{ox}} = Capacitance\ of\ the\ Oxide\ Layer$

$\mathrm{N_A} = Acceptor\ Concentration$

$\psi_\mathrm{s} = Surface\ Potential$

$\mathrm{V_G} = Gate\ voltage$

$\mathrm{V_{FB}} = Flatband\ voltage$

$\mathrm{t_{ox}} = Thickness\ of\ Oxide\ Layer$

$\varepsilon_\mathrm{s} = Permittivity\ of\ Silicon$

$\varepsilon_\mathrm{ox} = Permittivity\ of\ Silicon\ Oxide\ Layer$

$\mathrm{L_D} = Extrinsic\ Debye\ Length$

$\rho = Resistivity\ of\ a\ Certain\ Material$

$l = Channel - Length$

$R = Resistance$

$A = Area$

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CHAPTER 1

PROJECT BACKGROUND

This chapter will provide a basic review of the background study of this project. It will start with brief introduction to MOSFET, and the major problems associated with scaling MOSFET size. To begin the research, there are some objectives and scope of study that will be referred throughout the project.

1.1 Background study

Over the years, there are improvements done on MOSFET. Most of the improvements are on increasing the performance, while scaling the dimension of the device at the same time. It is a concept that has been introduced and developed by Gordon Moore and Robert Dennard [1] [2]. Both of them are convinced that the components that can be put inside an area can be doubled every two years.

But there are problems when developing small-scale MOSFET. When we arrive at MOSFET with nano-scale channel-length, we encountered problems related to the performance. This is mainly caused by interface trap density.

The two most prominent techniques to extract interface trap density; capacitance-voltage (C-V) method and Deep Level Transient Spectroscopy (DLTS). These methods apply MOS capacitance concept in the evaluation.

There is another technique developed in 1993, which applies the concept of sub-threshold swing. This method is not as popular as the other two methods, eventhough it is claimed to be more accurate than C-V method.

1.2 Problem statement

Eventhough this method is claimed to be more accurate, it is claimed to be only applicable for MOSFETs with channel-length longer than 1µm. In 1993, MOSFET with channel-length of 1µm is considered to be really small. Nowadays, MOSFETs are fabricated in nano-scale. So the method should be considered as obsolete.

1.3 Objectives

Before this method can be officially claimed to be obsolete, we have to confirm using the latest technology. After these 19 years, it is possible that we already have sufficient technology to perform the procedure to the nano-scale MOSFETs.

After the results evaluation phase, we will produce an academic paper to conclude the findings. If we can prove that this method is applicable for channel-length smaller than 1µm, we can publish the update of this method. If we obtain the same results, it is safe for us to claim that this method is obsolete.

1.4 Scope of Study

The scope of the project will cover on data gathering and analysis based on sub-threshold swing and the I-V characteristics of different channel-length MOSFETs.

CHAPTER 2

LITERATURE REVIEW

This chapter will deal with literature research of the effects of channel-length variation on tranconductance of n-channel MOSFETs. We will be discussing the problems in designing MOSFETs and the effects of channel-length variation.

2.1 Architecture of MOSFET

Metal-Oxide Semiconductor Field Effect Transistor (MOSFET) is commonly found on electronics, such as computers, televisions, and mobile phones, to name a few. Basically, MOSFETs are used to convert voltage. [3]

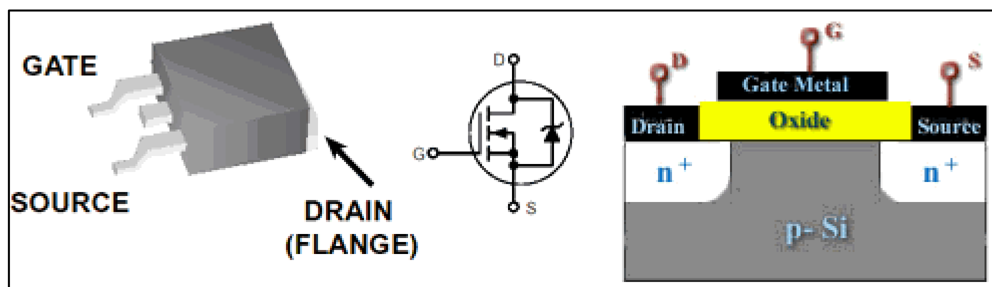

Figure 1: MOSFET architecture [3]

Unlike bipolar transistors which are driven by current, MOSFETs are voltage-controlled power devices.

Since the discovery in 1930s, MOSFETs have gone from several micrometers into tens of nanometers. The trend of minimizing the size occurred because of several reasons:

a) To pack more devices in a given chip area
b) To reduce production cost
c) To improve switching time

In order to maintain the reliability of MOSFETs, minimizations always being done with reference to scaling standards.

2.2 Difficulties Arising Due to MOSFET Size Reduction

However, there are some issues regarding MOSFET channel-length reduction. As the size of MOSFETs fabricated is getting smaller, the reliability of MOSFET has become a serious issue. Mainly, the issues revolve in threshold voltage shift, gate-oxide leakage, junction leakage, transconductance, and heat production, to name a few.

Eventhough MOSFET size reduction is done by scaling the parameters, there are some issues associated with semiconductor device fabrication process; the need to use very low voltages, and with poorer electrical performance necessitating circuit redesign and innovation.

These problems had big impacts to the design of MOSFET. Development of better MOSFET would not be able to be continued if these problems are not overcame. It is important to study the effects

2.3 The Effects of Channel-Length Variation

Throughout the years, there are a lot of researches has been done to study the effects of channel-length variation on small scale MOSFETs. There are a number of finding s have been discovered.

These are some discoveries related to channel-length variation:

a) Hot Channel Injection [4]
b) Negative Bias Temperature Instability (NBTI) [5]
c) Random Telegraph Signal (RTS) [6]
d) Electromigration [7]
e) Introduction of Fluorine in MOSFET [8]
f) Channel-Length Modulation [8]
g) Drain Induced Barrier Lowering (DIBL) [8]
h) Punch Through [8]
i) Velocity Saturation [8]
j) Time Dependent Destructive Breakdown (TDDB) [8]

	What?	**Effects?**
Hot Channel Injection	**-** Particles accelerated by high electric field. - Attain very high kinetic energy. - Injected to the gate dielectric. - Trapped inside oxide layer. - Would cause interface states to be generated.	- V_{th} shift - Transconductance Degradation
Negative Bias Temperature Instability (NBTI)	**-** Increase and decrease in Vth according to the bias. - Caused by increase in temperature.	- V_{th} increase - I_D decrease - Transconductance Degeneration
Random Telegraph Signal (RTS)	- Electric noise that occurs in semiconductors. - Sudden step-like transitions between two or more discrete voltage or current levels.	- Oxide trap generated. - V_{th} shift
Electro-migration	Momentum transfer from the electrons moving into the electric field.	Decrease in semiconductor lifecycle.
Fluorine	A method to improve MOSFET.	Improve device resistance to hot- channel carrier.
Channel Length Modulation	Increase of the depletion layer width at the drain as the drain voltage increased.	- Shorter channel-length. - I_D increase.
Drain Induced Barrier Lowering (DIBL)	- Reduction in Gate Length without properly scaling the other dimensions. - I_D and V_D increase. - V_D controls the inversion layer charge at the drain.	- V_{th} shift. - Gate length reduced
Punch through	Depletion layers between S and D regions merged into a single depletion region.	- Increase in current - I_s and I_D increase
Velocity Saturation	- Smaller devices, higher electric field. - Carriers in the channel have an increase velocity. - No linear relation between the electric field and the velocity at high fields. Velocity saturates reaching the saturation velocity.	- Transconductance degradation - Transit time of carriers through the channel increases.
Time Dependent Destructive Breakdown (TDDB)	- Gate oxide scaled down. - Higher fields in the oxide increase the tunneling of carriers from the channel into the oxide.	Degrade oxide quality

Table 1: Explanation on the effects of channel-length reduction

2.4 Interface Trap Density

One of the most important parameters for estimation of MOS device reliability is the interface trap densityD_{it},. It is difficult to extract D_{it} using conventional methods due to capacitor measurement, as most of them (C-V and DLTS) are based on the capacitor measurement.

There are several types of interface traps exist in a single MOS with the different features and effects to the MOS characteristic [9]. The clarifications of the charges are explained in the following table:

Types	Location	Description
Interface Trap Density and Charges (D_{it}&Q_{it})	Si-SiO_2 interface forbidden band-gap	- Occurs from excess Si (trivalent Si), broken Si-H bonds, excess oxygen, impurities - Bias dependent - Can be extracted - Exist due to interruption of the periodic lattice structure at the crystal surface - Interface have both donor and acceptor character - Not fast enough to respond to high frequency signal
Fixed oxide charges (Q_f)	At or near interface SiO_x	- Immobile under applied electric field
Oxide trapped charges (Q_{ot})	At the Si-SiO_2 , distribute inside oxide layer	- Can be created using x-ray radiation, Hot-Electron Injection
Mobile Ionic Charges (Q_m)	In the SiO_2	- Example charge, sodium ions (Na^+, K^+) - Mobile under NBTI condition

Table 2: Types of interface traps

2.5 Sub-threshold region

The sub-threshold slope is a feature of a MOSFET's current-voltage characteristic. In the sub-threshold region, the I_D behavior is similar to exponentially increasing current of a forward biased diode, though being controlled by the gate terminal. Therefore a plot of logarithmic I_D versus V_G with V_D, V_S fixed will exhibit approximately linear behavior in this MOSFET operating regime. The slope is the sub-threshold slope [10].

It is also called sub-threshold swing.

The sub-threshold region is particularly important for low-voltage, low-power applications, and MOSFETs are used as switches in digital logic and memory applications, because the sub-threshold region describes the degree of ideality, influencing switching speed and power dissipation between on and off states. Therefore, factors determining the sub-threshold slope, such as gate oxide thickness, channel dopant concentration and interface trap density should be optimized sufficiently to satisfy the required on-off current ratio [11].

In 1975, the sub-threshold slope technique was developed for simple estimations of D_{it} in MOSFETs [12], but at that time, it is not applicable to short-channel MOSFETs because various high drain voltage are required to extract D_{it}, thus leading to an increase of surface potential. Besides, only the average interface trap density can be obtained at the surface potential located at near 1.5 times the Fermi potential. However, this technique requires an accurate evaluation of the channel dopant concentration for the calculation of the depletion layer capacitance prior to the extraction of the equivalent capacitance of the interface traps.

2.6 Extraction Methods

There are also researches that intend to find a method for extracting interface trap density on short-channel MOSFETs. Two of the most prominent methods are high-frequency/quasi-static capacitance-voltage (C-V) method and Deep-Level Transient Spectroscopy (DLTS). These methods have been proved to be very accurate and reliable.

2.6.1 C-V method

Capacitance-Voltage (C-V) method is a common method that can be used in various tests, such as I-V characteristics, interface trap density extraction, surface potential, dopant concentration to name a few. It basically performed by applying bias voltage onto MOSFET, and then measuring the values using AC signal.

2.6.2 DLTS

Deep Level Transient Spectroscopy (DLTS) was developed in 1974 by D.V. Lang to investigate energetically "deep" charge trapping levels in semiconductor space charge structures, which may be either P-N junctions or Schottky barriers. It utilizes the fact that the RF capacitance of the sample (usually measured at 1 MHz under reverse bias) depends on the charge state of deep levels in the space charge region **[9]**.

2.6.3 Sub-threshold swing method

There is another method to extract trap density, as proposed by Jong-Son Lyu [12]. This method is also proved to be reliable as to C-V method.

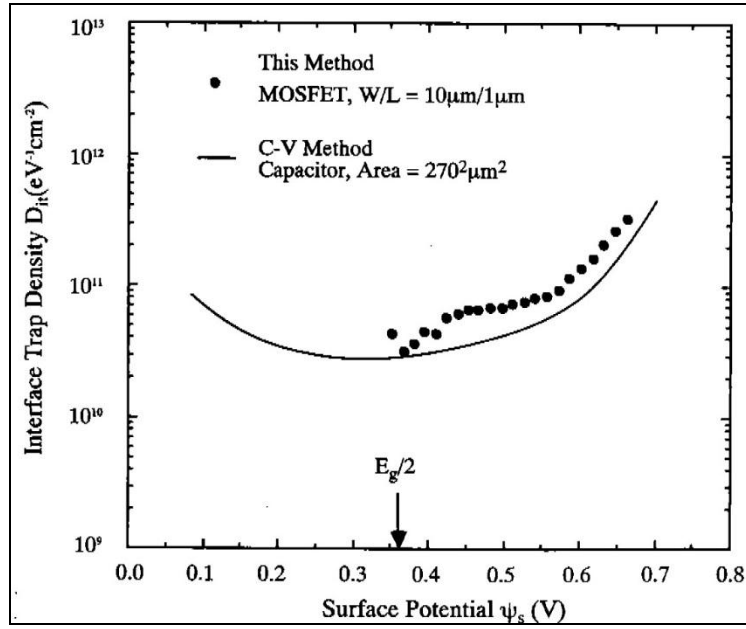

Figure 2: The energy distribution of interface traps in the band gap for the n-MOSFET through the subthreshold slope measurement (.) and that for a capacitor through the C-V method (-)

There is only one setback in this method. It is claimed that the extraction is only possible MOSFET with channel-length at 1.0 microns or larger. MOSFETs with smaller channel-length than 1.0 microns would not exhibit the same outcome. The experimental results comparing different channel-length are provided below.

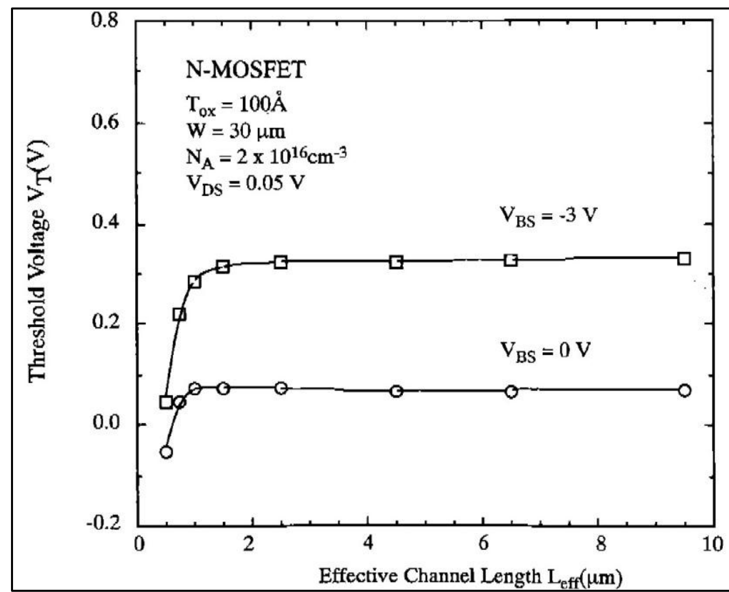

Figure 3: Short-channel effect (threshold voltage shift) of n-MOSFETs.The effective channel dopant concentration is about 2 x 10^{16} cm^{-3}. When the drain voltage is low (<0.1 V), threshold voltage shift is negligible for the channel-lengths larger than 0.8 μm so that the MOSFETs have long-channel behavior. [12]

CHAPTER 3

METHODOLOGY

This chapter will cover the process and flow through the project. Along with the project activities and Gantt chart, and equipment used will also be discussed in this chapter.

3.1 Research Methodology

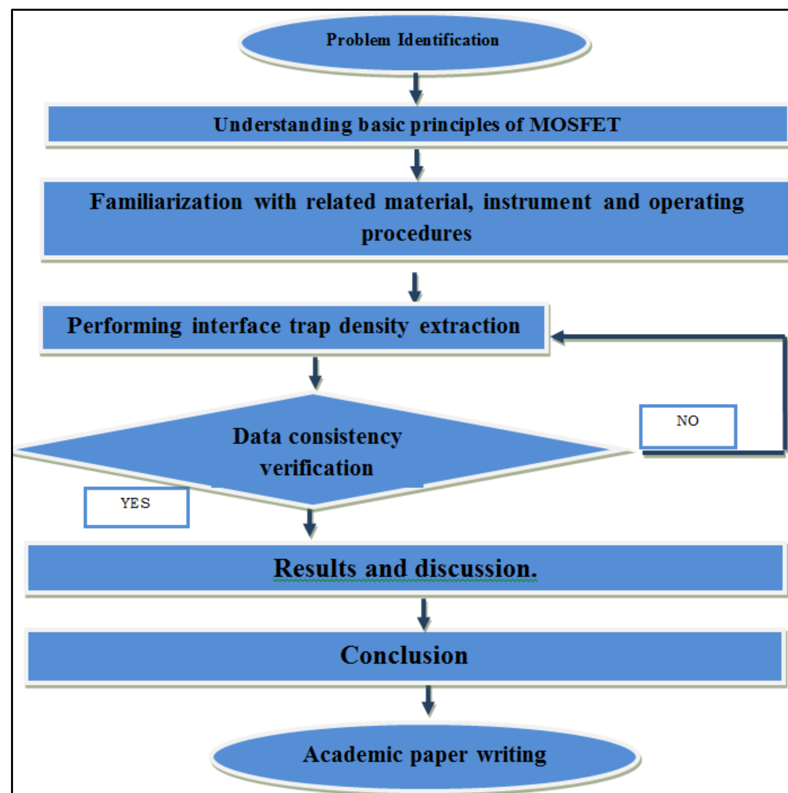

Figure 4: Project Flow Chart

3.1.1 Research on the topic

Since we are dealing with MOSFET channel-length, the basics of MOSFET should be understood first. Subsequently, researches regarding the effects of channel-length reduction of MOSFET will be done. A list to summarize the findings will be established to help finding the common attributes among the effects.

3.1.2 Determine suitable method to induce interface trap density

Once the effects are studied, it is time to move on with the methods to induce interface trap density. There are at least three methods; high-frequency/quasi-static capacitance-voltage (C-V) method and Deep-Level Transient Spectroscopy (DLTS), and the sub-threshold swing method.

As C-V and DLTS methods are well-known, I would like to verify the sub-threshold method using current technology.

3.1.3 Perform literature review and extended proposal

As the method has been agreed upon, we will proceed with the literature review and extended proposal. This will be done by following the guideline provided by UTP.

3.1.4 Performing experiments

The sub-threshold swing method claims to be only applicable to induce trap density for channel length larger than 1 micrometer. We are going to verify this claim by performing the experiments on MOSFETs that have channel-length of 0.4 and 4.0 micrometer. Training prior performing the experiments (equipment and die handling) will be done.

3.1.5 Evaluating experiments result

The results of the experiment will be compared. We will the results based on I-V characteristics of MOSFETs.

3.1.6 Conclusion and academic paper writing

From the evaluations, we will come up with a conclusion and proceed with writing the academic paper to be submitted to a conference.

3.2 Equipment

Since this project will require the student to perform experiments, equipment and tools needed for the experiments are available in a special lab in building 22.

The followings are the equipment and material used in this project.

3.2.1 Probe station

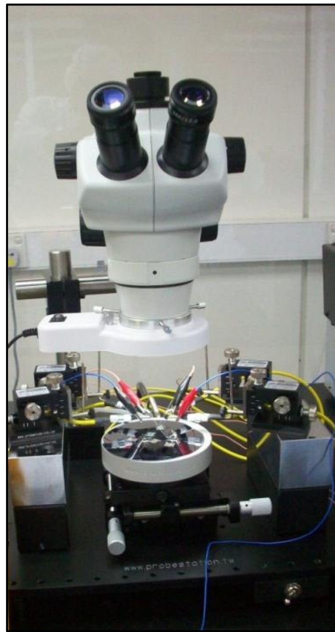

Figure 5: Probe station

Probe station is used to place the sample, and also to determine the exact location to put the probe tip. Microscope is used to guide the user placing the tip.

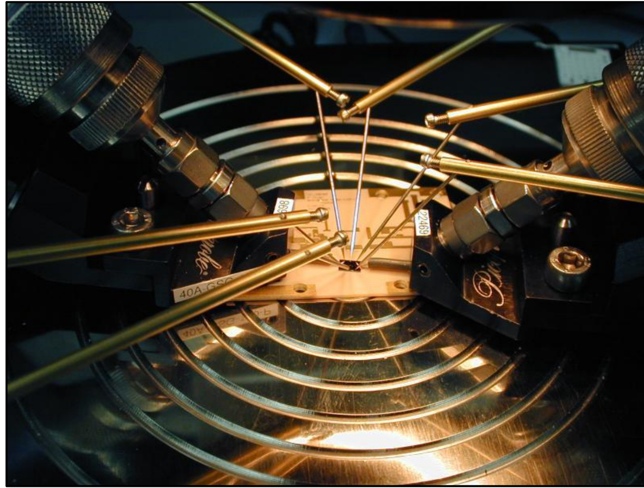

Figure 6: Close up view of the probe tip [11]

3.2.2 Analyzer

Figure 7: Agilent B1500A semiconductor analyzer [12]

This analyzer is used to perform tests on MOSFETs. It is connected to the sample via the probe tip.

3.3 Material

3.3.1 Wafer

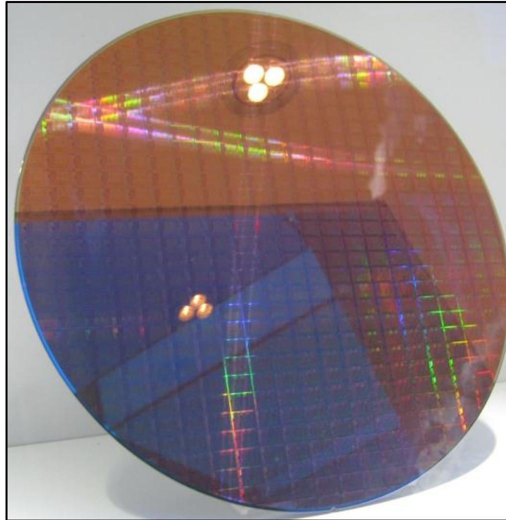

Figure 8: A wafer [13]

Wafer is a small block of semiconducting material, on which a given functional circuit is fabricated. Typically, integrated circuits are produced in large batches on a single wafer of electronic-grade silicon (EGS) or other semiconductor (such as GaAs) through processes such as photolithography. The wafer is cut ("diced") into many pieces, each containing one copy of the circuit. Each of these pieces is called a die. Die is sensitive to light, explaining the absence of photo of actual die used in this report.

3.4 Experiment procedures

1. Prepare everything; equipment and material. As a standard procedure, the analyzer will be turned on for an hour before performing the experiments.
2. Select the desired die to be experimented. Use microscope to determine the exact location of MOSFET.

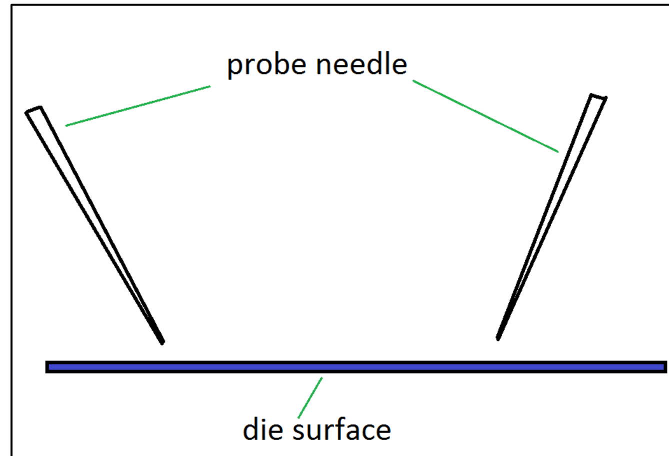

Figure 9: Initial condition

By adjusting the leveler of the probe station, the tip of the probe needle will touch die surface.

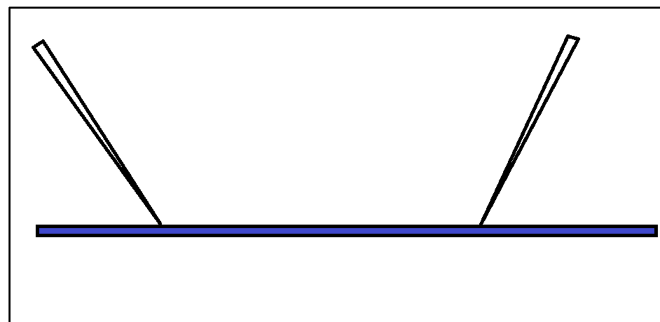

Figure 10: Probe needles touch die surface

To ensure that the needle really touched die surface, we will further adjust the level until the needles moved inward.

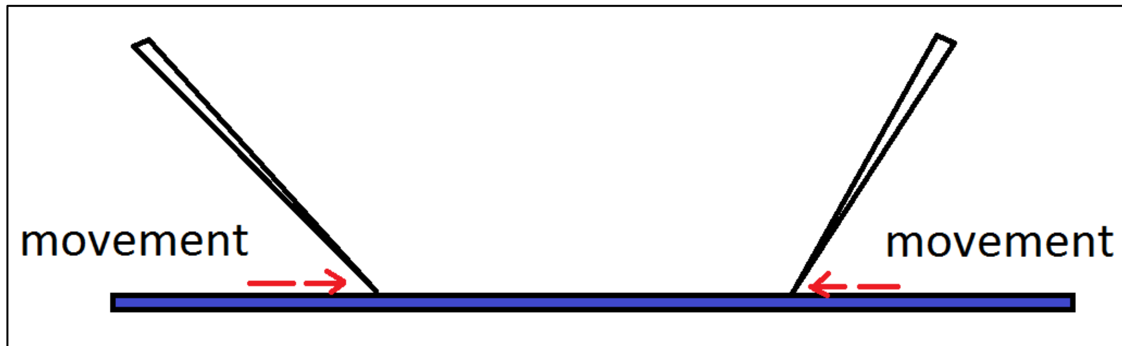

Figure 11: Ensuring the needles really touch die surface

3. Next, we move on with the analyzer. We choose the suitable tests to be performed.

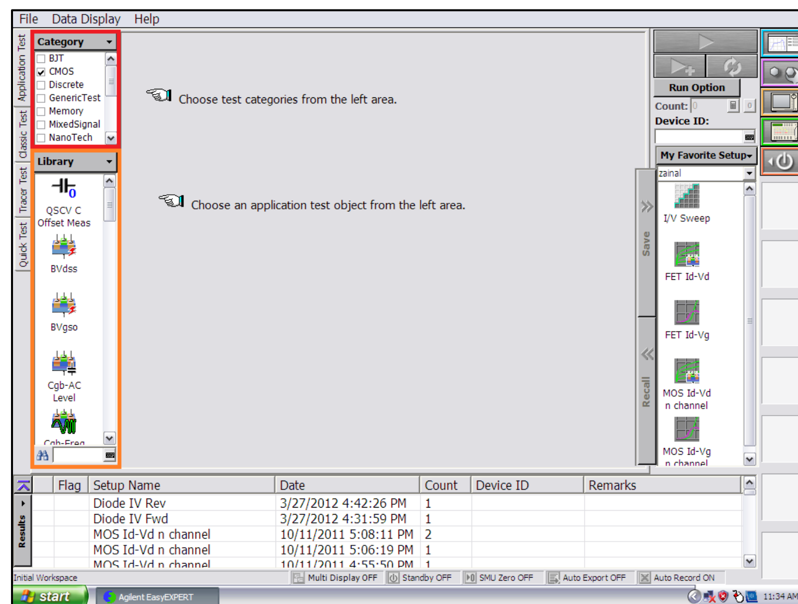

Figure 12: Main interface of the EasyEXPERT

To illustrate in this report, we choose I_d-V_d pulse test as an example. The setup of the experiment will be displayed on the screen. Ensuring all parameters are set, we can start the experiment by touching the start button (indicated with red circle in Figure 14).

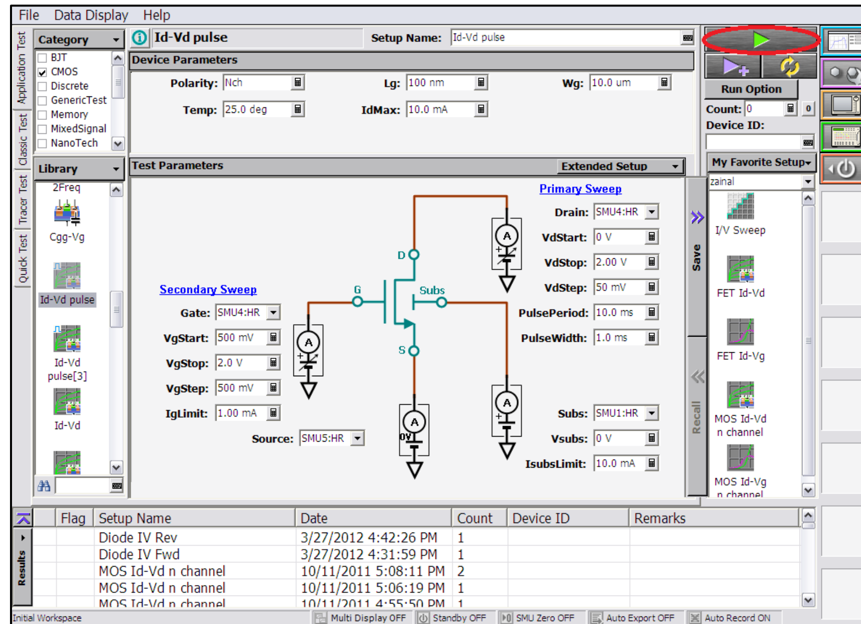

Figure 13: I_d-V_d pulse test interface

4. After several minutes, the experiment is done. Collect data from the analyzer.

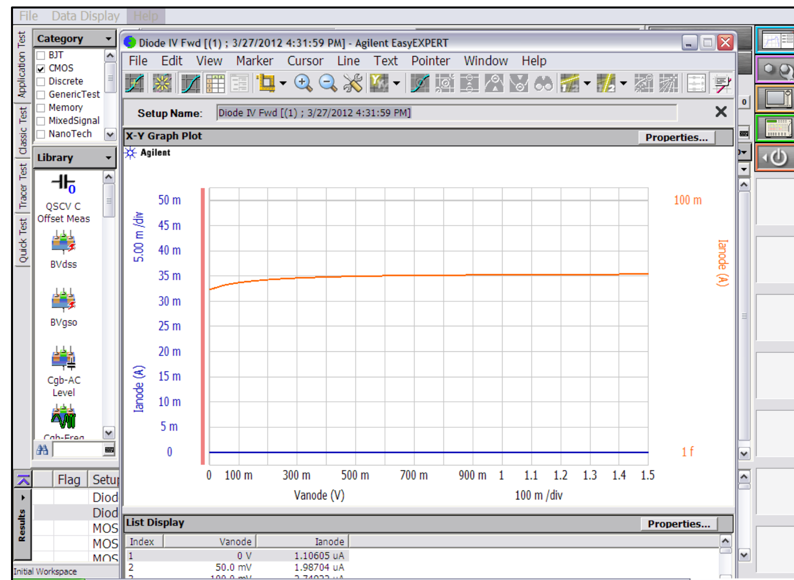

Figure 14: Example of experiment result

5. Repeat experiment for MOSFETs with channel-length 0.4 and 4.0 micrometer. Perform analysis on the results.

CHAPTER 4

RESULTS AND DISCUSSION

4.1 Results

In order to perform the calculation, we need to obtain all the parameters from the sample.

Using the Agilent parameter analyzer, we managed to obtain these values:

Maximum Transconductance, G_{mmax}	
Drain current, I_D	Threshold voltage, V_{TH}

Table 3: Values obtained from Agilent Parameter Analyzer

A batch of devices has 18 n-channel MOSFETs. None of these MOSFETs have similar dimensions. There are differences either in the length or the width of the channel-length. Column 1 and 2 MOSFETs share the same channel-width of 20.6µm, and Column 3 MOSFETs have the same channel-length of 0.24µm.

Column 1	Column 2
4.00 x 20.6	0.20 x 20.6
0.40 x 20.6	0.22 x 20.6
0.38 x 20.6	0.24 x 20.6
0.35 x 20.6	0.26 x 20.6
0.34 x 20.6	0.28 x 20.6
0.32 x 20.6	0.30 x 20.6

Column 3
0.24 x 1.5
0.24 x 1.0
0.24 x 0.8
0.24 x 0.7
0.24 x 0.6
0.24 x 0.5

Table 4: Location and dimension of MOSFET in a batch

In order to get reliable results, the experiments are done using two batches of device (18 n-channel MOSFETs for each batch).

These are the data comparisons between the batches. We arrange the data according to the increment of channel-length.

4.1.1 Threshold voltage, V_{TH}

L x W	Batch 1	Batch 2
0.20 x 20.6	0.5433	0.5772
0.22 x 20.6	0.6027	0.6279
0.24 x 20.6	0.6494	0.6674
0.26 x 20.6	0.685	0.6973
0.28 x 20.6	0.7114	0.7185
0.30 x 20.6	0.7354	0.7396
0.32 x 20.6	0.7476	0.7508
0.34 x 20.6	0.7691	0.7755
0.35 x 20.6	0.7859	0.7822
0.38 x 20.6	0.7992	0.7947
0.40 x 20.6	0.8134	0.8111

Table 5: Measurement of threshold voltage of two batches of devices

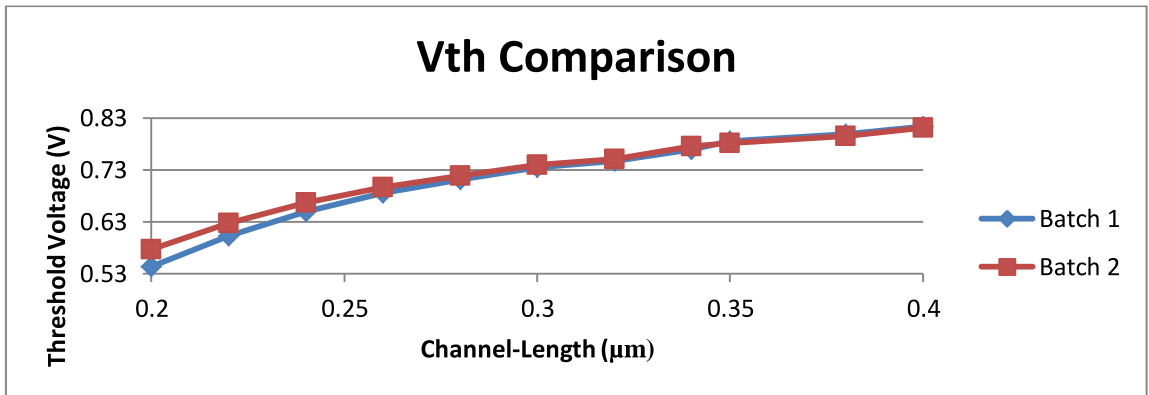

Figure 15: Threshold voltage measurement comparison between two batches

As mentioned beforehand, for a similar channel-width of 20.6µm, we compare the threshold voltage value for different channel-lengths. As the channel-length getting higher, the voltage required for the device to work increase. The tests were done on two batches of MOSFETs with similar dimensions.

4.1.2 Drain current, I_D

L x W	Batch 1	Batch 2
0.20 x 20.6	0.00213	0.00199
0.22 x 20.6	0.00187	0.00175
0.24 x 20.6	0.00164	0.00158
0.26 x 20.6	0.0015	0.0014
0.28 x 20.6	0.00139	0.00135
0.30 x 20.6	0.00131	0.00124
0.32 x 20.6	0.00125	0.00124
0.34 x 20.6	0.00116	0.00112
0.35 x 20.6	0.00112	0.0011
0.38 x 20.6	0.00109	0.00106
0.40 x 20.6	0.00103	0.00099

Table 6: Measurement of drain current of two batches of device

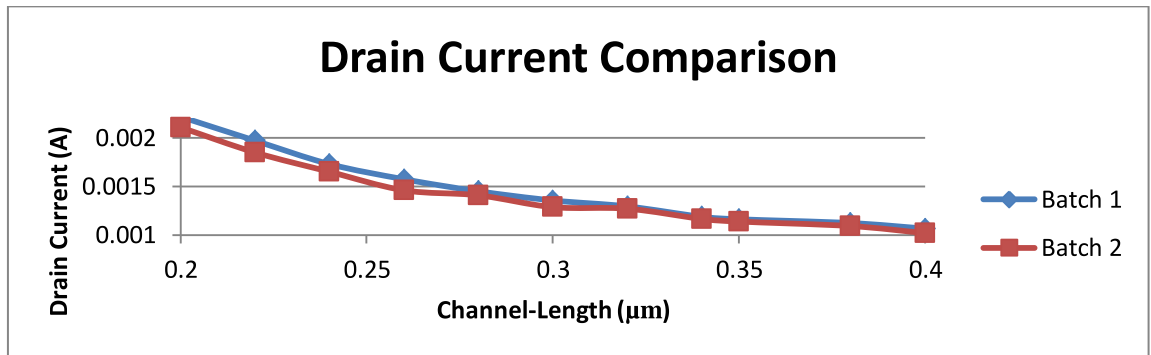

Figure 16: Drain current measurement comparison between two batches

Parallel to previous measurement, for a similar channel-width of 20.6µm, we compare the drain current value for different channel-lengths. As the channel-length getting higher, the current that flow through the drain junction decreased. The tests were done on two batches of MOSFETs with similar dimensions.

4.2 Discussion

The effects occurred are mainly categorized as Short Channel Effects.

To explain the physics behind the increase of drain current as we decrease channel-length, we need to consider the resistance equation:

$$R = \rho \frac{l}{A}$$

$R = \text{Resistance}$

$\rho = \text{Resistivity}$

$l = \text{Channel} - \text{Length}$

$A = \text{Area}$

As resistance is proportional to length, short channel will lead to better conductivity, resulting in higher drain current compared to MOSFET with longer channel-lengths.

As mentioned in the literature review, an effect called Drain-Induced Barrier Lowering (DIBL) occurs to short channel MOSFETs, resulting in lover Vth as the channel-length gets smaller. This happens especially when the reduction in gate length without properly scaling the other dimensions, which problem is quite common as we are developing very small MOSFETs.

When the drain and source junctions of MOSFET getting closer, both of them become electrostatically coupled. This will result in drain bias that would affect the potential barrier to carrier flow at the source junction **[15]**.

The purpose of this project is to validate the method proposed by Jong-Son Lyu in 1993. To evaluate, we examine the standard equation for calculating sub-threshold swing.

$$S = \frac{dV_{GS}}{d(\log I_{DS})}$$

This is equation proposed by Jong-Son Lyu **[10]**.

$$S \approx \frac{kT}{q} \ln 10. \left[1 + \frac{(C_D + C_{it})}{C_{ox}}\right]$$

Where, Cd (differential capacitance of the semiconductor depletion layer) and Cit (equivalent capacitance for the interface traps) are derived from these equations.

$$C_D \approx \left[\frac{q\epsilon_S N_A}{2(\psi_s + |V_{BS}| - \frac{1}{\beta}}\right]^{\frac{1}{2}}$$

$$C_{it} = qD_{it}$$

While ψ_s (surface potential) is derived from this equation.

$$\psi_s = (V_G - V_{FB}) - \frac{\alpha^2}{2\beta}\left\{\left[1 + \frac{4}{\alpha^2}(\beta V_G - \beta V_{FB} - 1)\right]^{\frac{1}{2}} - 1\right\}$$

α and β are constants defined as:

$$\alpha = \frac{\sqrt{2}\varepsilon_s t_{ox}}{\varepsilon_{ox} L_D}$$

$$\beta = \frac{q}{kT}$$

4.3 Challenges

As discussed in section 4.2, there are a number of parameters needed in order to do the evaluation.

We encountered some issues in performing the measurement. The biggest problem is the Agilent parameter analyzer itself. The equipment is capable of doing more measurements, as suggested in the manual, but we have difficulties in setting up the equipment.

Agilent representative also did not offer us much help. So for now, we are still waiting feedback from Agilent.

In order to evaluate the performance of MOSFETs in terms of sub-threshold swing, we need interface trap density parameter. As we have encountered some difficulties in obtaining the parameter, it does severely affect the progress of this project. Until this problem is solved, the evaluation would not take place.

There is also another evaluation in the planning stage, which is to study the effects of Random Telegraph Signal (RTS). Since the preparation of the MOSFETs require high voltage injection, device damage is inevitable. As no more tests could be done on damaged MOSFETs, we rank this test in the last place, hence explains why we could not perform this test yet.

CHAPTER 5

CONCLUSION

There are a number of effects in MOSFET performance that are associated with channel-length. A handful of techniques can be utilized to determine the performance of MOSFET. Most of them show that channel-length is one of the main reasons for all these issues. It is important for MOS device designers to be able to understand and appreciate the effects of channel-length variation on transconductance n-channel MOSFET.

However, certain techniques have its' own limitation. It could be caused by the properties of MOSFET itself, while technology could also play a role in this aspect. As engineers/researchers, we must understand and appreciate these effects in order to develop better MOSFETs in the future.

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