COMPARATIVE STUDY OF MULTIPLE CONTROLLER DESIGN FOR HIGH FREQUENCY CONVERTER

By

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FINAL PROJECT REPORT

Submitted to the Department of Electrical & Electronic Engineering
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Bachelor of Engineering (Hons)
(Electrical & Electronic Engineering)

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CERTIFICATION OF APPROVAL

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A project dissertation submitted to the
Department of Electrical & Electronic Engineering
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Approved:

_____

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TRONOH, PERAK

May 2012

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

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Izzah Khairani binti Suhaimi

ABSTRACT

This paper compares the performance of the high frequency converter with controller circuit and without controller circuit. The comparison is done in term of the output ripple voltage and current, output voltage and current and the body diode conduction loss. The reason to do this research is because at high frequency, the Pulse Width Modulator becomes less efficient and produces higher losses, therefore there is a need to find a new controller. The design is tested using a synchronous rectifier buck converter (SRBC) circuit with a switching frequency of 1 MHz. The design and simulation are done with the aid of PSpice software. At the end of the research, it is found that the Compensator with AGD produces the best result.

ACKNOWLEDGEMENTS

In the name of Allah, the Most Gracious, the Most Merciful. Praise to Him the Almighty that in his will and blessing in giving me the strength and opportunity to accomplish this Final Year project.

My deepest appreciation goes to my supervisor, Dr. Nor Zaihar bin Yahaya for his guidance throughout the project. His wide experience in the field helped to guide me to complete the project. His knowledge and constructive comments helped me to do the project and thesis faster. I could not have gone through the entire project without his help.

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Thank you.

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LIST OF ABBREVIATIONS

AGD	Adaptive Gate Drive
CCM	Continuous Conduction Mode
D	Duty cycle
DBW	Desired Bandwidth
DC	Direct Current
DCM	Discontinuous Conduction Mode
ESR	Equivalent Series Resistance of the output capacitor
$FESR$	Zero frequency
FLC	Double pole frequency
MOSFET	Metal Oxide silicon field effect transistor
PWM	Pulse Width Modulation
SRBC	Synchronous Rectifier Buck Converter
f_s	Switching frequency
I_{L1}	Inductor current
P_{BD}	Body diode conduction losses
T_{BD}	Body diode conduction time
t_D	Dead time
T_f	Fall time
T_r	Rise time
V_{L1}	Inductor voltage
V_{ds}	Drain to source voltage
V_{gs}	Gate to source voltage
V_{pulse}	Pulse voltage source

CHAPTER 1 INTRODUCTION

This chapter discusses the background of research work, the problem statement, the objectives of the project, the challenges faced during this project, the significant of the project, the contribution of the project and the scope of research for this project.

1.1 Background of Research Work

There is one controller to be studied and evaluated for this project which is the compensator-Adaptive Gate Drive (AGD). The controller will be observed for the advantages and disadvantages based on the application of the synchronous rectifier buck converter (SRBC) circuit.

The operation and characteristics of the mentioned controller will be observed and analyzed through the output results. SRBC is chosen because it is widely used in the industry for lower power conversion. The switches in the SRBC are connected to the compensator and the respective gate drive which is the AGD. The performance of the SRBC with the application of the controller will be observed. The switching frequency used is 1 MHz.

1.2 Problem Statement

Previously, SRBC circuits used pulse width modulators (PWM) as the gate drive. However, as the switching frequency increases to MHz range, the PWM method can no longer cater as an efficient gate drive. The change of frequency to a higher range causes higher turn-on and turn-off losses leading to lower efficiency and higher power loss of the gate drivers. The controller circuit to be studied is the compensator-AGD. The study of the controller needs to be conducted thoroughly so that the substantial differences between PWM controlled and the controller could be observed and analyzed.

1.3 Objectives

The objectives of this project are:

1. To understand the concept and theory of controller circuits.
2. To study the differences between controller circuits and how they work.
3. To compare and evaluate the performance of the converter using different controllers.

1.4 Challenges

The main challenge for this project is to implement the controller circuits and find correct value of each parameter used. The proposed design needed to be designed carefully so that the optimum result could be obtained. Time constraint is also one of the challenges to complete this project.

1.5 Significant of Project

The resultant output of the SRBC is observed based on the implementation of the three controller circuits. The results are then analyzed so that the best controller circuit could be obtained from the study. Thus, the implementation of the new controller circuit could increase the efficiency of the SRBC.

1.6 Contribution of Work

The study contributes to the decision of the most suitable control circuit to be implemented to the high frequency converters.

1.7 Scope of Research

In this study, the evaluations for the controller are narrowed down to the average output voltage and current, body diode conduction losses and output ripple peak-to-peak current and voltages of the controller. All the circuit parameters are calculated based on the SRBC conduction mode which is in continuous conduction mode (CCM).

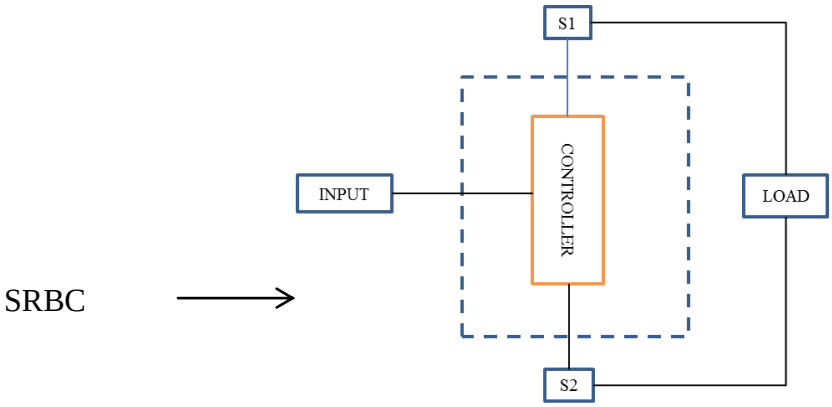

Figure 1: The block diagram of the research

Figure 1 shows the block diagram of the SRBC. This block diagram represents the main focus for the project is which the controller part that will be connected to the switches S_1 and S_2 of the converter. The controller will be evaluated accordingly and the results will be analyzed thoroughly.

CHAPTER 2 LITERATURE REVIEW

Chapter 2 is mainly about the literature review which was conducted to understand the operation of the controller and to gain an insight on the differences between them. The design of the controller is also done based on the literature review conducted in this chapter.

2.1 Pulse Width Modulation (PWM)

Pulse width modulation is a common technique used to control power converters. The technique had been developed for more than 40 years and is applied as the gate driver in converters which is used to drive the MOSFET to the ON or OFF position so that the desired output could be obtained.

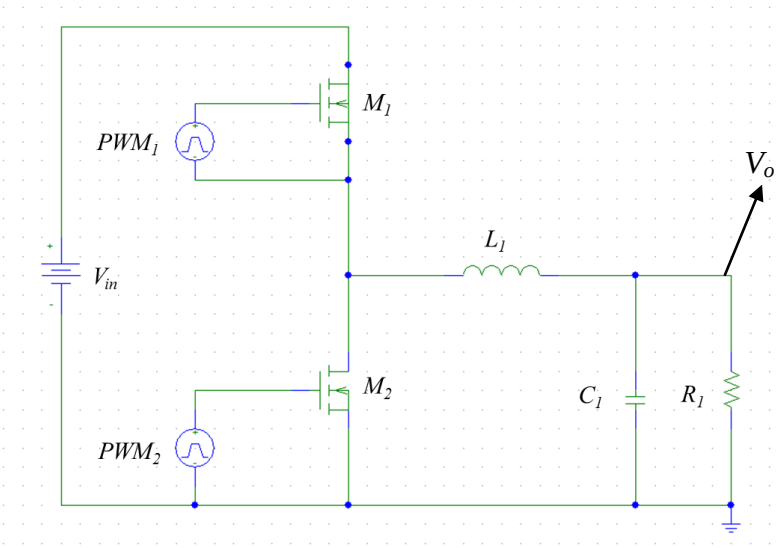

Figure 2: SRBC circuit.

Figure 2 shows the SRBC circuit. The operating principle of the PWM is that the output voltage of the SRBC, V_o is compared with the V_{ref} of the PWM where V_{ref} is the desired voltage to be supplied to the system. When $V_o < V_{ref}$, M_1 at SRBC turns on for inductor charging and when the $V_o > V_{ref}$, M_2 at SRBC turns on for inductor discharging. The duty cycle controls the on-time and the off-time of the transistors to regulate the output voltage, V_o. [1]

There are two types of PWM which is the analog PWM and the digital PWM. The analog PWM uses the triangular waveform to be compared with the V_{ref} while the digital PWM uses the digital representation of V_{ref}.[1]

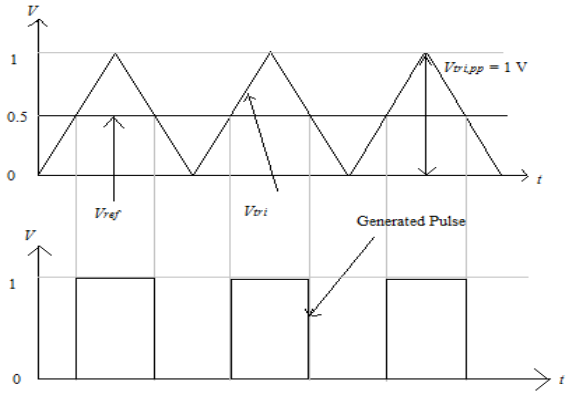

Figure 3: Example of analog PWM signal[2]

Figure 3 shows the example of the generation of the pulse width by comparing the triangular voltage with the $V_{ref.}$ The pulse width can be varied by varying the V_{ref} and the output voltage generated depends on the swing voltage applied to the comparator.

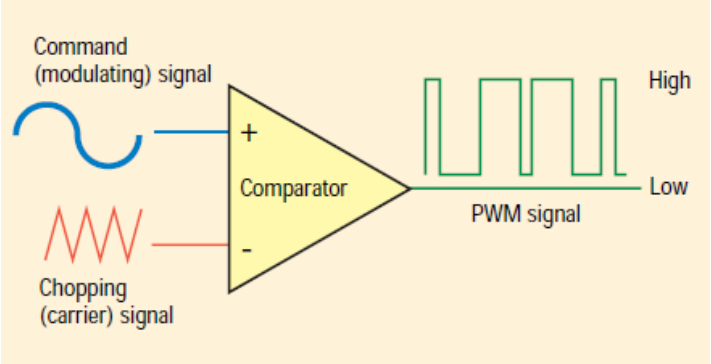

Figure 4: The generation of PWM signal [3].

Figure 4 shows that the PWM signal is generated by comparing the carrier signal with the command signal which is the output voltage from the SRBC at the comparator.

PWM is an accurate system because the signal remains digital from the processor to the controlled system therefore, no analog-to-digital conversion is needed. Thus, the noise effects will be minimized and will not be enough to affect the system. [4,5]

An accurate design of the PWM is required specifically for the gate driver application because the range of the gate voltage must be higher than the threshold voltage to ensure that it turns on with sufficient charge. At high frequency switching, PWM produces high harmonic distortion and noise, thus making the design more complex and less desirable. This is the cause for the study to find the best controller circuit for the high frequency converters.

2.2 Synchronous Rectifier Buck Converter

SRBC is a modified version of the buck converter circuit where the diode, *D*, in the buck converter is replaced with a second switch. By replacing the diode with a second switch, the efficiency of the SRBC is more than the conventional buck converter [4]. Figure 5 and 6 show the conventional buck converter circuit and the SRBC circuit.

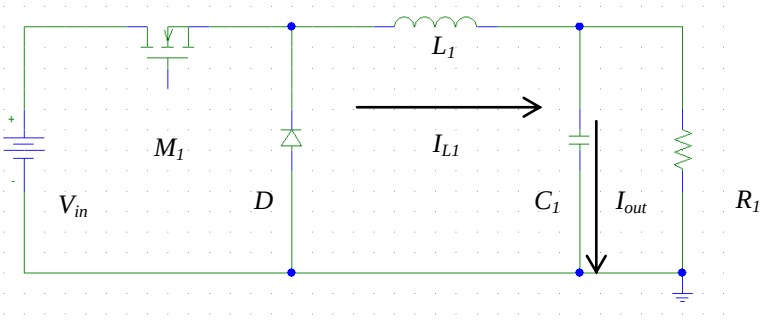

Figure 5: Conventional Buck Converter

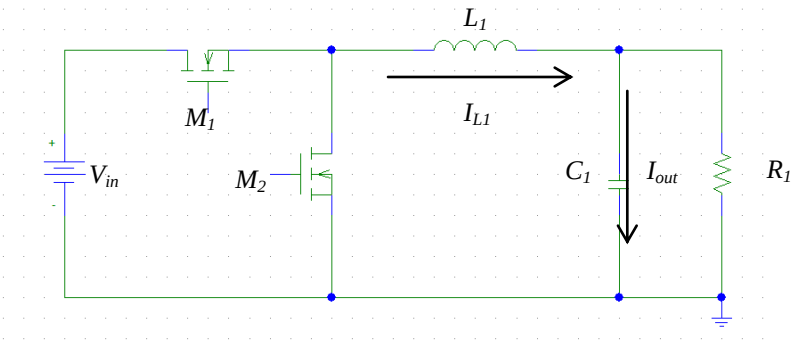

Figure 6: Synchronous Rectifier Buck Converter

Figure 5 and 6 show the conventional buck converter compared with the SRBC. In SRBC, the diode *D* used in buck converter is replaced with a second switch, M_2.

The SRBC is advantageous compared to the buck converter because:

1. It allows bi-directional power flow.
2. Its efficiency is increased due to the less on-state voltage drops of M_2 than forward voltage of diode.

However, by replacing the diode with M_2, there is a chance that the performance of the converter at light load to decrease. Light load is where the converter is operating with small load current. This shows that the SRBC can operate at higher switching frequency but will produce lower performance at low output power. The lower switch usually costs more than the freewheeling diode in the buck converter. The complexity of the converter is also increased by the need for a complementary-output switch driver. [6]

The operation of the SRBC is simple where the inductor is controlled by two switches, M_1 and M_2. The switches alternate the inductor from connecting to the source voltage where the inductor is charging and to the load where it is discharged. The SRBC runs in two conduction modes namely the Continuous Conduction Mode (CCM) and the Discontinuous Conduction Mode (DCM). The CCM is where the current in the energy transfer inductor never goes to zero between the switching cycles while the DCM is where the current through the inductor falls to zero during part of the period. [6]

2.3 Adaptive Gate Drive (AGD)

AGD is a control scheme which was introduced to overcome the limitation in the PWM. It uses a control loop which includes a digital delay line where it senses the drain to source voltage, v_{ds} of the M_2 and adjusts the digital delay line according to the amount of delay that should be applied to turn on M_2. Therefore, M_2 only turns on when the switch node voltage is equal to zero. [7] The AGD control scheme is shown in Figure 7.

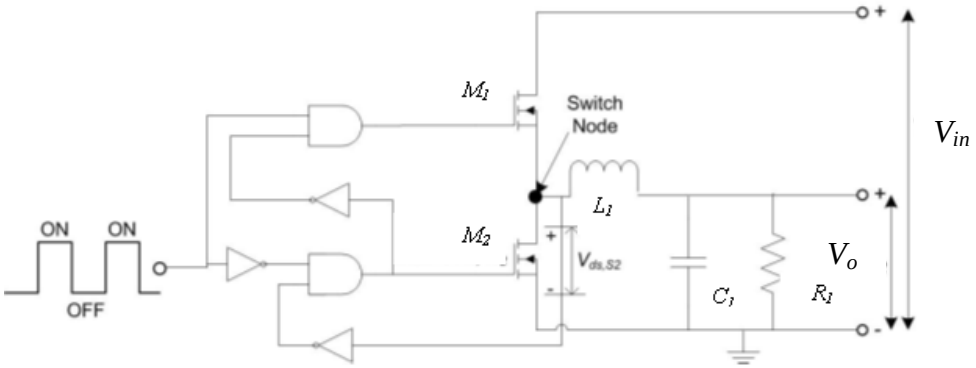

Figure 7: Digital Delay Line for AGD Control Circuit [7]

Figure 7 shows the digital delay line for AGD control circuit. The circuit consists of logic gates which are the NOT, AND and OR. AGD is connected to the switch M_2 of the SRBC. AGD takes the input from the switch node and compares it with the V_{ref} and the output of the AGD will give supply to the switch M_2.

The advantage of AGD is where it can reduce the dead time, T_D, but at the same time not making it too small which may damage the component. The dead time is a time gap where no signal is applied to the MOSFET [7]. AGD can adjust the delay according to the type of MOSFET. However, the disadvantage of AGD is the variation of body diode conduction time due to the logic components that are used as the feedback.

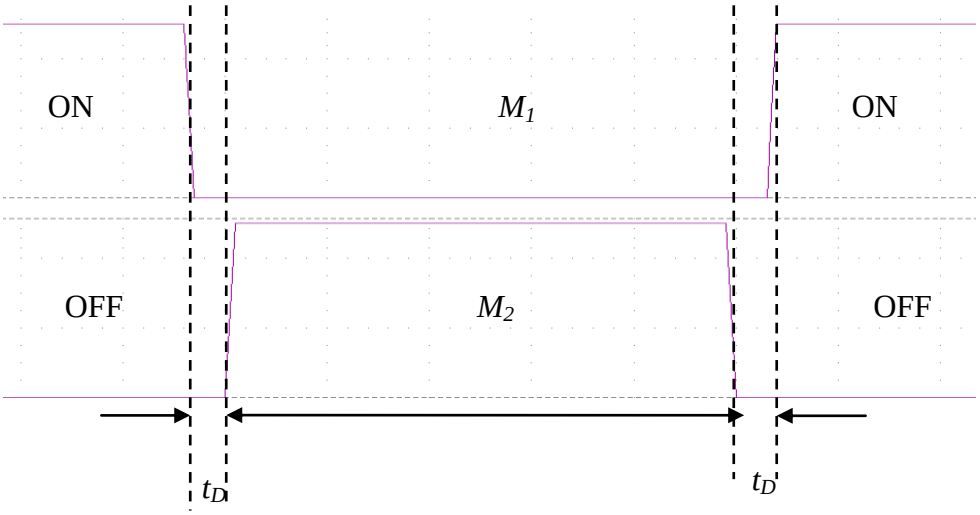

Figure 8: The dead time

Figure 8 shows the dead time where there is no signal applied to the MOSFET.

2.4 Compensator

The compensator is important for a system performance as it functions to control the turn on and turn off M_1 with respect to V_o. The compensator is used to determine the low values of compensation capacitors to stabilize the system. Compensator system has an advantage of the ability to reach high switching frequency, f_s, which can lead to designing high bandwidth loop compensation.

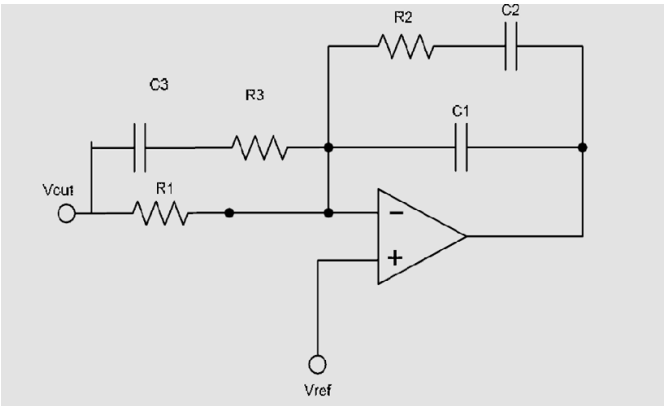

Figure 9: Type III Compensator. [13]

Figure 9 shows the compensator. The compensator consists of a comparator, capacitors and resistors. Type III compensator is applied at M_1 to compensate the high f_s synchronous converter in shaping the profile with gain with respect to the frequency so that two zeros for phase boost of 180º could be utilized. [2,8] The input for the compensator is the output voltage, V_o, from the SRBC which is used to be compared with the V_{ref} for the SRBC.

2.5 Body Diode Loss P_{bd}

The body diode conduction occurs when the switch M_1 is turned on and M_2 is turned off, the energy will be transferred to the load. When T_D is applied, there is a delay between M_1 turn-off and M_2 turn-on. During this delay, the inductor current keeps flowing through the body diode of M_2 due to the inductive load. After T_D ends, M_2 will then turn on. Figure 10 shows the body diode conduction effect. For a higher T_D, the body conduction effect will be longer. This has a degrading effect because it contributes to losses which is known as the body diode losses, P_{bd}.[5]

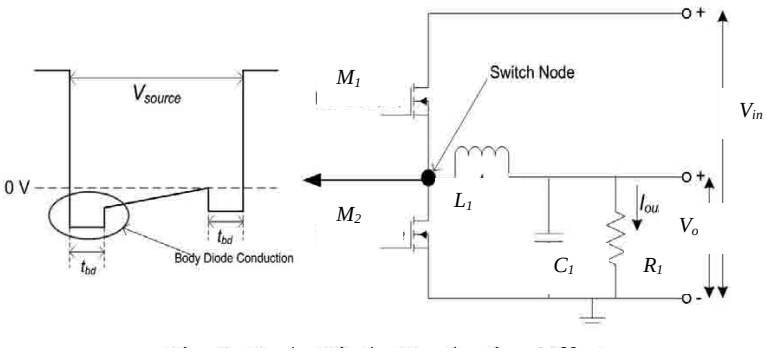

Figure 10: Body diode conduction effect.[5]

The equation for the body diode losses is as stated below. [5]

Body diode loss, P_{bd}

$$P_{bd} = V_f . I_{out} . f_{sw} . [t_{bd}(rise) + t_{bd}(fall)] \quad (1)$$

Assuming that $t_{bd}(rise) = t_{bd}(fall)$,

$$P_{bd} = V_f . I_{out} . f_{sw} . 2t_{bd} \quad (2)$$

where:

V_f=body diode forward voltage drop

I_{out}=output current

f_{sw}=switching frequency

t_{bd}=body diode conduction time

Table 1: The comparison between controllers.

Controllers	**Issues**	**Advantages**
PWM [4,5]	• Requires long dead time, T_D.	• Simple control circuit.
AGD [7]	• T_{bd} cannot be easily predicted. • Complex design.	• Adjustment of delay made adaptively.

Table 1 shows the comparison between the PWM and the AGD. The advantages and disadvantages of each controller are viewed in this table.

CHAPTER 3 METHODOLOGY

This chapter discusses the methodology for this project which starts with the flowchart, followed by the circuit design and schematic for the controller. This chapter also discusses analysis methodology.

3.1 Flowchart

The flowchart for the project is as Figure 1.

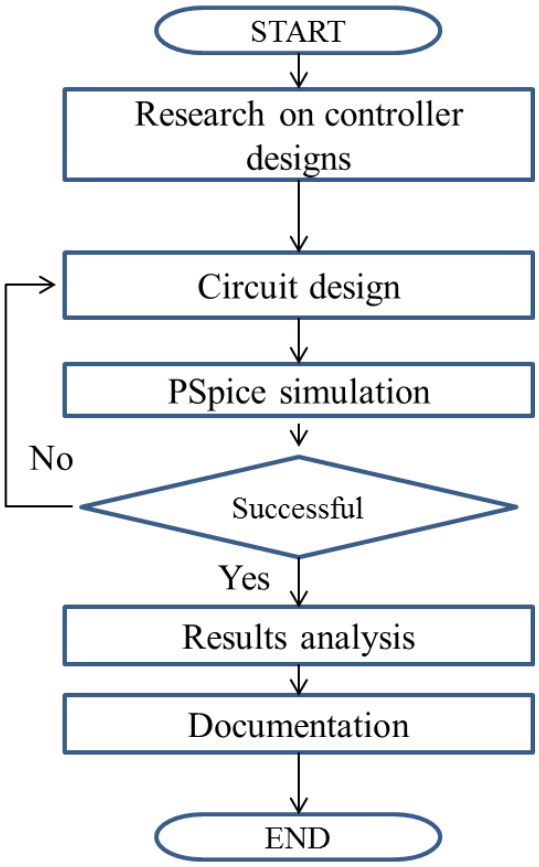

Figure 11: Flowchart of the project

Figure 11 shows the flowchart for this project. Each part is explained below.

3.1.1 Research on Controller Designs

Various controller designs to be used with the high frequency converter were studied by referring to journals and books to understand about the working principle properly. The designs were studied and compared in term of the advantages, disadvantages, functionality and suitability.

3.1.2 Circuit Design

The circuit for each controller circuits was design by calculating the parameters to be used in the simulation. The parameters must be correct to ensure that the results obtained are correct. All of the controllers were designed to be able to cater to the switching frequency of 1 MHz.

3.1.3 PSpice Simulation

After the circuit designing was completed, the circuit was simulated in the PSpice so that the output of the SRBC could be observed and the results could be obtained and analyzed. The simulation could also show that the calculated parameters earlier were correct or needed to be repaired. In case the result is not satisfactory, the process is repeated where the parameters will be calculated again so that the result obtained fulfills the project requirement.

3.1.4 Results Analysis

The results obtained from the simulation will be analyzed to see the average output voltage and current, output ripple voltage and current and to calculate the body diode conduction losses. The result for each controllers will be compared to see which one of the controllers is the best controller to be implemented with high frequency converters.

3.1.5 Documentation

The documentation is where all the research work, methods and outcome of the project is documented. This is so that the progress of the project could be seen and to ensure that it can be a reference for other people.

The whole progress for the whole project is as stated in APPENDIX A and APPENDIX B.

3.2 Software Required

Since this project is simulation based, there are no other tools required. The simulation software used in this project is the PSpice Software. The details of the software are shown in Table 2.

Table 2: Details about PSpice Software

Name	PSpice
Version	9.1
Build	101
Developer	Cadence Design System Inc.

3.3 Circuit Schematics

SRBC and compensator with AGD are used and designed in this project. The related topologies, selection of suitable components, parameters and calculations will be determined.

The circuits that will be designed in this project are:

1. SRBC

2. SRBC with compensator-AGD.

Both circuits will be tested using the switching frequency, f_s, of 1 MHz.

3.3.1 SRBC

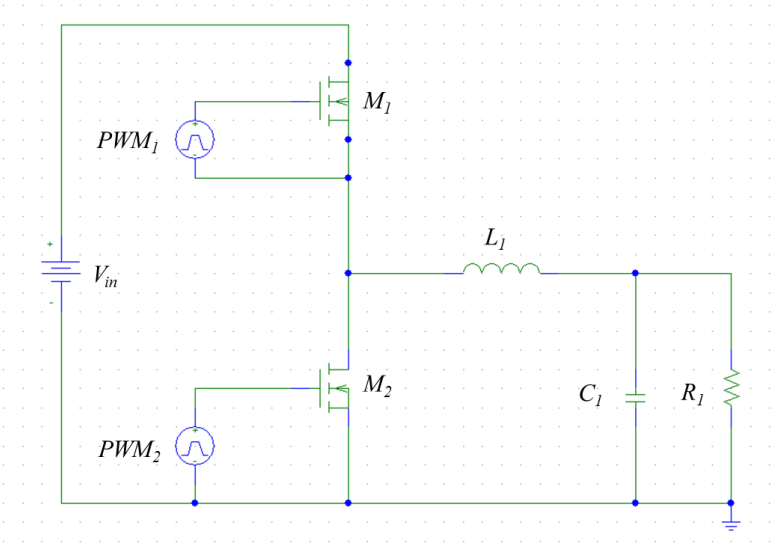

Figure 12: SRBC circuit schematic

Figure 12 shows the schematic of the SRBC used in this project. The value of inductor, capacitor and resistor for this circuit are calculated based on the designed Eq. (3) to Eq. (8) [9-12]. The PWM setting for both M_1 and M_2 are based on Table 3.

Induction voltage, $V_{L1} = L1\frac{di}{dt} = V_{in} - V_o$ (3)

Output Ripple Voltage, $\Delta V_{L1}(t) = \frac{\Delta I_{L1}(t) T_s}{8C_1}$ (4)

Inductor Ripple Current, $\Delta I_{L1}(t) = 8C_1 f_s . \Delta V_{L1}(t)$ (5)

Output Inductor, $L_1 \geq DT_s \frac{V_{in} - V_o}{\Delta I_{L1}(t)}$ (6)

Output Capacitor, $C_1 = \frac{\Delta I_{L1}(t)}{8 f_s . \Delta V_0}$ (7)

Output filter cut-off frequency, $f_c = \frac{1}{2\pi\sqrt{L_1 C_1}}$ (8)

Table 3: Simulation Parameters for SRBC

Components	Parameter Settings in PSPICE simulator and Component used.
PWM_1	V1=0, V2=5V, T_d = 0ns T_r = 5ns, T_f = 5ns, PW = 240ns, PER= 1000ns
PWM_2	V1=0, V2=5V, T_d = 265ns, T_r = 5ns, T_f = 5ns, PW = 710ns, PER= 1000ns
V_{in}	12 V
M_2	IRFP250
M_1	IRFR9212
R_1	1 Ω
L_1	10 µH
C_1	0.375 µF

Table 3 shows the simulation parameters for SRBC for f_s of 1 MHz. These parameters are applied to the simulation in the PSpice software.

3.3.2 SRBC with Compensator-AGD

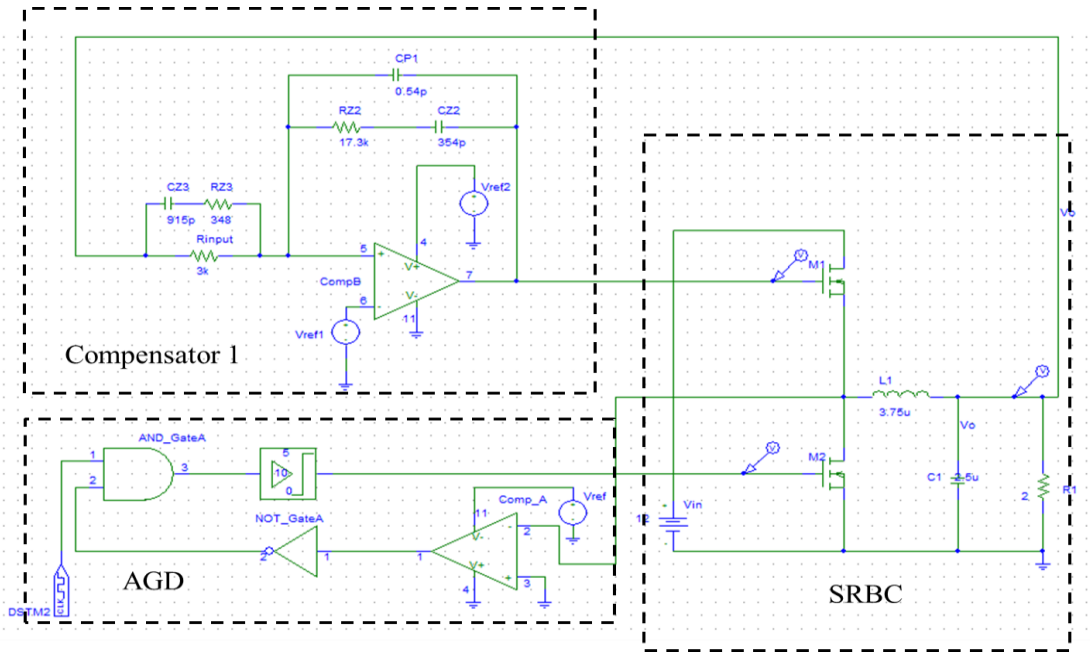

Figure 13: SRBC-Compensator-AGD schematics. [6]

Figure 13 shows the schematics for the SRBC with compensator and AGD. The parameters for the compensator will be determined by the following several guidelines:[13-15]

a) R_{input} value is chosen between 2 kΩ to 5 kΩ. 3 kΩ is chosen for the purpose of this project.

b) A gain, (R_{z2} / R_{input}) is selected. R_{z2} is calculated using equation (9) where the desired bandwidth, *DBW* is 0.3 from f_s.

$$R_{z2} = \frac{DBW}{FLC} R_{input} \quad (9)$$

c) The zero is then positioned at 50% of the output filter double pole frequency, FLC. The parameter C_{z2} is now obtained.

$$C_{z2} = \frac{1}{\pi . R_{z2} . FLC} \quad (10)$$

d) The first pole is placed at the ESR zero frequency, FESR to determine the C_{p1} value.

$$C_{p1} = \frac{1}{(2\pi . R_{z2} . C_{z2} FESR) - 1} \quad (11)$$

e) The second pole at half *fs* and second zero are set at the output filter double pole. Therefore, the value of R_{z3} and C_{z3} could be calculated.[15]

$$R_{z3} = \frac{R_{input}}{\left(\frac{f_{sw}}{2.FLC}\right) - 1} \quad (12)$$

$$C_{z3} = \frac{1}{\pi . R_{z3} f_{sw}} \quad (13)$$

Table 4: Simulation Parameters of SRBC with compensator-AGD. [2]

Components	Parameter Settings in PSPICE simulator and Component used.
C_{z3}	1.93 nF
C_{p1}	1.63 pF
C_{z2}	383.68 pF
R_{z2}	34.62 k Ω
R_{z3}	164.49 Ω
R_{input}	3 kΩ
Comp_A, Comp_B	MAX942CPA/MXM
Not_GateA	7404
And_GateA	7408
V_{ref}	5 V
V_{ref1}	3 V
V_{ref2}	4 V
V_{in}	12 V
M_2	IRFP250
M_1	IRFR9212
R_1	1 Ω
L_1	10 µH
C_1	0.375 µF

Table 4 shows the simulation parameters to be used for the SRBC with Compensator-AGD.

3.4 Analysis

After all simulation has been done and the results are obtained, the results are then analysed to get the output ripple voltage, $V_{op\text{-}p}$, output ripple current, $I_{op\text{-}p}$, average output voltage, $V_{o(avg)}$, average output current, $I_{o(avg)}$, and body diode conduction loss, P_{bd}. The results are then tabulated to see the differences between the controller circuits and to select which is the best controller to be applied to the converters.

3.4.1 Output Ripple Voltage

The output ripple voltage is calculated using Eq. (20)

$$V_{op-p}\ (\%) = \frac{V_{max} - V_{min}}{\frac{V_{max} + V_{min}}{2}} \times 100\% \quad (20)$$

3.4.2 Output Ripple Current

The output ripple current is calculated using Eq. (21)

$$I_{op-p}\ (\%) = \frac{I_{max} - I_{min}}{\frac{I_{max} + I_{min}}{2}} \times 100\% \quad (21)$$

3.4.3 Average Output Voltage

The average output voltage is calculated using Eq. (22)

$$V_{avg} = \frac{V_{max} + V_{min}}{2} \quad (22)$$

3.4.4 Average Output Current

The average output current is calculated using Eq. (23)

$$\mathrm{I}_{avg} = \frac{I_{max} + I_{min}}{2} \quad (23)$$

3.4.5 Body diode conduction loss

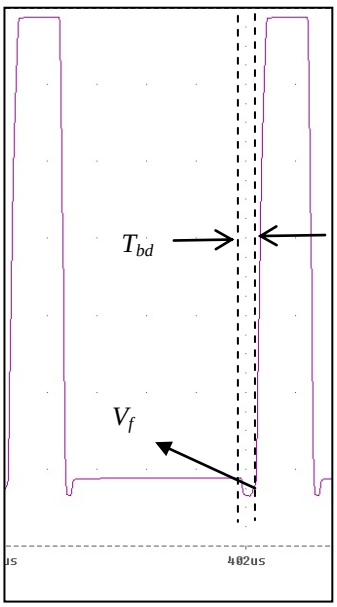

Figure 14: Node Voltage of SRBC.

Figure 16 shows the node voltage for SRBC. The figure shows where the body diode conduction time, T_{bd} is and where the forward voltage, V_f is. The T_{bd} and V_f are important because the values are used to calculate the body diode conduction loss, P_{bd} as seen in Eq. (24).[4]

$$P_{bd} = 2 \times T_{bd} \times V_f \times I_{o(avg)} \times f_s \quad (24)$$

CHAPTER 4 RESULTS AND DISCUSSIONS

This project focuses on the comparative study between multiple controller designs which are to be applied to the high frequency converters. The output circuit used is the SRBC and the controller circuits applied is the AGD. The compensator is attached to the switch M_1 of the SRBC while the controller circuit is applied to the switch M_2.

The graphs that show the output voltage, V_o, output current, I_o and ripple current, I_{ripple} are analyzed to compare the results between the controller and the SRBC without any controller. Here, the controller with the least body diode conduction loss P_{bd} is chosen.

4.1 Circuits Results

4.1.1 SRBC

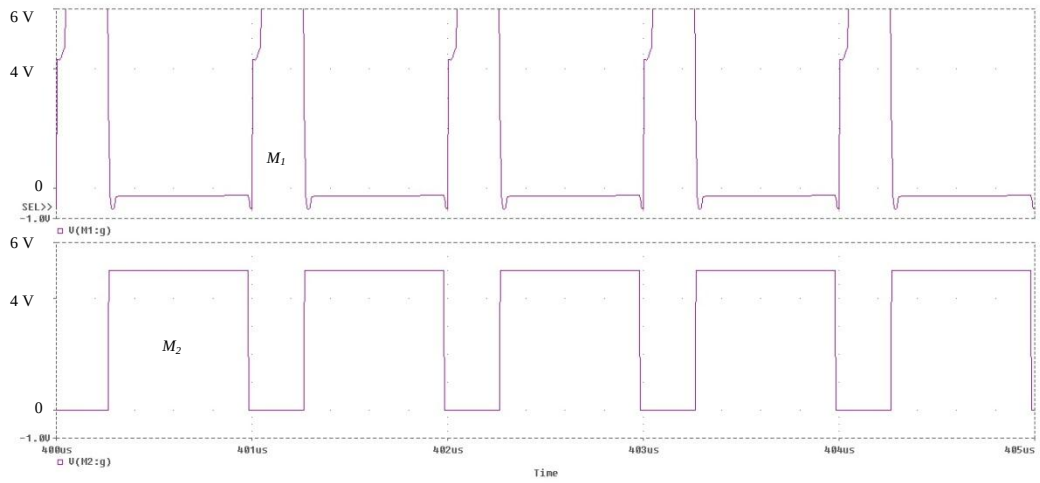

Figure 15: PWM of SRBC

Figure 15 shows the PWM of the SRBC. As can be seen from the figure, the switches M_1 and M_2 turns on alternately to allow the current charging and discharging at the inductor.

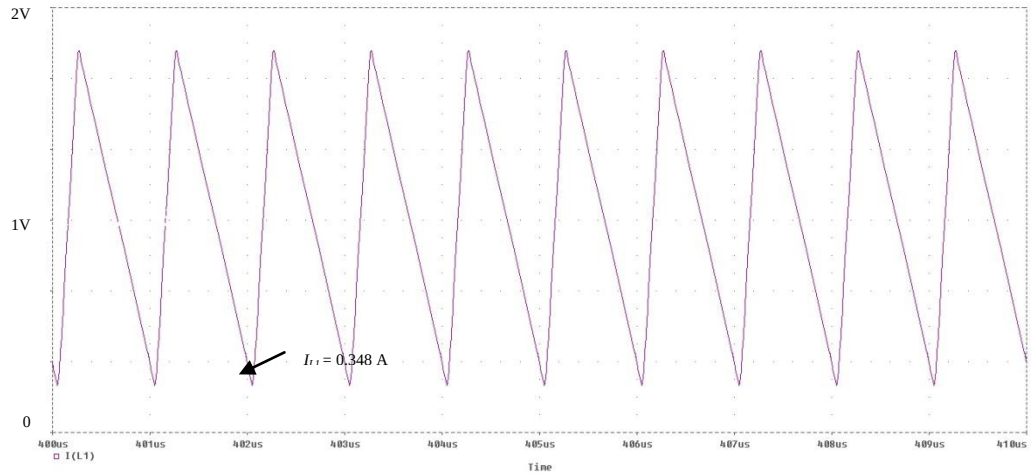

Figure 16: Inductor current for SRBC

Figure 16 shows the inductor current for the SRBC circuit without any controller. During the switching of M_1 to M_2, the current did not go to zero which satisfies the condition that the simulation was done in CCM mode.

4.1.2 SRBC-Compensator-AGD

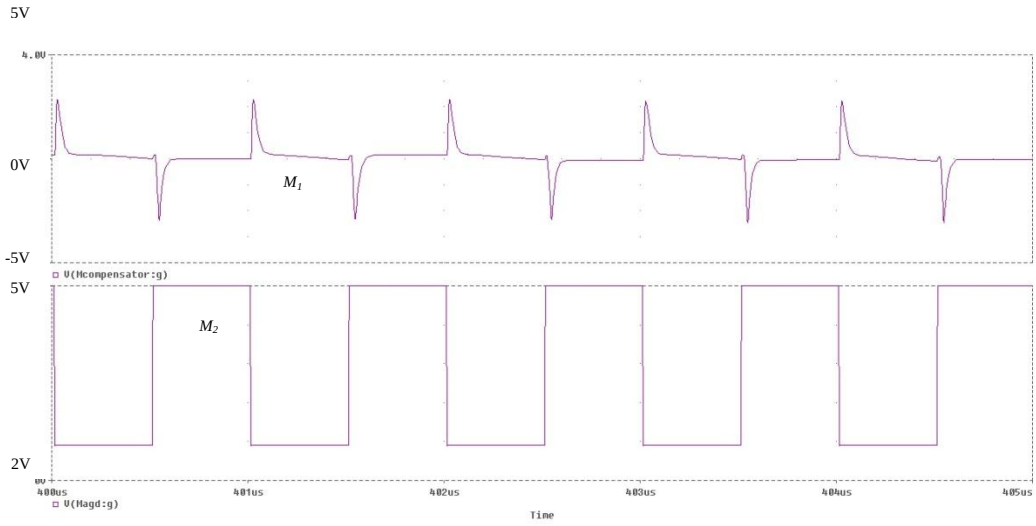

Figure 17: PWM of SRBC-Compensator-AGD

Figure 17 shows the PWM of the SRBC with Compensator and AGD. The switches can be seen to turn on alternately as well for this controller circuit.

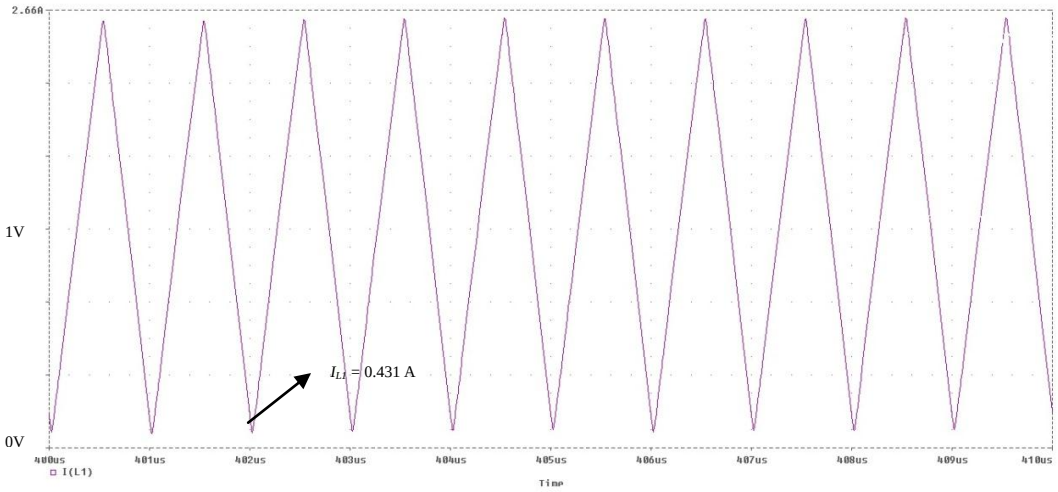

Figure 18: Inductor current for SRBC-Compensator-AGD

The inductor current for the SRBC-Compensator-AGD also did not go to zero during the switching from M_1 to M_2. This corresponds to the CCM mode that the circuit is tested on where the inductor current must not go to zero which can be seen in Figure 18.

4.2 Comparison between controller circuit outputs

The comparison will be done in term of the output voltage and current, output ripple voltage and current, and the node voltage to find the body diode conduction loss.

4.2.1 Output Voltage, (V_o) for SRBC and SRBC-Compensator-AGD

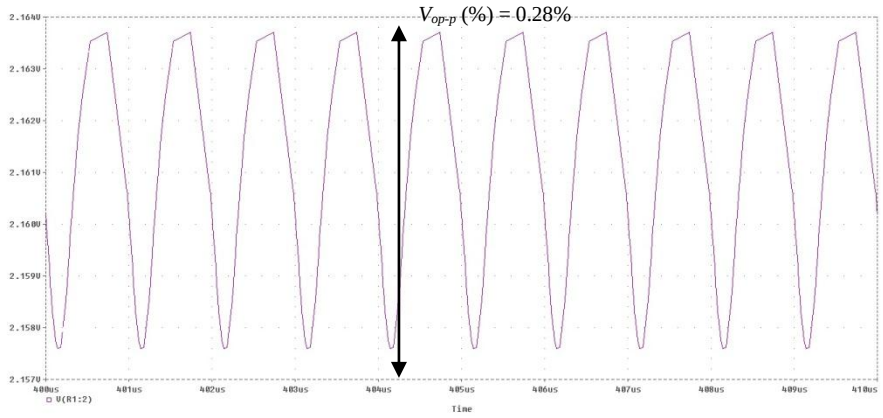

Figure 19: Output Voltage for SRBC

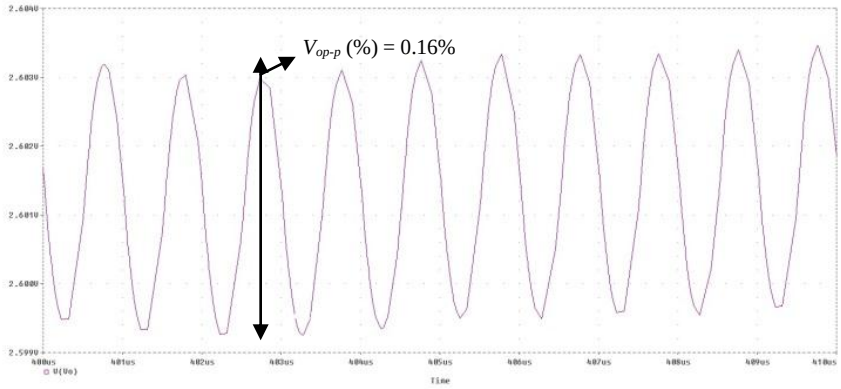

Figure 20: Output Voltage for SRBC-Compensator-AGD

Figure 19 and 20 show the output voltage of multiple controller circuits. Figure 19 shows the output voltage from SRBC while Figure 20 shows the output voltage from SRBC with compensator and AGD controllers. The average output voltage for Figure 19 is 2.16 V. The ripple percentage is 0.28% $= \left(\frac{(\mathbf{2.1637 - 2.1576})}{\left(\frac{\mathbf{2.1637 + 2.1576}}{\mathbf{2}}\right)} \times \mathbf{100}\% \right)$. As for Figure 20, the average output voltage is 2.60 V while the output ripple voltage is 0.16% $= \left(\frac{(\mathbf{2.6035 - 2.5993})}{\left(\frac{\mathbf{2.6035 + 2.5993}}{\mathbf{2}}\right)} \times \mathbf{100}\% \right)$.

4.2.2 Output Current, (I_o) for SRBC and SRBC-Compensator-AGD

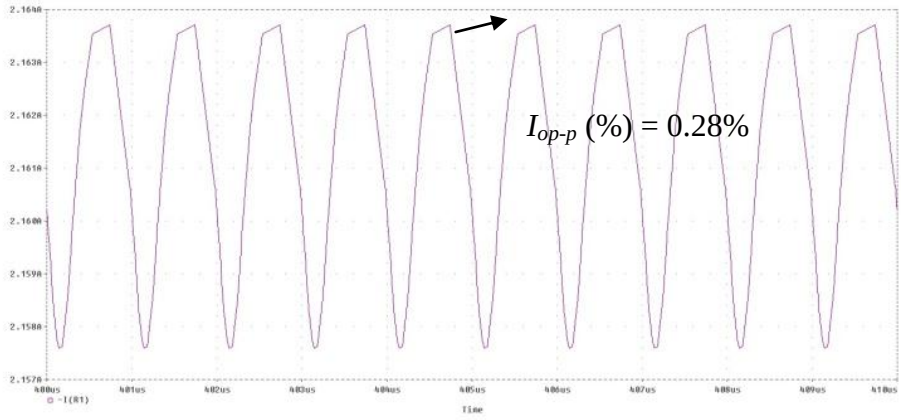

Figure 21: Output Current for SRBC

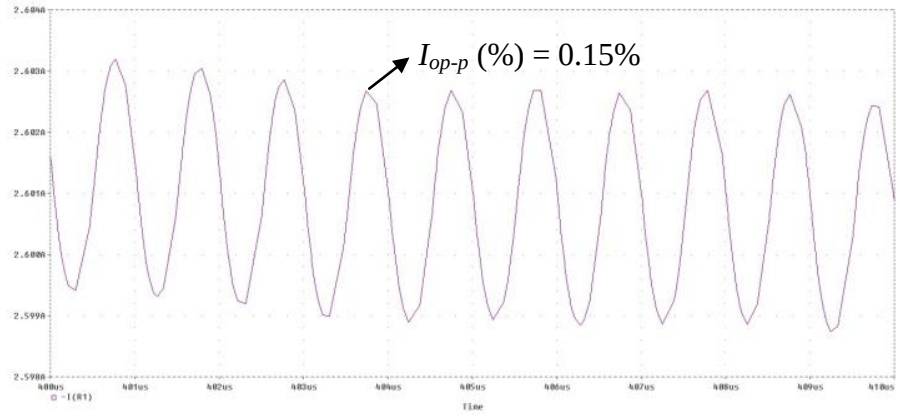

Figure 22: Output current for SRBC-Compensator-AGD

Figure 21 and 22 show the output current from multiple controller circuit and are divided to Figure 21 which is from SRBC and Figure 22 which is from SRBC with compensator and AGD controller circuit. From Figure 21, the average output current is 2.16 A and the percentage ripple current is 0.28% $= \left(\frac{(\mathbf{2.1637-2.1576})}{\left(\frac{\mathbf{2.1637+2.1576}}{\mathbf{2}}\right)} \times \mathbf{100}\% \right)$. From Figure 22, the average output current is 2.60 A and the percentage ripple current is 0.15% $= \left(\frac{(\mathbf{2.6032-2.5993})}{\left(\frac{\mathbf{2.6032+2.5993}}{\mathbf{2}}\right)} \times \mathbf{100}\% \right)$.

4.2.3 Node Voltage, (V_{node}) for SRBC and SRBC-Compensator-AGD

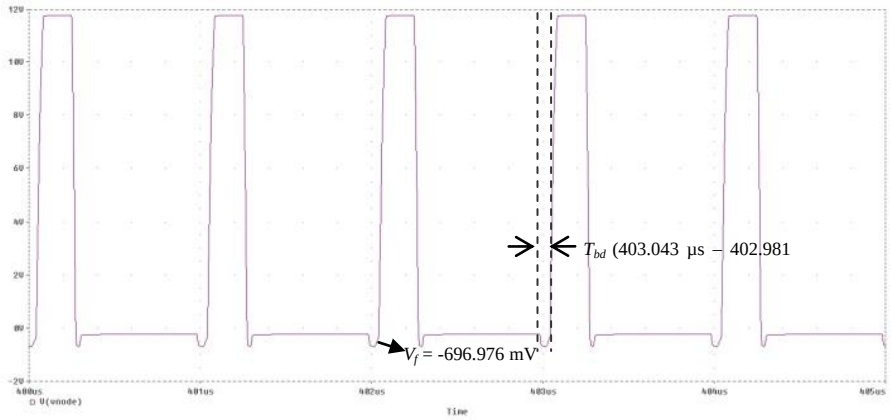

Figure 23: Node Voltage from SRBC

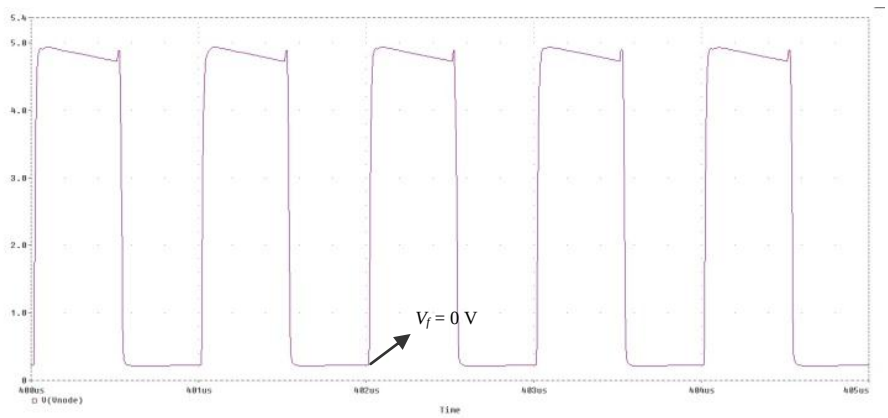

Figure 24: Node voltage from SRBC-Compensator-AGD

Figure 23 shows the node voltage from SRBC where it can be seen that there is a body diode conduction time which is for 69 ns. There is also forward voltage, V_f = -696.976 mV. On the other hand, in Figure 24 which is from the SRBC with compensator and AGD control circuit, no forward voltage is present and therefore there is no body diode conduction time. For Figure 23, the body diode conduction loss, P_{bd} is 207.75 mW. For Figure 24, there is no body diode conduction loss as there is no forward voltage.

4.2.4 Comparison between controller circuits

Table 5: Comparison between SRBC and SRBC-Compensator-AGD circuits.

	SRBC	**SRBC with compensator and AGD**	**Difference**
V_o **(avg) (V)**	2.16	2.60	20.37%
I_o **(avg) (A)**	2.16	2.60	20.37%
$V_{op\text{-}p}$ **(%)**	0.28	0.16	-57.00%
$I_{op\text{-}p}$ **(%)**	0.28	0.15	-53.57%
P_{BD} **(mW)**	207.75	0	-

Table 5 shows the tabulated comparison between multiple controller circuits and conventional SRBC. From the table, it can be seen that the average output voltage and current for SRBC with compensator and AGD improved by 20.37% from SRBC. The output ripple voltage increased by 57% for the SRBC with compensator and AGD compared to the SRBC while the output ripple current increased by 53.57%. The body diode conduction loss for the SRBC with compensator and AGD also increase drastically to no loss at all. Therefore, it can be concluded that the SRBC with compensator and AGD control circuit is better than the conventional SRBC.

CHAPTER 5 CONCLUSIONS

From this project, it can be concluded that the concept and theory of controller circuits were successfully understood and applied. The differences between each controller circuits were also studied and analyzed successfully. The best controller was found to be the Compensator-AGD because it produces less loss and has the highest output voltage and current.

More research could be done to find a more accurate result as the switching sequence was not very accurate during the study for this paper. The current results are still not perfect and could be improved in the future. The research could focus on the switching sequence and also the node voltage to produce a better result.

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APPENDICES

APPENDIX A

GANTT CHART FOR FYP I

No.	Detail/ Week	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1	Selection and Confirmation of Project Title								M							S	
									I							T	
2	Literature review								D							U	
																D	
3	Submission of Preliminary Report								S							Y	
									E							/	
4	Circuit design I (Compensator with AGD)								M							E	
									E							X	
6	Circuit Design II (compensator with PGD)								S							A	
									T							M	
7	Literature review on compensator								E								
									R							W	
8	Circuit Design III (compensator with MPPT)															E	
									B							E	
9	Submission of Interim Draft Report								R							K	
									E								
10	Submission of Interim Final Report								A								
									K								

APPENDIX B

GANTT CHART FOR FYP II

No.	Detail/ Week	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1	Circuit design and testing I (SRBC-Compensator-AGD)								M							S	
									I							T	
2	Circuit design and testing II (SRBC-Compensator-PGD)								D							U	
																D	
3	Circuit design and testing III (SRBC-Compensator-MPPT)								S							Y	
									E							/	
4	Submission of Progress Report								●							E	
									E							X	
6	Analysis								S							A	
									T							M	
7	Submission of Draft Report								E				●				
									R							W	
8	Submission of Technical Paper													●		E	
									B							E	
9	Submission of Final Report								R					●		K	
									E								
10	Submission of Final Report (Hardcover)								A								●
									K								