DESIGN AND ANALYSIS OF SYNCHRONOUS DC-DC CONVERTER

By

IMTIAZ ALI SHAIKH

FINAL PROJECT REPORT

Submitted to the Electrical & Electronics Engineering Programme
in Partial Fulfillment of the Requirements
for the Degree
Bachelor of Engineering (Hons)
(Electrical & Electronics Engineering)

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CERTIFICATION OF APPROVAL

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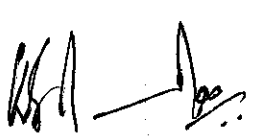

Dr. K.S Rama Rao
Project Supervisor

UNIVERSITI TEKNOLOGI PETRONAS
TRONOH, PERAK

June 2008

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

Imtiaz Ali Shaikh

ABSTRACT

This report presents literature and detailed theory of the synchronous converter. The objective of the project is to *Design and analyze synchronous d.c. to d.c. converter.* Synchronous rectification could be found in two main circuit topologies (i) Forward converters and (ii) flyback converter. The Flyback converter is a d.c. to d.c. converter. The author analyzed both converter types and came up with successful results. Synchronous Conversion is a growing concept; where the main objective is to reduce down power losses during rectification of power. By using synchronous rectifiers we manage to minimize the size of the power supplies used in portable appliances like Laptops and Mobile phones.

In order to design and analyze the circuit some parameters are to be fixed like; operating frequency as 300 KHz, primary voltage for transformer as 15 Vdc, secondary voltage as 3.3 Vdc and the output current as 0.8A. Any Mobile Phone charger is having the same parameters. The author can claim that this would not be the conventional/normal Mobile Phone charger as Synchronous rectification concept is used.

ACKNOWLEDGEMENTS

I would like to express my great attribute to those who guide and helped me in order to achieve my Final Year project at successful end. My enormous gratitude goes to my FYP supervisor Dr. K.S Rama Rao, without him it was not possible to achieve it, Mr. Musa, Miss Yanti, Misses Hawa, and Mr. Yaseen. I am also thankful to those who guide and assist me indirectly. It was really great learning and continuous support from them. I really appreciate their effort they put in to, as to get results.

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LIST OF ABBREVIATIONS

Vds (on) – Saturation Voltage, drain to source

Vgs - Gate Source Voltage

Vth – Threshold Voltage

Id – continuous drain current

Is – Continuous source current

Igss – Gate-to-source current

Rds (on) – Static drain-source ON-State resistance.

UTP – University Technology PETRONAS

CCM – Continuous Conduction Mode

DCM – Discontinuous Conduction Mode

CHAPTER 1
INTRODUCTION

This chapter contains Introduction to the Project, some definitions, background of study, project objective and problem statement. And it also includes the progress made that relates to this part of the chapter.

A DC to DC converter is a circuit which converts a source of direct current (DC) from one voltage to another. It is a class of power converter. DC to DC converters are important in portable electronic devices such as cellular phones and laptop computers, which are supplied with power from batteries. Such electronic devices often contain several sub-circuits with each sub-circuit requiring a unique voltage level different than that supplied by the battery (sometimes higher or lower than the battery voltage, and possibly even negative voltage). Additionally, the battery voltage declines as its stored power is drained.

Owing to rapid development in power electronics, Speed of data processing is continuously being increased and Prevent power consumption from being extreme are great task to handle. The power supply voltages for these circuits are being reduced to 5 to 3.3 volts and even up to 1 volt for some *Portable Electronic Instruments;* this is achieved by using low- output-voltage dc power supplies. With this development we are facing the problem like conduction power loss in rectifiers of the power supply feeding. The rectifier conduction loss is proportional to the product of its forward-voltage drop, *VF*, and the forward conduction current, *IF*. In order to keep progressing we need to have smart enough system to avoid above problem (power loss) efficiently by using like, Synchronous Rectifier. A solution to a dilemma is needed is a rectifier more suitable for high- frequency operation also than any of these above. The rectification can be achieved by using the active devices also like; Bipolar Junction Transistor (BJT) or MOSFET. In order to cause active devices to behave as rectifiers,

the base or gate signal must be synchronized with the ac wave to be rectified. This accounts for the name of process synchronized rectification; the circuitry for accomplishing ac to dc conversion is appropriately called a synchronous rectifier [3].

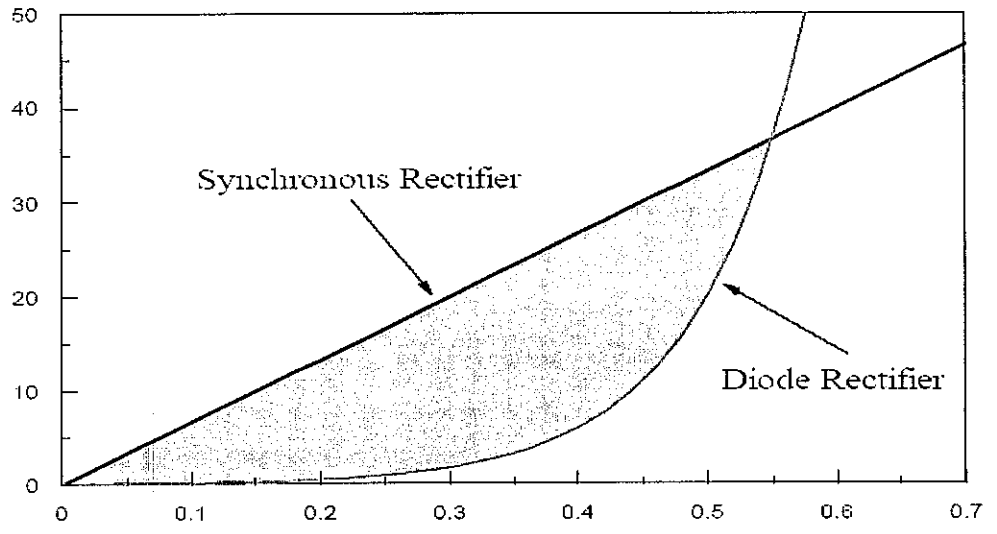


Figure 1: Forward-voltage comparison between synchronous rectifier and diode rectifier. Area has conduction loss saving by using synchronous rectifiers

1.1 Advantages of dc-to-dc Converters

- DC to DC converters offer a method of generating multiple controlled voltages from a single variable battery voltage.

- Saving space instead of using multiple batteries to supply different parts of the device.

1.2 Problem Statement

Step-down (buck) switching converters are integral to modern electronics. They can convert a voltage source (typically 8 V to 25 V) into a lower regulated voltage (typically 0.5 V to 5 V). Step-down converters transfer small packets of energy using a switch, a diode, an inductor and several capacitors. Though substantially larger and noisier than their linear-regulator counterparts, buck converters offer higher efficiency in most cases.

Rapid developments in power electronics, (i) Speed of data processing is continuously being increased and (ii) Prevent power consumption from being extreme are great task to handle. The power supply voltages for these circuits are being reduced to 5 to 3.3 volts and even up to 1 volt for some *Portable Electronic Instruments;* this is achieved by using low- output-voltage dc power supplies. With this development we are facing the problem like conduction power loss in rectifiers of the power supply feeding.

Despite their widespread use, buck-converter designs can pose challenges to both novice and intermediate power-supply designers because almost all of the rules of thumb and some of the calculations governing their design are hard to find. And though some of the calculations are readily available in IC data sheets, even these calculations are occasionally reprinted with errors. Buck-converter manufacturers often specify a typical application circuit to help engineers quickly design a working prototype, which in turn often specifies component values and part numbers. What they rarely provide is a detailed description of how the components are selected. Suppose a customer uses the exact circuit provided. When a critical component becomes obsolete or a cheaper substitute is needed, the customer is usually without a method for selecting an equivalent component.

For this project "Design and analysis of Synchronous DC – DC Converter" author is proposing same technique above specified. With the assistance from *International Rectifiers Company* it is proposed to design the circuit schematic diagram and their values. But just before, to know about circuit components, following design parameters are required.

- **Design Parameters**:
  - Input Voltage = 15 V
  - Output Voltage = 3.3 V
  - Output Current = 0.8 Amp
  - Converter's Switching Frequency = 300 KHz

1.3 Background of study

Electronic switch-mode DC to DC converters are available to convert one DC voltage level to another. These circuits, very similar to a switched mode power supply, generally perform the conversion by applying a DC voltage across an inductor or transformer for a period of time (usually in the 100 kHz to 5 MHz range) which causes current to flow through it and store energy magnetically, then switching this voltage off and causing the stored energy to be transferred to the voltage output in a controlled manner. By adjusting the ratio of on/off time, the output voltage can be regulated even as the current demand changes. This conversion method is more power efficient (often 80 % to 95 %) than linear voltage conversion which must dissipate unwanted power. This efficiency is beneficial to increasing the running time of battery operated devices. A drawback to switching converters is the electronic noise they generate at high frequencies, which must sometimes be filtered.

Isolated DC-DC converters convert a DC input power source to a DC output power while maintaining isolation between the input and the output, generally allowing differences in the input-output ground potentials in the range of hundreds or thousands of volts. They can be an exception to the definition of DC-DC converters in that their output voltage is often (but not always) the same as the input voltage.

A current-output DC-DC converter accepts a DC power input, and produces as its output a constant current, while the output voltage depends on the impedance of the load. The various topologies of the DC to DC converter can generate voltages higher,

lower, higher and lower or negative of the input voltage; their names are Buck ,Boost ,Buck-boost ,Inverting ,Forward, Flyback, Push-pull, Half bridge, Full bridge, Ćuk, SEPIC. The author is using Flyback topology circuit here.

In general, the term "DC to DC converter" almost always refers to one of these switching converters. Switching DC to DC converters are available in a wide variety of input and fixed or adjustable output voltages. DC to DC converters are now available as integrated circuits needing minimal extra components to build a complete converter. DC to DC converters are also available as complete hybrid circuits, ready for use within an electronic device.

1.3.1 Application of Synchronous Rectifier (SR)

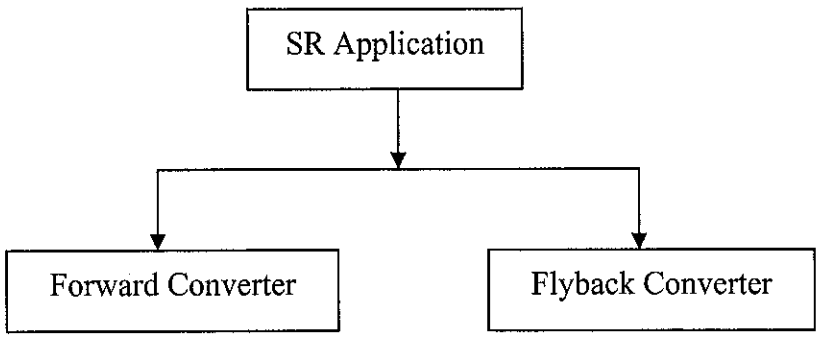


Figure 2: Applications of SR

1.3.2 Driving Strategies

After selecting the application of the synchronous rectifiers i.e. "Flyback converter" the next step is to choose the control strategy of the circuit. This can be achieved by considering two options (1) is by using hardware, by implementing any analog circuit like Pulse Width modulation (PWM) circuit. And it also can be achieved by (2) software implementation; like using C language or Assembly language.

When we use any Microprocessor, C language (software) code is generated and if we want to use any DSP (Digital signal Processing) IC, Assembly Language (software) code is to be generated. After code generation we interface our power circuit with any PC through DSP IC/ microprocessor and then we download the code over circuit. Both strategies are successfully having been used so for. Now the author has proposed other option is to use one of the branded IC (integrated chip) by IOR (International Rectifier).

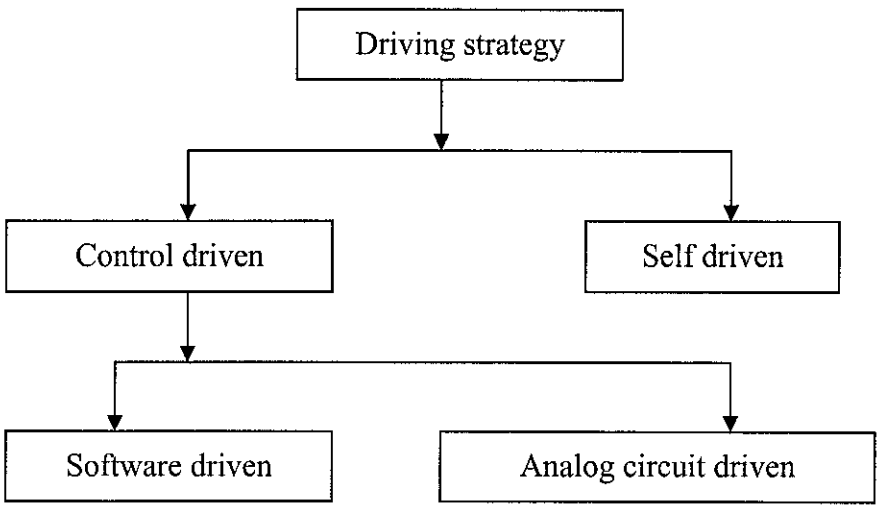


Figure 3: Driving SR

The progress shows the over all working and simulation of Forward converter circuit topology. The circuit topology which author worked over it is "Forward *Converter with Control-Driven Synchronous rectifiers (SR)*" could not satisfy the objectives of project (according to authors knowledge). Its simulation is not workable and circuit brief description was not available (see CHAPTER 4 for simulation results)

so for. Therefore the author proposes to one of the Flyback converter circuit topology that is "Constant-Frequency (CF) Continuous-Conduction-Mode (CCM)". This report also shows the work done for both circuit topologies.

1.4 Synchronous Rectification in Forward Converter

As already discussed about different types of circuit topologies to achieve Synchronous Rectification, the author has worked on *control driven SR* using the *forward Converter* that is "Forward Converter with Control-Driven Synchronous rectifiers (SR)". In a control-driven SR implementation, the SRs are driven by gate-drive signals derived from the gate-drive of the main switch as shown in blow Figure 4. After some minor changes made to actual circuit which was taken from [5] is given blow also in Figure 5. So for the figure 4 seems to be converter, therefore input supply is d.c and output also d.c. In order to work this circuit as a rectifier author changed the circuit some how. The reason was, supply voltage because designing a rectifier must have the a.c. input where as the actual circuit do not have. .

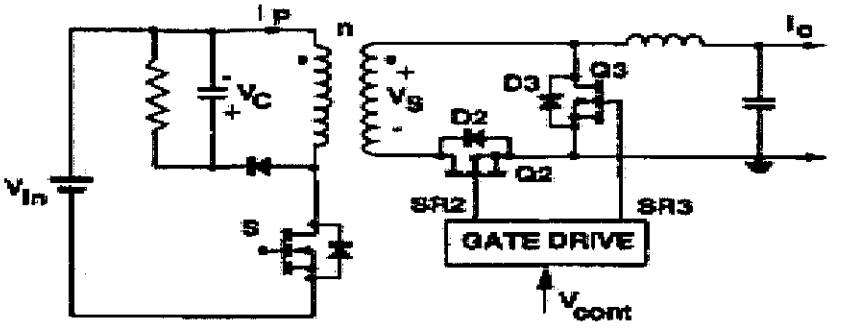


Figure 4: Forward converter with control driven SR

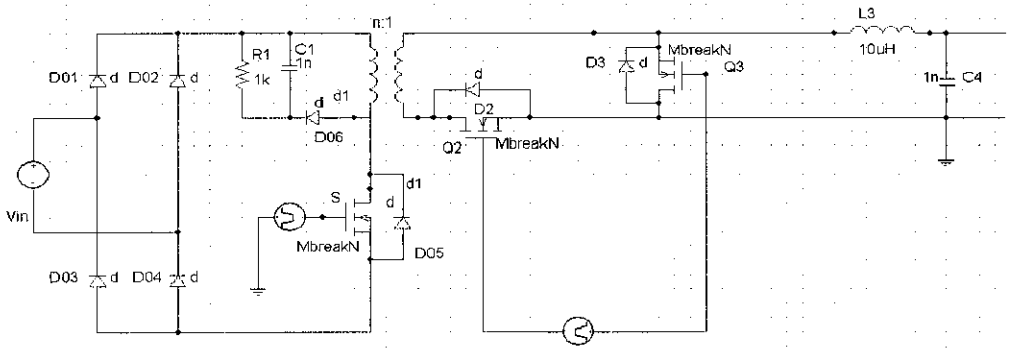


Figure 5: Forward converter with control driven Sr. (After minor change)

1.4.1 How Forward Converter Works

The circuit of Figure 4 operates as the full-wave synchronous rectifier. We know that the MOSFET also provided with an *internal diode*, in order to keep the internal diode from becoming forward-biased in to its conduction region we should have to have low Rd (drain resistance). In this circuit, transistors *Q2* and *Q3* are driven by gate-drive signals derived from the primary-switch gate drive. As a result, the conduction times of the synchronous rectifiers are independent of the transformer-resetting method, but solely depend on the timing of the gatedrive signals. The gate-drive timing of SRs should allow no conduction of the body diodes of the SRs. Now the question appears that, how can we know either the SRs are rectifying or the internal diodes. It is simple to know, the output voltage should be well below 600 mv to ensure that the rectification is not being performed by the internal diodes of the MOSFETS. If this condition can not be meet under worst condition (full-load and maximum operating condition). Or otherwise finally it is needed to select a power MOSFET with lower voltage drop under operating conditions.

- At one time either MOSFETs (Q3,Q2) works or Internal Diodes works (D3,D2)
- MOSFETs works simultaneously, as to rectify synchronously
- By looking at output voltage, that rectification is done through diodes or MOSFETs
- MOSFET Gate signal is given externally

1.5 Synchronous Rectification in Flyback Converter

A number of applications of the SR in the flyback converter have also been reported. However, in all of these applications, the main purpose of the SR was to provide

- Post-regulation of output voltage - The post-regulation of the output voltage and not to maximize the conversion efficiency. Specifically,
- Voltage-controlled resistor - The SR is used as a voltage-controlled resistor in a control loop which adjusts the SRs resistance so that the output voltage is maintained within the regulation range

Generally, the regulation range of these post-regulation approaches is limited to the forward-voltage drop of the SR body diode, i.e., ~ 0.7 V. Moreover, since the voltage drop across the SR is not minimized because of the resistance modulation, the conversion efficiency of these post regulators is reduced, compared to that of the converter with the "true" SR.

1.5.1 How SRs Work in Flyback Converter

A flyback converter with the SR is shown in Figure: 6 taken [2]. For proper operation of the converter, conduction periods of primary switch SW and secondary-side switch SR must not overlap. To avoid the simultaneous conduction of the SW and the SR, a delay between the turnoff instant of switch SW and the turn-on instant of the SR as well as between the turn-on instant of the SW and turn-off instant of the SR must be introduced in the gate-drive waveforms of the switches. With properly designed gate drives, the operation of the circuit shown in Figure 4 is identical to that with a conventional diode rectifier. Namely, during the time switch SW is turned on, energy is stored in the transformer magnetizing inductance and transferred to the output after SW is turned off.

Generally, the circuit sown in Figure 6 can work in Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM) either with a constant or variable switching frequency PWM control. Design considerations and SR loss estimates for various modes of operation and different control approaches are explained in the next chapter [2].

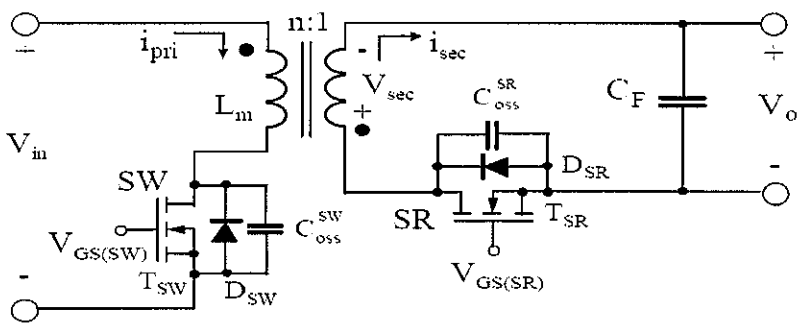


Figure 6: Flyback Converter with SR Example

CHAPTER 2

LITERATUE REVIEW

This chapter includes the literature study made by the author. This section also includes the circuit operation principles and some technical terms. Flyback converters can run over two principles (i) Continuous Conduction Mode (CCM) and (ii) Discontinuous Conduction Mode (DCM). For this project author propose the CCM. In this chapter the author has detailed about the working of a common CCM operation and also about the circuit used for the project.

2.1 Constant-Frequency (CF) Continuous-Conduction-Mode (CCM)

The key waveforms of the flyback converter with the SR operating in CCM are given in Figure 7, [2].

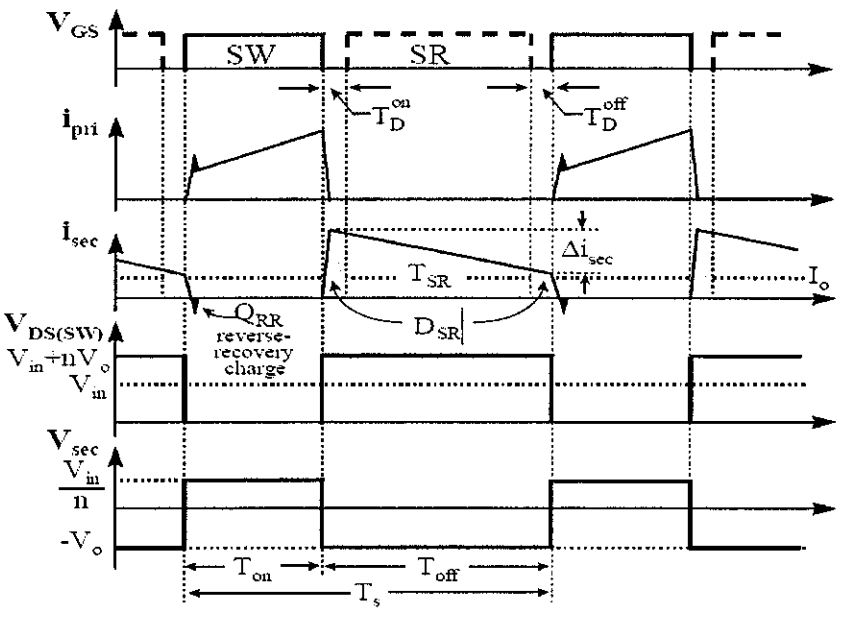


Figure 7: Key waveforms of CF CCM flyback converter with SR.

(Body diode of SR conducts in shaded area)

During delay times $T_{D\ on}$ and $T_{D\ off}$, secondary current i_{sec} flows through the body diode of the SR. From Figure 7; the conduction of body diode *DSR* not only increases the *conduction loss* when primary switch *SW* is turned on. The conduction loss of the SR is given by the sum of the channel-resistance loss and body-diode loss as

$$P_{cond}^{SR} = R_{DS(on)}\left[\frac{I_o^2}{1-D} + \frac{\Delta I_{sec}^2 (1-D)}{12}\right] + V_D I_D (T_D^{on} + T_D^{off}) f_s$$

Where

- *RDS(on)* is the SR on-resistance,
- $D = Ton/Ts$ is the duty-ratio of the primary switch *SW*,
- *Io* is the output current,
- *DIsec* is the secondary peak-to-peak ripple current,
- *VD* and *ID* are the forward voltage drop and current of the body diode, respectively.

But it (conduction of body diode) also introduces a reverse-recovery loss when primary switch *SW* is turned on. The reverse-recovery loss of the SR body diode is given by

$$P_{RR}^{SR} = Q_{RR}(V_o + \frac{V_{in}}{n}) f_s$$

Where

- Q_{RR} is the recovered charge of the SR body diode, and
- $V_o + V_{in}/n$ is the steady-state reverse voltage across the SR.

2.2 CCM operation in Project Circuit:

Refer to figure 8; taken from an application note "Design of secondary side rectification using IR1167 SmartRectifier control IC" [2]. The SmartRectifier Control Technique is based on sensing the voltage across the MOSFET and comparing it with two negative thresholds to determine the turn on and off transition for the device. A higher negative threshold, VTH2, detects current through the body diode and hence, controls the turn on transition for the power device. Similarly, a second externally programmable smaller negative threshold, VTH1, determines the level of the current at which the device turns off. Additional control logic has been incorporated to prevent false turn off and gate chattering when the device current transitions between its body diode and channel.

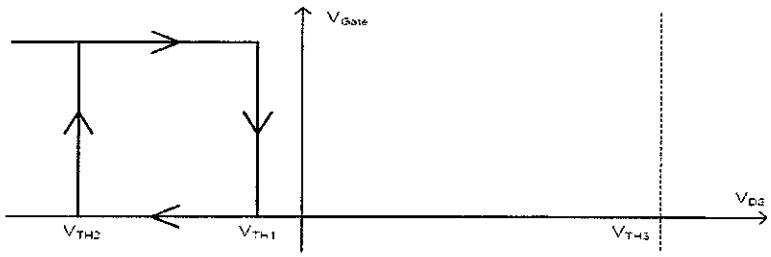


Figure 8: IR1167 SmartRectifier™ control IC differential voltage sensing thresholds

When the power device is turned on, the instantaneous sensed voltage reduces to *RDSon. I* and depending on the level of the device current could fall below the turn off threshold and cause false device turn off. Additionally, the device turn on is also associated with some parasitic ringing between the transformer leakage inductance and device output capacitance.

2.2.1 Operation and analysis in Continuous Conduction Mode (CCM) in Flyback

The IR1167 SmartRectifier™ IC can emulate the operation of diode rectifier by properly driving a Synchronous Rectifier (SR) MOSFET. The rectifier current is sensed by the input comparator using the power MOSFET RDSon as a shunt resistance and the GATE pin of the MOSFET is driven accordingly depending on the level of the sensed voltage with respect to the 3 thresholds shown in Figure 8. Internal blanking

logic is used to prevent spurious transitions and guarantee operation in continuous (CCM), discontinuous (DCM) and critical (CrCM) conduction mode. The modes of operation for a *Flyback circuit differ mainly for the turn-off phase* of the SR switch, while the turn-on phase of the secondary switch (which corresponds to the turn off of the primary side switch) is identical.

2.2.2 Turn On Phase

Refer to Figure 9, taken from an application note [2]. When the conduction phase of the SR FET is initiated, current will start flowing through its body diode, generating a negative Vds voltage across it. The body diode has generally a much higher voltage drop than the one caused by the MOSFET on resistance and therefore will trigger the turn-on threshold VTH2. At that point, the IR1167 will drive the gate of MOSFET on which will in turn cause the conduction voltage Vds to drop down. This drop is usually accompanied by some amount of ringing, that can trigger the input comparator to turn off; hence, an externally programmable Minimum On Time (MOT) blanking period is used that will maintain the power MOSFET on for a minimum amount of time. The programmed MOT will limit also the minimum duty cycle of the SR MOSFET and, as a consequence, the max duty cycle of the primary side switch.

Notice both Minimum On Time and Blanking time logic are allowed only once per switching cycle; it is necessary that Vds reaches VTH3 (therefore primary turn on) for them being enabled again (therefore ready for the next switching cycle).

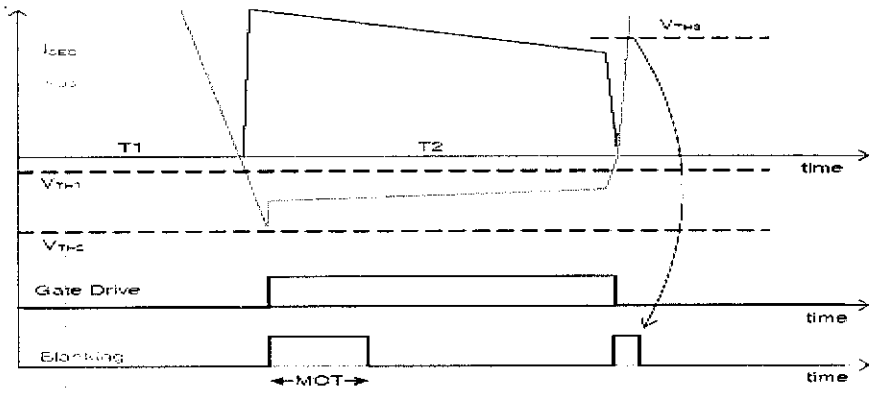


Figure 9: Secondary side CCM operation, MOT and Tblank during operation

2.2.3 CCM Turn Off Phase

Refer to Figure 10, taken from [2]. During the SR FET conduction phase the current will decay linearly, and so will Vds on the SR FET. Once the primary switch will start to turn back on, the SR FET current will rapidly decrease crossing VTH1 and turning the gate off. The turn off speed is more critical here to avoid cross conduction on the primary side and reduce switching losses. The blanking period is also applied in this case, but given the very fast nature of this transition, it will be reset as soon as Vds crosses VTH3 [2].

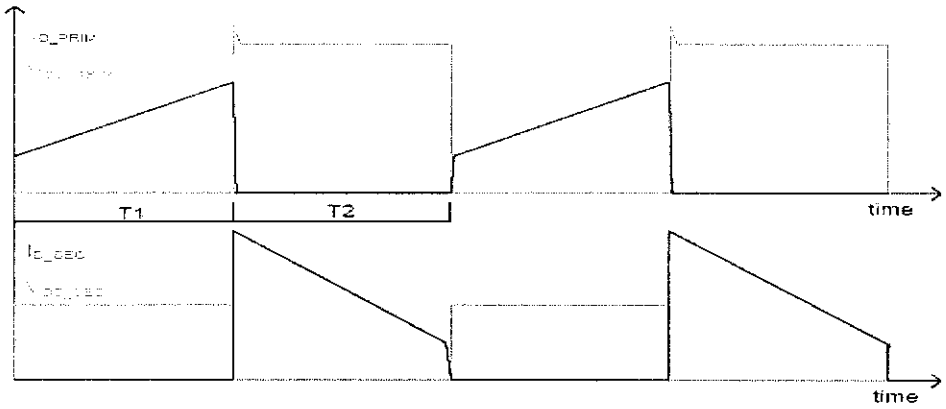


Figure 10: Primary and secondary currents and voltages for CCM

CHAPTER 3

METHODOLOGY

The methodology section is where the objective for this project is to be achieved and realized. Below were the steps taken in order for objectives to realize.

3.1 Design and verification

Research has been done in order to achieve the project objective "Design and analysis d.c. to d.c. synchronous rectifier". The author could review information through many resources as to come to find final working circuit prototype. After research over many circuit topologies finally the Flyback converter topology (Figure 11, [1]) could fulfill the objective. Much information is already discussed and given in this report about the circuit. Circuit parameters are;

- Primary voltage = 15 Vdc
- Secondary Voltage = 3.3 Vdc
- Secondary side current = 0.8 Amp
- Operating frequency = 300 KHz

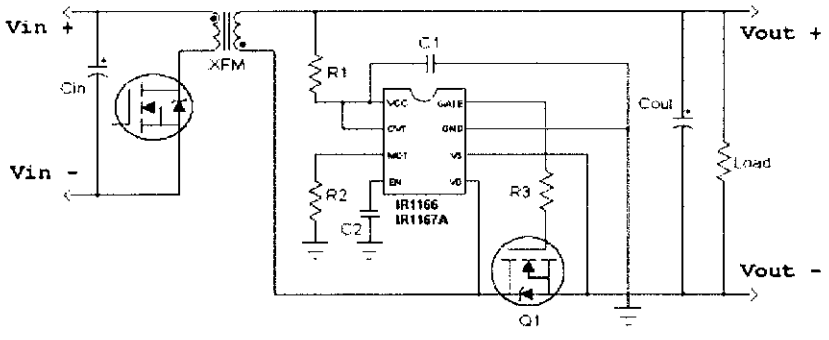
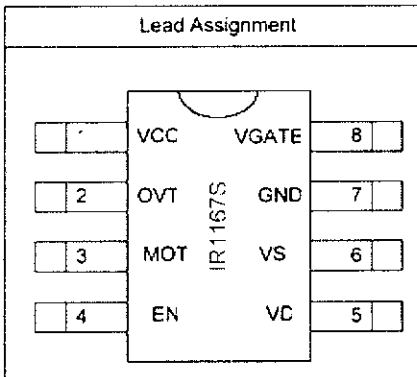


Figure 11: Flyback converter circuit topology

Refer Figure 12 taken from [1]. Below IR1167S is a smart secondary-side driver IC designed to drive N-Channel power MOSFETs used as synchronous rectifiers in isolated Flyback converters. The IC can control one or more paralleled MOSFETs to emulate the behavior of Schottky diode rectifiers [1]. The drain to source voltage of the MOSFET is sensed differentially to;

- Determine the level of the current and
- The device is turned on and off in close proximity of the zero current transition



Pin#	Symbol	Description
1	VCC	Supply Voltage
2	OVT	Offset Voltage Trimming
3	MOT	Minimum On Time
4	EN	Enable
5	VD	FET Drain Sensing
6	VS	FET Source Sensing
7	GND	Ground
8	GATE	Gate Drive Output

Figure 12: IR1167 Smart Rectifier control IC pin assignment

- **Detailed Pin Description**

  - **GND*: Ground***

This is ground potential pin of the integrated control circuit. The internal devices and gate driver are referenced to this point.

  - **MOT*: Minimum On Time***

The MOT programming pin controls the amount of minimum on time. Once V_{TH2} is crossed for the first time, the gate signal will become active then turn on the power FET. Spurious ringing and oscillations can trigger the input comparator off. The MOT blanks the input comparator keeping the FET on for a minimum time.

- **OVT:** ***Offset Voltage Trimming***

The OVT pin will program the amount of input offset voltage for the turn-off threshold V_{TH1}. The pin can be optionally tied to ground, to Vcc or left floating, to select three ranges of input offset trimming. This programming feature allows for accommodating different RDSon MOSFETs.

- **GATE:** ***Gate Drive Output***

This is the gate drive output for the IC. Drive voltage is internally limited and provides 2A peak source and 5A peak sink capability. Although this pin can be directly connected to the direct MOSFET gate, the use of minimal gate resistor is recommended, especially when putting multiple FETs in parallel. Care must be taken in order to keep gate loop as short and as small as possible in order to achieve optimal switching performance.

- **VS:** ***Source Voltage Sense***

VS is the differential sense pin for the power MOSFET source. This pin must not be connected directly to the power ground pin (7) but must be used to creat a Kelvin contact as close as possible to the power MOSFET source pin.

- **VD:** ***Drain Voltage Sense***

VD is the voltage sense pin for the power MOSFET Drain. This is a high voltage pin and particularly care must be taken in properly routing the connection to the power MOSFET drain. Additionally filtering and or current limiting on this pin os not recommended as it would limit switching performance of the IC.

- **VCC:** ***Power Supply***

This is the supply voltage pin of the IC and it is monitored by the under voltage lockout circuit. It is possible to turn off the IC by pulling this pin below the minimum turn off threshold voltage, without damage to the IC. The prevent noise problems, a bypass ceramic capacitor connected to Vcc and GND should be placed as close as possible to the IR1167S. This pin is internally clamped.

- **EN:** ***Enable***

This pin is used to activate the IC "sleep" mode by pulling the voltage level below 2.5V (typ). In sleep mode the IC will consume a minimum amount of current. However all switching functions will be disabled and the gate will be inactive.

3.1.1 Research and Analysis

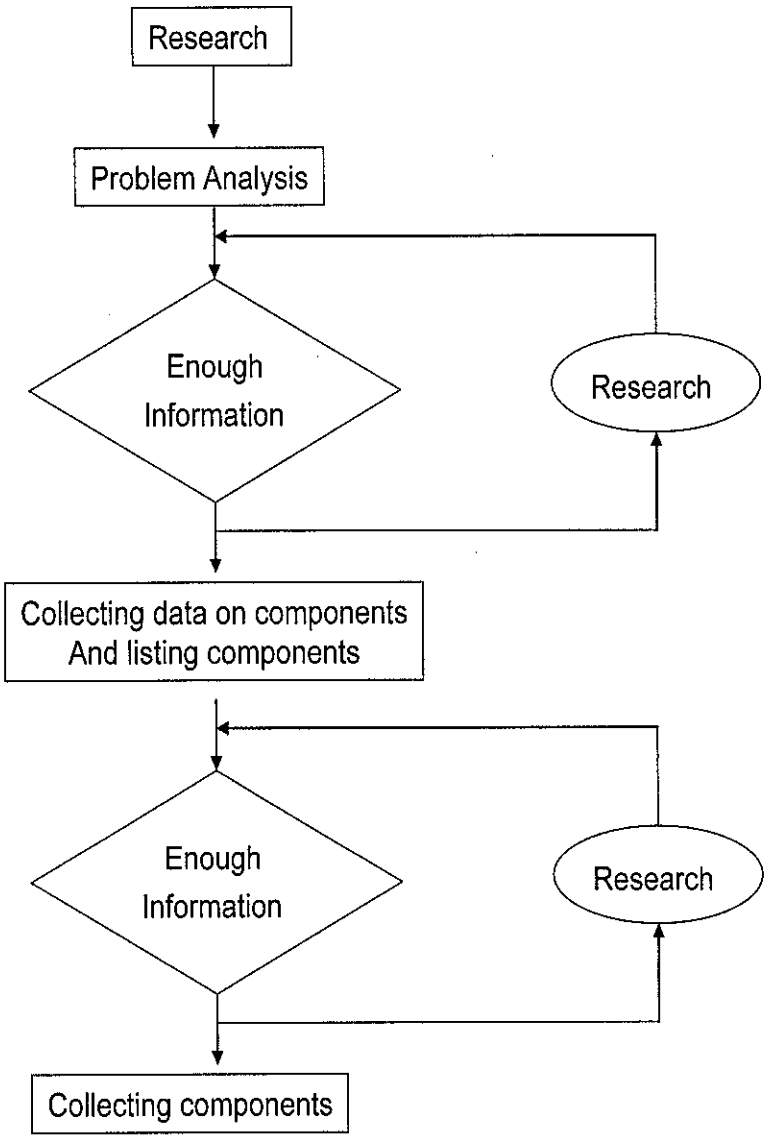


Figure 13: Flow chart of the Research and Analysis

3.1.2 Circuit development

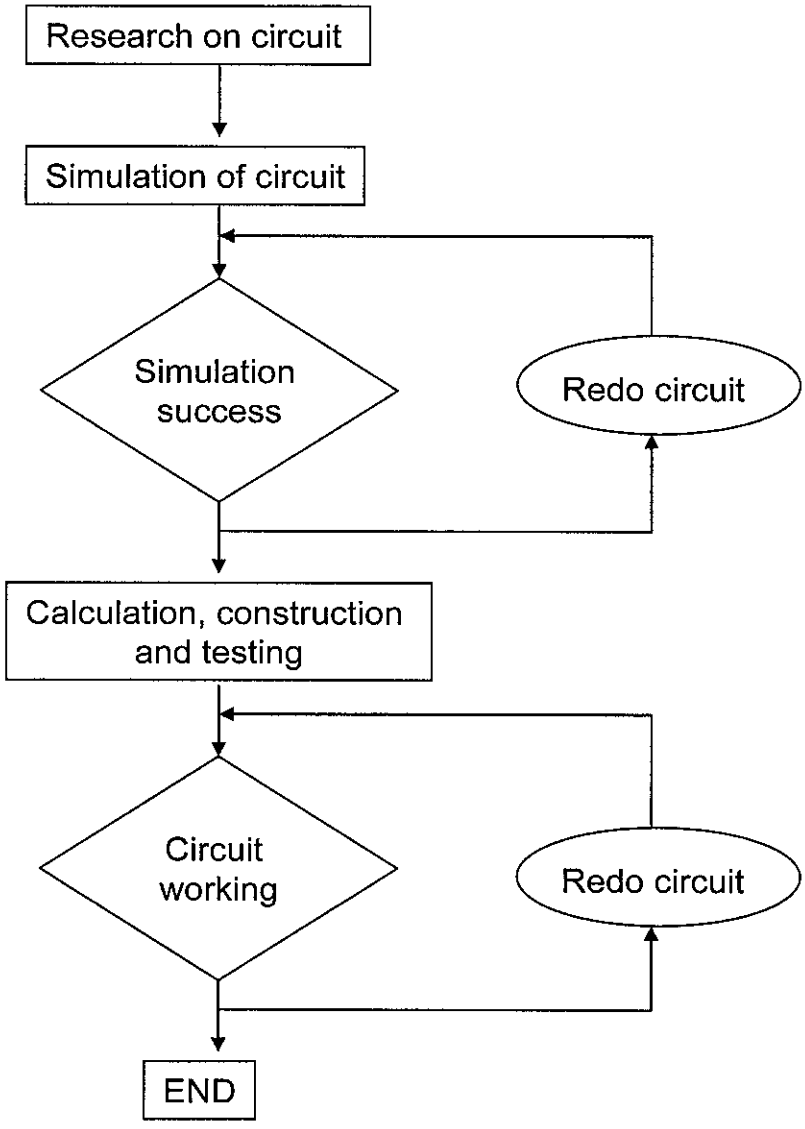


Figure 14: Flow Chart of the circuit development

CHAPTER 4

RESULTS AND DISCUSSION

In order to achieve the results of the circuit for the both circuit topologies (i) Forward converters and (ii) Flyback converters, simulation has been done on Multisim Simulation software. The simulation was done for both circuits which author has already discussed. The required circuit parameters are given below in order to simulate.

- Output voltage = 3.3 V
- Bias Voltage = 15.0 V
- Output current = 0.8 A
- Switching frequency = 300 KHz

4.1 *Forward Converter* Simulation Results

Author has shown the simulation results in Figure 16 for the Forward converter circuit. The wave form shows the exact circuit parameters as expected discussed in beginning of this chapter. The required results were achieved successfully as expected i.e. output voltage, current and the power.

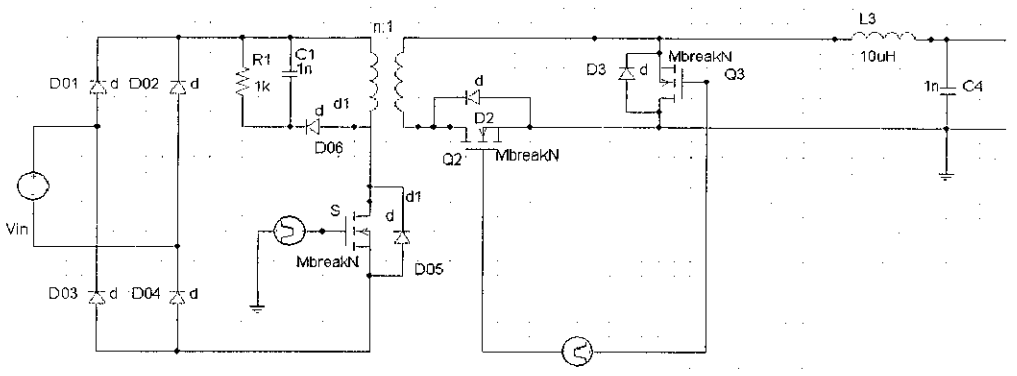


Figure 15: Forward converter (After minor change)

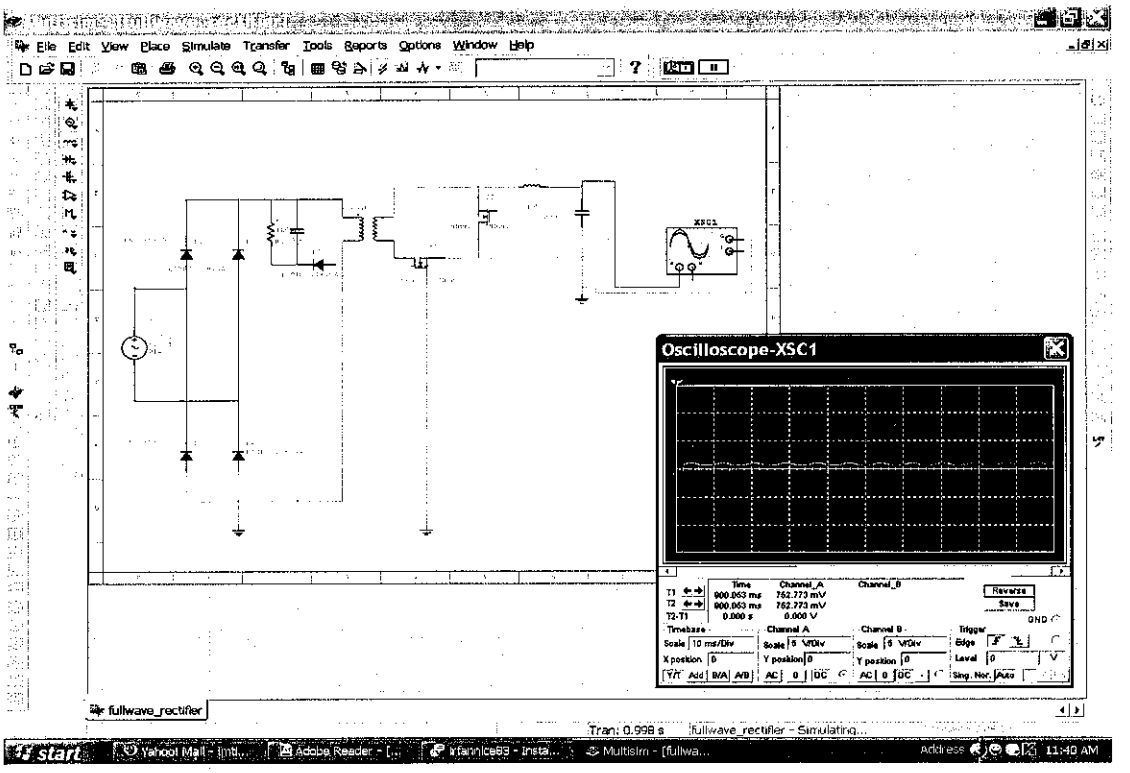


Figure 16 (a): Simulation Result for the Forward converter

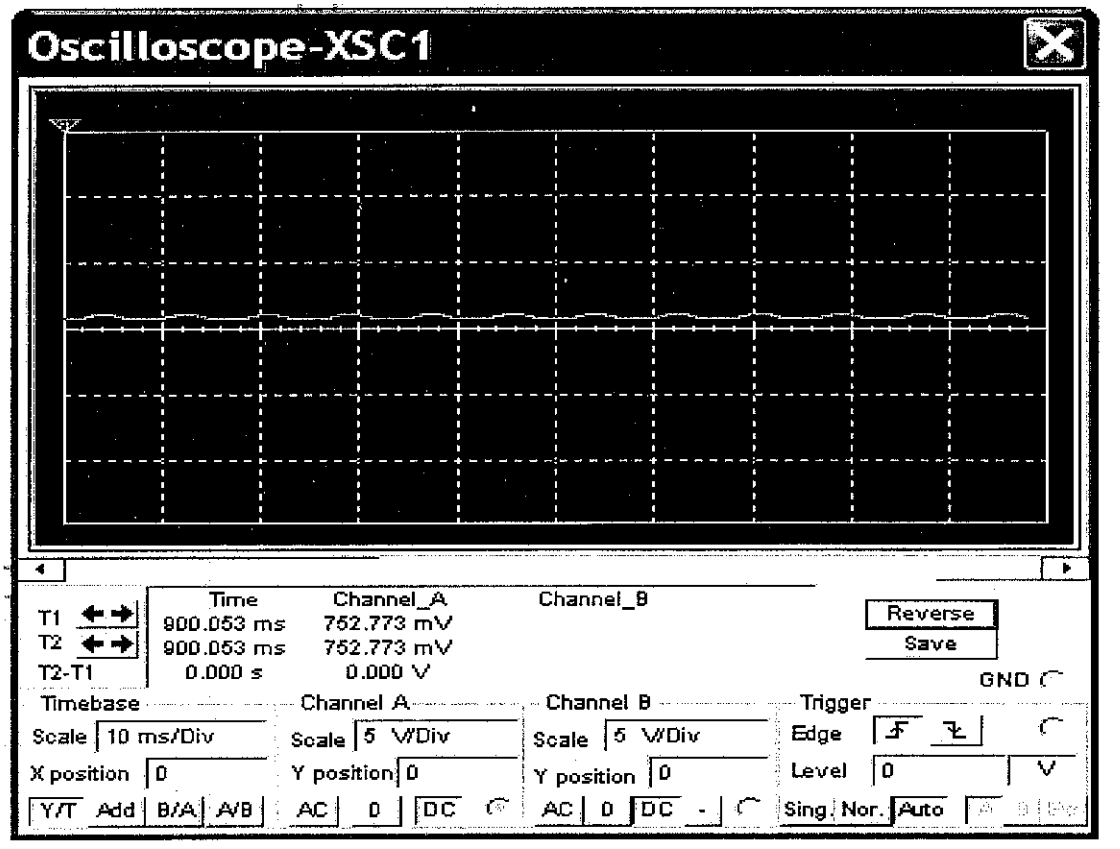


Figure 16 (b): Waveform for the Forward converter

4.2 *Flyback Converter* Simulation Results

Table 1 which shows the components and the values. These components and values are got with the help of online database of *International Rectifiers* Company. These component values are for the flyback converter circuit in Figure 17. This is the actual circuit for the flyback converter circuit [1]. The circuit was simulated using the Multisim Simulation software. It was simulated using the circuit parameters, presented in Table 1.

Figure 8 shows the simulation of flyback converter without the control IC IR1167A. In order to conform, author contacted one of the Engineers of *International Rectifiers* Company. He replied that; successful results will be achieved after building the circuit and testing in laboratory.

Table 1: SR components value

Component	Ref Des	Value	Power Dissipation	Calculations
Controller	U1	IR1166SPBF	0.406 W	102.0 °C Tj
Sync Rec MOSFET	Q1	IRFR3710ZPBF (x2)	2.421 W	99.9 °C Tc max
Voltage Drop Resistor	R1	30.0 Ω	0.033 W	
MOT Resistor	R2	36.0 kΩ		1.44 µs min ON time
Gate Resistor	R3	1.0 Ω	0.131 W	
Decoupling Capacitor	C1	1.00 µF	N/A	281 mV Vcc max ripple voltage
Start time Capacitor	C2	0.33 nF	N/A	90 µs start time

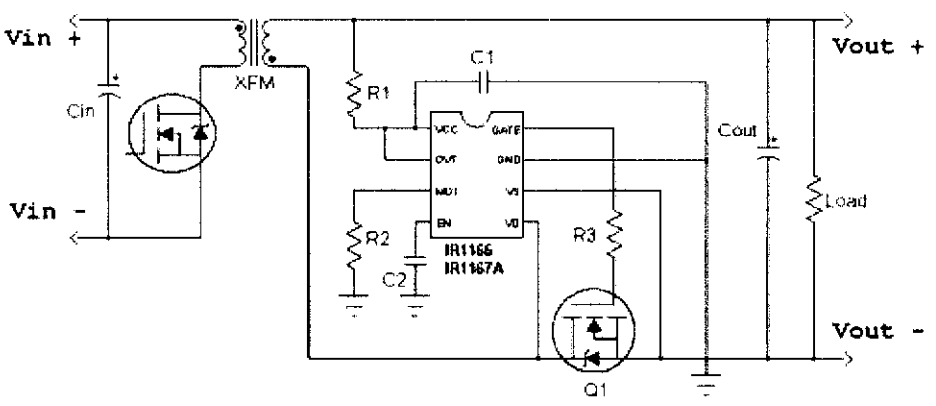


Figure 17: Flyback converter circuit topology

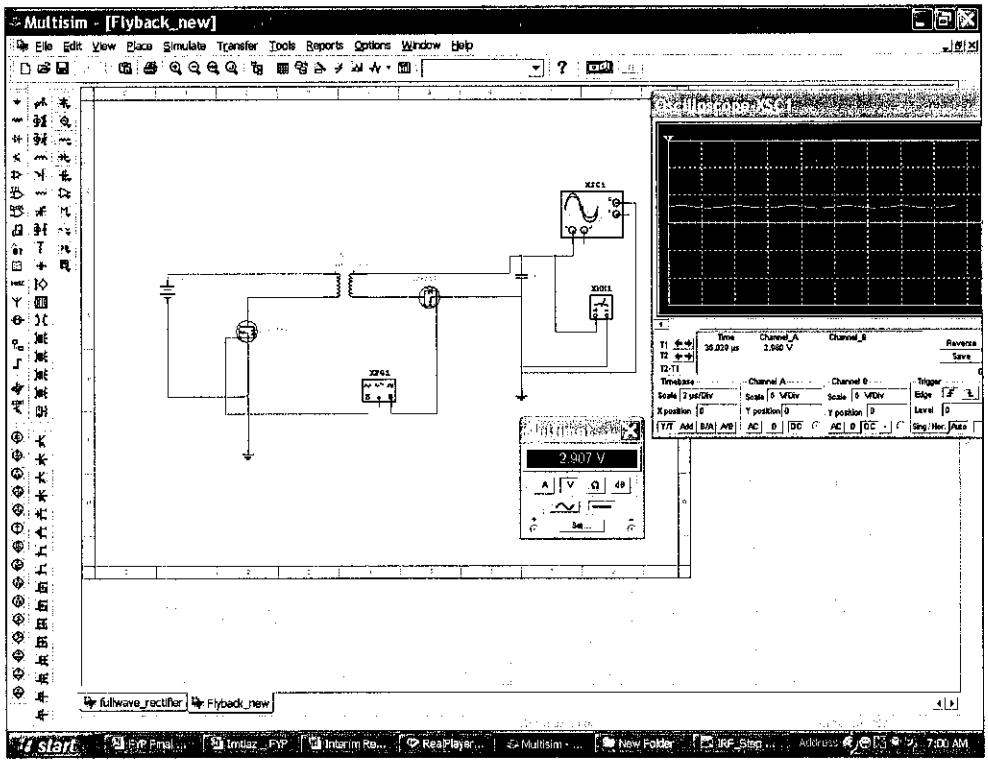


Figure 18 (a): Simulation Results for *Flyback Converter*

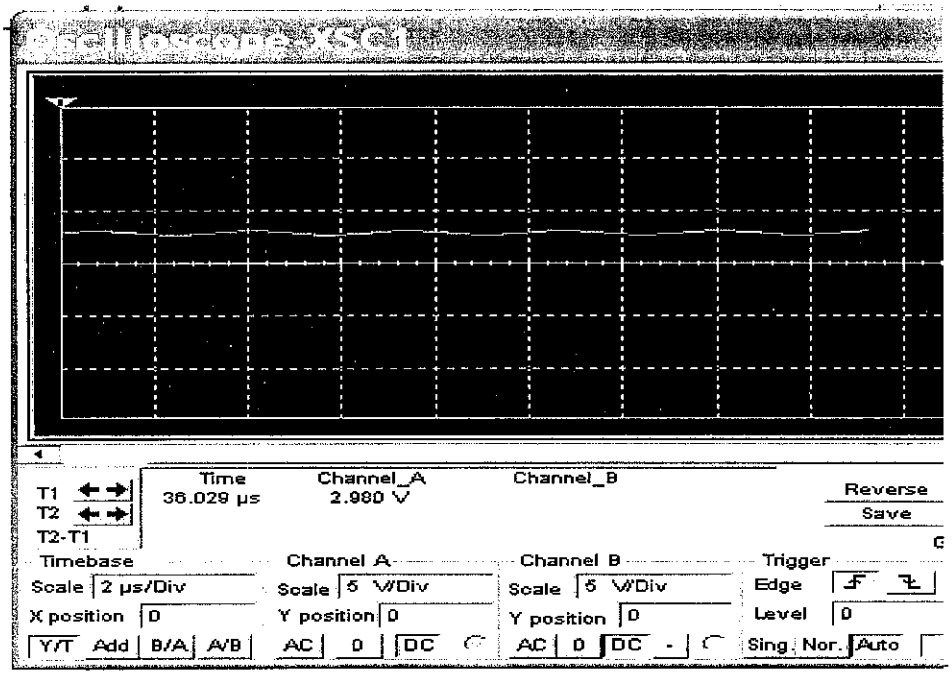


Figure 18 (b): Waveform for simulation

CHAPTER 5

CONCLUSION AND RECOMMENDATION

5.1 Conclusion

The main objective of the final year project *"Design and analysis of synchronous d.c. to d.c. converter"* has been achieved successfully. Research was done, in order to design and analyze the converter. Author focused two main circuit topologies for synchronous converters, (i) *Forward Converter* with Control-Driven Synchronous rectifiers (SR) and (ii) *Flyback converter* with Constant-Frequency (CF) Continuous-Conduction-Mode (CCM). This report details the brief back ground study, literature review, results and discussion about the both converter type i.e. Forward converters and Flyback converters. Author achieved the required converter parameters by using Multisim simulation software. Author believes that Synchronous Conversion is a growing concept; where the main objective is to reduce down power losses during rectification of power. By using synchronous rectifiers we manage to minimize the size of the power supplies used in portable appliances like Laptops and Mobile phones.

5.2 Recommendation

Author believes that, continuation to his work can achieve the remarkable work in future. One can easily understand and get to know as to continue this work. His work came up with some new things. Author remains successful to achieve objective of the project. This project's main concern was to design and analyze and now he recommend, building and constructing this circuit since the simulation went success.

REFERENCES

[1] Maurizio Salato, Adnaan Lokhandwala, Marco Soldano, "Design of Secondary Side Rectification using IR1167 SmartRectifier™ Control IC" Application Note AN-1087.

[2] Michael T. Zhang, *Member, IEEE,* Milan M. Jovanovi'c, *Senior Member, IEEE,* and Fred C. Y. Lee, *Fellow,* "Design Considerations and Performance Evaluations of Synchronous Rectification in Flyback Converters" IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 13, NO. 3, MAY 1998

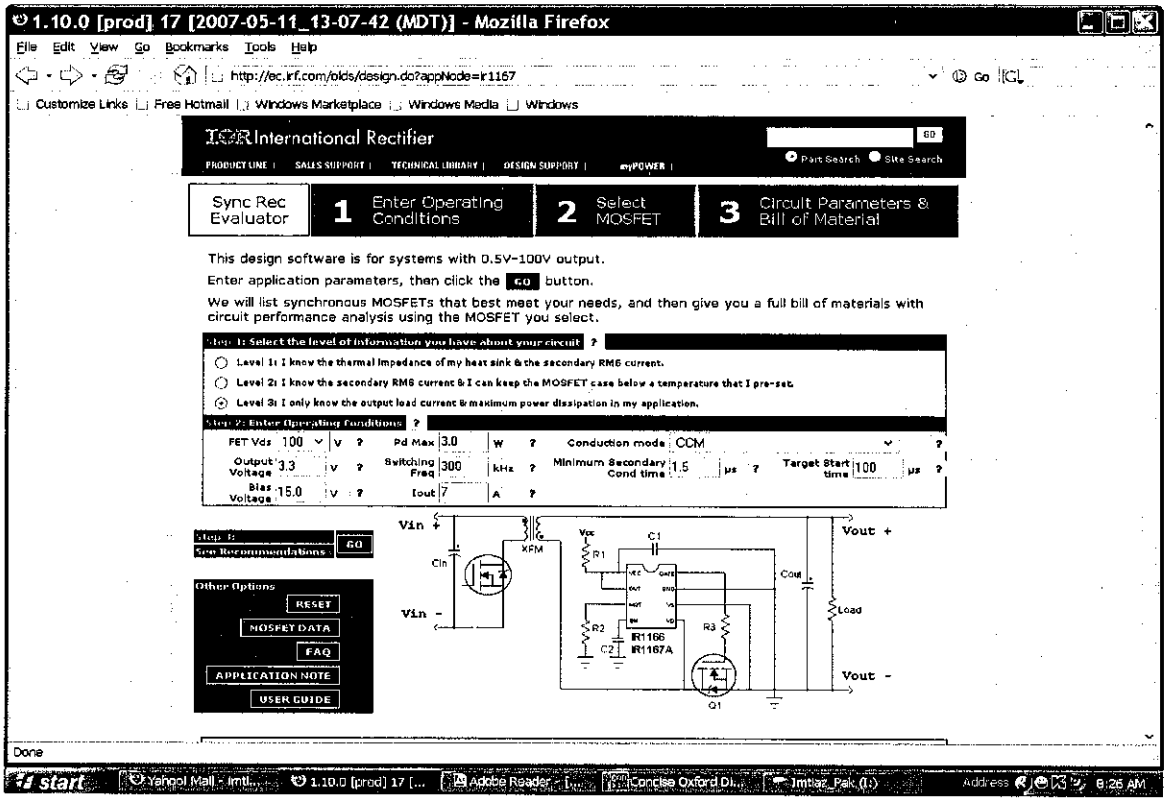
[3] C. Blake, D. Kinzer, and P. Wood, "Synchronous rectifiers versus Schottky diodes: comparison of the losses of a synchronous rectifier versus the losses of a Schottky diode rectifier," *Proc. IEEE Appl. Power Electron. Conf.*, 1994, pp. 17-23.

[4] "Flyback Transformer Design for the IRIS40xx Series", Application Note AN-1024, www.irf.com

[5] Milan M. JovanoviC, *Senior Member, IEEE,* Michael T. Zhang, and Fred C. Lee, *Fellow, IEEE.* "Evaluation of Synchronous-Rectification Efficiency Improvement Limits in Forward Converters". IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 42. NO. 4, AUGUST 1995.

[6] *Power Product Data Book,* Siliconix, 1994, pp. 6121-6-124.

APPENDIX A
PROCEDURE TO SELECT CIRCUIT COMPONENTS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File Edit View Go Bookmarks Tools Help
http://ec.irf.com/olds/design.do?appNode=ir1167
Customize Links Free Hotmail Windows Marketplace Windows Media Windows
International Rectifier
Sync Rec Evaluator
1 Enter Operating Conditions
2 Select MOSFET
3 Circuit Parameters & Bill of Material
This design software is for systems with 0.5V~100V output.
Enter application parameters, then click the GO button.
We will list synchronous MOSFETs that best meet your needs, and then give you a full bill of materials with circuit performance analysis using the MOSFET you select.
Step 1: Select the level of information you have about your circuit
Level 1: I know the thermal impedance of my heat sink & the secondary RMS current.
Level 2: I know the secondary RMS current & I can keep the MOSFET case below a temperature that I pre-set.
Level 3: I only know the output load current & maximum power dissipation in my application.
Step 2: Enter Operating Conditions
FET Vds 100 V
Pd Max 3.0 W
Conduction mode CCM
Output Voltage 3.3 V
Switching Freq 300 kHz
Minimum Secondary Cond time 1.5 µs
Target Start time 100 µs
Bias Voltage 15.0 V
Iout 7 A
Step 3: See Recommendations GO
Other Options
RESET
MOSFET DATA
FAQ
APPLICATION NOTE
USER GUIDE
Vin +
Vin -
Cin
XFM
Vcc
C1
R1
R2
C2
IR1166
IR1167A
R3
Q1
Cout
Load
Vout +
Vout -
Done
start
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Address
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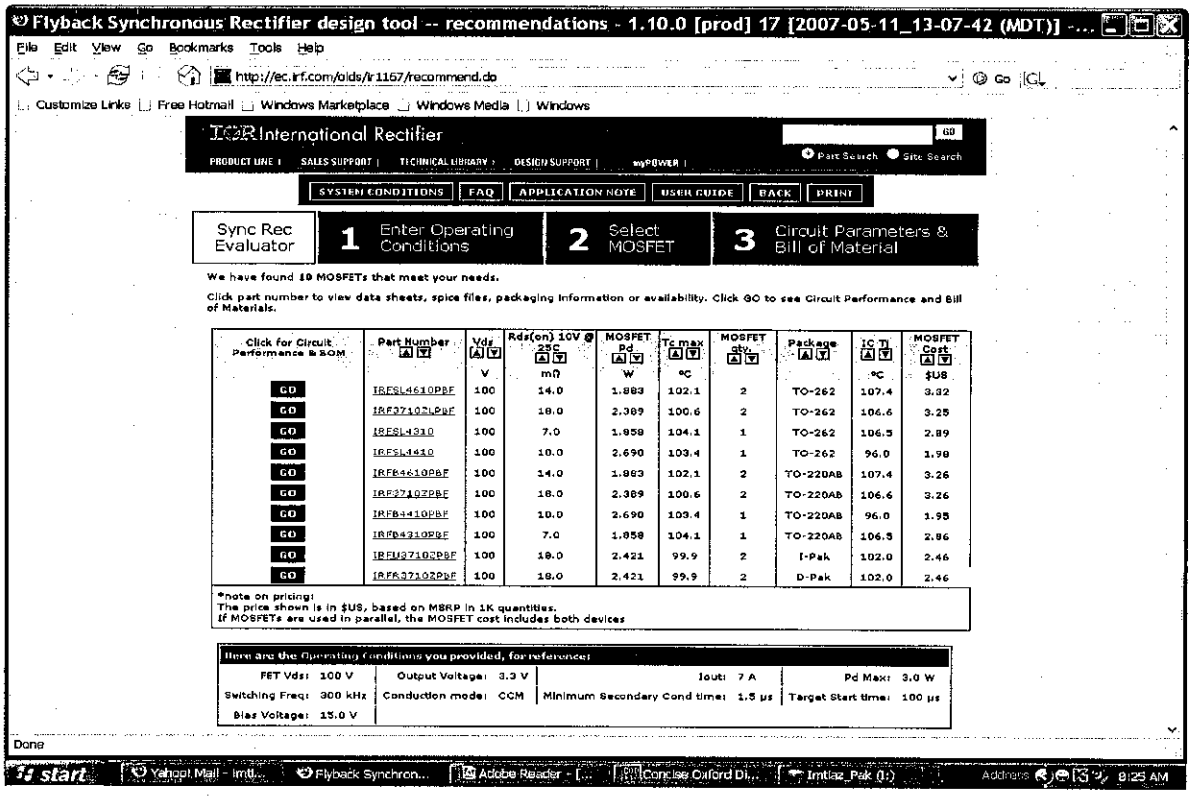
Step 1


Flyback Synchronous Rectifier design tool -- recommendations - 1.10.0 [prod] 17 [2007-05-11_13-07-42 (MDT)]
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http://ec.irf.com/olds/ir1167/recommend.do
Customize Links Free Hotmail Windows Marketplace Windows Media Windows
International Rectifier
SYSTEM CONDITIONS FAQ APPLICATION NOTE USER GUIDE BACK PRINT
Sync Rec Evaluator
1 Enter Operating Conditions
2 Select MOSFET
3 Circuit Parameters & Bill of Material
We have found 10 MOSFETs that meet your needs.
Click part number to view data sheets, spice files, packaging information or availability. Click GO to see Circuit Performance and Bill of Materials.
Click for Circuit Performance & BOM
Part Number
Vds V
Rds(on) 10V @ 25C mΩ
MOSFET Pd W
Tc max °C
MOSFET qty.
Package
IC Tj °C
MOSFET Cost $US
GO IRFSL4610PBF 100 14.0 1.883 102.1 2 TO-262 107.4 3.32
GO IRF3710ZLPBF 100 18.0 2.389 100.6 2 TO-262 106.6 3.25
GO IRFSL4310 100 7.0 1.958 104.1 1 TO-262 106.5 2.89
GO IRFSL4410 100 10.0 2.690 103.4 1 TO-262 96.0 1.98
GO IRF4610PBF 100 14.0 1.883 102.1 2 TO-220AB 107.4 3.26
GO IRF3710ZPBF 100 18.0 2.389 100.6 2 TO-220AB 106.6 3.26
GO IRF4410PBF 100 10.0 2.690 103.4 1 TO-220AB 96.0 1.98
GO IRF4310PBF 100 7.0 1.958 104.1 1 TO-220AB 106.5 2.86
GO IRFU3710ZPBF 100 18.0 2.421 99.9 2 I-Pak 102.0 2.46
GO IRFR3710ZPBF 100 18.0 2.421 99.9 2 D-Pak 102.0 2.46
*note on pricing:
The price shown is in $US, based on MSRP in 1K quantities.
If MOSFETs are used in parallel, the MOSFET cost includes both devices
Here are the Operating Conditions you provided, for reference:
FET Vds: 100 V
Output Voltage: 3.3 V
Iout: 7 A
Pd Max: 3.0 W
Switching Freq: 300 kHz
Conduction mode: CCM
Minimum Secondary Cond time: 1.5 µs
Target Start time: 100 µs
Bias Voltage: 15.0 V
Done
start
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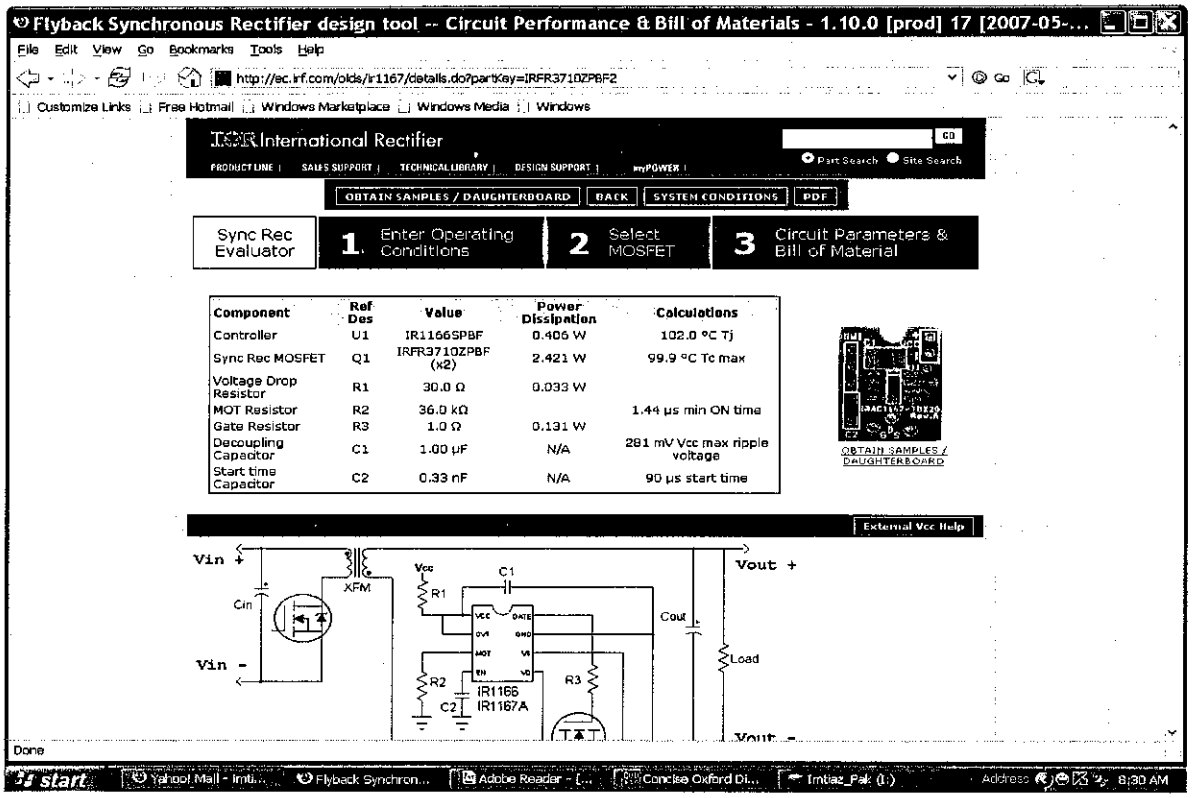
Step 2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International Rectifier
PRODUCT LINE | SALES SUPPORT | TECHNICAL LIBRARY | DESIGN SUPPORT | myPOWER |
Part Search Site Search
OBTAIN SAMPLES / DAUGHTERBOARD BACK SYSTEM CONDITIONS PDF
Sync Rec Evaluator
1. Enter Operating Conditions
2 Select MOSFET
3 Circuit Parameters & Bill of Material
Component Ref Des Value Power Dissipation Calculations
Controller U1 IR1166SPBF 0.406 W 102.0 °C Tj
Sync Rec MOSFET Q1 IRFR3710ZPBF (x2) 2.421 W 99.9 °C Tc max
Voltage Drop Resistor R1 30.0 Ω 0.033 W
MOT Resistor R2 36.0 kΩ 1.44 µs min ON time
Gate Resistor R3 1.0 Ω 0.131 W
Decoupling Capacitor C1 1.00 µF N/A 281 mV Vcc max ripple voltage
Start time Capacitor C2 0.33 nF N/A 90 µs start time
OBTAIN SAMPLES / DAUGHTERBOARD
External Vcc Help
Vin +
Vin -
Cin
XFM
Vcc
C1
R1
Cout
Vout +
Load
R2
C2
IR1166
IR1167A
R3
Vout -
Done
start
Yahoo! Mail - Imti...
Flyback Synchron...
Adobe Reader - [...
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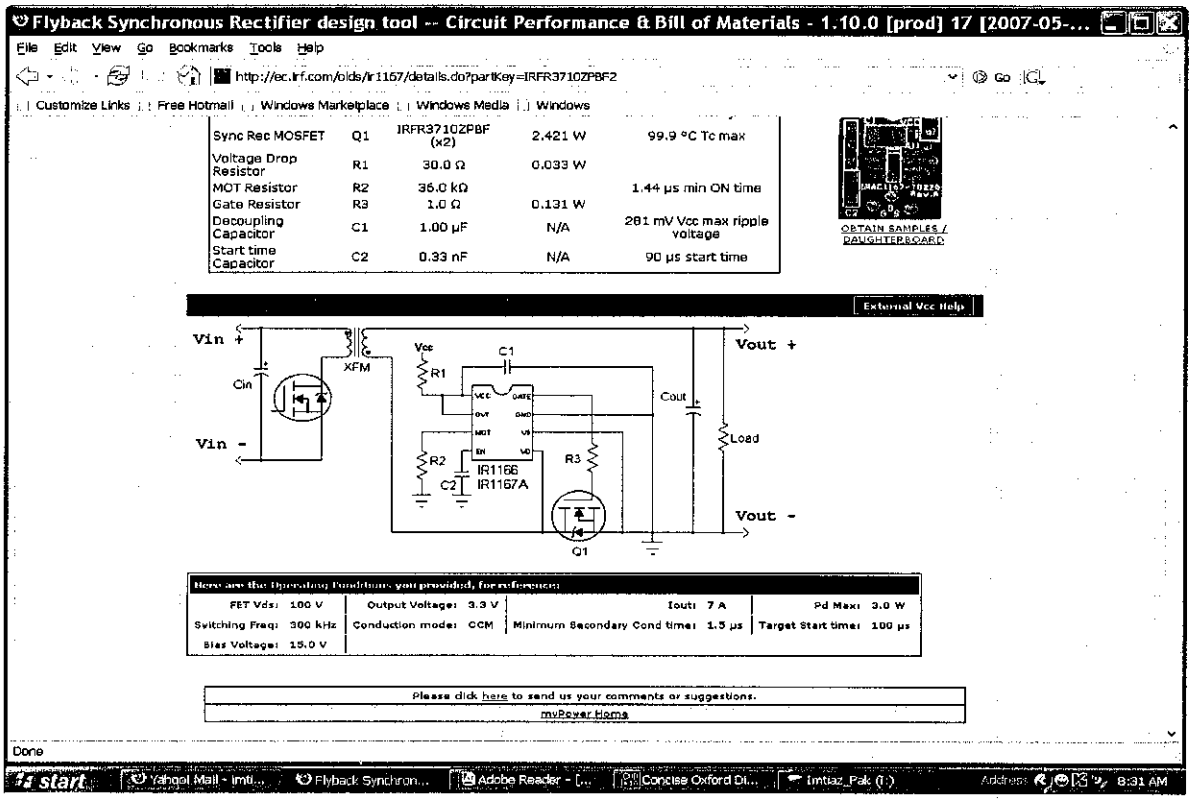
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Customize Links Free Hotmail Windows Marketplace Windows Media Windows
Sync Rec MOSFET Q1 IRFR3710ZPBF (x2) 2.421 W 99.9 °C Tc max
Voltage Drop Resistor R1 30.0 Ω 0.033 W
MOT Resistor R2 36.0 kΩ 1.44 µs min ON time
Gate Resistor R3 1.0 Ω 0.131 W
Decoupling Capacitor C1 1.00 µF N/A 281 mV Vcc max ripple voltage
Start time Capacitor C2 0.33 nF N/A 90 µs start time
OBTAIN SAMPLES / DAUGHTERBOARD
External Vcc Help
Vin +
Vin -
Cin
XFM
Vcc
C1
R1
Cout
Vout +
Load
R2
C2
IR1166
IR1167A
R3
Q1
Vout -
Here are the Operating Conditions you provided, for reference:
FET Vds: 100 V
Output Voltage: 3.3 V
Iout: 7 A
Pd Max: 3.0 W
Switching Freq: 300 kHz
Conduction mode: CCM
Minimum Secondary Cond time: 1.5 µs
Target Start time: 100 µs
Bias Voltage: 15.0 V
Please click here to send us your comments or suggestions.
myPower Home
Done
start
Yahoo! Mail - Imti...
Flyback Synchron...
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8:31 AM

Step 3

International
IOR Rectifier

AUTOMOTIVE MOSFET

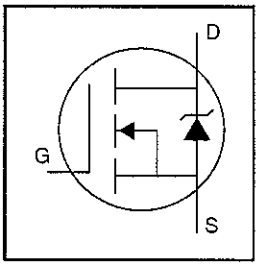
PD - 94740A

IRFR3710Z
IRFU3710Z

HEXFET® Power MOSFET

Features

- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax



V_{DSS} = 100V

$R_{DS(on)}$ = 18mΩ

I_D = 42A

Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating . These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

D-Pak
IRFR3710Z

I-Pak
IRFU3710Z

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	56	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	39	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Package Limited)	42	
I_{DM}	Pulsed Drain Current ①	220	
P_D @T_C = 25°C	Power Dissipation	140	W
	Linear Derating Factor	0.95	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy②	150	mJ
E_{AS} (Tested)	Single Pulse Avalanche Energy Tested Value ⑥	200	
I_{AR}	Avalanche Current ①	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy ⑤		mJ
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.05	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount) ⑦	—	40	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

HEXFET® is a registered trademark of International Rectifier.

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.088	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	15	18	mΩ	V_{GS} = 10V, I_D = 33A ③
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
gfs	Forward Transconductance	39	—	—	S	V_{DS} = 25V, I_D = 33A
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V_{DS} = 100V, V_{GS} = 0V
		—	—	250		V_{DS} = 100V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V_{GS} = -20V
Q_g	Total Gate Charge	—	69	100		I_D = 33A
Q_{gs}	Gate-to-Source Charge	—	15	—	nC	V_{DS} = 80V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	25	—		V_{GS} = 10V ③
$t_{d(on)}$	Turn-On Delay Time	—	14	—		V_{DD} = 50V
t_r	Rise Time	—	43	—		I_D = 33A
$t_{d(off)}$	Turn-Off Delay Time	—	53	—	ns	R_G = 6.8 Ω
t_f	Fall Time	—	42	—		V_{GS} = 10V ③
L_D	Internal Drain Inductance	—	4.5	—		Between lead,
					nH	6mm (0.25in.)
L_S	Internal Source Inductance	—	7.5	—		from package
						and center of die contact
C_{iss}	Input Capacitance	—	2930	—		V_{GS} = 0V
C_{oss}	Output Capacitance	—	290	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	180	—	pF	f = 1.0MHz
C_{oss}	Output Capacitance	—	1200	—		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	—	180	—		V_{GS} = 0V, V_{DS} = 80V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	—	430	—		V_{GS} = 0V, V_{DS} = 0V to 80V ④

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current	—	—	56		MOSFET symbol
	(Body Diode)				A	showing the
I_{SM}	Pulsed Source Current	—	—	220		integral reverse
	(Body Diode) ①					p-n junction diode.
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 33A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	—	35	53	ns	T_J = 25°C, I_F = 33A, V_{DD} = 50V
Q_{rr}	Reverse Recovery Charge	—	41	62	nC	di/dt = 100A/μs ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

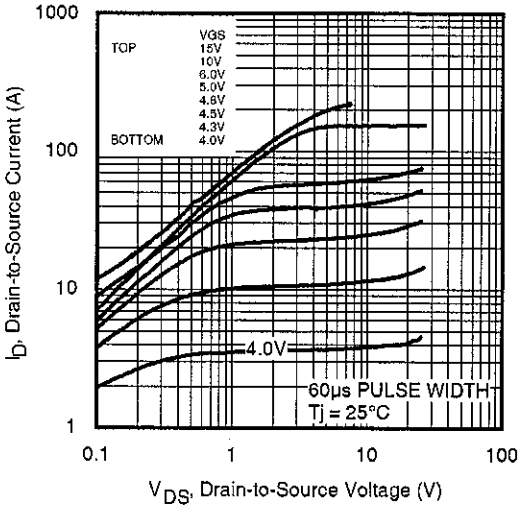


Fig 1. Typical Output Characteristics

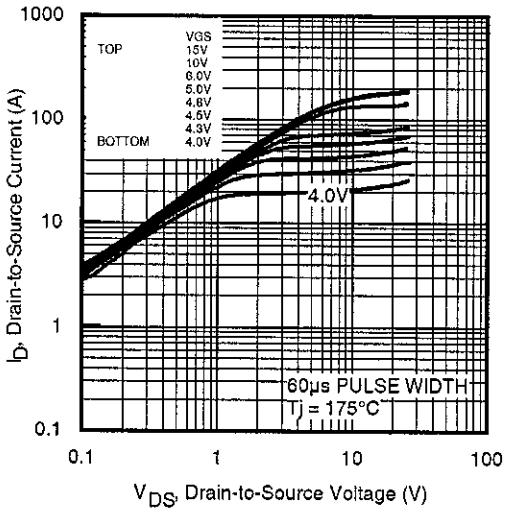


Fig 2. Typical Output Characteristics

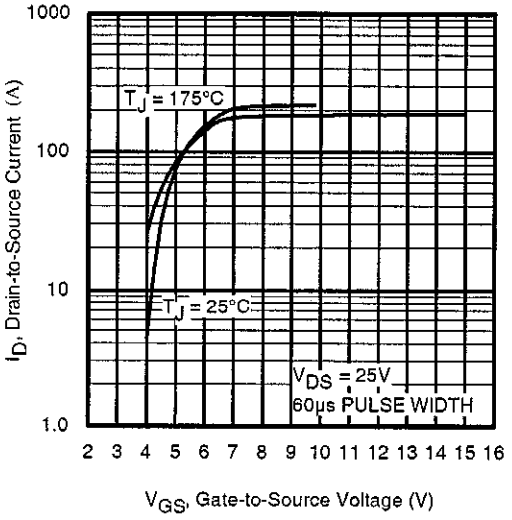


Fig 3. Typical Transfer Characteristics

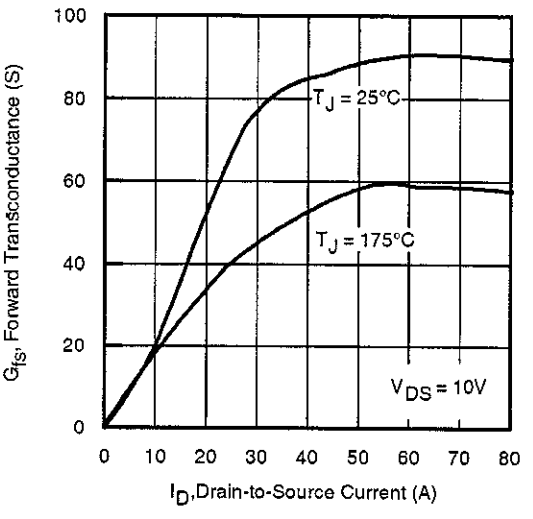


Fig 4. Typical Forward Transconductance vs. Drain Current

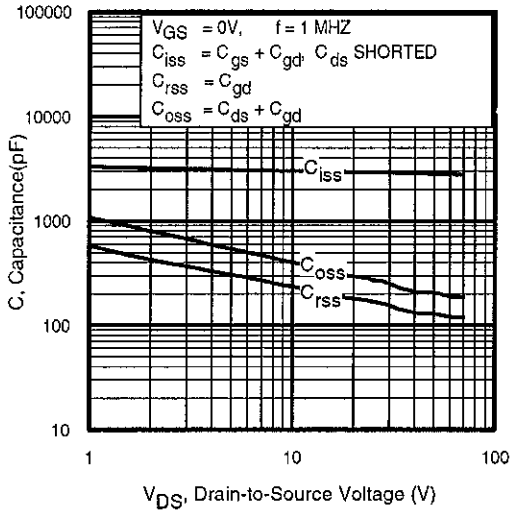


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

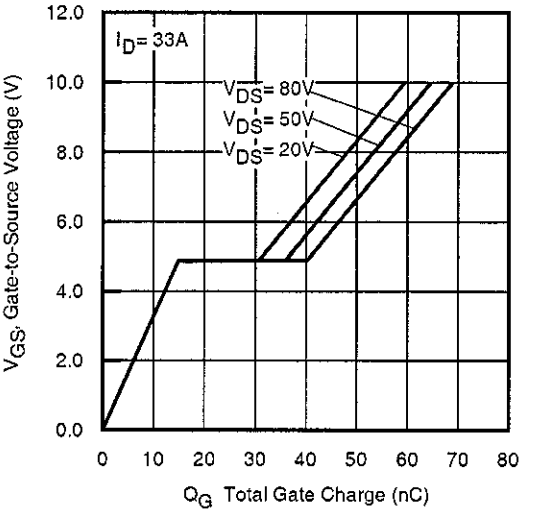


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

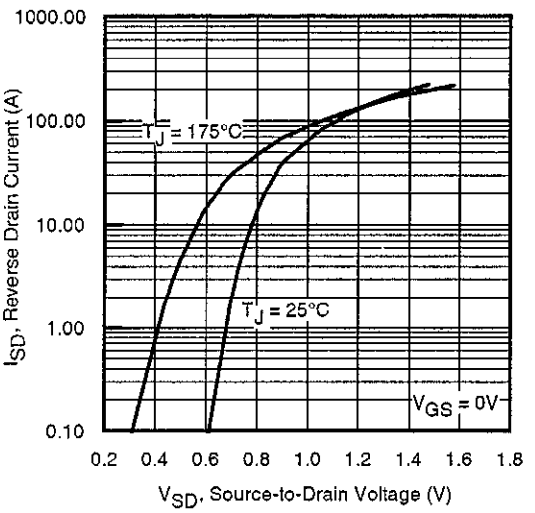


Fig 7. Typical Source-Drain Diode Forward Voltage

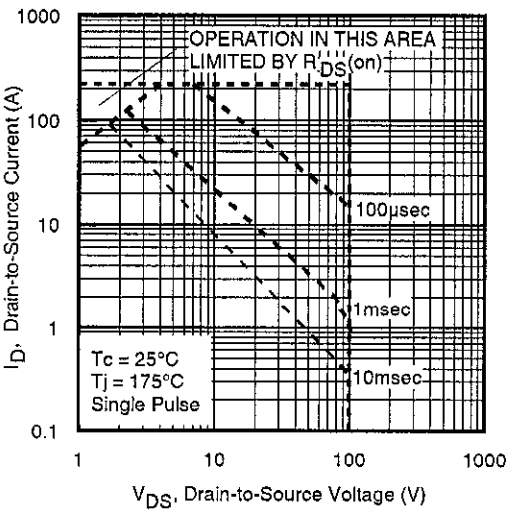


Fig 8. Maximum Safe Operating Area

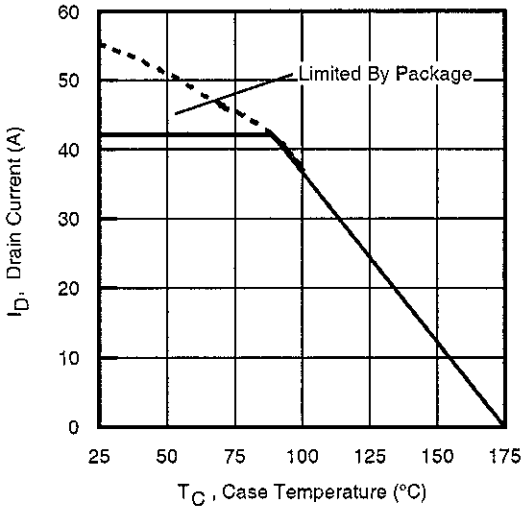


Fig 9. Maximum Drain Current vs. Case Temperature

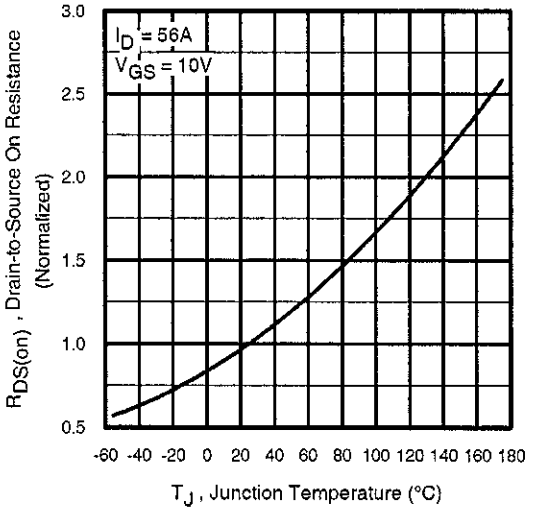


Fig 10. Normalized On-Resistance vs. Temperature

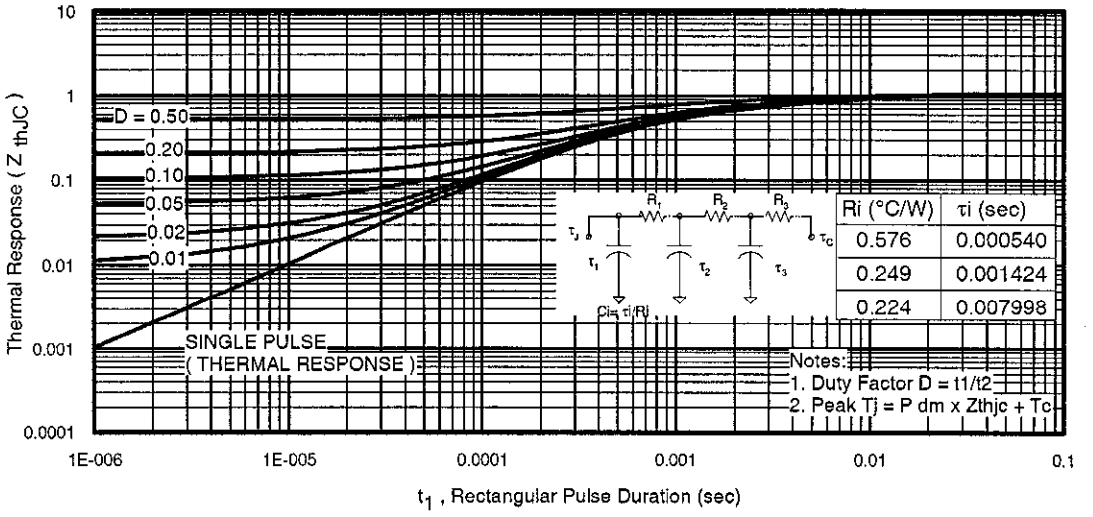


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

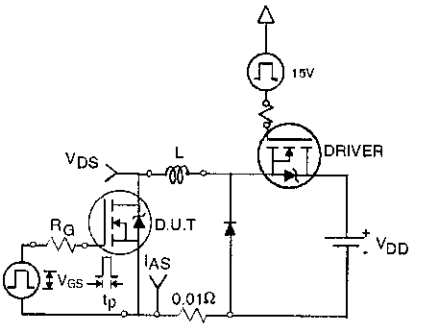


Fig 12a. Unclamped Inductive Test Circuit

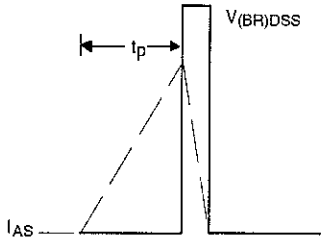


Fig 12b. Unclamped Inductive Waveforms

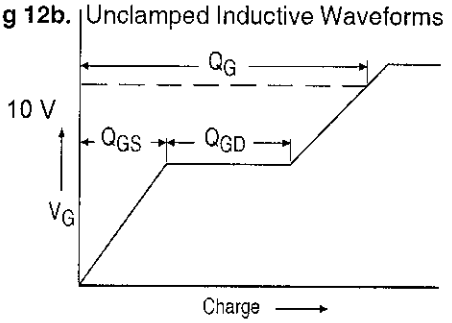


Fig 13a. Basic Gate Charge Waveform

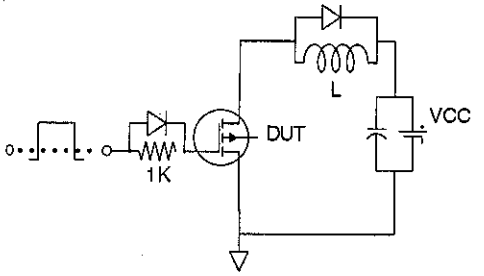


Fig 13b. Gate Charge Test Circuit

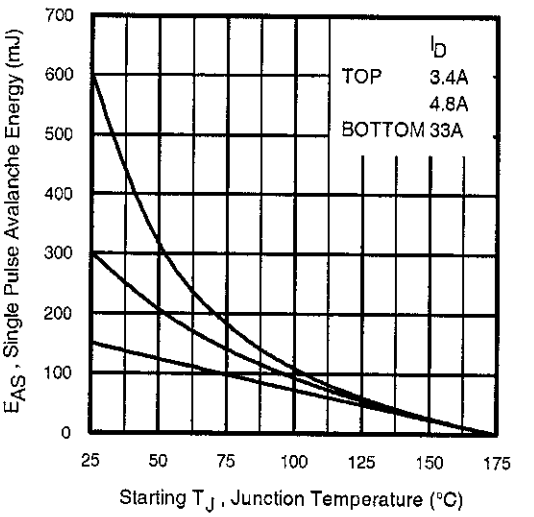


Fig 12c. Maximum Avalanche Energy vs. Drain Current

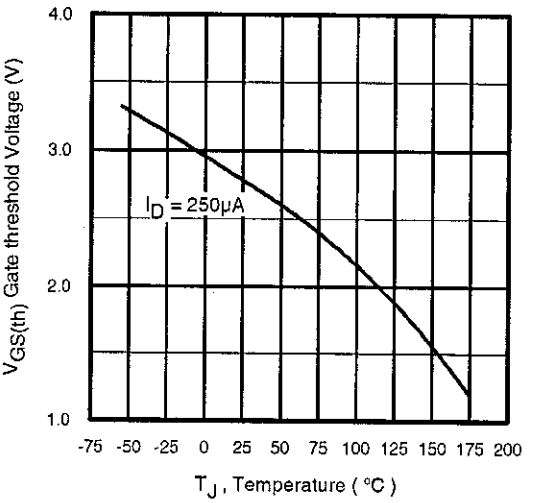


Fig 14. Threshold Voltage vs. Temperature

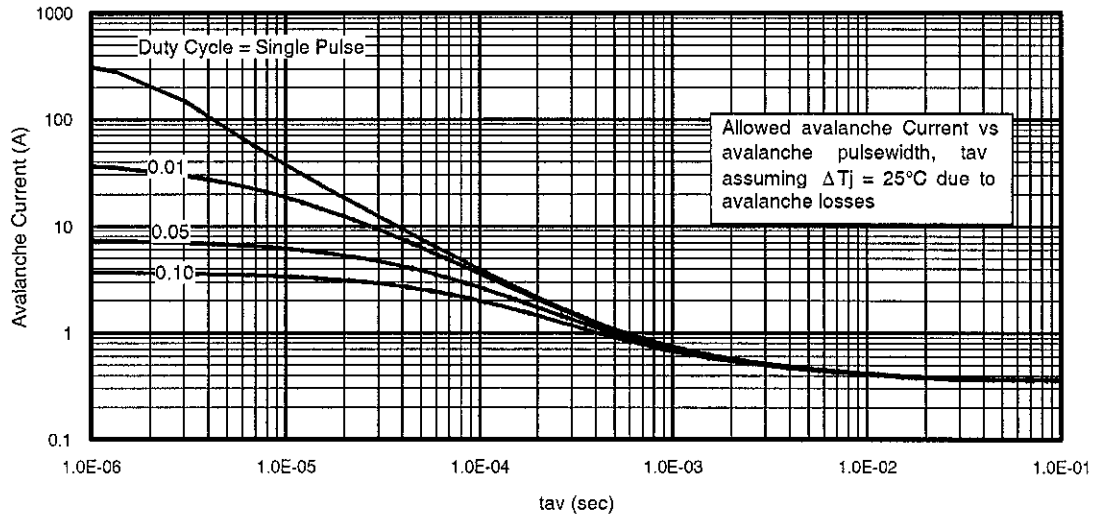


Fig 15. Typical Avalanche Current vs.Pulsewidth

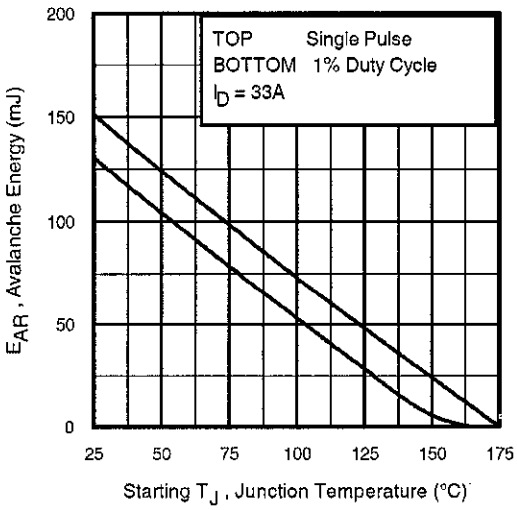


Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

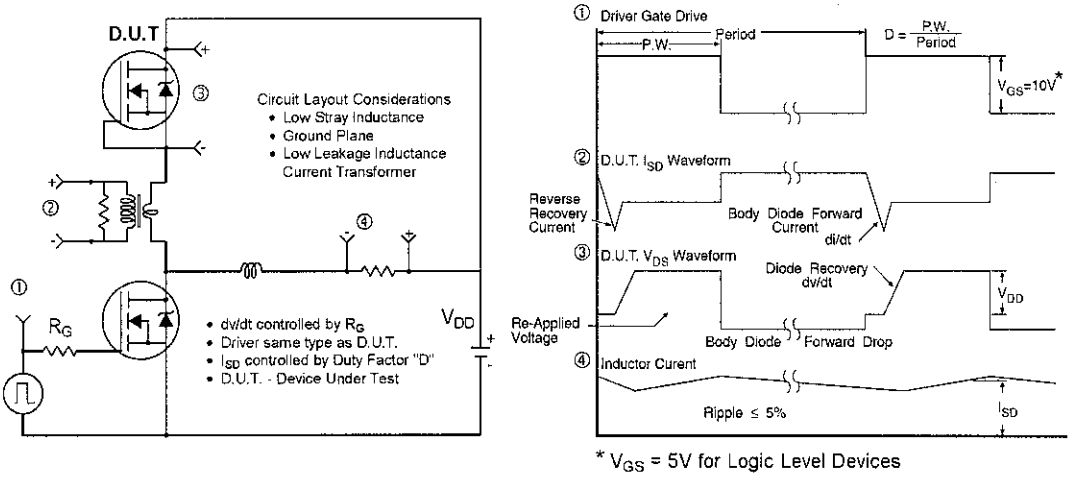


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

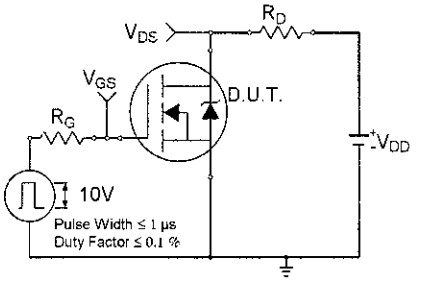


Fig 18a. Switching Time Test Circuit

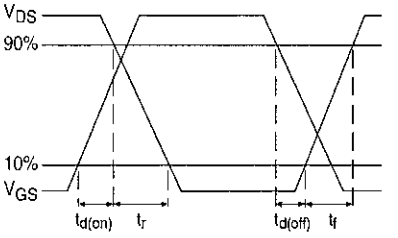
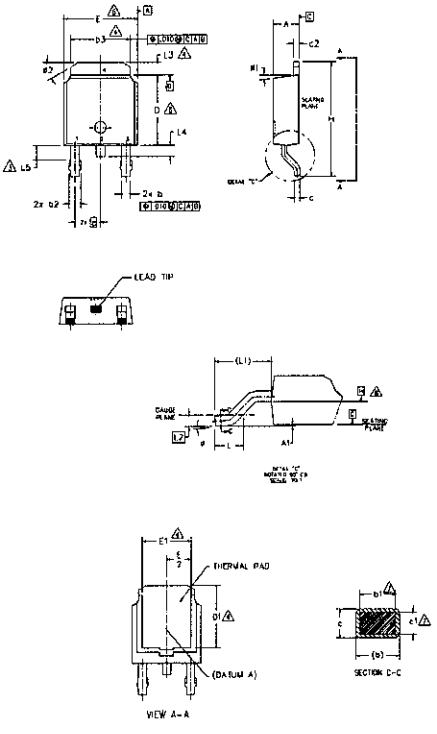


Fig 18b. Switching Time Waveforms

D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:
1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].
3 LEAD DIMENSION UNCONTROLLED IN L5.
4 DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
5.- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
6 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
7 DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
8 DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	–	0.13	–	.005	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	–	.205	–	4
E	6.35	6.73	.250	.265	6
E1	4.32	–	.170	–	4
e	2.29 BSC		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	4
L4	–	1.02	–	.040	
L5	1.14	1.52	.045	.060	3
ø	0°	10°	0°	10°	
ø1	0°	15°	0°	15°	
ø2	25°	35°	25°	35°	

LEAD ASSIGNMENTS

HEXFET

1.- GATE
2.- DRAIN
3.- SOURCE
4.- DRAIN

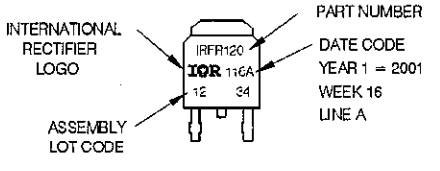
IGBT & CoPAK

1.- GATE
2.- COLLECTOR
3.- EMITTER
4.- COLLECTOR

D-Pak (TO-252AA) Part Marking Information

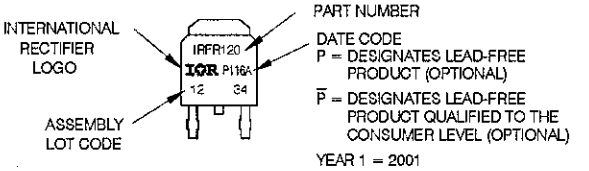
EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 2001
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position indicates "Lead-Free"



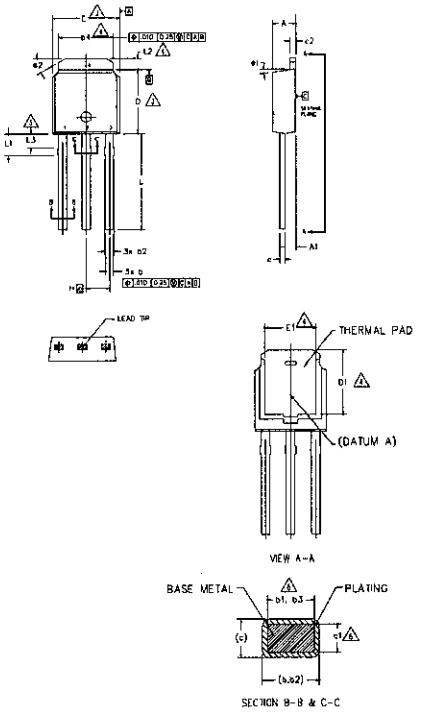
"P" in assembly line position indicates "Lead-Free" qualification to the consumer-level

OR



I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES

1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994

2 - DIMENSION ARE SHOWN IN INCHES [MILLIMETERS]

3 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.

4.- THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.

5.- LEAD DIMENSION UNCONTROLLED IN L3.

6.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.

7.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA (Date 06/02).

8 - CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	0.89	1.14	.035	.045	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	6
b2	0.76	1.14	.030	.045	
b3	0.76	1.04	.030	.041	6
b4	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	6
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	3
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	3
E1	4.32	-	.170	-	4
e	2.29 BSC		.090 BSC		
L	8.89	9.65	.350	.380	
L1	1.91	2.29	.045	.090	
L2	0.89	1.27	.035	.050	4
L3	1.14	1.52	.045	.060	5
θ1	0°	15°	0°	15°	
θ2	25°	35°	25°	35°	

LEAD ASSIGNMENTS

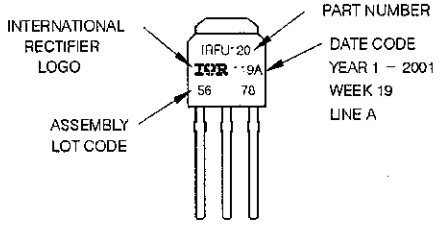
HEXFET

1.- GATE
2.- DRAIN
3.- SOURCE
4.- DRAIN

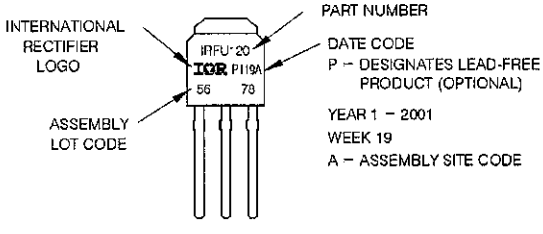
I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120
WITH ASSEMBLY
LOT CODE 5678
ASSEMBLED ON WW 19, 2001
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position
indicates Lead-Free"

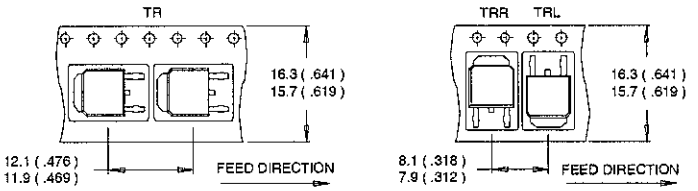


OR

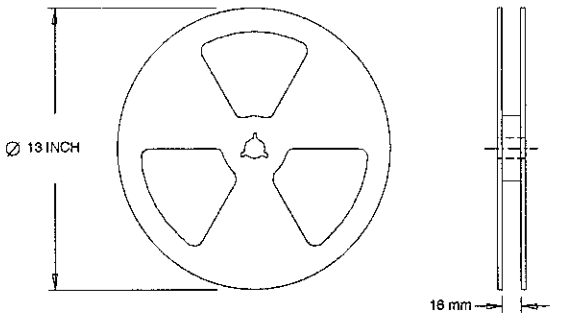


D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).

② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.28mH R_G = 25Ω, I_{AS} = 33A, V_{GS} =10V. Part not recommended for use above this value.

③ Pulse width ≤ 1.0ms; duty cycle ≤ 2%.

④ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⑤ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

⑥ This value determined from sample failure population. 100% tested to this value in production.

⑦ When mounted on 1" square PCB (FR-4 or G-10 Material) . For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Automotive [Q101] market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.11/06

International
IOR Rectifier

Data Sheet PD60254D

IR1167ASPbF
IR1167BSPbF

SmartRectifier™ CONTROL IC

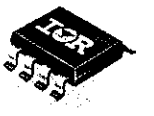
Features

- Secondary side high speed SR controller
- DCM, CrCM and CCM flyback topologies
- 200V proprietary IC technology
- Max 500KHz switching frequency
- Anti-bounce logic and UVLO protection
- 7A peak turn off drive current
- Micropower start-up & ultra low quiescent current
- 10.7/14.5V gate drive clamp
- 50ns turn-off propagation delay
- Vcc range from 11.3V to 20V
- Direct sensing of MOSFET drain voltage
- Minimal component count
- Simple design
- Lead-free
- Compatible with 1W Standby, Energy Star, CECP, etc.

Description

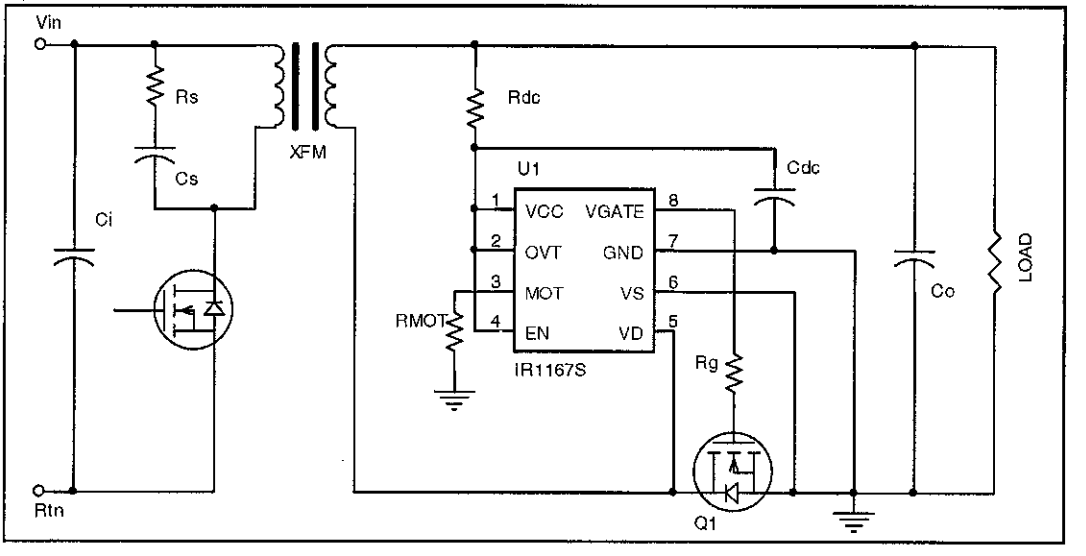
IR1167S is a smart secondary side driver IC designed to drive N-Channel power MOSFETs used as synchronous rectifiers in isolated Flyback converters.
The IC can control one or more paralleled N-MOSFETs to emulate the behavior of Schottky diode rectifiers. The drain to source voltage is sensed differentially to determine the polarity of the current and turn the power switch on and off in proximity of the zero current transition.
Ruggedness and noise immunity are accomplished using an advanced blanking scheme and double-pulse suppression which allow reliable operation in continuous, discontinuous and critical current mode operation and both fixed and variable frequency modes.

Package



8-Lead SOIC

IR1167 Application Diagram



Absolute Maximum Ratings

Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions are not implied. All voltages are absolute voltages referenced to GND. Thermal resistance and power dissipation are measured under board mounted and still air conditions.

Parameters	Symbol	Min.	Max.	Units	Remarks
Supply Voltage	V_{CC}	-0.3	20	V	
Enable Voltage	V_{EN}	-0.3	20	V	
Cont. Drain Sense Voltage	V_D	-3	200	V	
Pulse Drain Sense Voltage	V_D	-5	200	V	
Source Sense Voltage	V_S	-3	20	V	
Gate Voltage	V_{GATE}	-0.3	20	V	V_{CC}=20V, Gate off
Operating Junction Temperature	T_J	-40	150	°C	
Storage Temperature	T_S	-55	150	°C	
Thermal Resistance	$R_{\theta JA}$		128	°C/W	SOIC-8
Package Power Dissipation	P_D		970	mW	SOIC-8, T_{AMB}=25°C
ESD Protection	V_{ESD}		2	kV	Human Body Model*
Switching Frequency	fsw		500	kHz	

* Per EIA/JESD22-A114-B(discharging a 100pF capacitor through a 1.5kΩ series resistor).

Electrical Characteristics

The electrical characteristics involve the spread of values guaranteed within the specified supply voltage and junction temperature range T_J from – 25° C to 125°C. Typical values represent the median values, which are related to 25°C. If not otherwise stated, a supply voltage of V_{CC} =15V is assumed for test condition.

Supply Section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks	
Supply Voltage Operating Range	V_{CC}	12		18	V	GBD	
V_{CC} Turn On Threshold	$V_{CC\ ON}$	9.8	10.5	11.3	V		
V_{CC} Turn Off Threshold (Under Voltage Lock Out)	$V_{CC\ UVLO}$	8.4	9	9.7	V		
V_{CC} Turn On/Off Hysteresis	$V_{CC\ HYST}$	1.4	1.55	1.7	V		
Operating Current	I_{CC}		8.5	10	mA	IR1167A	C_{LOAD}=1nF, fsw = 400kHz
			50	65			C_{LOAD}=10nF, f_{SW} = 400kHz
			10.3	12		IR1167B	C_{LOAD}=1nF, fsw = 400kHz
			66	80			C_{LOAD}=10nF, f_{SW} = 400kHz
Quiescent Current	I_{QCC}		1.8	2.2	mA		
Start-up Current	$I_{CC\ START}$		100	200	µA	V_{CC}=$V_{CC\ ON}$ - 0.1V	
Sleep Current	I_{SLEEP}		150	200	µA	V_{EN}=0V, V_{CC} =15V	
Enable Voltage High	V_{ENHI}	2.25	2.75	3.1	V		
Enable Voltage Low	V_{ENLO}	1.3	1.6	1.9	V		
Enable Pull-up Resistance	R_{EN}		1.5		MΩ	GBD	

Comparator Section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Turn-off Threshold	V_{TH1}	-7	-3.5	0	mV	OVT = 0V, V_S=0V
		-15	-10.5	-7		OVT floating, V_S=0V
		-23	-19	-15		OVT = V_{CC}, V_S=0V
Turn-on Threshold	V_{TH2}	-150		-50	mV	
Hysteresis	V_{HYST}		55		mV	
Input Bias Current	I_{IBIAS1}		1	7.5	µA	V_D = -50mV
Input Bias Current	I_{IBIAS2}		30	100	µA	V_D = 200V
Comparator Input Offset	V_{OFFSET}			2	mV	GBD
Input CM Voltage Range	V_{CM}	-0.15		2	V	

One-Shot Section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Blanking pulse duration	t_{BLANK}	10	15	20	µs	
Reset Threshold	V_{TH3}		2.5		V	V_{CC}=10V - GBD
			5.4		V	V_{CC}=20V - GBD
Hysteresis	V_{HYST3}		40		mV	V_{CC}=10V - GBD

Minimum On Time Section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Minimum on time	T_{ONmin}	190	240	290	ns	R_{MOT} =5kΩ, V_{CC}=12V
		2.4	3	3.6	µs	R_{MOT} =75kΩ, V_{CC}=12V

Minimum On Time Section

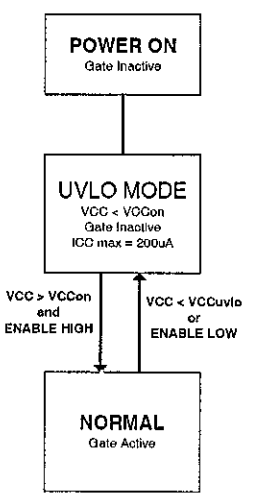
Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Minimum on time	T_{ONmin}	190	240	290	ns	R_{MOT} =5kΩ, V_{CC}=12V
		2.4	3	3.6	µs	R_{MOT} =75kΩ, V_{CC}=12V

Gate Driver Section

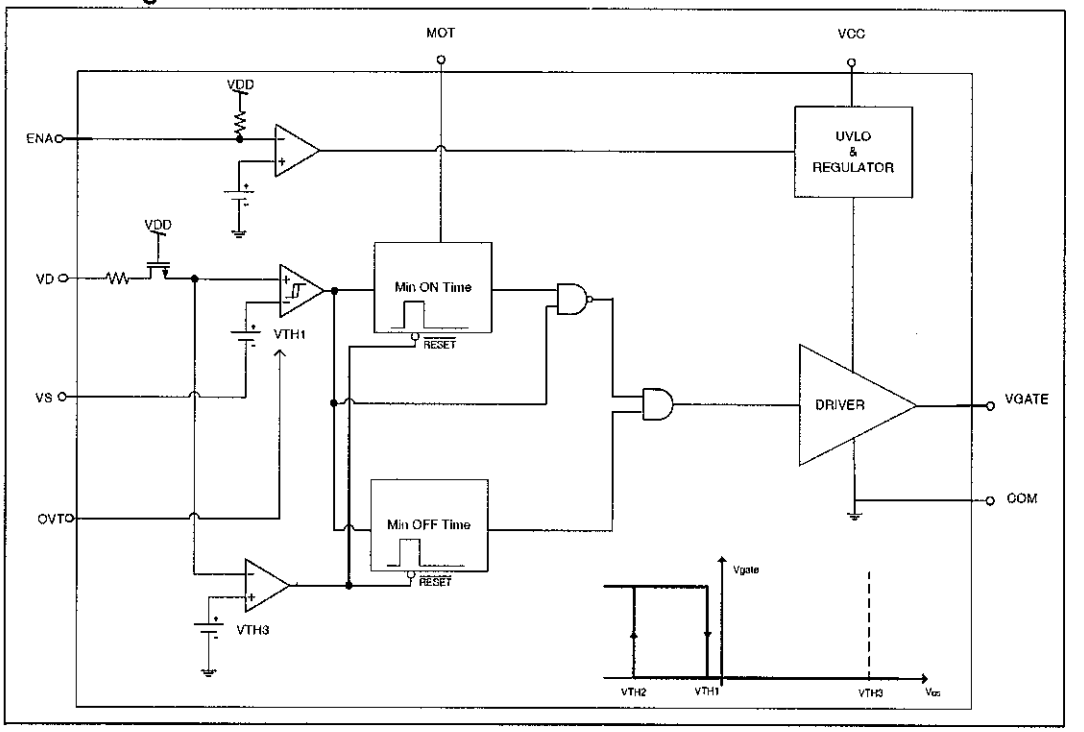
Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Gate Low Voltage	V_{GLO}		0.3	0.5	V	I_{GATE} = 200mA
Gate High Voltage	V_{GTH}	9.5	10.7	12.5	V	IR1167A - V_{CC}=12V-18V (internally clamped)
Gate High Voltage	V_{GTH}	12.5	14.5	16.5	V	IR1167B - V_{CC}=12V-18V (internally clamped)
Rise Time	t_{r1}		18		ns	C_{LOAD} = 1nF, V_{CC}=12V
	t_{r2}		125		ns	C_{LOAD} = 10nF, V_{CC}=12V
Fall Time	t_{f1}		10		ns	C_{LOAD} = 1nF, V_{CC}=12V
	t_{f2}		30		ns	C_{LOAD} = 10nF, V_{CC}=12V
Turn on Propagation Delay	t_{Don}		60	80	ns	V_{DS} to V_{GATE} -100mV overdrive
Turn off Propagation Delay	t_{Doff}		40	65	ns	V_{DS} to V_{GATE} -100mV overdrive
Pull up Resistance	r_{up}		4		Ω	I_{GATE} = 1A - GBD
Pull down Resistance	r_{down}		0.7		Ω	I_{GATE} = -200mA
Output Peak Current (source)	$I_{O\ source}$		2		A	C_{LOAD} = 10nF - GBD
Output Peak Current (sink)	$I_{O\ sink}$		7		A	C_{LOAD} = 10nF - GBD

** Guaranteed by Design

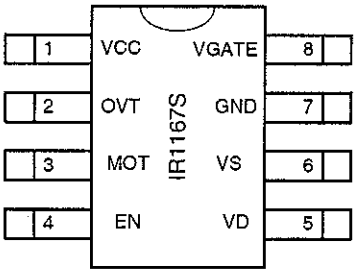
STATE AND TRANSITIONS DIAGRAM



Block Diagram



Lead Assignments & Definitions



Pin#	Symbol	Description
1	VCC	Supply Voltage
2	OVT	Offset Voltage Trimming
3	MOT	Minimum On Time
4	EN	Enable
5	VD	FET Drain Sensing
6	VS	FET Source Sensing
7	GND	Ground
8	GATE	Gate Drive Output

Detailed Pin Description

GND: Ground
This is ground potential pin of the integrated control circuit. The internal devices and gate driver are referenced to this point.

MOT: Minimum On Time
The MOT programming pin controls the amount of minimum on time. Once V_{TH2} is crossed for the first time, the gate signal will become active and turn on the power FET. Spurious ringings and oscillations can trigger the input comparator off. The MOT blanks the input comparator keeping the FET on for a minimum time.
The MOT is programmed between 200ns and 3us (typ.) by using a resistor referenced to GND.

OVT: Offset Voltage Trimming
The OVT pin will program the amount of input offset voltage for the turn-off threshold V_{TH1}.
The pin can be optionally tied to ground, to VCC or left floating, to select 3 ranges of input offset trimming. This programming feature allows for accomodating different RDSon MOSFETs.

GATE: Gate Drive Output
This is the gate drive output of the IC. Drive voltage is internally limited and provides 2A peak source and 5A peak sink capability. Although this pin can be directly connected to the power MOSFET gate, the use of minimal gate resistor is recommended, expecially when putting multiple FETs in parallel.
Care must be taken in order to keep the gate loop as short and as small as possible in order to achieve optimal switching performance.

VS: Source Voltage Sense
VS is the differential sense pin for the power MOSFET Source. This pin must not be connected directly to the power ground pin (7) but must be used to create a kelvin contact as close as possible to the power MOSFET source pin.

VD: Drain Voltage Sense
VD is the voltage sense pin for the power MOSFET Drain. This is a high voltage pin and particular care must be taken in properly routing the connection to the power MOSFET drain.
Additional filtering and or current limiting on this pin is not recommended as it would limit switching performance of the IC.

VCC: Power Supply
This is the supply voltage pin of the IC and it is monitored by the under voltage lockout circuit. It is possible to turn off the IC by pulling this pin below the minimum turn off threshold voltage, without damage to the IC.
To prevent noise problems, a bypass ceramic capacitor connected to Vcc and GND should be placed as close as possible to the IR1167S.
This pin is internally clamped.

EN: Enable
This pin is used to activate the IC "sleep" mode by pulling the voltage level below 2.5V (typ). In sleep mode the IC will consume a minimum amount of current. However all switching functions will be disabled and the gate will be inactive.

STATES OF OPERATION

UVLO/Sleep Mode

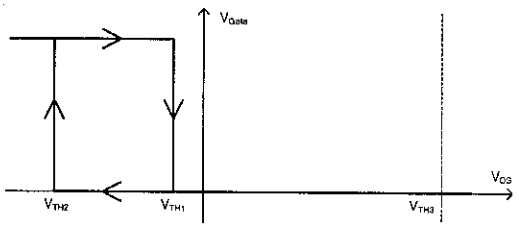
The IC remains in the UVLO condition until the voltage on the VCC pin exceeds the VCC turn on threshold voltage, $V_{CC\ ON}$.
During the time the IC remains in the UVLO state, the gate drive circuit is inactive and the IC draws a quiescent current of $I_{CC\ START}$. The UVLO mode is accessible from any other state of operation whenever the IC supply voltage condition of VCC < $V_{CC\ UVLO}$ occurs.
The sleep mode is initiated by pulling the EN pin below 2.5V (typ). In this mode the IC is essentially shut down and draws a very low quiescent supply current.

Normal Mode

The IC enters in normal operating mode once the UVLO voltage has been exceeded. At this point the gate driver is operating and the IC will draw a maximum of I_{CC} from the supply voltage source.

GENERAL DESCRIPTION

The IR1167 Smart Rectifier IC can emulate the operation of diode rectifier by properly driving a Synchronous Rectifier (SR) MOSFET.
The direction of the rectified current is sensed by the input comparator using the power MOSFET R_{DSon} as a shunt resistance and the GATE pin of the MOSFET is driven accordingly.
Internal blanking logic is used to prevent spurious transitions and guarantee operation in continuous (CCM), discountinuous (DCM) and critical (CrCM) conduction mode.



Input comparator thresholds

The modes of operation for a Flyback circuit differ mainly for the turn-off phase of the SR switch, while the turn-on phase of the secondary switch (which correspond to the turn off of the primary side switch) is identical.

Turn-on phase

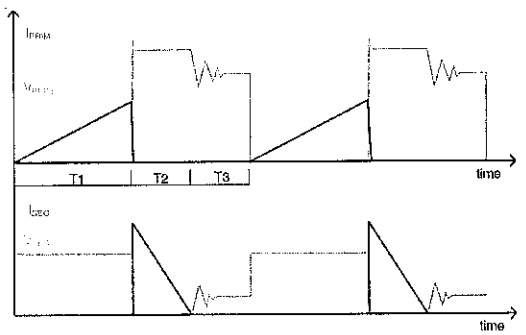
When the conduction phase of the SR FET is initiated, current will start flowing through its body diode, generating a negative V_{DS} voltage across it. The body diode has generally a much higher voltage drop than the one caused by the MOSFET on resistance and therefore will trigger the turn-on threshold V_{TH2}.
At that point the IR1167 will drive the gate of MOSFET on which will in turn cause the conduction voltage V_{DS} to drop down. This drop is usually accompained by some amount of ringing, that can trigger the input comparator to turn off; hence, a Minimum On Time (MOT) blanking period is used that will maintain the power MOSFET on for a minimum amount of time.
The programmed MOT will limit also the minimum duty

cycle of the SR MOSFET and, as a consequence, the max duty cycle of the primary side switch.

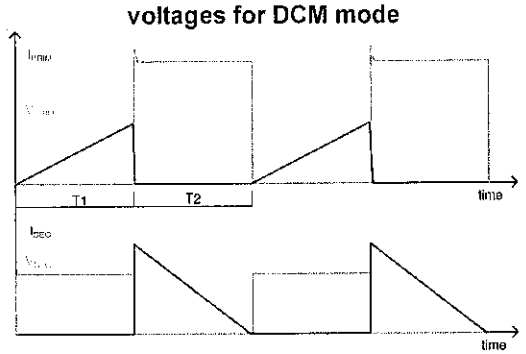
DCM/CrCM Turn-off phase

Once the SR MOSFET has been turned on, it will remain on until the rectified current will decay to the level where V_{DS} will cross the turn-off threshold V_{TH1}. This will happen differently depending on the mode of operation.

In DCM the current will cross the threshold with a relatively low dI/dt. Once the threshold is crossed, the current will start flowing again through the body diode,



Primary and secondary currents and voltages for DCM mode



Primary and secondary currents and voltages for CrCM mode

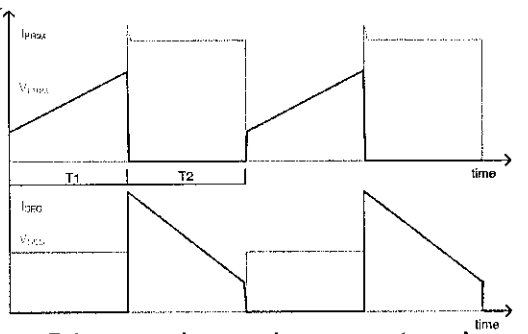
causing the V_{DS} voltage to jump negative. Depending on the amount of residual current, V_{DS} may trigger once again the turn on threshold: for this reason V_{TH2} is blanked for a certain amount of time (T_{BLANK}) after V_{TH1} has been triggered.

The blanking time is internally set. As soon as V_{DS} crosses the positive threshold V_{TH3} also the blanking time is terminated and the IC is ready for next conduction cycle.

CCM Turn-off phase

In CCM mode the turn off transition is much steeper and dI/dt involved is much higher. The turn on phase is identical to DCM or CrCM and therefore won't be repeated here.

During the SR FET conduction phase the current will decay linearly, and so will VDS on the SR FET.

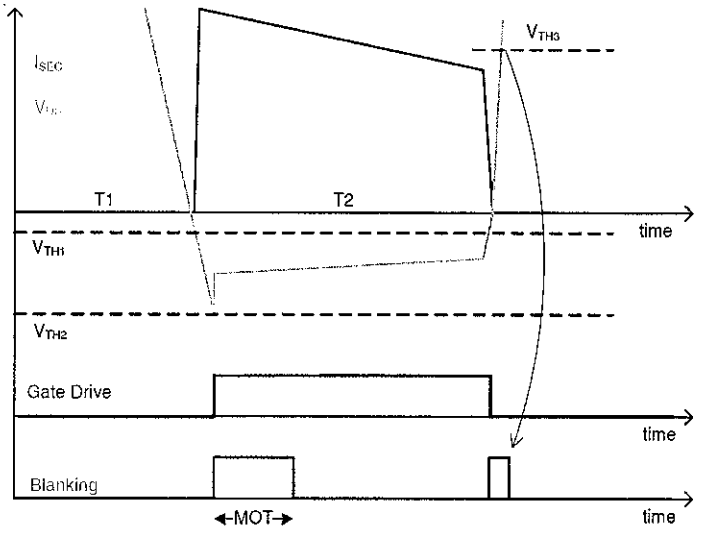


Primary and secondary currents and voltages for CCM mode

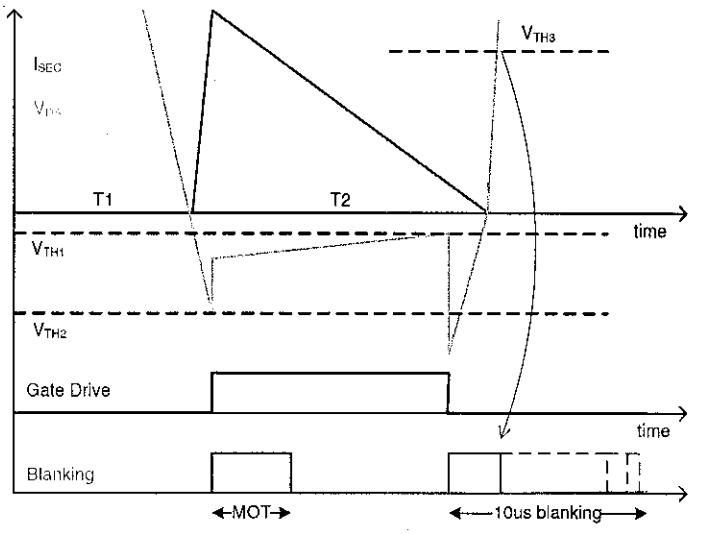
Once the primary switch will start to turn back on, the SR FET current will rapidly decrease crossing V_{TH1} and turning the gate off.

The turn off speed is critical to avoid cross conduction on the primary side and reduce switching losses.

also in this case a blanking period will be applied, but given the very fast nature of this transition, it will be reset as soon as V_{DS} crosses V_{TH3}.



Secondary side CCM operation



Secondary side DCM/CrCM operation

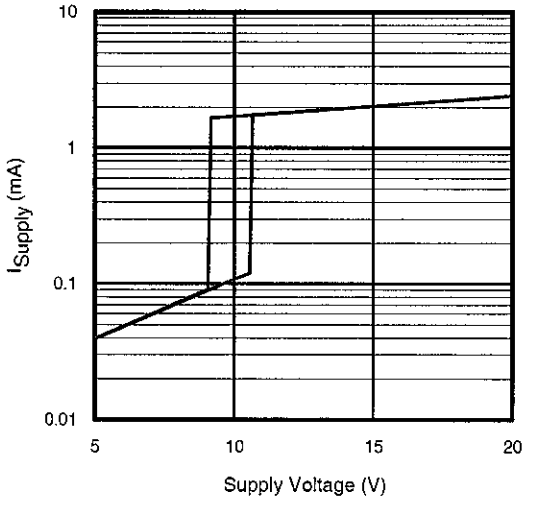


Fig 1. Supply Current vs. Supply Voltage

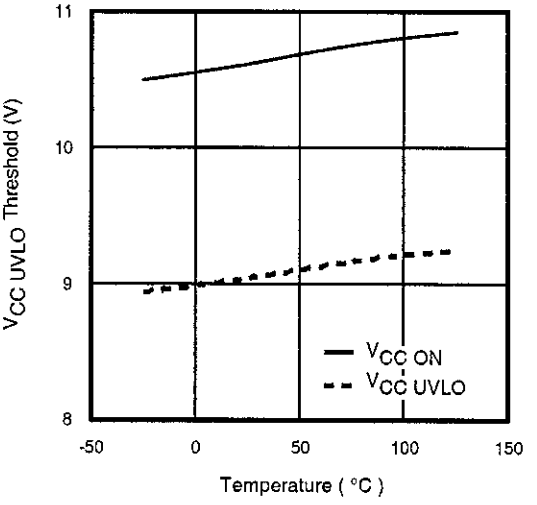


Fig 2. Under Voltage Lockout vs. Temp.

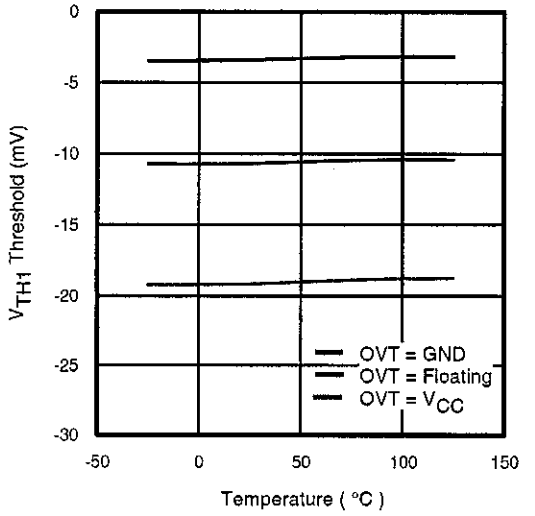


Fig 3. V_{TH1} vs. Temp.

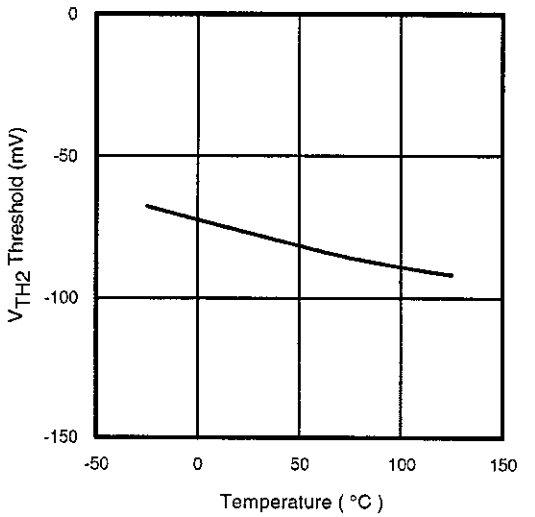


Fig 4. V_{TH2} vs. Temp.

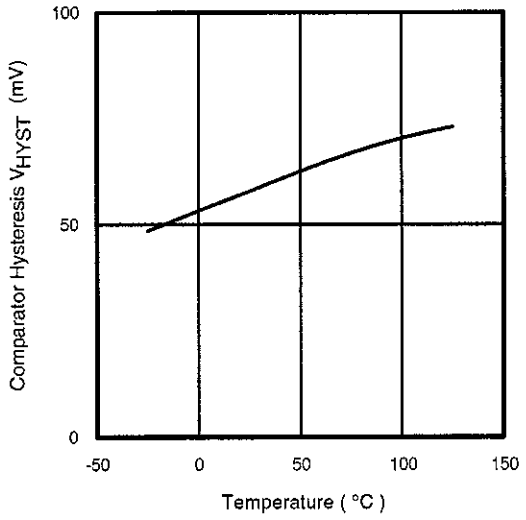


Fig 5. Comparator Hysteresis vs. Temp.

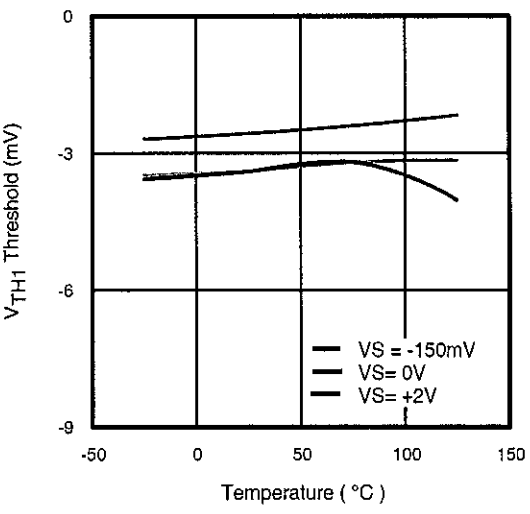


Fig 6. V_{TH1} vs. Temp. and Common Mode (OVT=GND)

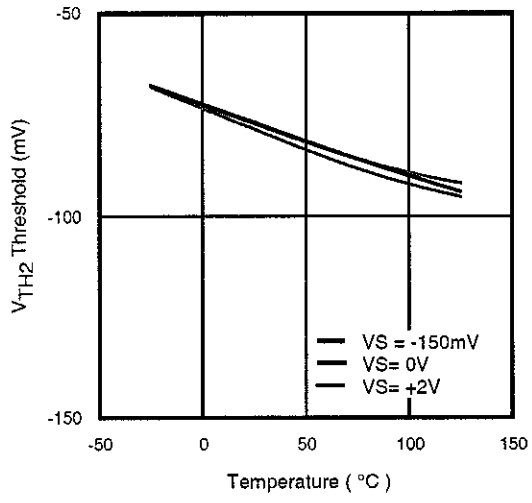


Fig 7. V_{TH2} vs. Temp. and Common Mode (OVT=GND)

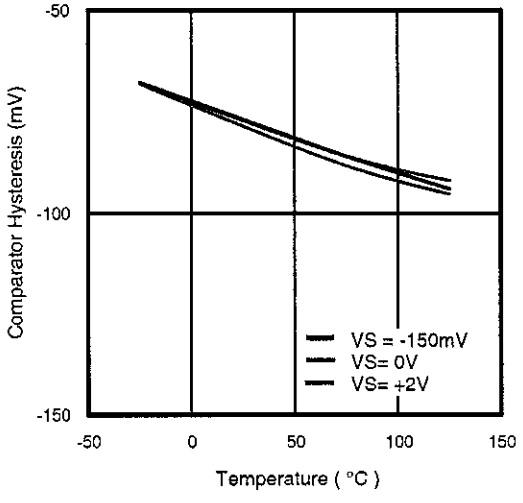


Fig 8. Comparator Hysteresis vs. Temp. and Common Mode (OVT=GND)

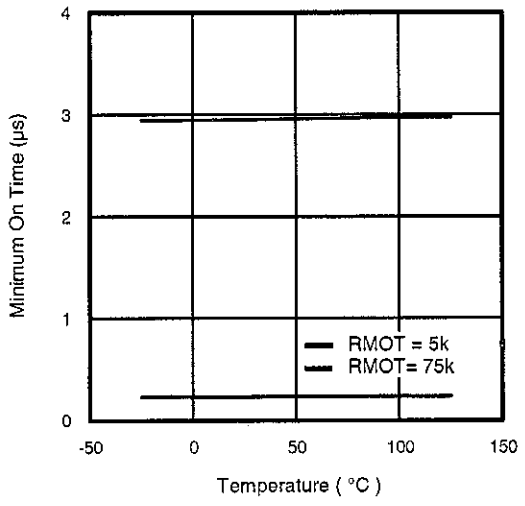


Fig 9. MOT vs. Temp.

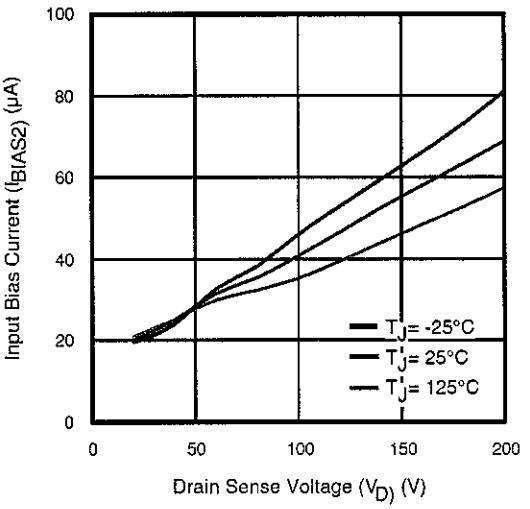


Fig 10. Input Bias Current vs. V_D.

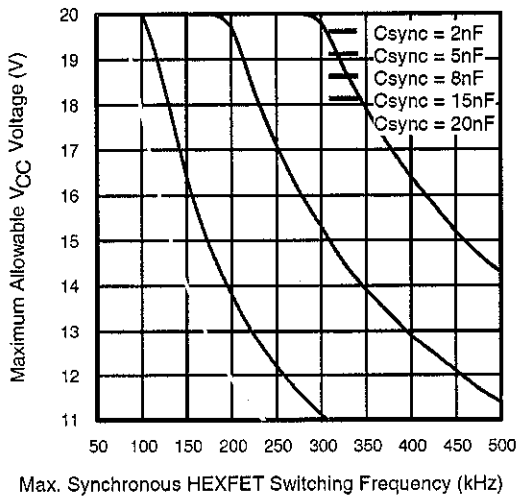


Fig 11. Max. V_{CC} Voltage vs. Synchronous Rectifier Switching Freq, T_J=125°C, T_{IC} = 85°C, external R_G=1Ω, 1Ω HEXFET Gate Resistance included

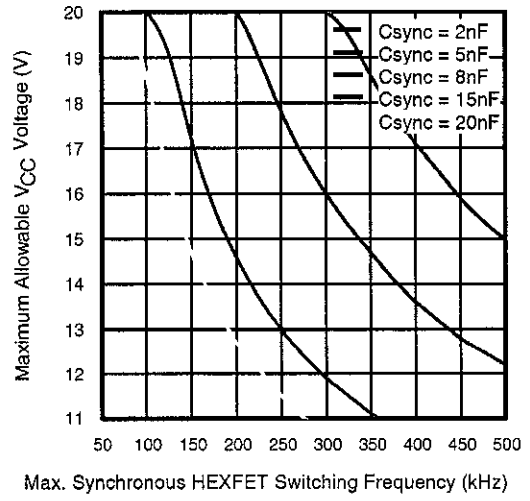


Fig 12. Max. V_{CC} Voltage vs. Synchronous Rectifier Switching Freq, T_J=125°C, T_{IC} = 85°C, external R_G=2Ω, 1Ω HEXFET Gate Resistance included

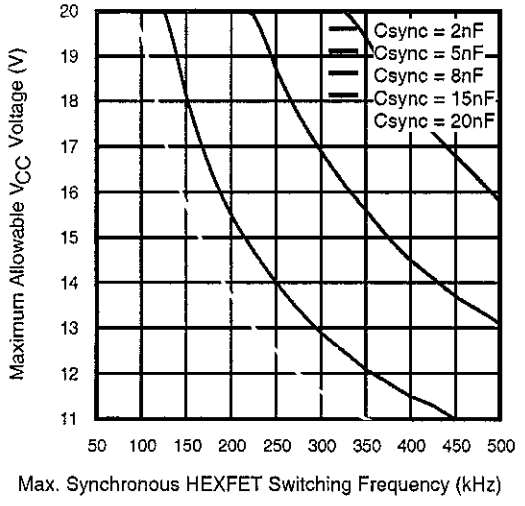


Fig 13. Max. V_{CC} Voltage vs. Synchronous Rectifier Switching Freq, T_J=125°C, T_{IC} = 85°C, external R_G=4Ω, 1Ω HEXFET Gate Resistance included

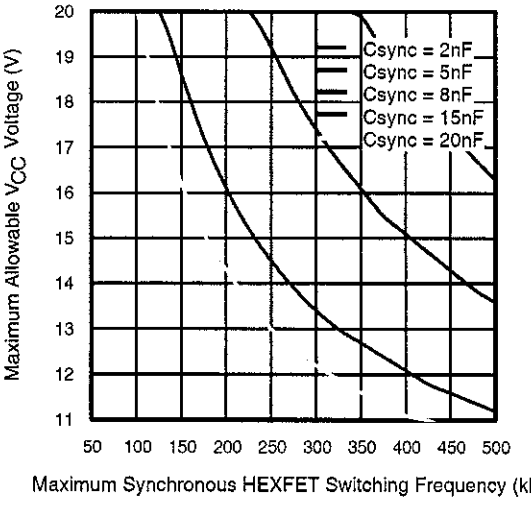


Fig 14. Max V_{CC} Voltage vs. Synchronous Rectifier Switching Freq, T_J=125°C, T_{IC} = 85°C, external R_G=6Ω, 1Ω HEXFET Gate Resistance included

Figures 11-14 shows the maximum allowable V_{CC} voltage vs. maximum switching frequency for different loads which are calculated using the design methodology discussed in AN1087.

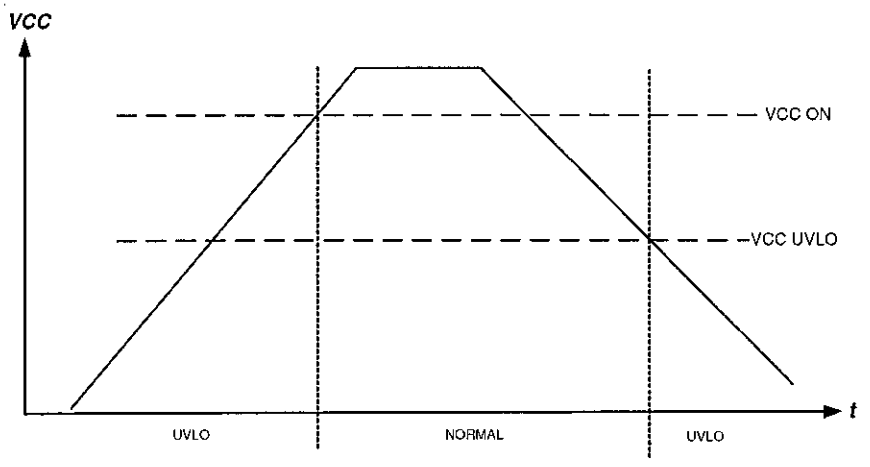


Fig. 14 - V_{cc} Under Voltage Lockout

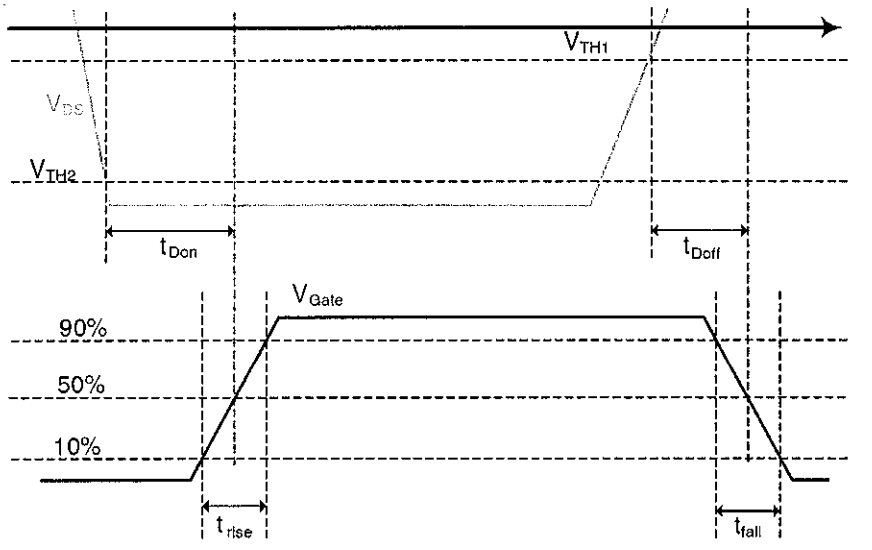
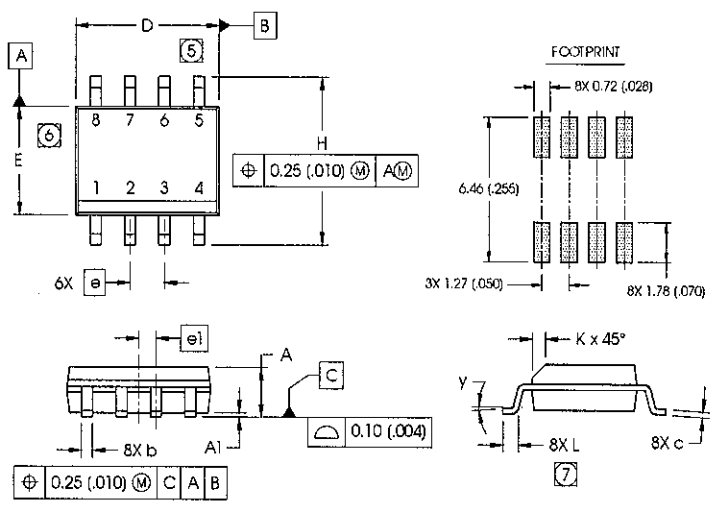


Fig. 15 - Timing Diagrams

Case outline



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

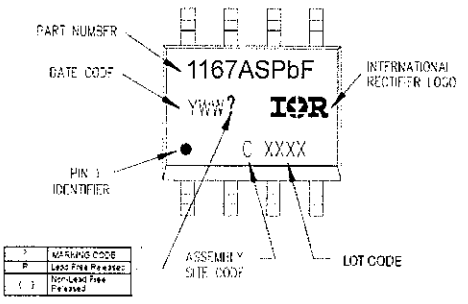
NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 (.006).
6 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 (.010).
7 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

01-6027
01-0021 11 (MS-012AA)

8-Lead SOIC

TOP MARKING (LASER)



Data and specifications subject to change without notice.
Qualification Standards can be found on IR's Web site.