HARDWARE IMPLEMENTATION OF A MINIMALLY COMPLEX RFID BASED DATA RETRIEVAL SYSTEM

By

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FINAL PROJECT REPORT

Submitted to the Electrical & Electronics Engineering Programme
in Partial Fulfillment of the Requirements
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(Electrical & Electronics Engineering)

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CERTIFICATION OF APPROVAL

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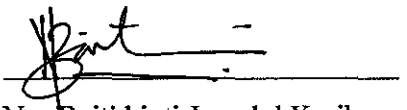
JUNE 2008

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.



Nur Baiti binti Jamalul Karib

ABSTRACT

The topic of this project is 'Hardware Implementation of a Minimally Complex RFID Based Data Retrieval System'. Data retrieving has now become a need in our daily life. The focus of this project is on designing the data retrieval system and hardware implementation of the designed system. This project is then proceed to the stage of testing the data retrieval system that has been implemented. In this project, the circuit is designed to be built by using digital circuits. The circuit is divided into small parts according to their functions such as the update control logic, search control logic, reset control logic and the memory. Data retrieval system has a very wide range of applications. The data retrieval system in the library is used as the example of data retrieval system application in designing the system for this project. In this project, the data retrieval system builds to take the input from the RFID reader. RFID stands for Radio Frequency Identification. It is a technology that is using electromagnetic signals. RFID has a wide range of applications such as in a security system, items storage systems in factories and hypermarkets, books storage system in the libraries and many more. RFID has a lot of advantages as compared to the barcodes systems.

ACKNOWLEDGEMENTS

I would like to express my greatest gratitude towards The Almighty for giving me the strength to complete my Final Year Project. I would also like to thank my project supervisors, Dr. Nor Hisham Hamid and Mr. Ho Tatt Wei who have been so great and really helpful to me. Thanks to a friend of mine, Mohd Shahrul Zharif bin Shaharuddin, who had shared his knowledge and thus contributing to this project. To my family, thank you for being supportive and to all my friends who have given me their opinions through out completing this project.

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1. UPC – Universal Product Code
2. RFID – Radio Frequency Identification
3. K-Maps - Karnaugh Maps
4. LED – Light Emitting Diode
5. FYP – Final Year Project

CHAPTER 1
INTRODUCTION

'Hardware Implementation of a Minimally Complex RFID Based Data Retrieval System' is a project on building a data retrieval system which can contribute in data retrieving process.

1.1 Background of Study

As the technologies continue to grow, a lot of devices and systems are implemented to make our day to day life better each day. Data retrieving is a need in human life nowadays. Data of a particular thing can be stored in the memory of its system. The purpose of this is definitely to enable people to access the information on that particular thing easily. A data retrieval system should be efficient enough so that the users can get the information in a good condition. In this project, the data retrieval system is built to take the input from the RFID reader. Logic gates are used in implementing the circuits. Knowledge on digital electronics is crucial and basic understanding of RFID would definitely be helpful.

1.2 Problem Statement

The main purpose of this project is to build a RFID based data retrieval system. This project will focus mainly on the hardware implementation for this system. It is a simple system that is expected to be able to perform basic operations of a data retrieval system. The data retrieval system build in this project takes the library data retrieval

system as its application. Data retrieval system is build to make information to be accessible. By building data retrieval system, data can be stored and managed in a proper way. A part from that, the most important thing is the information can easily be accessed by the users.

Data retrieval system has a very wide range of applications such as books storage system in the libraries, data of items in the supermarkets and factories, and many more. Taking the books storage system in a library as an example, the data retrieval system will need to have enough memory space. The amount of data that can be stored depends on the memory size of this particular system. A big memory size is needed to store a large number of data. A part from that, an acceptable access time of the system is also important. This will ensure the system is reliable for the users. This books storage system also needs a subsystem to update the data that has been stored in its memory. When a book is borrowed or returned to the library, this system will change the data on the amount of that particular book accordingly in its memory.

1.2.1 Significance of the Project

The circuit that is implemented in this project a simple circuit of a data retrieval system. For a start, this circuit can be used in future digital electronics classes. It will be a good introduction to digital electronics circuits' applications for the students. Further improvement done on this project in the future, might lead to a wider range of applications for this project.

1.3 Objectives

The objective of this project is:

- Design a circuit to take data from RFID input and compare with the data in the memory.

1.4 Scope of Study

The scope of this project is to design a data retrieval system using discrete logic gates and RFID reader as the input device. The circuit that has been designed is then implemented using the hardware that has been determined in the designing stage. As the hardware has been implemented, the circuit is then tested.

CHAPTER 2
LITERATURE REVIEW AND THEORY

As stated earlier, the library data retrieval system is used as the reference in designing this system. Most of the libraries use either barcodes system or the RFID as the input device. Thus, some literature review has been done on both barcodes system and the RFID system.

2.1 Barcodes

Barcodes is one of information representations where the information can be read by a machine known as the barcodes reader. Data in the barcodes are stored in the width and spacing of the printed parallel lines. Barcodes are widely used to implement auto ID data capture systems resulting in improvement of the speed and accuracy of computer data entry.

Barcodes reader usually completed with a light source, a lens and a photo conductor translating optical impulses into electrical impulses. Most of the barcodes readers contain decoder circuitry. This decoder is used in analyzing the barcode's image data provided by the photo conductor and send the data to the output device.

2.1.1 UPC barcodes

"UPC" is an abbreviation for Universal Product Code. It is the most common and widely use barcodes. The UPC barcodes consist of two parts; machine-readable barcode and 12-digit UPC number that can be read by human.

Figure 1 : UPC barcodes

2.2 RFID

RFID is abbreviation for Radio Frequency Identification. It is a wireless technology to detect items. The signals that are transmitted by RFID are electromagnetic signals. RFID system usually built up by a scanning antenna which is use to detect the RFID tag, a transceiver that is completed with decoder to interpret the data, and a transponder or the RFID tag. Data of a particular thing is programmed in the RFID tag.

2.2.1 RFID tags

There are various kinds of RFID tags. One of them is passive RFID tag which has an antenna that can act as a coil to generate electric current in an electromagnetic field that is produce by the RFID reader. An electromagnetic pulse will then be transmitted back to the reader. Another kind of RFID tag is an active RFID tag which has an internal

power source. An active RFID tag transmits its signal to the receiver on the specified frequency. The RFID tags consist of three parts; chip, antenna and packaging.

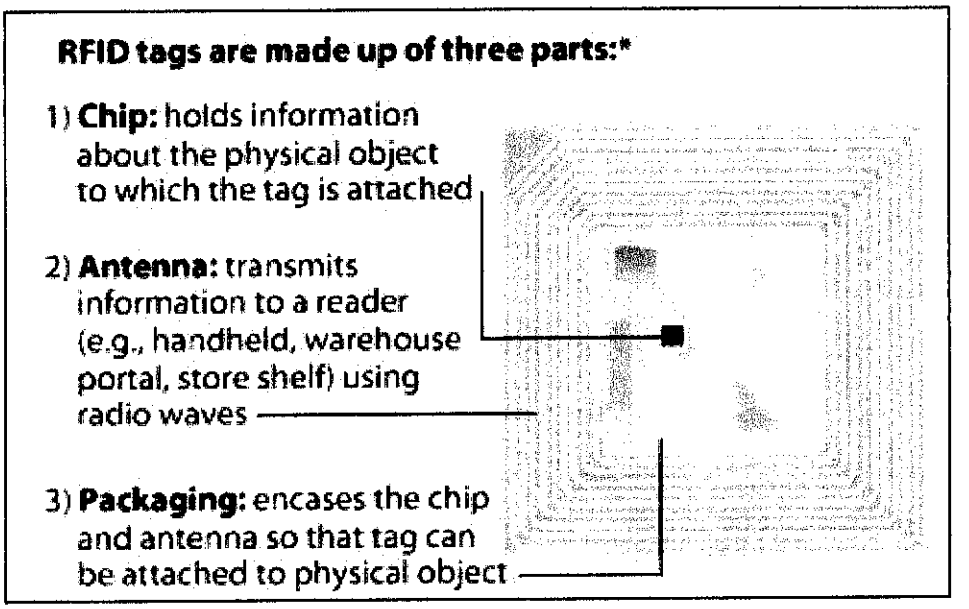

Figure 2 : RFID Tag

2.3 RFID advantages over barcodes

The advantages of using RFID compared to the barcodes are the RFID tag can be hidden inside the items and the detection can be done at a greater distance than the barcodes. The detection process of the RFID tag is less than 100 milliseconds. Scanning process and data logging for RFID system can be done automatically without additional human involvement. More data can be stored in the RFID tag compared to the barcodes. A large number of the RFID tags can be read at once rather than detecting them item by item.

For security purpose, the RFID tag can trigger alarm systems if the item is removed from its correct location. The RFID tags are programmable with read and write storage where each of them is uniquely serialized. Thus, the item can be detected if it is lost or stolen so that further action can be done as soon as it is identified.

Even though the RFID is a more sophisticated system compared to the barcodes system, the RFID system has more capability. Considering the advantages that the RFID system holds over the barcode system, it is decided that this project will be designed to take the input from the RFID. This will certainly add the value on this project.

CHAPTER 3
METHODOLOGY

This methodology section will briefly show the pre-determined steps in completing this project.

3.1 Procedure Identification

The flow chart shown below is part of the project completion process for FYP.

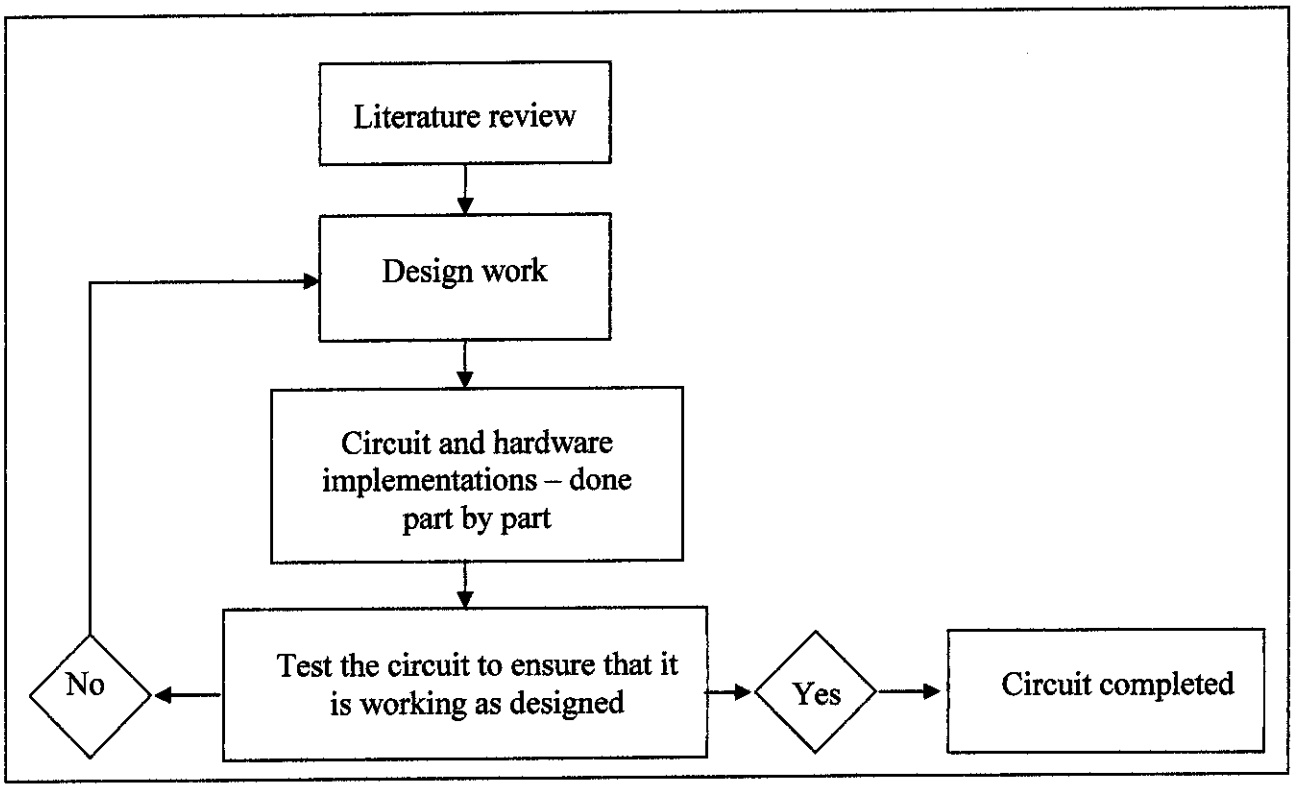

Figure 3 : Flow chart of methodology

Figure 3 shows the general steps in completing this project. Below are the explanations on the steps.

3.1.1 Design Work

The first step taken was identifying the operation of the whole system. Then, the circuits needed in this system are designed. As the circuits have been designed, the ICs that will be used in the circuits are determined as well as the quantity of the ICs needed. This process is done on paper.

3.1.1.1 Overall system

The system is designed as shown in Figure 3 below.

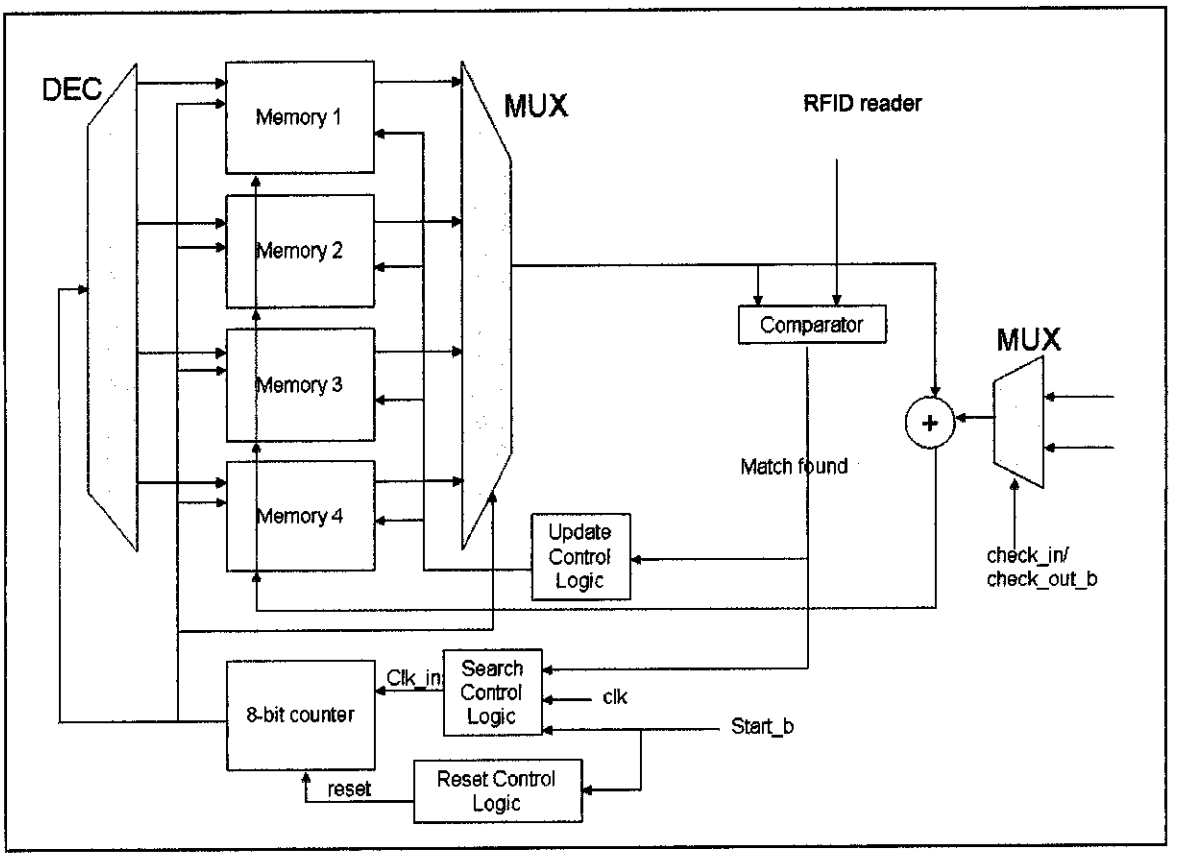

Figure 4 : Circuit Block Diagram

As the RFID sense the input signal, the comparator will compare the input data with the data available from the memory. When the match is found, the data will be sent to the update control logic and search control logic. The update control logic will update the data stored in the memory while the search control logic will retrieve data from the memory. From the search control logic, the input data is then sent to the 8-bit counter. The data will then go to the decoder and memory. The adder is used to add or subtract the data available in the memory.

Taking a library data retrieval system as the example, the operations of the system is simplified as in Figure 5 below.

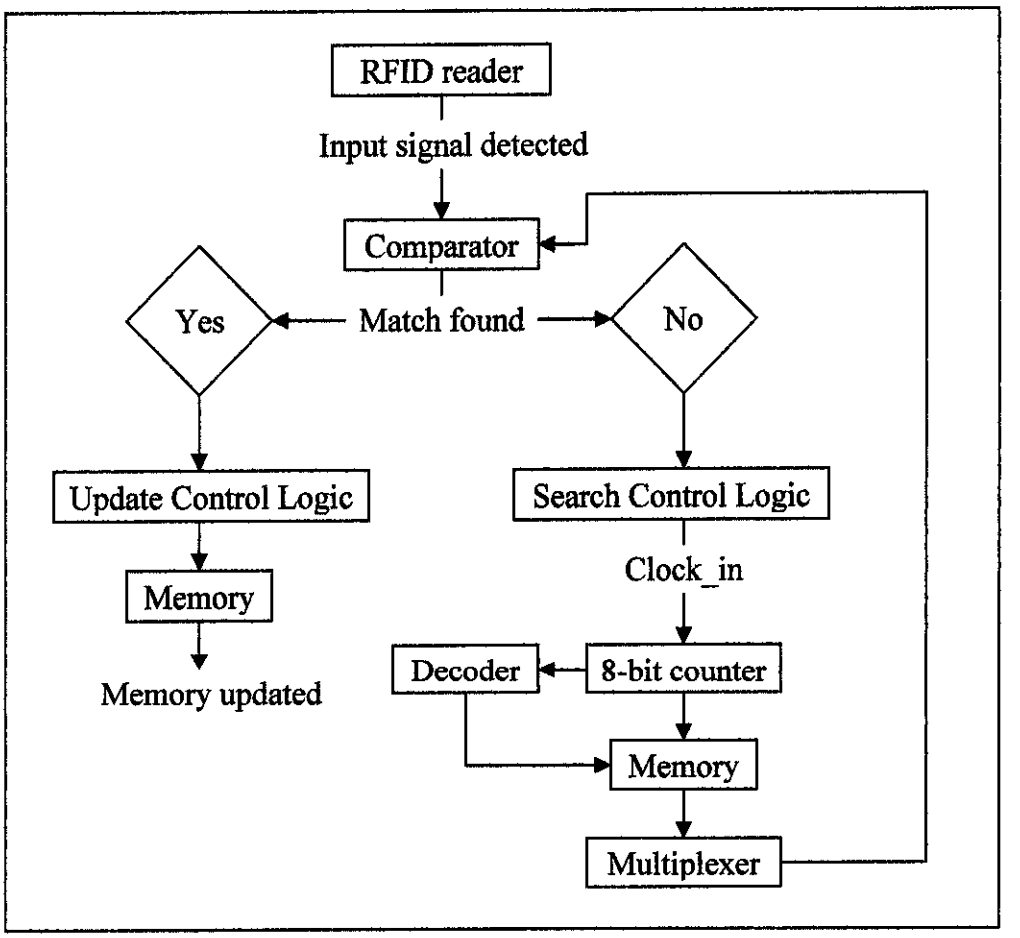

Figure 5 : Circuit Operation Flow Chart

3.1.1.2 States machine

In order to control the memory operations, a state machine has been designed. State machine is a model of computation for a complete cycle of a particular system. It consists of a finite number of states where each state represents its own condition that is call as its present state. Among those states, there are specified transitions which indicate the changes of the states. State machine is use to determine the next-state table. In order to find out the logic gates needed to perform a particular task in the system, state machine is very important.

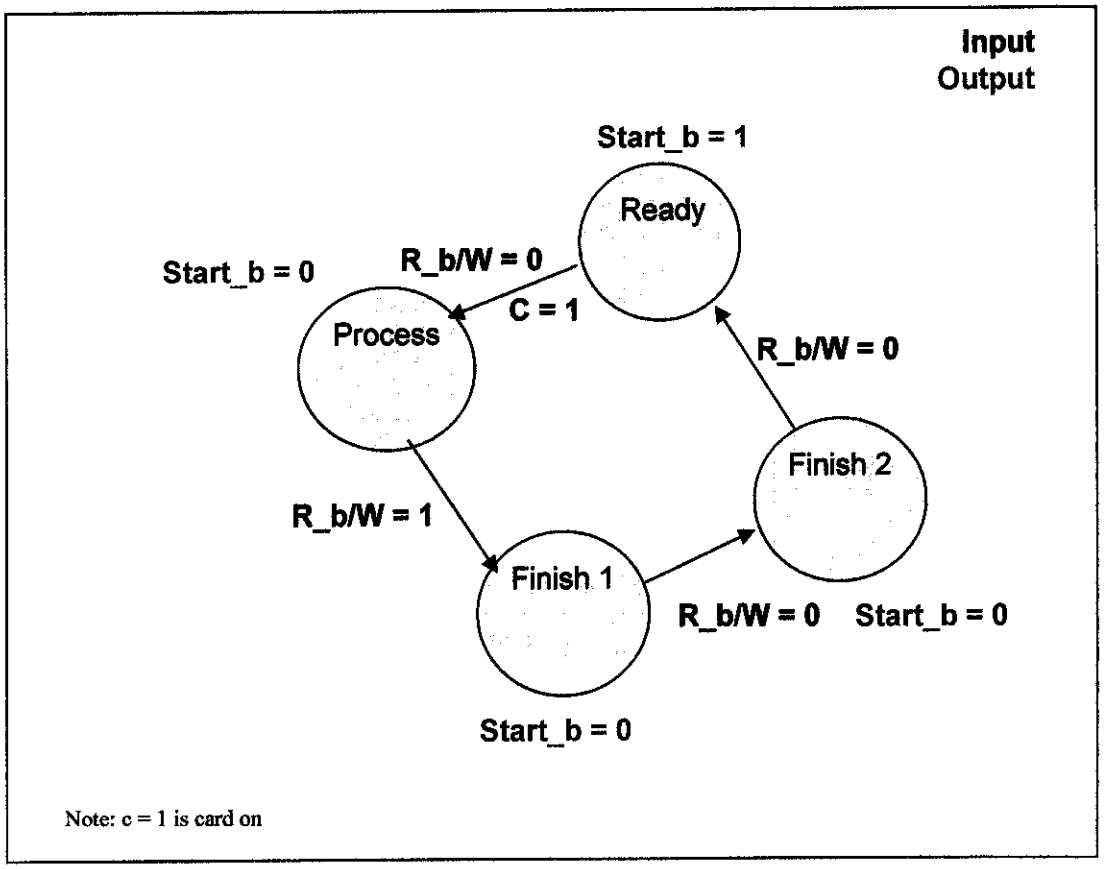

Figure 6 : State Machine Block Diagram

From the state machine, the next-state tables are constructed.

Table 1 : General Next-State Table for State Machines Diagram

INPUT		CURRENT STATE	NEXT STATE	B
C	M			
0	0	0 0	0 0	0
1	0	0 0	0 1	0
0	1	0 0	0 0	1
1	1	0 0	0 0	1
0	0	0 1	0 1	0
1	0	0 1	0 1	0
0	1	0 1	1 0	0
1	1	0 1	1 0	0
0	0	1 0	1 1	0
1	0	1 0	1 1	0
0	1	1 0	1 0	0
1	1	1 0	1 0	0
0	0	1 1	0 0	0
1	0	1 1	0 0	0
0	1	1 1	1 1	0
1	1	1 1	1 1	0

Table 2 : Next-State Table of Output Q_1' for State Machines Diagram

INPUT		Q_1	Q_2	Q_1'
C	M			
0	0	0	0	0
1	0	0	0	0
0	1	0	0	0
1	1	0	0	0
0	0	0	1	0
1	0	0	1	0
0	1	0	1	1
1	1	0	1	1
0	0	1	0	1
1	0	1	0	1
0	1	1	0	1
1	1	1	0	1
0	0	1	1	0
1	0	1	1	0
0	1	1	1	1
1	1	1	1	1

The K-Map is built from the above next-state table.

Table 3 : K-Map for Q_1'

Q_1'

Q_1Q_2 \ CM	00	01	11	10
00	0	0	0	0
01	0	1	1	0
11	0	1	1	0
10	1	1	1	1

From the K-Map above, the Boolean expression for Q_1' is obtained:

$$Q_1' = \overline{Q_1}\, Q_2\, \overline{C}\, M\, \overline{Q_1}\, Q_2\, C\, M\, Q_1\, Q_2\, \overline{C}\, M\, Q_1\, Q_2\, C\, M + Q_1\, \overline{Q_2}\, \overline{C}\, \overline{M}\, Q_1\, \overline{Q_2}\, \overline{C}\, M\, Q_1\, \overline{Q_2}\, C\, M\, Q_1\, \overline{Q_2}\, C\, \overline{M}$$

$$Q_1' = Q_2\, M + Q_1\, \overline{Q_2}$$

From the Boolean expression of the Q_1', the logic circuit is drawn:

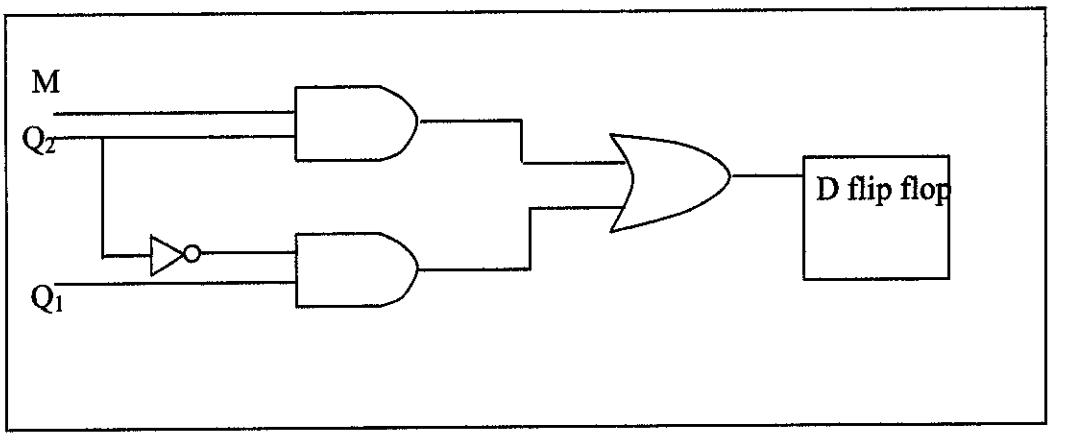

Figure 7 : Logic Circuit for Q_1'

The next-state table for Q_2' is identified.

Table 4 : Next-State Table of Output Q_2' for State Machines Diagram

INPUT		Q_1	Q_2	Q_2'
C	M			
0	0	0	0	0
1	0	0	0	1
0	1	0	0	0
1	1	0	0	0
0	0	0	1	1
1	0	0	1	1
0	1	0	1	0
1	1	0	1	0
0	0	1	0	1
1	0	1	0	1
0	1	1	0	0
1	1	1	0	0
0	0	1	1	0
1	0	1	1	0
0	1	1	1	1
1	1	1	1	1

The K-Map is built from the next-state table.

Q_2' Table 5 : K-Map for Q_2'

Q_1Q_2 \ CM	00	01	11	10
00	0	0	0	1
01	1	0	0	1
11	0	1	1	0
10	1	0	0	1

From the K-Map, the Boolean expression for Q_2' is obtained:

$$Q_2' = \overline{Q_1}\,\overline{Q_2}\,C\,\overline{M}\,\overline{Q_1}\,Q_2\,C\,\overline{M} + \overline{Q_1}\,Q_2\,\overline{C}\,\overline{M}\,\overline{Q_1}\,Q_2\,C\,\overline{M} + Q_1\,Q_2\,\overline{C}\,M\,Q_1\,Q_2\,C\,M + Q_1\,\overline{Q_2}\,\overline{C}\,\overline{M}\,Q_1\,\overline{Q_2}\,C\,\overline{M}$$

$$Q_2' = \overline{Q_1}\,C\,\overline{M} + \overline{Q_1}\,Q_2\,\overline{M} + Q_1\,Q_2\,M + Q_1\,\overline{Q_2}\,\overline{M}$$

From the Boolean expression of the Q_2', the logic circuit is drawn:

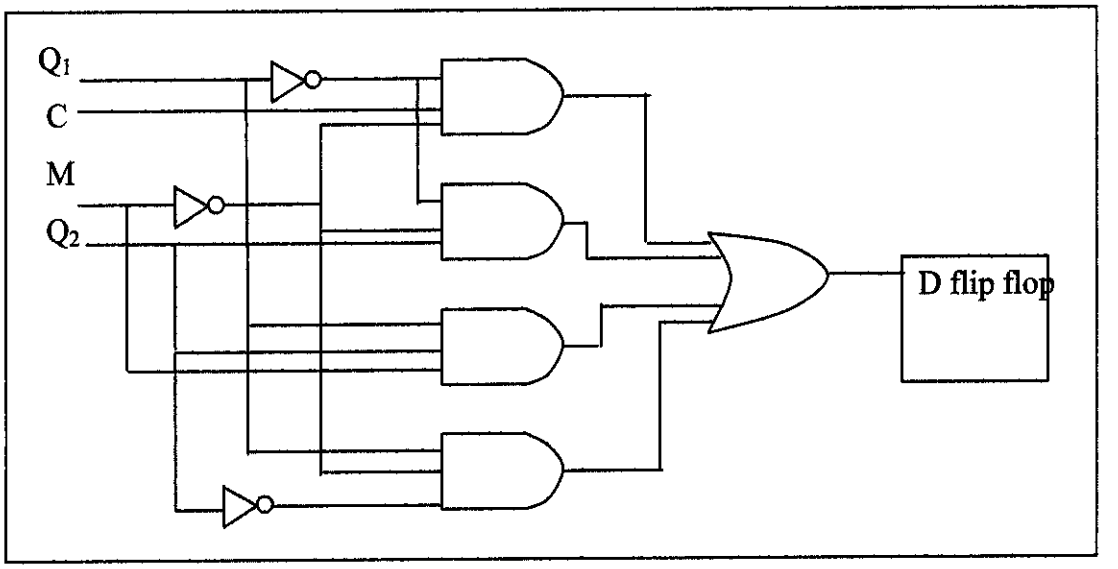

Figure 8 : Logic Circuit for Q_2'

The next-state table for output B is identified.

Table 6 : Next-State Table of Output B for State Machines Diagram

INPUT		Q_1	Q_2	B
C	M			
0	0	0	0	0
1	0	0	0	0
0	1	0	0	1
1	1	0	0	1
0	0	0	1	0
1	0	0	1	0
0	1	0	1	0
1	1	0	1	0
0	0	1	0	0
1	0	1	0	0
0	1	1	0	0
1	1	1	0	0
0	0	1	1	0
1	0	1	1	0
0	1	1	1	0
1	1	1	1	0

The K-Map is built from the next-state table.

B Table 7 : K-Map for B

Q_1Q_2 \ CM	00	01	11	10
00	0			0
01	0	0	0	0
11	0	0	0	0
10	0	0	0	0

From the K-Map, the Boolean expression for Q_2' is obtained:

$B = \overline{Q_1}\,\overline{Q_2}\,\overline{C}\,M\,\overline{Q_1}\,\overline{Q_2}\,C\,M$

$B = \overline{Q_1}\,\overline{Q_2}\,M$

From the Boolean expression of the B, the logic circuit is drawn:

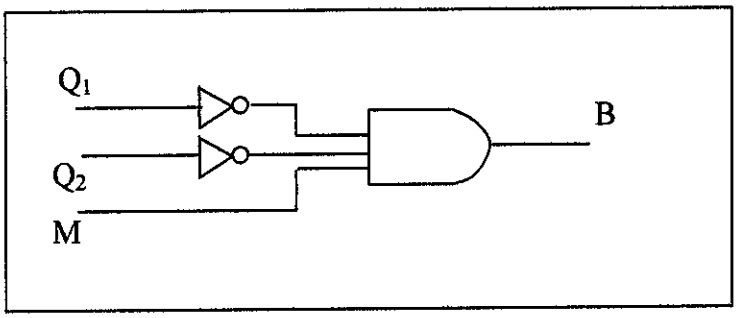

Figure 9 : Logic Circuit for B

The design of the overall circuit for this system is attached as Appendix A.

3.1.1.3 Reset control logic

Reset control logic is build to take the input from the states machine and reset the operations of the 8-bit counter. This is to ensure that each time the system has completed it's overall process, the 8-bit counter will not have the location of the data in the memory for the pervious operation. Thus, the 8-bit counter will be reset to its initial condition.

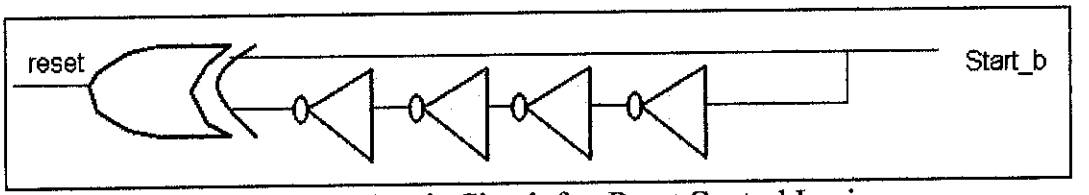

Figure 10 : Logic Circuit for Reset Control Logic

3.1.1.4 Search control logic

Search control logic is build to take the input from the comparator and the states machine and send the data into the 8-bit counter. The purpose of this search control logic is to determine the data from the memory which has the same identification with the input data sent by the RFID reader.

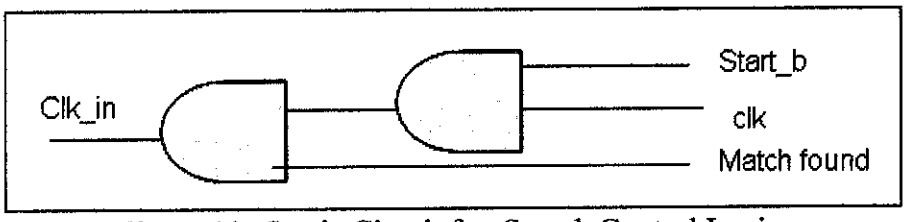

Figure 11 : Logic Circuit for Search Control Logic

3.1.1.5 Update control logic

Update control logic is build to update the data in the memory.

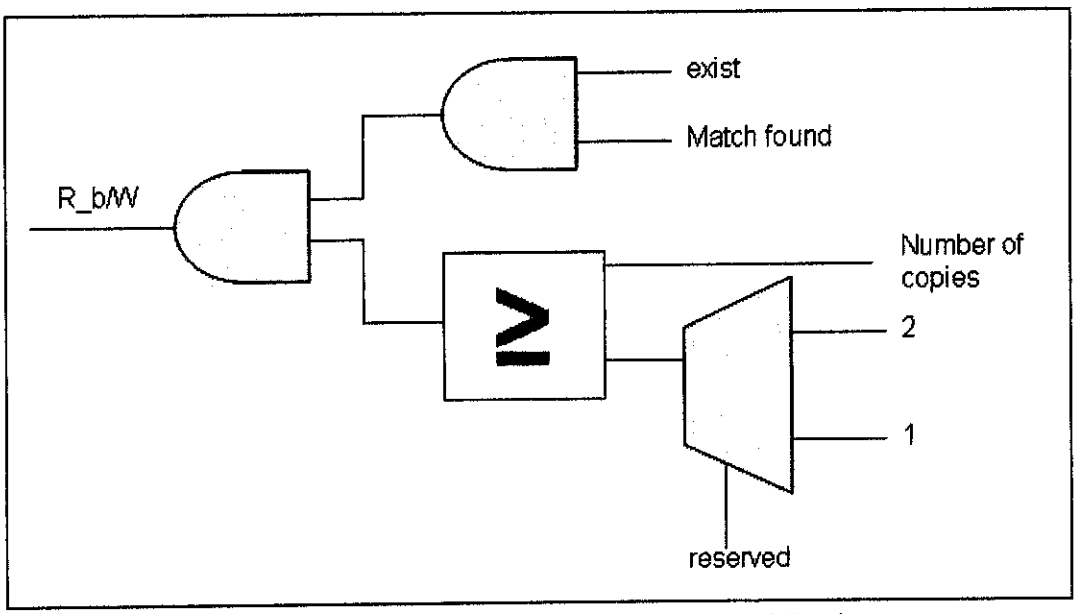

Figure 12 : Logic Circuit for Update Control Logic

3.1.2 Circuits and Hardware Implementations

As the design work has been completed, the next step will be the circuits and hardware implementations. In this step, the physical circuits and hardware will be assembled and connected as determined in the design work process. All the connections must be correctly done so that the system will work properly.

Before implementing the circuit, in order to ensure that the circuits that have been designed will be working as desired, a simulation of the designed circuit has been done with PSPICE. For the time being, the circuit that has been completely implemented is the circuit of the state machine. The overall circuit is divided into parts to make it easy to implement and test.

3.1.3 Testing the System

As each part of the overall circuit is completely build, each circuit will be tested to ensure that it is working as in the design. Though the circuit for the state machine has been built, the circuit is yet to be tested.

When all the hardware has been connected, the system will be tested. This is meant to ensure that the system is working and meet the objectives of this project. Corrections and improvements will be done through out this process.

3.2 Hardware Needed

As for the time being, the ICs that will be used in this project are listed below. Since the circuits are divided into few parts, the ICs needed are listed according to the circuits' part.

The ICs needed for the circuit of the state machines are:

- 1 DM74LS08 (4 x 2 input AND gates)
- 2 DM74LS11 (3 x 3 input AND gates)
- 1 DM74LS32 (4 x 2 input OR gates)
- 1 DM74LS74A (2 x D flip flop)
- 1 SN74LS04 (6 x NOT gates)

The ICs needed for the circuit of the reset control logic are:

- 1 SN74LS04 (6 x NOT gates)
- 1 SN74LS136 (4 x 2 input XOR gates)

The ICs needed for the circuit of the search control logic is:

- 1 DM74LS08 (4 x 2 input AND gates)

The ICs needed for the circuit of the update control logic are:

- 1 DM74LS08 (4 x 2 input AND gates)
- 1 DM74LS157 (4 x 2-1 multiplexer)

The ICs needed for the circuit for the over all circuits are:

- 1 DM74LS157 (4 x 2-1 multiplexer)
- 1 SN74LS153 (2 x 4-1 multiplexer)
- 1 SN74LS682 (comparator)
- 2 DM74LS283 (adder)
- 4 UT6264B (8 bit CMOS SRAM)

CHAPTER 4
RESULTS AND DISCUSSION

4.1 Results

As up to this time, the circuit that has been completely implemented is the circuit for the state machine. This circuit is built of 2 DM74LS11 (3 x 3 input AND gates), 1 DM74LS08 (4 x 2 input AND gates), 1 DM74LS32 (4 x 2 input OR gates), 1 SN74LS04 (6 x NOT gates) and 1 DM74LS74A (2 x D flip flop).

The state machine is designed in such way because that is the least states that can be obtained without violating the conditions that are desired to be fulfilled. The circuit of this state machine has been tested. In testing the circuit, 5 LEDs are used to indicate the circuit is working as stated in the next state table. 2 LEDs are connected to Q_1 and Q_2 respectively before the D flip-flop, 2 LEDs are connected to Q_1 and Q_2 respectively after the D flip-flop and another 1 LED is connected to indicate the output B.

Before testing the implemented circuit, a simulation using PSPICE has been done. The circuit simulated in the PSPICE is exactly the same as the circuit that has been designed to be implemented.

4.1.1 PSPICE Simulation Results

4.1.1.1 PSPICE Simulation Results for Q_1'

The output waveform for this simulation is high (1) by default. Refer to Table 2 and Figure 7;

Table 8 : Input-Output Table for Simulation 1

INPUT			OUTPUT
M	Q_1	Q_2	Q_1'
0	0	0	0

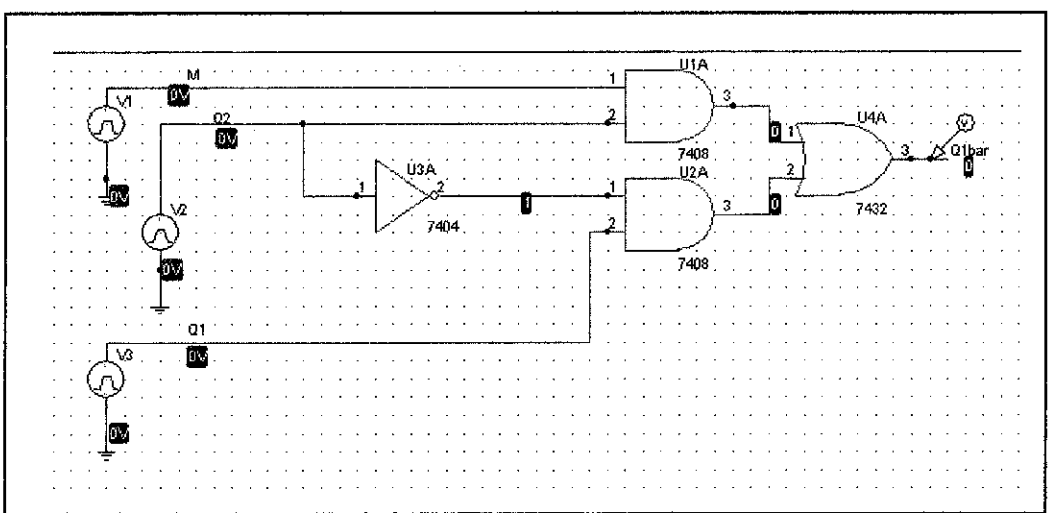

Figure 13 : Logic Circuit for Simulation 1

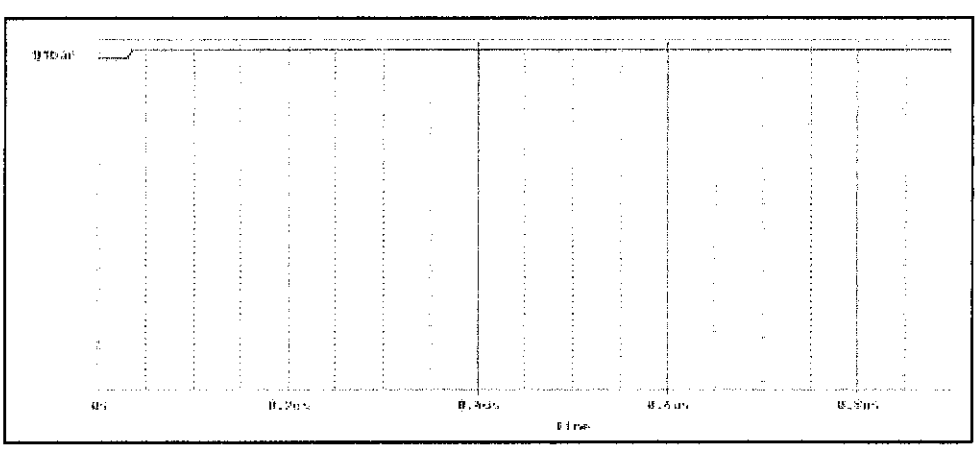

Figure 14 : Output Waveform for Simulation 1

Table 9 : Input-Output Table for Simulation 2

INPUT			OUTPUT
M	Q_1	Q_2	Q_1'
1	0	0	0

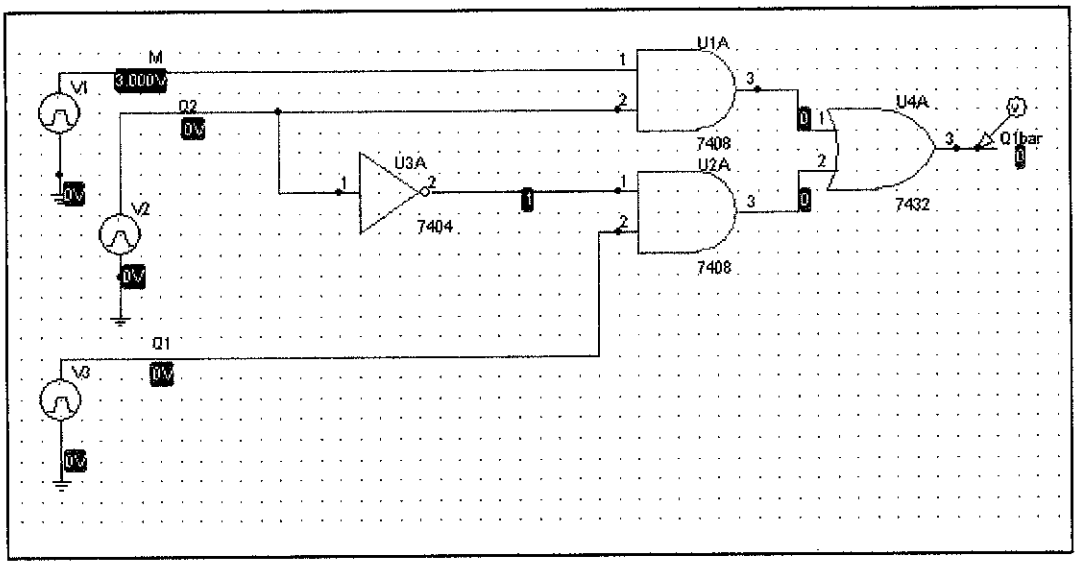

Figure 15 : Logic Circuit for Simulation 2

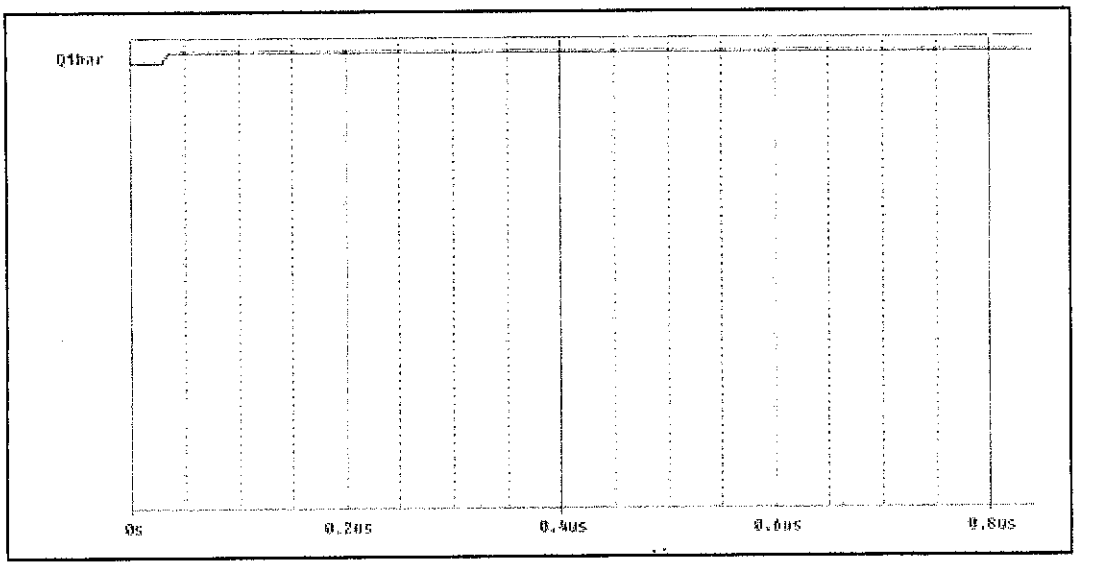

Figure 16 : Output Waveform for Simulation 2

Table 10 : Input-Output Table for Simulation 3

INPUT			OUTPUT
M	Q_1	Q_2	Q_1'
0	0	1	0

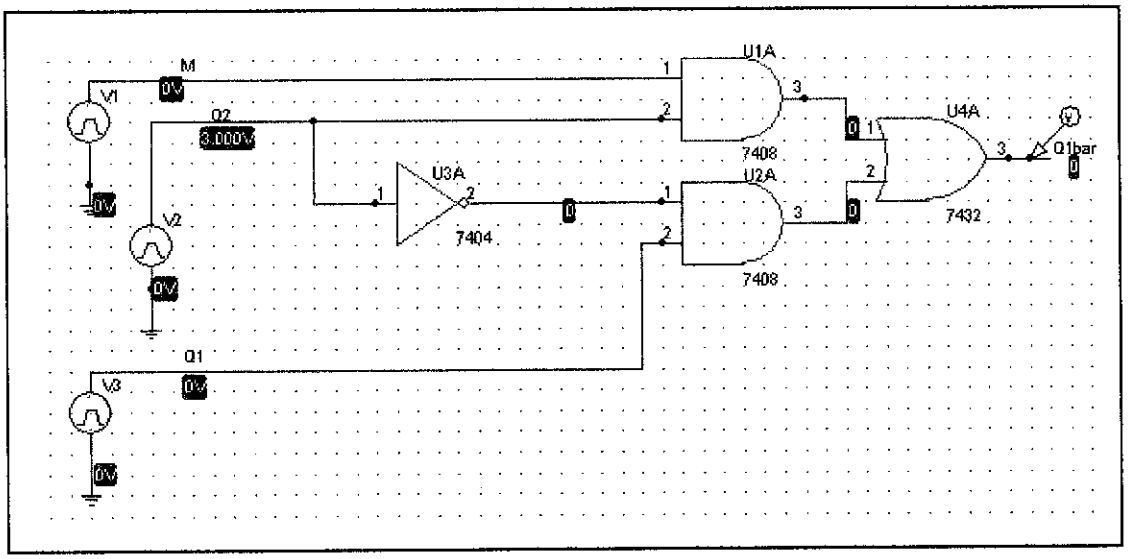

Figure 17 : Logic Circuit for Simulation 3

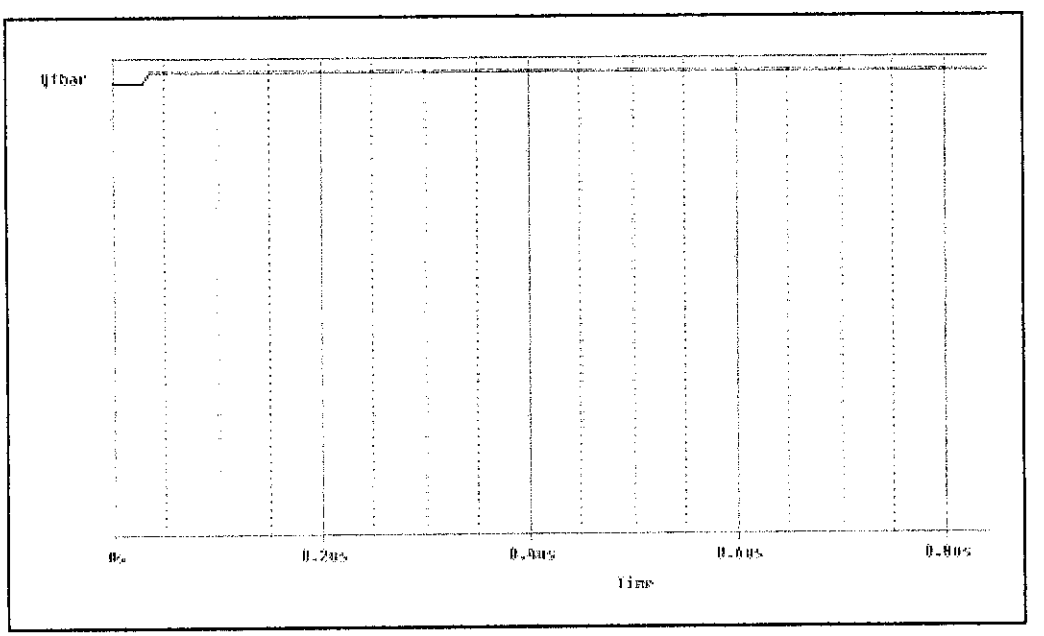

Figure 18 : Output Waveform for Simulation 3

Table 11 : Input-Output Table for Simulation 4

INPUT			OUTPUT
M	Q_1	Q_2	Q_1'
1	0	1	1

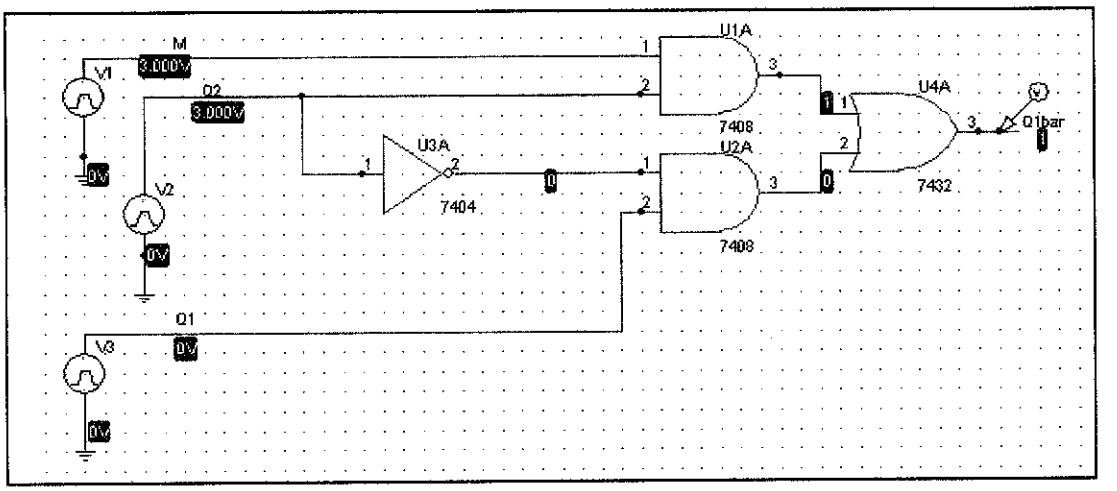

Figure 19 : Logic Circuit for Simulation 4

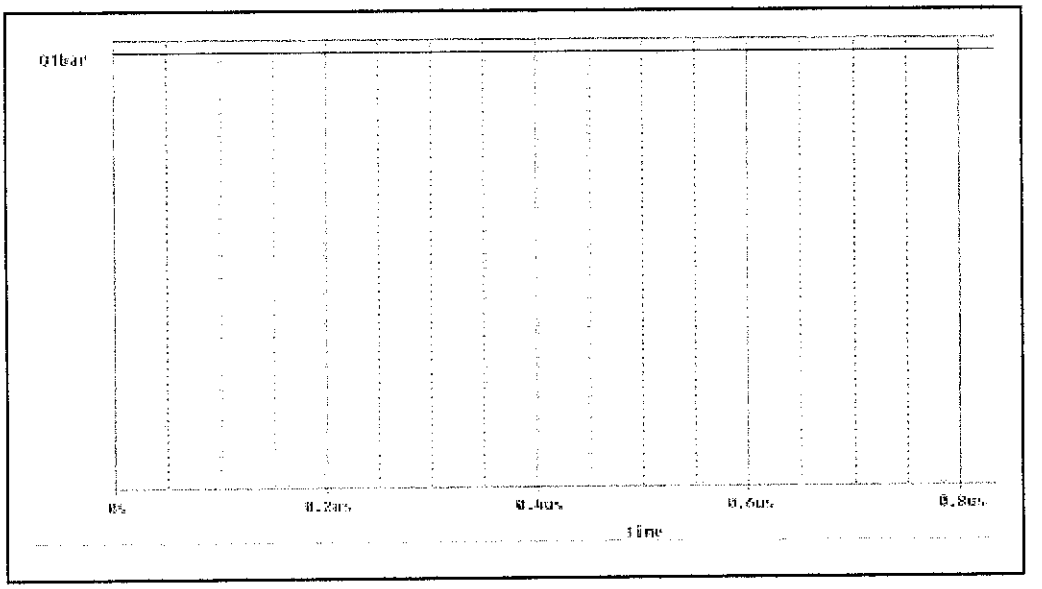

Figure 20 : Output Waveform for Simulation 4

Table 12 : Input-Output Table for Simulation 5

INPUT			OUTPUT
M	Q_1	Q_2	Q_1'
0	1	0	1

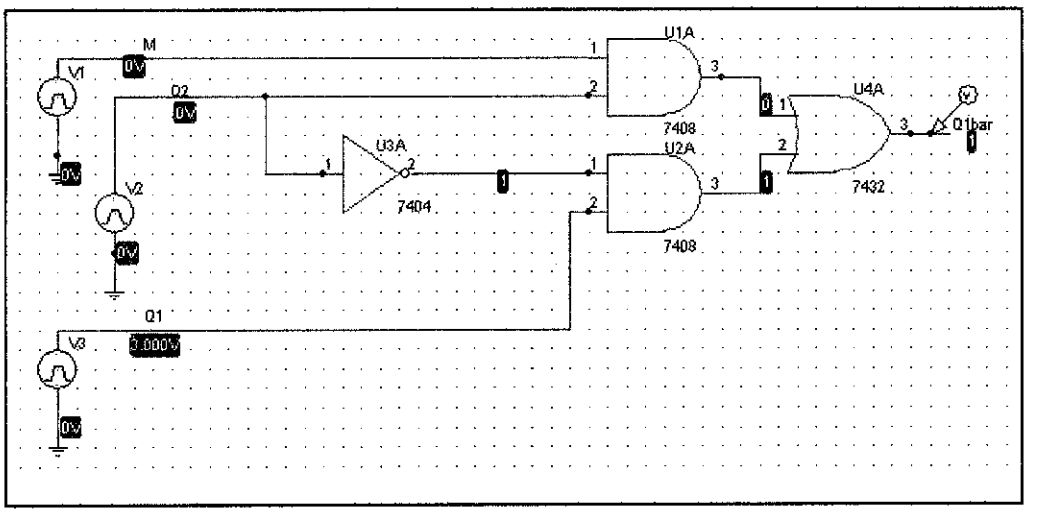

Figure 21 : Logic Circuit for Simulation 5

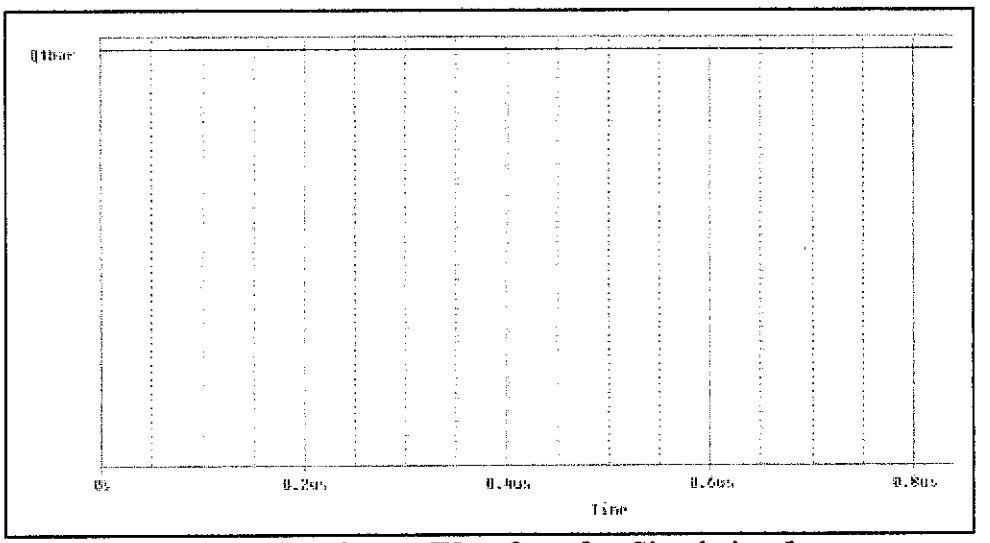

Figure 22 : Output Waveform for Simulation 5

Table 13 : Input-Output Table for Simulation 6

INPUT			OUTPUT
M	Q_1	Q_2	Q_1'
1	1	0	1

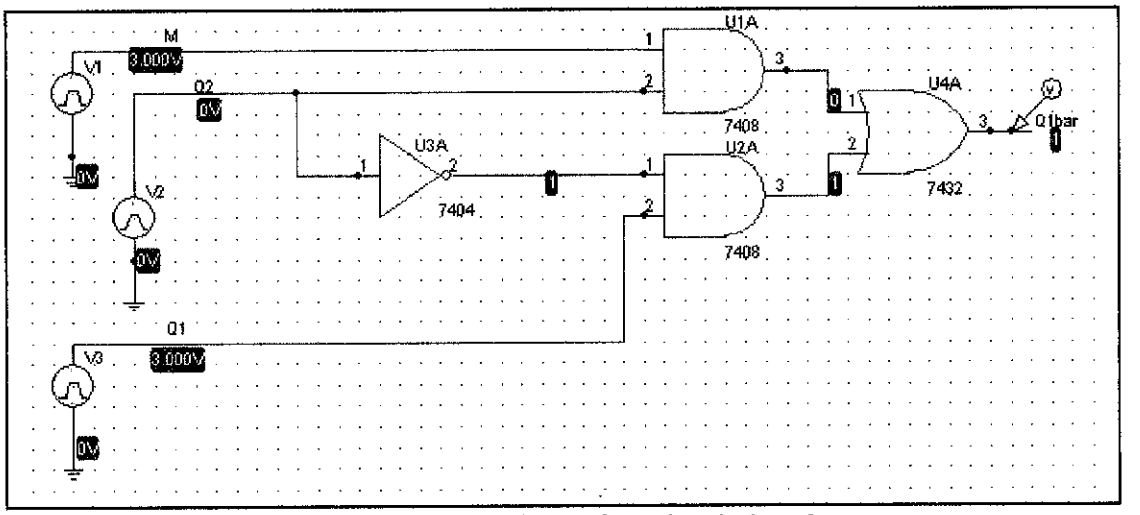

Figure 23 : Logic Circuit for Simulation 6

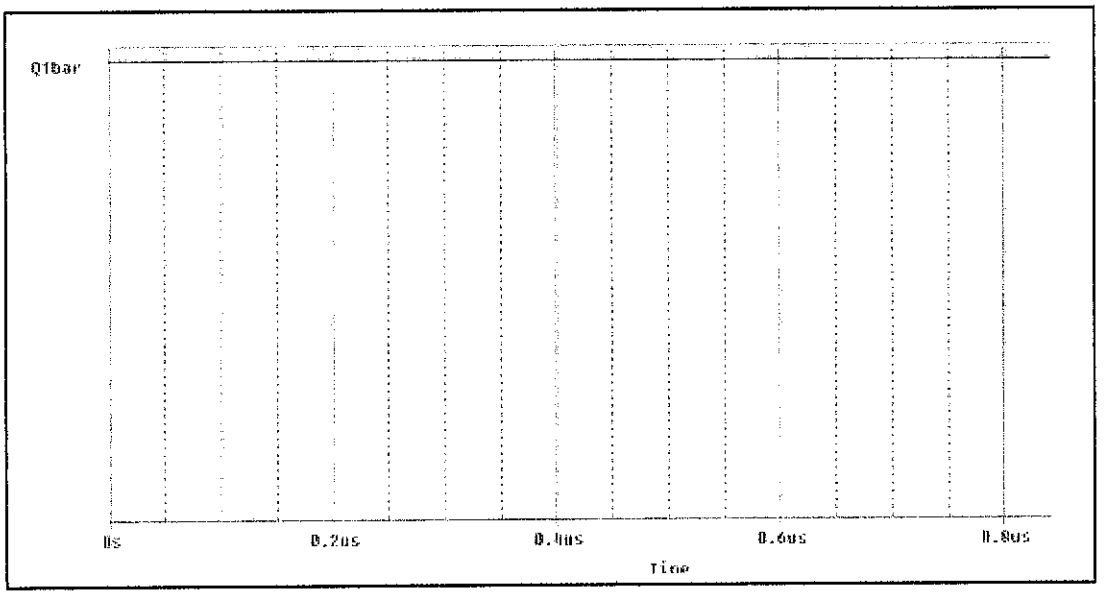

Figure 24 : Output Waveform for Simulation 6

Table 14 : Input-Output Table for Simulation 7

INPUT			OUTPUT
M	Q_1	Q_2	Q_1'
0	1	1	0

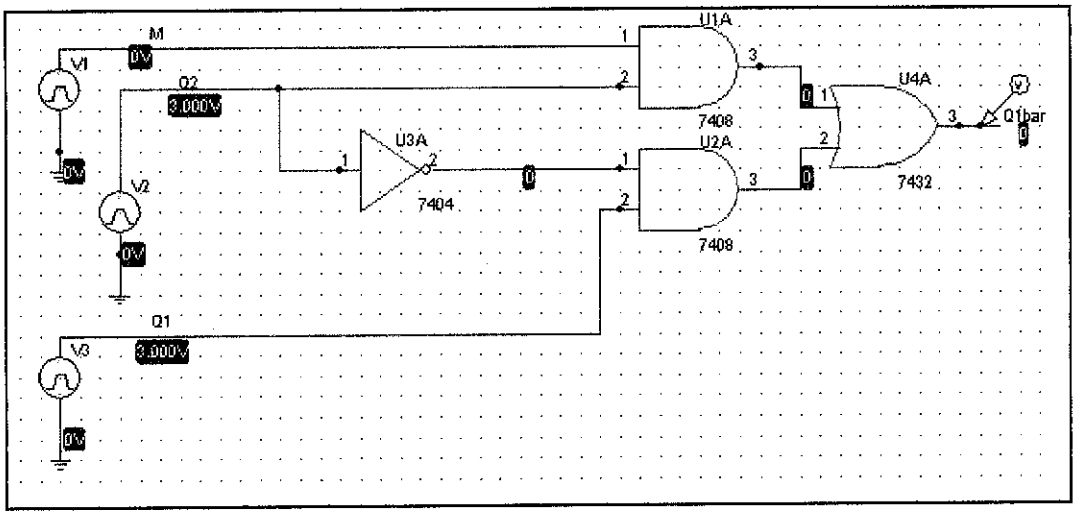

Figure 25 : Logic Circuit for Simulation 7

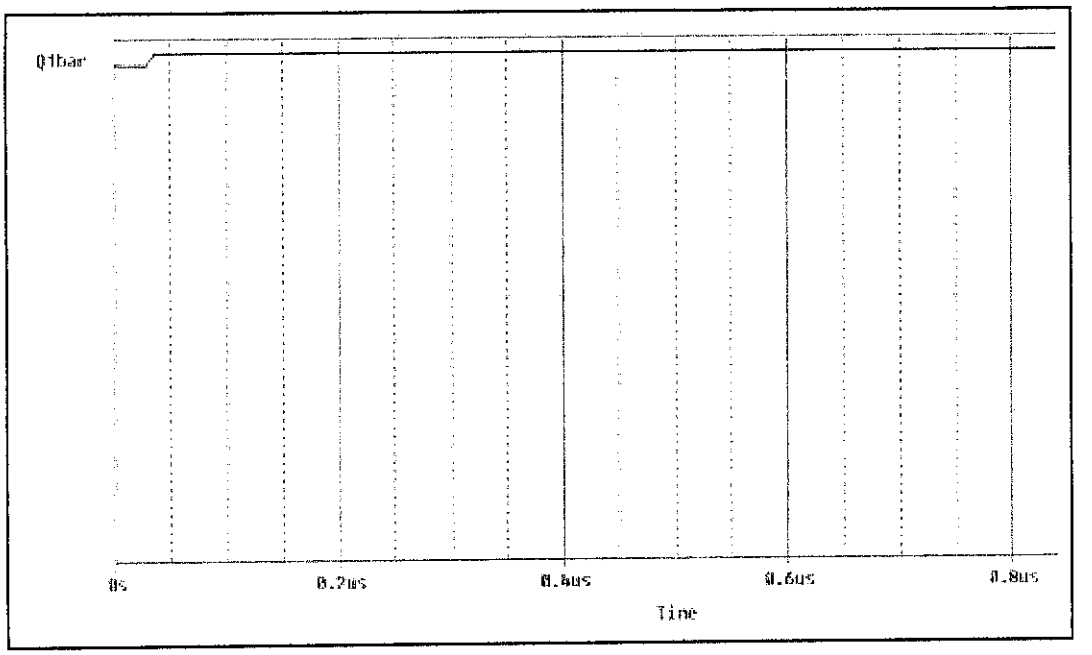

Figure 26 : Output Waveform for Simulation 7

Table 15 : Input-Output Table for Simulation 8

INPUT			OUTPUT
M	Q_1	Q_2	Q_1'
1	1	1	1

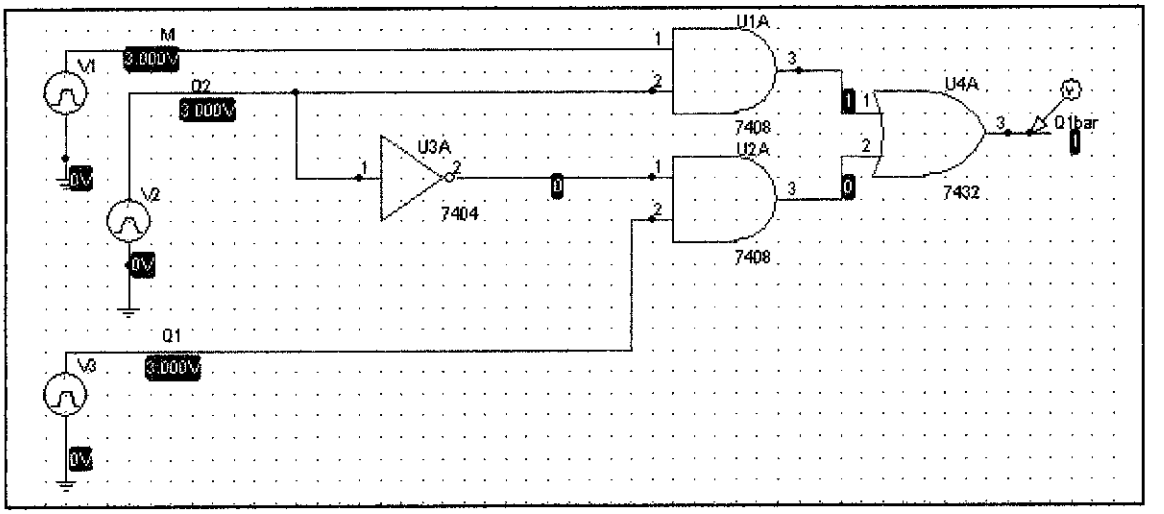

Figure 27 : Logic Circuit for Simulation 8

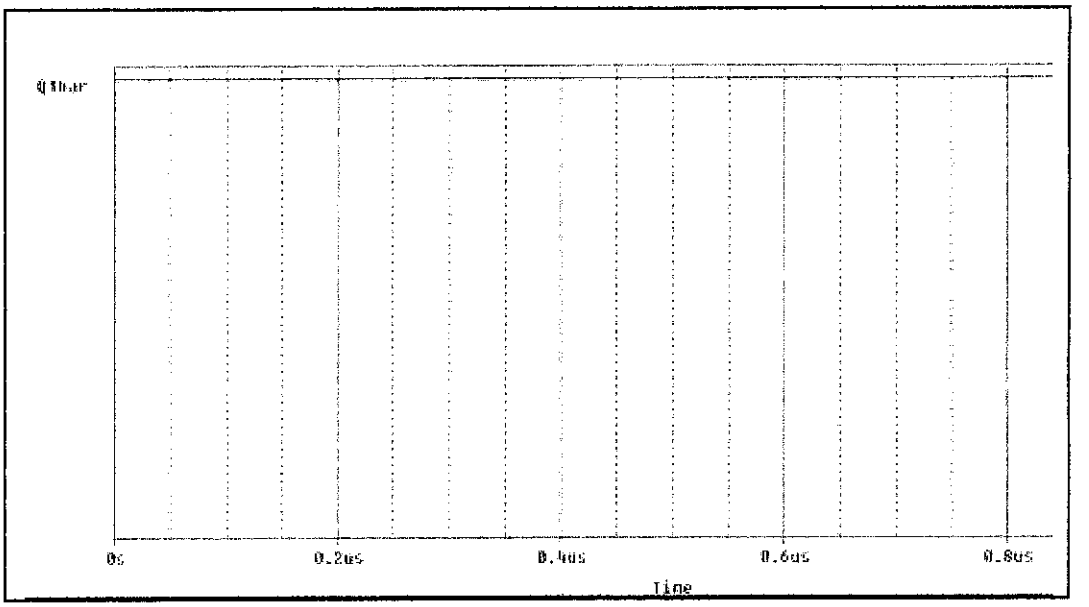

Figure 28 : Output Waveform for Simulation 8

4.1.1.2 PSPICE Simulation Results for Q_2'

The output waveform for this simulation is high (1) by default. Refer to Table 4 and Figure 8;

Table 16 : Input-Output Table for Simulation 9

INPUT				OUTPUT
C	M	Q_1	Q_2	Q_2'
0	0	0	0	0

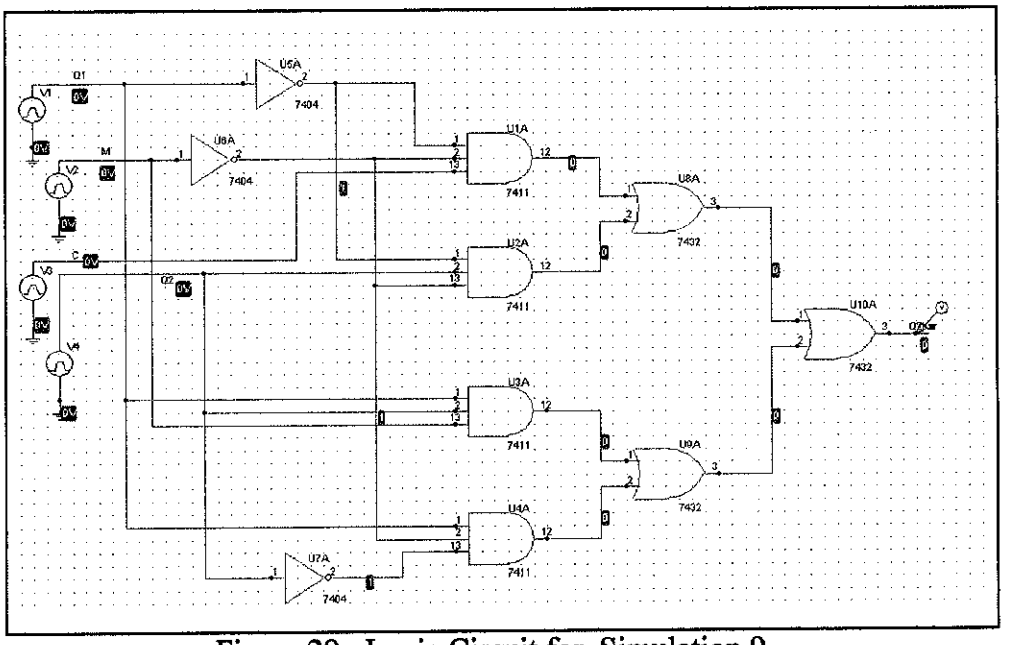

Figure 29 : Logic Circuit for Simulation 9

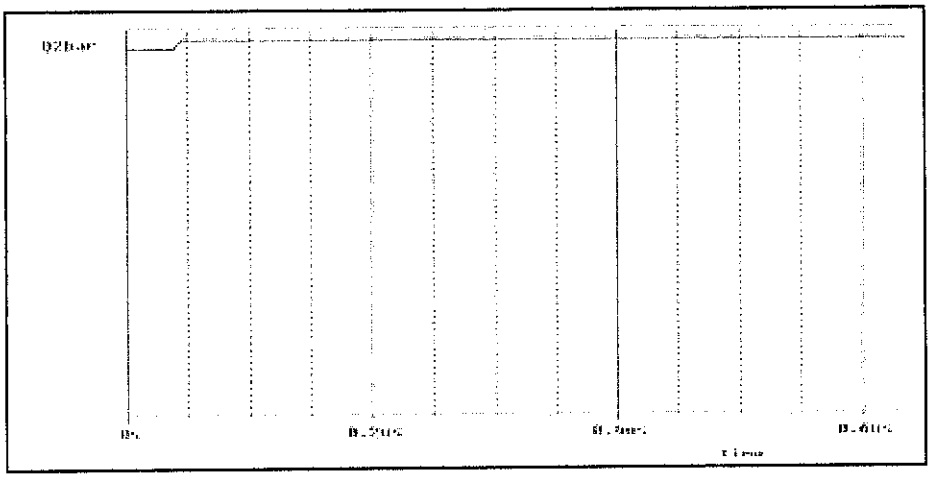

Figure 30 : Output Waveform for Simulation 9

Table 17 : Input-Output Table for Simulation 10

INPUT				OUTPUT
C	M	Q_1	Q_2	Q_2'
1	0	0	0	1

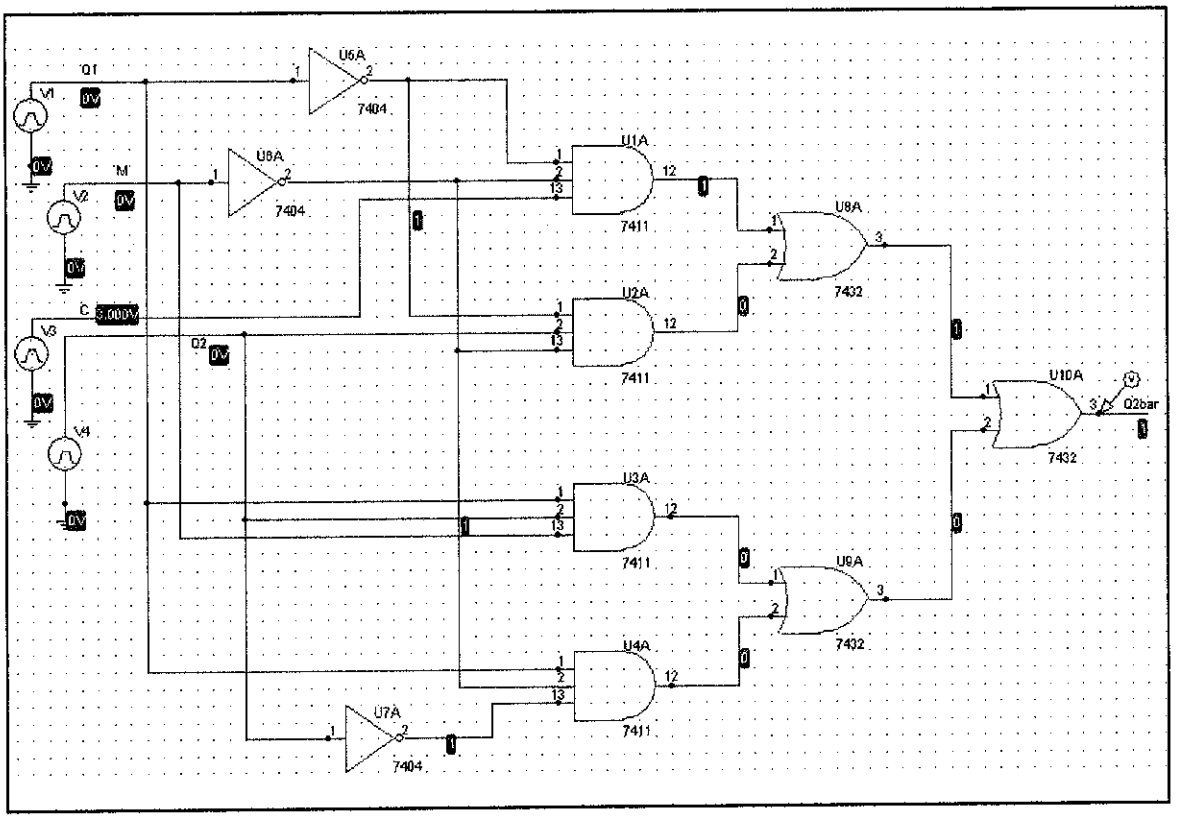

Figure 31 : Logic Circuit for Simulation 10

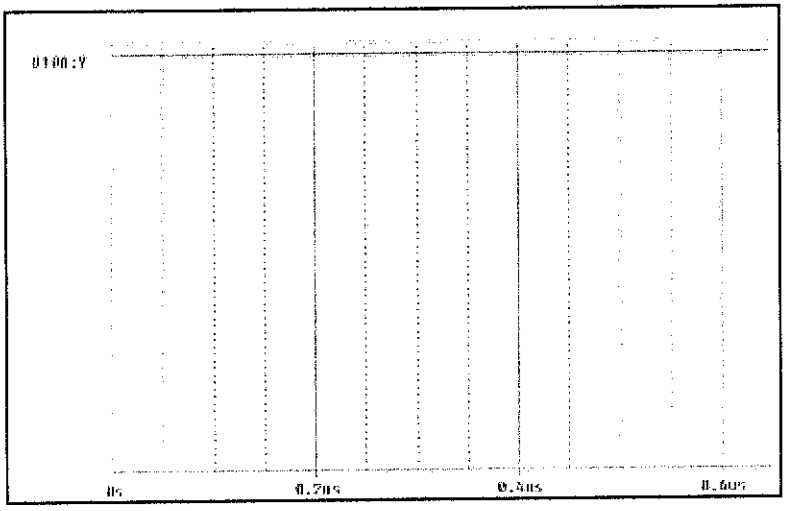

Figure 32 : Output Waveform for Simulation 10

Table 18 : Input-Output Table for Simulation 11

INPUT				OUTPUT
C	M	Q_1	Q_2	Q_2'
0	1	0	0	0

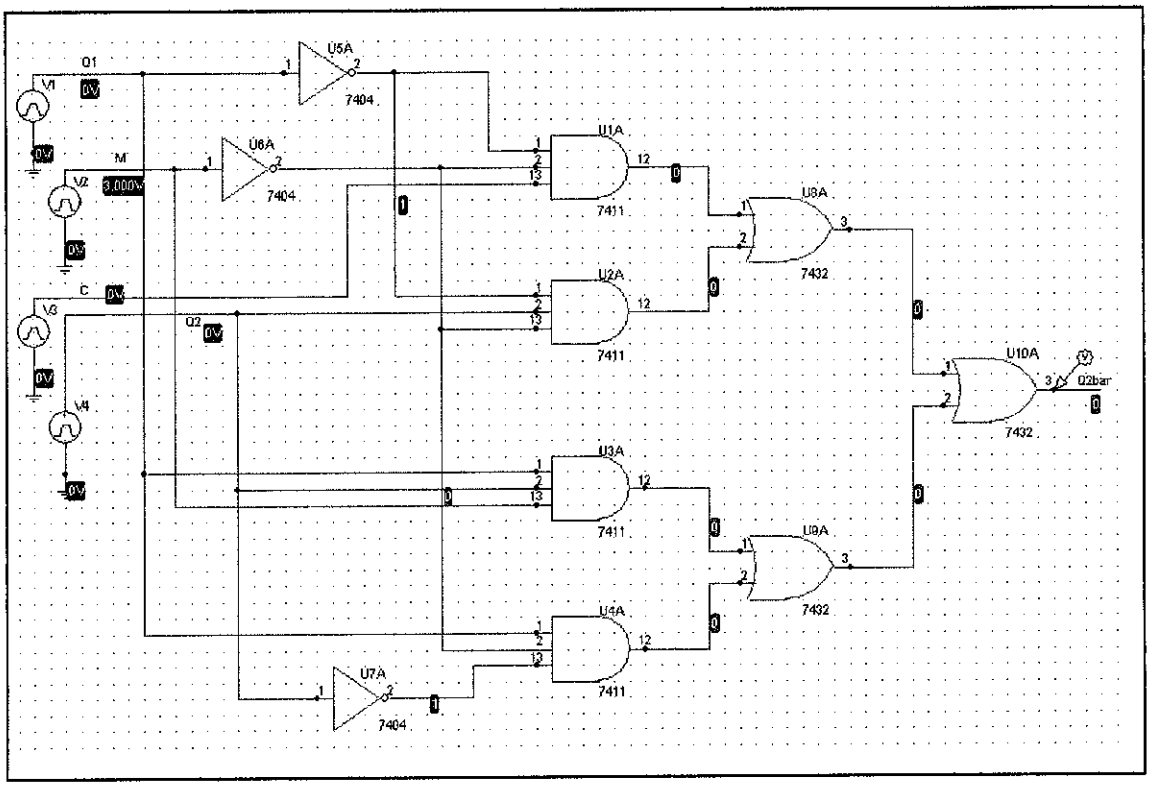

Figure 33 : Logic Circuit for Simulation 11

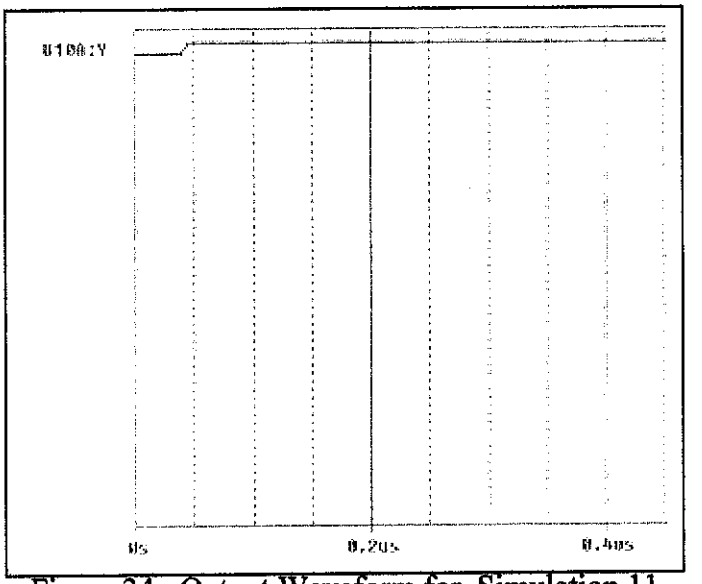

Figure 34 : Output Waveform for Simulation 11

Table 19 : Input-Output Table for Simulation 12

INPUT				OUTPUT
C	M	Q_1	Q_2	Q_2'
1	1	0	0	0

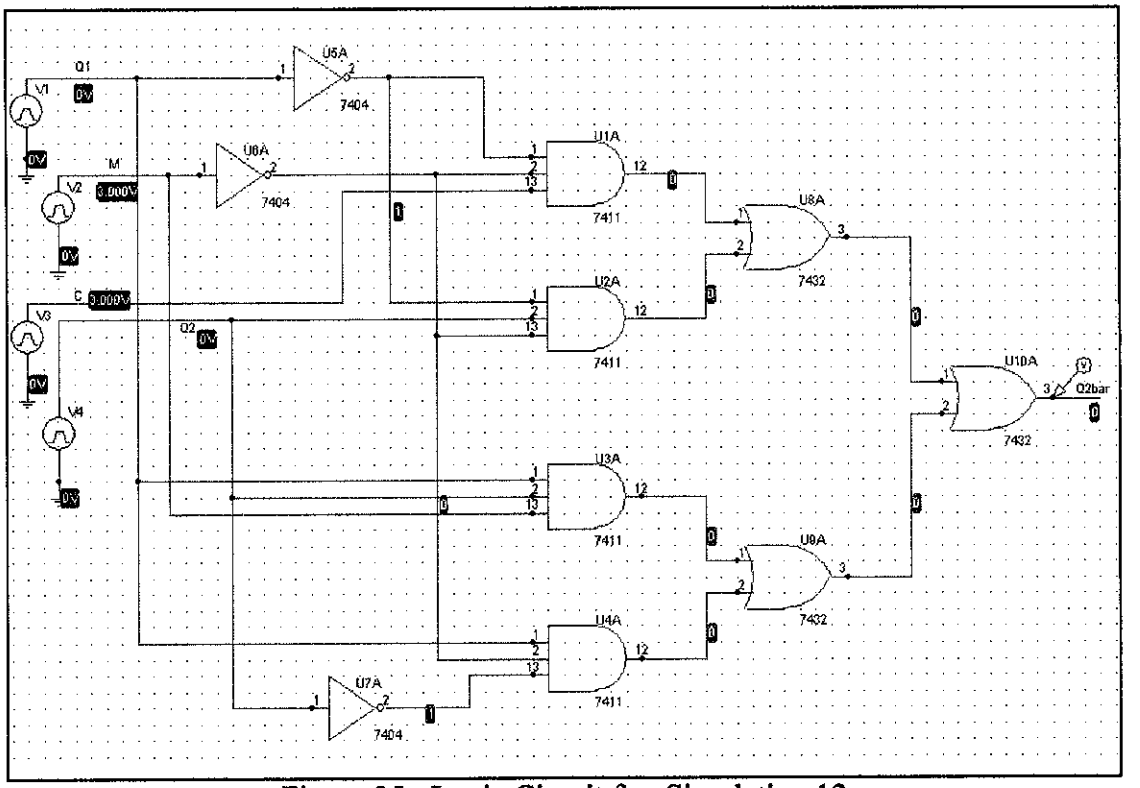

Figure 35 : Logic Circuit for Simulation 12

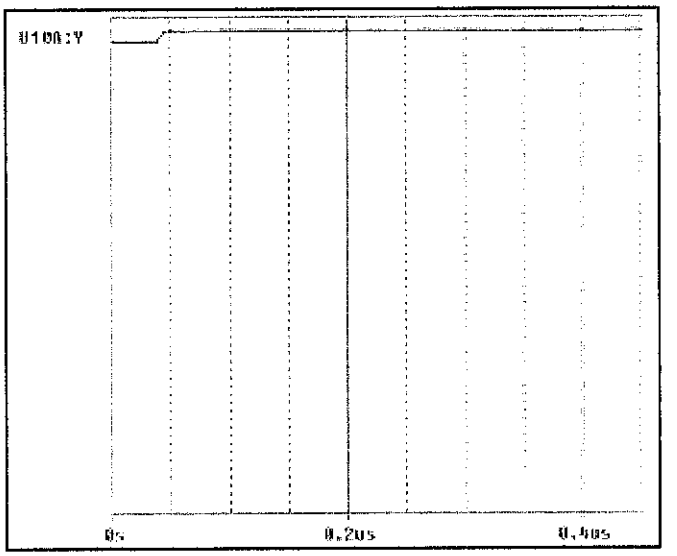

Figure 36 : Output Waveform for Simulation 12

Table 20 : Input-Output Table for Simulation 13

INPUT				OUTPUT
C	M	Q_1	Q_2	Q_2'
0	0	0	1	1

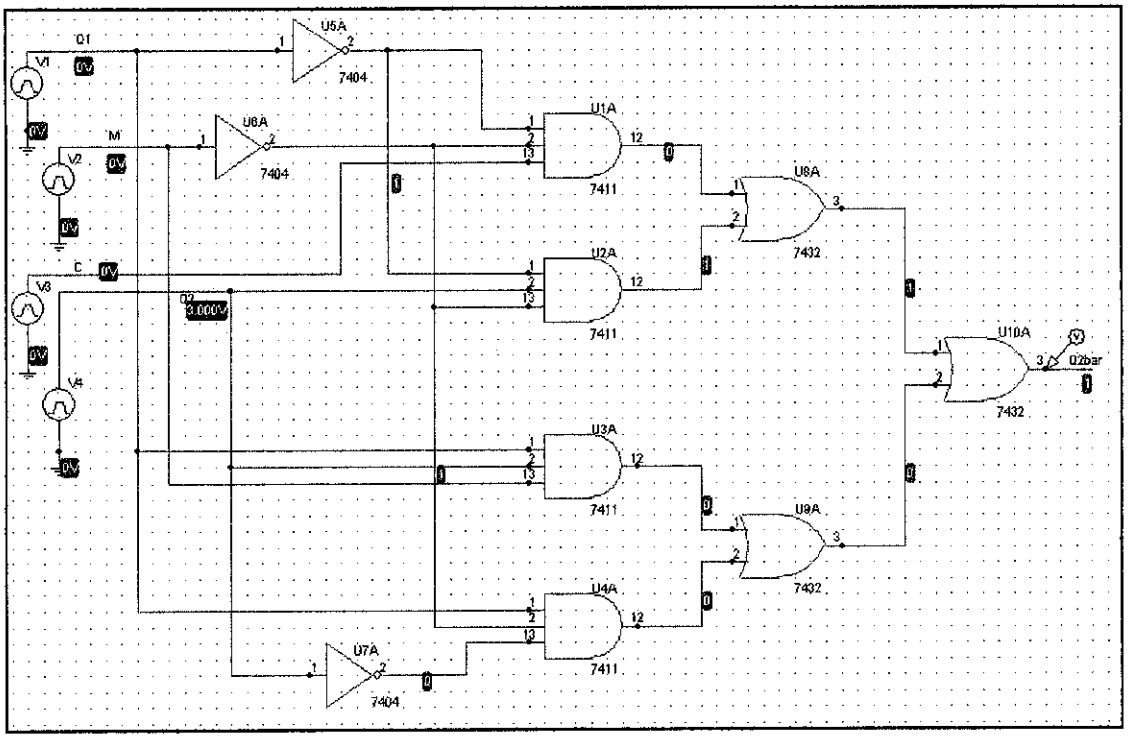

Figure 37 : Logic Circuit for Simulation 13

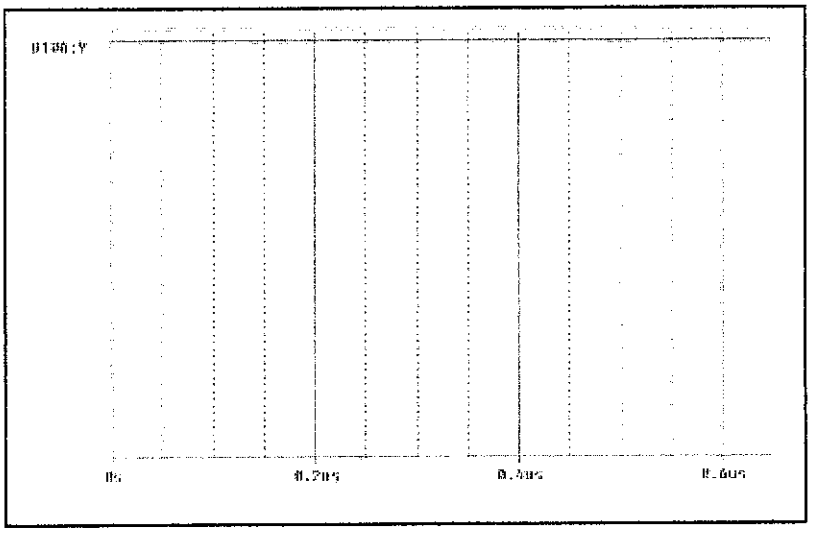

Figure 38 : Output Waveform for Simulation 13

Table 21 : Input-Output Table for Simulation 14

INPUT				OUTPUT
C	M	Q_1	Q_2	Q_2'
1	0	0	1	1

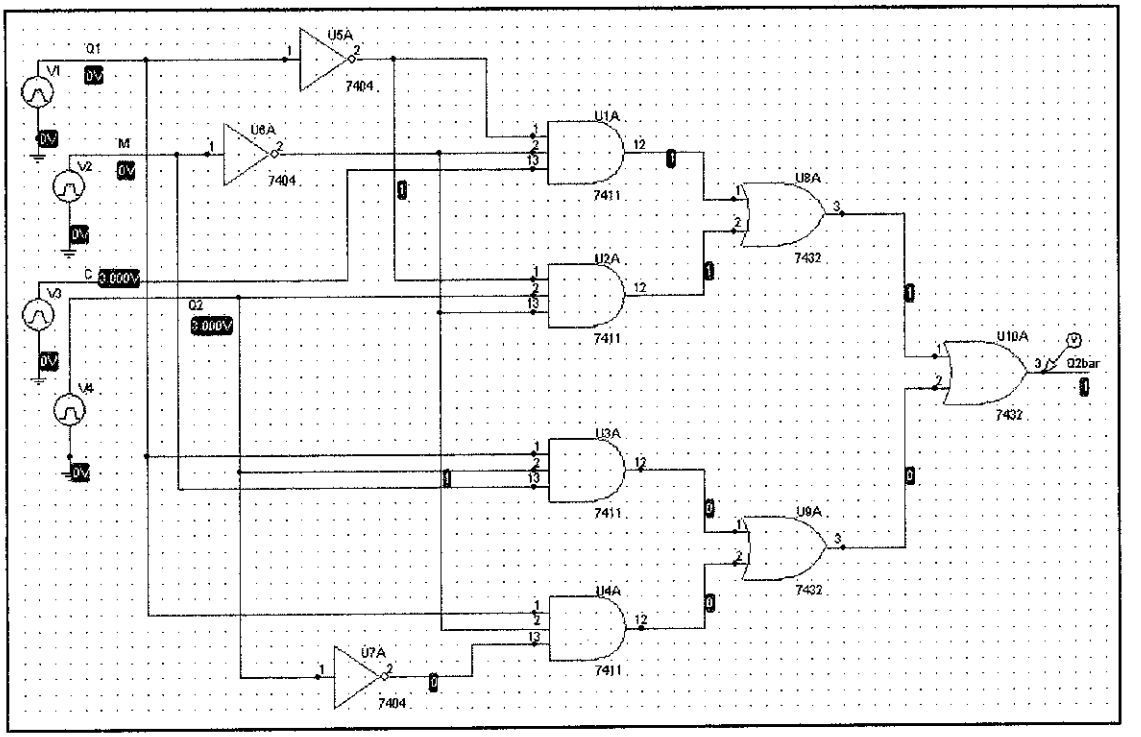

Figure 39 : Logic Circuit for Simulation 14

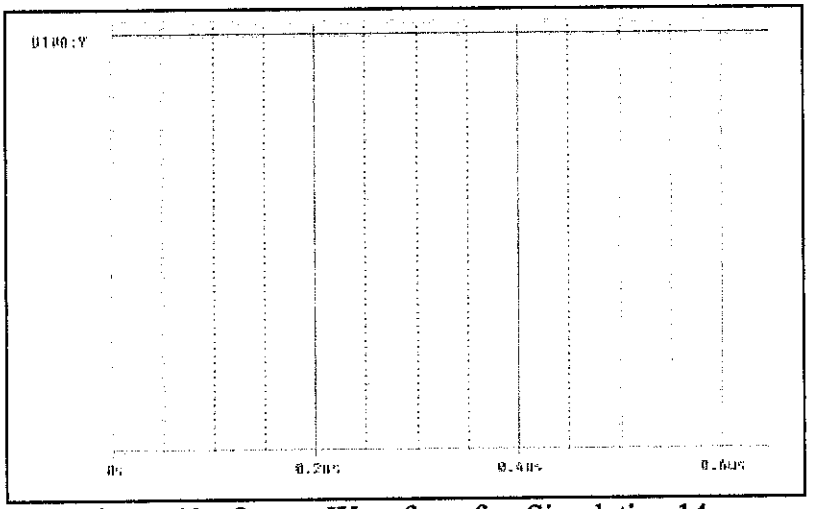

Figure 40 : Output Waveform for Simulation 14

Table 22 : Input-Output Table for Simulation 15

INPUT				OUTPUT
C	M	Q_1	Q_2	Q_2'
0	1	0	1	0

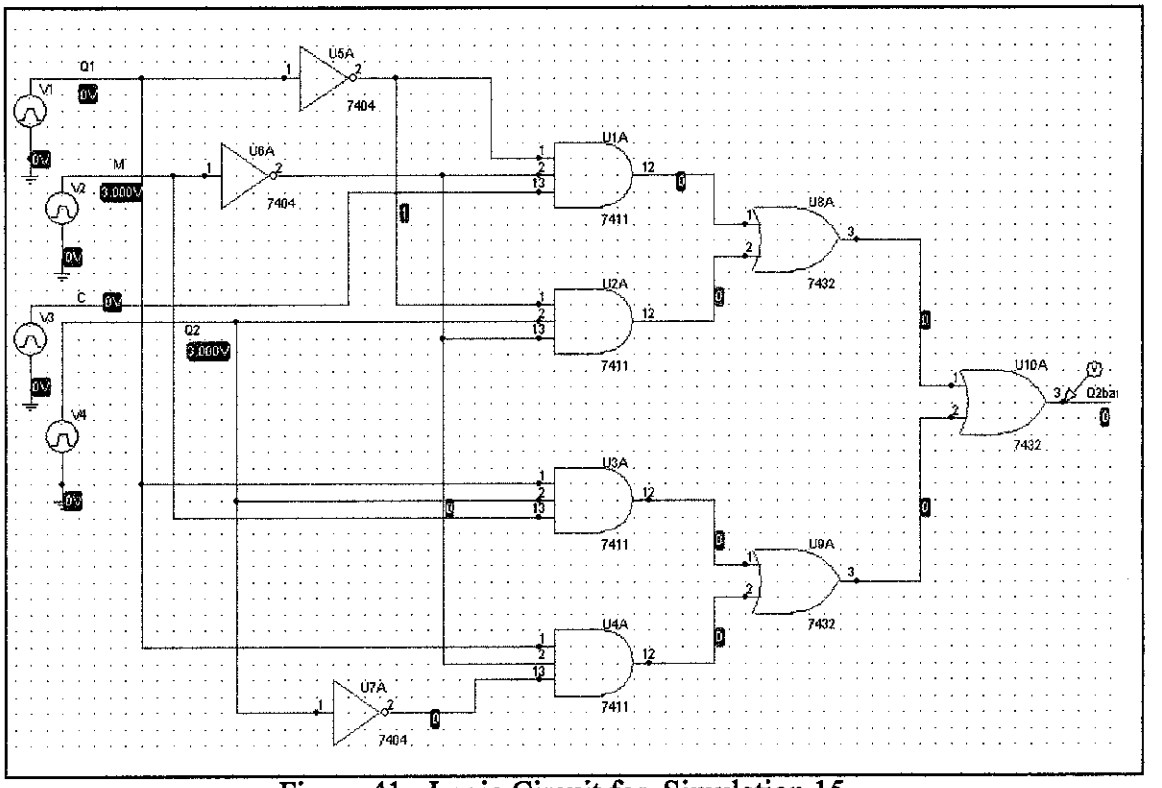

Figure 41 : Logic Circuit for Simulation 15

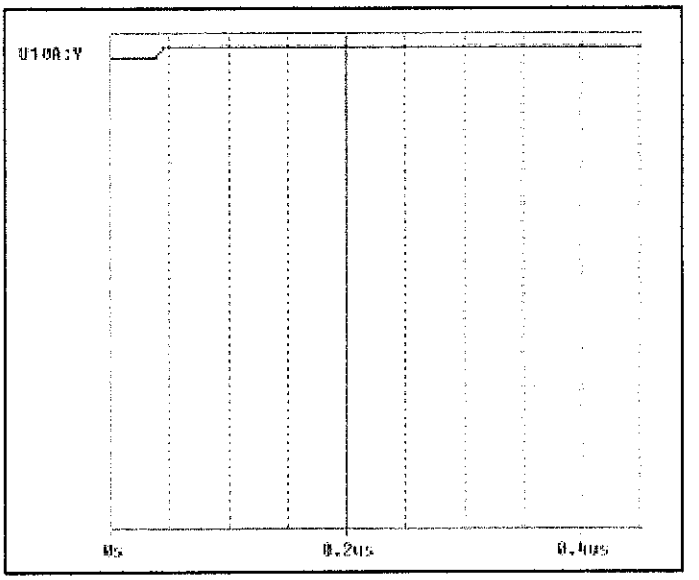

Figure 42 : Output Waveform for Simulation 15

Table 23 : Input-Output Table for Simulation 16

INPUT				OUTPUT
C	M	Q_1	Q_2	Q_2'
1	1	0	1	0

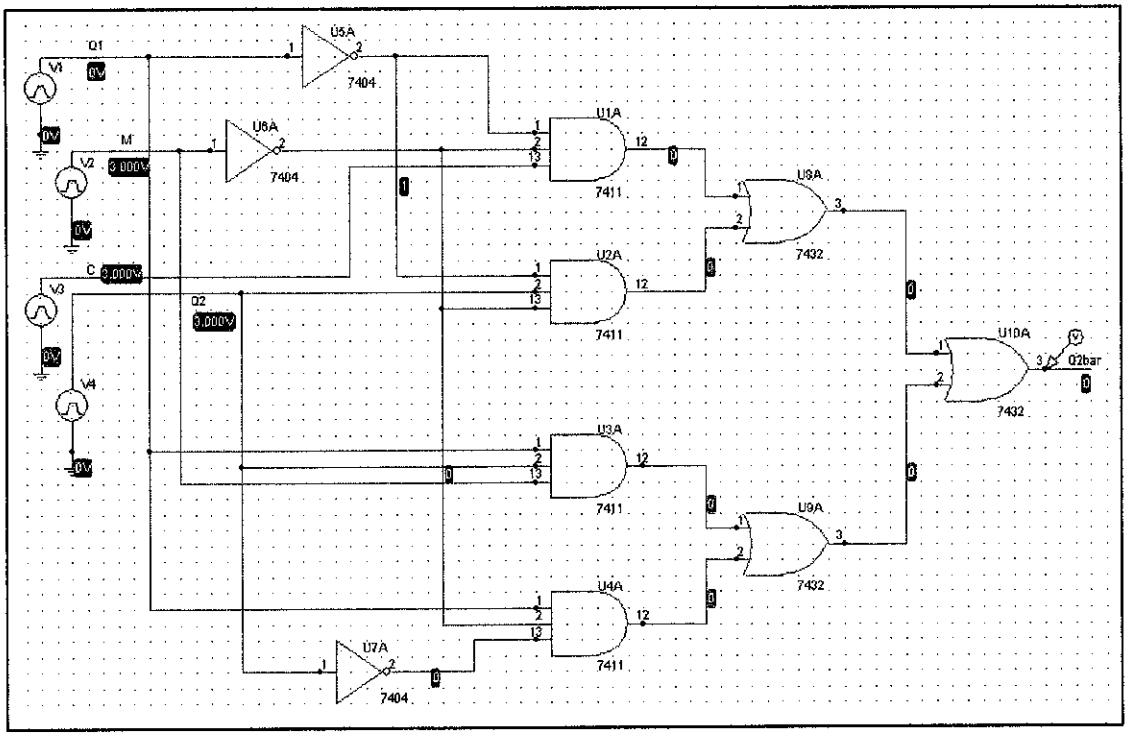

Figure 43 : Logic Circuit for Simulation 16

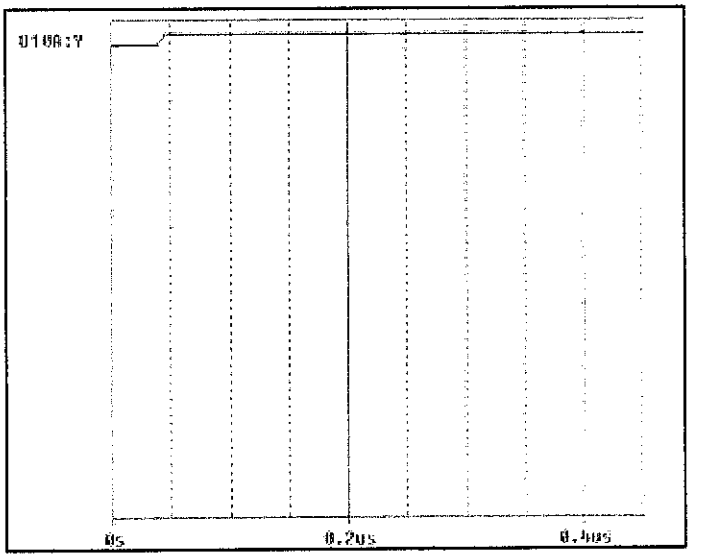

Figure 44 : Output Waveform for Simulation 16

Table 24 : Input-Output Table for Simulation 17

INPUT				OUTPUT
C	M	Q_1	Q_2	Q_2'
0	0	1	0	1

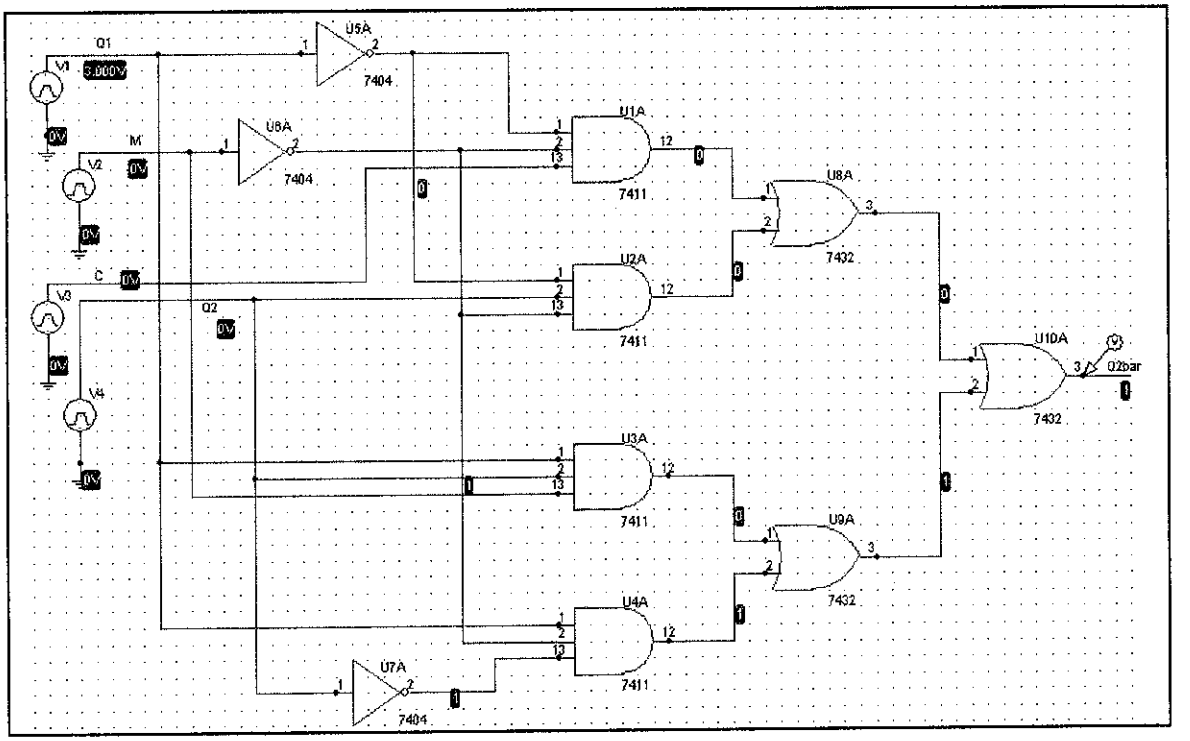

Figure 45 : Logic Circuit for Simulation 17

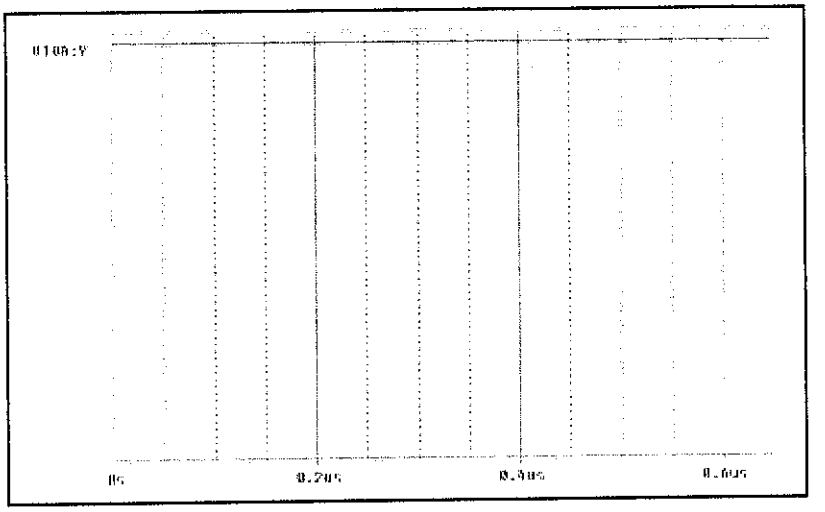

Figure 46 : Output Waveform for Simulation 17

Table 25 : Input-Output Table for Simulation 18

INPUT				OUTPUT
C	M	Q_1	Q_2	Q_2'
1	0	1	0	1

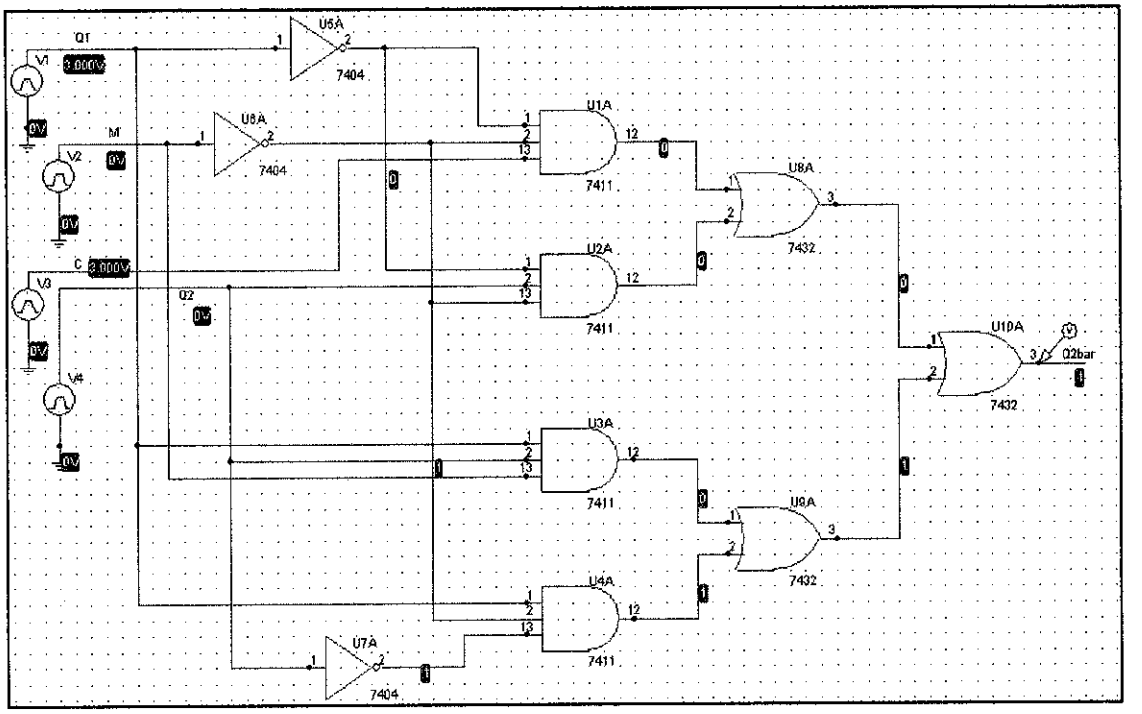

Figure 47 : Logic Circuit for Simulation 18

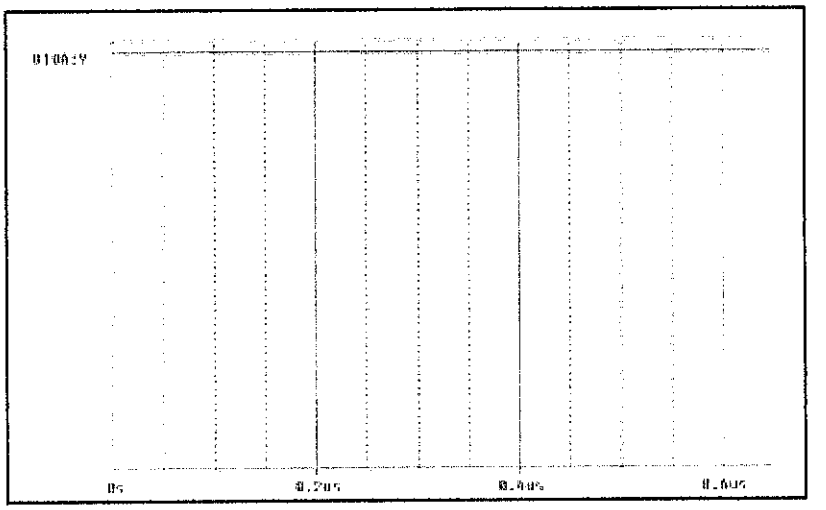

Figure 48 : Output Waveform for Simulation 18

Table 26 : Input-Output Table for Simulation 19

INPUT				OUTPUT
C	M	Q_1	Q_2	Q_2'
0	1	1	0	0

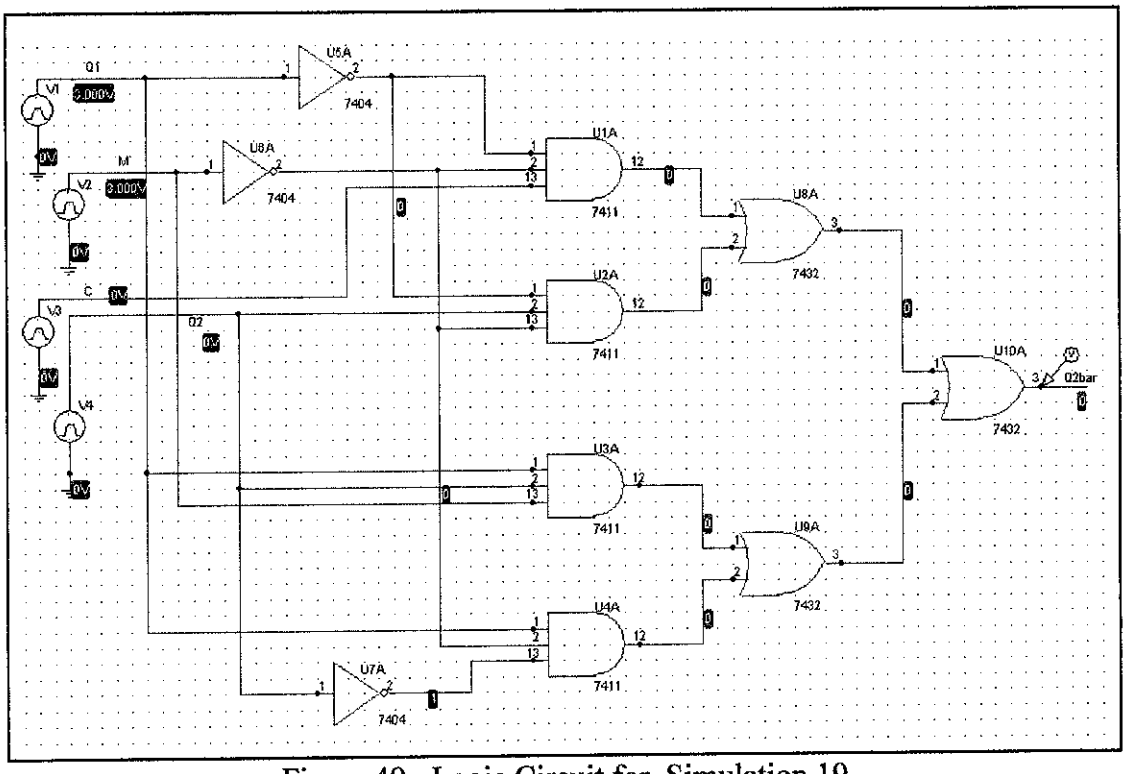

Figure 49 : Logic Circuit for Simulation 19

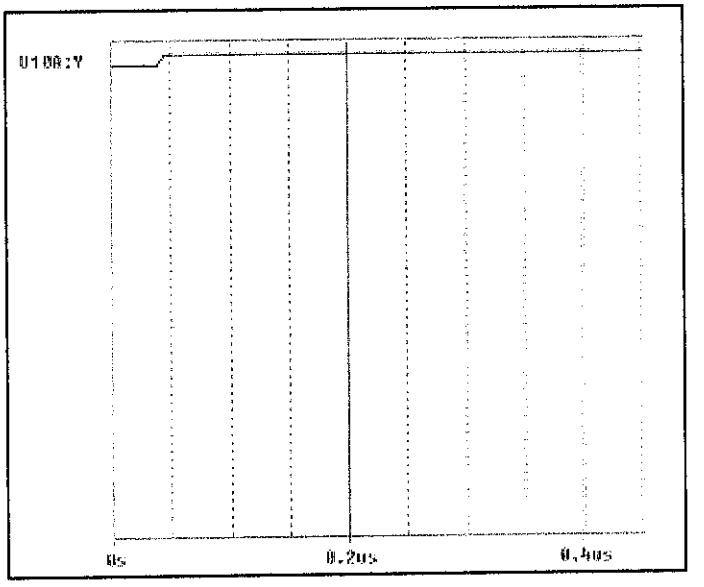

Figure 50 : Output Waveform for Simulation 19

Table 27 : Input-Output Table for Simulation 20

INPUT				OUTPUT
C	M	Q_1	Q_2	Q_2'
1	1	1	0	0

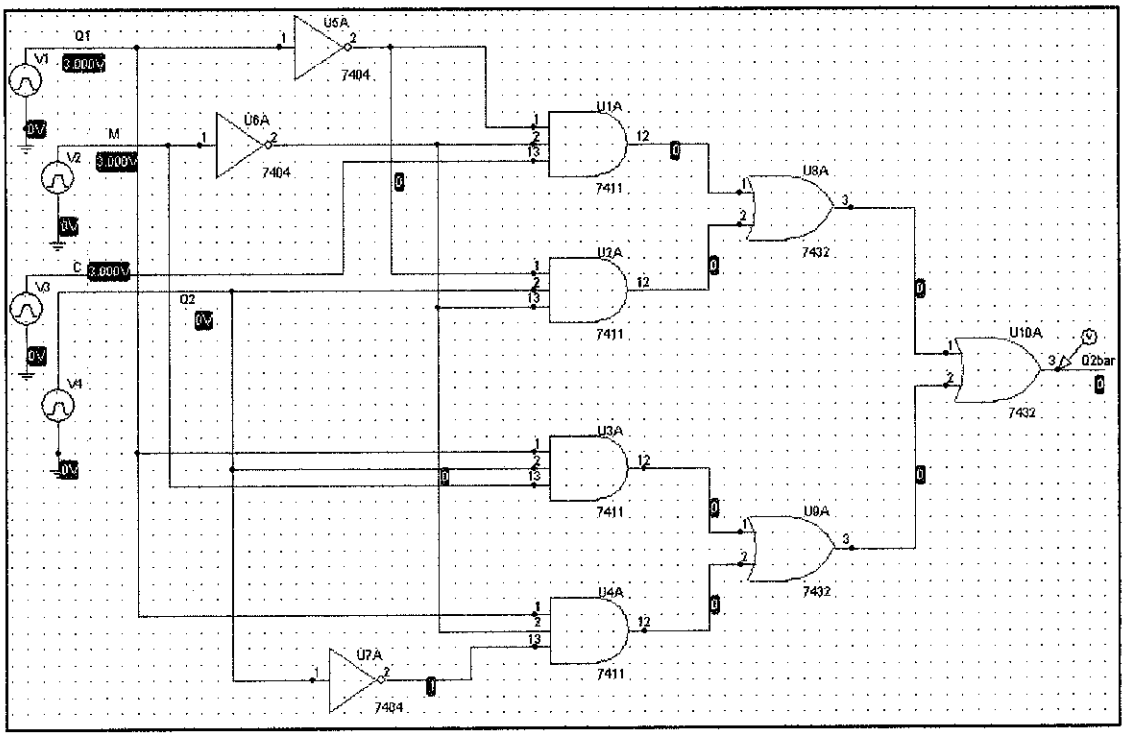

Figure 51 : Logic Circuit for Simulation 20

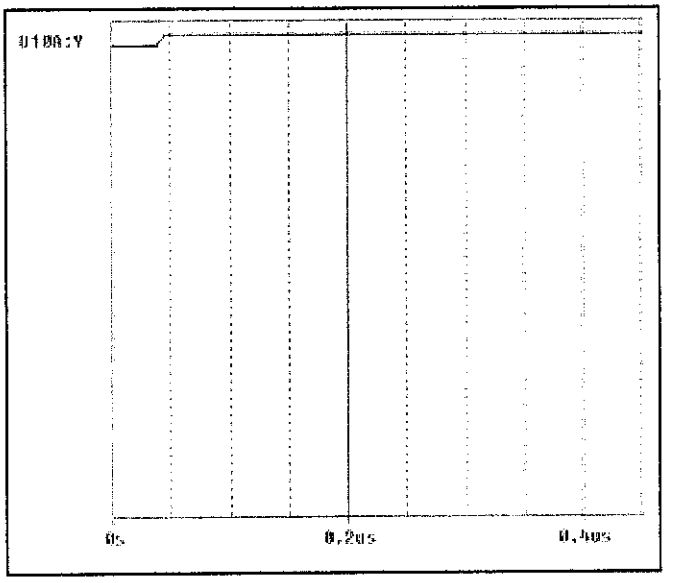

Figure 52 : Output Waveform for Simulation 20

Table 28 : Input-Output Table for Simulation 21

INPUT				OUTPUT
C	M	Q_1	Q_2	Q_2'
0	0	1	1	0

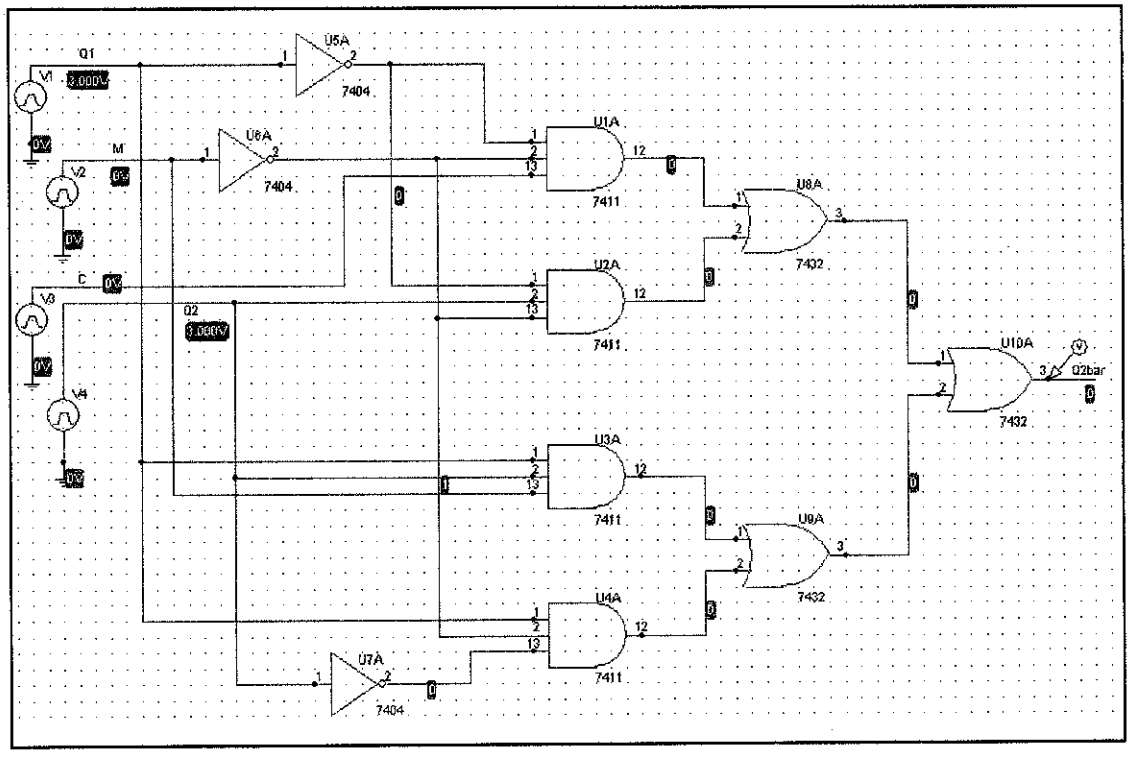

Figure 53 : Logic Circuit for Simulation 21

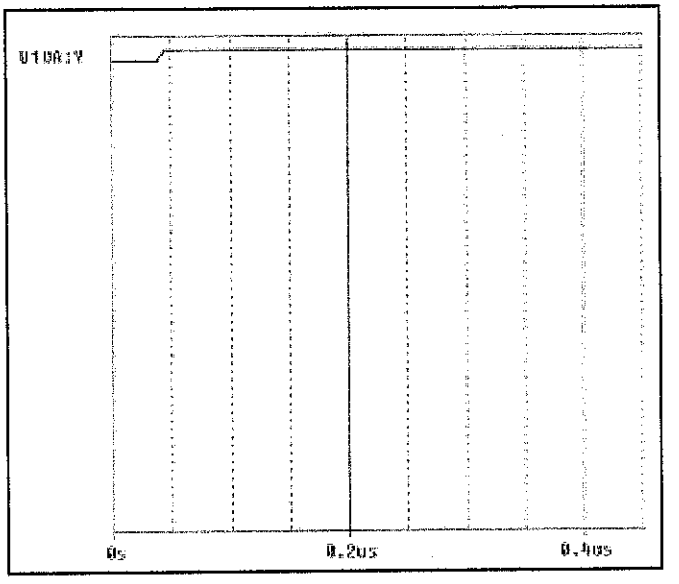

Figure 54 : Output Waveform for Simulation 21

Table 29 : Input-Output Table for Simulation 22

INPUT				OUTPUT
C	M	Q_1	Q_2	Q_2'
1	0	1	1	0

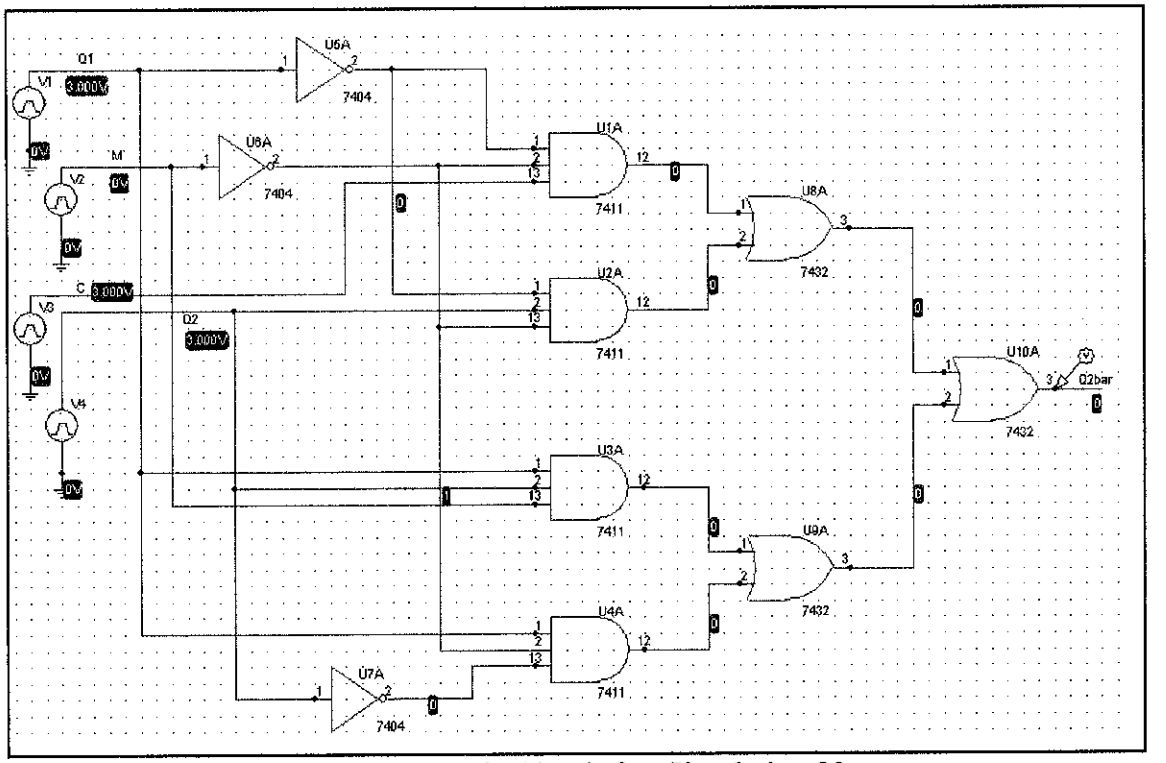

Figure 55 : Logic Circuit for Simulation 22

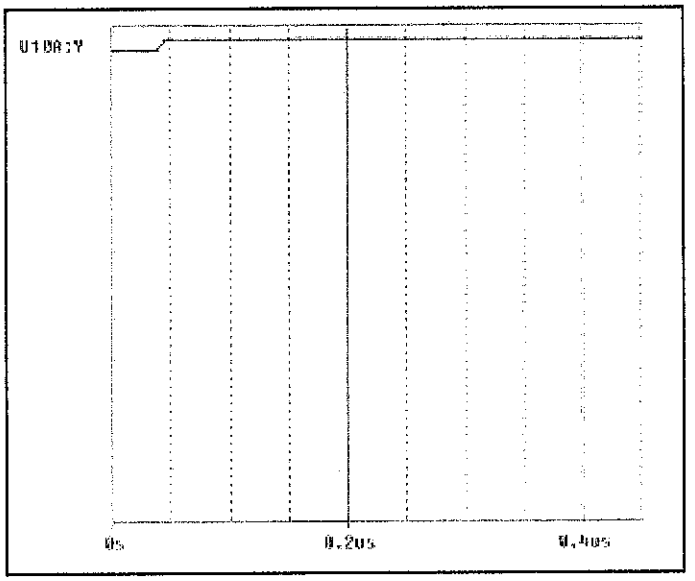

Figure 56 : Output Waveform for Simulation 22

Table 30 : Input-Output Table for Simulation 23

INPUT				OUTPUT
C	M	Q_1	Q_2	Q_2'
0	1	1	1	1

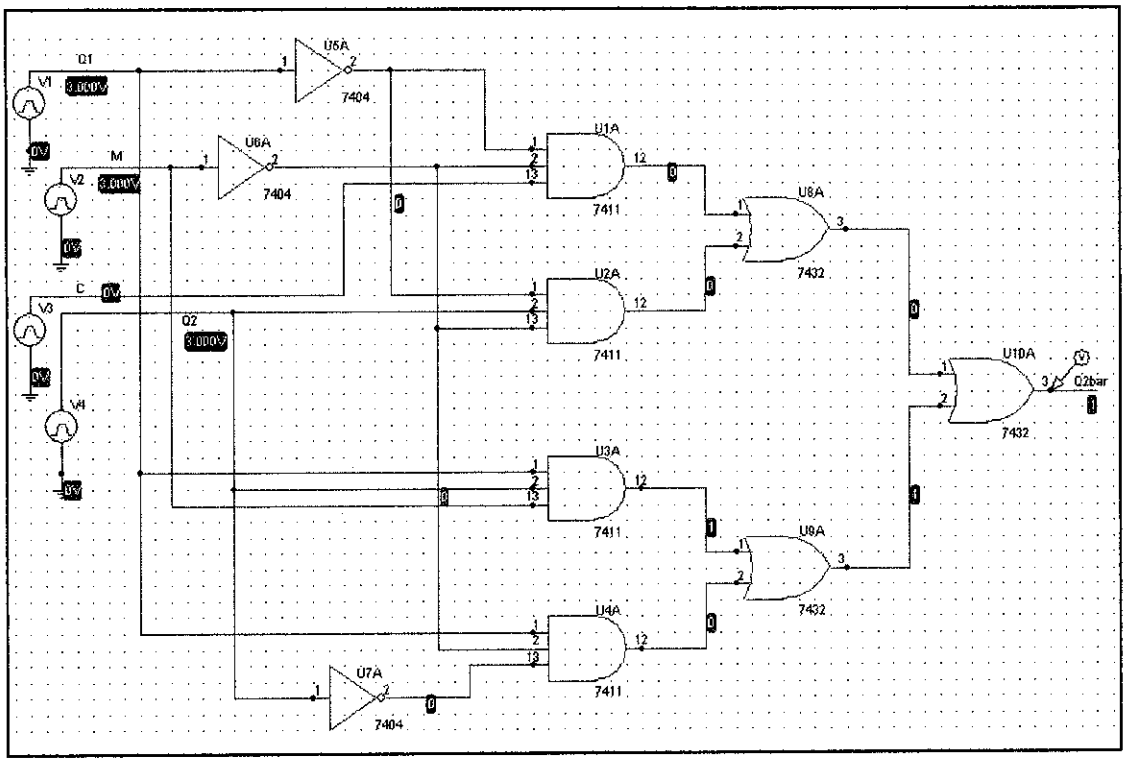

Figure 57 : Logic Circuit for Simulation 23

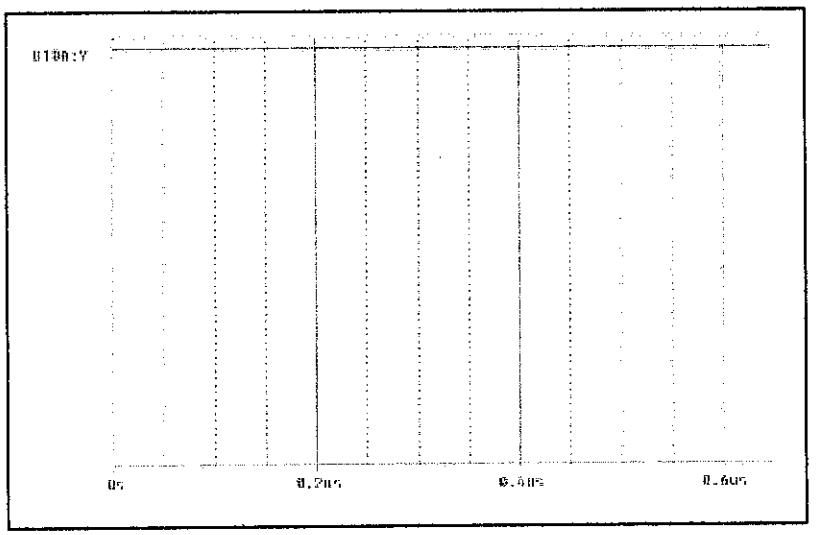

Figure 58 : Output Waveform for Simulation 23

Table 31 : Input-Output Table for Simulation 24

INPUT				OUTPUT
C	M	Q_1	Q_2	Q_2'
1	1	1	1	1

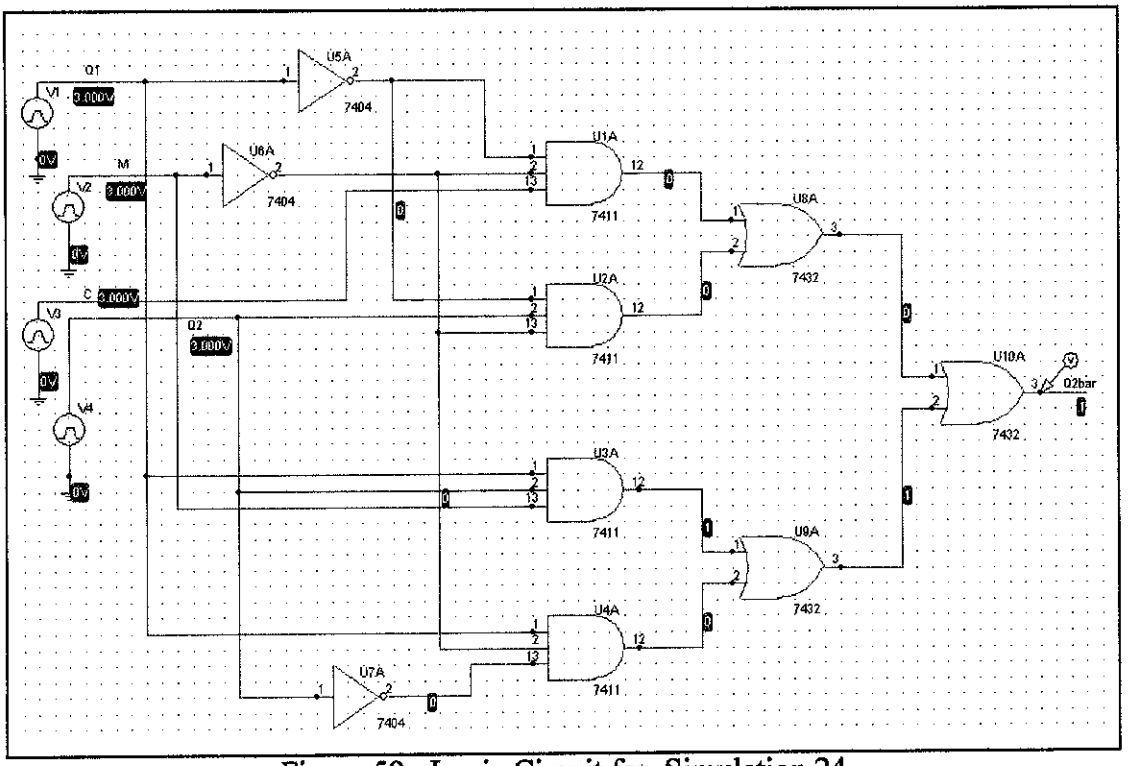

Figure 59 : Logic Circuit for Simulation 24

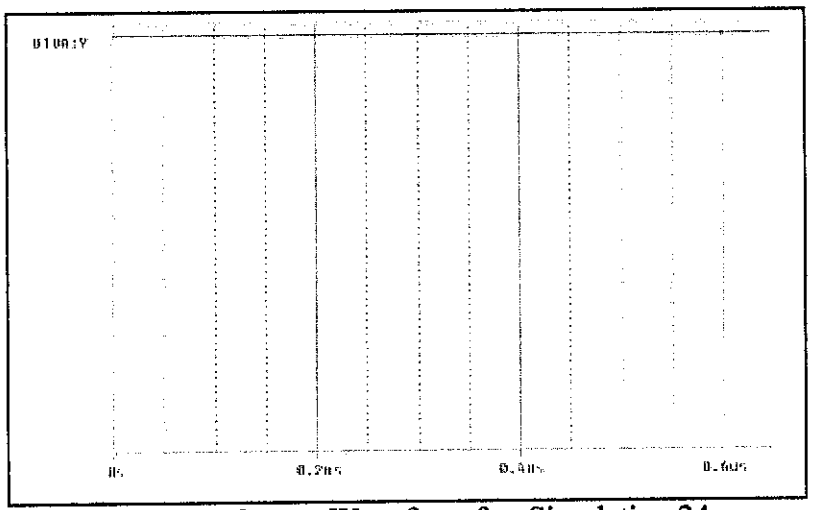

Figure 60 : Output Waveform for Simulation 24

4.1.1.3 *PSPICE Simulation Results for B*

The output waveform for this simulation is low (0) by default. Refer to Table 6 and Figure 9;

Table 32 : Input-Output Table for Simulation 25

INPUT			OUTPUT
M	Q_1	Q_2	B
0	0	0	0

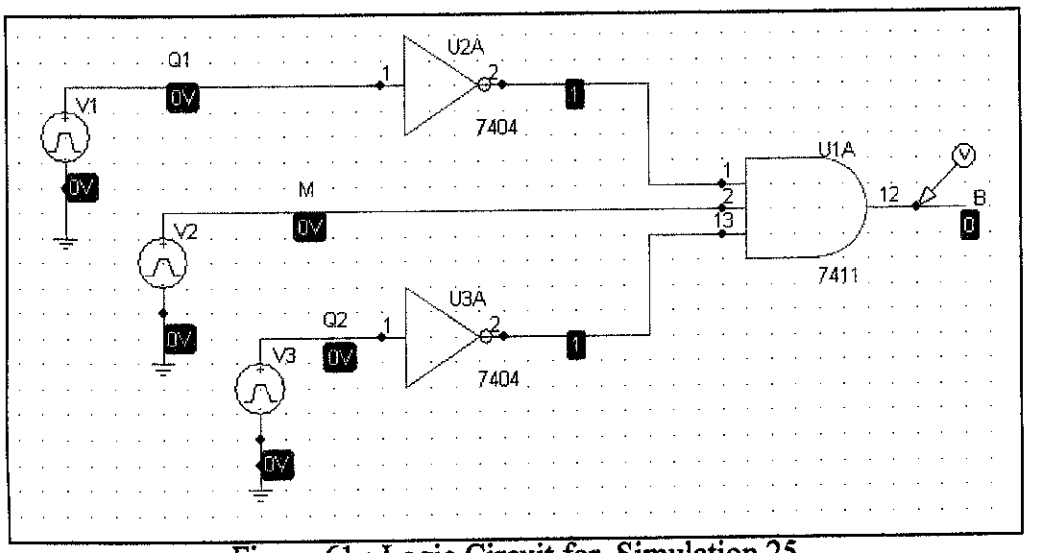

Figure 61 : Logic Circuit for Simulation 25

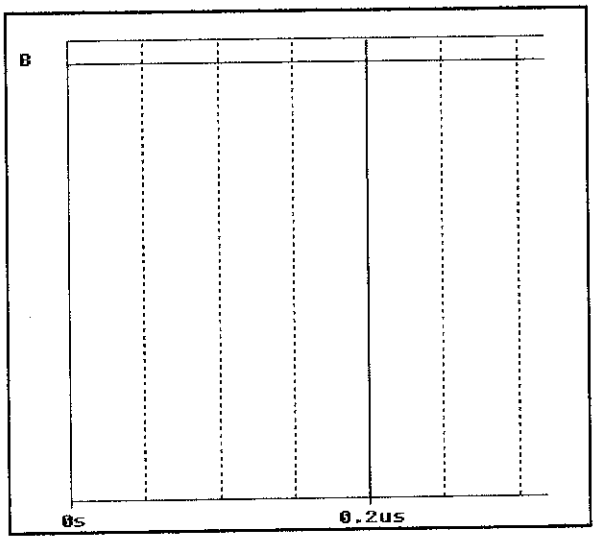

Figure 62 : Output Waveform for Simulation 25

Table 34 : Input-Output Table for Simulation 27

INPUT			OUTPUT
M	Q_1	Q_2	B
0	0	1	0

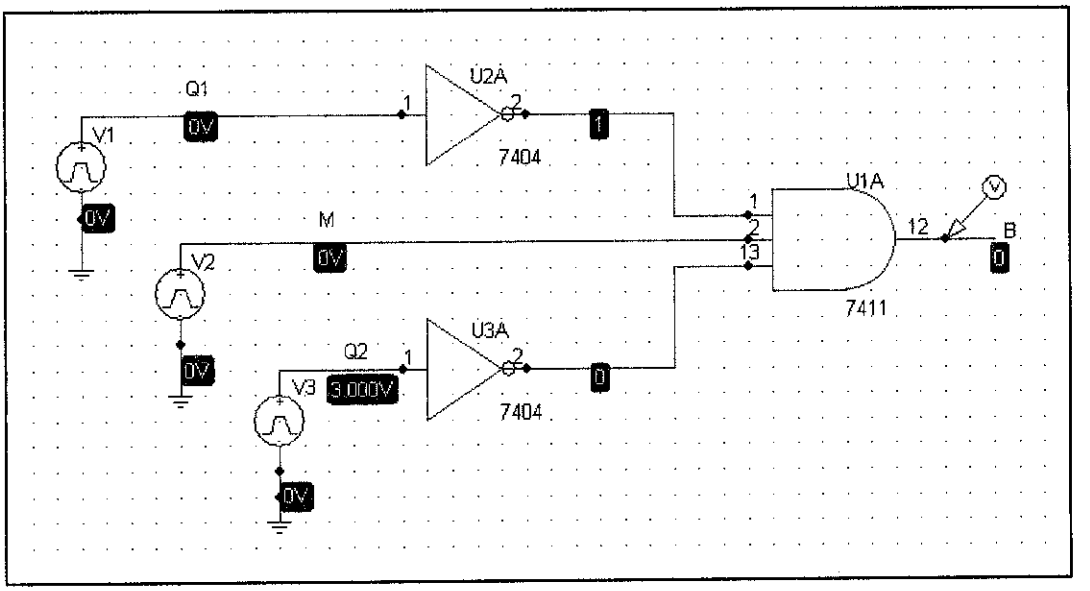

Figure 65 : Logic Circuit for Simulation 27

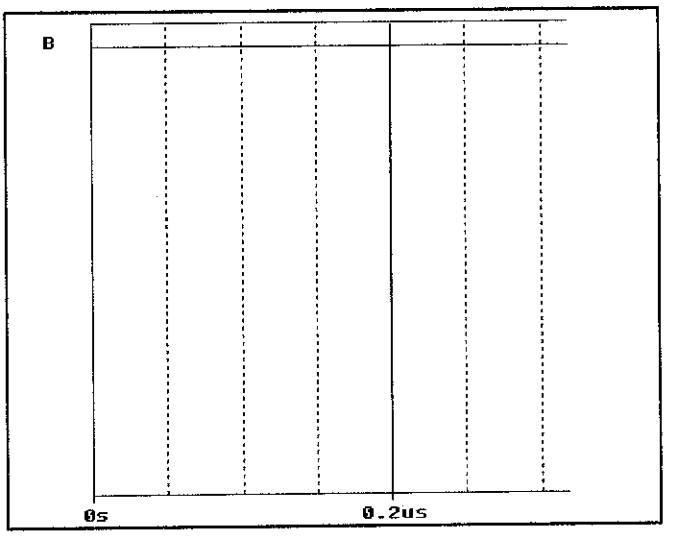

Figure 66 : Output Waveform for Simulation 27

Table 35 : Input-Output Table for Simulation 28

INPUT			OUTPUT
M	Q_1	Q_2	B
1	0	1	0

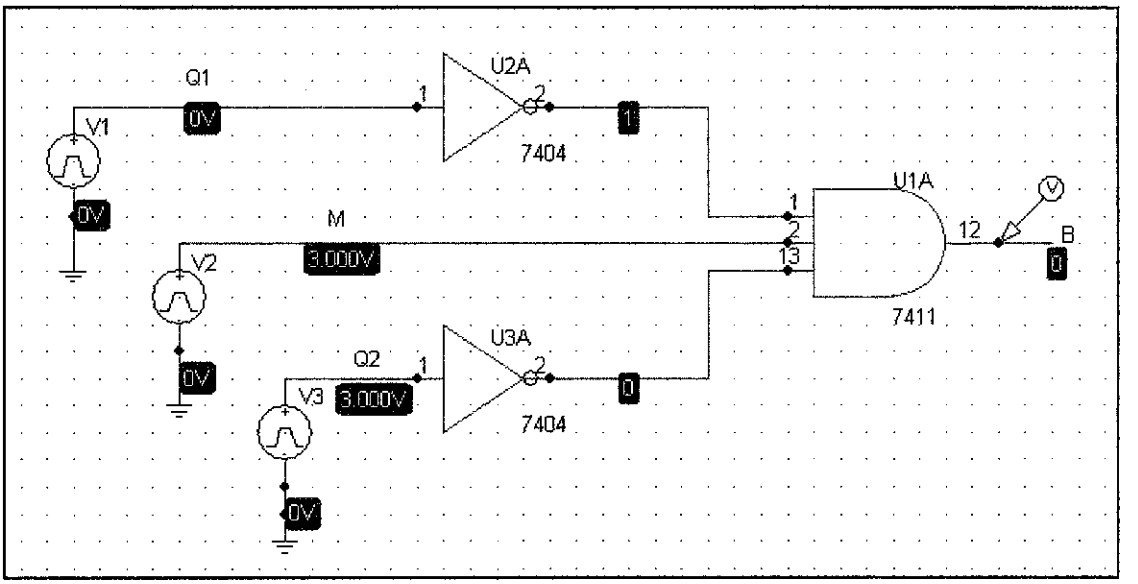

Figure 67 : Logic Circuit for Simulation 28

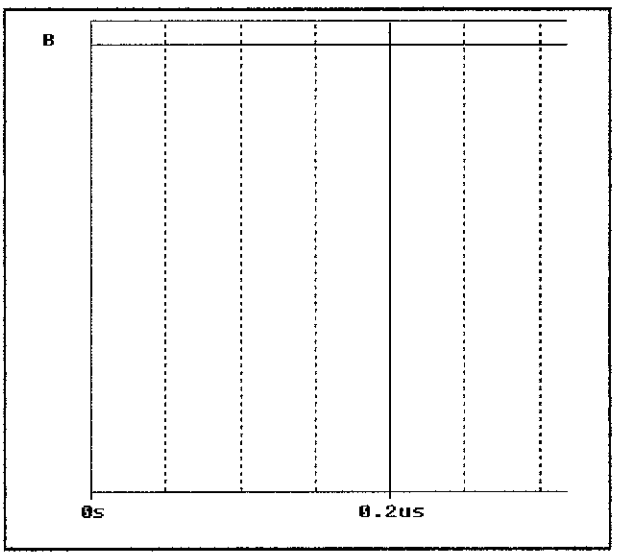

Figure 68 : Output Waveform for Simulation 28

Table 36 : Input-Output Table for Simulation 29

INPUT			OUTPUT
M	Q_1	Q_2	B
0	1	0	0

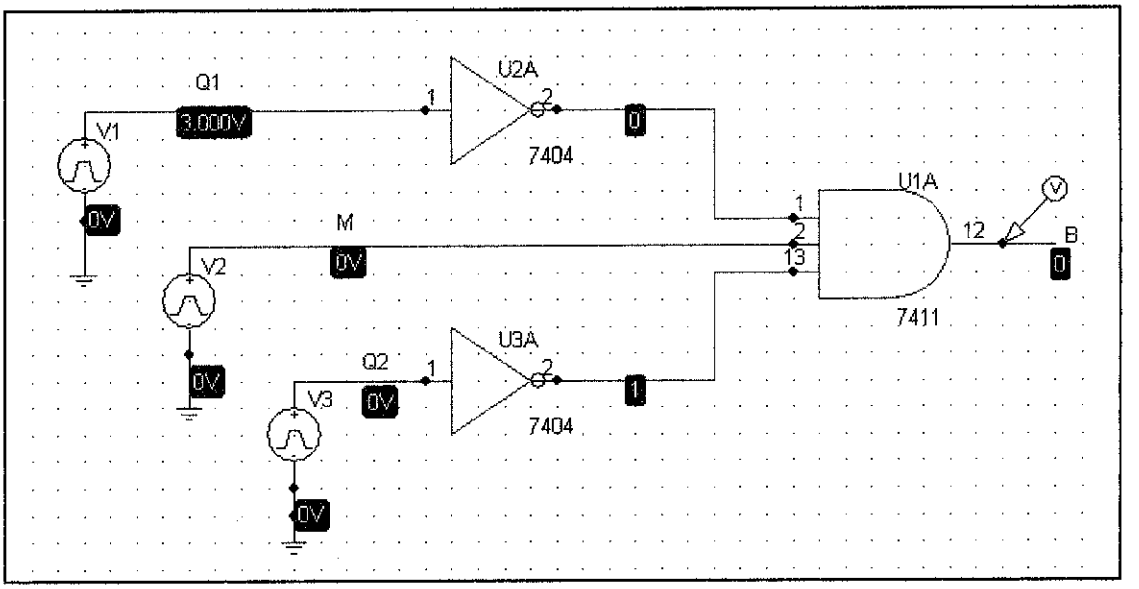

Figure 69 : Logic Circuit for Simulation 29

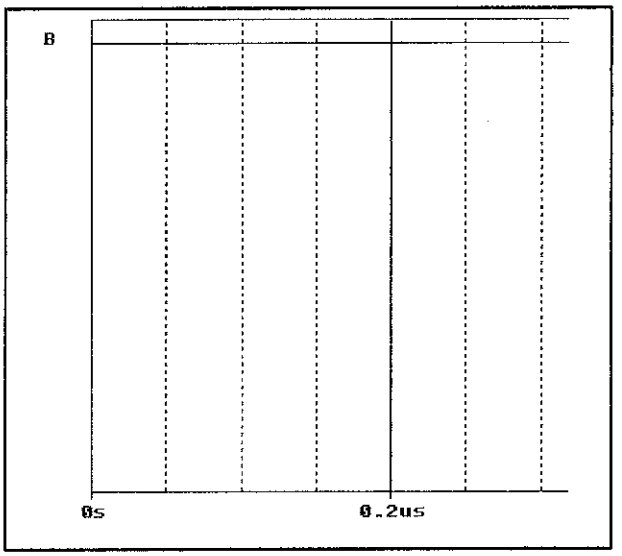

Figure 70 : Output Waveform for Simulation 29

Table 37 : Input-Output Table for Simulation 30

INPUT			OUTPUT
M	Q_1	Q_2	B
1	1	0	0

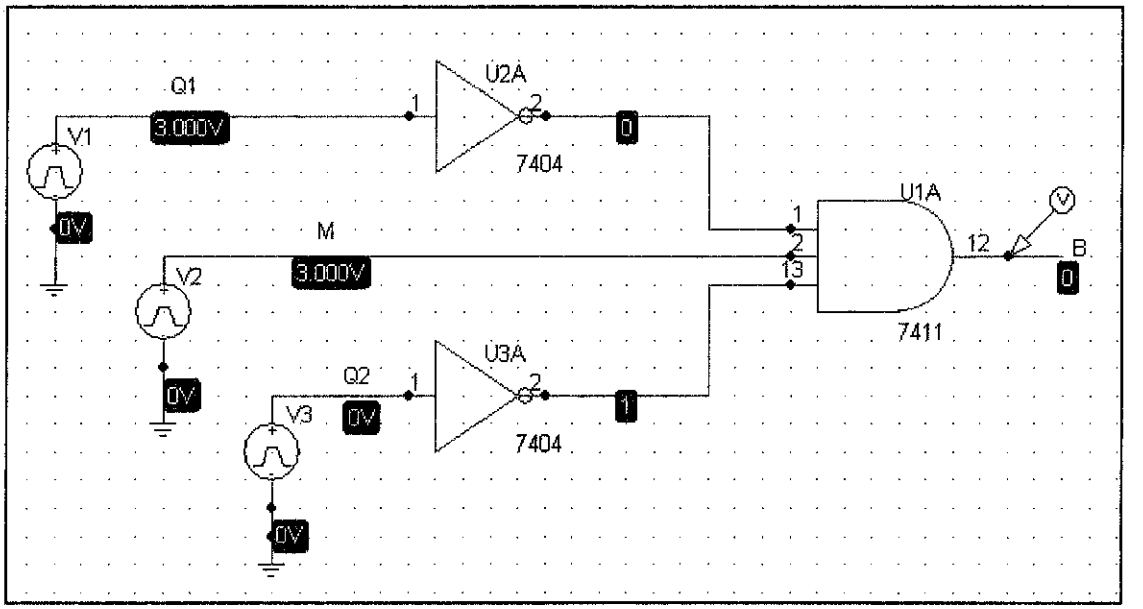

Figure 71 : Logic Circuit for Simulation 30

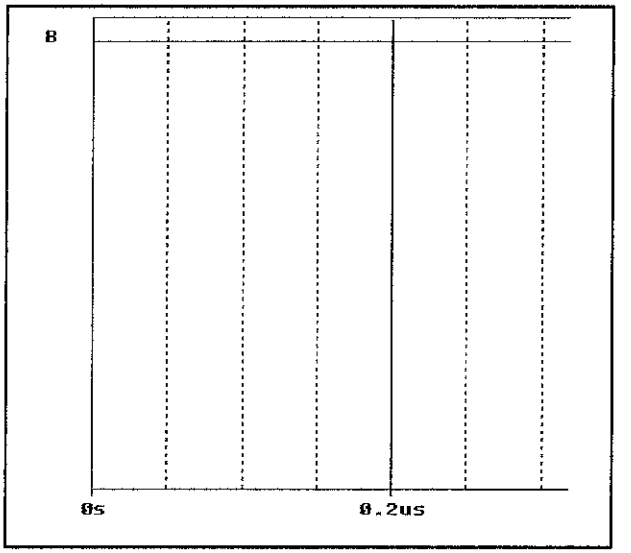

Figure 72 : Output Waveform for Simulation 30

Table 38 : Input-Output Table for Simulation 31

INPUT			OUTPUT
M	Q_1	Q_2	B
0	1	1	0

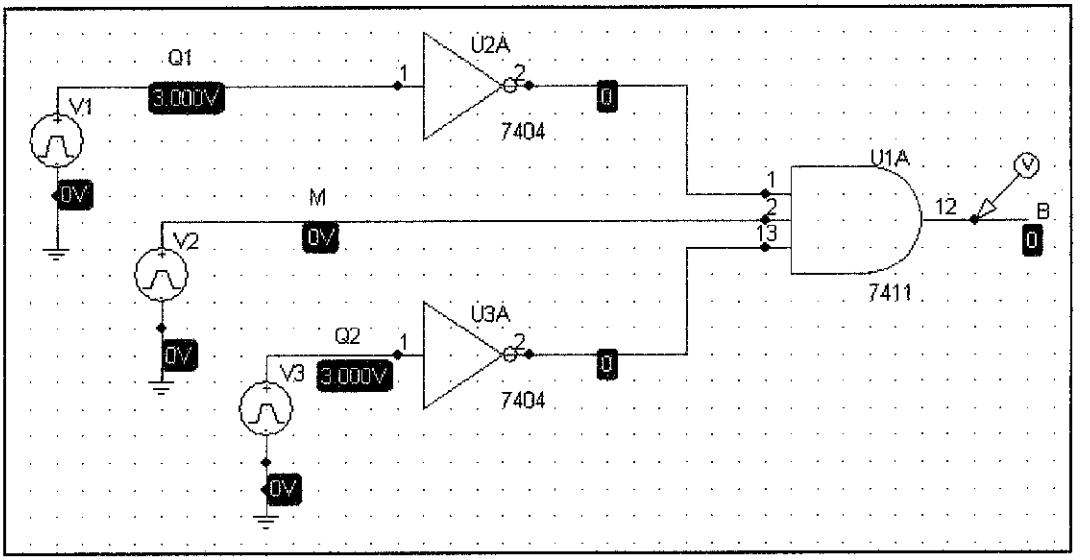

Figure 73 : Logic Circuit for Simulation 31

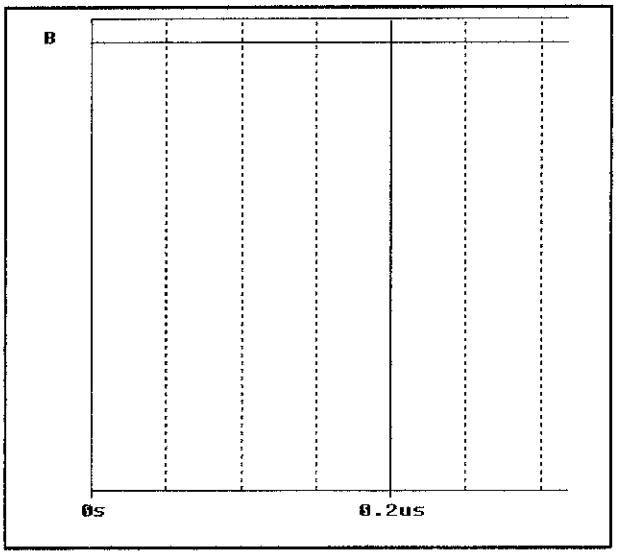

Figure 74 : Output Waveform for Simulation 31

Table 39 : Input-Output Table for Simulation 32

INPUT			OUTPUT
M	Q_1	Q_2	B
1	1	1	0

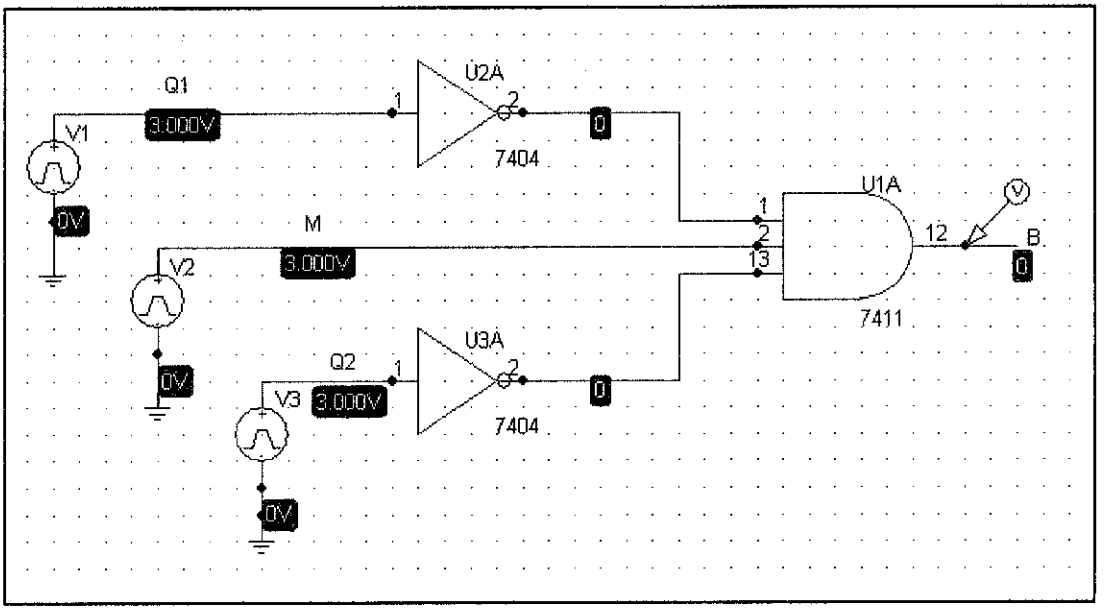

Figure 75 : Logic Circuit for Simulation 32

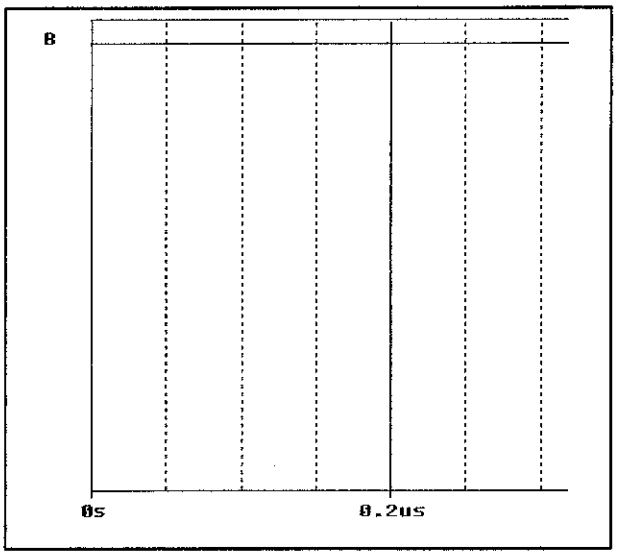

Figure 75 : Output Waveform for Simulation 32

4.1.2 Circuit Implementation Test Results

The results of the test are as shown in the table below:

Table 40 : Results of the Circuit Test Using LEDs

INPUT				OUTPUT						
C	**M**	**Q_1**	**Q_2**	**Q_1'**	**LED before D flip-flop**	**LED after D flip-flop**	**Q_2'**	**LED before D flip-flop**	**LED after D flip-flop**	**B**
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1	1	0	0
0	1	0	0	0	0	0	0	0	0	1
1	1	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	1	1	0	0
1	0	0	1	0	0	0	1	1	0	0
0	1	0	1	1	1	0	0	0	0	0
1	1	0	1	1	1	0	0	0	0	0
0	0	1	0	1	1	0	1	1	0	0
1	0	1	0	1	1	0	1	1	0	0
0	1	1	0	1	1	0	0	0	0	0
1	1	1	0	1	1	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0
0	1	1	1	1	1	0	1	1	0	0
1	1	1	1	1	1	0	1	1	0	0

For the test of LEDs before the D flip-flop, both Q_1' and Q_2' satisfy the next state table. This means that the circuit is working as desired. While for the LEDs after the flip-flop, both Q_1' and Q_2' did not satisfy the next state table. The LEDs for both outputs Q_1' and Q_2' did not light up for every input combination. This is because the clocks for the D flip-flops are not triggered. Thus, another test will be conducted in the future with the triggering clocks for the D flip-flops are set. For the LED connected to output B, the results are same as desired.

4.2 Discussion

The circuit of the state machine has been tested. This circuit is supplied by 5V power supply. In conducting the test on the circuit, the inputs of this circuit that are named as C, M, Q_1 and Q_2 are supplied with 0V if the input is 0 and they are supplied by 2V if the input is 1.

The output of this circuit is seen by connecting the LEDs at the outputs. When the output should be 0, the LED did not light up while when the output is 1, the LED lights up. Another test will be conducted soon with the clocks for the D flop-flops are set to get the desired results. The test is done one by one according to the next-state table.

CHAPTER 5
CONCLUSIONS AND RECOMMENDATIONS

5.1 Conclusions

This project on data retrieval system is very significant to be developed in order to provide a way for the users to retrieve information. This project will definitely benefit not only the users but also the system coordinator where the data can be managed properly. For the first part of FYP, after doing some literature review, the focus is more on designing the circuits and implementation of circuits for this system.

The design of the overall circuit has been completed. This project is now in the hardware implementation and testing stage. The overall circuit is divided into small parts according to their functions. As for the time being, the circuit that has been completely built is only the circuit for the state machine and it has been tested. Some corrections need to be done to the state machine circuit where the D flip-flops need to be connected to a clock. The other circuits will be implemented as soon as the state machine's circuit is tested and proved it is working as designed earlier.

5.2 Recommendations

For further development and improvement on this project in the future, these are some recommendations that perhaps could be considered. Add the amount of data that can be stored in this system. This can be done by using other memory such as a 16 bit memory and others that can provide a bigger memory size. Other than that, the access time of this system could also be shorten. This will add up the value and the reliability of this system.

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