POWER POINT TRACKING CONTROLLER FOR PHOTOVOLTAIC (PV) ARRAY

By

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FINAL PROJECT REPORT

Submitted to the Electrical & Electronics Engineering Programme
in Partial Fulfillment of the Requirements
for the Degree
Bachelor of Engineering (Hons)
(Electrical & Electronics Engineering)

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CERTIFICATION OF APPROVAL

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Approved:

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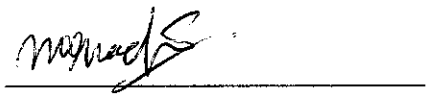
Project Supervisor

UNIVERSITI TEKNOLOGI PETRONAS
TRONOH, PERAK

June 2006

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.



Nornadia Salmee bt Salehuddin

ABSTRACT

There is a need for the applications of photovoltaic (PV) system in Malaysia, due to the rising of world oil prices. Malaysia is well endowed with non – renewable and renewable energy source. Bulk of our electricity demand is met by the use of fossil – fuel based electrical power plants. TNB's current energy generation mix is approximately 35% coal, 34.7% natural gas and 18.26% hydro with the remaining 12.1% from oil, gas and diesel for a combined installed capacity of 10481 MW. A shift towards alternative energy such as solar energy, one of the abundant energy in Malaysia, is essential. There are many initiatives have been initiated in moving towards the development of solar energy in Malaysia. Use of PV in harnessing solar energy to generate electricity is a proven technology, but the utilization of PV is not optimized. PV cell is expensive and the efficiency of PV is relatively low. A good tracking system is crucial in order to optimize PV performance in generating electricity. Thus, in this project the focus is in designing a system that will track the sun for better PV performance. A hybrid tracking system is introduced in this project, where it consists of two controlling methods. The automatic controller system will control the motion of the tracker in East – to – West direction, while the manual system will control North – to – South motion. As a conclusion, this project offers simple yet practical system that can help to improve the efficiency of the PV related system.

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Alhamdulillah, all praises be to Him for succeeded me in completing my Final Year Project for two semesters. Without His blessing, the project is impossible to be completed.

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

Abbreviation	Description
CW	Clockwise
EEPROM	Electrically Erasable Programmable Read Only Memory
PV	Photovoltaic
RAM	Random Access Memory
N	North
S	South
E	East
W	west

NOMENCLATURE

Symbol	Description and Reference
μm	Micro meter
^0C	Degree Celcius
CH_4	Methane
CO	Carbon monoxide
CO_2	Carbon dioxide
E	Equation of time
h	hour
$\overline{H}$	Monthly mean of the daily global solar radiation
H_0	Daily horizontal extraterrestrial solar radiation
$\overline{H_o}$	Monthly mean of the daily extraterrestrial
$\overline{H_d}$	Monthly mean of the daily diffusion radiation
I_b	Beam or direct radiation
$\overline{I_b}$	Hourly mean beam radiation
I_d	Diffuse radiation
$\overline{I_d}$	Hourly mean diffuse radiation
$\overline{I_G}$	Hourly mean global radiation
I_{ext}	Extraterrestrial radiation
I_{Global}	Global radiation
I_{sc}	Solar constant
$\overline{K_T}$	Monthly average clearness index
kJ	Kilo Joule
L_{loc}	Local meridian of the location
L_{st}	Standard meridian for the local time zone
m^2	Square meter (dimension or area)
MJ	Mega Joule
MW	Mega watt
n	Number of days

nm	Nano meter
NO_2	Nitrogen dioxide
rads	radians
R_b	Ratio of beam radiation on a tilted surface to the radiation on a horizontal surface
R_d	Ratio of diffuse radiation on a tilted surface to the radiation on a horizontal surface
t_l	Standard time
t_s	Solar time
V	Volt
W	Watt

Greek Symbol	**Description and Reference**
β	Slope of the plane
α	Altitude angle
α_s	Solar altitude angle
γ	Surface azimuth angle
γ_s	Solar altitude angle
δ	Declination angle
θ	Angle between an incident beam of flux I_b and the normal to plane surface
θ_i	Angle of incidence
θ_z	Zenith angle
ω	Hour angle
ω_s	Sunset hour angle

CHAPTER 1
INTRODUCTION

The use of solar energy in daily activity is nothing new. As an example in 1830s, British astronomer John Herschel used a solar collector box to cook food during the expedition to Africa. Now, people are trying to use the sun's energy for a lot of things including generating electricity (Smith, 1995).

1.1 Background of Study

In this section, a brief introduction to solar energy technology will be explained especially photovoltaic (PV).

1.1.1 Solar Energy

The Earth's surface receives so much solar energy from the sun everyday, thus making it as an inexhaustible source of energy. The power from the sun that is intercepted by the earth is about 1.8×10^{11} MW, which is many thousands of times larger than the present consumption rate on the earth of all commercial energy sources (Sukhatme, 1996). Thus, solar energy could supply all the present and future energy needs for the world. This makes it one of the most promising renewable energy sources.

There is a considerable interest, research effort and funding in this field. This worldwide interest is attributed to a variety of factors such as search for new energy due to heavy pressure on conventional fuels, simplicity, cleanliness and direct conversion into electricity. Regarding these benefits, Malaysia is now moving towards this solar resource. In the Eighth Malaysian Plan, renewable energy was announced as the fifth fuel in the new five fuel strategy in the energy supply mix. It is targeted that renewable source will able to contribute 5% of the country's total electricity demand (KTKM, 2005).

Solar energy is used in two primary forms. One of it is thermal solar, where the heat of the sun is used to heat water or other working fluid, which later drives turbines or other machinery to create electricity. Such application of thermal are water heating, space heating, power generation space cooling and refrigeration and etc. Another form is photovoltaic, where it generates or produces electricity directly without any moving parts. Photovoltaic is the example which produces electricity directly from the sun. Photovoltaic conversion is useful for several reasons. Conversion from sunlight to electricity is direct; therefore, mechanical generator systems are unnecessary. The modular characteristic of photovoltaic energy allows arrays to be installed quickly and in any size required or allowed.

1.1.2 Photovoltaic (PV)

PV captures the sun's energy and converts it to electricity. Today there is more study being done on solar PV systems. The wide acceptance and utilization of the PV cells or arrays in generation of electricity depends on reducing the cost of the power generated and improving the energy efficiency of PV systems. A major advantage of PV cells is it can directly convert the solar radiation into electricity using PV effect without going through a thermal process. This can reduce cost on the equipment or setup of the system. Besides that, PV is reliable, modular and maintenance free and therefore, suitable even in isolated and remote areas. In addition, PV is quiet, benign, compatible with almost all environments, responds instantaneously with solar radiation, and have an expected lifetime of 20 years (EERE Energy, 2005).

There are a lot of studies being done on the method of tracking the sun using PV. In Malaysia, government has invested about RM 4.9 million for PV projects (KTKM, 2005). The installation of solar PV cells in the country is done mainly in rural areas, where there is difficulty in setting up the electricity cables or it is used by individual in their private homes.

A photovoltaic cell is usually made from silicon alloys. The silicon has dopant atoms introduced to create a p-type and an n-type region and thereby producing a p-n junction. This doping can be done by high temperature diffusion or ion implantation.

Actually, there are many other methods of doping silicon. The introduction of dopants into silicon can be done during the deposition of the films or layers (Reslab, 2006).

To understand the operation of a PV cell, both the nature of the material and the nature of sunlight need to be considered. PV cells consist of two types of material, often p-type silicon and n-type silicon. Light of certain wavelengths is able to ionize the atoms in the silicon and the internal field produced by the junction separates some of the positive charges (holes) from the negative charges (electrons) within the photovoltaic device. The holes are swept into the positive or p-layer and the electrons are swept into the negative or n-layer. Although these opposite charges are attracted to each other, most of them can only recombine by passing through an external circuit outside the material because of the internal potential energy barrier. Therefore if a circuit is made as in Figure 1, power can be produced from the cells under illumination, since the free electrons have to pass through the load to recombine with the positive holes (Reslab, 2006).

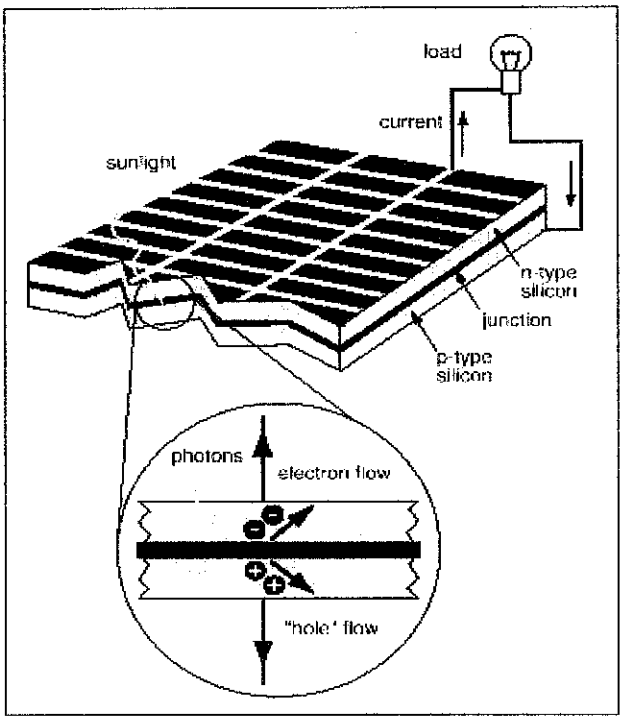


Figure 1 The PV effect in solar cell (Reslab, 2006)

1.1.3 Types of PV

Silicon solar cells are made using single crystal (monocrystalline) wafers, polycrystalline wafers or thin films.

Single Crystal Silicon Cell

Single crystal silicon cells are thin wafers about 300μm in thickness, sliced from a large single crystal ingot which has been grown at around 1400 °C, which is a very expensive process. The silicon must be of very high purity and have a near perfect crystal structure (Reslab, 2006).

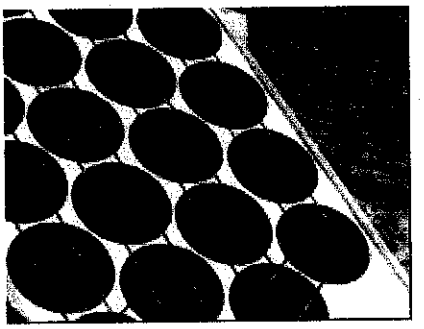


Figure 2 Single crystal solar cells in panel (Reslab, 2006)

Polycrystalline Silicon Cell

Polycrystalline wafers are made by a casting process in which molten silicon is poured into a mould and allowed to set. Then it is sliced into wafers (Figure 2). As polycrystalline wafers are made by casting they are significantly cheaper to produce, but not as efficient as single crystal cells. The lower efficiency is due to imperfections in the crystal structure resulting from the casting process (Reslab, 2006).

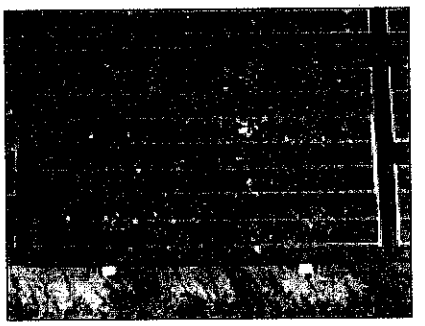


Figure 3 Polycrystalline solar panel (Reslab, 2006)

Thin – Film Silicon

Amorphous silicon, one of the thin film technologies, is made by depositing silicon onto a glass substrate from a reactive gas such as Silane (SiH4). This type of solar cell can be applied as a film to low cost substrates such as glass or plastic. Other thin film technologies include thin multicrystalline silicon, copper indium diselenide/cadmium sulphide cells, cadmium telluride/cadmium sulphide cells and gallium arsenide cells. There are many advantages of thin film cells including easier deposition and assembly, the ability to be deposited on inexpensive substrates or building materials, the ease of mass production, and the high suitability to large applications (Reslab, 2006).

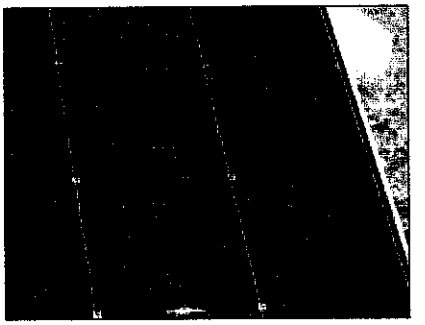


Figure 4 Thin – film solar panel (Reslab, 2006)

1.2 Problem Statement

Solar energy has been commercialized ever since there was a need for alternative energy sources. Our country has invested a lot of money in solar project especially for those projects that use PV (NST, 2005). However, the utilization of PV in the project is not optimized. Currently, all the solar tracking systems that are being applied are in stand – still mode regardless to the position of the sun. Example of project that utilized PV was set up in Pulau Pemanggil, Johor (NST, 2005). It used static PV to track the sun. PV becomes less efficient when its position is not directly facing the sun. To overcome the problem, an active solar tracker is introduced where the system can follow the sun's track from its rising to its setting. It will keep the PV cell facing the sun all the times. Therefore, the system can get better input from the sunshine and the PV performance can be better.

1.3 Objective and Scope of Study

The objectives of this project are:

1. To study and do modeling on solar geometry – sun's path
2. To build prototype of solar tracker
3. To mount PV on the solar tracker
4. To verify the tracker PV assembly performance under actual local meteorological conditions.

There are several aspects that need to be focused on this project. The divisions of the project components are as follows:

1. The study on solar radiation on earth, basically focus on Malaysia solar radiation.
2. The study on the tracking modes that can be used in this project.
3. The development of the system and its main components.

CHAPTER 2
LITERATURE REVIEW AND THEORY

2.1 Solar Radiation outside the Earth Atmosphere

Solar radiation is the electromagnetic radiation emitted by the sun, where most of the radiation is in the broadband solar radiation wavelength region of 280 nm to 4000 nm. The region of the spectrum that is visible to all of us is in the wavelength range of about 380 nm to 720 nm (Serway & Beichner, 2000). Solar radiation which can be converted to useful energy lies between 0.3 μm and 3.0 μm (Garg & Prakash, 1997).

Energy flux that is received from the sun outside the earth's atmosphere is essentially constant. The solar constant I_{sc} is the rate at which energy is received from the sun on a unit area perpendicular to the rays of the sun, at the mean distance of the earth from the sun (Sukhatme, 1996). The average intensity of solar radiation that is reaching the upper atmosphere is about 1353 W/m^2. However, based on subsequent measurements, a revised value of 1367 W/m^2 has been recommended (Frolich & Brusca, 1981). The difference between the two values is only 1%.

The earth revolves around the sun in an elliptical orbit having a very small eccentricity, and with the sun at one of the foci. Therefore, the distance between the sun and earth varies a little throughout the year. Because of this variation, the extraterrestrial flux also varies. The value of extraterrestrial radiation can be calculated by Equation (2.1) (Sukhatme, 1996),

$$I_{ext} = I_{sc}\left(1 + 0.033\cos\frac{360n}{365}\right) \tag{2.1}$$

where n is the day of the year.

2.2 Solar Radiation at the Earth's Surface

Solar radiation is received at the earth's surface in an attenuated form because it is subjected to the mechanisms of absorption and scatterings as it passes through the earth's atmosphere. Absorption occurs in the presence of ozone, water vapor and other gases (like CO_2, NO_2, CO, O_2 and CH_4), while scattering occurs due to all gaseous molecules as well as particulate matter in the atmosphere. The scattered radiation is redistributed in all directions, some going back into space and some reaching the earth's surface.

The atmosphere on the earth surface is often classified into two broad types – an atmosphere without clouds and an atmosphere with clouds. In the former case, the sky is cloudless, while the latter is partially or fully covered with clouds. It is obvious that less attenuation takes place in a cloudless sky. Consequently maximum radiation is received on the earth's surface under the condition of cloudless sky.

Solar radiation received at the earth's surface (in line with the sun) is known as beam or direct radiation, I_b. The radiation received at the earth's surface from all parts of the sky's hemisphere (after being subjected scattering in the atmosphere) is called as diffuse radiation, I_d. So the sum of the beam and diffuse radiation is referred to as global radiation.

$$I_{Global} = I_b + I_d \tag{2.2}$$

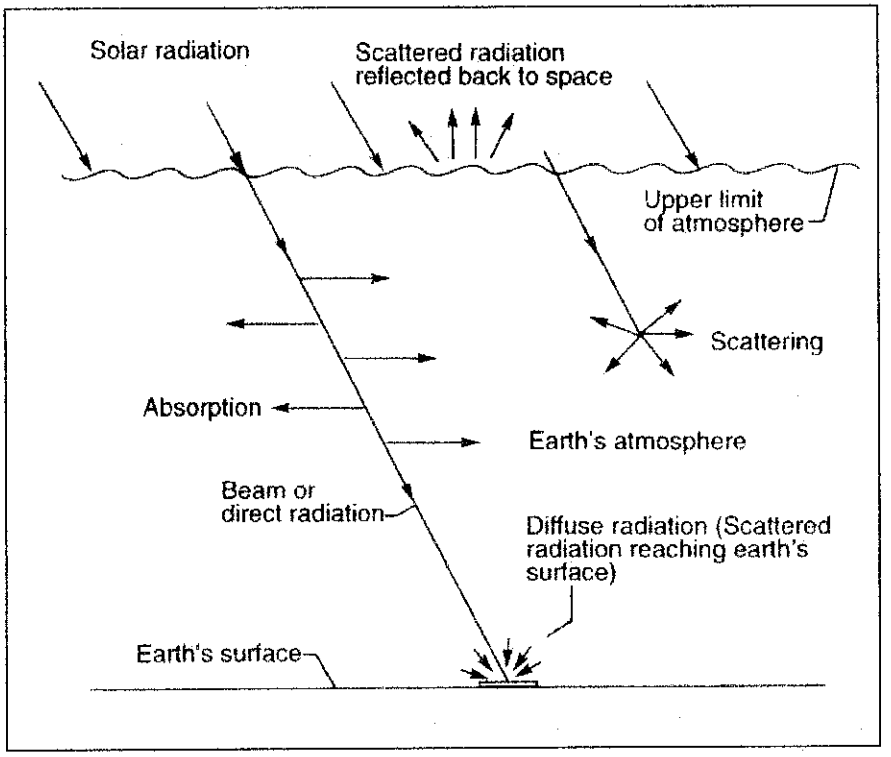


Figure 5 Schematic representation of (i) Mechanism of Absorption and Scattering , and (ii) Beam and Diffuse Radiation Received at the Earth's Surface (Sukhatme, 1996)

2.3 Solar Radiation Geometry

Identifying location of the sun relative to earth at all times during the day is the basic concept that is used in sun tracking systems. The rotation of earth around itself causes the sequence of day and night. Solar time is based on the apparent angular motion of the sun across the sky. At solar noon, the sun crosses the meridian of the observer, and this is used in all the sun – angle relationships, while the local time is determined according to political time zones and other approximations. The difference between the mean solar time and true solar time is called the equation of time, Equation (2.3) (M.Alata, 2004),

$$E = 229.2(0.000075 + 0.001868\cos B - 0.032077\sin B - 0.014615\cos 2B - 0.04089\sin 2B) \quad (2.3)$$

where

$$B = (n-1)\frac{360}{365} \quad \text{and} \quad 1 \le n \le 365$$

To convert the local standard time to solar time, Equation (2.4) (Alata, 2004) is used

$$t_s - t_1 = 4(L_{st} - L_{loc}) + E \tag{2.4}$$

where t_s is the solar time, t_1 is the standard time, L_{st} is the standard meridian for the local time zone and L_{loc} is the local meridian of the location. The **hour angle, ω** is the angular rotation of the sun to the east or west of the local meridian due to the rotation of the earth about its polar axis (morning negative and afternoon positive). ω is given by Equation (2.5) (Alata, 2004)

$$\omega = 15(t_s - 12) \tag{2.5}$$

The energy flux of beam radiation on a surface with any orientation can be obtained from the knowledge of flux either on a surface perpendicular to the sun rays or on a horizontal surface. If θ is the angle between an incident beam of flux I_b and the normal to a plane surface, then the equivalent flux falling normal to the surface is given by $I_b \cos\theta$. The angle θ can be related by a general equation to ϕ the latitude, δ the declination, γ the surface azimuth angle, ω the hour angle and β the slope.

Latitude (ϕ): The latitude of a location is the angle made by the radial line, joining the given location to the center of the earth, with it's projection on the equatorial plane. The latitude is positive for northern hemisphere and negative for southern hemisphere.

Declination (δ): Angle that is made by the line joining the centers of the sun and the earth and its projection on the equatorial plane. This declination angle is due to the rotation of the earth about its axis which makes an angle of 66.5^0 with the plane of it's rotation around the sun. The declination varies from a maximum value of 23.45^0 on June 21 to a minimum value of – 23.45^0 on December 21. To find the angle of declination Equation (2.6) (Alata, 2004) is used,

$$\delta = 23.5\sin\left(360\frac{284+n}{365}\right) \tag{2.6}$$

Zenith (θ_z): It is the angle between the sun's ray and perpendicular line to the horizontal plane.

Altitude (α): It is defined as the angle between the sun's ray and its projection in a horizontal plane. Also $\alpha = 90 - \theta_z$.

Solar altitude angle (α_s): It is the angle between the sun's ray and its projection in a horizontal plane. Usually $\alpha = \alpha_s$.

Slope (β): It is the angle in the horizontal plane, between the line due to the south and the projection of the normal to the surface (inclined plane) on the horizontal plane.

Solar azimuth angle (γ_s): It is the angle in a horizontal plane, between the line due south and the projection of beam radiation on the horizontal plane.

Angle of incidence (θ_i) : It is the angle between beam radiation on the surface and the normal to that surface.

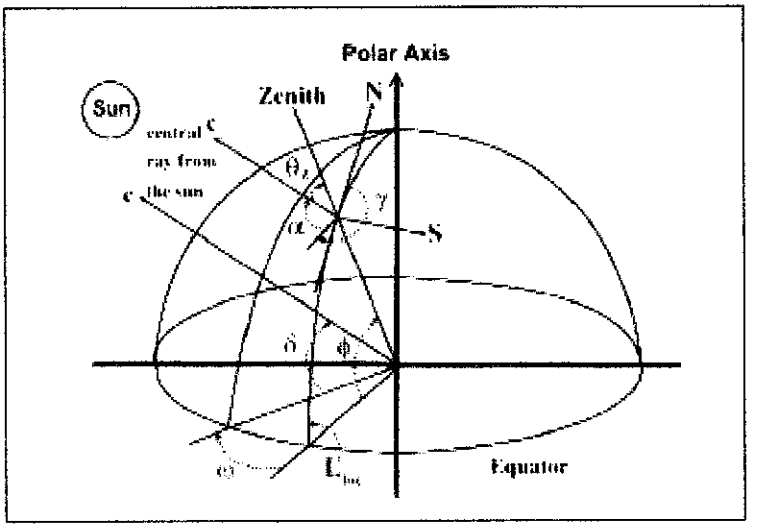


Figure 6 Schematic of representation of solar geometry (Alata, 2004)

In general, the angle of incidence is shown in Equation (2.7) (Sukhatme, 1996),

$$\cos\theta_i = \sin\phi(\sin\delta\cos\beta + \cos\delta\cos\gamma\cos\omega\sin\beta) + \cos\phi(\cos\delta\cos\omega\cos\beta - \sin\delta\cos\gamma\sin\beta) + \cos\delta\sin\gamma\sin\omega\sin\beta \quad (2.7)$$

2.4 Angle of Incidence for Tracking Mechanism

After understand the solar angles, especially the angle of incidence, the most suitable tracking mode is choose and will be implemented later. Basically there are five modes of tracking available. All of the modes will be discussed in the next section.

A plane or plate (PV array) is oriented with its focal axis pointed either in the east – west or the north – south direction. In the east – west orientation, the focal axis is horizontal, while in the north – south orientation, the focal axis may be horizontal or inclined. The various tracking modes are as follows.

2.4.1 Mode I

The focal axis for this mode is east – west and horizontal. The PV is rotated about a horizontal E – W axis and adjusted on daily basis. This is done so that the solar beam is normal to the PV plane at solar noon on that day. In this mode, the plane is an imaginary surface with either $\gamma = 0^0$ or $\gamma = 180^0$. The case of $\gamma = 0^0$ occurs when $(\phi - \delta) > 0$, while the case of $\gamma = 180^0$ occurs when $(\phi - \delta) < 0$. So to find the slope, β of the plane, the condition at solar noon ($\omega = 0^0$, $\theta = 0^0$) is substituted into Equation (2.7). Thus yields Equation (2.8) and (2.9) (Sukhatme, 1996),

$$\beta = (\phi - \delta) \qquad for \quad \gamma = 0° \quad (2.8)$$

and

$$\beta = (\delta - \phi) \qquad for \quad \gamma = 180° \quad (2.9)$$

So the angle of incidence for both cases are as in Equation 2.10 (Sukhatme, 1996),

$$\cos\theta = \sin^2\delta + \cos^2\delta\cos\omega \quad (2.10)$$

2.4.2 Mode II

For this second mode, the focal axis is still east – west and horizontal. But then the PV array is now rotated about a horizontal E – W axis and adjusted continuously so that the solar beam makes the minimum angle of incidence with the plane at all times. In this mode also the plane is an imaginary surface with either $\gamma = 0^0$ or $\gamma = 180^0$. In order to get θ minimum, right hand side of Equation (2.7) is differentiated with respect to β and equates it to zero. The equation yields as in Equation (2.11) and (2.12) (Sukhatme, 1996),

$$\tan(\phi - \beta) = \tan\delta / \cos\omega \qquad for \quad \gamma = 0° \tag{2.11}$$

and

$$\tan(\phi + \beta) = \tan\delta / \cos\omega \qquad for \quad \gamma = 180° \tag{2.12}$$

Equation (2.11) and (2.12) can be used to find the slope of the plane. Equation (2.11) is used if the magnitude of γ_s is less than 90^0, while Equation (2.12) is used if the magnitude of γ_s is greater than 90^0. So for both cases, the angle of incidence is as in Equation (2.13) (Sukhatme, 1996),

$$\cos\theta = \sqrt{\left(1 - \cos^2\delta \sin^2\omega\right)} \tag{2.13}$$

2.4.3 Mode III

The focal axis is north – south and horizontal. The plane is rotated about a horizontal N – S axis and adjusted continuously so that the solar beam makes the minimum angle of incidence with the plane all the time. For this type of mode, the surface azimuth angle $\gamma = +90^0$ before noon and -90^0 after noon. Thus before noon Equation (2.7) becomes

$$\cos\theta = (\sin\phi\sin\delta + \cos\phi\cos\delta\cos\omega)\cos\beta + \cos\delta\sin\omega\sin\beta \tag{2.14}$$

To find minimum θ, right hand side of Equation (2.14) (Sukhatme, 1996) is differentiated with respect to β and equates to zero. The equation become as in Equation (2.15) (Sukhatme, 1996),

$$\beta = \tan^{-1}\left[\frac{\cos\delta\sin\omega}{\sin\phi\sin\delta + \cos\phi\cos\delta\cos\omega}\right] \tag{2.15}$$

The expression of the corresponding minimum angle of incidence is obtained by substituting Equation (2.15) in Equation (2.14) giving Equation (2.16) (Sukhatme, 1996),

$$\cos\theta = \sqrt{(\sin\phi\sin\delta + \cos\phi\cos\delta\cos\omega)^2 + \cos^2\delta\sin^2\omega} \tag{2.16}$$

After noon, with γ = - 90^0, the slope equation is given by Equation (2.17) (Sukhatme, 1996),

$$\beta = \tan^{-1}\left[\frac{-\cos\delta\sin\omega}{\sin\phi\sin\delta + \cos\phi\cos\delta\cos\omega}\right] \tag{2.17}$$

The expression for angle of incidence remains the same.

2.4.4 Mode IV

The focal axis is north – south and inclined at a fixed angle equal to the latitude. Thus it is parallel to the earth's axis. The plane is rotated about an axis parallel to the earth's axis at an angular velocity equal and opposite to the earth's rate of rotation (15^0 per hour). It is adjusted such that at solar noon the plane is an inclined surface facing due south. Thus, by substituting $\beta = \phi$ and $\omega = 0$ in Equation (2.17), yields Equation (2.18) (Sukhatme, 1996),

$$\cos\theta = \cos\delta \tag{2.18}$$

2.4.5 Mode V

The focal axis is north – south and inclined. The plane is rotated continuously (but not at a constant angular velocity) about an axis parallel to the focal axis, as well as about a horizontal axis perpendicular to this axis, and adjusted so that the solar beam is normally incident on the plane at all times. In this situation, angle of incidence, cos θ = 1. It is easy to show that at solar noon, $\beta = |\phi - \delta|$.

2.5 Global Radiation Separation Method

Usually, the solar radiation data obtained from the local meteorological department is the global or total solar radiation. The data is measured for horizontal surfaces and includes both direct and diffuse radiation. Direct or commonly referred to, as beam radiation is one of the components of global radiation, besides diffuse radiation. In the performance analysis of a tracking mechanism, it is important to separate the beam radiation from diffuse radiation.

2.5.1 Extraterrestrial Solar Radiation on Horizontal Surface

Earlier, Equation (2.1) gave the value of I_{ext}, the extraterrestrial solar radiation that would be received by a surface if there were no atmosphere. In the calculation of daily solar, radiation, it is necessary to have the extraterrestrial solar radiation arriving on a horizontal surface to be integrated for daily solar insolation. The following Equation (2.19) gives the daily horizontal extraterrestrial solar radiation obtained for the period from sunrise to sunset (Klein, 1977).

$$H_O = 27490.9 I_{ext}\left[\cos\phi\cos\delta\sin\omega_s + \left(\frac{11}{630}\omega_s\sin\phi\sin\delta\right)\right] \qquad (2.19)$$

Here the angle ω_s is the sunset hour angle and is obtained when the zenith angle θ_Z equals to 90°. Equation (2.20) gives the expression for zenith angle θ_Z, which will be used to derive Equation (2.21) by using θ_Z equals to 90° (Goswami *et al.*, 2000).

$$\cos\theta_Z = \cos\delta\cos\phi\cos\omega + \sin\delta\sin\phi \qquad (2.20)$$

$$\omega_s = \cos^{-1} - \tan\phi\tan\delta \qquad (2.21)$$

The monthly mean of the daily extraterrestrial solar radiation $\bar{H}_o$ is obtained by using n and δ for the mean day of a particular month. Once the value of $\bar{H}_o$ is obtained, together with the horizontally measured monthly mean of the daily global solar radiation $\bar{H}$, the monthly average clearness index can be determined by using Equation (2.22) (Rabl, 1985).

$$\overline{K}_T = \frac{\overline{H}}{\overline{H}_O} \tag{2.22}$$

2.5.2 Monthly Mean of the Daily Diffuse Radiation

To estimate the fractions of global horizontal solar radiation that is beam and diffuses, Equation (2.23) that was developed by Page (1961) can be used. The correlation is used to estimate the monthly mean of the daily diffuse radiation, for latitudes between 40° N and 40°S.

$$\overline{H}_d = (1.000 - 1.130\overline{K}_T)\overline{H} \tag{2.23}$$

The estimated value of $\overline{H}_d$ is based on $\overline{H}$, which is the measured value for monthly mean of daily global horizontal radiation.

2.5.3 Monthly Mean of the Hourly Diffuse Radiation

The last step in obtaining the desired hourly mean diffuse solar radiation is by using the correlation developed by Liu & Jordan (1960). The correlation is given as Equation (2.24) and uses the hour angle ω as well as sunset hour angle ω_s (Liu & Jordan, 1960).

$$\bar{I}_d = \frac{11\overline{H}_d}{84}\left(\frac{\cos\omega - \cos\omega_s}{\sin\omega_s - \frac{11}{630}\omega_s\cos\omega_s}\right) \tag{2.24}$$

Once the hourly mean diffuse solar radiation is determined, the hourly mean beam solar radiation I_b can be obtained by using a simple relationship as given by Equation (2.25), where $\bar{I}_G$ is the measured hourly mean horizontal global radiation (Magal, 1990).

$$\bar{I}_b = \bar{I}_G - \bar{I}_d \tag{2.25}$$

2.6 Hourly Solar Radiation on Tilted Surface

Since the global solar radiation provided by the local meteorological department is measured horizontally, there is a need to calculate the hourly radiation on tilted surfaces. This is essential for the purpose of designing a solar thermal device and to carry out performance analysis of the whole system.

The geometric factor R_b that is the ratio of beam radiation on a tilted surface to the radiation on a horizontal surface will be useful to calculate the amount of solar radiation that is received by the tilted surface of solar collectors. The evaluation of R_b involves the angle of incidence θ and zenith angle θ_z. The relationship between these two angles is given in Equation (2.26) (Liu & Jordan, 1961).

$$R_b = \frac{\cos\theta}{\cos\theta_z} \tag{2.26}$$

The diffuse component of solar radiation also uses a factor R_d to calculate the diffuse radiation on tilted surfaces. The factor R_d is defined as the ratio of diffuse radiation on a tilted surface to diffuse radiation on a horizontal surface. The value of R_d can be obtained by using Equation 2.27 (Liu & Jordan, 1961).

$$R_d = \frac{1+\cos\beta}{2} \tag{2.27}$$

2.7 Stepper Motor

For applications where precise measuring of a motors position is critical, stepper motor is the best choice. Stepper motors operate differently from other motors; rather than voltage being applied and the rotor spinning smoothly, stepper motors turn on a series of electrical pulses to the motor's windings. Each pulse rotates the rotor by an exact degree. These pulses are called steps, hence the name "stepper motor" (Images Si Inc., 2006).

2.7.1 Principle of Operation

Stepper motors consist of a permanent magnet rotating shaft, called the rotor, and electromagnets on the stationary portion that surrounds the motor, called the stator. Figure 7 illustrates one complete rotation of a stepper motor. At position 1, we can see that the rotor is beginning at the upper electromagnet, which is currently active (has voltage applied to it). To move the rotor clockwise (CW), the upper electromagnet is deactivated and the right electromagnet is activated, causing the rotor to move 90 degrees CW, aligning itself with the active magnet. This process is repeated in the same manner at the south and west electromagnets until we once again reach the starting position (Images Si Inc., 2006).

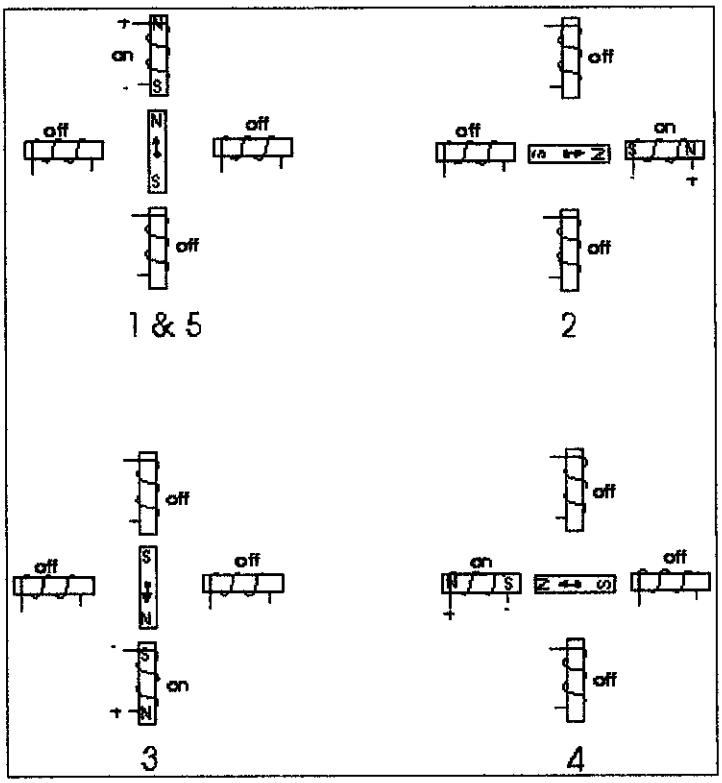


Figure 7 Complete rotation of a stepper motor (Images Si Inc., 2006)

In the above example, motor with a resolution of 90 degrees is used for demonstration purposes. In reality, this would not be a very practical motor for most applications. The average stepper motor's resolution -- the amount of degrees rotated per pulse -- is much higher than this. For example, a motor with a resolution of 5 degrees would move its rotor 5 degrees per step, thereby requiring 72 pulses (steps) to complete a full 360 degree rotation (Images Si Inc., 2006).

The resolution of some motors may be double by a process known as "half-stepping". Instead of switching the next electromagnet in the rotation on one at a time, with half stepping you turn on both electromagnets, causing an equal attraction between, thereby doubling the resolution. In Figure 8 it shows that in the first position only the upper electromagnet is active, and the rotor is drawn completely to it. In position 2, both the top and right electromagnets are active, causing the rotor to position itself between the two active poles. Finally, in position 3, the top magnet is deactivated and the rotor is drawn all the way right. This process can then be repeated for the entire rotation (Images Si Inc., 2006).

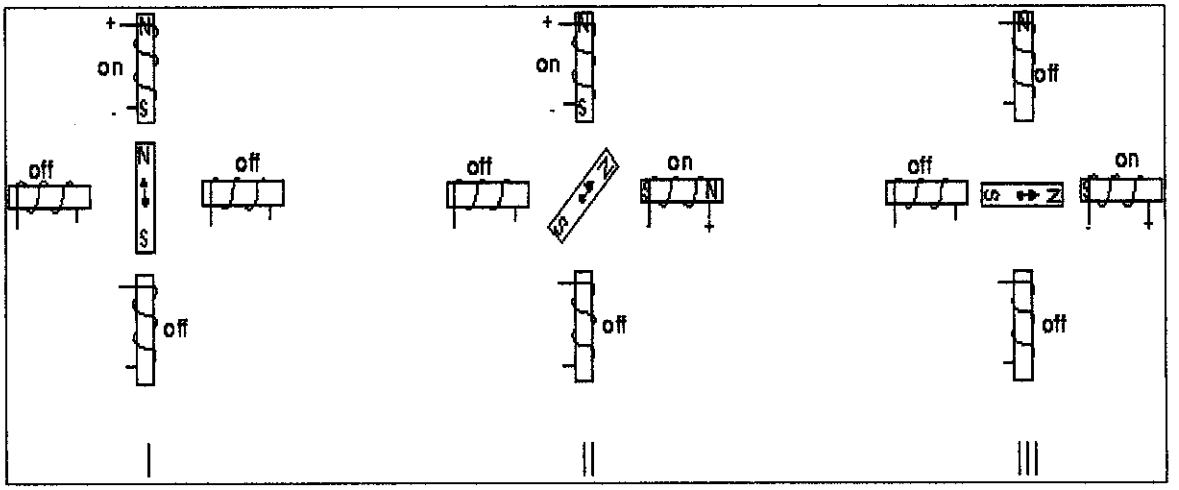


Figure 8 Half stepping process of a stepper motor (Images Si Inc., 2006)

2.8 PIC 16F84

PIC16F84 perfectly fits many uses, from automotive industries and controlling home appliances to industrial instruments, remote sensors, electrical door locks and safety devices. It is also ideal for smart cards as well as for battery supplied devices because of its low consumption (Matic, 2005).

In Figure 7 it shows a simplified block diagram of the interior of the microcontroller. Basically in PIC 16F84 it works a lot with this four main blocks. The first block is the program memory. It contains the programs that have been written. The program is a set of instruction that the microcontroller will perform as desired. The software (instructions) will be written in a computer and then programed (burned) into the

"program memory". This memory is an EEPROM memory which can be rewritten thousand times (Passagen, 2006).

The next block is the REGISTER and RAM box. It contains all the internal registers and a small RAM memory where data can be stored temporary. The RAM memory is not large about 64-128 byte. For example, a program loop is made, and then a variable is needed to change value each time the loop runs and then use that variable to define the RAM address for it to hold the counter value. The content in the Register and RAM-info will disappear when the power is off (Passagen, 2006).
There is another memory which will work the same as the RAM and that is the EEPROM-memory. This is a small memory where it can read and write data, but the data will not disappear when the power is off. Next time when the power is on, user can go into this memory and fetch the data again. For example, if there is a code lock alarm, a right code is needed to deactivate the alarm. The right code is stored in the EEPROM and just compares the actual pressed keys with the value in the EEPROM. The alarm code can be changed by rewriting the key in the EEPROM (Passagen, 2006).

The last box is the port of this circuit. The port is the input and output pins of the actual circuit. The pins can be defined as either inputs or outputs. By writing or reading to the port, each pin can be controlled as desired (Passagen, 2006).

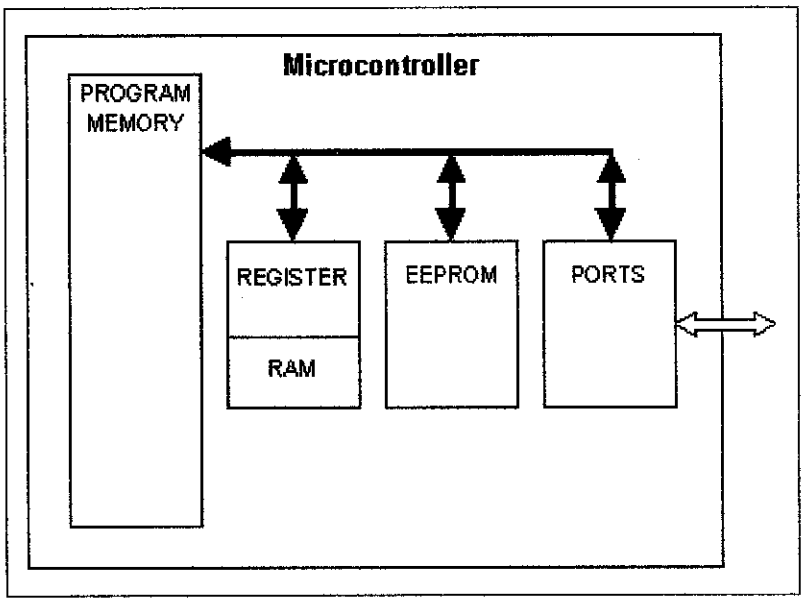


Figure 9 Block diagram of the microcontroller (Passagen, 2006)

CHAPTER 3
METHODOLOGY AND PROJECT WORK

3.1 Procedure Identification

This project will go through the steps as shown in Figure 4 given on next page. Basically this project will start with research and studies conducted based on journals, books and articles obtain from both resource center and internet. Later on, a suitable tracking mechanism is chosen and the basic concept of the system is designed. From the design of the system, each part of the system needs further research and studies. After that, all the circuit design and programming language is going to be developed. Lastly, when all analysis of the system has been completed, the prototype fabrication will be started.

3.1.1 Literature Review/ Theory

In this initial stage of the project, it involved extensive literature research on the topic of the project and its entire related subject. These involve performing research on the subject by various means such as books, journals, magazines and websites. A good understanding on the subject matter to the topic is really crucial so that the project can run smoothly.

3.1.2 Research and Analyses on the Theoretical Component

For this second stage, after understanding all the theory, analysis needs to be done. The analysis is done by conducting a few hands on works such as experimental activities. The experimental activities are necessary in order to develop understanding on the subject matter that related to the topic. Besides that, analysis has also been done to verify the theory that has been studied earlier.

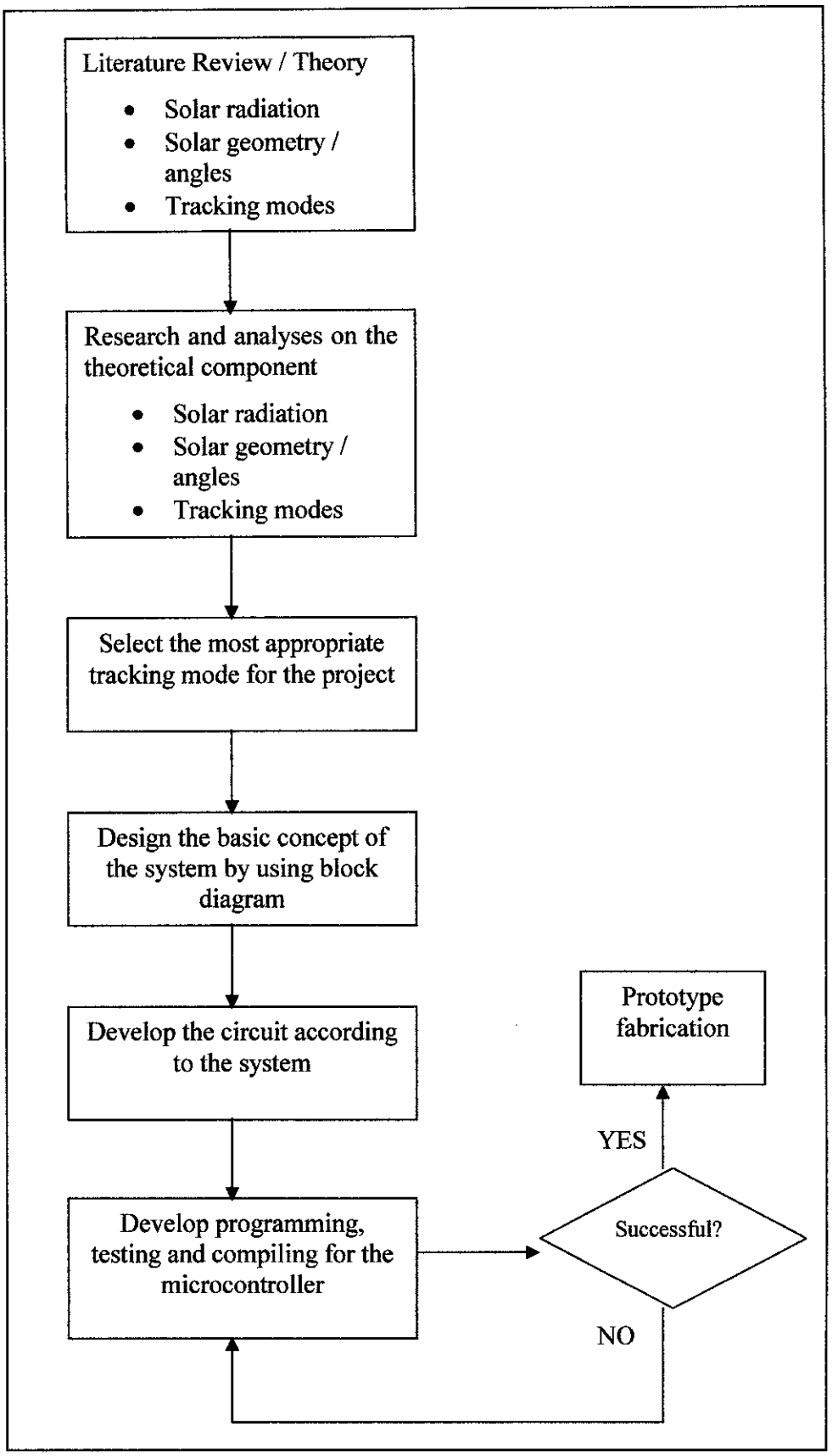


Figure 10 Flow chart for procedure identification

3.1.3 Selection of Tracking Mode

There are steps to select the most appropriate tracking mode. The flow of the process is as follows.

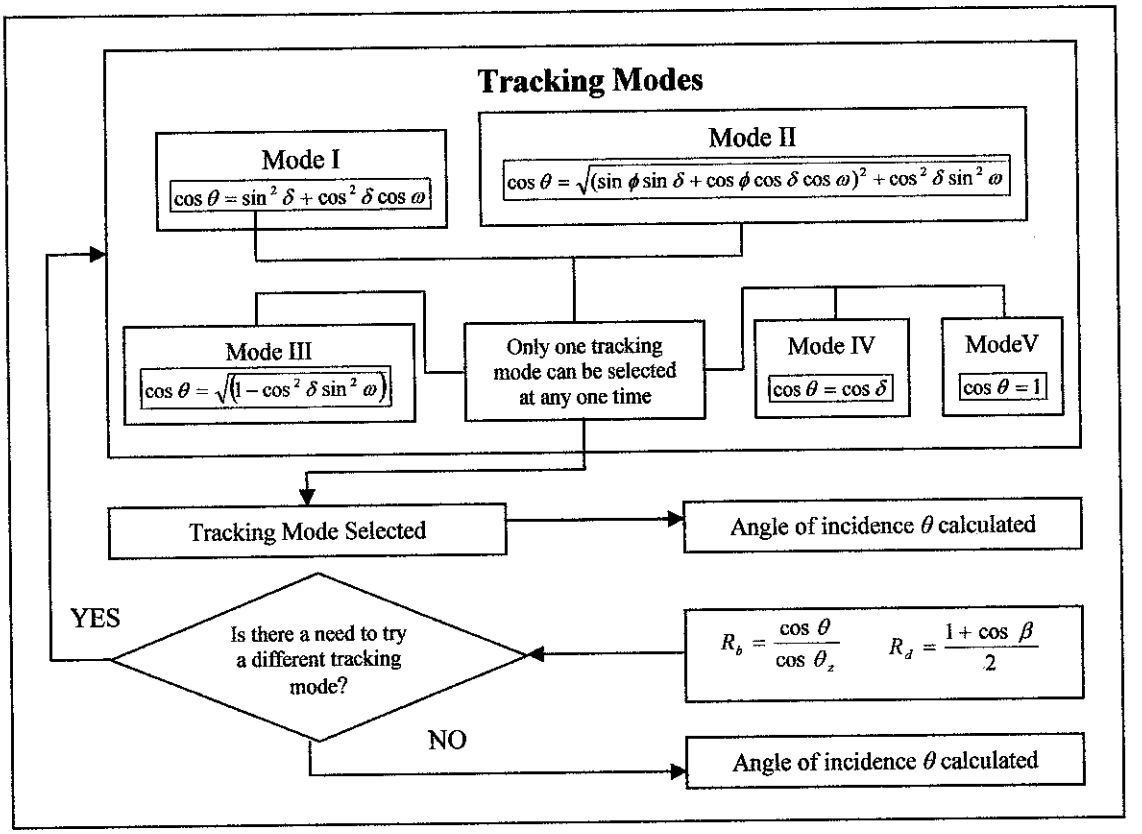


Figure 11 The tracking mode module flowchart for optimization

For the tracking mode module flowchart, it must be utilized together with the meteorological data processing module. Below are the steps on how to compare and evaluate each mechanism using the meteorological data.

Comparison of Tracking Mechanisms

An analysis has been done to calculate the beam radiation that would fall on one square meter of the aperture plane. It is done for each mechanism. For this analysis, data from the solar radiation for Ipoh is made use. The solar radiation data is obtained from the local meteorological department. It shows the global or total solar radiation in Ipoh area. In order to proceed with the analysis, separation methods for global radiation need to be done. By using Equation (2.19) to Equation (2.25) the calculation for the separation of the global radiation is done. Sample of the calculations are as follows.

On 2nd of August, n = 214. From Equation (2.6),

$$\delta = 23.5\sin\left(360\frac{284+n}{365}\right)$$

$$\delta = 17.65°$$

From Equation (2.21), the sunrise hour angle

$$\omega_s = \cos^{-1}(-\tan\phi\tan\delta)$$

$$\omega_s = \cos^{-1}(-\tan 4.57°\tan 17.65°)$$

$$\omega_s = 91.45° = 1.596 \quad rads$$

By using I_{sc} = 1353 W/m^2,

$$I_{ext} = I_{sc}\left(1+0.033\cos\frac{360n}{365}\right)$$

$$I_{ext} = 1391.2 \quad W/m^2$$

From Equation (2.19),

$$H_O = 27490.9 I_{ET}\left[\cos\phi\cos\delta\sin\omega_s + \left(\frac{11}{630}\omega_s\sin\phi\sin\delta\right)\right]$$

$$H_O = 366674 \quad kJ/m^2$$

Therefore, from Equation (2.22),

$$\overline{K}_T = \frac{\overline{H}}{\overline{H}_O}$$

$$\overline{K}_T = \frac{1.38M}{36674k}$$

$$\overline{K}_T = 0.038$$

From Equation (2.23),

$$\overline{H}_d = (1.000 - 1.130\overline{K}_T)\overline{H}$$

$$\overline{H}_d = [1.000 - 1.130(0.038)]1.38M$$

$$\overline{H}_d = 1.32 \quad MJ/m^2 - day$$

For time 0700 hours, from Equation (2.24),

$$\bar{I}_d = \frac{11\bar{H}_d}{84}\left(\frac{\cos\omega - \cos\omega_s}{\sin\omega_s - \frac{11}{630}\omega_s\cos\omega_s}\right)$$

$$\bar{I}_d = 27.3 \quad kJ/m^2 - h$$

Therefore, the beam radiation can be obtained by using Equation (2.25),

$$\bar{I}_b = \bar{I}_G - \bar{I}_d$$

$$\bar{I}_b = 0.19M - 27.3k$$

$$\bar{I}_b = 162.7 \quad kJ/m^2 - h$$

$$\bar{I}_b = 45.2 \quad W/m^2$$

The same calculation is done for other hours as well. So, the hourly beam radiation for the 2nd August is as in Table 1.

Table 1 Values of beam radiation after separation method

Time (h)	I_b (W / m^2)	Time (h)	I_b (W / m^2)
0600	0.00	1300	552.8
0700	45.2	1400	580.6
0800	163.9	1500	594.4
0900	419.4	1600	561.1
1000	522.2	1700	199.7
1100	550.0	1800	11.1
1200	766.7	1900	0.00

After getting the beam radiation values, the comparison of the tracking mechanism is done. By using Ipoh as the base station (4^0 34' N, 101^0 06' E) and Kuala Lumpur as reference station (3^0 08' N, 101^0 41' E), the calculations are as follows.

On 2nd August 2005, at 1000 h and $\beta = 0^0$,

$$\cos\theta_z = \sin\phi\sin\delta + \cos\phi\cos\delta\cos\omega$$

$$\cos\theta_z = \sin 4.57°\sin 17.65° + \cos 4.57°\cos 17.65°\cos(37.35)$$

$$\cos\theta_z = 0.7792$$

For tracking mode I, from Equation (2.10),

$$\cos\theta = \sin^2\delta + \cos^2\delta\cos\omega$$

$$\cos\theta = \sin^2 17.65 + \cos^2 17.65\cos 37.35$$

$$\cos\theta = 0.0919 + 0.9081(0.7949)$$

$$\cos\theta = 0.8137$$

Therefore, tilt factor r_b for the plane, from Equation (2.26)

$$r_b = \frac{\cos\theta}{\cos\theta_z} = \frac{0.8137}{0.7792} = 1.0443$$

Beam flux incident normally on plane $= I_b r_b$

$$= 522.2 \times 1.0443$$

$$= 545.33 \quad W/m^2$$

Similar calculation is continued for the other tracking modes. The following results are obtained for all the modes.

Table 2 Comparison of tracking modes

LAT (h)	$I_b r_b$ (W / m^2)				
	Mode I	Mode II	Mode III	Mode IV	Mode V
0600	0.00	0.00	0.00	0.00	0.00
0700	42.37	115.16	335.18	627.49	350.46
0800	210.78	227.20	459.19	686.18	477.33
0900	481.41	488.66	719.73	709.47	744.53
1000	585.97	587.59	698.75	686.18	720.13
1100	613.58	613.76	640.51	627.49	658.52
1200	838.97	838.88	823.12	805.40	845.25
1300	619.18	619.24	607.96	594.88	624.30
1400	648.06	648.25	677.88	664.07	696.90
1500	661.58	685.71	772.35	777.41	815.86
1600	633.44	519.72	1025.25	939.04	986.14
1700	248.99	269.03	547.70	542.57	569.45
1800	27.75	43.60	127.58	127.14	133.42
1900	0.00	0.00	0.00	0.00	0.00
Total	5612.00	5656.80	7435.20	7262.46	7622.30

From Table 2, it shows that the maximum total is obtained with mode V. This is as expected since mode V involves two – axis tracking and gives normal incidence. The other modes involve continuous one – axis tracking or one daily adjusted and give lesser totals. The results obtained are obviously dependent on the latitude of the location, the day of the year and the input radiation data. In reality, modes II, III and IV are the most preferred and not V. This is due to its complexity of providing motion about two axes, though it gives the maximum total of beam radiation. As for this project, mode II has been selected because of its simplicity and also practicability.

3.1.4 Basic Concept of the System

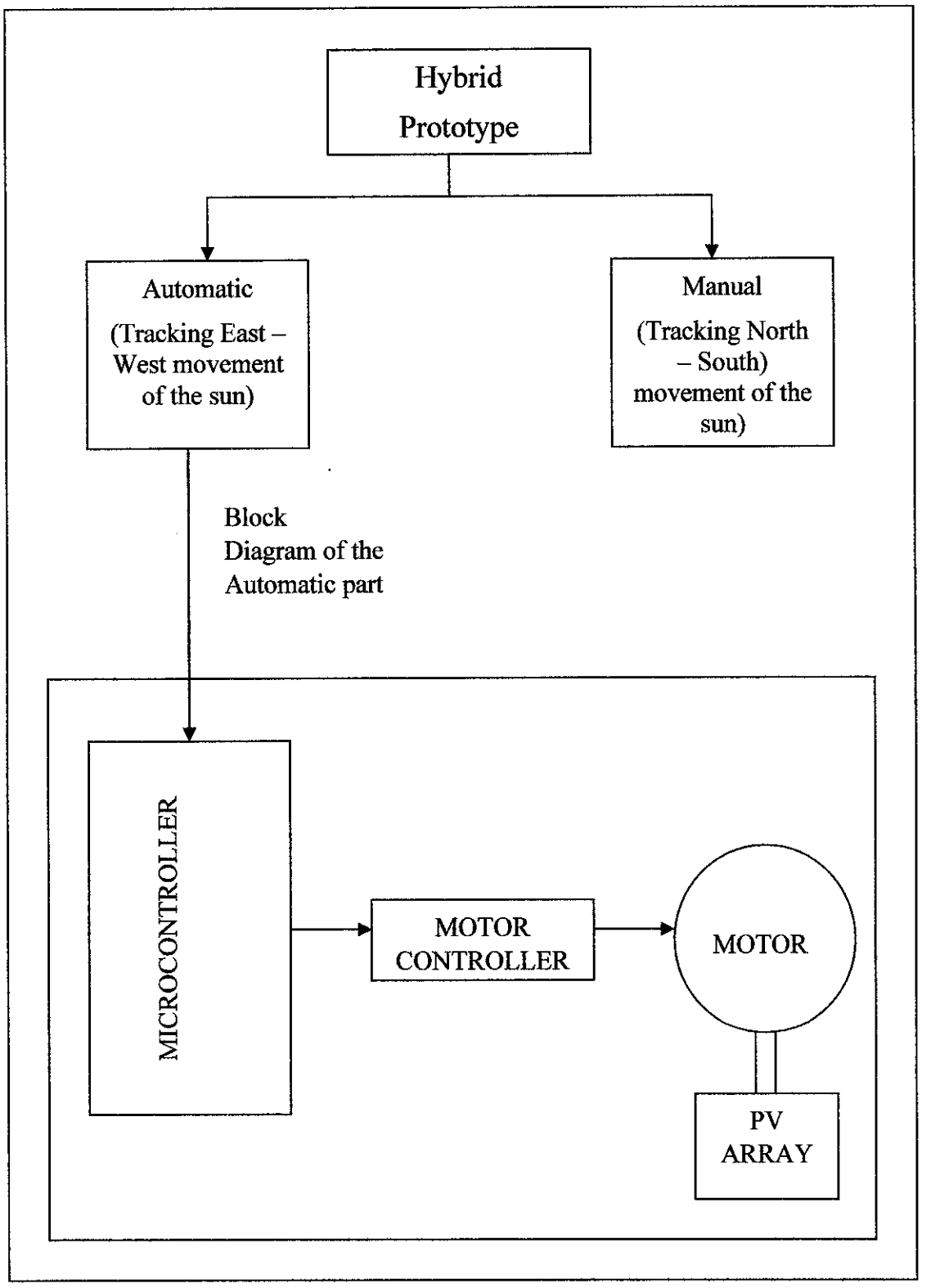


Figure 12 The design concept of the tracker

So for the design of the tracker, the author proposed to have a hybrid type of tracker. In this hybrid design, it will have two – axis tracking mode. One axis will be controlled automatically and the other axis is controlled manually. By having this type of tracker, the maximum power point tracking can be optimized and also the cost saving can be done here. Besides that, the tracker can have two – axis tracking mode without having the complexity in controlling both axis automatically. In this design, the automatic part will control East – West motion of the motor while the manual part, for North – South.

For the automatic part, the heart of the system is the microcontroller. There will be a motor controller in between the microcontroller and motor. The microcontroller will give a signal to the motor controller. Then, the motor controller will give instruction to motor to rotate how many degrees corresponding to the position of the sun at that hour. The PV array will be attached to the motor gear system.

3.1.5 Development of the Circuit of the System and the Programming

At this stage, the programming of the microcontroller is developed. The program will help to control the motion of the motor according to the movement of the sun. There is a driver circuit for the stepper motor. This circuit is functioning as an interface of the motor with microcontroller. So, the driver circuit will drive the motor when a signal is received from the microcontroller.

Stepper Motor Driver Board

A simple circuit is designed for the driver board. Though it is simple it is able to drive the stepper motor well. Figure 13 shows the schematic of the circuit. From this figure, it shows that the PIC's output lines are first buffered by a 4050 hex. This hex inverter buffer is needed in order to maintain 5V supply along the line. Without this buffer, the circuit may have a larger voltage drop and cause less current to energize the coil of the stepper motor. Then, the hex inverter buffer is connected to an NPN transistor. The transistor that is being used is TIP 120, which is actually a NPN Darlington. The TIP120's acts like switches, activating one stepper motor coil at a time. Due to a inductive surge created when a coil is toggled, a standard 1N4001 diode is usually placed across the transistor, providing a safe way of dispersing reverse current

without damaging the transistor. Sometimes this diode is known as a snubbing diode. The TIP 120 transistors do not need an external snubbing diode since they have a built in diode which is not shown in the schematic.

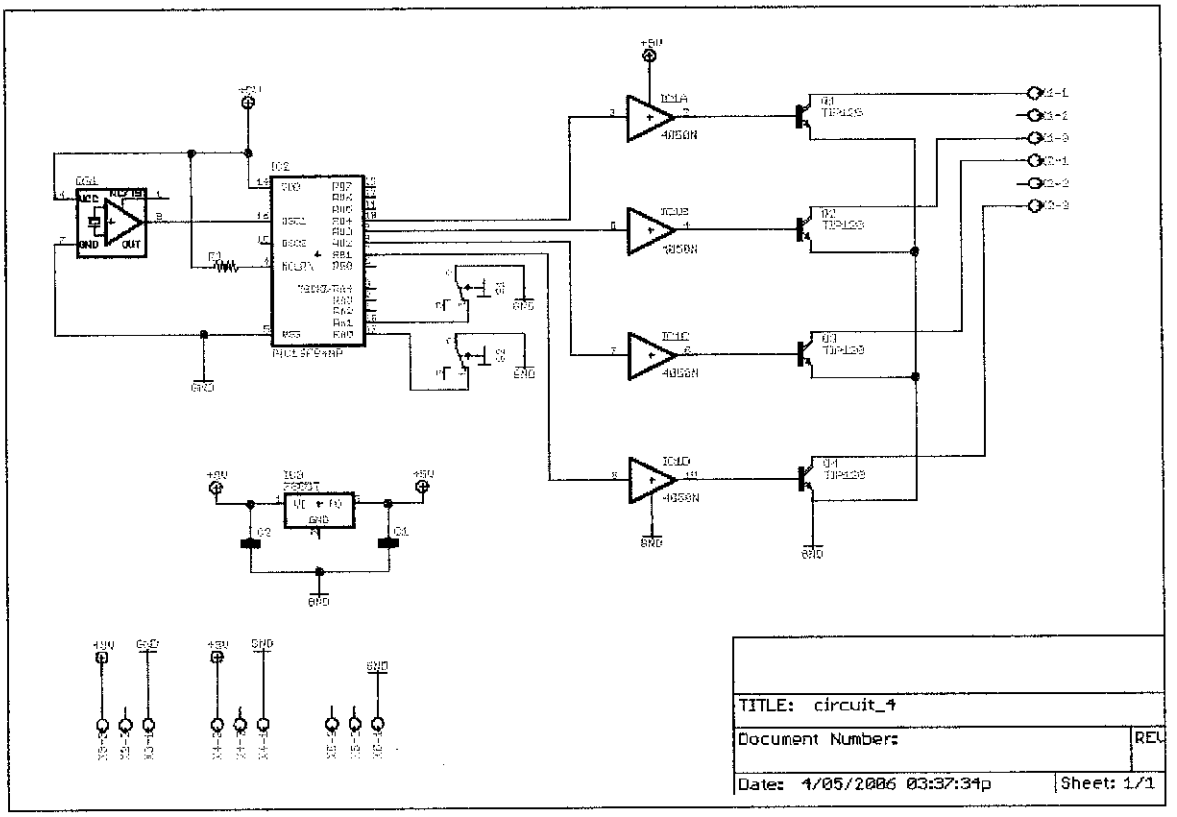


Figure 13 Schematic of the stepper motor driver board

Development of the program

Before developing the program, it is essential to understand the movement of the motor. The motor has 4 coils that are used to cause the revolution of the drive shaft. Each coil must be energized in the correct order for the motor to spin. To make sure the correct coil is energized, it is essential to figure out the step sequence of the motor. The correct step sequence is crucial so that the motor can rotate accurately. Each of the sequence turns on only two transistors at a time. For stepper motor with 7.5 degree/ step, the step sequence (full step) is as below.

Table 3 Step sequence (full step) of the stepper motor

Coils / Step no.	A	B	C	D
1	ON	OFF	ON	OFF
2	OFF	ON	ON	OFF
3	OFF	ON	OFF	ON
4	ON	OFF	OFF	ON

Later on, the program of the controller is developed. The C language is used for the programming. This language is simple to develop compared to assembly language, which needs a lot of initialization. The program for controlling the motor is attached in Appendix B.

In this program, the motor is programmed according to the movement of the sun's path during day light. From the research that has been done before, it is found out that the sun is moving about 15 degree every hour. Therefore, to make the motor to have an approximate movement as the sun, it is programmed to rotate about 0.3 degree each minute. The rotation of the stepper motor is vital since it will determine how accurate is the tracker to track the sun's position that later can lead to a better efficiency for the PV. Besides that, the motor is programmed to have a bi – directional movement, so that the motor can rotate either in forward or backward manner. Hence the motor can reverse to its original position the next day to operate all over again.

3.1.6 Fabrication and Verification of Prototype

This is the last stage of the project. Before fabrication is done, the functioning of the program and the circuit is necessary. If both criteria are not met, then it will agitate the fabrication of the prototype. When the fabrication is done, the prototype performance is verified by doing experiment under actual local meteorological conditions. Figure 14 shows the overall of the hybrid solar tracker prototype.

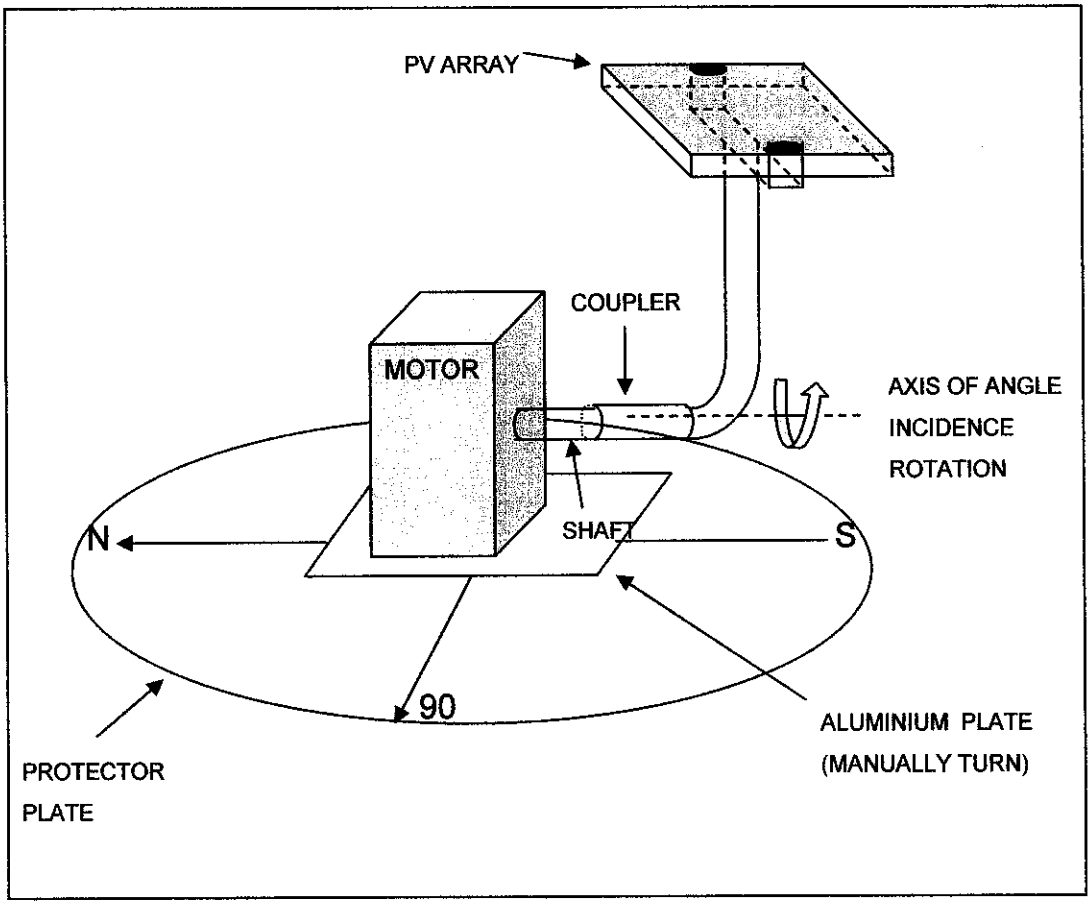


Figure 14 Hybrid solar tracker

CHAPTER 4
RESULTS AND DISCUSSION

In this chapter, results and findings of this project is going to be discussed. The results are obtained from the experimental analysis that has been done to observe the performance and efficiency of the PV under actual meteorological condition. Besides that, the experiment is also meant for verification and evaluation for the prototype.

4.1 Experimental Analysis

An experiment has been conducted by using the PV array. This experiment is meant to observe the variation of voltage that is going to be provided by the PV over a period of time. For this experiment the performance and efficiency of the PV is compared in two conditions. One is using the solar tracking system that has been fabricated in this project and the other condition is in stand – still mode.

4.1.1 Stand – still Mode

This experiment is conducted by fixed the position of the PV array and let it stay under the sun over a period of time. It was conducted from 1300 hours to 1500 hours. The results are as follows.

Table 4 Output voltage of the PV array over a period of time

Time (hours)	Voltage (V)	Time (hours)	Voltage (V)
1300	9.051	1408	8.243
1316	9.024	1406	8.168
1324	8.945	1424	8.137
1320	8.945	1432	8.098
1340	8.915	1440	8.011
1348	8.937	1448	8.197
1356	8.929	1456	7.998

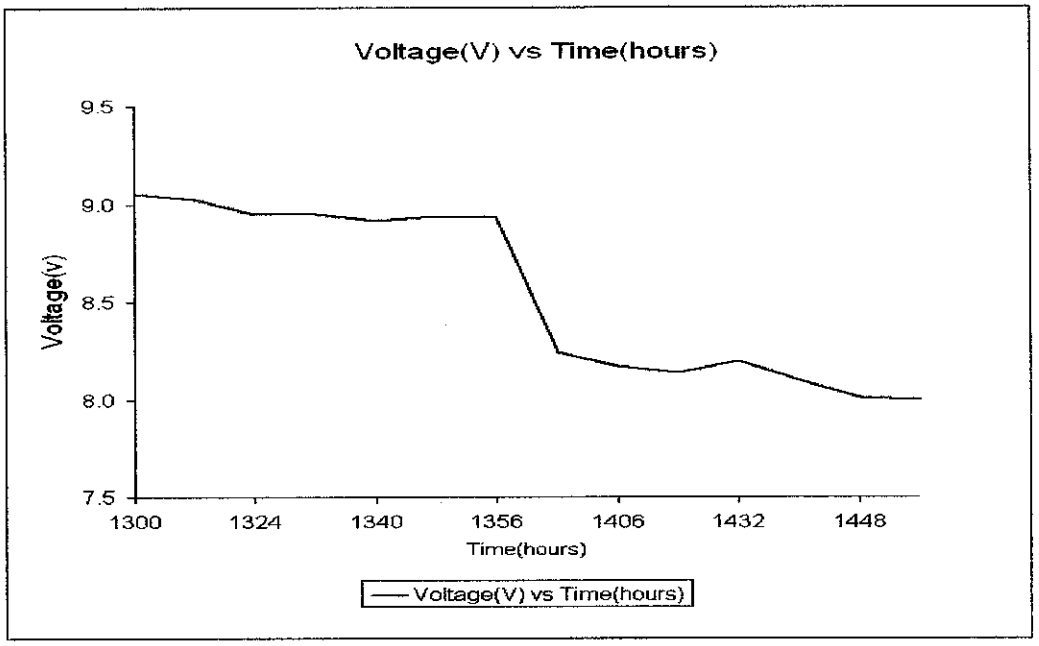


Figure 15 Voltage variation over time with stand – still mode

From the results of the experiment, what can be observed is that as the time goes by, the output voltage of the PV array becomes less. This is because the PV array is fixed at one angle, and as the time goes by, the sun has moved to a different angle. So there isn't any direct beam from the sun to the array anymore. So it is understood that to get a maximum voltage, direct beam between the sun and the PV array is necessary.

4.1.2 Solar tracking system

This experiment has been conducted simultaneously with the stand – still mode experiment. The results of the experiment are as follows.

Table 5 Output voltage of the PV array over a period of time

Time (hours)	Voltage (V)	Time (hours)	Voltage (V)
1300	9.051	1408	9.045
1316	9.024	1406	9.039
1324	8.989	1424	8.998
1320	9.011	1432	9.007
1340	9.051	1440	9.018
1348	9.027	1448	9.001
1356	8.929	1456	8.979

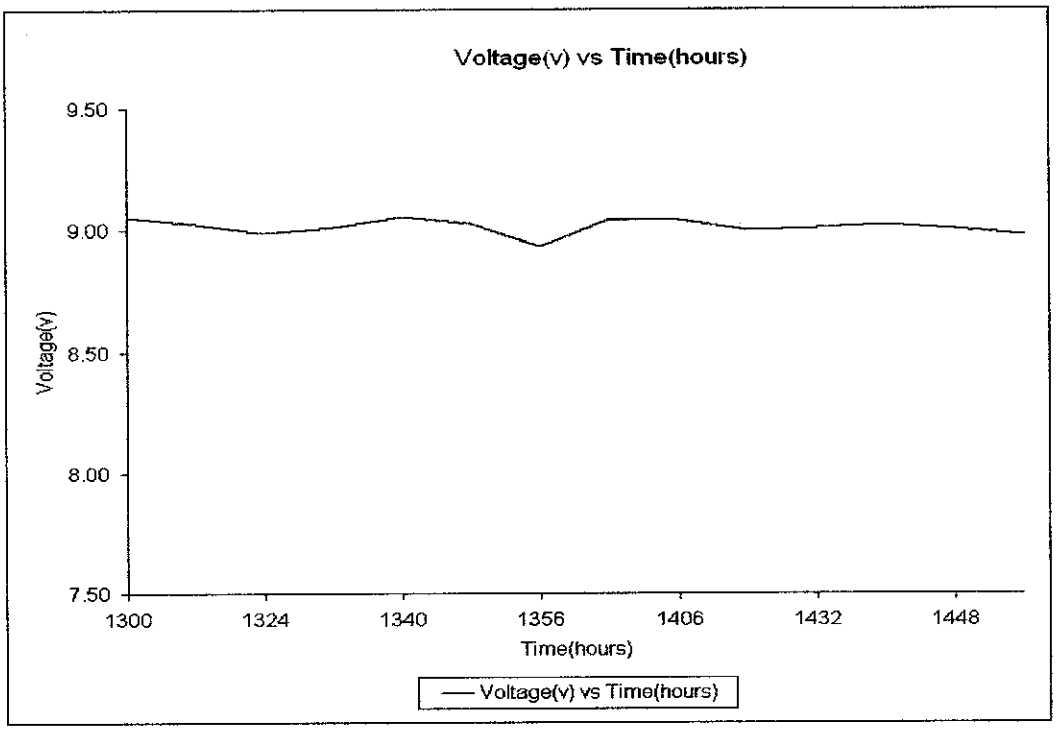


Figure 16 Voltage variation over time with solar tracking system

From the table and also the graph, it shows that the position of the PV array do effect the voltage reading. It is cleared that when the position of the sun's beam and PV array are always perpendicular (direct sun's beam on the PV array), the array gives a constant value of voltage output which is around 9.000 V. This is due to the value of angle of incidence, θ with the normal of the plane. When both the sun's beam and the PV array are in perpendicular the angle of incidence is equal to zero and value of cos $\theta = 1$. So from this experiment, it is known that direct beam radiation on the PV array give a constant maximum voltage.

Therefore, what can be concluded from both experiments is that the output voltage of the array really depends on the angle of incidence of the sun with the normal of the plane. When the angle of incidence is getting larger, it indicates that the position of the PV and the sun's beam is not perpendicular anymore and can cause deficiency on the performance of the PV. Hence, it is verified that the efficiency and the performance of the PV is better when it is integrated with a solar tracking system.

CHAPTER 5
CONCLUSION AND RECOMMENDATION

This project is a very interesting project. It gives a lot of experiences and knowledge in problem solving and troubleshooting skills. In addition, this project also gives a real practice on how to conduct an engineering project. Other than that, this project has lots of values since it can improve the utilization of renewable energy, which is now being one of the hottest issues in Malaysia. Therefore, this project is beneficial to the country in developing renewable energy technology.

From this project, it is known that there are several mechanisms can be used for designing a PV tracking system. After doing the analysis and research, 1 – axis tracking system has been chose. In 1 – axis tracker, it will move according to East – West axes. It is chosen because of its simplicity and practicability for this project. However, research has show that 2 – axis tracking system will give better performance in tracking the sun. Due to its complexity and also cost saving purposes, it is not going to be implemented for this project. To make the design of the tracker more efficient, a hybrid tracking system is introduced. It will consist of two controlling method. First is the automatic control for East – West motion, and second is the manual control for North – South motion. For the automatic part, the system is mainly controlled by using the microcontroller (PIC 16F84). All the control functions are loaded into this PIC and the system is running according to the program. As for the manual part, the solar tracker is manually controlled by adjusting the position of the PV monthly. Instead of tracking in 1 – axis only, now the tracker can function such as a 2 – axis tracking system. By implementing this system, cost of the tracker can be reduced and also the complexity is less compared to automatic two – axis controller.

For project enhancement, a few changes to the system can be made. One of it is the integration of the system with the computer interface. This can be done via serial port

or parallel port of the computer. The computer can be used to monitor the angle of the motor in order to make sure the position of the sun's ray and the PV array is always in perpendicular. Besides that, the computer also monitors the output voltage of the PV and even does some adjustment to the solar tracker angle.

Improvement to the project also can be done by placing a feedback path to the system. Feedback system can improve the control performance of the tracker. This system makes use of an output of a system in deciding the way to influence an input to the system. A sensor can be introduced to the tracker system and later, output of the sensor is then feedback to system and used to control the movement of the tracker.

Other than the above suggestions, the project can be augmented by implementing the two – axis system. This requires more number of motors and also other components. In addition to that, the system also getting more complex to develop, but the efficiency of the PV will be greatly improved.

REFERENCES

Alata, M. (2004). Developing a Multipurpose Sun Tracking System Using Fuzzy Control. 4. P. 1229 – 1245.

Garg, H.P & Prakash, J.(1997). Solar Energy: Fundamentals and Applications. NewDelhi: Mc Grawhill.

Goswami, D.Y, Kreith, F. & Kreider, J.F.(2000). Principles of Solar Engineering, 2nd Edn. USA: Taylor & Francis.

Images Si Inc. (2006). How Stepper Motors Work. 15th February 2006 from http://www.imagesco.com

Klein, S.A. (1977). Calculation of Monthly Average Insolation on Tilted Surfaces. Solar Energy. 19. 325.

KTKM. (2005). Renewable Energy. 21st October 2005 from http://www.ktkm.gov.my.

Liu, B.Y.H & Jordan, R.C. (1960). The Interrelatiohship & Characteristic Distribution of Direct, Diffuse & Total Solar Radiation. Solar Energy. 4 (3). P. 1-19.

Magal, B.S. (1990). Solar Power Engineering. New Delhi: Tata Mc Graw – Hill Publishing Company Limited.

NST. (2005). Renewed Interest in Renewable Energy. Port Dickson. 23rd August 2005.

Page, J.K. (1961). The Estimation of Monthly Mean Values of Daily Short – Wave Radiation on Vertical & Inclined Surfaces from Sunshine Records for Latitudes 40N – 40 S. Proc of UN Conference on New Sources of Energy. 4. P. 378 – 390.

Rabl, A. (1985). Active Solar Collectors and Their Application. New York. Oxford University Press.

Reslab. (2006). Solar Cell Principles and Application. 15th February 2006 from http://www.reslab.com.au

Serway, R.A. & Beichner, R.J. (2000). Physics for Scientists & Engineers with Modern Physics. 5th Edn. USA: Sanders College Publishing: A Division of Hartcourt College Publishers.

Smith, C. (1995). History of Solar Energy: Revisiting Solar Power's Past. The Solar Energy Newsletter July. http://www.solarenergy .com/info_history.html

Sukhatme, S.P. (1999). Solar Energy: Principles of Thermal Collection and Storage. New Delhi: Tata Mc Grawhill.

The Malay Mail. (2005). TNB May Get Nod to Up Power Prices by 10 pc. Kuala Lumpur. 5th August 2005.

APPENDICES

APPENDIX A

GANTT CHART

Gantt Chart for Final Year Project (first semester)

No	DETAIL/ WEEK NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	Selection of Project Topic														
2	Preliminary Research Work														
	-Project planning														
	-Introduction to Solar Energy														
	-Introduction to Various Sun Tracking Method														
	-Literature Reviews														
3	Submission of Preliminary Report														
4	Project Work														
	-Identify which tracking method will be used														
	-Do Experiment for the Detection of the Solar using PV														
	-Do Comparison for Tracking Modes														
5	Submission of Progress Report														
6	Project Work Continue														
	-Basic Design Concept of Tracking System														
7	Submission of Interim Report Final Draft														
8	Submission of Interim Report														
9	Oral Presentation														

Gantt Chart for Final Year Project (second semester)

No.	Detail/Week	1	2	3	4	5	6	7	8	9	10	11	12	13	14	SW	EW	19	20
1	Project work continue																		
	- Research on stepper motor controller																		
2	Laboratory Work																		
	- Microcontroller Program Development																		
	- Circuit Development and Troubleshooting																		
	- Fabricate the prototype																		
	- Troubleshooting and prototype adjustment																		
	- Meteorological Experiment																		
3	Submission of Progress Report 1																		
4	Submission of Progress Report 2																		
5	Planning Documentation																		
6	Submission of Draft Report																		
7	Submission of Final Report (Soft Cover)																		
8	Oral Presentation																		
9	Submission of Technical Report	Due on 12th June 2006																	
10	Submission of Final Report (Hard Cover)	Due on 23rd June 2006																	

APPENDIX B

SOURCE CODE SAMPLE

```
#include <16f84.h>
#USE DELAY(CLOCK=4000000)
#FUSES XT, NOWDT, NOPROTECT, NOPUT
char a, b, n, m;
void main()
{
 set_tris_b(0x00);
 a = input (PIN_A0);
 b = input (PIN_A1);
while(1)
        {
                if ( a == 1)      //forward path
                {
                        for(n=1;n<=600;n++)
                                {
                                        output_high (PIN_B1);       // step 1
                                        output_low (PIN_B2);
                                        output_high (PIN_B3);
                                        output_low (PIN_B4);
                                        delay_ms (60000);

                                        output_low (PIN_B1);       // step 2
                                        output_high (PIN_B2);
                                        output_high (PIN_B3);
                                        output_low (PIN_B4);
                                        delay_ms (60000);

                                        output_low (PIN_B1);       // step 3
                                        output_high (PIN_B2);
                                        output_low (PIN_B3);
                                        output_high (PIN_B4);
                                        delay_ms (60000);

                                        output_high (PIN_B1);       // step 4
                                        output_low (PIN_B2);
                                        output_low (PIN_B3);
                                        output_high (PIN_B4);
                                        delay_ms (60000);
                                }
                }
                else if ( b == 1)         //backward path
                {
                        for(m=1;m<=600;m++)
                                {
```

```
                output_high (PIN_B1);      // step 4
                output_low (PIN_B2);
                output_low (PIN_B3);
                output_high (PIN_B4);
                delay_ms (60000);

                output_low (PIN_B1);       // step 3
                output_high (PIN_B2);
                output_low (PIN_B3);
                output_high (PIN_B4);
                delay_ms (60000);

                output_low (PIN_B1);       // step 2
                output_high (PIN_B2);
                output_high (PIN_B3);
                output_low (PIN_B4);
                delay_ms (60000);

                output_high (PIN_B1);      // step 1
                output_low (PIN_B2);
                output_high (PIN_B3);
                output_low (PIN_B4);
                delay_ms (60000);
            }
        }
    }
}
```

APPENDIX C

SPECIFICATION SHEET FOR PIC16F84

MICROCHIP

PIC16F8X

18-pin Flash/EEPROM 8-Bit Microcontrollers

Devices Included in this Data Sheet:

- PIC16F83
- PIC16F84
- PIC16CR83
- PIC16CR84
- Extended voltage range devices available (PIC16**L**F8X, PIC16**L**CR8X)

High Performance RISC CPU Features:

- Only 35 single word instructions to learn
- All instructions single cycle except for program branches which are two-cycle
- Operating speed: DC - 10 MHz clock input
  DC - 400 ns instruction cycle

Device	Program Memory (words)	Data RAM (bytes)	Data EEPROM (bytes)	Max. Freq (MHz)
PIC16F83	512 Flash	36	64	10
PIC16F84	1 K Flash	68	64	10
PIC16CR83	512 ROM	36	64	10
PIC16CR84	1 K ROM	68	64	10

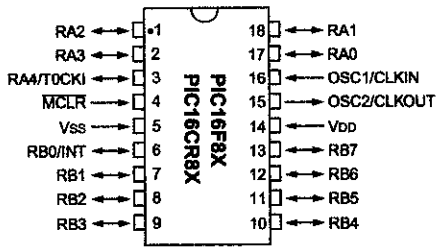
- 14-bit wide instructions
- 8-bit wide data path
- 15 special function hardware registers
- Eight-level deep hardware stack
- Direct, indirect and relative addressing modes
- Four interrupt sources:
  - External RB0/INT pin
  - TMR0 timer overflow
  - PORTB<7:4> interrupt on change
  - Data EEPROM write complete
- 1000 erase/write cycles Flash program memory
- 10,000,000 erase/write cycles EEPROM data memory
- EEPROM Data Retention > 40 years

Peripheral Features:

- 13 I/O pins with individual direction control
- High current sink/source for direct LED drive
  - 25 mA sink max. per pin
  - 20 mA source max. per pin
- TMR0: 8-bit timer/counter with 8-bit programmable prescaler

Pin Diagrams

PDIP, SOIC



Special Microcontroller Features:

- In-Circuit Serial Programming (ICSP™) - via two pins (ROM devices support only Data EEPROM programming)
- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Code-protection
- Power saving SLEEP mode
- Selectable oscillator options

CMOS Flash/EEPROM Technology:

- Low-power, high-speed technology
- Fully static design
- Wide operating voltage range:
  - Commercial: 2.0V to 6.0V
  - Industrial: 2.0V to 6.0V
- Low power consumption:
  - < 2 mA typical @ 5V, 4 MHz
  - 15 µA typical @ 2V, 32 kHz
  - < 1 µA typical standby current @ 2V

1.0 GENERAL DESCRIPTION

The PIC16F8X is a group in the PIC16CXX family of low-cost, high-performance, CMOS, fully-static, 8-bit microcontrollers. This group contains the following devices:

- PIC16F83
- PIC16F84
- PIC16CR83
- PIC16CR84

All PICmicro™ microcontrollers employ an advanced RISC architecture. PIC16F8X devices have enhanced core features, eight-level deep stack, and multiple internal and external interrupt sources. The separate instruction and data buses of the Harvard architecture allow a 14-bit wide instruction word with a separate 8-bit wide data bus. The two stage instruction pipeline allows all instructions to execute in a single cycle, except for program branches (which require two cycles). A total of 35 instructions (reduced instruction set) are available. Additionally, a large register set is used to achieve a very high performance level.

PIC16F8X microcontrollers typically achieve a 2:1 code compression and up to a 4:1 speed improvement (at 20 MHz) over other 8-bit microcontrollers in their class.

The PIC16F8X has up to 68 bytes of RAM, 64 bytes of Data EEPROM memory, and 13 I/O pins. A timer/counter is also available.

The PIC16CXX family has special features to reduce external components, thus reducing cost, enhancing system reliability and reducing power consumption. There are four oscillator options, of which the single pin RC oscillator provides a low-cost solution, the LP oscillator minimizes power consumption, XT is a standard crystal, and the HS is for High Speed crystals. The SLEEP (power-down) mode offers power saving. The user can wake the chip from sleep through several external and internal interrupts and resets.

A highly reliable Watchdog Timer with its own on-chip RC oscillator provides protection against software lock-up.

The devices with Flash program memory allow the same device package to be used for prototyping and production. In-circuit reprogrammability allows the code to be updated without the device being removed from the end application. This is useful in the development of many applications where the device may not be easily accessible, but the prototypes may require code updates. This is also useful for remote applications where the code may need to be updated (such as rate information).

Table 1-1 lists the features of the PIC16F8X. A simplified block diagram of the PIC16F8X is shown in Figure 3-1.

The PIC16F8X fits perfectly in applications ranging from high speed automotive and appliance motor control to low-power remote sensors, electronic locks, security devices and smart cards. The Flash/EEPROM technology makes customization of application programs (transmitter codes, motor speeds, receiver frequencies, security codes, etc.) extremely fast and convenient. The small footprint packages make this microcontroller series perfect for all applications with space limitations. Low-cost, low-power, high performance, ease-of-use and I/O flexibility make the PIC16F8X very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions; serial communication; capture, compare and PWM functions; and co-processor applications).

The serial in-system programming feature (via two pins) offers flexibility of customizing the product after complete assembly and testing. This feature can be used to serialize a product, store calibration data, or program the device with the current firmware before shipping.

1.1 Family and Upward Compatibility

Those users familiar with the PIC16C5X family of microcontrollers will realize that this is an enhanced version of the PIC16C5X architecture. Please refer to Appendix A for a detailed list of enhancements. Code written for PIC16C5X devices can be easily ported to PIC16F8X devices (Appendix B).

1.2 Development Support

The PIC16CXX family is supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a low-cost development programmer and a full-featured programmer. A "C" compiler and fuzzy logic support tools are also available.

TABLE 1-1 PIC16F8X FAMILY OF DEVICES

		PIC16F83	PIC16CR83	PIC16F84	PIC16CR84
Clock	Maximum Frequency of Operation (MHz)	10	10	10	10
Memory	Flash Program Memory	512	—	1K	—
	EEPROM Program Memory	—	—	—	—
	ROM Program Memory	—	512	—	1K
	Data Memory (bytes)	36	36	68	68
	Data EEPROM (bytes)	64	64	64	64
Peripherals	Timer Module(s)	TMR0	TMR0	TMR0	TMR0
	Interrupt Sources	4	4	4	4
	I/O Pins	13	13	13	13
Features	Voltage Range (Volts)	2.0-6.0	2.0-6.0	2.0-6.0	2.0-6.0
	Packages	18-pin DIP, SOIC	18-pin DIP, SOIC	18-pin DIP, SOIC	18-pin DIP, SOIC

All PICmicro™ Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC16F8X Family devices use serial programming with clock pin RB6 and data pin RB7.

2.0 PIC16F8X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements the proper device option can be selected using the information in this section. When placing orders, please use the "PIC16F8X Product Identification System" at the back of this data sheet to specify the correct part number.

There are four device "types" as indicated in the device number.

1. **F**, as in PIC16F84. These devices have Flash program memory and operate over the standard voltage range.
2. **LF**, as in PIC16**LF**84. These devices have Flash program memory and operate over an extended voltage range.
3. **CR**, as in PIC16**CR**83. These devices have ROM program memory and operate over the standard voltage range.
4. **LCR**, as in PIC16**LCR**84. These devices have ROM program memory and operate over an extended voltage range.

When discussing memory maps and other architectural features, the use of **F** and **CR** also implies the **LF** and **LCR** versions.

2.1 Flash Devices

These devices are offered in the lower cost plastic package, even though the device can be erased and reprogrammed. This allows the same device to be used for prototype development and pilot programs as well as production.

A further advantage of the electrically-erasable Flash version is that it can be erased and reprogrammed in-circuit, or by device programmers, such as Microchip's PICSTART® Plus or PRO MATE® II programmers.

2.2 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices have all Flash locations and configuration options already programmed by the factory. Certain code and prototype verification procedures do apply before production shipments are available.

For information on submitting a QTP code, please contact your Microchip Regional Sales Office.

2.3 Serialized Quick-Turnaround-Production (SQTP℠) Devices

Microchip offers the unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number which can serve as an entry-code, password or ID number.

For information on submitting a SQTP code, please contact your Microchip Regional Sales Office.

2.4 ROM Devices

Some of Microchip's devices have a corresponding device where the program memory is a ROM. These devices give a cost savings over Microchip's traditional user programmed devices (EPROM, EEPROM).

ROM devices (PIC16CR8X) do not allow serialization information in the program memory space. The user may program this information into the Data EEPROM.

For information on submitting a ROM code, please contact your Microchip Regional Sales Office.

3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16CXX family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16CXX uses a Harvard architecture. This architecture has the program and data accessed from separate memories. So the device has a program memory bus and a data memory bus. This improves bandwidth over traditional von Neumann architecture where program and data are fetched from the same memory (accesses over the same bus). Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. PIC16CXX opcodes are 14-bits wide, enabling single word instructions. The full 14-bit wide program memory bus fetches a 14-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions (Example 3-1). Consequently, all instructions execute in a single cycle except for program branches.

The PIC16F83 and PIC16CR83 address 512 x 14 of program memory, and the PIC16F84 and PIC16CR84 address 1K x 14 program memory. All program memory is internal.

The PIC16CXX can directly or indirectly address its register files or data memory. All special function registers including the program counter are mapped in the data memory. An orthogonal (symmetrical) instruction set makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16CXX simple yet efficient. In addition, the learning curve is reduced significantly.

PIC16CXX devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register (W register), and the other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a $\overline{\text{borrow}}$ and $\overline{\text{digit borrow}}$ out bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

A simplified block diagram for the PIC16F8X is shown in Figure 3-1, its corresponding pin description is shown in Table 3-1.

FIGURE 3-1: PIC16F8X BLOCK DIAGRAM

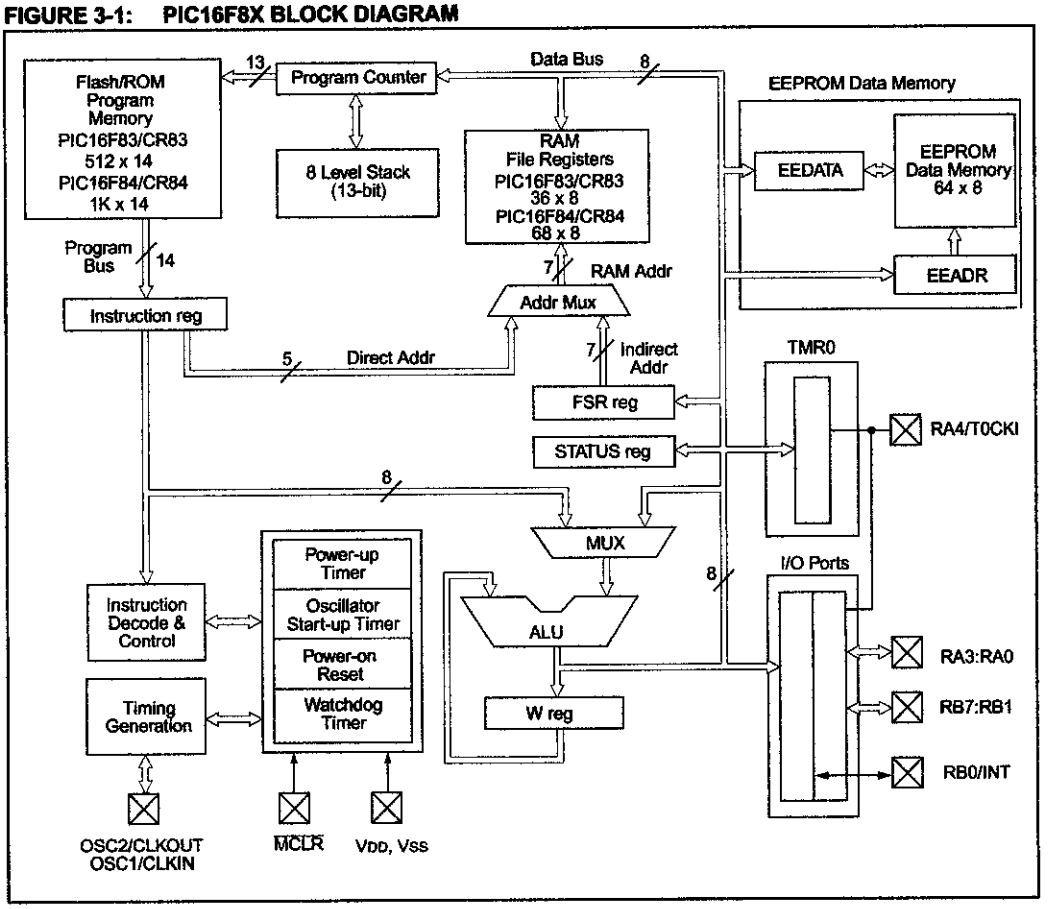


TABLE 3-1 PIC16F8X PINOUT DESCRIPTION

Pin Name	DIP No.	SOIC No.	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	16	16	I	ST/CMOS (3)	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	15	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
$\overline{MCLR}$	4	4	I/P	ST	Master clear (reset) input/programming voltage input. This pin is an active low reset to the device.
					PORTA is a bi-directional I/O port.
RA0	17	17	I/O	TTL	
RA1	18	18	I/O	TTL	
RA2	1	1	I/O	TTL	
RA3	2	2	I/O	TTL	
RA4/T0CKI	3	3	I/O	ST	Can also be selected to be the clock input to the TMR0 timer/counter. Output is open drain type.
					PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	6	6	I/O	TTL/ST (1)	RB0/INT can also be selected as an external interrupt pin.
RB1	7	7	I/O	TTL	
RB2	8	8	I/O	TTL	
RB3	9	9	I/O	TTL	
RB4	10	10	I/O	TTL	Interrupt on change pin.
RB5	11	11	I/O	TTL	Interrupt on change pin.
RB6	12	12	I/O	TTL/ST (2)	Interrupt on change pin. Serial programming clock.
RB7	13	13	I/O	TTL/ST (2)	Interrupt on change pin. Serial programming data.
VSS	5	5	P	—	Ground reference for logic and I/O pins.
VDD	14	14	P	—	Positive supply for logic and I/O pins.

Legend: I= input O = output I/O = Input/Output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in serial programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

3.1 Clocking Scheme/Instruction Cycle

The clock input (from OSC1) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the program counter (PC) is incremented every Q1, the instruction is fetched from the program memory and latched into the instruction register in Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-2.

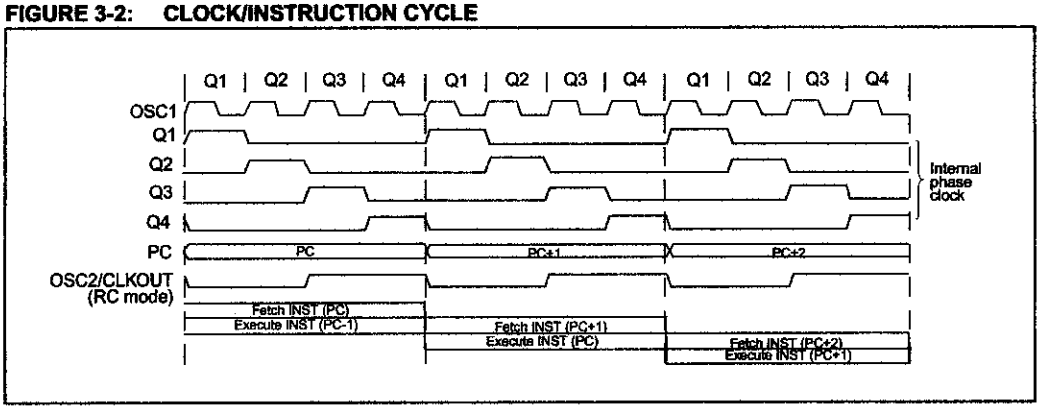
3.2 Instruction Flow/Pipelining

An "Instruction Cycle" consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO) then two cycles are required to complete the instruction (Example 3-1).

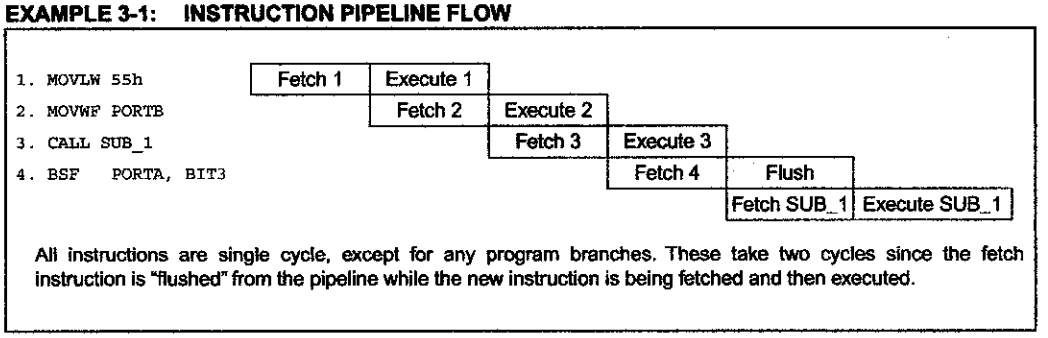
A fetch cycle begins with the Program Counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the "Instruction Register" in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-2: CLOCK/INSTRUCTION CYCLE



EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW



All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is "flushed" from the pipeline while the new instruction is being fetched and then executed.

4.0 MEMORY ORGANIZATION

There are two memory blocks in the PIC16F8X. These are the program memory and the data memory. Each block has its own bus, so that access to each block can occur during the same oscillator cycle.

The data memory can further be broken down into the general purpose RAM and the Special Function Registers (SFRs). The operation of the SFRs that control the "core" are described here. The SFRs used to control the peripheral modules are described in the section discussing each individual peripheral module.

The data memory area also contains the data EEPROM memory. This memory is not directly mapped into the data memory, but is indirectly mapped. That is, an indirect address pointer specifies the address of the data EEPROM memory to read/write. The 64 bytes of data EEPROM memory have the address range 0h-3Fh. More details on the EEPROM memory can be found in Section 7.0.

4.1 Program Memory Organization

The PIC16FXX has a 13-bit program counter capable of addressing an 8K x 14 program memory space. For the PIC16F83 and PIC16CR83, the first 512 x 14 (0000h-01FFh) are physically implemented (Figure 4-1). For the PIC16F84 and PIC16CR84, the first 1K x 14 (0000h-03FFh) are physically implemented (Figure 4-2). Accessing a location above the physically implemented address will cause a wrap-around. For example, for the PIC16F84 locations 20h, 420h, 820h, C20h, 1020h, 1420h, 1820h, and 1C20h will be the same instruction.

The reset vector is at 0000h and the interrupt vector is at 0004h.

FIGURE 4-1: PROGRAM MEMORY MAP AND STACK - PIC16F83/CR83

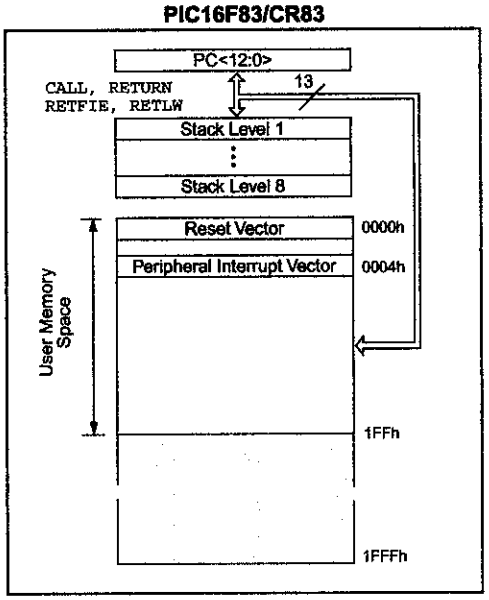
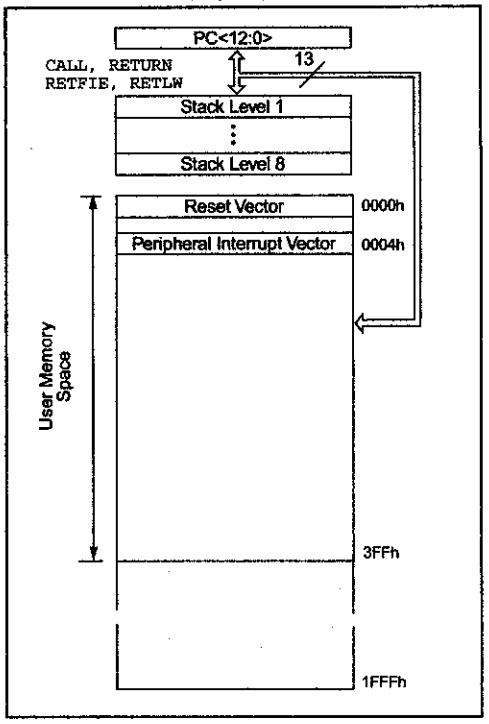


FIGURE 4-2: PROGRAM MEMORY MAP AND STACK - PIC16F84/CR84



4.2 Data Memory Organization

The data memory is partitioned into two areas. The first is the Special Function Registers (SFR) area, while the second is the General Purpose Registers (GPR) area. The SFRs control the operation of the device.

Portions of data memory are banked. This is for both the SFR area and the GPR area. The GPR area is banked to allow greater than 116 bytes of general purpose RAM. The banked areas of the SFR are for the registers that control the peripheral functions. Banking requires the use of control bits for bank selection. These control bits are located in the STATUS Register. Figure 4-1 and Figure 4-2 show the data memory map organization.

Instructions MOVWF and MOVF can move values from the W register to any location in the register file ("F"), and vice-versa.

The entire data memory can be accessed either directly using the absolute address of each register file or indirectly through the File Select Register (FSR) (Section 4.5). Indirect addressing uses the present value of the RP1:RP0 bits for access into the banked areas of data memory.

Data memory is partitioned into two banks which contain the general purpose registers and the special function registers. Bank 0 is selected by clearing the RP0 bit (STATUS<5>). Setting the RP0 bit selects Bank 1. Each Bank extends up to 7Fh (128 bytes). The first twelve locations of each Bank are reserved for the Special Function Registers. The remainder are General Purpose Registers implemented as static RAM.

4.2.1 GENERAL PURPOSE REGISTER FILE

All devices have some amount of General Purpose Register (GPR) area. Each GPR is 8 bits wide and is accessed either directly or indirectly through the FSR (Section 4.5).

The GPR addresses in bank 1 are mapped to addresses in bank 0. As an example, addressing location 0Ch or 8Ch will access the same GPR.

4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers (Figure 4-1, Figure 4-2 and Table 4-1) are used by the CPU and Peripheral functions to control the device operation. These registers are static RAM.

The special function registers can be classified into two sets, core and peripheral. Those associated with the core functions are described in this section. Those related to the operation of the peripheral features are described in the section for that specific feature.

FIGURE 4-1: REGISTER FILE MAP - PIC16F83/CR83

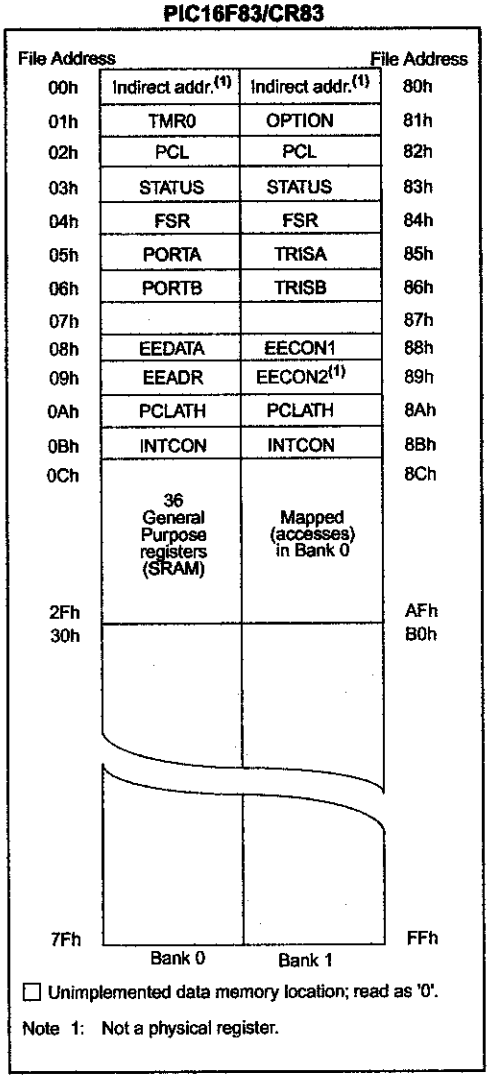


FIGURE 4-2: REGISTER FILE MAP - PIC16F84/CR84

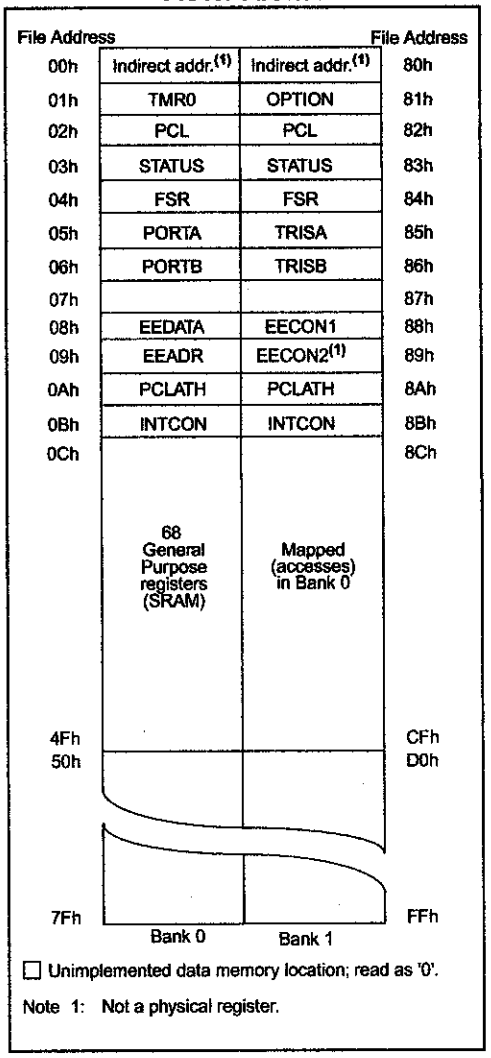


TABLE 4-1 REGISTER FILE SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note3)
Bank 0											
00h	INDF	Uses contents of FSR to address data memory (not a physical register)								---- ----	---- ----
01h	TMR0	8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu
02h	PCL	Low order 8 bits of the Program Counter (PC)								0000 0000	0000 0000
03h	STATUS (2)	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
04h	FSR	Indirect data memory address pointer 0								xxxx xxxx	uuuu uuuu
05h	PORTA	—	—	—	RA4/T0CKI	RA3	RA2	RA1	RA0	---x xxxx	---u uuuu
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0/INT	xxxx xxxx	uuuu uuuu
07h		Unimplemented location, read as '0'								---- ----	---- ----
08h	EEDATA	EEPROM data register								xxxx xxxx	uuuu uuuu
09h	EEADR	EEPROM address register								xxxx xxxx	uuuu uuuu
0Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of the PC (1)					---0 0000	---0 0000
0Bh	INTCON	GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
Bank 1											
80h	INDF	Uses contents of FSR to address data memory (not a physical register)								---- ----	---- ----
81h	OPTION_ REG	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h	PCL	Low order 8 bits of Program Counter (PC)								0000 0000	0000 0000
83h	STATUS (2)	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
84h	FSR	Indirect data memory address pointer 0								xxxx xxxx	uuuu uuuu
85h	TRISA	—	—	—	PORTA data direction register					---1 1111	---1 1111
86h	TRISB	PORTB data direction register								1111 1111	1111 1111
87h		Unimplemented location, read as '0'								---- ----	---- ----
88h	EECON1	—	—	—	EEIF	WRERR	WREN	WR	RD	---0 x000	---0 q000
89h	EECON2	EEPROM control register 2 (not a physical register)								---- ----	---- ----
0Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of the PC (1)					---0 0000	---0 0000
0Bh	INTCON	GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u

Legend: x = unknown, u = unchanged, - = unimplemented read as '0', q = value depends on condition.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a slave register for PC<12:8>. The contents of PCLATH can be transferred to the upper byte of the program counter, but the contents of PC<12:8> is never transferred to PCLATH.

2: The $\overline{TO}$ and $\overline{PD}$ status bits in the STATUS register are not affected by a $\overline{MCLR}$ reset.

3: Other (non power-up) resets include: external reset through $\overline{MCLR}$ and the Watchdog Timer Reset.

4.2.2.1 STATUS REGISTER

The STATUS register contains the arithmetic status of the ALU, the RESET status and the bank select bit for data memory.

As with any register, the STATUS register can be the destination for any instruction. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper-three bits and set the Z bit. This leaves the STATUS register as `000u uluu` (where `u` = unchanged).

Only the `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions should be used to alter the STATUS register (Table 9-2) because these instructions do not affect any status bit.

Note 1:	The IRP and RP1 bits (STATUS<7:6>) are not used by the PIC16F8X and should be programmed as cleared. Use of these bits as general purpose R/W bits is NOT recommended, since this may affect upward compatibility with future products.
Note 2:	The C and DC bits operate as a $\overline{borrow}$ and digit borrow out bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.
Note 3:	When the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. The specified bit(s) will be updated according to device logic

FIGURE 4-1: STATUS REGISTER (ADDRESS 03h, 83h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **IRP**: Register Bank Select bit (used for indirect addressing)
0 = Bank 0, 1 (00h - FFh)
1 = Bank 2, 3 (100h - 1FFh)
The IRP bit is not used by the PIC16F8X. IRP should be maintained clear.

bit 6-5: **RP1:RP0**: Register Bank Select bits (used for direct addressing)
00 = Bank 0 (00h - 7Fh)
01 = Bank 1 (80h - FFh)
10 = Bank 2 (100h - 17Fh)
11 = Bank 3 (180h - 1FFh)
Each bank is 128 bytes. Only bit RP0 is used by the PIC16F8X. RP1 should be maintained clear.

bit 4: $\overline{TO}$: Time-out bit
1 = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3: $\overline{PD}$: Power-down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2: **Z**: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1: **DC**: Digit carry/$\overline{borrow}$ bit (for `ADDWF` and `ADDLW` instructions) (For $\overline{borrow}$ the polarity is reversed)
1 = A carry-out from the 4th low order bit of the result occurred
0 = No carry-out from the 4th low order bit of the result

bit 0: **C**: Carry/$\overline{borrow}$ bit (for `ADDWF` and `ADDLW` instructions)
1 = A carry-out from the most significant bit of the result occurred
0 = No carry-out from the most significant bit of the result occurred
Note: For $\overline{borrow}$ the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high or low order bit of the source register.

4.2.2.2 OPTION_REG REGISTER

The OPTION_REG register is a readable and writable register which contains various control bits to configure the TMR0/WDT prescaler, the external INT interrupt, TMR0, and the weak pull-ups on PORTB.

Note: When the prescaler is assigned to the WDT (PSA = '1'), TMR0 has a 1:1 prescaler assignment.

FIGURE 4-1: OPTION_REG REGISTER (ADDRESS 81h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **RBPU**: PORTB Pull-up Enable bit
1 = PORTB pull-ups are disabled
0 = PORTB pull-ups are enabled (by individual port latch values)

bit 6: **INTEDG**: Interrupt Edge Select bit
1 = Interrupt on rising edge of RB0/INT pin
0 = Interrupt on falling edge of RB0/INT pin

bit 5: **T0CS**: TMR0 Clock Source Select bit
1 = Transition on RA4/T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4: **T0SE**: TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on RA4/T0CKI pin
0 = Increment on low-to-high transition on RA4/T0CKI pin

bit 3: **PSA**: Prescaler Assignment bit
1 = Prescaler assigned to the WDT
0 = Prescaler assigned to TMR0

bit 2-0: **PS2:PS0**: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

4.2.2.3 INTCON REGISTER

The INTCON register is a readable and writable register which contains the various enable bits for all interrupt sources.

Note:	Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>).

FIGURE 4-1: INTCON REGISTER (ADDRESS 0Bh, 8Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **GIE:** Global Interrupt Enable bit
1 = Enables all un-masked interrupts
0 = Disables all interrupts

Note: For the operation of the interrupt structure, please refer to Section 8.5.

bit 6: **EEIE:** EE Write Complete Interrupt Enable bit
1 = Enables the EE write complete interrupt
0 = Disables the EE write complete interrupt

bit 5: **T0IE:** TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt

bit 4: **INTE:** RB0/INT Interrupt Enable bit
1 = Enables the RB0/INT interrupt
0 = Disables the RB0/INT interrupt

bit 3: **RBIE:** RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2: **T0IF:** TMR0 overflow interrupt flag bit
1 = TMR0 has overflowed (must be cleared in software)
0 = TMR0 did not overflow

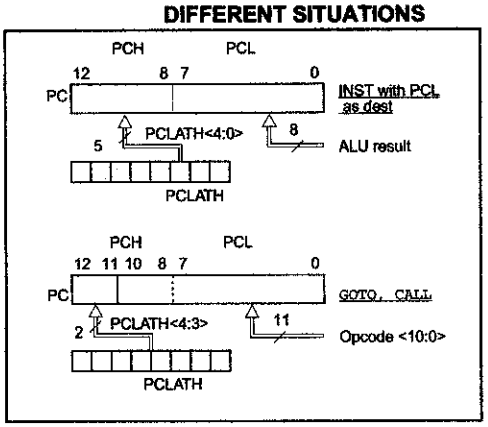
bit 1: **INTF:** RB0/INT Interrupt Flag bit
1 = The RB0/INT interrupt occurred
0 = The RB0/INT interrupt did not occur

bit 0: **RBIF:** RB Port Change Interrupt Flag bit
1 = When at least one of the RB7:RB4 pins changed state (must be cleared in software)
0 = None of the RB7:RB4 pins have changed state

4.3 Program Counter: PCL and PCLATH

The Program Counter (PC) is 13-bits wide. The low byte is the PCL register, which is a readable and writable register. The high byte of the PC (PC<12:8>) is not directly readable nor writable and comes from the PCLATH register. The PCLATH (PC latch high) register is a holding register for PC<12:8>. The contents of PCLATH are transferred to the upper byte of the program counter when the PC is loaded with a new value. This occurs during a CALL, GOTO or a write to PCL. The high bits of PC are loaded from PCLATH as shown in Figure 4-1.

FIGURE 4-1: LOADING OF PC IN DIFFERENT SITUATIONS



4.3.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When doing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256 word block). Refer to the application note *"Implementing a Table Read"* (AN556).

4.3.2 PROGRAM MEMORY PAGING

The PIC16F83 and PIC16CR83 have 512 words of program memory. The PIC16F84 and PIC16CR84 have 1K of program memory. The CALL and GOTO instructions have an 11-bit address range. This 11-bit address range allows a branch within a 2K program memory page size. For future PIC16F8X program memory expansion, there must be another two bits to specify the program memory page. These paging bits come from the PCLATH<4:3> bits (Figure 4-1). When doing a CALL or a GOTO instruction, the user must ensure that these page bits (PCLATH<4:3>) are programmed to the desired program memory page. If a CALL instruction (or interrupt) is executed, the entire 13-bit PC is "pushed" onto the stack (see next section). Therefore, manipulation of the PCLATH<4:3> is not required for the return instructions (which "pops" the PC from the stack).

Note:	The PIC16F8X ignores the PCLATH<4:3> bits, which are used for program memory pages 1, 2 and 3 (0800h - 1FFFh). The use of PCLATH<4:3> as general purpose R/W bits is not recommended since this may affect upward compatibility with future products.

4.4 Stack

The PIC16FXX has an 8 deep x 13-bit wide hardware stack (Figure 4-1). The stack space is not part of either program or data space and the stack pointer is not readable or writable.

The entire 13-bit PC is "pushed" onto the stack when a CALL instruction is executed or an interrupt is acknowledged. The stack is "popped" in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a push or a pop operation.

Note:	There are no instruction mnemonics called push or pop. These are actions that occur from the execution of the CALL, RETURN, RETLW, and RETFIE instructions, or the vectoring to an interrupt address.

The stack operates as a circular buffer. That is, after the stack has been pushed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

If the stack is effectively popped nine times, the PC value is the same as the value from the first pop.

Note:	There are no status bits to indicate stack overflow or stack underflow conditions.

4.5 Indirect Addressing; INDF and FSR Registers

The INDF register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR register (FSR is a *pointer*). This is indirect addressing.

EXAMPLE 4-1: INDIRECT ADDRESSING

- Register file 05 contains the value 10h
- Register file 06 contains the value 0Ah
- Load the value 05 into the FSR register
- A read of the INDF register will return the value of 10h
- Increment the value of the FSR register by one (FSR = 06)
- A read of the INDF register now will return the value of 0Ah.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF register indirectly results in a no-operation (although STATUS bits may be affected).

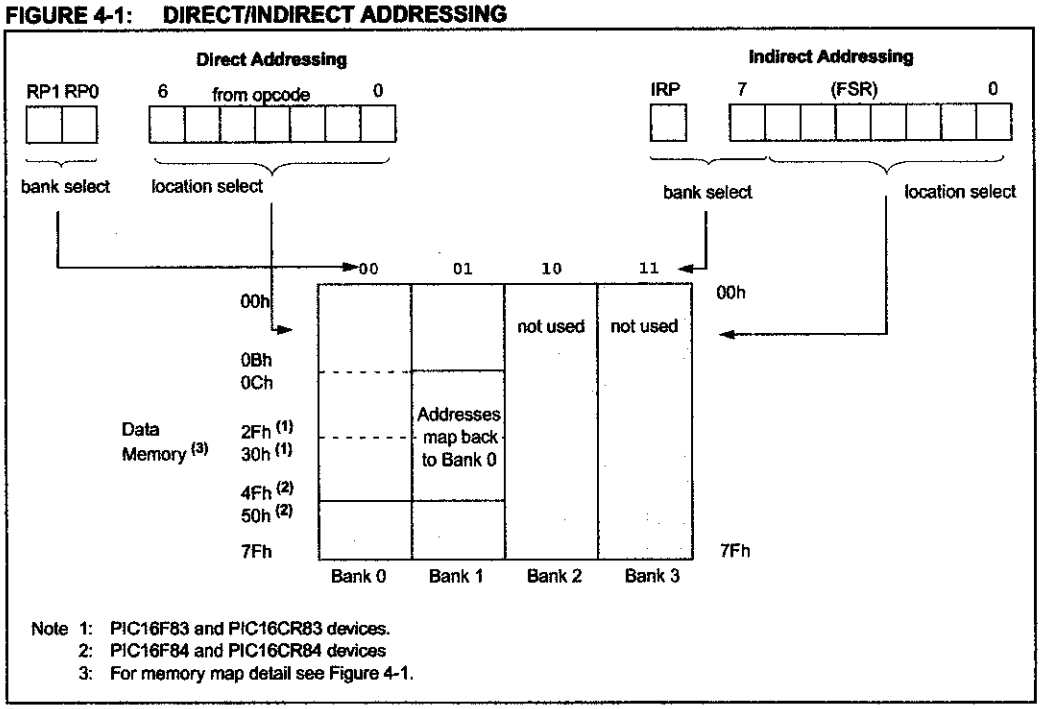
A simple program to clear RAM locations 20h-2Fh using indirect addressing is shown in Example 4-2.

EXAMPLE 4-2: HOW TO CLEAR RAM USING INDIRECT ADDRESSING

```
        movlw   0x20  ;initialize pointer
        movwf   FSR   ;  to RAM
NEXT    clrf    INDF  ;clear INDF register
        incf    FSR   ;inc pointer
        btfss   FSR,4 ;all done?
        goto    NEXT  ;NO, clear next
CONTINUE
        :             ;YES, continue
```

An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 4-1. However, IRP is not used in the PIC16F8X.

FIGURE 4-1: DIRECT/INDIRECT ADDRESSING



Note 1: PIC16F83 and PIC16CR83 devices.
2: PIC16F84 and PIC16CR84 devices
3: For memory map detail see Figure 4-1.

5.0 I/O PORTS

The PIC16F8X has two ports, PORTA and PORTB. Some port pins are multiplexed with an alternate function for other features on the device.

5.1 PORTA and TRISA Registers

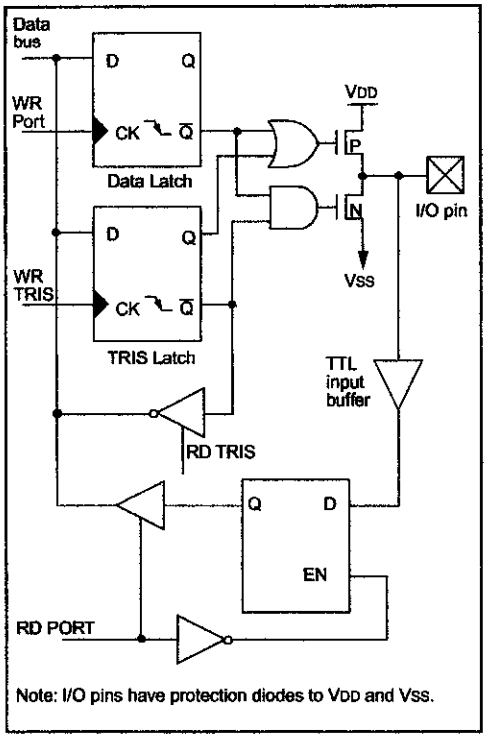
PORTA is a 5-bit wide latch. RA4 is a Schmitt Trigger input and an open drain output. All other RA port pins have TTL input levels and full CMOS output drivers. All pins have data direction bits (TRIS registers) which can configure these pins as output or input.

Setting a TRISA bit (=1) will make the corresponding PORTA pin an input, i.e., put the corresponding output driver in a hi-impedance mode. Clearing a TRISA bit (=0) will make the corresponding PORTA pin an output, i.e., put the contents of the output latch on the selected pin.

Reading the PORTA register reads the status of the pins whereas writing to it will write to the port latch. All write operations are read-modify-write operations. So a write to a port implies that the port pins are first read, then this value is modified and written to the port data latch.

The RA4 pin is multiplexed with the TMR0 clock input.

FIGURE 5-1: BLOCK DIAGRAM OF PINS RA3:RA0



EXAMPLE 5-1: INITIALIZING PORTA

```
CLRF    PORTA       ; Initialize PORTA by
                    ; setting output
                    ; data latches
BSF     STATUS, RP0 ; Select Bank 1
MOVLW   0x0F        ; Value used to
                    ; initialize data
                    ; direction
MOVWF   TRISA       ; Set RA<3:0> as inputs
                    ; RA4 as outputs
                    ; TRISA<7:5> are always
                    ; read as '0'.
```

FIGURE 5-2: BLOCK DIAGRAM OF PIN RA4

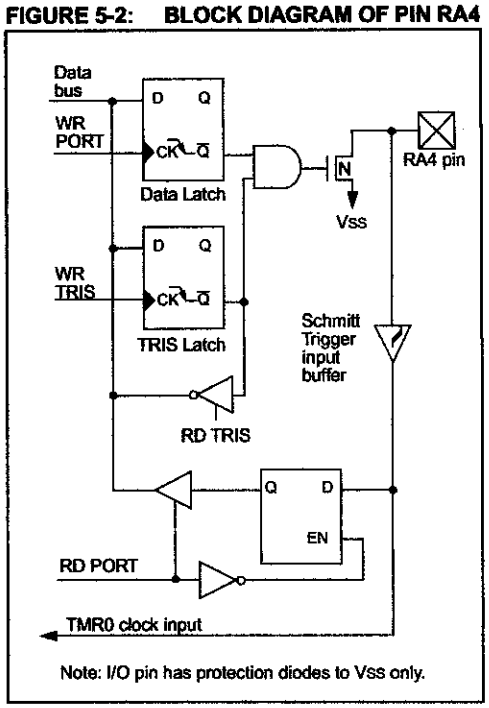


TABLE 5-1 PORTA FUNCTIONS

Name	Bit0	Buffer Type	Function
RA0	bit0	TTL	Input/output
RA1	bit1	TTL	Input/output
RA2	bit2	TTL	Input/output
RA3	bit3	TTL	Input/output
RA4/T0CKI	bit4	ST	Input/output or external clock input for TMR0. Output is open drain type.

Legend: TTL = TTL input, ST = Schmitt Trigger input

TABLE 5-2 SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
05h	PORTA	—	—	—	RA4/T0CKI	RA3	RA2	RA1	RA0	---x xxxx	---u uuuu
85h	TRISA	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	---1 1111	---1 1111

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are unimplemented, read as '0'

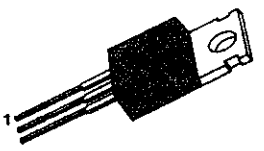
APPENDIX D

SPECIFICATION SHEET FOR TIP120

NPN EPITAXIAL
TIP120/121/122 DARLINGTON TRANSISTOR

MEDIUM POWER TRANSISTOR
SWITCHING APPLICATIONS
• Complementary to TIP125/126/127

TO-220



1.Base 2.Collector 3.Emitter

ABSOLUTE MAXIMUM RATINGS

Characterist: TIP120	Symbol	Rating	Unit
Collector-Base Voltage : TIP121	V_{CBO}	60	V
: TIP122		80	V
		100	V
Collector-Emitter Voltag : TIP120	V_{CEO}		
: TIP121		60	V
: TIP122		80	V
		100	V
Emitter-Base Voltage	V_{EBO}	5	V
Collector Current (DC)	I_C	5	A
Collector Current (Pulse)	I_C	8	A
Base Current (DC)	I_B	120	mA
Collector Dissipation (T_A=25°C)	P_C	2	W
Collector Dissipation (T_C=25°C)	P_C	65	W
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	-65 ~ 150	°C

ELECTRICAL CHARACTERISTICS (T_C =25°C)

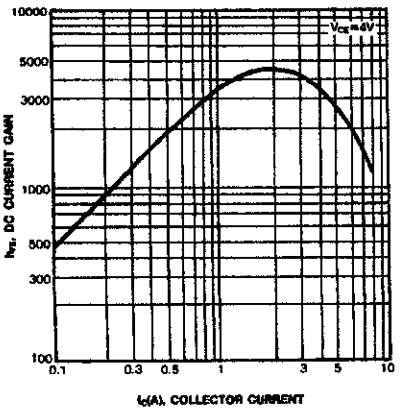
Characteristic	Symbol	Test Conditions	Min	Max	Unit
Collector Emitter Sustaining V : TIP120	V_{CEO}(sus)	I_C = 100mA, I_B = 0			
: TIP121			60		V
: TIP122			80		V
			100		V
Collector Cutoff Current : TIP120	I_{CEO}	V_{CE} = 30V, I_B = 0		2	mA
: TIP121		V_{CE} = 40V, I_B = 0		2	mA
: TIP122		V_{CE} = 50V, I_B = 0		2	mA
Collector Cutoff Current : TIP120	I_{CBO}	V_{CB} = 60V, I_E = 0		1	mA
: TIP121		V_{CB} = 80V, I_E = 0		1	mA
: TIP122		V_{CB} = 100V, I_E = 0		1	mA
Emitter Cutoff Current	I_{EBO}	V_{BE} = 5V, I_C = 0		2	mA
* DC Current Gain	h_{FE}	V_{CE} = 3V, I_C = 0.5A	1000		
		V_{CE} = 3V, I_C = 3A	1000		
* Collector Emitter Saturation Voltage	V_{CE}(sat)	I_C = 3A, I_B = 12mA		2.0	V
		I_C = 5A, I_B = 20mA		4.0	V
* Base Emitter On Voltage	V_{BE}(on)	V_{CE} = 3V, I_C = 3A		2.5	V
Output Capacitance	C_{OB}	V_{CB} = 10V, I_E = 0, f = 0.1MHz		200	pF

* Pulse Test: PW≤300$_m$s, Duty Cycle≤2%

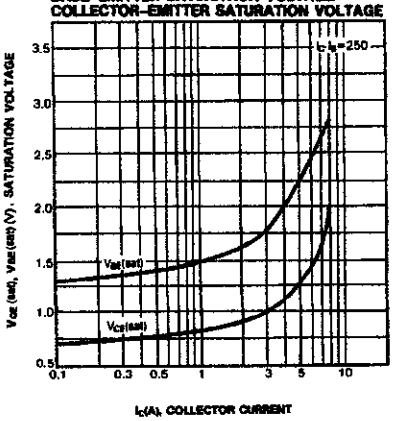
Rev. B.1

FAIRCHILD
SEMICONDUCTOR TM

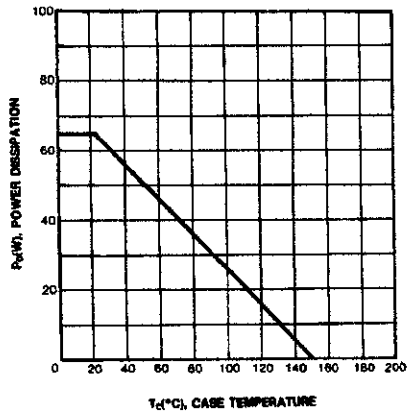
DC CURRENT GAIN



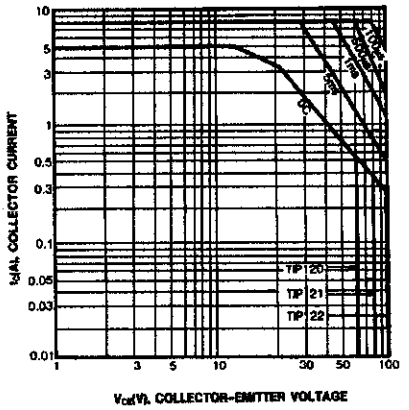
BASE-EMITTER SATURATION VOLTAGE
COLLECTOR-EMITTER SATURATION VOLTAGE



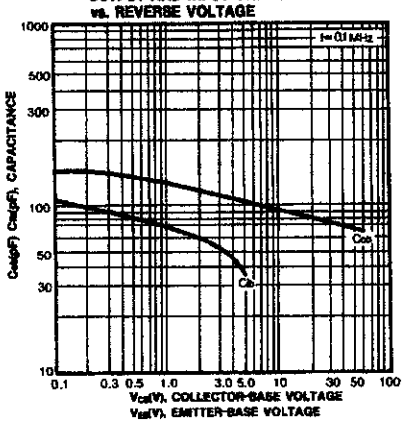
POWER DERATING

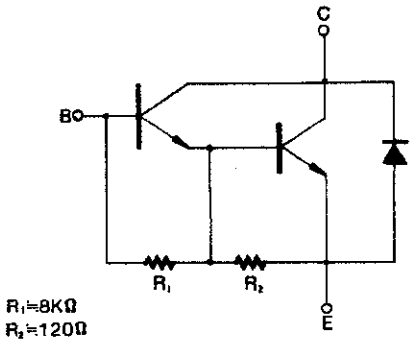


SAFE OPERATING AREA



OUTPUT AND INPUT CAPACITANCE
vs. REVERSE VOLTAGE





R_1≒8KΩ
R_2≒120Ω

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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

APPENDIX E

SPECIFICATION SHEET FOR 4050N HEX BUFFER

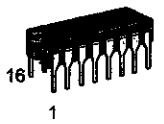
MC54/74HC4049
MC54/74HC4050

ex Buffers/Logic-Level
own Converters
gh–Performance Silicon–Gate CMOS

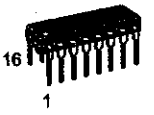
e MC54/74HC4049 consists of six inverting buffers, and the 4/74HC4050 consists of six noninverting buffers. They are identical in ıt to the MC14049UB and MC14050B metal–gate CMOS buffers. The :e inputs are compatible with standard CMOS outputs; with pullup tors, they are compatible with LSTTL outputs.

e input protection circuitry on these devices has been modified by nating the V_{CC} diodes to allow the use of input voltages up to 15 volts. , the devices may be used as logic–level translators that convert from a voltage to a low voltage while operating at the low–voltage power ly. They allow MC14000–series CMOS operating up to 15 volts to be 'aced with High–Speed CMOS at 2 to 6 volts. The protection diodes to are Zener diodes, which protect the inputs from both positive and itive voltage transients.

- utput Drive Capability: 10 LSTTL Loads
- utputs Directly Interface to CMOS, NMOS, and TTL
- perating Voltage Range: 2 to 6 V
- ow Input Current: 5 µA
- igh Noise Immunity Characteristic of CMOS Devices
- Compliance with the Requirements Defined by JEDEC Standard o. 7A
- hip Complexity: 36 FETs or 9 Equivalent Gates (4049)
  24 FETs or 6 Equivalent Gates (4050)



J SUFFIX
CERAMIC PACKAGE
CASE 620–10



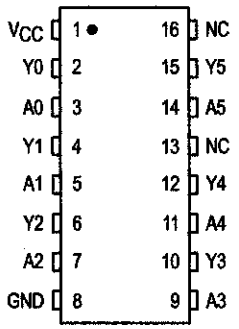
N SUFFIX
PLASTIC PACKAGE
CASE 648–08

D SUFFIX
SOIC PACKAGE
CASE 751B–05

ORDERING INFORMATION

MC54HCXXXXJ	Ceramic
MC74HCXXXXN	Plastic
MC74HCXXXXD	SOIC

PIN ASSIGNMENT



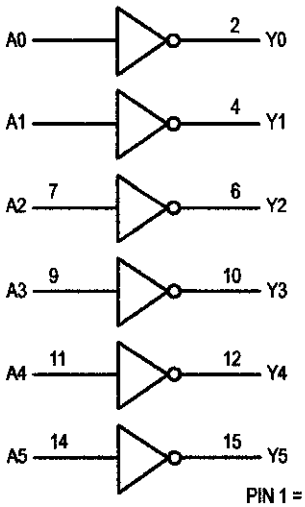
NC = NO CONNECTION

FUNCTION TABLE

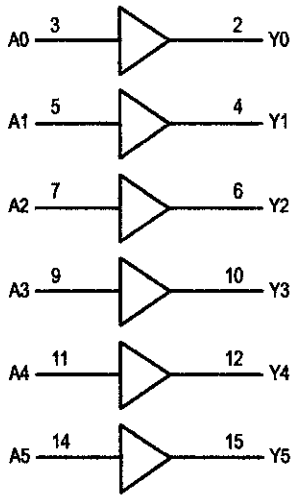
A Input	Y Outputs	
	HC4049	HC4060
L	H	L
H	L	H

LOGIC DIAGRAMS

HC4049 (INVERTING BUFFER)



HC4050 (NONINVERTING BUFFER)



PIN 1 = V_{CC}
PIN 8 = GND
PINS 13, 16 = NO CONNECTION

IMUM RATINGS*

ıbol	Parameter	Value	Unit
:C	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
in	DC Input Voltage (Referenced to GND)	– 1.5 to + 18	V
ıut	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
n	DC Input Current, per Pin	± 20	mA
ut	DC Output Current, per Pin	± 25	mA
:C	DC Supply Current, V_{CC} and GND Pins	± 50	mA
D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
tg	Storage Temperature	– 65 to + 150	°C
L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	 260 300	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields referenced to the GND pin, only. Extra precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, the ranges GND ≤ V_{in} ≤ 15 V and GND ≤ V_{out} ≤ V_{CC} are recommended.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

imum Ratings are those values beyond which damage to the device may occur.
ctional operation should be restricted to the Recommended Operating Conditions.
ating — Plastic DIP: – 10 mW/°C from 65° to 125°C
Ceramic DIP: – 10 mW/°C from 100° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
igh frequency or heavy load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

:OMMENDED OPERATING CONDITIONS

ıbol	Parameter		Min	Max	Unit
CC	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
/in	DC Input Voltage (Referenced to GND)		0	V_{CC} to 15	V
out	DC Output Voltage (Referenced to GND)		0	V_{CC}	V
ΓA	Operating Temperature, All Package Types		– 55	+ 125	°C
, tf	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

mbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
/IH	Minimum High–Level Input Voltage	V_{out} = V_{CC} – 0.1 V |I_{out}| ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
VIL	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V |I_{out}| ≤ 20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
/OH	Minimum High–Level Output Voltage	V_{in} = V_{IH} |I_{out}| ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} |I_{out}| ≤ 4.0 mA |I_{out}| ≤ 5.2 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
/OL	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} |I_{out}| ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} |I_{out}| ≤ 4.0 mA |I_{out}| ≤ 5.2 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
Iin	Maximum Input Leakage Current	V_{in} = V_{CC} or GND V_{in} = 15 V	6.0 6.0	±0.1 0.5	±1.0 5.0	±1.0 5.0	μA
CC	Maximum Quiescent Supply Current (per Package)	V_{in} = 15 V or GND I_{out} = 0 μA	6.0	2	20	40	μA

E: Information on typical parametric values can be found in Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

mbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
PLH, PHL	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	2.0 4.5 6.0	85 17 14	105 21 18	130 26 22	ns
TLH, THL	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
Cin	Maximum Input Capacitance		10	10	10	pF

ES:
For propagation delays with loads other than 50 pF, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).
Information on typical parametric values can be found in Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
CPD	Power Dissipation Capacitance (Per Buffer)*	27	pF

d to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the orola High–Speed CMOS Data Book (DL129/D).

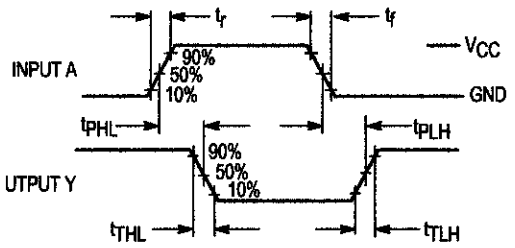


Figure 1a. Switching Waveforms (HC4049)

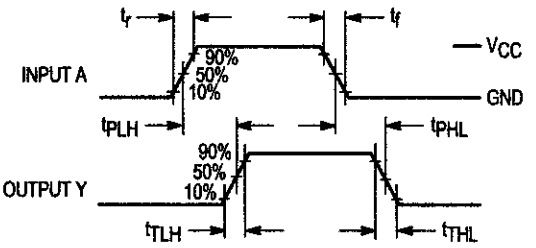
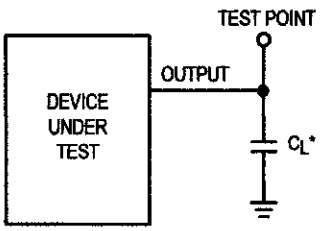


Figure 1b. Switching Waveforms (HC4050)

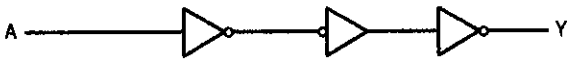


* Includes all probe and jig capacitance

Figure 2. Test Circuit

LOGIC DETAIL

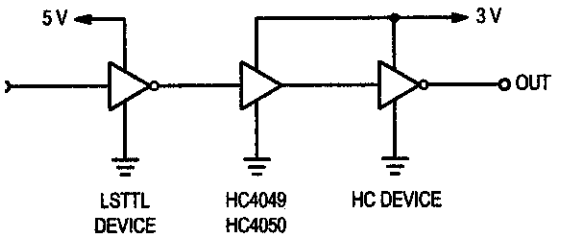
HC4049
(1/6 of the Device)



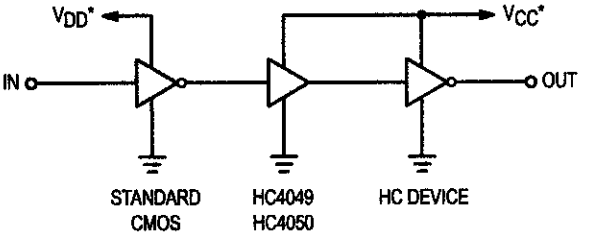
HC4050
(1/6 of the Device)

TYPICAL APPLICATIONS

LSTTL to Low–Voltalge HSCMOS



High–Voltage CMOS to HSCMOS



E: To determine the noise immunity for the LSTTL to low–voltage configuration, use Eq. 1 and Eq. 2:

(TTL) V_{OH} – (CMOS) V_{IH} Eq. 1
(TTL) V_{OL} – (CMOS) V_{IL} Eq. 2

For the supply levels shown:
2.4 – 3 (75%) = 2.4 – 2.25 = 0.15 V
0.4 – 3 (15%) = 0.4 – 0.45 = 0.05 V

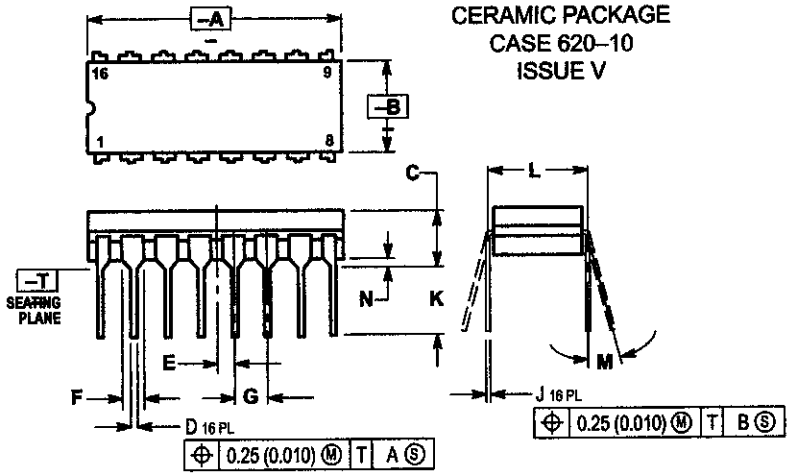
Therefore, worst case noise immunity is 50 mV.
For supply levels greater than 4.5 volts use the 74HCT04A for direct interface to TTL outputs.

***Table 1. Supply Examples**

V_{DD}	V_{CC}
15 V	2 V
12 V	5 V
12 V	3 V

OUTLINE DIMENSIONS

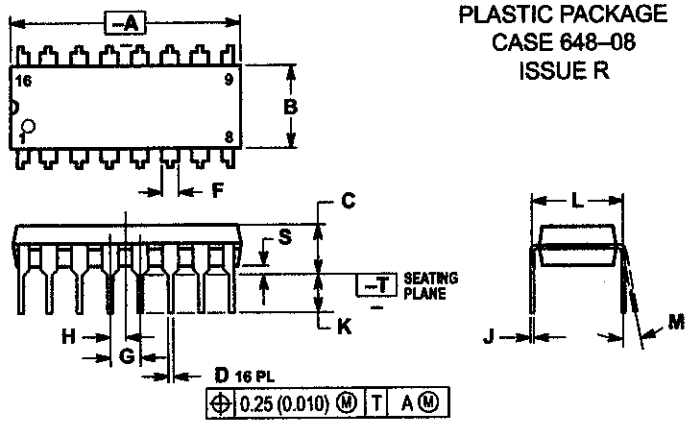
J SUFFIX
CERAMIC PACKAGE
CASE 620–10
ISSUE V



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

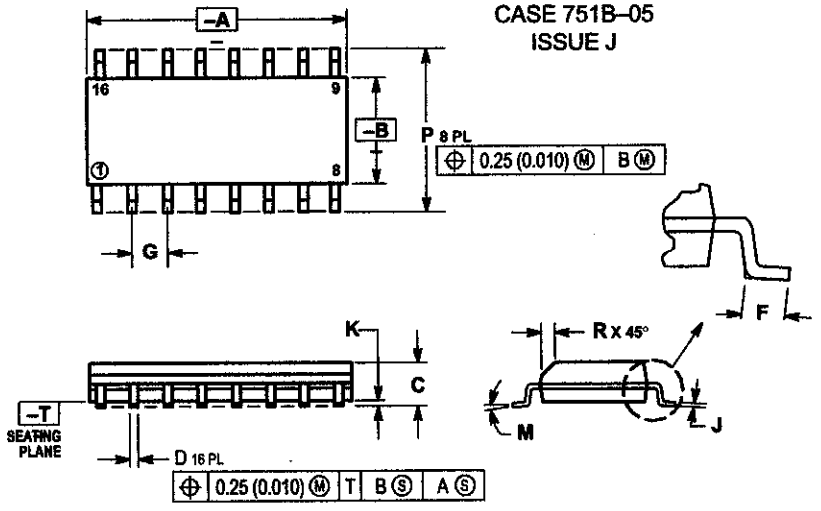
N SUFFIX
PLASTIC PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.070	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J

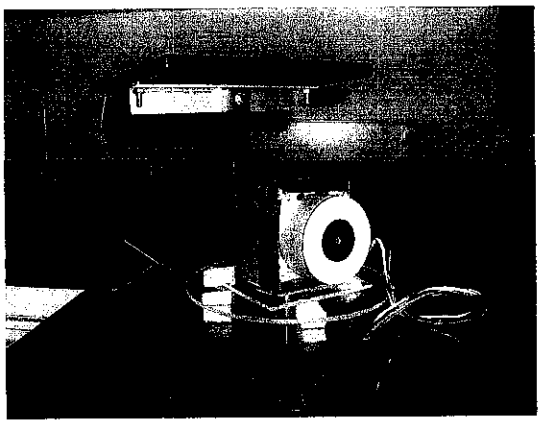


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

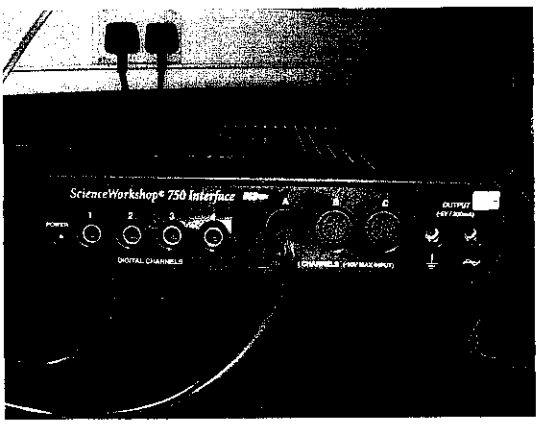
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

APPENDIX F

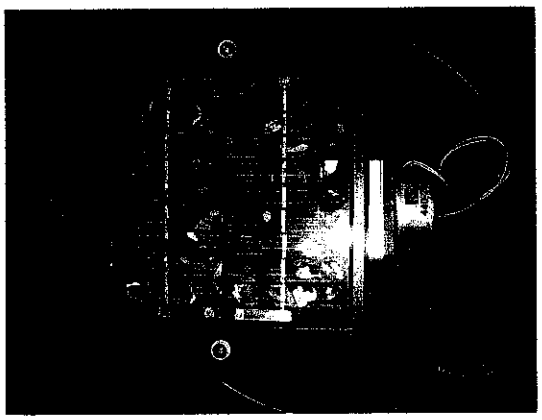
PHOTO GALLERY



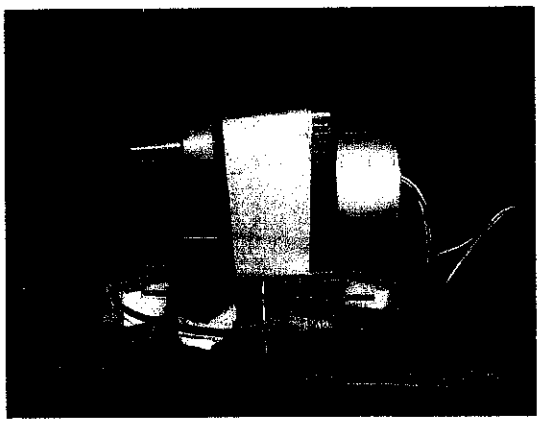
Power Point Tracking System



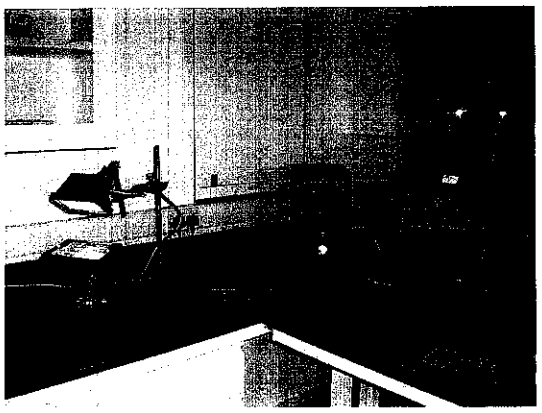
PASCO device for data recording



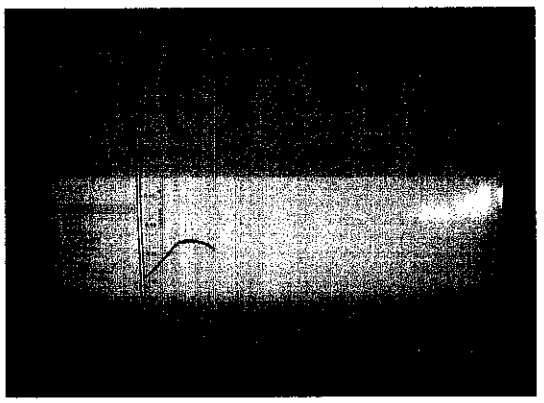
Polycrystalline photovoltaic (PV)



The tracker part



Experiment Setup



Data Studio