Dissertation

Design and Simulate Radio Frequency (RF) CMOS Mixer Circuit

by

Muhammad Syazwan bin Muhammad Adib (5751)

Dissertation submitted in partial fulfilment of
the requirements for the
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CERTIFICATION OF APPROVAL

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Approved by,

(A.P. Dr Mohammad b Awan)

UNIVERSITI TEKNOLOGI PETRONAS

TRONOH, PERAK

JUNE 2008

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

MUHAMMAD SYAZWAN BIN MUHAMMAD ADIB

Acknowledgment

"I would like to take this opportunity to express my heartfelt gratitude to those who had contributed in making my final year project (FYP) a success; whether directly or indirectly. To A.P. Dr Mohammad b Awan; your continuous support, good guidance and useful advices shall always be appreciated. My sincere gratitude also goes to my parent and my colleagues, for their continuous support and useful advices which I shall forever remember. Thank You."

[Muhammad Syazwan b Muhammad Adib, Electrical Department – Jan 2008]

ABSTRACT

Radio frequency design has been one of the principal research areas in the recent past. Much of work has been done in integrating data with wireless communication. Since a decade ago, the frequencies for such communication have been in free bands available in the low frequency spectrum like 900 MHz and lower. With rapid improvement in the technology of microelectronic nowadays, these frequency spectrums are improved to be within the range of ultra band frequencies of GHz. These emergences of several RF Wireless Communication standards of communication have demanded availability of low cost analogue blocks for use in transceiver. Despite rigorous research undergoing, it has been difficult to meet the design specification by low cost technologies like CMOS. In this project, the presented mixer down converts Radio Frequency (RF) of 1.8 GHz to 200 MHz which typifies specifications for a GSM 1800 receiver with Voltage Conversion Gain (VCG) of 7.703 dB, IIP3 of 10.916 dBm and Noise Figure (NF) of 11.094 dB with current utilization of 6 mA. This high conversion gain and low noise figure mixer is achieved by utilizing Differential Gilbert Mixer Cell. The mixer was simulated in analogue environment of Spectra Cadence Schematic.

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ABBREVIATIONS AND NOMENCLATURES

BICMOS	Bipolar Complimentary Metal Oxide Semiconductor
CMOS	Complimentary Metal Oxide Semiconductor
CG-CS	Common Gate-Common Source
dB	Decibels
dBm	Decibels with respect to 1mW
DC	Direct Current
DRC	Design Check Rule
DSB	Double Side Band
GaAs	Gallium Arsenide
gm	Gate Transconductance of a MOSFET
IC	Integrated Circuit
IF	Intermediate Frequency
IIP3	Input 3rd Order Intercept Point
LNA	Low Noise Amplifier
LO	Local Oscillator
LVS	Layout versus Schematic
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NF	Noise Figure
R	Resistance
RF	Radio Frequency
RFICs	Radio Frequency ICs
PSS	Periodic Steady State
SNR	Signal to Noise Ratio
SSB	Single Side Band
VCG	Voltage Conversion Gain
WiFi	Wireless Fidelity

CHAPTER 1
INTRODUCTION

1.0 Background of Study

The purpose of a CMOS mixer is to convert a base band or intermediate frequency to the higher RF frequency (up-conversion mixer) or to translate an RF frequency to a lower frequency base-band or Intermediate Frequency (IF) (down-conversion mixer) by multiplying the input signal with Local Oscillator (LO) signal. This report describes a down converter CMOS mixer that converts RF of 1.8 GHz to 200 MHz.

1.1 Problem Statement

The frequency translation process in a CMOS mixer will generate some unwanted signal or noises to degrade the Signal-to-Noise ratio (SNR). Linearity of a mixer also is an essential factor in designing a good high gain mixer and the linearity of the mixer effects. There are some tradeoffs with having high linearity and gain, the power consumption and noise of the circuit will also increase as well [1].

1.2 Objectives and Scope of Study

The objectives of the study are:

- To come up with a good design of a CMOS mixer circuit with high linearity and has the quality to improve the output to input gain as well as the SNR ratio.
- To simulate the complete circuit of a CMOS mixer using SPECTRE and verify its performances.
- To do some improvisations on the design parameters of the simulated mixer circuit wherever applicable.

The scope of study is to present the designed-CMOS mixer performance on Gain, 1dB Compression Gain, 3rd Order Intercept Point, Noise Figure (NF) and linearity by setting it up to the set design specifications.

The following specifications are used for guideline in designing a CMOS mixer circuit [1] :

Total Current < 20mA

V_{dd} = 3.3V

Power Consumption < 66mW

IIP3 > 20dBm

Gain between 0 to 5dB

Noise Figure < 18dB

RF signal = 1.8 GHz

LO signal = 1.6 GHz

The figures for the specification are used based on the latest design of a CMOS mixer circuit for a cable tuner utilizing 0.18 μ library technology.

CHAPTER 2
LITERATURE REVIEW

2.0 Mixer Theory

Mixer; or frequency converters are also sometimes called multipliers and in the early days of super heterodyne receivers they were often called "detectors". Whatever name it is known by, the requirement is that the mixer has the ability to:

- Convert the desired signal from the received frequency to the receiver's first IF frequency.
- Convert the signal with minimum distortion and/or additive noise
- Convert the signal with minimum loss
- Convert the signal with good frequency accuracy

Mixers are used for frequency translation; they convert the Radio Frequency (RF) to Intermediate Frequency (IF) by multiplying it with the Local Oscillator (LO) signal applied to the mixers. The operation is as shown in Figure 1. The mixing outcome produces two signal located at $w_{LO} + w_{RF}$ and $w_{LO} - w_{RF}$ frequency. One signal is the wanted signal and the other is the unwanted based on what type the mixer is configured whether an up converting or a down converting mixer respectively [1]. The method of operation can be defined by equation (1).

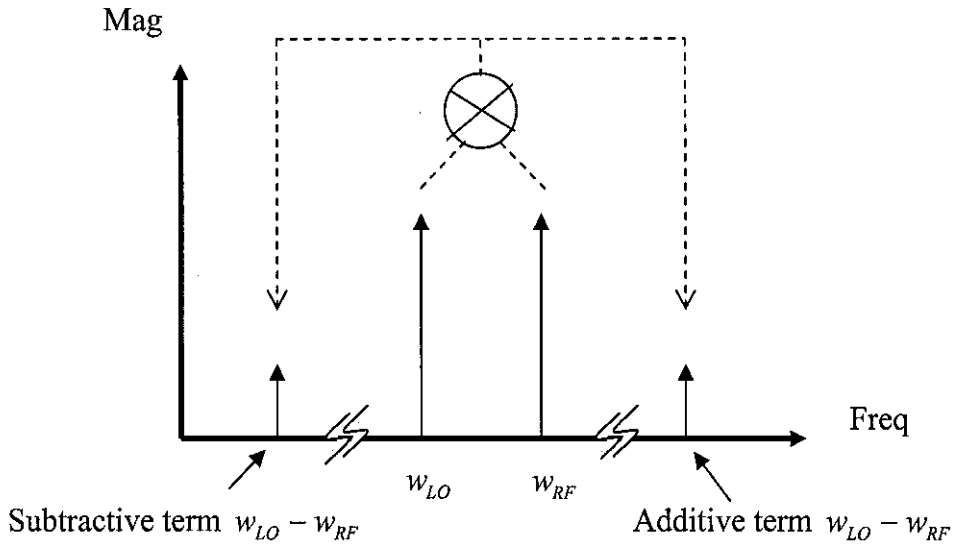

Figure 1: Multiplication of Two Different Frequency Terms

$$V_{out}(t) = \cos w_1 t \times \cos w_2 t$$

$$V_{out}(t) = \frac{1}{2}\left(\cos(w_1 - w_2)t + \cos(w_1 + w_2)t\right) \quad (1)$$

2.1 Preliminary Aspect of The Mixer Design

There are a few aspects that need to be understood in order to design a good CMOS mixer circuit. There are as follow:

2.1.1 CMOS Technology

CMOS is also known as complementary-symmetry metal–oxide–semiconductor which the term "complementary-symmetry" is referring to the fact that the digital design style of CMOS uses complementary and symmetrical pairs of p-type and n-type MOSFETs for logic functions.

A metal–oxide–semiconductor field-effect transistor (MOSFET) is based on the modulation of charge concentration caused by a MOS capacitance [2]. MOSFET have two terminals (source and drain) where each is connected to separate highly doped regions. These regions can be either p-type or n-type, but with condition that they must both be of the same type. These two regions must be separated with a

highly doped region of the same type which is called as the 'body' as shown in Figure 2. The 'gate' which is the active region of the MOS constitutes a MOS capacitance with a third electrode. This region is located above the 'body' and usually insulated with an oxide to separate it from the other regions.

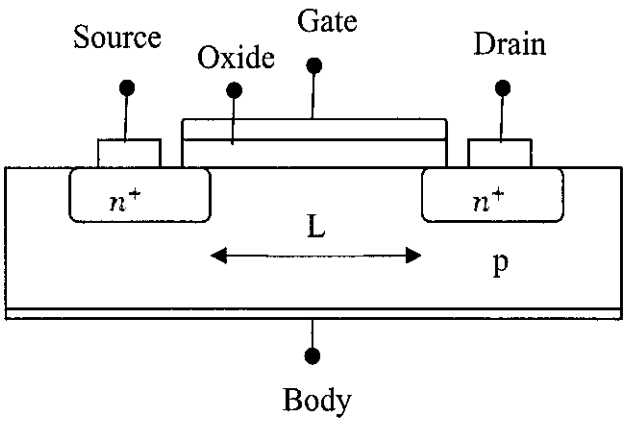

Figure 2: Cross Section of an NMOS

For an N-channel or n-MOSFET as in Figure 2, the source and the drain are from the 'n+' regions whereas the body is a 'p' region. As method of operation, when a positive voltage is supplied to the gate-source; by depleting the region of hole thus an N-channel will be created at the surface of the P region. This channel extends between the source and the drain. Current will only be conducted through this channel when the gate potential is high enough to attract electrons from the source into the channel. In contrary, when negative voltage is supplied to the gate-source, this channel disappears thus no current can flow from the source to the drain.

2.1.2 Competing Technology

The market interest is evolving from high cost technologies like GaAs (Gallium Arsenide) that provides active and passive devices able to work at radio frequency, but characterized by a low scale of integration; to a low cost standard technology like CMOS [2].

2.1.2.1 Gallium Arsenide Technology (GaAs)

GaAs gas can be found in high frequencies IC mainly due to its properties of high electron mobility (approximately 5 to 10 times more than Silicon) and high peak velocity. Thus for the same input voltages GaAs devices have higher output currents, and thus higher g_m than the corresponding silicon devices [2]. One characteristic that GaAs has is it enables faster charging and discharging of both load and parasitic capacitance which results in an increase in speed of operation. In addition, the substrate has higher resistivity (almost five times larger than silicon) which reduces the cross talk between devices.

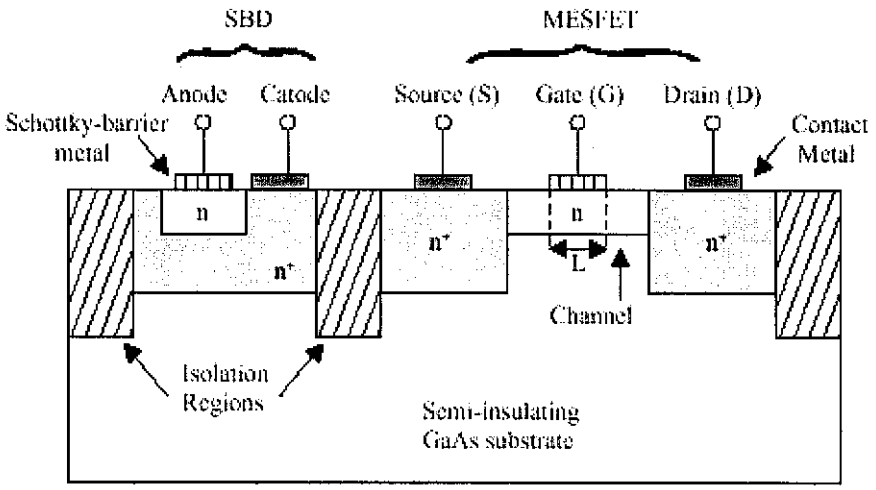

Figure 3: Cross Sectional View of GaAs MESFET

MESFET is a good example of device which utilizes this type of technology as in Figure 3. It operations is very similar to the silicon JFET but only for n-MOSFET. This technology cannot be implemented for p-mosfet as holes have relatively low drift mobility to be used in GaAs. In fact, this is the advantage of using GaAs technology as it lacks of complementary transistors. Another important feature that allows GaAs integrated circuits to have perfect performance in the GHz bands is the availability of high quality passive components [2].

2.1.2.2 Bipolar Complementary MOS Technology (BiCMOS)

This technology as laid in Figure 4 combines the abilities of CMOS like high scale integration, low power consumption, high noise immunity with plus points of bipolar technologies like high speed and high drive capabilities [2]. Definitely, this

technology is better than GaAs in term of cost estimation, but still costly relatively to the CMOS technology as it requires additional masks. Similarly to GaAs, the resistivity of the silicon substrate used in this technology is higher than CMOS technology. This is beneficial as it reduces the cross talk between devices.

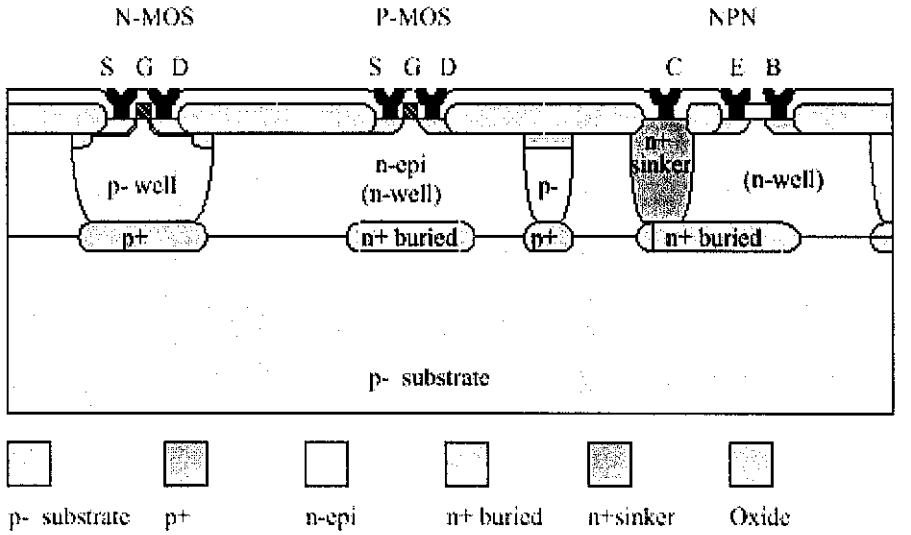

Figure 4: Cross Sectional View of Devices in BiCMOS Process

2.2 Advantages and Disadvantages of CMOS

As with the other available technologies, there are a few advantages and disadvantages of CMOS and it will be described in the next sub-section as follow:

2.2.1 Advantages of CMOS

The single major advantage of CMOS lies in very cheap and well-designed fabrication processes [2]. Undeniably, cost is a major concern in the chip-related industry, which CMOS is by far, the most economical in comparison to the other technologies. It is to be estimated that GaAs is at least 200 times costlier to MOS whereas Bipolar is 50 times. Furthermore, the fabrication of the CMOS has wide popularity due to its extensive digital design. Lately, with decrease in the channel length, the maximum usable frequency of MOS has also gone higher up to GHz [2].

2.2.2 Disadvantages of CMOS

MOS to be known not be suited for high frequency operation. MOS has a lower unity gain frequency as compared to the other competing technology. Besides, CMOS tends to be an undefined model at high frequency [2]. This is due to MOS has unpredictable operations at high frequency with low frequency models failed as well to predict its operations. Therefore, there surely is a difficulty when it comes to design using MOS as design tools when it fails to predict its exact operation. The noise contributed from MOS as well need to be studied properly as other technologies do not suffer from inconsistency of behaviour unlike CMOS.

2.3 Passive Device Used in CMOS Technology

Other than MOSFET which is an active device, there is as well passive device used in the CMOS technology such as resistor.

2.3.1 Resistors

There are several options available for resistor in MOS process include poly, source-drain diffusions, well, MOS transistor, metal interconnect and many more. Poly has more resistivity than metal layers, tolerance is often poor and the temperature coefficient may go high but in contrary it has the advantage of reasonable low parasitic capacitance per unit area and low voltage coefficients [2]. Source drain is very similar to poly in term of characteristic, but with larger parasitic capacitance and lower temperature coefficient. Meanwhile, well provides higher resistance of the order 1-10 $k\Omega$ but it has large parasitic capacitance, large temperature and voltage coefficients [2].

MOS transistors can be used as a resistor with suitable gate to source voltage. Incremental resistance of a long channel MOS in triode region is as in equation (2).

$$R_{ds} \approx \left[\mu C_{OX} \frac{W}{L} \left[(V_{GS} - V_T) - V_{DS} \right]^{-1} \right] \qquad (2)$$

2.4 Type of Noises Available

Undeniably, noise contributes a big motivation in almost all circuit design. But in wireless front-end design, its importance is overwhelmed. In electronics, noise is usually referred as unwanted signal that contains no information. There are many potential sources of noise which are external noise; which can be minimized using any shielding method while the other one is internal noise (fundamental noise). The latter type cannot be cancelled, but can only be minimized through better design. There a few types of fundamental noises in electronic systems; Thermal Noise, Shot Noise, Flicker Noise, Popcorn Noise and many more. However, these noises are not as significant as DSB and SSB noise figure and noises due to LO leakage.

2.4.1 DSB and SSB

When two signals are multiplied, two different frequencies terms will show up which are the additive term and the subtractive term. The output frequency spectrum also consists of two terms if the LO frequency is fixed. The IF term consists of two terms; one is $w_{LO} - w_{RF}$ which is the desired frequency term and the other is $w_{IM} - w_{LO}$. If the image term is considered, the amount of noise in the IF frequency spectrum will be doubled. If the noise figure is considered neglecting the image noise, it is called as double side band (DSB) noise figure. If the image noise is considered then it is called as single side band (SSB). However, SSB is 3dB higher than DSB noise as in Figure 5.

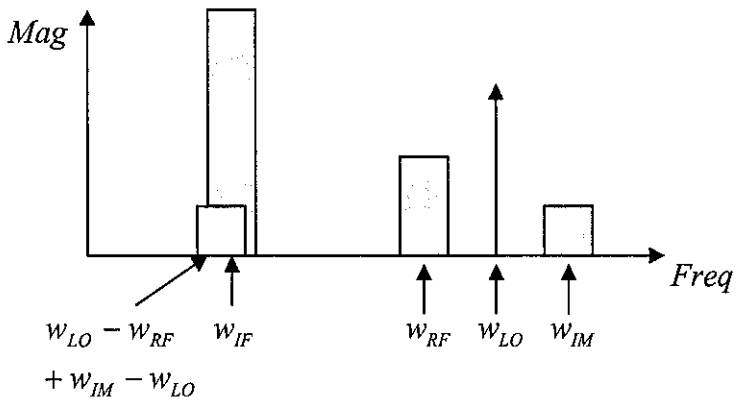

Figure 5: Accumulation of RF and Image Noise into The IF Band

2.4.2 LO Leakage

If a single balanced mixer is used, the LO signal appears at the IF output due to the bias current as in Figure 6, and the LO leakage signal makes the design of the IF filter more difficult because the LO leakage signal is close to IF frequency. Most of the LO leakage problems are caused by transistor mismatches [2]. The LO leakage problem is solved by using a double balanced mixer so that the DC bias current term at the output is cancelled. Hence, the LO signal does not appear at the IF output anymore.

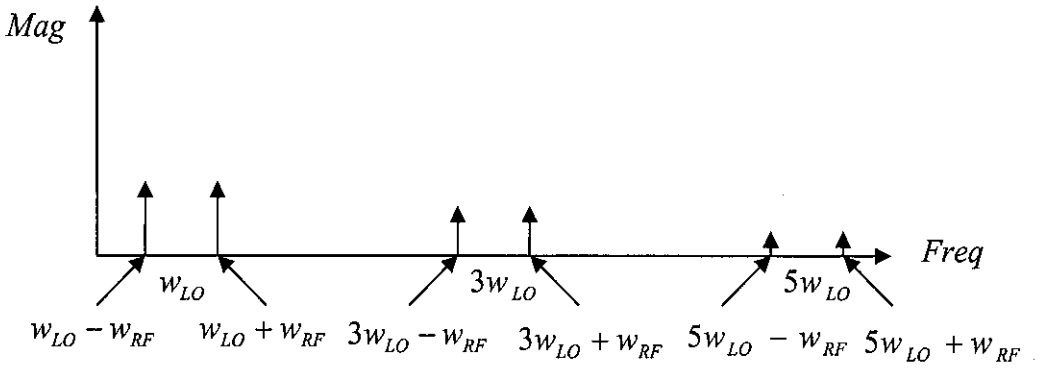

Figure 6: Output Frequency Spectrum of Double Balanced Mixer

2.5 Mixer Performances

There are several criteria that can be observed as measurement to the performance level of the CMOS Mixer. These include the Voltage Conversion Gain, Linearity as well as the Noise Figure.

2.5.1 Voltage Conversion Gain

Voltage Conversion Gain of a mixer is defined as the Root Mean Square (rms) voltage of the signal at the IF frequency divided by the rms voltage of the signal at the RF frequency [1]. The two basic types are conversion voltage gain and conversion power gain. If all switching MOS are perfect switches, therefore the conversion voltage gain can be approximated as following in equation (3).

$$G_V = \frac{2}{\pi} g_m . R_{out} \qquad (3)$$

Hence the conversion power gain is as in equation (4).

$$G_p = \left(\frac{2}{\pi} g_m . R_{out}\right)^2 \frac{R_{in}}{R_{out}} \qquad (4)$$

2.5.2 Linearity

Linearity describes the region of operation where the output signal varies proportionally to the input signal. There are several ways of measuring linearity performance of a mixer such as 1dB gain compression point and 3rd order intercept point (IIP3) [3].

2.5.2.1 1dB Gain Compression Point

The 1dB gain compression point is defined as the input power level in dBm at which the overall gain of amplifier is reduced by 1dBm from its maximum value where it would have been if it were an ideally linear device [3] as in Figure 7.

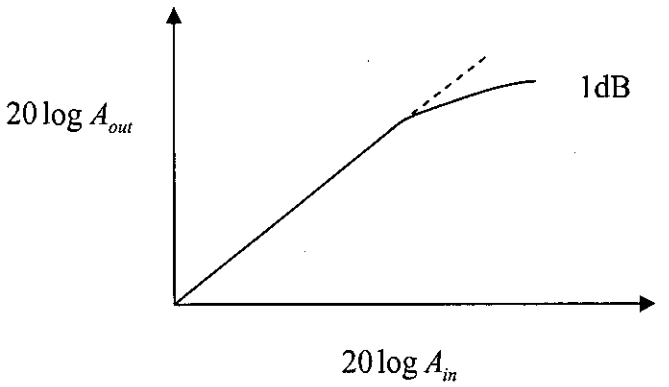

Figure 7: 1dB Compression Point

2.5.2.2 3rd Order Intercept Point (IIP3)

It is a theoretical point at which the fundamental and third order response intercepts. This point is found when two signals that are very close in frequency are applied to the mixer as shown in Figure 8. Suppose the input power level at f_1 is the same as at f_2. The IIP3 is defined as the intercept point of the extrapolated line of

output power at frequency $f_{lo} - (2_{f2} - f_1)$ versus extrapolated line of the linear output $f_{lo} - f_1$ [4]. 1dB compression point is about 9.66dBm below the intercept point of IIP3, thus equation (5) states

IIP3 = 1dB compression point (in dBm) + 9.66dBm (5)

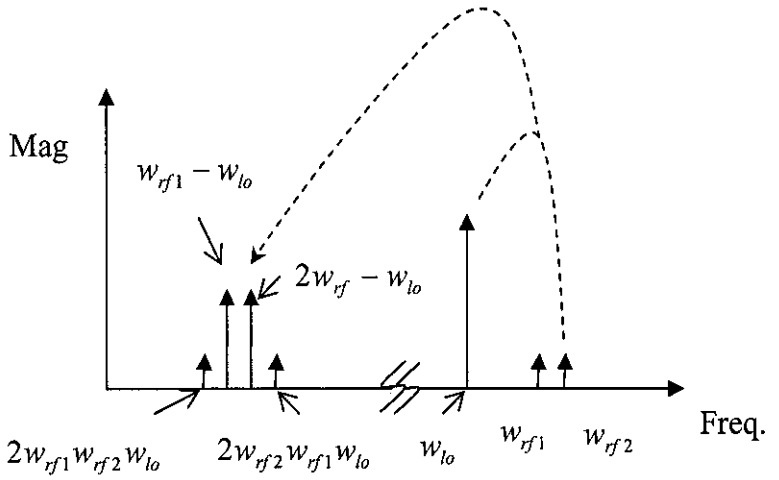

Figure 8: Frequency Spectrum of Two Tones Test of Mixer

2.5.3 Noise Figure

Noise Figure (NF) calculates how much the SNR of a signal degrades because of the added noise as it passes through the mixer. The NF of the mixer is defined as the ratio of total SNR of the RF signal to the total SNR of IF signal [3] as in equation (6).

$$NF(dB) = 10\log\left(\frac{SNR_{in}}{SNR_{out}}\right) \quad (6)$$

2.6 Mixer Topologies

Passive mixers have higher linearity and better frequency response but they do not have any gain thus are not widely used in RF systems. On the other hand, active mixers have gain hence reducing noise contributed by the succeeding stages [4]. There are five types of active mixer topologies available as follow:

2.6.1 Single-Balanced Design

This design is the simplest approach that can be implemented in most semiconductor processes. It offers a desired single-ended RF input for ease of application as it does not require a balun transformer at the input [4]. It also has moderate gain and low noise figure. This topology is as presented in Figure 9.

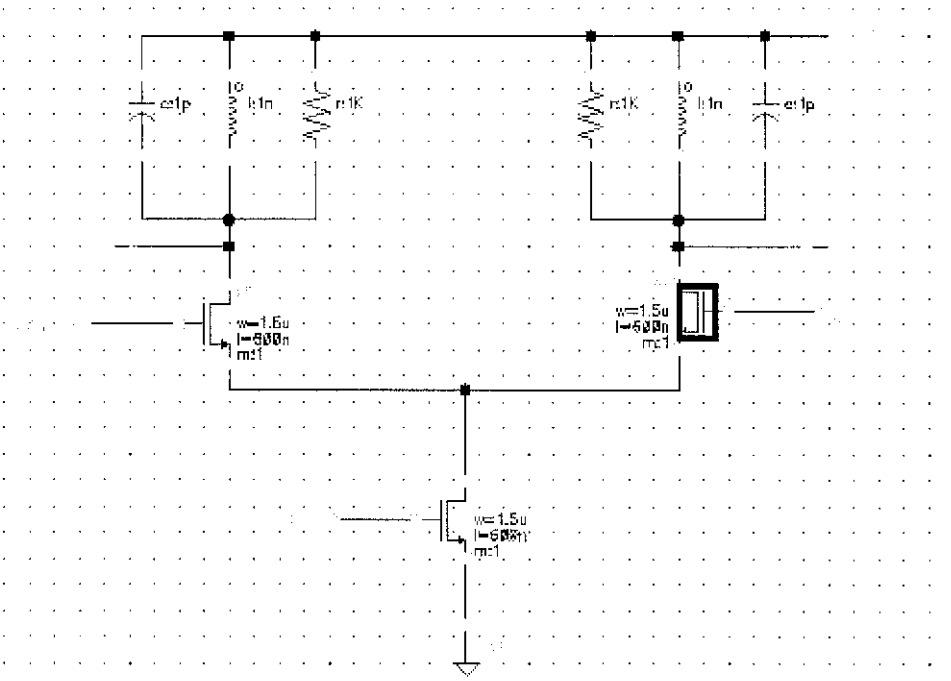

Figure 9: Schematic of a Single-Balanced Design Mixer

2.6.2 Gilbert Cell with Differential Inputs

The double balanced or Gilbert mixer as in Figure 10 is most desirable for high port to port isolation and spurious output rejection applications and it can provide high gain and very low noise figure [4]. A balun transformer is needed to convert the single-ended input to a differential signal for a mixer.

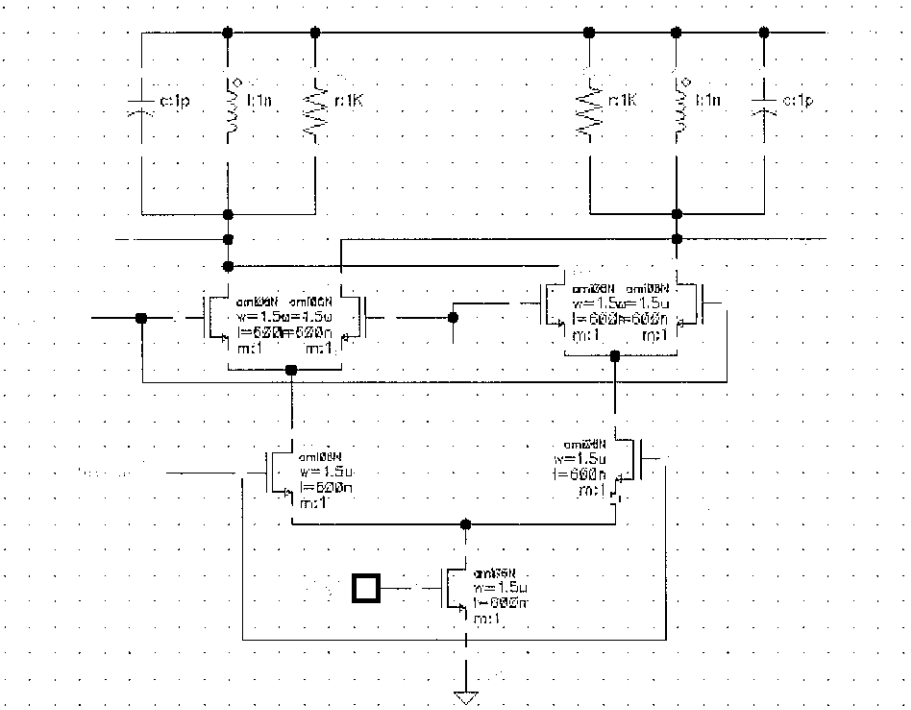

Figure 10: Schematic of a Gilbert Cell with Differential Inputs

2.6.3 Gilbert Cell with Single-Ended Inputs

To eliminate the balun transformer, the Gilbert Cell can be driven single ended with one side ac-grounded as in Figure 11. It exhibits similar performance to its differential counterpart except that it has lower dynamic range [4].

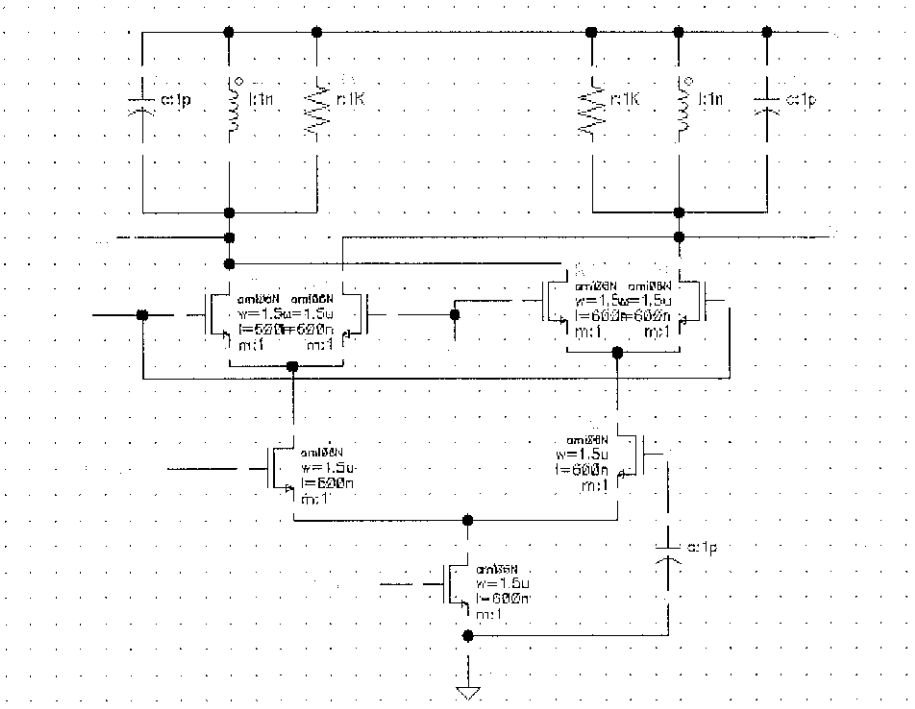

Figure 11: Schematic of a Gilbert Cell with Single-Ended Inputs

2.6.4 Micromizer

Micromizer as presented in Figure 12 offers the best input IP3 due to its third-order harmonic distortion cancellation mechanism. However, using this topology it would be difficult to reduce the noise figure or to increase the gain as the input is fed into the emitter of the transistor [4]. The balun transformer can be eliminated by using a current mirror.

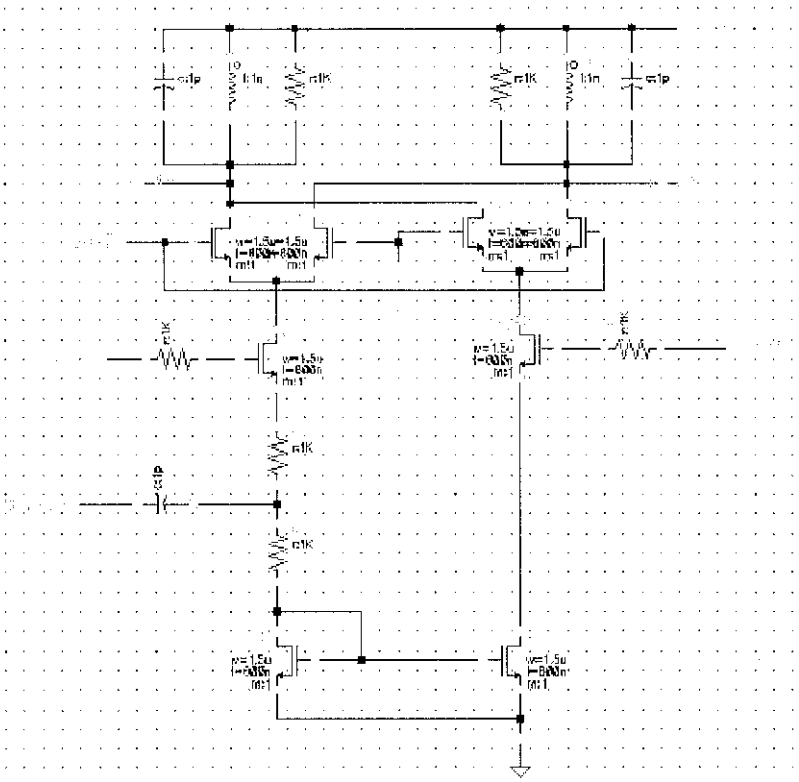

Figure 12: Schematic of a Micromizer

2.6.5 Common Gate-Common Source (CG-CS) Mixer

This mixer as in Figure 13 consists of two input transistors and four switching transistors. One transistor is operated in common-gate configuration while the other is operated in common-source configuration. Single to differential conversion is thus realized with the CG-CS configuration as the outputs of the two input transistors are equal but 180 degree out of phase [4]. Due to the balanced nature of the two outputs, port to port isolation and spurious output rejection are preserved. The design has high IP3 with modest noise figure [4].

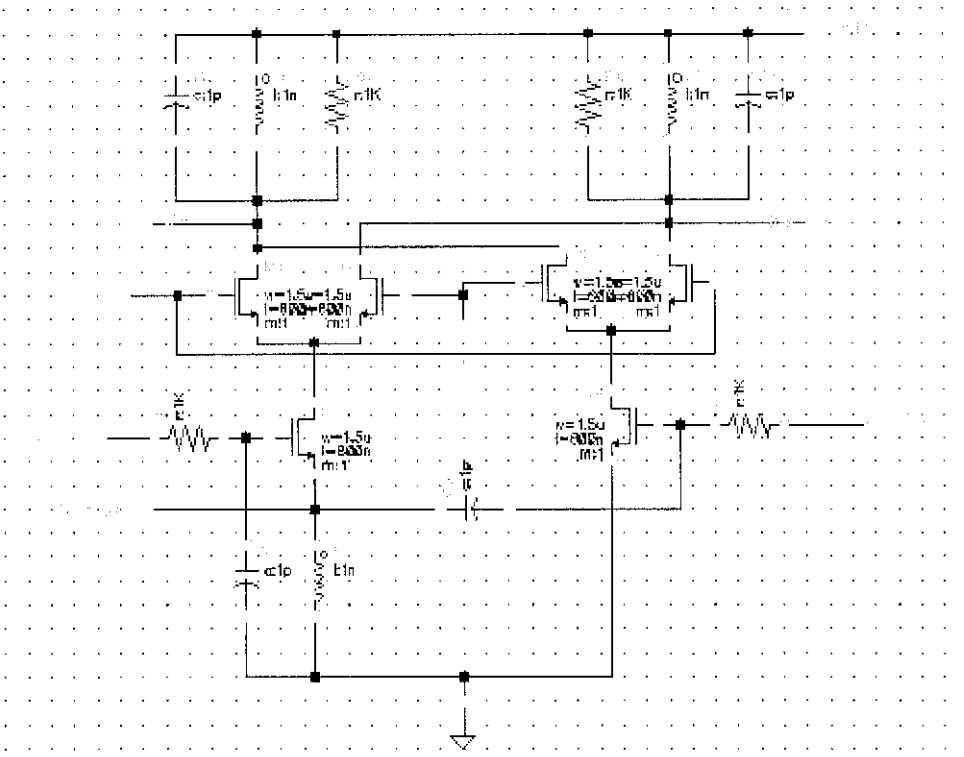

Figure 13: Schematic of a Common-Gate Common-Source Mixer

2.7 Mixer Design Characteristic

In the designing process, it is essential that we have a deep understanding on how the mixer works. There are several characteristics of mixer that need to be studied in order to design a good mixer with high gain and linearity.

2.7.1 Single Balanced vs Double Balanced Mixer

The basic schematic of a single balanced mixer is as shown in Figure 14. The mixer consists of two parts; one is RF current generation by using M1 while the other is switching action by using M2 and M3. The output will be the multiplication of the RF and the LO signal. The drawback is that LO signal appears as a component of the IF output spectrum due to the bias current [3].

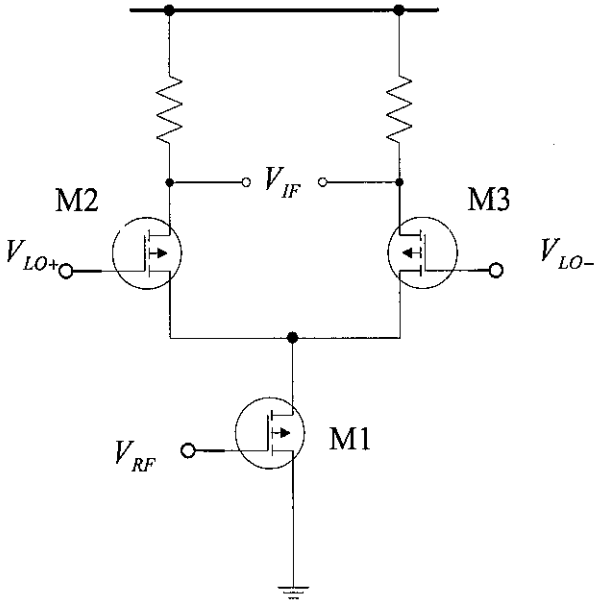

Figure 14: Schematic of Single Balance Mixer

To remove the LO signal from the output, double balance mixers are used as shown in Figure 15. Another multiplier cell is added compared to the single balance mixer so that the DC bias current at the output is cancelled if the transistors are perfectly matched.

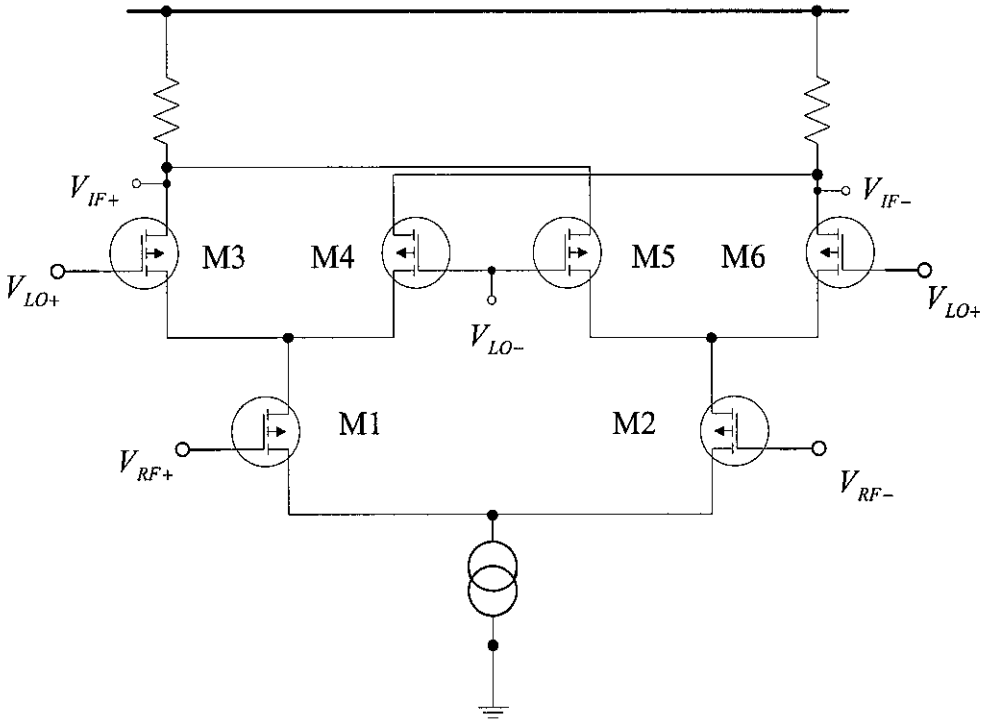

Figure 15: Schematic of Double Balance Mixer

2.7.2 MOS Behavior

All transistors are operated in the saturation region as shown in Figure 16. This is due to this region offers the largest gain and makes the current less susceptible to changing voltage across the transistors [1]. Equation (7) shows the simplified model of signal current for MOSFET is saturation operation. The transconductance, g_m of the device is dependent on $\frac{W}{L}$ and V_{gs} as shown in equation (8).

$$I_{DS} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2 \qquad (7)$$

$$g_m = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t) \qquad (8)$$

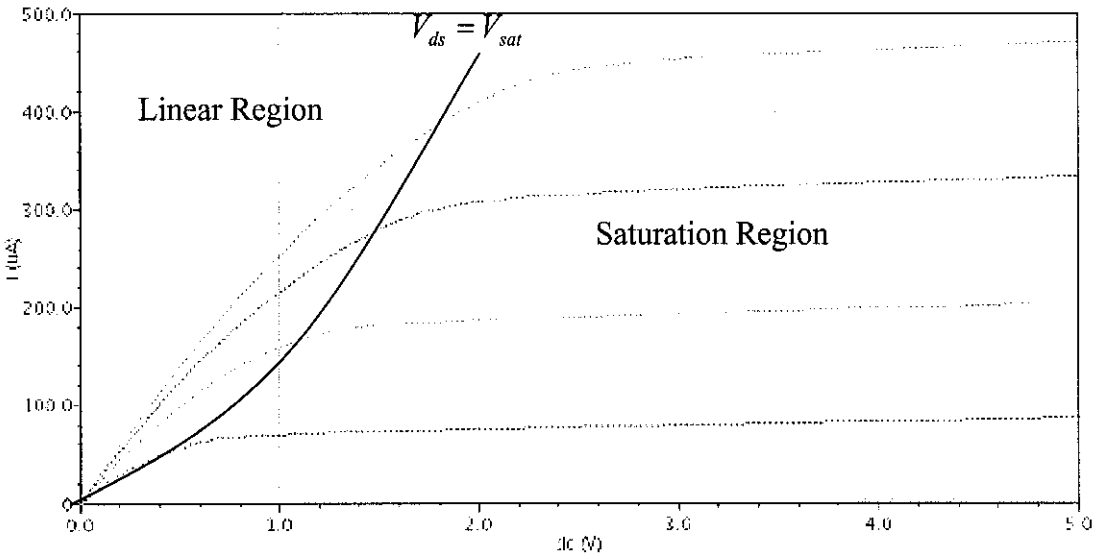

Figure 16: I_{ds} vs V_{ds} Plot showing the Different Regions of Operation

2.7.3 Switching Stage

When LO voltage level is too small, the output voltage is dependent on the LO level, which means gain will be larger for larger LO due to output voltage will be insensitive to the LO amplitude. Noise is also minimized for larger LO. However, if LO is too large, it will lead to spikes in the signals hence reducing switching speeds and may cause the transistors to leave the saturation region.

CHAPTER 3
METHODOLOGY

3.0 Introduction

In the previous chapter, Gilbert Cell mixer was proposed to be the best topology out of five other different common topologies of mixer due to its properties of providing high gain and low noise figure. This topology will be used as the primary reference through out the project. It shall be designed; later simulated using Cadence, SPECTRE and its performance shall be analyzed. Figure 17 represents the flow chart of project.

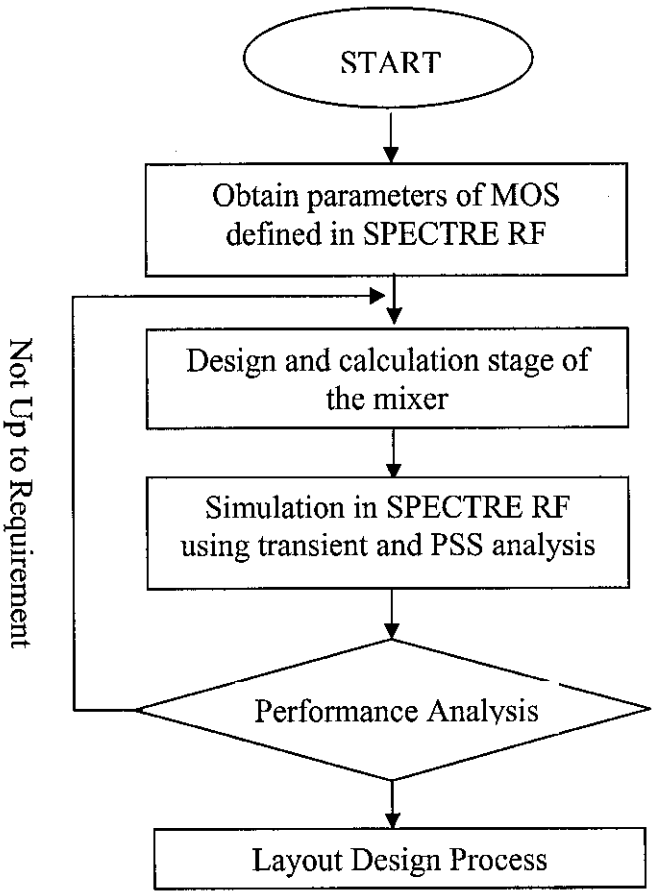

Figure 17: Flow Chart of Project

3.1 Design Approach

The model file used in the design in Cadence, SPECTRE is the 'ami06N.m' (refer to Appendix 1) and the model parameters of the NMOS are summarized as in Table 1.

Table 1: Model parameters of NMOS

μ_0	$533.695cm^2/Vs$
t_{ox}	1.41×10^{-8}
V_{th}	$0.7086V$

Based on the model parameters, the K_n is calculated as follow:

$$\mu_n = \mu_o = 533.695cm^2/Vs = 533.695\times10^8\,\mu m^2/Vs \tag{13}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.45\times10^{-11}}{1.41\times10^{-8}} = 2.447\times10^{-3}F/m^2 = 2.447\times10^{-15}F/\mu m^2 \tag{14}$$

$$K_n = \mu_n C_{ox} = 533.695\times10^8\,\mu m^2/V\times2.447\times10^{-15}F/\mu m = 130.595\mu A/V^2 \tag{15}$$

A current sink of $I_{ss} = 6\ mA$ was chosen to drive the mixer. Therefore $3\ mA$ of current is split between the differential pair. To preserve headroom, R_s was chosen such that there's only 0.1 V voltage drop across the resistor. To prevent compression at the IF signal, a voltage of 2.5 V was decided on the IF. Therefore,

$$R_s = \frac{V}{I} = \frac{0.1V}{3mA} = 33\Omega \tag{16}$$

$$R_L = \frac{V_{DD} - V_D}{I} = \frac{3.3V - 2.5V}{3mA} = 266.7\Omega \tag{17}$$

3.1.1 RF Stage

The gain is proportional to the transconductance of the RF pairs.

Gain = 5dB = 1.82 V/V

$$g_m{}^2 = 2\mu_n C_{ox}\frac{W}{L}I_{DS} \tag{18}$$

$$g_m = \left[\frac{2}{\pi}\frac{R_L}{Gain} - R_s\right]^{-1} = 16.6m\Omega \tag{19}$$

$$W_{1,2} = \frac{g_m{}^2 L}{2\mu_n C_{ox} I_{ds}} = \frac{(16.6m)^2 0.15\mu m}{2(130.595\mu)3mA} = 52.75\mu m \tag{20}$$

The chosen overdrive voltage $(V_{gs} - V_t)$ was 300 mV

Therefore,

$$V_g = V_s + V_t + 300\ mV = 0.5 + 0.7 + 0.3 = 1.5\ V \tag{21}$$

Let,

$$\begin{aligned} V_{ds} &= V_{gs} + 1 = 1.3V \\ V_{gs} &= V_g - V_s \\ V_{ds} &= V_d - V_s = 1.3 + 0.5 = 1.8V \end{aligned} \tag{22}$$

3.1.2 LO Stage

For proper switching, V_{gs} needed to be just slightly larger than V_t while W needs to be large. V_{gs} was chosen to be 0.8 V.

$$W = \frac{2LI_{ds}}{K_n(V_{gs} - V_t)^2} = \frac{2(150\eta m)(3mA)}{(130.595\mu)(0.8V - 0.7086V)^2} = 824.9\mu m \tag{23}$$

$$V_g = V_{gs} + V_s = 0.8 + 1.8 = 2.6V \tag{24}$$

3.1.3 Current Sinks

A large current consumption will be used for this design of CMOS Mixer. Therefore, if a MOS must drive a large current, its width would have to be very large making fabrication unrealizable. Therefore, two current sinks were used to provide these currents instead of only one as in Figure 18. The degeneration resistor R_s was connected between the two current sinks to improve linearity.

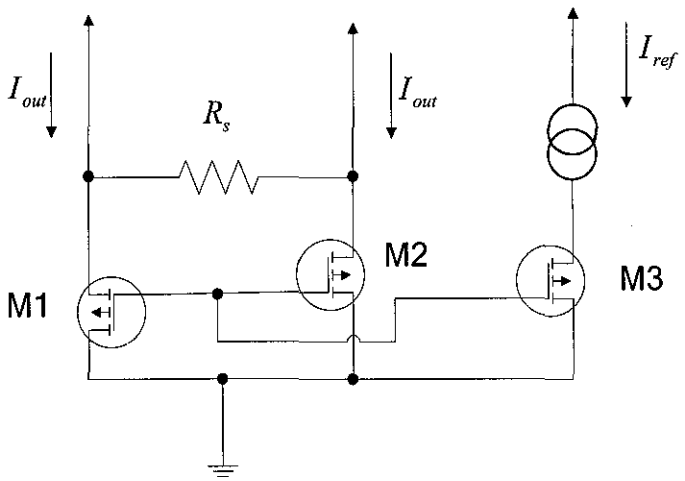

Figure 18: Two Current Sinks Circuit

$V_{ds} = 0.4\,\text{V}$ and current used is $I_{ss} = 6\ mA$. To keep r_0 high, $L_{7,8} = 540\eta m$.

$$V_{gs} = V_{ds7} = V_{gs8} = V_{th} + 300\ mV = 1.0086\ V \tag{25}$$

A small current of 100 μA was chosen for the reference current, I_{ref}.

$$W_8 = \frac{2LI_{ss}}{K_n(V_{gs8} - V_t)^2} = \frac{2(600\eta m)(3mA)}{(130.595\mu)(1.0086V - 0.7086V)^2} = 306.3\mu m \tag{26}$$

Since $L_8 = L_7$ and $\frac{I_{out}}{I_{ref}} = \frac{W_8}{W_7}$

$$W_7 = \frac{W_8 I_{ref}}{I_{ss}} = \frac{306.3\mu m \times 100\mu A}{6mA} = 5.105\mu m \tag{27}$$

3.2 Circuit Schematic

The finalized Gilbert Cell mixer schematic is as shown in Figure 19. The parameters calculated for the design is presented in Table 2.

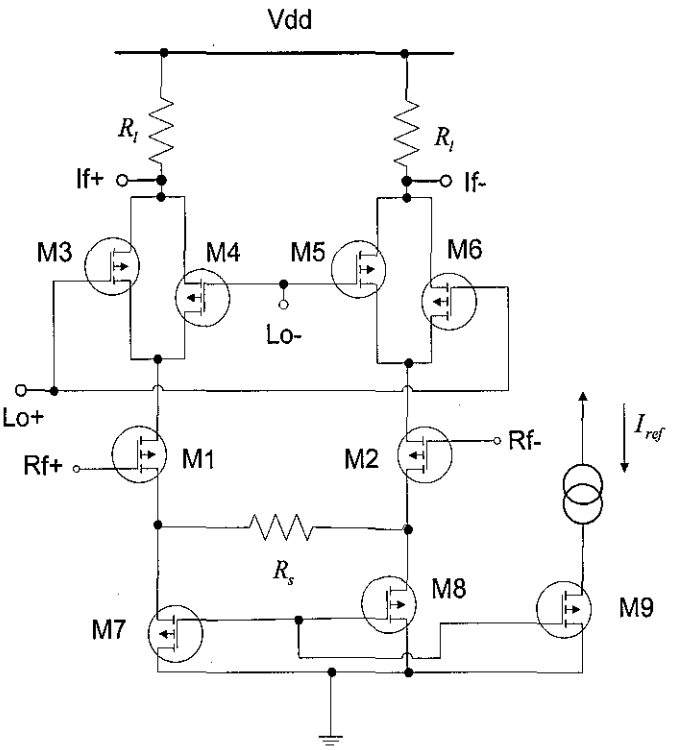

Figure 19: Finalized Gilbert Cell Mixer

Table 2: Values from the Calculation for Schematic

Parameters	Values
M1 (W)	52.8μm
M2 (W)	52.8μm
M3 (W)	824.9μm
M4 (W)	824.9μm
M5 (W)	824.9μm
M6 (W)	824.9μm
M7 (W)	306.3μm
M8 (W)	306.3μm
M9 (W)	5.105μm
R_s	33 Ω
R_l	266.7 Ω
R (current mirror)	33 $k\Omega$

CHAPTER 4
RESULT AND DISCUSSION

4.0 Schematic Simulation

The presented mixer schematic is simulated using Cadence, SPECTRE as shown in Figure 20. The applied signals of RF and LO signal is supplied from the oscillator circuits as shown in Figure 21.

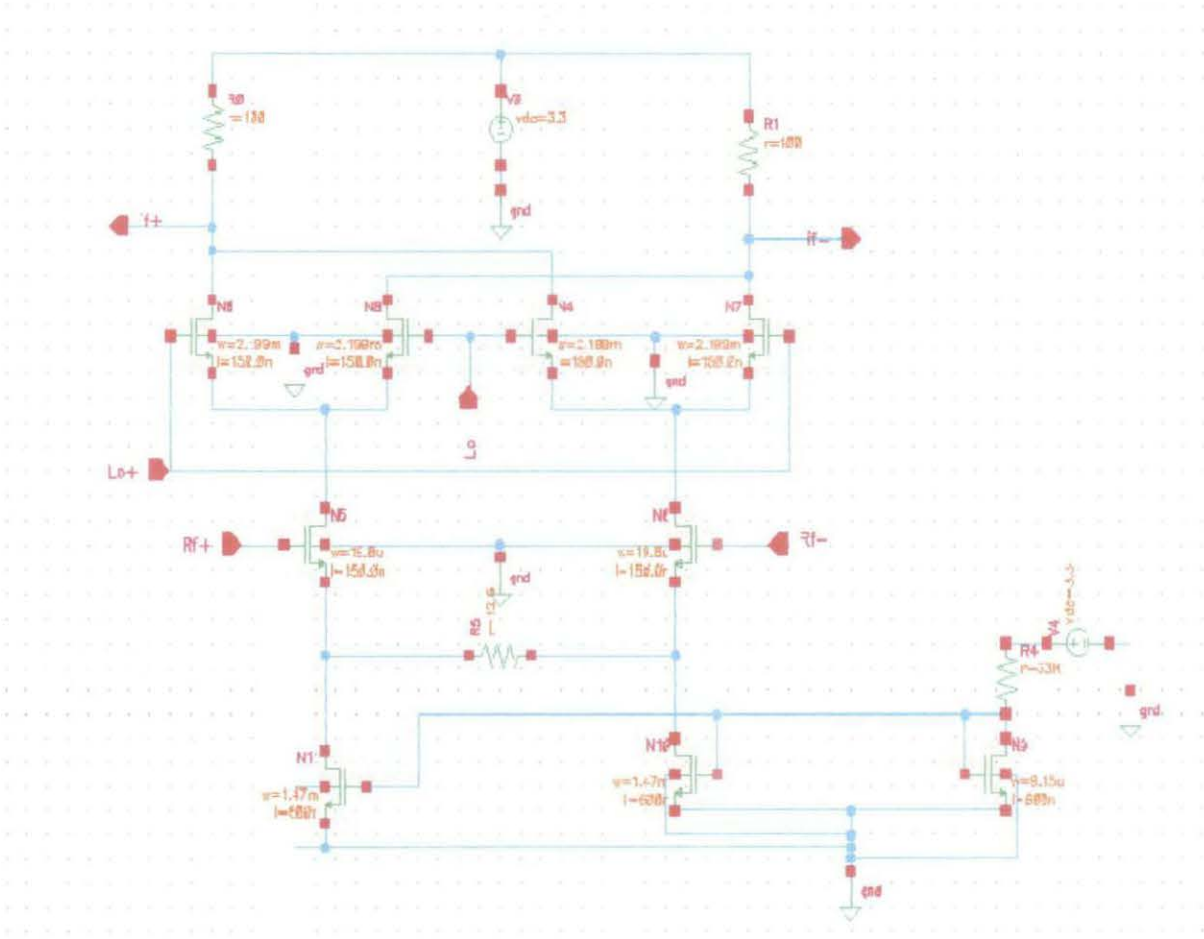

Figure 20: The Gilbert Mixer Schematic View

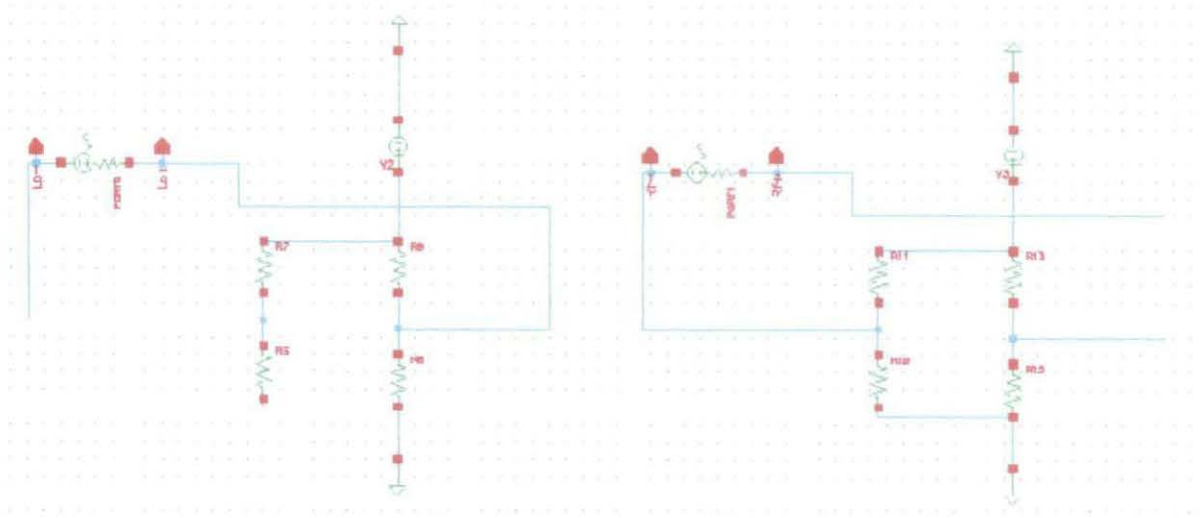

Figure 21: The Oscillator Circuit for RF and LO Signal

4.1 Transient Analysis

The transient simulation was used to find the transient response of the circuit when the input signals; RF and LO signal are applied to the mixer. When the RF and LO signals are mixed, the output result is a signal at the IF output located at 72 MHz. Figure 22 and Figure 23 show the time varying input signals of the RF and LO signal while Figure 24 shows the multiplied signal of IF signals as the outcome of the mixing.

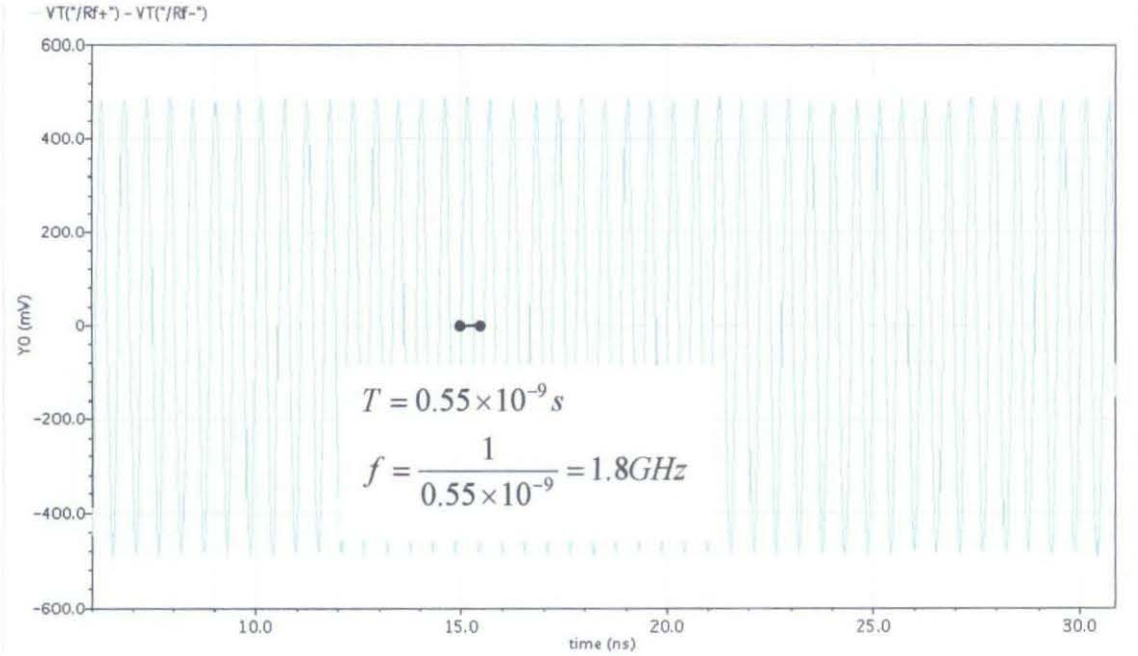

Figure 22: The Radio Frequency (RF) Signal located at 1.8 GHz

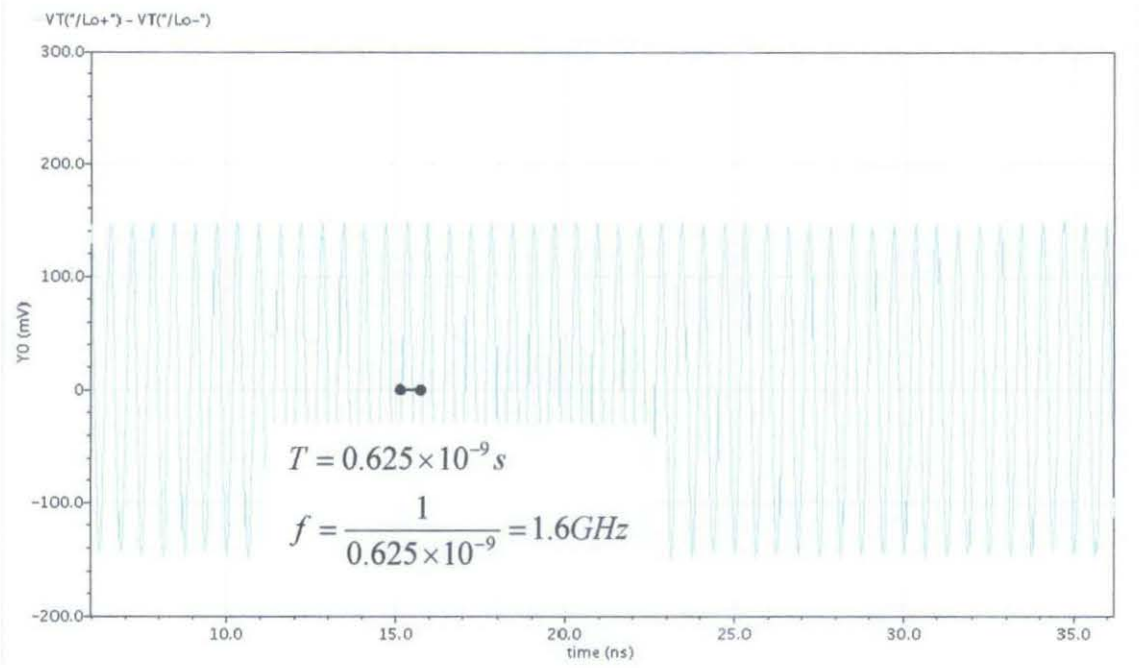

Figure 23: The Local Oscillator (LO) Signal located at 1.6 GHz

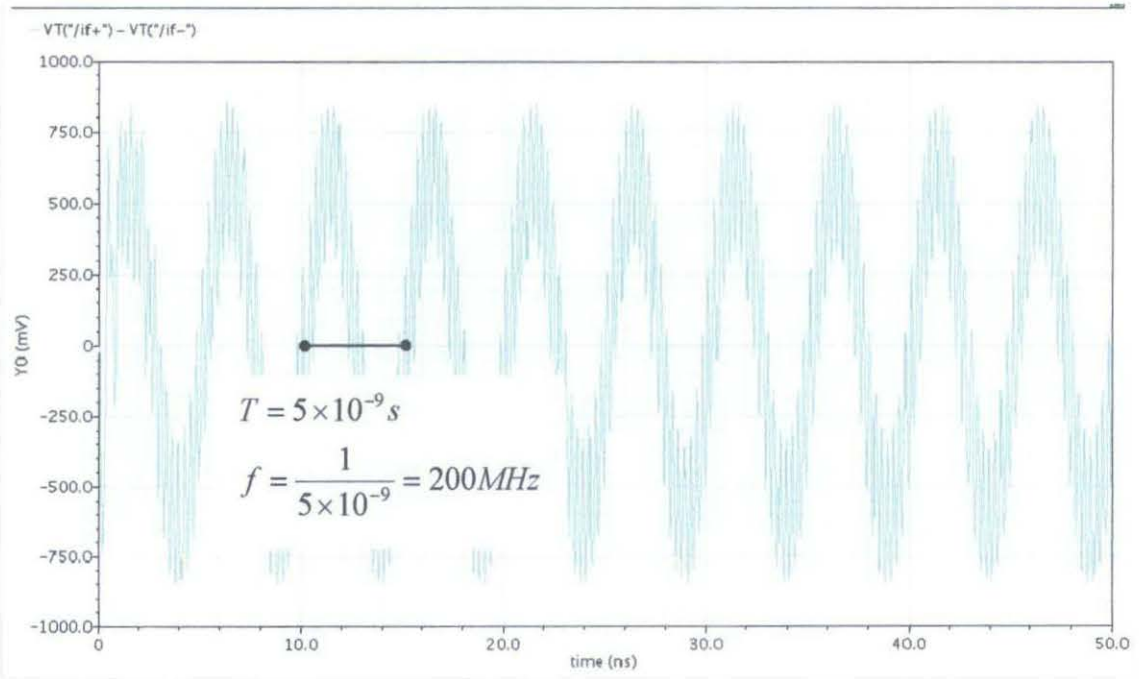

Figure 24: The Intermediate Frequency (IF) Signal located at 200 MHz

4.2 Voltage Conversion Gain

The voltage conversion gain of the Gilbert mixer was determined using Cadence, SPECTRE through Periodic Steady State (PSS) Analysis. It is the difference between the input and output power. Figure 25 shows the screenshot of the voltage conversion gain in PSS simulation for *6 mA*. Table 3 shows the conversion gain for different current consumptions for the mixer with two current mirrors.

The bias voltage (V_d of LO Stage) is determined by the resistor load R_l, the supply voltage and the bias current assuming matched pairs, as $V_d = V_{DD} - I_{bias}R_l$. As a consequence, the saturation mode of a MOS is varied by varying V_d and I_{bias}. This region of mode offers the largest gain as in VCG. The larger the current will be, the slower it will get to reach the saturation region; thus the lower the gain.

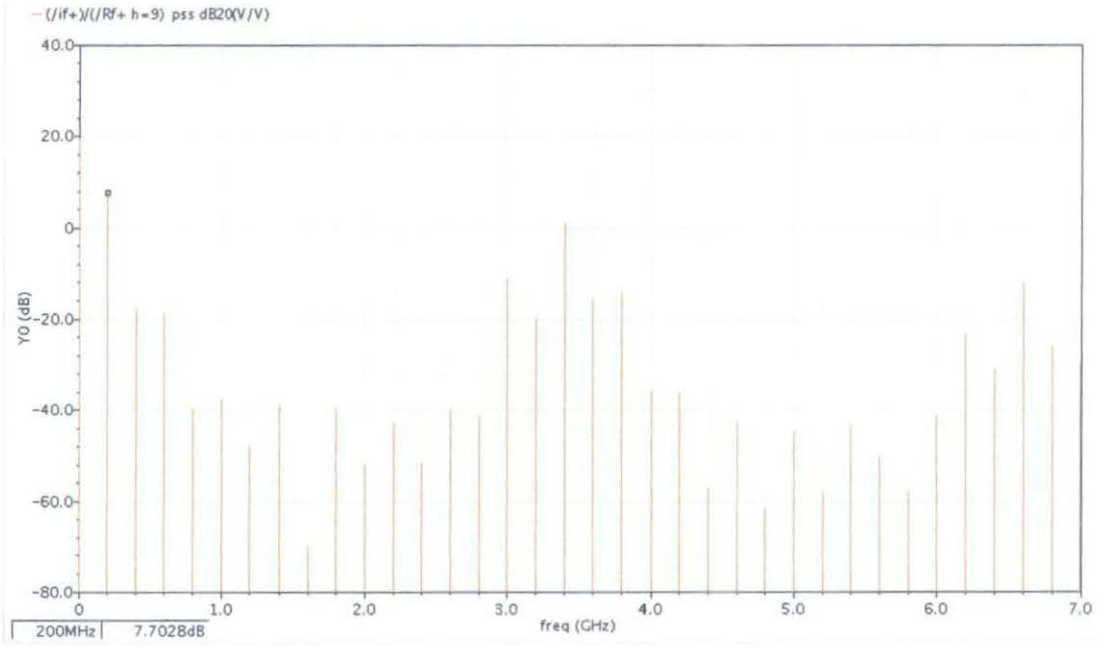

Figure 25: Voltage Conversion Gain in PSS Simulation for *6 mA*

Table 3: Voltage Conversion Gain (dB) for Different Currents

Currents	Voltage Conversion Gain
6 mA	7.703dB
10 mA	5.828dB
16 mA	2.240dB

4.3 The 1dB Compression Point

This 1dB compression gain is used to compute and find the linearity of the mixer. This analysis is a part in the Periodic Steady State (PSS) analysis. To find the 1dB compression, the input RF power was swept for a certain power range. Figure 26 shows the screenshot of the 1dB compression point in PSS simulation for *6 mA*. Table 4 shows the summary of the 1dB compression point for different current consumptions.

Improvement in the linearity may worsen the gain of the mixer and vice versa. Therefore as current is increased, gain is decreased but with increasing in linearity.

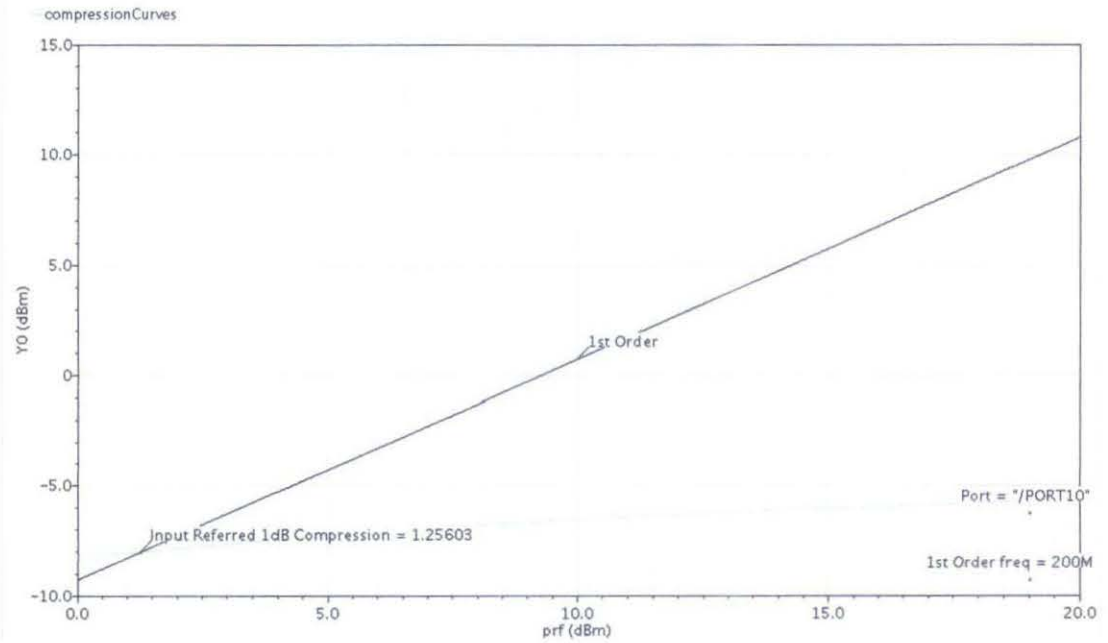

Figure 26: 1dB Compression Point in PSS Simulation for *6 mA*

Table 4: 1dB Compression Point (dBm) for Different Currents

Currents	1dB Compression Point
6 mA	1.256dBm
10 mA	1.983dBm
16 mA	5.141dBm

4.4 The Input 3rd Order Intercept Point (IIP3)

This analysis is also analyzed the linearity of the mixer circuit. To simulate for the IIP3, two signals were supplied to the mixer and the power of the signals were swept for the same range as for 1dB compression point plot. The simulation's summary is as shown in Table 5.

IIP3 has direct relationship to 1dB Compression Point as in equation (5). As 1dB Compression is increased as consequence of increasing the current, the IIP3 will increase as well.

IIP3 = 1dB compression point (in dBm) + 9.66dBm

Table 5: 3rd Order Intercept Point (IIP3) for Different Currents

Currents	3rd Order Intercept Point
6 mA	10.916dBm
10 mA	11.643dBm
16 mA	14.801dBm

4.5 PNOISE Analysis

The PNOISE analysis computes for the total noise at the output which includes contributions from the input source signals as well the output load. This analysis is used together with PSS analysis to determine the mixer's single sided Noise Figure (NF). This also includes the effects of aliasing, folding and during the conversion gain stage. Figure 27 shows the screenshot of the PNOISE analysis for *6 mA*. The noise Figure (NF) of the mixer is tabulated in Table 6 for different current consumptions.

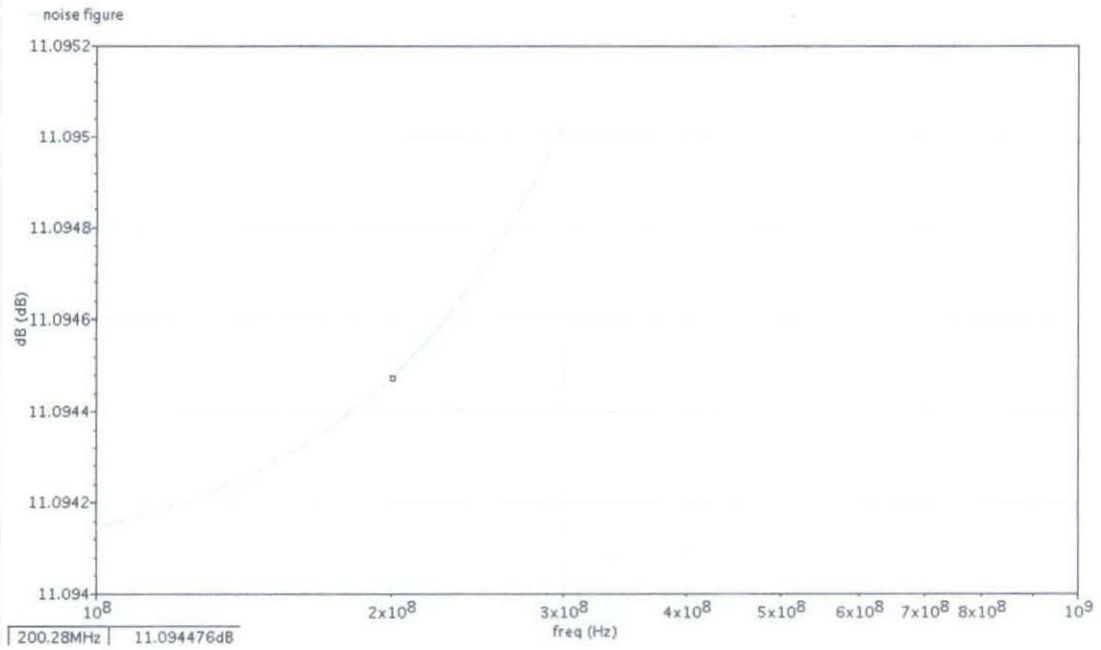

Figure 27: Noise Figure in PNOISE analysis for *6 mA*

Table 6: Noise Figure (dB) for Different Currents

Currents	**Noise Figure (NF)**
6 mA	11.094dB
10 mA	11.953dB
16 mA	14.243dB

CHAPTER 5
CONCLUSION AND RECOMMENDATION

5.0 Conclusion and Recommendation

The Differential Gilbert Cell mixer is designed for the application of GSM wireless communication. The RF signal of 1.8 GHz which is a typical specification for mobile phones technology is down converted to a desired signal of 200 MHz. Even though, there is a breakthrough in the current wireless technology with the introduction of WiFi communication which utilized up to 5 GHz frequency or more, the mixer still undeniably can cope with the significant input signal frequency. This is due to the breakthrough in the fabrication technology of microchip, to be exact in the CMOS technology. Lately, with decrease in channel length, the maximum usable frequency of MOS has also gone higher [2].

The design of the mixer was done using models pre-defined by the author in the Cadence Design Environment. Again, the design mixer simulation met all the requirement specifications with an exception to the linearity performance. By increasing the current supplied through the mixer; the linearity can be improved although it may double up the total power consumption and reduce the gain. Though, there is still limit of current that can be supplied to the mixer without damaging any of the electronic components. Too high current leads to high noise at the output, thus reduce the gain which simply the ratio of output over input.

The author starts the project with limited knowledge on the analogue electronic field. However, as the understanding of the knowledge of CMOS mixer design increased through researches and some trial errors, progress in this project was definitely made faster. Lots of knowledge on the integrated analogue are gained and learnt. Undeniably, future work shall be done in much shorter time and with full confident.

5.1 Future Work

Some design modifications shall be made to improve the linearity performance of the mixer. Linearity is by far an issue which needs to be tackled in the future while maintaining the gain of the mixer. There is a give and take between linearity and conversion gain, while improving one may worsen the other. Since mixer is usually connected to a low noise amplifier (LNA) in a transceiver, therefore other performance of the mixer can be sacrificed for the sake of improving the linearity as it must handle the power that produced by the LNA. The source degeneration resistor can be increased to improve linearity but it is to be reminded again that it may reduce the total gain performance of the mixer. Since the total current usage is by far too low compared to the design requirement and in addition to the fact that current consumption is no longer a big issue, therefore more currents can be utilized to drive the mixer improving the linearity.

For the future work, the other mixer design topologies shall be designed and simulated in Cadence, SPECTRE. The performances of each of the topologies shall be compared and analysed. This will again confirm the first assumption made during the designing stage which Differential Gilbert Cell mixer is the best topology available in term of performance.

The layout of the mixer shall be designed and simulate against the schematic. Proper layout design rules shall be incorporated during the layout process. These can be done using Design Rules Check (DRC) validation before going for Layout Versus Schematic (LVS) simulation. The area used for the whole layout process should be as minimum as possible and efficient as well.

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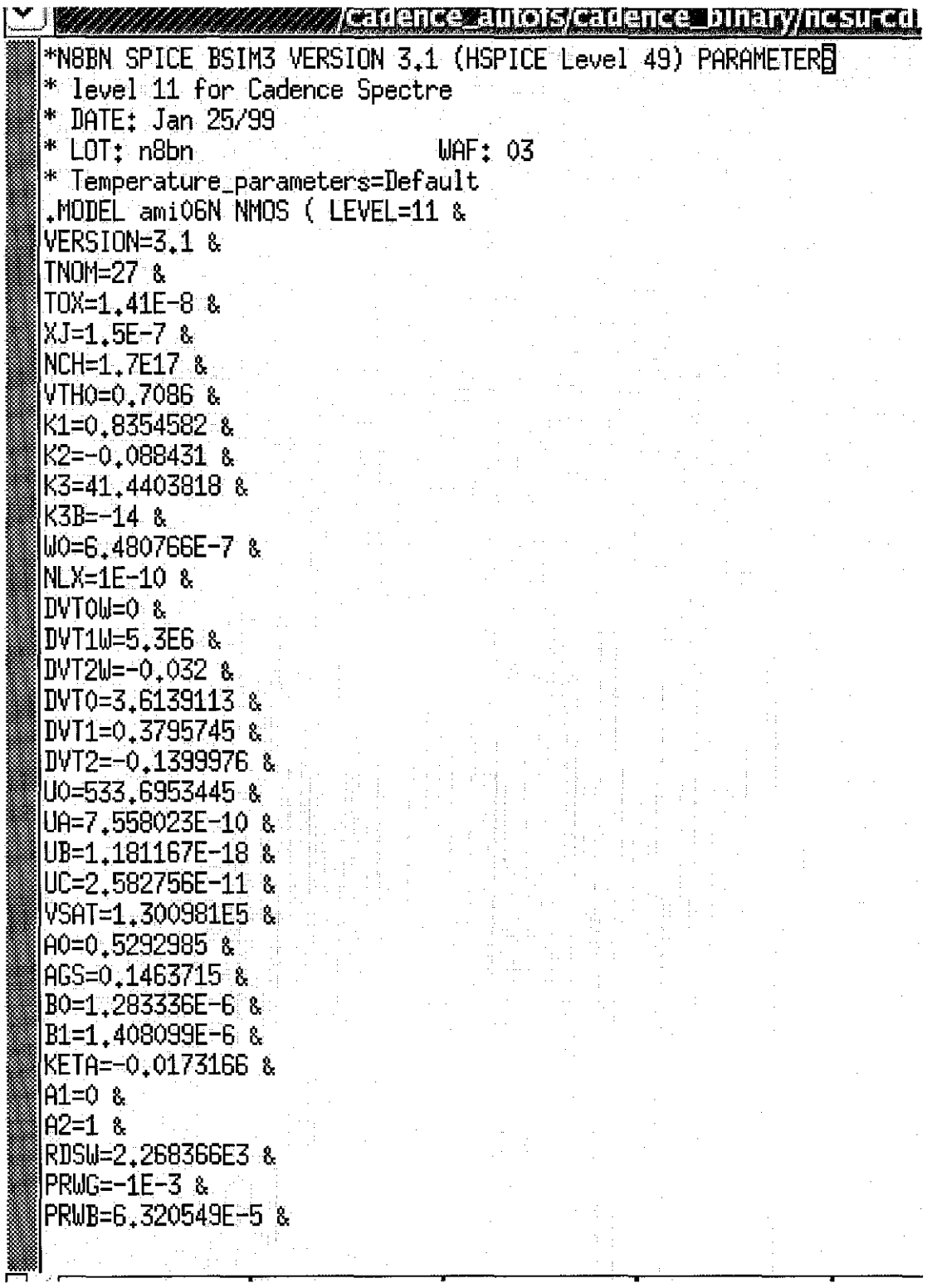
APPENDICES

Appendix 1



```
*N8BN SPICE BSIM3 VERSION 3.1 (HSPICE Level 49) PARAMETERS
* level 11 for Cadence Spectre
* DATE: Jan 25/99
* LOT: n8bn                    WAF: 03
* Temperature_parameters=Default
.MODEL ami06N NMOS ( LEVEL=11 &
VERSION=3.1 &
TNOM=27 &
TOX=1.41E-8 &
XJ=1.5E-7 &
NCH=1.7E17 &
VTH0=0.7086 &
K1=0.8354582 &
K2=-0.088431 &
K3=41.4403818 &
K3B=-14 &
W0=6.480766E-7 &
NLX=1E-10 &
DVT0W=0 &
DVT1W=5.3E6 &
DVT2W=-0.032 &
DVT0=3.6139113 &
DVT1=0.3795745 &
DVT2=-0.1399976 &
U0=533.6953445 &
UA=7.558023E-10 &
UB=1.181167E-18 &
UC=2.582756E-11 &
VSAT=1.300981E5 &
A0=0.5292985 &
AGS=0.1463715 &
B0=1.283336E-6 &
B1=1.408099E-6 &
KETA=-0.0173166 &
A1=0 &
A2=1 &
RDSW=2.268366E3 &
PRWG=-1E-3 &
PRWB=6.320549E-5 &
```

```
WR=1 &
WINT=2.043512E-7 &
LINT=3.034496E-8 &
XL=0 &
XW=0 &
DWG=-1.446149E-8 &
DWB=2.077539E-8 &
VOFF=-0.1137226 &
NFACTOR=1.2880596 &
CIT=0 &
CDSC=1.506004E-4 &
CDSCD=0 &
CDSCB=0 &
ETA0=3.815372E-4 &
ETAB=-1.029178E-3 &
DSUB=2.173055E-4 &
PCLM=0.6171774 &
PDIBLC1=0.185986 &
PDIBLC2=3.473187E-3 &
PDIBLCB=-1E-3 &
DROUT=0.4037723 &
PSCBE1=5.998012E9 &
PSCBE2=3.788068E-8 &
PVAG=0.012927 &
DELTA=0.01 &
MOBMOD=1 &
PRT=0 &
UTE=-1.5 &
KT1=-0.11 &
KT1L=0 &
KT2=0.022 &
UA1=4.31E-9 &
UB1=-7.61E-18 &
UC1=-5.6E-11 &
AT=3.3E4 &
WL=0 &
WLN=1 &
WW=0 &
WWN=1 &
```