COMPARATIVE STUDY OF COOLMOS AND MOSFET FOR HIGH FREQUENCY INVERTER DESIGN

By

NUR ALINA JELANI

Submitted to the Electrical & Electronics Engineering Programme
in Partial Fulfillment of the Requirements
for the Degree
Bachelor of Engineering (Hons)
(Electrical & Electronics Engineering)

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CERTIFICATION OF APPROVAL

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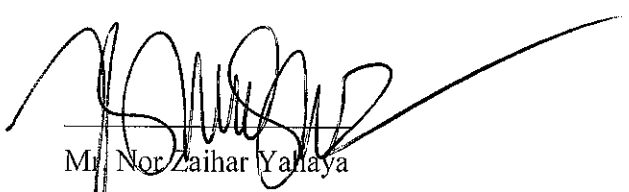
Approved:



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TRONOH, PERAK

December 2005

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

Nur Alina Jelani

ABSTRACT

In this paper, comparative study of MOSFET and COOLMOS in a high frequency inverter design is investigated. Recently, semiconductor power switch need greater efficiency with low switching energy losses. The study is performed using a single phase full bridge inverter design with a high frequency of 500 kHz, 150V input voltage, 0.5 duty ratio with an isolation at the load in providing a stable AC output catering for Uninterruptible Power Supply (UPS) system. MOSFET is widely use; COOLMOS is a new technology of MOSFET family using a new device concept called super-junction. Thus, will COOLMOS replace the traditional device MOSFET in high frequency inverter design for UPS application is to investigate. This project is carried out via simulations using Pspice Cadence PSD 14.2 software and via experimentation on Printed Circuit Board (PCB) layout. PCB layouts are designed using Multisim and Ultiboard 2001 software. Simulation and experimentation investigation shows COOLMOS having a superior performance with switching energy losses are reduced up to more than 50% compared to MOSFET. Verifying COOLMOS can replace the traditional device MOSFET in high frequency inverter design for UPS application to meet the need greater efficiency power switches with low switching energy losses.

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LIST OF ABBREVIATIONS

List of abbreviations used are as follows:

AC	Alternating Current
A/D	Analog to Digital
BJT	Bipolar Junction Transistor
COOLMOS	Cool Metal Oxide Semiconductor
D	Duty Ratio
DC	Direct Current
E	Switching Energy Losses
f	Frequency
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
S	Semiconductor Switch
UPS	Uninterruptible Power Supply
VSI	Voltage-Source inverter

CHAPTER 1
INTRODUCTION

1.1 Background of Study

Single-phase full-bridge high-frequency inverter is among the important parts in UPS system. In a voltage-source inverter (VSI) constant input 150V is used to comply with high rated voltage for UPS appliance. In this VSI design the output voltage; V_o is a function of inverter operation, meanwhile the load current I_o, is a function of the nature of the load. With this, the circuit is to generate a stable Alternating Current (AC) output of fifty percent (50%) duty cycle. This duty cycle is to obtain an equal proportion of positive and negative cycle at the output waveform. The expected output power is approximately 300W for high power UPS application in an uncontrollable isolated inverter.

This project are performed by two students with a high frequency inverter circuit is used as medium to compare the performances between two different power semiconductor devices as switches; MOSFET and COOLMOS. Here, the author focuses on investigating MOSFET as power switch. A high-frequency inverter design is referring to frequency of higher than 100 kHz. Specifically, a frequency of 500 kHz is selected, as to eliminate noise and distortion at the produced AC output. The performance comparison of these power semiconductor devices acting as power switches is investigated. MOSFET is an interesting device use in many high frequency and lower power converter applications. This kind of device is easy to drive, easy to parallel and switches fast. Recently, a new type of power MOSFET called super junction MOSFET (COOLMOS) was recently introduced [1]. In this project, the most efficient switches in inverter circuit for UPS application producing low switching losses are concluded between MOSFET and COOLMOS.

1.2 Problem Statement

Adequate power system reliability is essential as small disturbances in the main electricity supply can cause great damage. Power problems also can cause unplanned shutdowns and data losses. All these cost a considerable amount of money. A recent Power Quality Study revealed that the average computer system is subjected to 289 potentially damaging power disturbances per year [2]. Thus, one of the best solutions to avoid this problem is to provide the system with highly reliable and efficient UPS which will maintain a steady supply of power irrespective of the mains supply quality.

In the UPS systems focus on the inverter circuit design determining a high efficiency and reliable power supply. Inverter circuit is one of the important parts in the UPS system. One example of application requires the inverter to provide an AC supply to the load with fixed DC source supply is aircraft power supplies with variable-speed AC motor drives. Based on research, there exist approaches in designing inverter circuit to provide high quality AC output. There is an existing inverter with simple and highly efficient approach. However, since the front-end and the inverter stages share power switches, there is no isolation between the main line and the load [3]. Another existing inverter designed which provides isolation between main line, the battery set and the load that provides a good dynamic response; however the power topology is complex [4].

A solution proposed is an inverter circuit design with isolation in between the main line and the load, while maintaining the simplicity of the circuit in providing a stable AC output using full bridge single phase topology. Isolation is a must for protection, in case of power failure the load side is isolated. The solution proposed to perform comparative study of MOSFET and COOLMOS in high-frequency inverter design for UPS system. The studies of the switches are in the inverter circuit with lowest switching losses, leads to highest efficiency as main criteria. MOSFET well known for its low switching losses has been in the market quite some times. COOLMOS is a high voltage MOSFETs, 600V a recent new device based on concept called the super junction (SJ), [5]. The comparisons to select the best switch are in terms of switching losses (heat dissipation) in the switches during the switching activity. Also, leakage spike of current and voltage output waveform if there are any are investigated.

1.3 Objectives and Scope of Study

This project investigates the performances of MOSFET and COOLMOS in high-frequency inverter circuit for UPS applications. The best switch produces lowest switching energy losses is to be selected. It requires designing a VSI inverter with single phase full-bridge high-frequency topology, having a 150-Vdc input and a fifty percent (50%) duty cycle. Using this inverter circuit as platform, the two power switches performance are compared and analyzed. In this project the author focused on performing investigation using MOSFET as switches. For the comparative study of MOSFET and COOLMOS; COOLMOS investigation results performed by the author's partner are referred, [17].

1.3.1 Objectives

1. To construct a high frequency single-phase full-bridge inverter circuit with isolation between the main and the load in providing a stable AC output for UPS application.
2. To compare performance of MOSFET as power switches in high frequency inverter design:
    a. Via simulations using Cadence PSpice software
    b. Via experiments execution on PCB Layout
3. The performance of MOSFET switches are investigated with: frequency of 500 kHz, duty ratio of 0.5 and input voltage of 150-Vdc.
4. The output analyzed are:
    a. Output Voltage and Current
    b. Energy Switching Losses

1.3.2 Scope of Study

Scope covers power and analogue electronics area of specialization; inverter circuit design, power semiconductor devices; MOSFET and some mathematical formula analysis. The simulation performed using PSpice Cadence PSD 14.2 software; PCB layout designed using Multisim 2001 and Ultiboard 2001 software.

1.3.3 Gantt chart

The Gantt chart was developed to ensure the project to be feasible and done within the scope and time frame. The Gantt chart of this project is as attached in Appendix 1.

CHAPTER 2
LITERATURE REVIEW AND THEORY

Many studies by worldwide professional involves in designing a high frequency inverter design with the function of an inverter is to change a DC input voltage to a symmetric AC output voltage of desired fixed or variable magnitude and frequency by means of using the gate-driven semiconductor devices as switches, such as MOSFET are used. Thus, a high-frequency inverter circuit design is used as basis of comparative study of most efficient power switches, COOLMOS and MOSFET in terms of producing low switching losses.

2.1 Inverter Design

Figure 1 shows an inverter having both resistive and inductive (R-L) load under full-bridge topology.

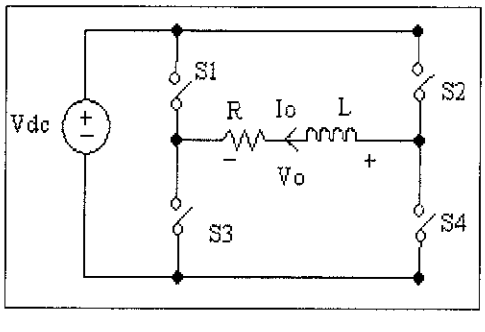


Figure 1 Full-bridge inverter with resistive-inductive load

An inverter design circuit operation depends highly on its switching sequences. The switching sequence of four switches; S1, S2, S3 and S4 in a 50% duty cycle at a switching frequency *f*, are turned on and off complimentarily between switches S2-S3 and S1-S4. In Figure 2, it shows the switching waveform at a 50% duty cycle of S1, S2, S3 and S4.

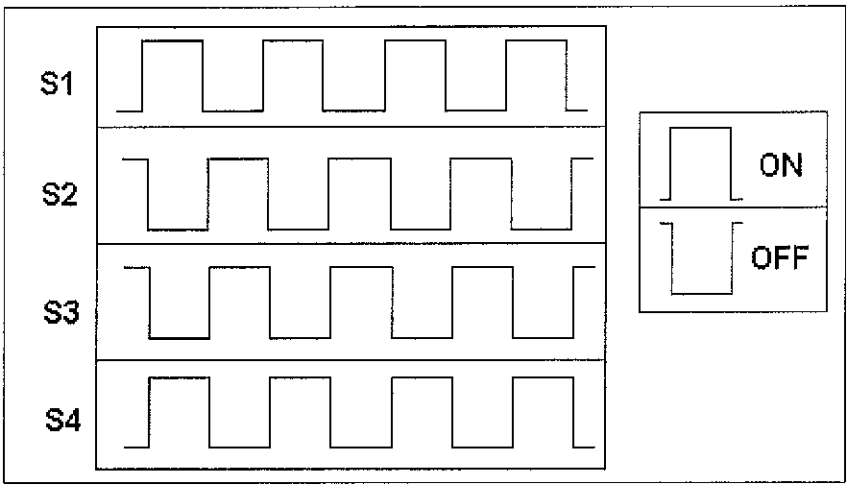


Figure 2 Switching sequences for full-bridge inverter at 50 % duty cycle

From the switching sequences shown in Figure 2, inverter circuit operates at a 50% duty cycle with a two-state output the current and voltage waveforms are as shown in Figure 3.

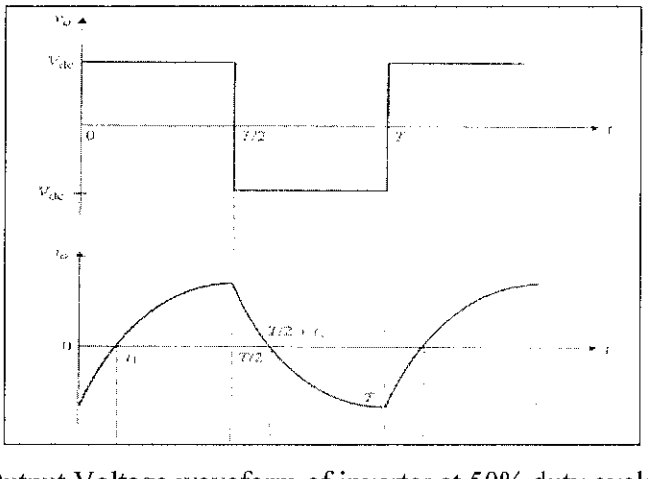


Figure 3 Output Voltage waveform of inverter at 50% duty cycle, [6]

The circuit generates a square ac voltage waveform across the load terminals from a constant dc source, The voltages V_{dc} and $-V_{dc}$ are applied across the load when S2-S3 are on and S1-S4 are off, respectively. The output voltage frequency is equal to $1/T$ and is determined by the switching frequency. This is true as long as S2-S3 and S1-S4 are switched complementarily.

The output voltage; the V_o is symmetric and is given by:

$$V_o = V_{dc} \qquad 0 < t < T/2$$

$$= -V_{dc} \qquad T/2 < t < T$$

Assuming the inverter operates in the steady state and the inductor current waveform produced, is initially negative value whereby, in the switches the current actually flows in reverse direction through the fly back diode of the bidirectional switch (MOSFET) as seen in Figure 4.

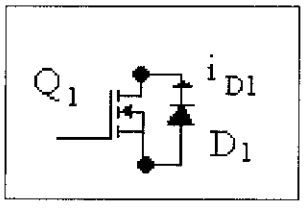


Figure 4 MOSFET switch

In steady-state, the following conditions apply:

$$i_L(0) = -i_L(T/2)$$

$$i_L(0) = i_L(T)$$

Where $\tau = L/R$. since $I_L(T/2) = -I_L(0)$, the initial condition at $t = 0$ is constant and given by;

$$I_L(0) = -\frac{V_{dc}}{R}\frac{1-e^{-\frac{T}{2\tau}}}{1+e^{-\frac{T}{2\tau}}}$$

2.2 MOSFET and COOLMOS Characteristics

The features and characteristics of MOSFET are studied to understand the power semiconductor devices. Features of MOSFET are as listed below:

- Blocking voltage technology of <600 V of *Vds*
- Dynamic *dV/dt* rating
- Repetitive Avalanche rated
- Isolated Central Mounting Hole
- Fast Switching
- Simple Drive Requirement
- Easy paralleling
- High frequency application

Power MOSFETs with appreciable on-state current carrying capability and off-state blocking voltage capability and have been in power electronic applications since early of 1980s, [7]. MOSFET contains minimal resistance when conducting and could sustain high voltages when the device is off, seems having limitation in high voltage levels due to its poor conduction properties. High Voltage design needs low doping concentration and decreased thickness of the epitaxial layer (n^-) to maintain the electric field below the semiconductor breakdown value. The same doping limits quantity of electrons available for the current flow. Thus, it defines the device resistivity giving the relation $R_{DS(on)} \approx V_{BR(DSS)}^{2.4\text{-}2.6}$,[1].

Lately, a new device concept called Super Junction called (SJ) MOSFET (COOLMOS) gaining more attention, [8-11]. COOLMOS is a novel power MOSFET with a "super-junction" for its drift region, which resulting a vastly improved relationship between the on resistance and breakdown voltage, [12].
The conventional MOSFET and COOLMOS structure are shown in Figure 5.

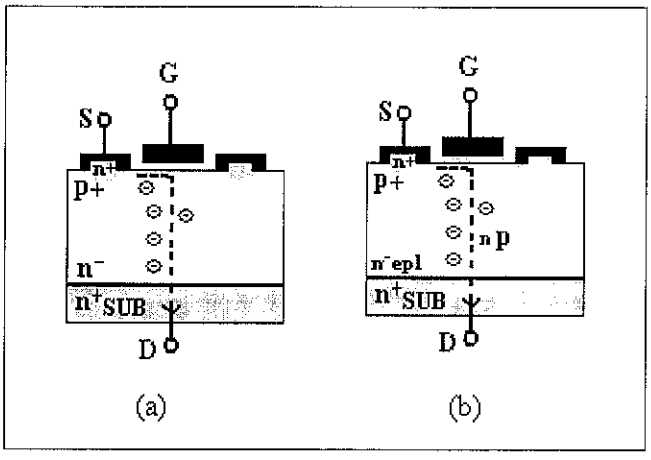


Figure 5 (a) Conventional MOSFET structure (b) COOLMOS structure, [1]

Referring to figure above, COOLMOS structure is based on conventional MOSFET. COOLMOS presents two vertically heavily doped p-type and n-type semiconductor columns in the drift region, This allows increase of the n- drift doping which permits a reduction of the resistance, $R_{DS(on)}$. Additionally, the structure allows electric field expansion both vertical and horizontal direction. The characteristics of COOLMOS are to be having $R_{DS(on)}$ reduction of 5 to 10 times for the same silicon area, parasitic capacitance reduction and better dynamic behavior as well device fabrication for high voltage breakdown.

COOLMOS exhibit very low gate charge compares to $R_{DS(ON)}$ of conventional MOSFET technology. The switching losses are determined by the charging process of the gate drain feedback capacitances. The lower the gate charge, the lower the switching losses. The drastic reduction of the gate charge in new COOLMOS technology is clearly visible from Figure 6, where a 0.9 Ω standard MOSFET is compared to a lower Ohmic COOLMOS device.

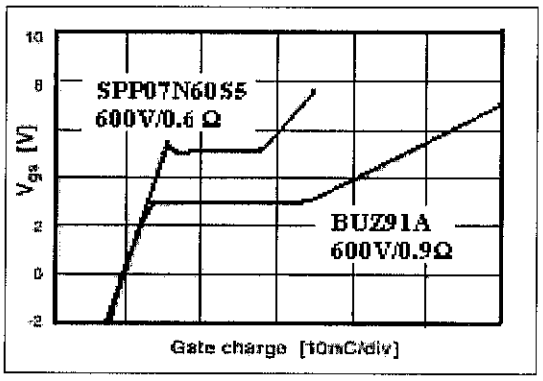


Figure 6 Gate Charge characteristics of COOLMOS vs. MOSFET, [13]

The generated energy converted into heat in every turn-on process increases with the chip area limits the minimum attainable power loss in hard switching circuit topologies. Based on Figure 7, the energy losses by using COOLMOS as power switches is lower compared to the standard MOSFET. Resulting COOLMOS can be operated with the lowest control power, the cheapest driver circuit and the highest switching frequencies.

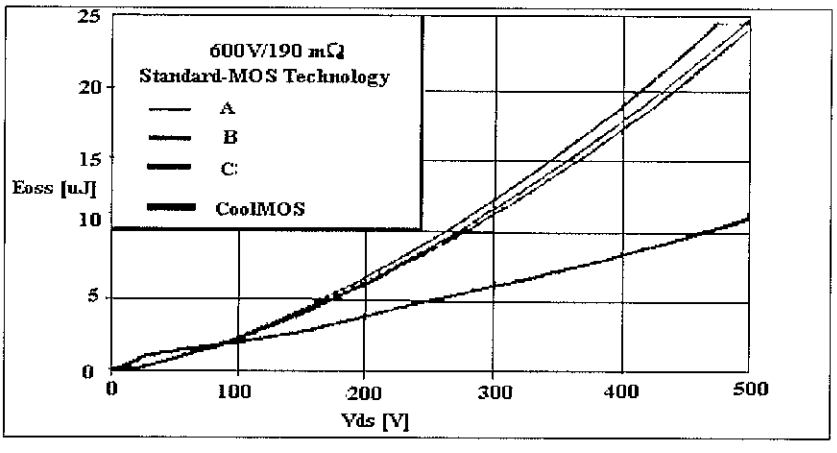


Figure 7 COOLMOS cuts the stored energy by a factor of two vs. MOSFETs, [13].

The switching behavior of COOLMOS can be observed for the turn-on and turn-off switching in Figure 8 and 9 respectively.

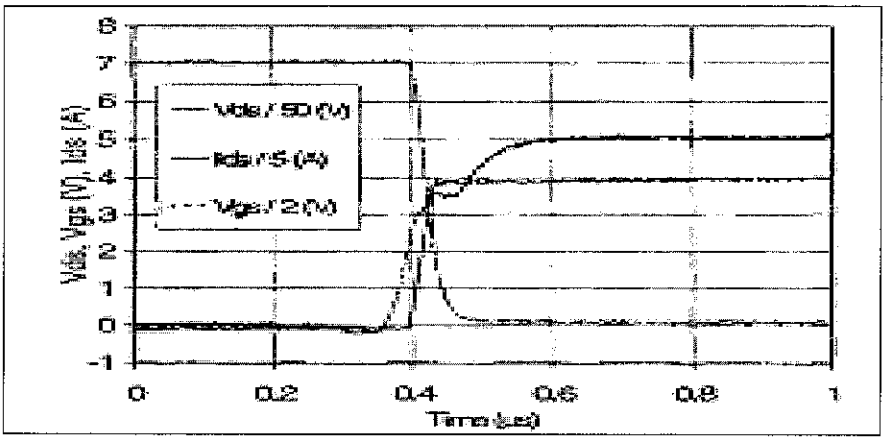


Figure 8 Turn-On behavior of COOLMOS with Ohmic load, [13]

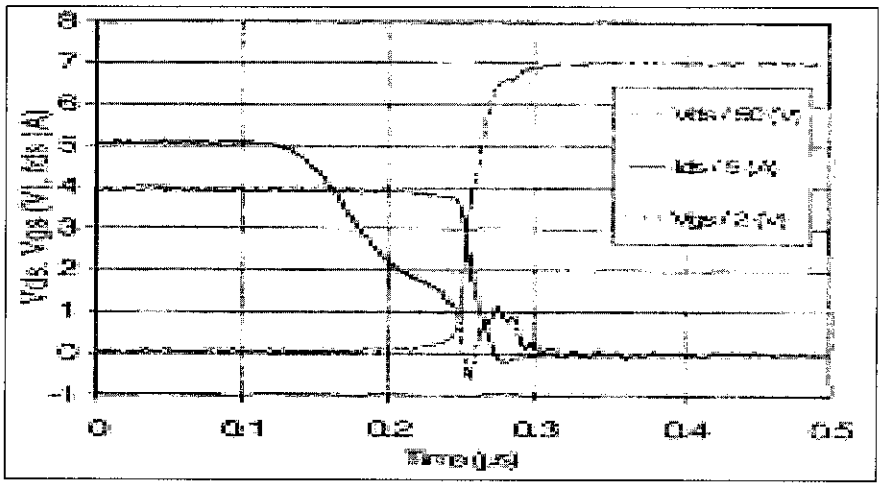


Figure 9 Turn-Off behavior of COOLMOS with Ohmic load, [13]

The turn-off characteristics show absolutely no tail current, with the soft switching behavior up to a voltage around 50 V which is clearly visible. During the turn-off, there is no carrier flow exists through the high field region. Hence, the COOLMOS is not sensitive to second breakdown phenomena, it can be switched at a very high *dV/dt* rates.

COOLMOS implements a compensation structure in the vertical drift region of a MOSFET in order to reduce the state resistance. Such structure makes it possible to reduce the on-state resistance of 600 V MOSFET to one fifth of that of the conventional MOSFET for the same circuit. Thus, COOLMOS achieves the fastest switching speed for the same given circuit [14].

CHAPTER 3
METHODOLOGY/PROJECT WORK

3.1 Methodology

The project is performed by two students are divided into two parts, first semester simulation investigation via Cadence PSpice software and second semester experimentation investigation on PCB layout. The author performs both simulation and experimentation using MOSFET and then compared the results with COOLMOS investigation outcomes. The flow chart for semester 1 is shown in Figure 10.

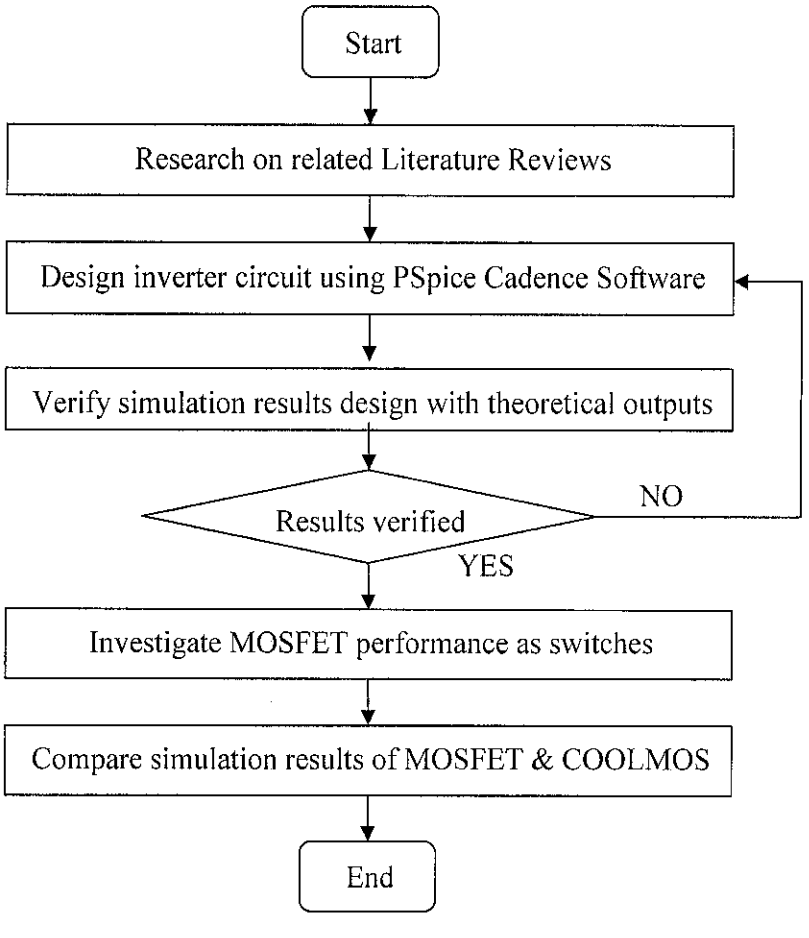


Figure 10 Process Flow for Semester 1

The flow chart for semester 2 is shown in Figure 11.

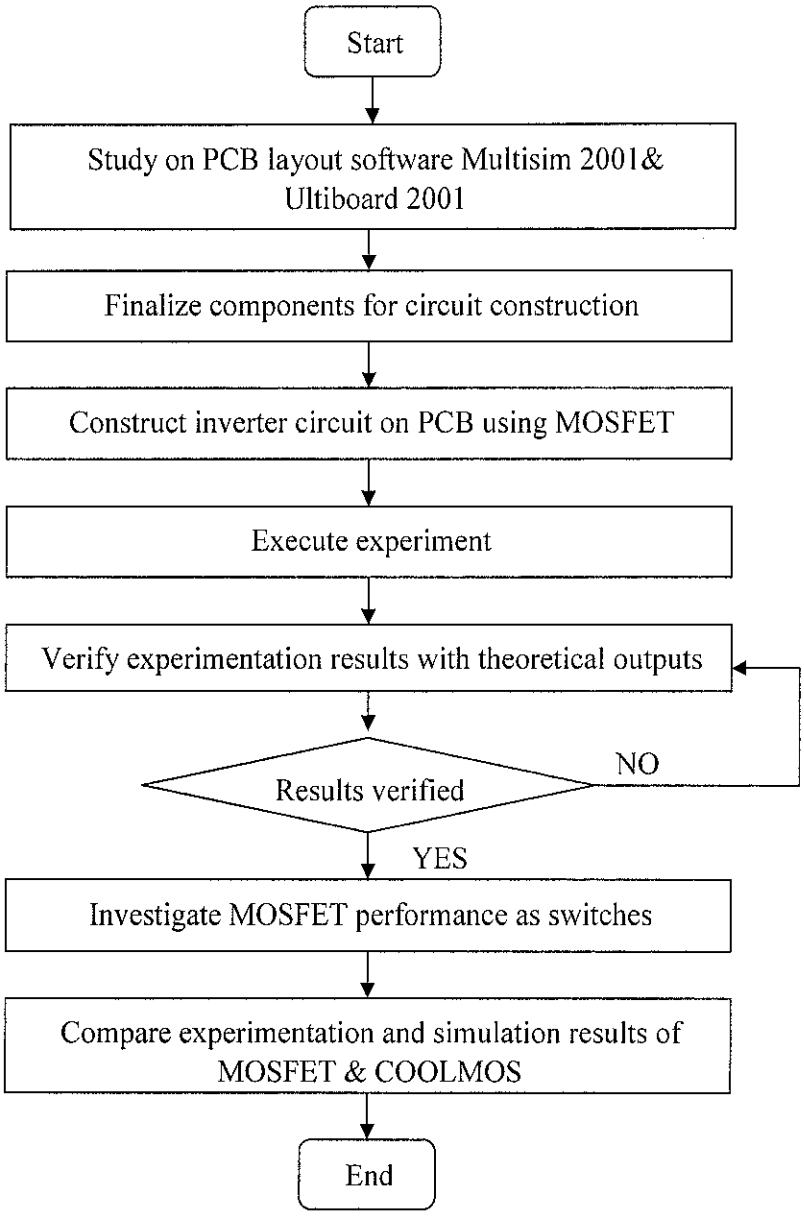


Figure 11 Process Flow for Semester 2

3.2 Procedure Identification

The Procedure Identification of the project is as follows:

1. Research on related Literature Reviews:

   Research mostly obtained from the IEEE Website of relevant information and data of the project. Researches of existing inverter circuits in UPS application are for exposure of current problems faced by industrial practitioners. Researches of MOSFET and COOLMOS datasheets, characteristics and features are for reference in inverter circuit design. The device rating is ensured not exceeded. Also, research is done on inverter circuit operation, the output waveforms and calculations are referred through Power Electronics Circuit by Issa Batarseh. Research on PSpice Cadence software is referred to the PSpice reference books [15, 16].

2. Design a high-frequency inverter circuit using PSpice Cadence software:

   A simple basic single-phase full-bridge inverter circuit with resistive-inductive load is practically used in the industry. The circuit is constructed in PSpice Cadence software with components use as shown in Table 1.

Table 1 Components For Simulation Inverter Circuit

NO.	ITEM
1	Power Switches: MOSFET Model: IRF644 ($V_{DSS} = 250V$)
2	Isolator: Transformer
3	Loads: Resistive Load: $R = 10\ \Omega$ Inductive Load: $L = 18\ \mu H$
4	Input Signal Resistor: $R_1 = R_2 = R_3 = R_4 = 1\ \Omega$

The selection type power switches of MOSFET are important to obtain the correct output waveforms verify with theoretical data. The transformer is use for protection to isolate the load side. The restive and inductive load is selected to apply the common practice by the industry. Although MOSFET is a voltage controlled device, is having an input signal resistor of 1 Ω is placed at the gate

terminal of MOSFET for protection purposes. Basically, selecting type of components in a circuit design is very crucial since each component has its own rating and characteristics, thus generates different results. The simulations are done repeatedly to get the expected theoretical results.

The inverter is set to be at high-frequency (>100 kHz) of 500 kHz to eliminate noise and distortion at the produced AC. The input voltage is 150-Vdc, to comply with high rated voltage for UPS application. The inverter is to have a 50% duty cycle, so a stable AC output can be generated with an equal proportion of positive and negative cycle at the output waveform. Once the inverter circuit is simulated and the output waveforms produced are verified with related theories. Then, a comparative study of the switches performance is investigated with the varying parameters as shown in Table 2.

Table 2 Simulation Comparative Study Parameters

PARAMETERS	BASE VALUE	PARAMETER VARIES	
Frequency , f	500 kHz	1 MHz	5 MHz
Duty ratio, D	0.5	0.4	0.6
Input Voltage, V_{in}	150V	200V	400V

The simulation is performed and the output voltage, output current and the switching losses waveforms are obtained. The waveforms are examined using MOSFET as switches.

3. The Simulation results :

The simulation investigated outputs are as follows:

i. Output Voltage, V_{out} and Current, I_{out}

Based on VSI design the output voltage; V_o is a function of inverter operation, meanwhile the load current I_o, is a function of the nature of the load. The performances of the switches are observed whether the peak magnitude of the waveform is achieved as calculated.

ii. Switching Losses at the switches

These are examined during the switching modes of turn-on and turn-off. The switching energy losses for the switches are calculated as an area under the graph of power losses.

4. Once investigation of inverter design using MOSFET as switches were done, the simulation results were compared with the outcomes of COOLMOS investigation done by the author's partner in this project. For output voltage and current waveform, the output waveforms produced that is similar to theoretical and achieved the peak value is considered as the better switch in the inverter circuit. Meanwhile the switching energy losses obtained the lowest are considered as the more efficient switch.

Based on Flow Chart in Figure 10, the steps taken in designing inverter circuit using Pspice Cadence software, the simulation outcomes are referred to the theoretical data for verification for MOSFET. Whenever problem is encountered and the simulation results does not match with the reference data, these steps are again repeated until satisfactory results obtained, before proceeding with the comparative study.

5. Study on PCB layout software such as Multisim 2001 & Ultiboard 2001
   For construction of the inverter circuit on PCB both software Multisim 2001 & Ultiboard 2001 are used. Before proceed with construction of the PCB layout the software are first studied.

6. Finalize the components for circuit construction:
   The components selections are based on simulation performed, for frequency of 500 kHz, duty ratio 0.5 and input voltage of 150 Vdc. This selection includes factors on limitation of cost and availability in the market. The components selected and the details are as shown in Table 3 below.

Table 3 Components Details

NO.	ITEM	ORDER CODE	NO. OF ITEM	PRICE
1	Inductor 18 uH Inductor Series 2100	4981601	1	RM 13.03
2	Resistor 10 Ohm Wire-wound Aluminum Clad, 200W	272723	1	RM 100.02
3	Resistor 1 Ohm Wire-wound Aluminum Clad, 100W	652453	4	RM 31.77

4	MOSFET Model: IRF644 (Vdss:250V, f= 1.0MHz)	2288849	4	RM 7.17
5	Capacitor 250VAC 4700pF	3531892	1	RM 1.69
6	Capacitor 200 VDC 100pF	286930	1	RM 0.99

*For further reference please refer to Appendix 3

7. Construct inverter circuit on PCB:

   Constructing inverter circuit on PCB requires the circuit designed using Multisim 2001 software transferred to Ultiboard 2001 software to produce gerber file, before the PCB fabrication.

   i. *Multisim 2001 software*: The inverter circuit is designed with the components placed are specifically selected from the library folder to match the required footprint.

   ii. *Ultiboard 2001 software:* From Multisim software, the inverter circuit file is transferred to Ultiboard 2001 software with only the components and information layer are shown. By default, components are placed outside the board outline when the netlist is imported from Multisim. The components are then dragged into the correct place as to be printed on the PCB layout. The PCB specify as a single layer and having copper bottom design. Trace width, drill hole diameter of the pads and the spacing between components are designed specifically before auto-routing function is activated for auto-route the traces between components. Before exporting to the Gerber file any open traced ends and unused vias left on the board are deleted. Gerber file produced by exporting the designed in the Gerber file format. RS274X and NC Drill are chosen and the entire available layers list is exported.

8. Execute experiment:

   An extra external circuit is constructed using Bipolar Junction Transistor (BJT) with only 1 function generator are use to trigger the switches. The function generator pulse is use to trigger switches for positive cycle, meanwhile the output of this extra circuit is to trigger switches for negative cycle of the inverter as shown in Figure 12.

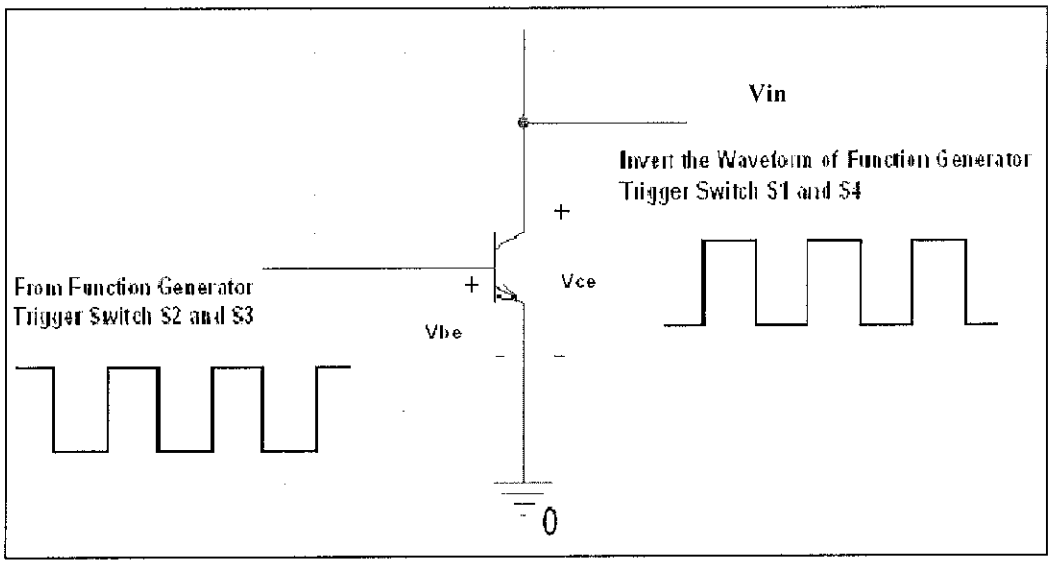


Figure 12 BJT switch for switches input signal

The setup for experiment execution is as shown in Figure 13.

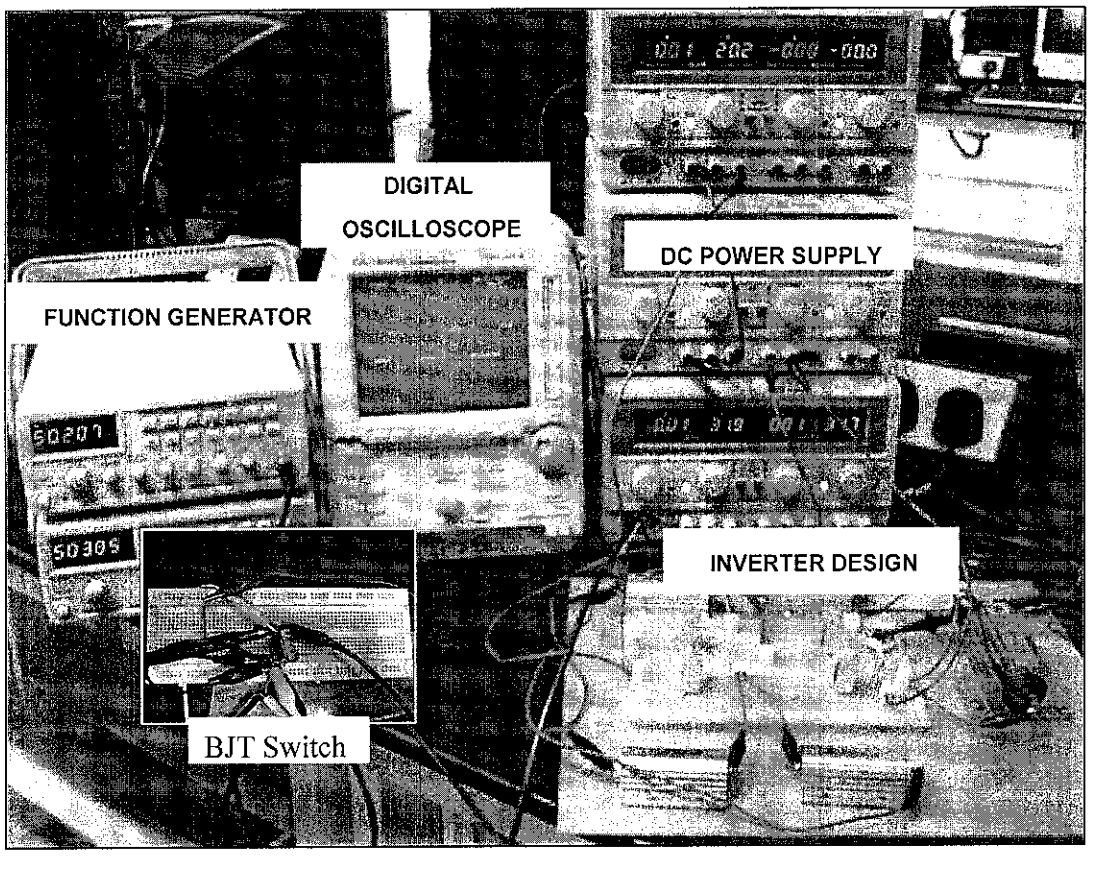


Figure 13 Experimentation setup

Experiments are executed by using base value parameters are as shown in Table 4.

Table 4 Experimentation Comparative Study Parameters

PARAMETERS	BASE VALUE
Frequency , f	500 kHz
Duty ratio, D	0.5
Input Voltage, V_{in}	150V

With these values, the experiment is executed and the output voltage, output current and switching losses waveforms are obtained. The waveforms are examined using MOSFET as switches. The experimental results are then compared to simulation results as well compared with outcomes of COOLMOS investigation. For investigating the switches performances, the energy switching losses are obtained as follows:

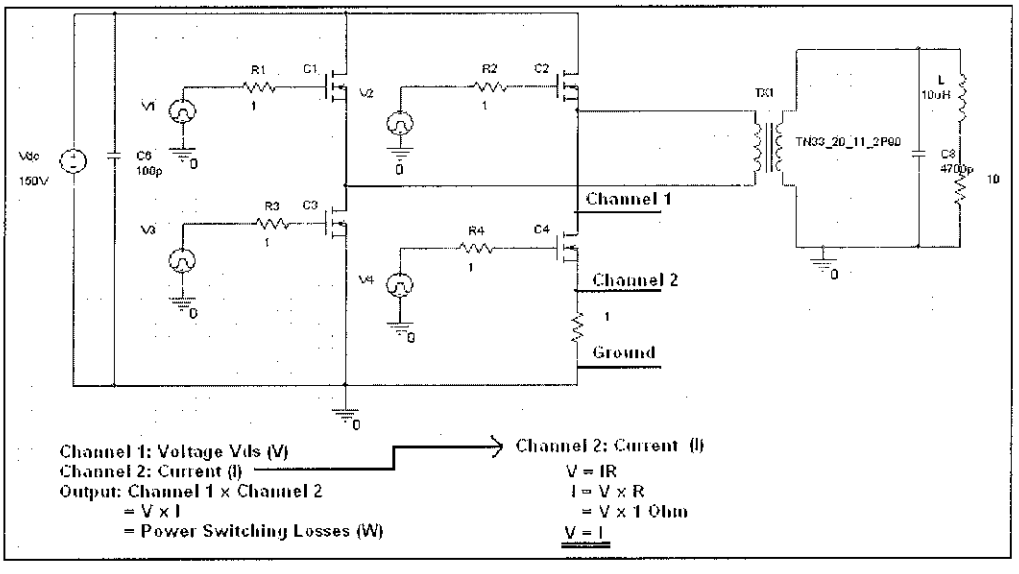


Figure 14 Experiment Circuit Configuration to obtain Power Losses Waveform

The energy switching losses are obtained by calculating area under graph of power losses waveform of the switch. The power losses waveform obtained by peforming multiplication via Math function of the digital oscilloscope.

Channel 1: Voltage across the drain to source terminal of the switch (*Vds*).

Channel 2: Current flow through the 1Ω resistor.

As the oscilloscope can only plot the voltage waveform, an extra 1Ω resistor placed between the source and ground terminal.

Theoretically:

$$V = IR$$
$$V = I \times 1\Omega$$
$$\therefore V = I$$

Thus, the current waveform is obtained in channel 2 by taking the voltage across resistor 1Ω.

3.3 Tools

The main tools used in this project are:

1. PSpice Cadence PSD 14.2 software
2. Multisim 2001 and Ultiboard 2001software.
3. Electrical and Electronics Components:
    i. Power Supply
    ii. Function Generator
    iii. Digital Oscilloscope

CHAPTER 4
RESULTS AND DISCUSSION

The comparative study of COOLMOS and MOSFET are performed using a high-frequency single-phase full-bridge inverter circuit as platform to compare the switches. The investigations are done via simulations using Cadence PSpice and via experiment executions on PCB Layout. All MOSFET investigation outcomes were performed by the author and were compared with the COOLMOS investigation outcomes perform by the author's partner in this project, in doing the comparative study. All data and information obtained from the author's partner part of investigation which is yet to be published report, [17].

First the simulation is performed with the parameters set to be as shown in Table 5.

Table 5 Parameter and setting for the simulations

• Switching Frequency, f_s	= 500 kHz
• Duty Ratio, D	= 0.5
• Period, PER	= 2.0 μs
• Pulse Width, PW	= 1.0 μs
• Time Delay, TD (for V_1 and V_4)	= 1.0 μs
• Time Delay, TD (for V_2 and V_3)	= 0
• Rise Time, T_R and Fall Time, T_F	= 0.1 μs
• Start saving data after	= 1040 μs
• Maximum step size	= 1.0 ns
• Transient point iteration limit	= 1000

Listed below are parameters varied for investigation of switches performances:

- Frequency, f
- Duty Ratio, D
- Input Voltage, Vin

The comparative study of the switches performance is investigated with the varying parameters as shown in the procedure identification (refer Table 2).

The simulation performed using the schematic inverter circuit as shown in Figure 15.

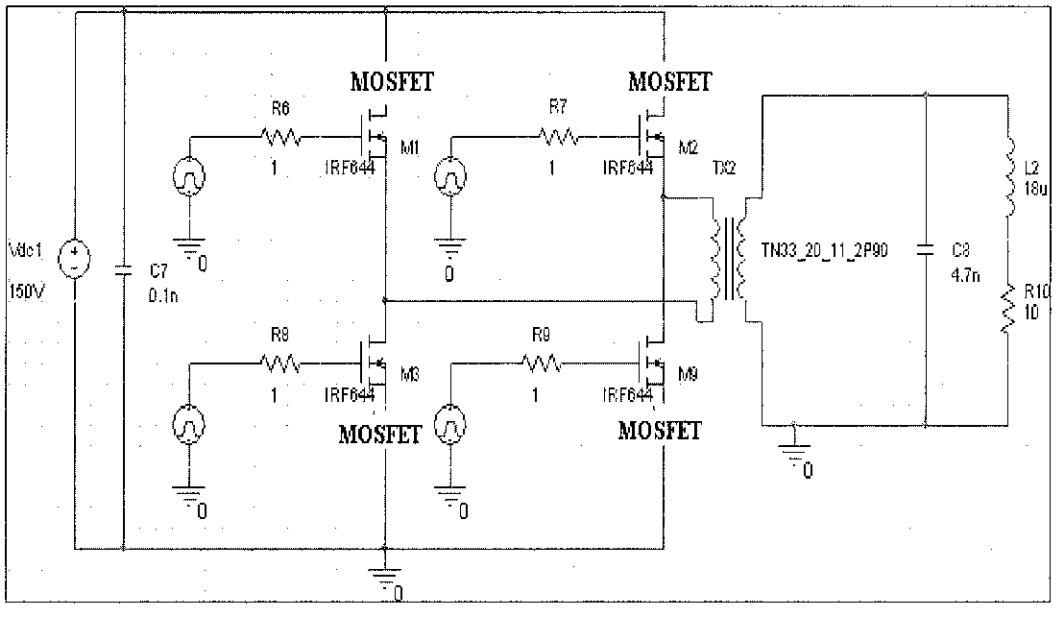


Figure 15 Simulation Full-Bridge Inverter Circuit using MOSFET as switches

Secondly, the experiment is done by constructing the single phase full bridge inverter circuit design using MOSFET as switches on the Printed Circuit Board, PCB placed with high rated resistors on acrylic board as shown in Figure 16.

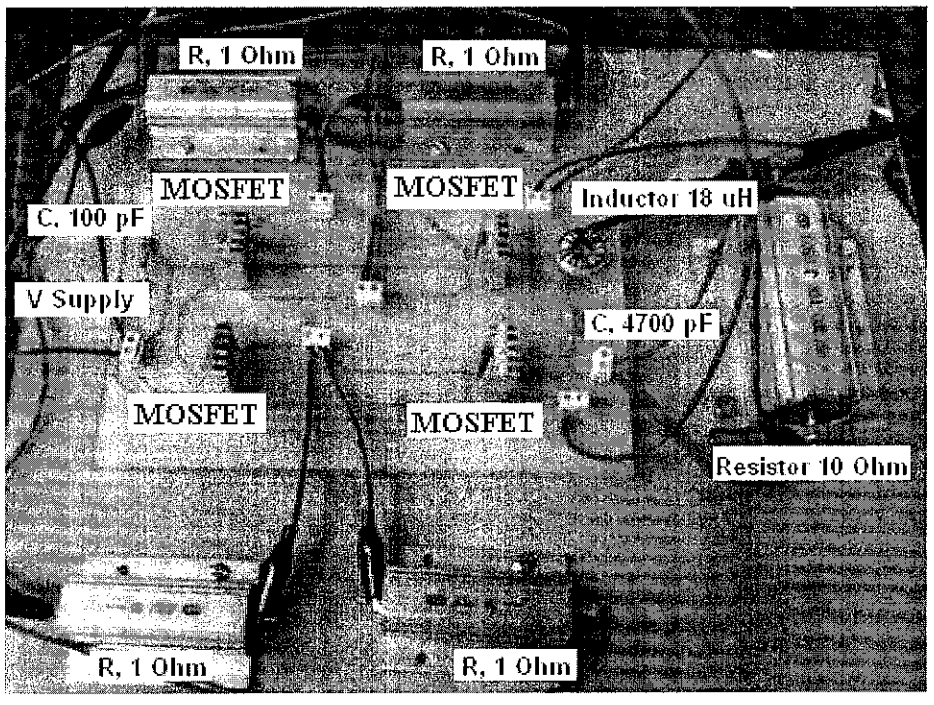


Figure 16 Full-Bridge Inverter Circuit for Experimentation

During the experimentation the pulse signals use to trigger the power switches for positive and negative cycle is as shown in Figure 17.

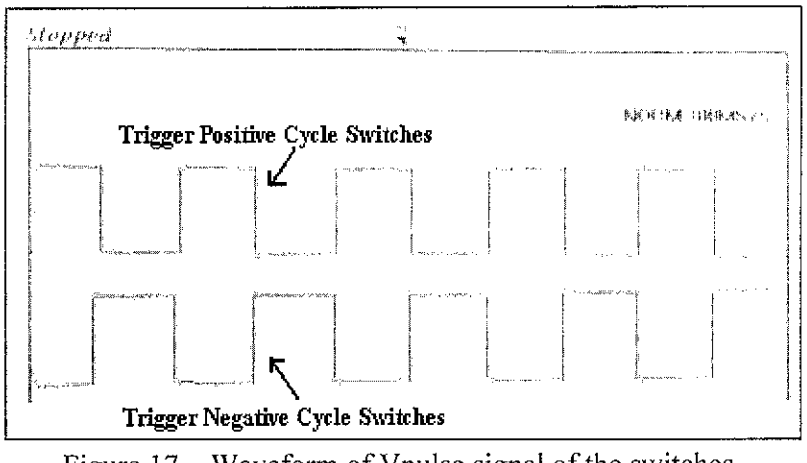


Figure 17 Waveform of Vpulse signal of the switches
(Scale; x:1us/div, y:5V/div)

4.1 Output Voltage and Current waveforms

The investigation resultant output voltage waveforms obtained for MOSFET were compared with resultant waveforms COOLMOS:

MOSFET

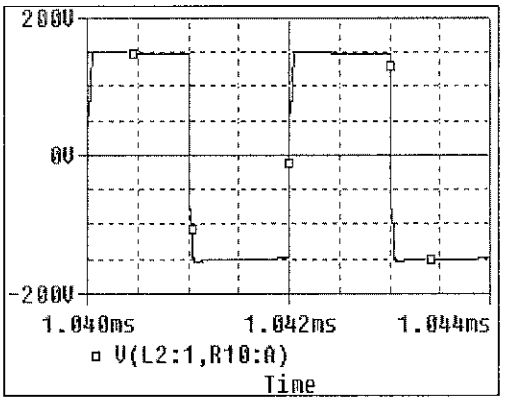


Figure 18 MOSFET simulation output voltage

COOLMOS

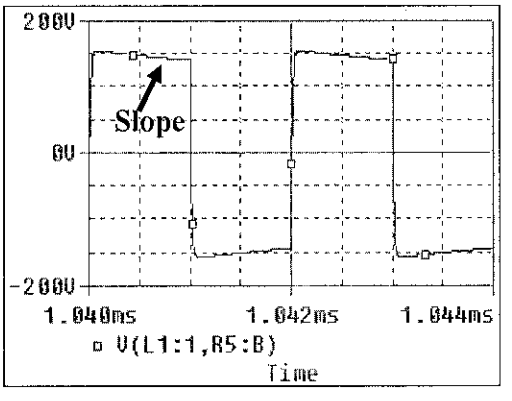


Figure 19 COOLMOS simulation output voltage, [17]

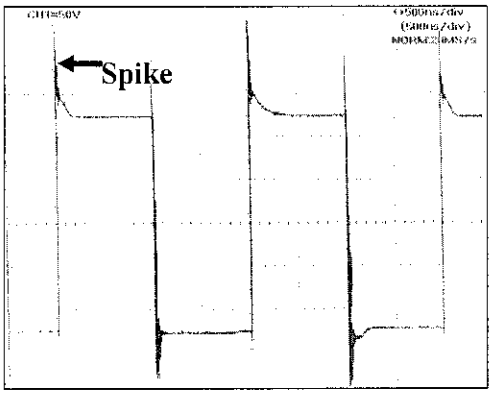


Figure 20 MOSFET experimental output voltage
(Scale; x:500ns/div, y:50V/div)

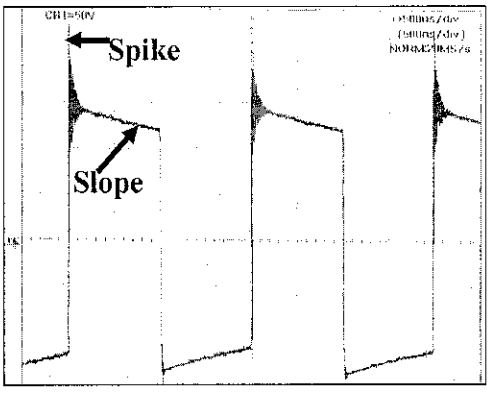


Figure 21 COOLMOS experimental output voltage, [17]
(Scale ; x:500ns/div, y:50V/div)

Figure 18 and 19 are simulation investigation of MOSFET compared to COOLMOS. Both are similar except that COOLMOS waveform shows the extreme *dV/dt* rated characteristics with a slope at the peak of the output voltage square waveform. Figure 20 and 21 are experimentation investigation of MOSFET compared to COOLMOS, observed having spike at the beginning of the waveforms; the voltage spike during turn-on and off are caused by internal noise exists in the components during

experiment. Both simulation and experimentation with input of 150-Vdc having the output produced by the inverter circuit is 150-Vac.

The investigation resultant output current waveforms obtained for MOSFET and COOLMOS are very similar. Thus the output current waveforms produced by MOSFET investigation are compared between simulation and experimentation resultant waveforms.

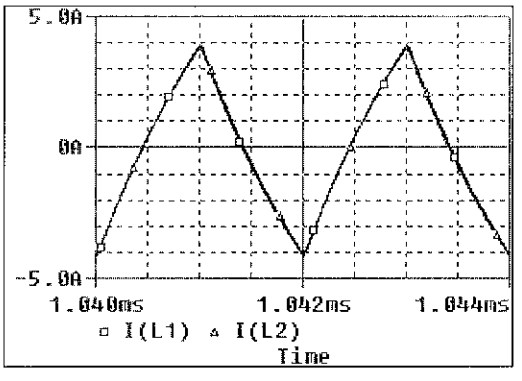


Figure 22 MOSFET simulation output current

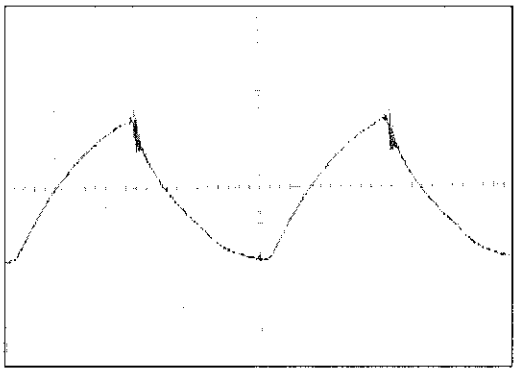


Figure 23 MOSFET experimental output current
(Scale ; x:400ns/div, y:2V/div)

The waveforms in Figure 22 and 23 shows the MOSFET output current waveform comparing both simulation and experimentation results. The output current starts at an initial current are calculated based on formula discussed in "Literature Review and Theory" of chapter 2 are as follows:

$$Io = -\frac{Vdc}{R}\frac{1-e^{-\frac{T}{2\tau}}}{1+e^{-\frac{T}{2\tau}}} = -\frac{150}{10}\frac{1-e^{-\frac{2}{2(1.8)}}}{1+e^{-\frac{2}{2(1.8)}}} = -4.063A$$

Where

$$T = \frac{1}{f} = \frac{1}{500k} = 2us$$

$$\tau = \frac{L}{R} = \frac{18u}{10} = 1.8us$$

The peak-to-peak output current using MOSFET as switches for simulation is 6.8A, meanwhile experimentally, is 4.6A. The differences mostly due to resistance exists in the wire connections and the components it selves.

4.2 Switching Energy Losses

The investigation of switching energy losses during switching operation of *turn-on* and *turn-off* were done via simulation for MOSFET and compared with resultant investigation of COOLMOS. As the switching losses during *turn-on* and *turn-off* are similar for experimental only switching energy losses during turn on were obtained and investigated. Simulation switching energy losses during *turn-off* are calculated based on Figure 24 and 25 for switches MOSFET and COOLMOS respectively.

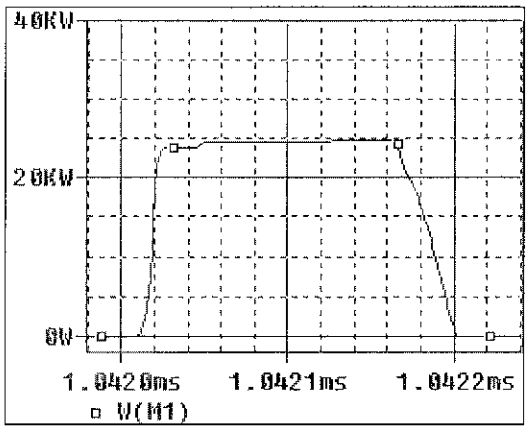


Figure 24 MOSFET simulation switching energy losses during turn-off

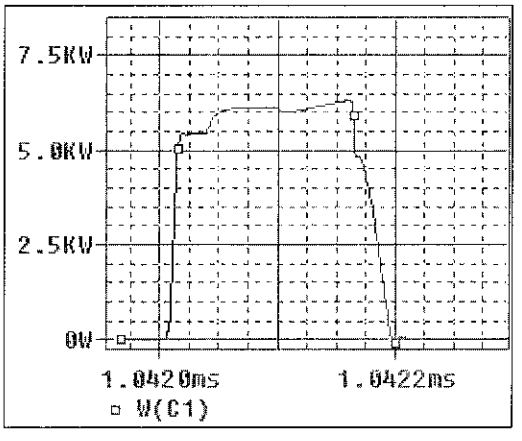


Figure 25 COOLMOS simulation switching energy losses during turn-off, [17]

The power losses waveform of the switches during turn-off switching operation is in kWatts. The switching energy losses are calculated as area under the graph of the power losses waveform as shown in Table 6.

Table 6 Calculation of Switching Energy Losses

SWITCHING ENERGY LOSSES
= Area under the graph of power losses waveform (kWatts)
= Nos. of boxes x Time (x-axis) x Power (y-axis)
= (Joules)

The calculation of MOSFET is compared with COOLMOS switching energy losses during turn-off switching operation are as shown in Table 7.

Table 7 Calculation of Switching Energy Losses during turn-off

SWITCHING ENERGY LOSSES	SIMULATION
MOSFET	= 2.1 x 100 ns x 20 kW **= 4.2 mJ**
COOLMOS	= 2.4 x 100 ns x 5 kW **= 1.2 mJ**

It can be concluded that the switching energy losses experience by MOSFET is greater than MOSFET up o 75% compared to MOSFET. Thus, comparative investigations are continued during turn-on switching operation as shown in figure 26 and 27 for simulation and figure 28 and 29 for experimental results analysis.

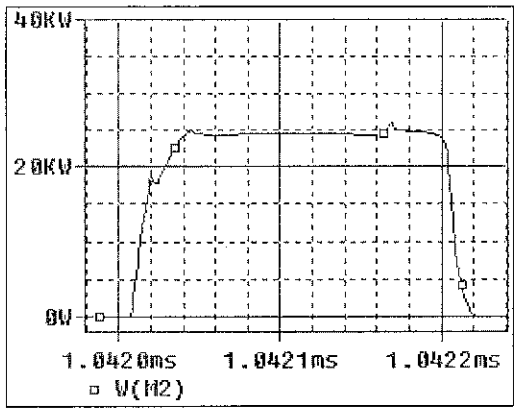


Figure 26 MOSFET simulation switching energy losses during turn-on

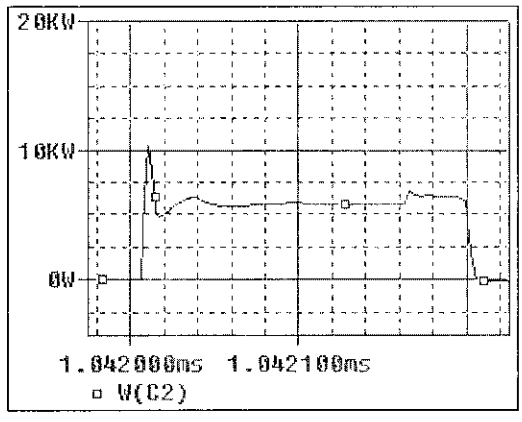


Figure 27 COOLMOS simulation switching energy losses during turn-on, [17]

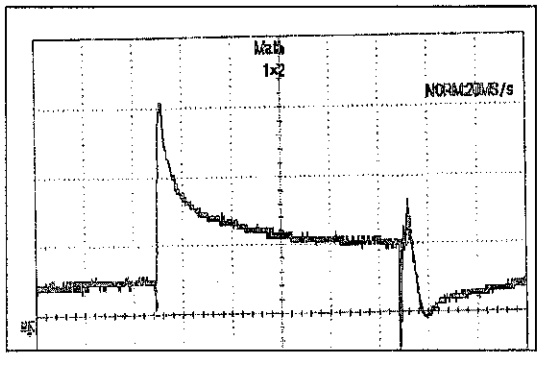


Figure 28 MOSFET experimental switching energy losses during turn-on
(Scale ; x:200ns/div, y:5kV/div)

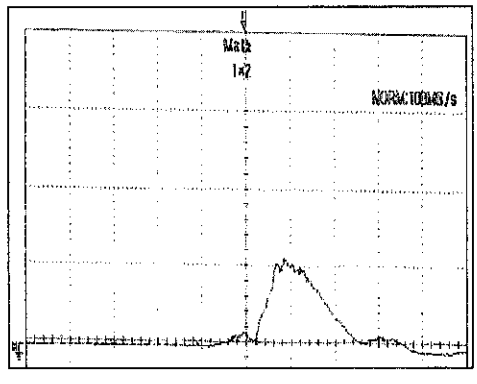


Figure 29 COOLMOS experimental switching energy losses during turn-on, [17]
(Scale ; x:200ns/div, y:5kV/div)

Then, the switching losses are calculated for both experimental and simulation waveforms. For the experimental results, both COOLMOS and MOSFET obtained at 200ns/divison and 5kV/division. The switching energy losses experienced by MOSFET are compared to COOLMOS as shown in Table 8.

Table 8 Switching Energy Losses

SWITCHING ENERGY LOSSES	SIMULATION	EXPERIMENTATION
MOSFET	= 2.5 x 100 ns x 20 kW **= 5 mJ**	= 7 x 200 ns x 5 kW **= 7 mJ**
COOLMOS	= 2.4 x 100ns x 5 kW **= 1.2 mJ**	= 1.25 x 200 ns x 5 kW **= 1.25 mJ**

Here, the comparison of switching energy losses between MOSFET and COOLMOS, for both simulation and experimentation shows MOSFET have greater switching energy losses up to 50% compared to COOLMOS. Comparing the switching energy losses of experimentation, which are slightly higher than simulation, are as in experimentation the resistance of the PCB tracks, connection wires and digital oscilloscope probes are accounted for. The comparison of simulation and experimental switching energy losses is plotted as in Figure 30.

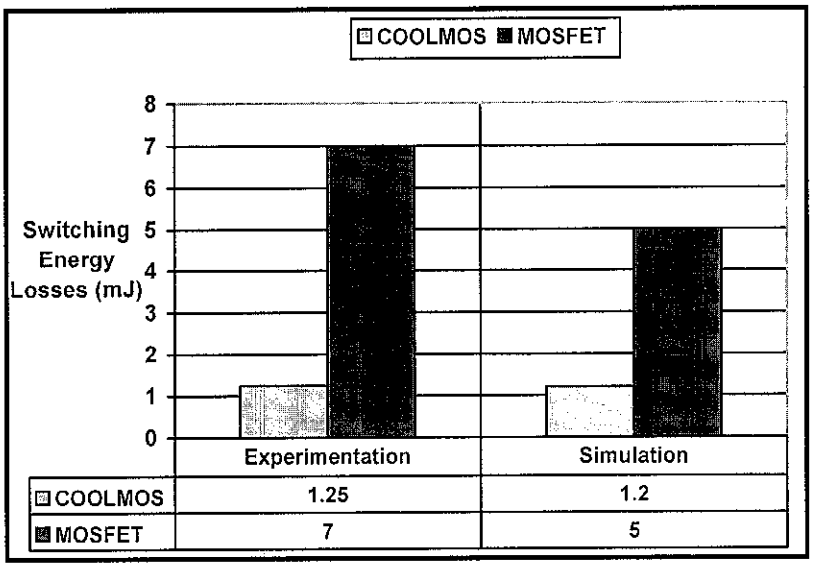


Figure 30 Simulation and Experimentation Switching Losses

4.3 Extra-investigation via simulation

It is highlighted here that for the extra investigation done in comparative study of MOSFET and COOLMOS in a high frequency inverter design performed via simulation using Cadence PSpice software are done together MOSFET and COOLMOS. This is to obtained clearer comparison of resultant waveforms of MOSFET and COOLMOS. Thus all the resultant waveforms shown are similar to the author's partner results, [17].

4.3.1 Varying f = 1, 5 & 10 MHz with constant D = 0.5 and Vin = 150V.

At frequency of 1 MHz the output voltage and current waveforms are acceptable as theoretical. However at frequency of 5 MHz, the output voltage and current waveforms obtained of the inverter circuit for both switches MOSFET and COOLMOS are experiencing a slight distortion. The waveforms are as attached in Appendix 2. Comparing the Maximum Output Voltage and Current at 3 Frequencies are as shown in Table 9.

Table 9 Comparing Simulation Maximum Output at 3 Frequencies

Frequency, f	Maximum Output Voltage (V)		Maximum Output Current (A)	
	MOSFET	COOLMOS	MOSFET	COOLMOS
500 kHz	150.326	153.001	3.2869	3.3908
1 MHz	149.896	150.650	1.3136	1.3659
5 MHz	149.85	149.85	0.3139	0.2677

For very high frequency of 10 MHz, the resultant output voltage and current waveforms of both switches are severe distorted as shown in Figure 31 and 32 respectively.

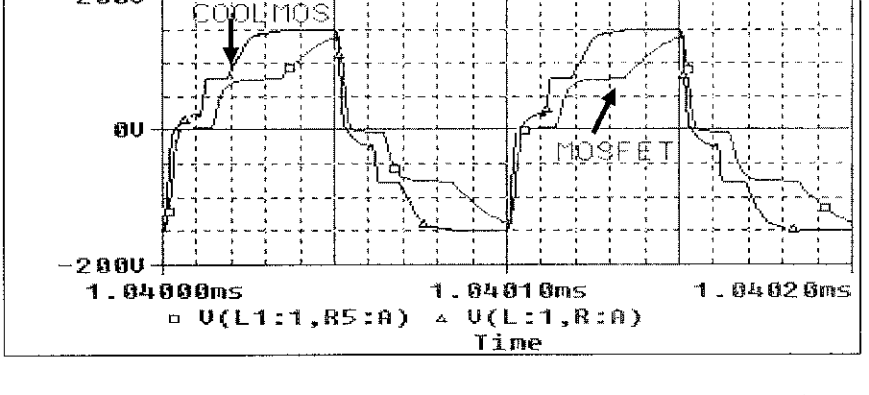


Figure 31 Output Voltage, *Vout* with *Vin* = 150V, *f* = 10 MHz and *D* = 0.5

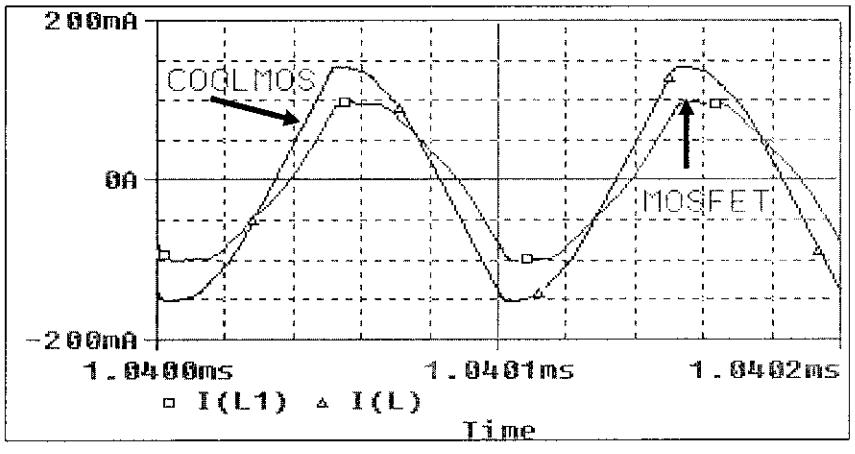
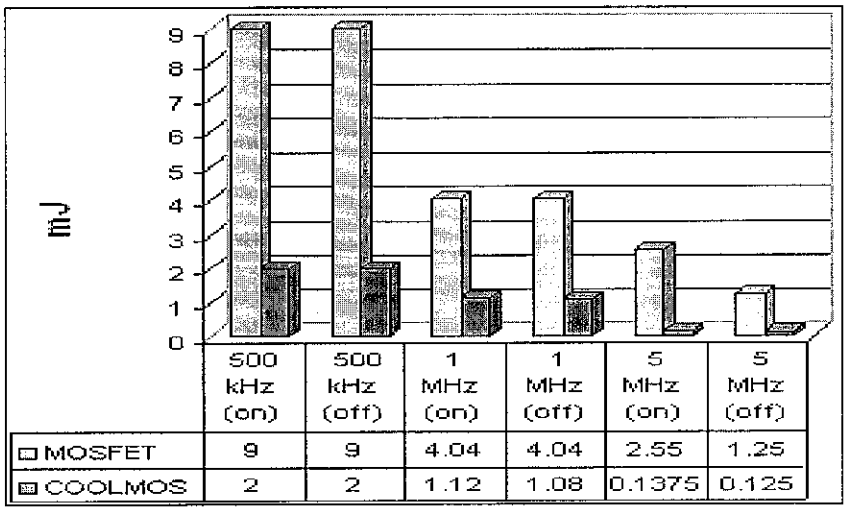


Figure 32 Output Current, *Iout* with *Vin*= 150V, f = 10 MHz and D = 0.5

Based on the output waveform obtained, thus it proves both switches unable to operate at very high frequency. This distortion is caused by the internal structure of switches, which could not sustain the high switching frequency more than 5 MHz. This output voltage waveform is having a severe distortion which is highly degrades the performances of the switches. The AC output voltage produced is no longer stable. Hence, the switching frequency of 10 MHz for both switches is not acceptable in inverter design for UPS application.

The switching energy losses at f = 500 kHz, 1 MHz & 5 MHz for both COOLMOS and MOSFET are compared in Bar Chart shown in Figure 33 below:



	500 kHz (on)	500 kHz (off)	1 MHz (on)	1 MHz (off)	5 MHz (on)	5 MHz (off)
MOSFET	9	9	4.04	4.04	2.55	1.25
COOLMOS	2	2	1.12	1.08	0.1375	0.125

Figure 33 Bar Chart of Switching Energy Losses at f=500kHz, 1MHz & 5MHz

Overall switching energy losses for MOSFET are higher more than 50% than COOLMOS. As the operating frequency increases, the switching energy losses decrease. This is based on the relations between power, energy and frequency.

Given:

Power $= P$ (Watts)

Energy $= E$ (Joules)

Time $= T$ (Seconds)

Power Equation: $P = \frac{E}{T}$ with $T = \frac{1}{f}$

Thus, $P = Ef$ and the frequency is $f = \frac{P}{E}$

Energy is inversely proportional to the frequency. As the frequency is increases, the energy losses are reducing for both COOLMOS and MOSFET during turn-on and turn-off.

The comparison of COOLMOS and MOSFET efficiency for 3 different frequencies is as shown in Figure 34.

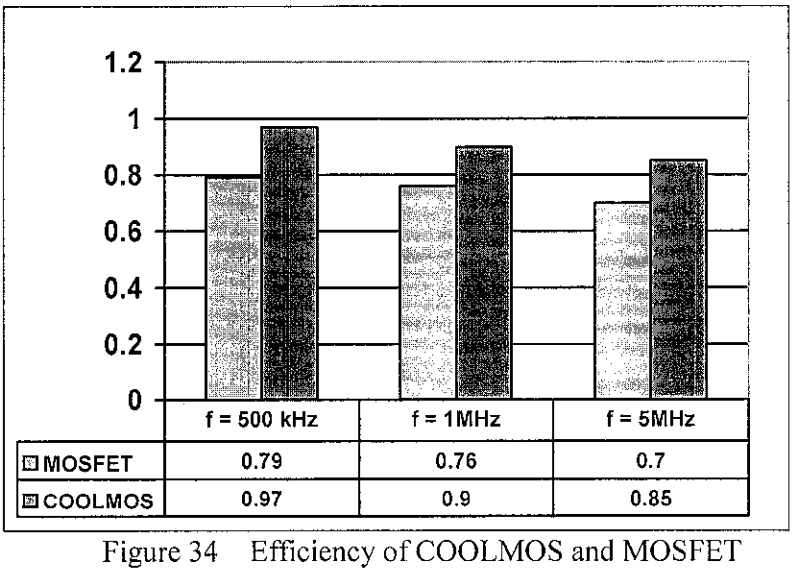


Figure 34 Efficiency of COOLMOS and MOSFET

Overall, the efficiency of COOLMOS is higher than MOSFET, thus showing that COOLMOS having a superior performances as power switches.

4.3.2 Varying D = 0.4 & 0.6 with constant f = 500 kHz and Vin = 150V.

Comparative studies are also performed by vary the duty ratio at 0.4 and 0.6. The resultant output waveforms obtained of the inverter circuit for MOSFET and COOLMOS produced are acceptable compared to theoretical. For the 0.4 duty ratio, having the 'on' proportion is 40%, instead for the 0.6 duty ratio the 'on' proportion is 60% of the total one cycle period, *T*. The resultant waveforms are as attached in Appendix 2.

Comparing the Maximum Output Voltage and Current at 3 Duty Ratio is as shown in Table 10.

Table 10 Comparing Simulation Maximum Output at 3 Duty Ratios

Duty Ratio, D	Maximum Output Voltage (V)		Maximum Output Current (A)	
	MOSFET	COOLMOS	MOSFET	COOLMOS
0.4	179.620	180.983	3.2389	3.2630
0.5	150.326	153.001	3.2869	3.3908
0.6	109.436	114.037	2.8514	2.9268

Overall it is observed that COOLMOS has a slight higher maximum output voltage compared to MOSFET. With three difference duty ratios, the output voltage becomes lower or larger than the dc input voltage. Hence, the maximum output voltage is depending on the duty ratio.

The switching energy losses at D = 0.4, 0.5 and 0.6 for both COOLMOS and MOSFET are compared in Bar Chart shown in Figure 35.

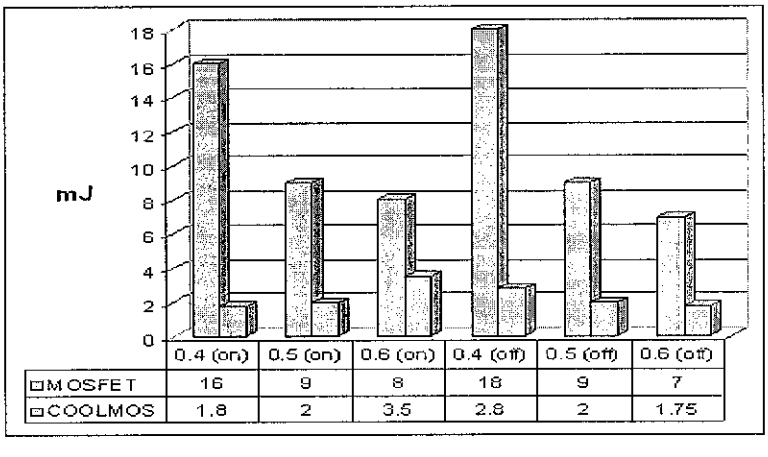


Figure 35 Bar Chart of Switching Energy Losses at D = 0.4, 0.5 and 0.6.

Basically, the pattern of switching energy losses produced as the duty ratio varies is based on the relations between pulse width, duty ratio, and frequency. Given:

Pulse Width = PW (Seconds)

Duty Ratio = D

Time = T (Seconds)

Frequency = f (Hertz)

Table 11 Switching Energy Losses and Duty Ratio

DURING TURN-ON	DURING TURN-OFF
With T is given by $T = \frac{1}{f}$	With T is given by $T = \frac{1}{f}$
Pulse Width, $PW = DT = \frac{D}{f} = \frac{D}{P/E}$	$PW = (1-D)T = \frac{(1-D)}{f} = \frac{(1-D)}{P/E}$
Thus, Energy is equals to: $E = \frac{PWxP}{D}$	Thus, Energy is equal to: $E = \frac{PWxP}{(1-D)}$

During turn-on, the energy losses during on state are directly and inversely proportional to the power losses and duty ratio respectively. As for COOLMOS switches, when the duty ratio is increases during turn-on, the switching energy losses are increase since the power losses are increase. Meanwhile for MOSFET switches, the switching energy losses are decrease since the switches experienced lesser power losses, as the duty ratio is increase. During turn-off, the equation that relates switching energy losses and duty ratio having equation *(1- D)* applies. As the duty ratio is increases, switching energy losses for both switches are decrease since the switches are having smaller power losses.

Overall, based on the simulation results obtained the switching energy losses during turn-on and turn-off of the switching energy losses experienced by MOSFET are 80% greater than COOLMOS. Thus, clarify that COOLMOS having superior performances with lowest switching energy losses.

4.3.3 Varying Vin = 200 & 400V with constant f = 500 kHz and D = 0.5

Comparative study are also performed by vary the input voltage to 200V and 400V. The resultant output voltage waveforms obtained of the inverter circuit for both switches MOSFET and COOLMOS at an input voltage of 200V are acceptable and verified with theoretical with the maximum output voltage equal to the input voltage applied. The same goes to the output current waveform having acceptable results compared to theoretical. The resultant waveforms are as attached in Appendix 2.

Comparing the Maximum Output Voltage and Current at 3 Input Voltages is as shown in Table 12.

Table 12 Comparing Simulation Maximum Output at 3 Input Voltages

Input Voltage, Vin	Maximum Output Voltage (V)		Maximum Output Current (A)	
	MOSFET	COOLMOS	MOSFET	COOLMOS
150 V	150.326	153.001	3.2869	3.3908
200 V	201.317	204.923	4.4149	4.4628
400 V	-	410.249	-	8.9663

However, for an input voltage of 400V, the resultant output voltage and current waveforms for MOSFET switches are distorted as follows:

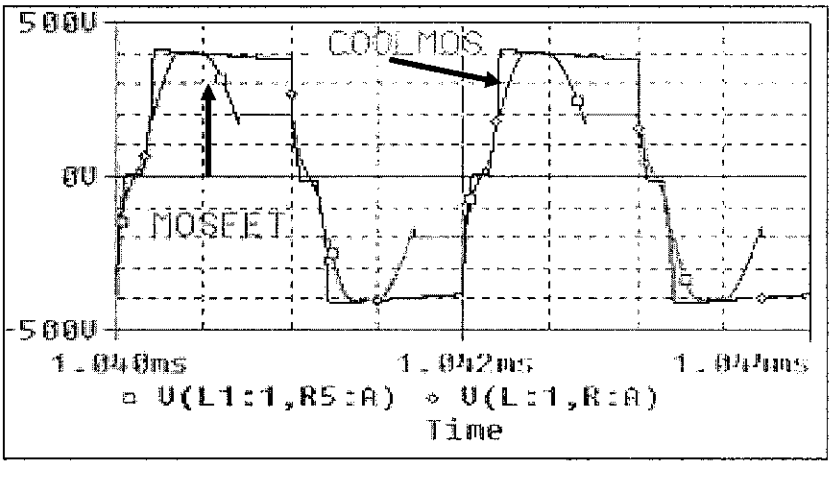


Figure 36 Output Voltage, *Vout* at *Vin* = 400V

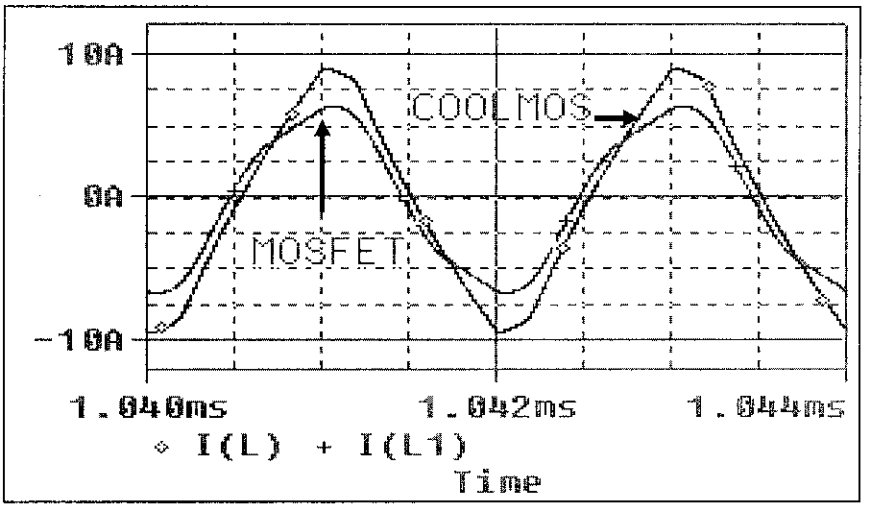


Figure 37 Output Current, *Iout* at *Vin* = 400V

At an input voltage of 200V, both switches are able to cater the high voltage input to the load. This is due to the value of input voltage, which does not exceed the rated voltage of both switches, MOSFET (V_{DSS} = 250Vdc) and COOLMOS (V_{DSS} = 600Vdc). However, at an input voltage of 400V, MOSFET output voltage and current waveforms experienced severe distortion due to the rated voltage of MOSFET (V_{DSS} = 250Vdc) has been exceeded. This condition is undesirable and may cause damaged to the internal structure of the component, MOSFET. Thus, this clarify that MOSFET are to cater the application of low voltage application only. However, COOLMOS can sustain the high voltage application higher than 600V applications, due to its characteristics having the 'super-junction' internal structure as discussed in "Literature Review and Theory" section in Chapter 2.

CHAPTER 5
CONCLUSIONS & RECOMMENDATIONS

5.1 Conclusions

As a conclusion, the objectives in performing comparative study of COOLMOS and MOSFET in a single-phase full-bridge high-frequency inverter design for UPS application are achieved. The inverter circuit is designed at high frequency of 500 kHz, 150V input voltage, 0.5-duty ratio with an isolation at the load in providing a stable AC output for UPS application. This is done while maintaining simplicity of the inverter circuitry. In this study the COOLMOS power switches are selected to be more effective than MOSFET in inverter circuit in ensuring reliability of power supply. This is selected based on performance investigation done at the output voltage and current and also the switching energy losses.

The performances of power switches COOLMOS and MOSFET are analyzed in term of lowest switching losses most preferable investigated through simulation using Cadence PSpice software and experimentally on PCB. COOLMOS power switches are concluded to be a better power switches compared to MOSFET in a high-frequency inverter design as it shows a superior performance with the percentage of switching energy losses are reduced up to more than 50% compared to MOSFET which proves by simulation and experiment in this project. Thus, COOLMOS can replace the traditional device MOSFET in high frequency inverter design for UPS application to meet the need greater efficiency power switches with low switching energy losses.

5.2 Recommendations

Recommendations for future works of this project are that as due to time constraint for the experimental implementation, a number of software such as Multisim 2001 and Ultiboard 2001 software required to self-learned which is time consuming. It is better if the Electrical and Electronics engineering Final Year project (EE FYP) committee could have a proper filing system for the students to access the manual and procedures of the software. The same goes for the manual and procedures for using the equipments. For example, different digital oscilloscope may have different operating procedures. Meanwhile, the recommendation for the project is that a number of experiment parameters are tested. With more data obtained from both simulations and experimental results, the better the analysis can be made. Thus, the behavior of the switches can be observed more clearly.

REFERENCES

[1] A. Claudio, M. Cotorogea, J. Macedonio, "Comparative *Analysis of SJ-MOSFET and Conventional MOSFET by Electrical Measurements*", Guadalajara, Mexico, October 20-24.

[2] "PQ Frequently Asked Question.html": www.linnet-tec.co.uk/html.htm

[3] Uematsu, T., Ikeda, T., Hirao, N., Totsuka, S., Ninomiya, T., Kawamoto, H., "A study of the high performance single-phase UPS", *Power Electronics Specialists Conference, 1998. PESC 98*, pp. 1872-1878 Fukuoka Japan, May 1998.

[4] Vazquez, N., Aguilar, C., Alvarez, J., Caceres, R., Barbi, I., Arau, J., "A different approach to build an uninterruptible power supply system with power factor correction", *VI IEEE International Power Electronics Congress, 1998. CIEP 98*, pp. 119-124 Morelia Mexico, Oct. 1998.

[5] Bo Zhang, Zhenxue Xu, Alex Q. Huang, "Forward and Reverse Biased Safe Operating Areas of the COOLMOS", *IEEE 31st Annual Power Electronics Specialists Conference, 2000, vol. 3*, pp. 81-86 Galway Ireland, June 2000.

[6] Issa Batarseh, "*Power Electronic Circuits*," published by John Wiley & Sons, Inc., 2004.

[7] Ned Mohan, Tore M. Undeland, William P. Robbins, "*Power Electronics: Converters, Application and Design*", published by Media Enhanced Third Edition, John Wiley & Sons, Inc.2003.

[8] Tore M. Undelan, Frode Kleveland, Pal Andreassen, "*Switching Properties of the CoolMOS Transistor*", Norweigan University of Science and Technology (NTNU).

[9] A. E. Schlog, G. Deboy yotros, "*Properties of CoolMOS Between 420K and 89K*", Power Semiconductor Devices and ISc, 1999, Pages 91-94.

[10] L. Lorenz, "*CoolMOS a new approach Toward an Idealized Power Switch*", Infeneon Technologies, Munich Germany.

[11] L. Lorenz, M. Marz, H. Zollinger, "*CoolSET-A new approach to Integrated Power Supplies*", Infeneon Technologies AG, Munich Germany.

[12] Bobby J. Daniel, Chetan D. Parikh and Makesh B. Patil, "Modeling of the COOLMOS Transistor-Part1: Device Physics", *Departmental of Electrical*

Engineering, Indian Institute of Technology, Mumbai, India. *IEEE Transactions, 2002, vol. 49, Issue 5,* pp. 916-922, May 2002

[13] L. Lorentz, G. Deboy, A. Knapp and M. Marz, "COOLMOS-a new milestone in high voltage Power MOS", *the 11th International Symposium Power Semiconductor Devices and ICs, ISPSD 99*, Toronto, Canada, May 1999.

[14] B.K. Bose, "*Modern Power Electronics Evolution, Technology and Applications*", Institute of Electrical and Electronics Engineer, Inc., 1992.

[15] Muhammad H. Rashid, "*Introduction to PSpice Using OrCAD for Circuits and Electronics,*" Third Edition, published by PEASON, Prentice Hall, 2004.

[16] Marc E. Herniter, "*Schematic Capture with Cadence PSpice,*" Second Edition, published by Prentice Hall, 2003.

[17] Siti Sakinah Sari'at, "*Comparative Study of COOLMOS and MOSFET for High Frequency Inverter Design*" Final Year project yet to be published January 2006, Universiti Teknologi PETRONAS, Tronoh, Perak.

APPENDIX 1
GANTT CHART

Gantt Chart for Final Year Project 1

NAME : 1. Nur Alina Jelani 2572

FYP TITLE : Comparative Study of Coolmos and Mosfet for High Frequency Inverter Design

NO.	DETAIL / WEEK	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1.0	*Selection of Project Topic*	▨													
	- Introductory FYP Briefing														
	- Approval on Project Title Selection														
2.0	*Preliminary Research work*	▨	▨	▨	▨										
	- Introduction														
	- Objective														
	- Project Planning														
	- List of References / Literature review														
3.0	*Submission of Preliminary Report*				O										
4.0	*Project Work*				▨	▨	▨	▨	▨	▨					
	- Reseacrh work of Reference / Literature														
	- Practical / Laboratory works														
5.0	*Submission of Progress Report*									O					
6.0	*Project Work Continue*									▨	▨	▨	▨		
7.0	*Submission of Interim Report Final Draft*												O		
8.0	*Oral Presentation*													O	
9.0	*Submission of Project Dissertation*														O

NOTE : **O** Milestone ▨ Process

Gantt Chart for Final Year Project 2

NAME : 1. Nur Alina Jelani 2572

FYP TITLE : Comparative Study of Coolmos and Mosfet for High Frequency Inverter Design

NO.	DETAIL / WEEK	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	19	21
1.0	*Project Work Continue*	▨	▨	▨	▨													
	- FamiliarizE with Multisim 2001 software																	
	- Selecting and purchasing the components																	
2.0	Submission of Progress Report 1				O													
3.0	*Project Work*				▨	▨	▨	▨	▨									
	- Construction of inverter circuit on PCB																	
4.0	Submission of Progress Report 2								O									
5.0	*Project Work continue*								▨	▨	▨	▨	▨	▨				
	- Practical/Laboratory Work																	
	- Experimentation execution																	
6.0	Submission of Draft Report													O				
7.0	*Submission of Final Report (Soft Cover)*															O		
8.0	Submission of Technical Report															O		
9.0	*Oral Presentation*																O	
10.0	*Submission of Final Report (Hard Cover)*																	O

NOTE : **O** Milestone ▨ Process

APPENDIX 2
EXTRA-INVESTIGATION SIMULATIONS

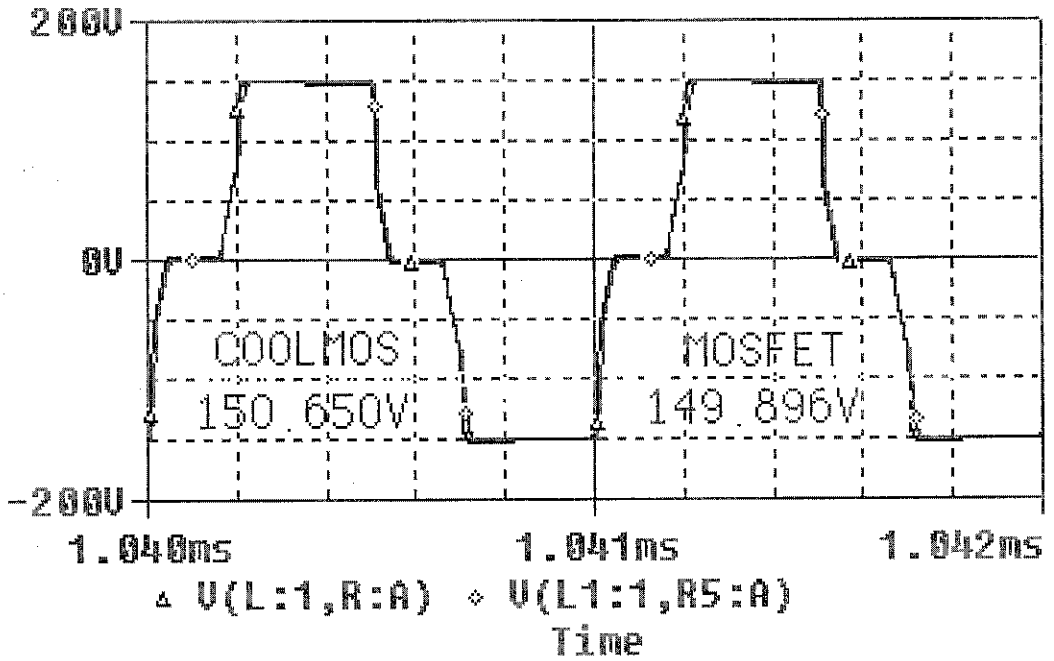


Figure 1 Output Voltage, *Vout* with *Vin* = 150V, *f* = 1 MHz and *D* = 0.5

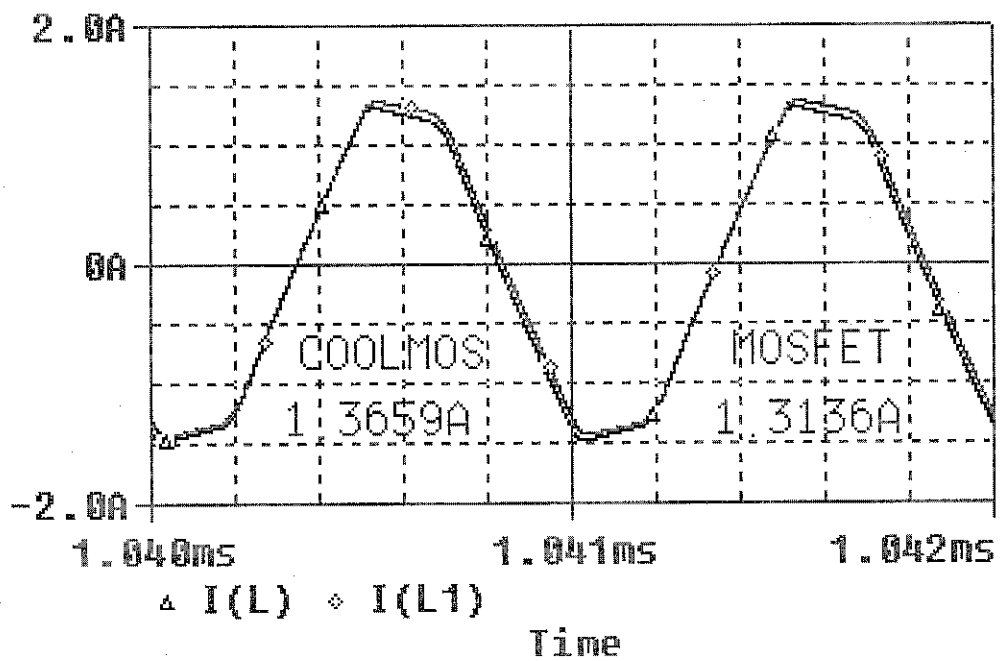


Figure 2 Output Current, *Iout* with *Vin* = 150V, *f* = 1 MHz and *D* = 0.5

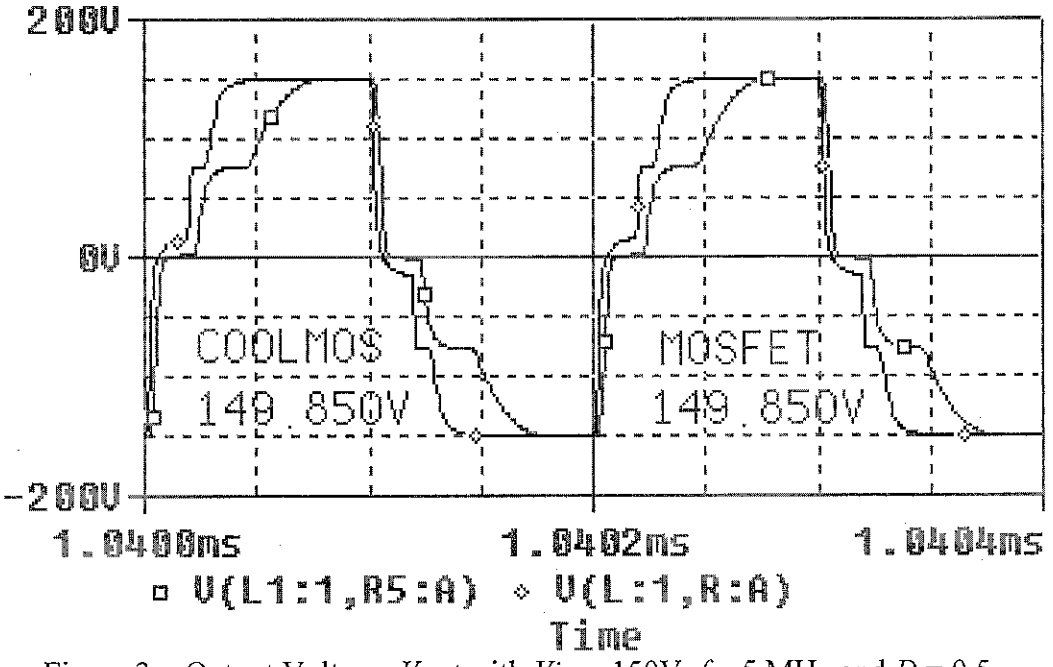


Figure 3 Output Voltage, *Vout* with *Vin* = 150V, *f* = 5 MHz and *D* = 0.5

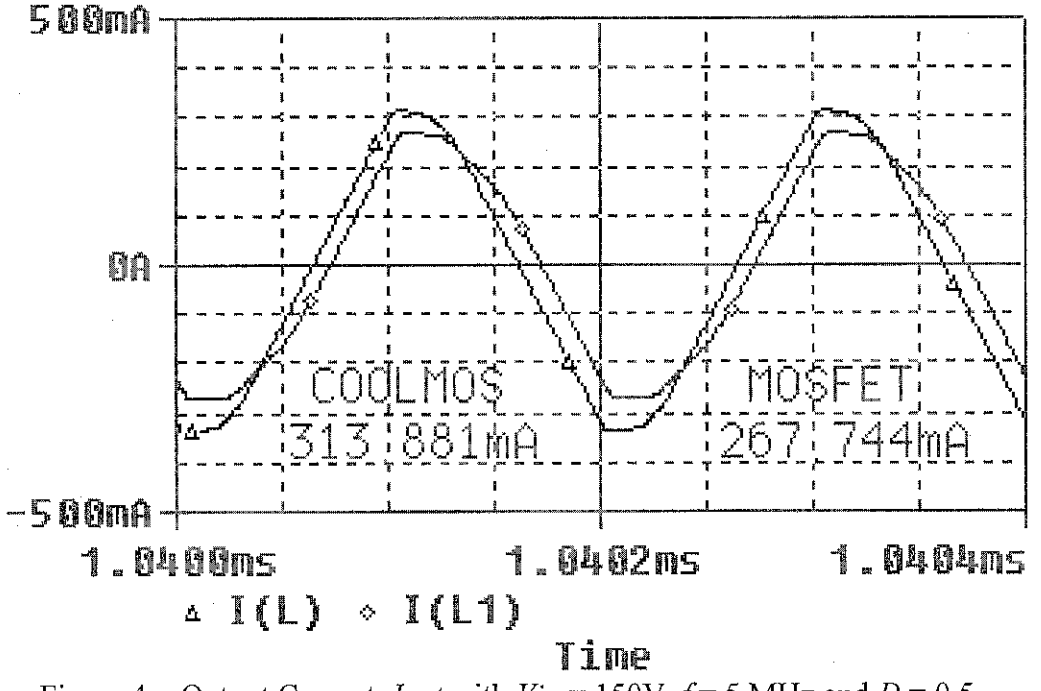


Figure 4 Output Current, *Iout* with *Vin* = 150V, *f* = 5 MHz and *D* = 0.5

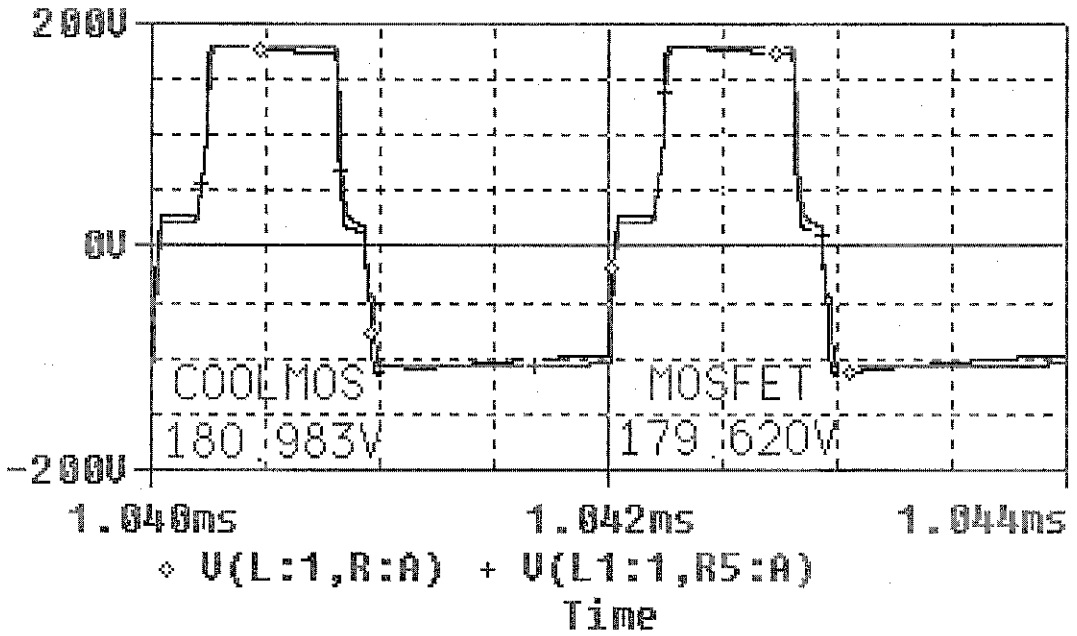


Figure 5 Output Voltage, *Vout* with *Vin* = 150V, *f* = 500 kHz and *D* = 0.4

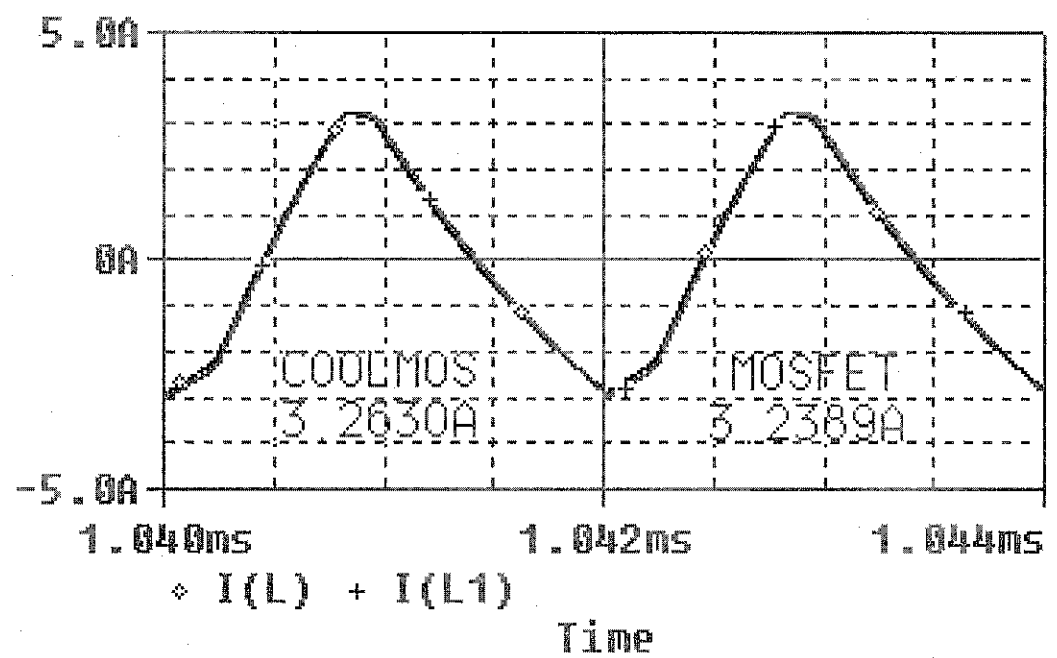


Figure 6 Output Current, *Iout* with *Vin* = 150V, *f* = 500 kHz and *D* = 0.4

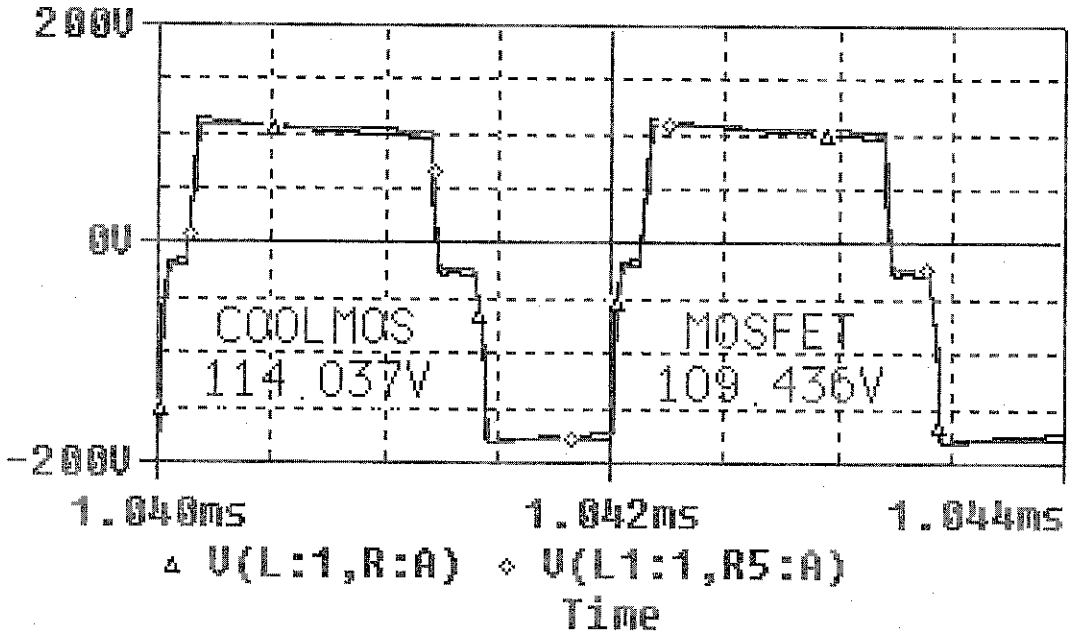


Figure 7 Output Voltage, *Vout* with *Vin* = 150V, *f* = 500 kHz and *D* = 0.6

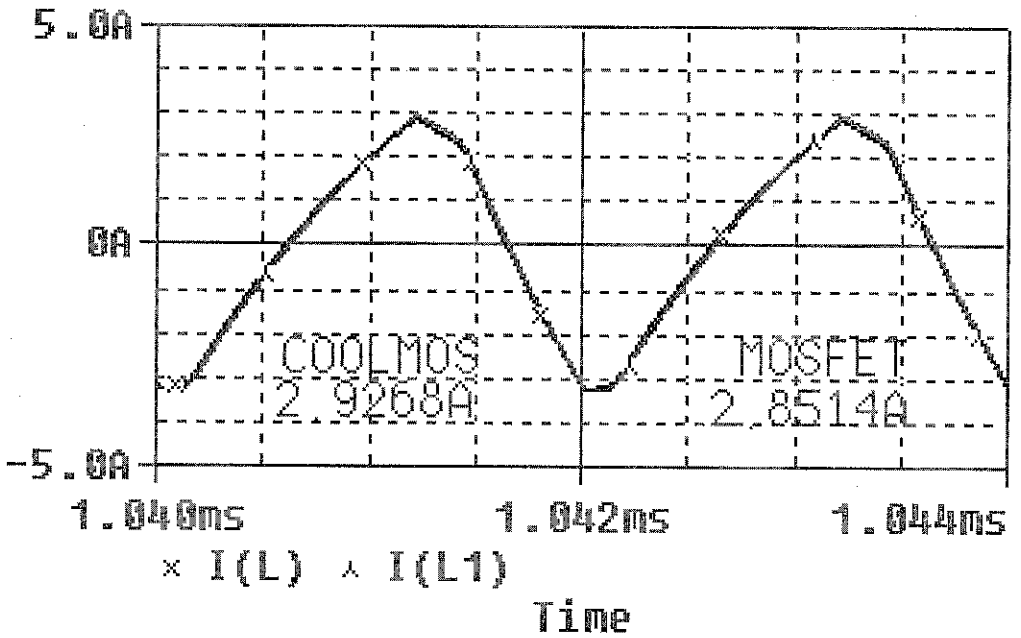


Figure 8 Output Current, *Iout* with *Vin* = 150V, *f* = 500 kHz and *D* = 0.6

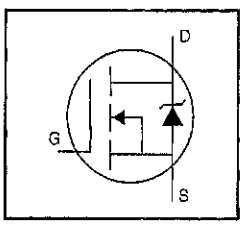
APPENDIX 3
DATASHEETS

PD-9.527B

IRF644

HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements



V_{DSS} = 250V

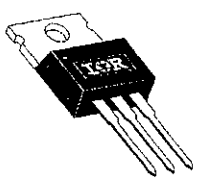
$R_{DS(on)}$ = 0.28Ω

I_D = 14A

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



TO-220AB

DATA SHEETS

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10 V	14	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10 V	8.5	
I_{DM}	Pulsed Drain Current ①	56	
P_D @ T_C = 25°C	Power Dissipation	125	W
	Linear Derating Factor	1.0	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	550	mJ
I_{AR}	Avalanche Current ①	14	A
E_{AR}	Repetitive Avalanche Energy ①	13	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.8	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	1.0	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	250	—	—	V	V_{GS}=0V, I_D= 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.34	—	V/°C	Reference to 25°C, I_D= 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.28	Ω	V_{GS}=10V, I_D=8.4A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS}=V_{GS}, I_D= 250μA
g_{fs}	Forward Transconductance	6.7	—	—	S	V_{DS}=50V, I_D=8.4A ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V_{DS}=250V, V_{GS}=0V
		—	—	250		V_{DS}=200V, V_{GS}=0V, T_J=125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS}=20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS}=-20V
Q_g	Total Gate Charge	—	—	68	nC	I_D=7.9A
Q_{gs}	Gate-to-Source Charge	—	—	11		V_{DS}=200V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	35		V_{GS}=10V See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	11	—	ns	V_{DD}=125V
t_r	Rise Time	—	24	—		I_D=7.9A
$t_{d(off)}$	Turn-Off Delay Time	—	53	—		R_G=9.1Ω
t_f	Fall Time	—	49	—		R_D=8.7Ω See Figure 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1300	—	pF	V_{GS}=0V
C_{oss}	Output Capacitance	—	330	—		V_{DS}=25V
C_{rss}	Reverse Transfer Capacitance	—	85	—		f=1.0MHz See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	14	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	56		
V_{SD}	Diode Forward Voltage	—	—	1.8	V	T_J=25°C, I_S=14A, V_{GS}=0V ④
t_{rr}	Reverse Recovery Time	—	250	500	ns	T_J=25°C, I_F=7.9A
Q_{rr}	Reverse Recovery Charge	—	2.3	4.6	μC	di/dt=100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is neglegible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

② V_{DD}=50V, starting T_J=25°C, L=4.5mH R_G=25Ω, I_{AS}=14A (See Figure 12)

③ I_{SD}≤14A, di/dt≤150A/μs, V_{DD}≤$V_{(BR)DSS}$, T_J≤150°C

④ Pulse width ≤ 300 μs; duty cycle ≤2%.

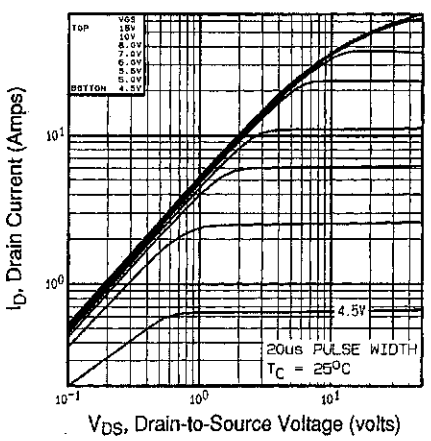


Fig 1. Typical Output Characteristics, T_C=25°C

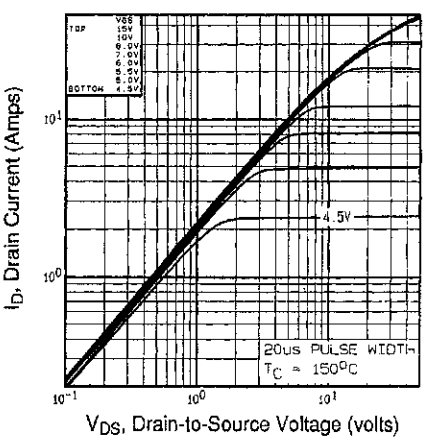


Fig 2. Typical Output Characteristics, T_C=150°C

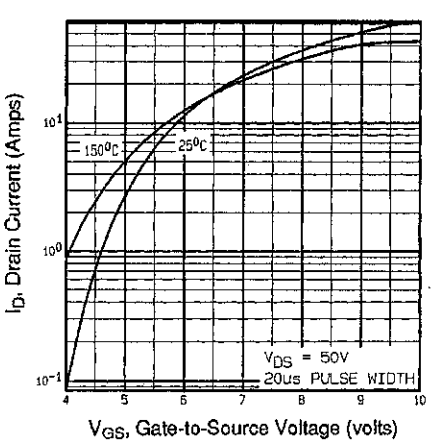


Fig 3. Typical Transfer Characteristics

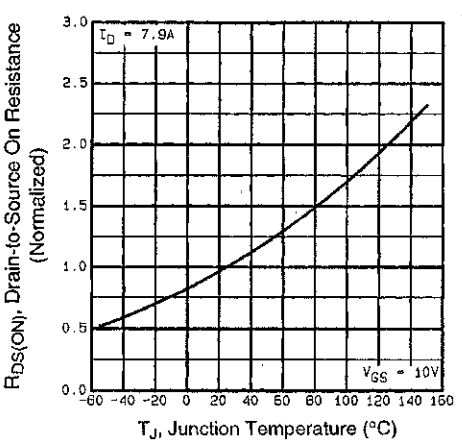


Fig 4. Normalized On-Resistance Vs. Temperature

DATA SHEETS

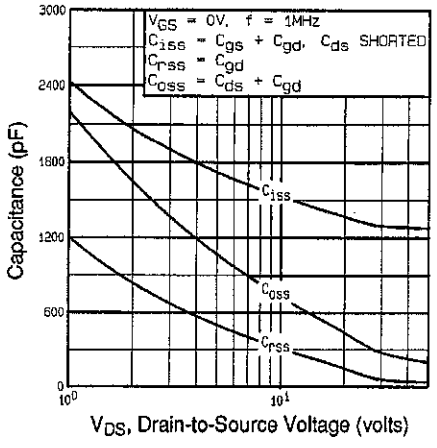


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

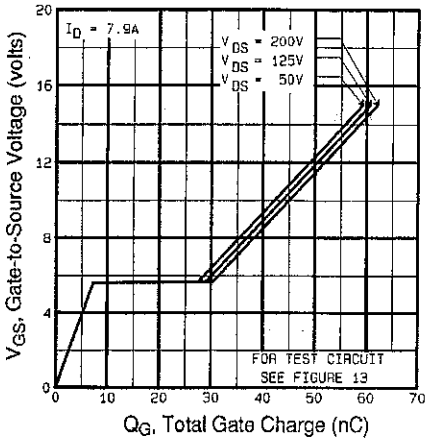


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

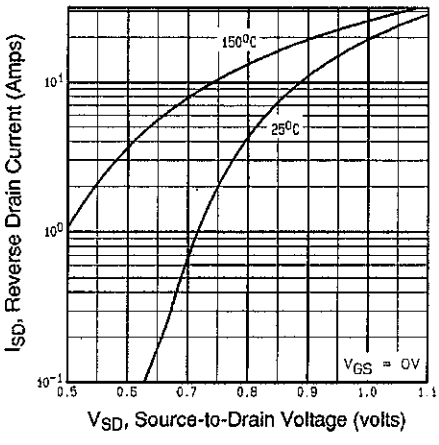


Fig 7. Typical Source-Drain Diode Forward Voltage

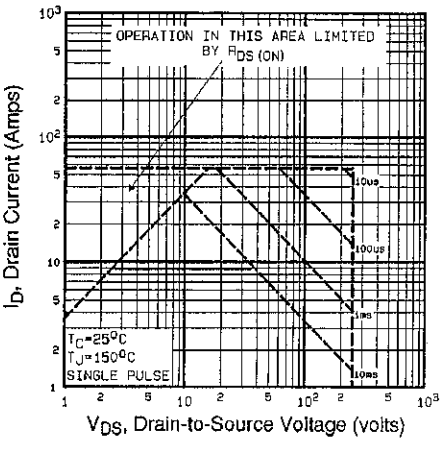


Fig 8. Maximum Safe Operating Area

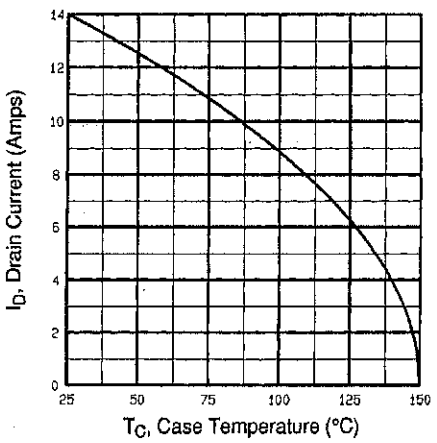


Fig 9. Maximum Drain Current Vs. Case Temperature

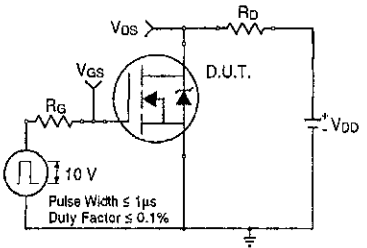


Fig 10a. Switching Time Test Circuit

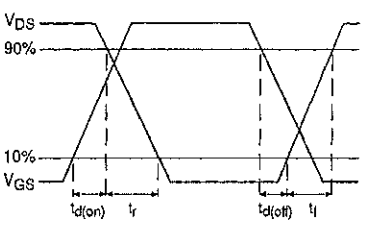


Fig 10b. Switching Time Waveforms

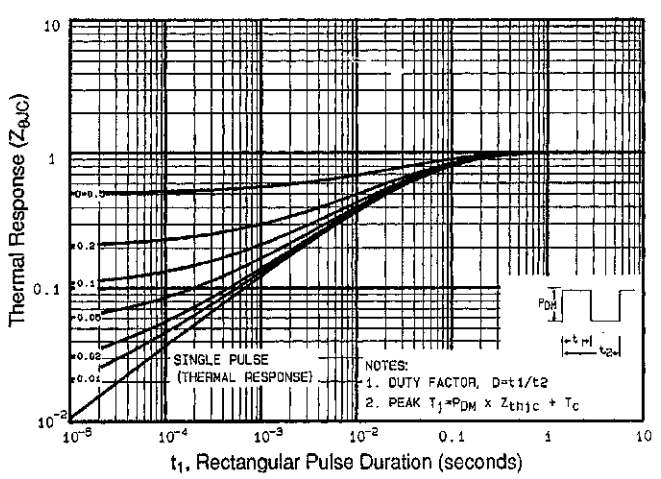


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

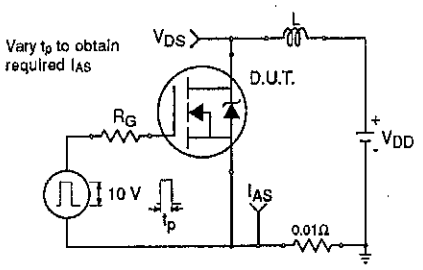


Fig 12a. Unclamped Inductive Test Circuit

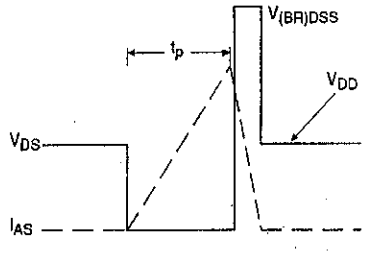


Fig 12b. Unclamped Inductive Waveforms

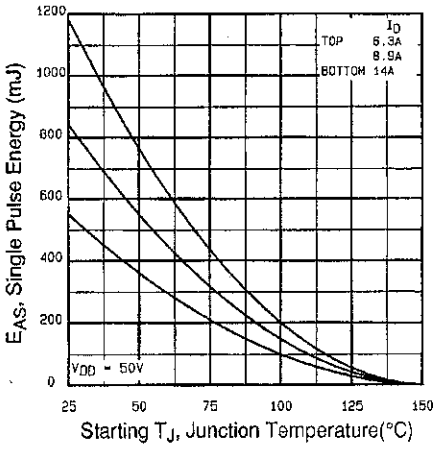


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

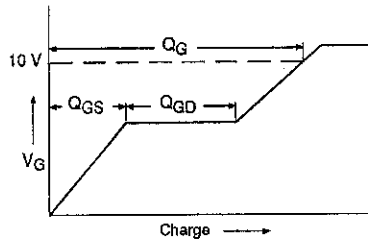


Fig 13a. Basic Gate Charge Waveform

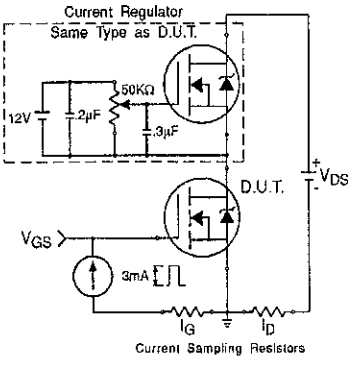


Fig 13b. Gate Charge Test Circuit

Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit – See page 1505

Appendix B: Package Outline Mechanical Drawing – See page 1509

Appendix C: Part Marking Information – See page 1516

Appendix E: Optional Leadforms – See page 1525

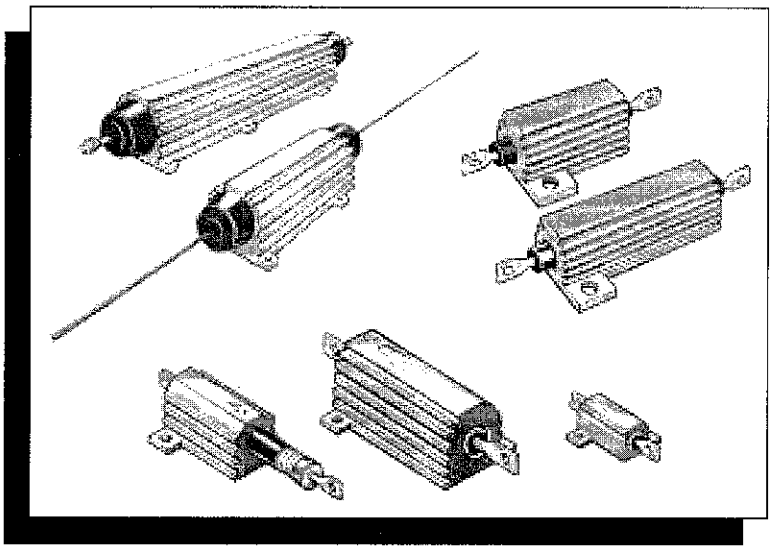
International IOR Rectifier

MEGGITT CGS

HIGH VOLTAGE RESISTORS
HIGH VALUE RESISTORS
HIGH POWER RESISTORS
ALUMINIUM CLAD RESISTORS
CURRENT SENSE RESISTORS

Aluminium Housed High Power Resistors

TYPE HS SERIES



MEGGITT CGS KEY FEATURES

- UP TO 1000 WATTS WITH HEATSINK
- LOW OHMIC VALUES AVAILABLE
- CECC - BS APPROVED
- NON INDUCTIVE + TIGHT TOLERANCE OPTIONS
- UP TO 2500 VOLTS DC
- RANGE OF CONNECTORS
- ATTRACTIVELY PRICED
- PROVEN RELIABILITY
- AVAILABLE IN DISTRIBUTION
- CUSTOM DESIGN OPPORTUNITIES WELCOMED

MEGGITT ELECTRONIC COMPONENTS

SALES ACTION DESK
TEL: (01793 611666)
FAX: (01793 611777)
EMAIL: sales@megelec.co.uk
WEB SITE: www.megelec.co.uk

LOG No L1000 ISSUE 7 7 PAGES 02-01

he HS series is the 'flagship' product of the CGS product nge.

GS are the leading European supplier of standard and custom esigned Aluminum Clad Resistors for general purpose use, ower supplies, power generation and the traction industries. he latest introduction - the HSX offers increased creepage oltage by virtue of a remodelled and extended nose cone, aking it entirely suitable for the latest VDE European Safety quirements.

he HS is a range of extemely stable, high quality wirewound sistors capable of dissipating high power in a limited space ith relatively low surface temperature. The power is rapidly ssipated as heat through the aluminium housing to a ecified heatsink.

The resistors are made from quality materials for optimum reliability and stability.

Certain styles are approved to CECC specification, others are designed to conform to the relevent MIL, CGS or customer specification.

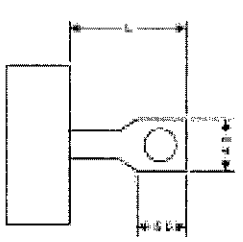
We will be happy to advice on the use of resistors for pulse applications, and to supply information for high voltage use, low ohmic value components, alternative mountings and terminations. For high power applications, a range of special designs are available, power dissipation up to 1000 Watts, insulated and designed to withstand 12KV impulse.

SA AND HSC TYPE 5 WATTS TO 300 WATTS

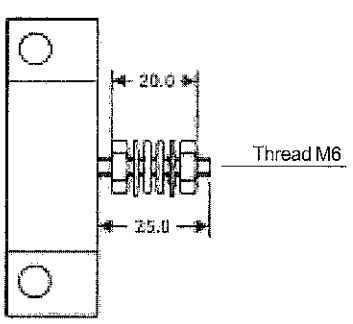
S Type	HSA 5	HSA 10	HSA 25	HSA 50	HSC 75	HSC 100	HSC 150	HSC 200	HSC 250	HSC 300
ECC 40203 - 001	AA	BA	CA	DA						
issipation at 25°C (Watts)										
/ith Heatsink	10	16	25	50	75	100	150	200	250	300
/ithout Heatsink	5.5	8	12.5	20	45	50	55	50	60	75
hmic Value										
in.	R01	R01	R01	R01	R05	R05	R10	R10	R10	R10
ax.	10K	15K	36K	100K	50K	100K	100K	50K	68K	82K
ax. Working Voltage (DC/AC RMS)										
	160	265	550	1250	1400	1900	2500	1900	2200	2500
ielectric Strength (AC Peak)										
	1400	1400	2500	2500	5000	5000	5000	5600	5600	5600
ability % Resistance										
ange, 1000 hrs.	1	1	1	1	2	2	2	3	3	3
rface Temperature Rise Mounted on Standard Heatsink										
/W	5.5	5.0	4.4	2.9	1.2	1.1	1.0	0.75	0.65	0.60
andard Heatsink										
ea, cm^2	415	415	535	535	995	995	995	3750	4765	5780
ickness, mm.	1	1	1	1	3	3	3	3	3	3
ounting Style	← 2 Hole →				← 4 Hole →			← 6Hole →		
pproximate										
eight, grams.	5	10	16	35	90	120	180	475	600	700
creased Dielectric Strength (AC Peak)						KHSA25			KHSA50	
						3500			3500	
rminations										

Types HSA5 to HSC150

Type	L
HSA5, 10	7
HSA25, 50	10
HSA75, 100, 150	8



Types HSC200, 250, 300



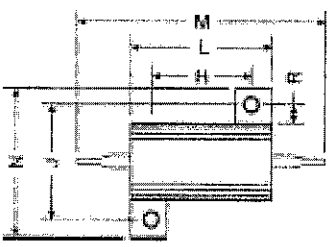
Faston connections available on request

DIMENSIONS (mm.)

HS Type	HSA 5	HSA 10	HSA 25	HSA 50	HSC 75	HSC 100	HSC 150	HSC 200	HSC 250	HSC 300
H ± 0.3	11.3	14.3	18.3	39.7	29.0	35.0	58.0	35.0	44.5	52.0
J ± 0.3	12.4	15.9	19.8	21.4	37.0	37.0	37.0	57.2	57.2	59.0
K ± 0.2	2.4	2.4	3.3	3.3	4.4	4.4	4.4	5.3	5.3	6.5
L Max.	17.0	21.0	29.0	51.0	49.0	65.5	98.0	90.0	109.0	128.0
M Max.	30.0	36.5	51.8	72.5	71.0	87.5	122.0	143.0	163.0	180.0
N Max.	17.0	21.0	28.0	30.0	47.5	47.5	47.5	73.0	73.0	73.0
P Max.	9.0	11.0	15.0	17.0	26.0	26.0	26.0	45.0	45.0	45.0
R Min.	1.9	1.9	2.8	2.8	5.0	5.0	5.0	5.6	5.6	6.0
T ± 0.5	3.4	5.2	7.2	7.9	11.5	11.5	11.5	22.2	22.2	22.2
U Max.	2.5	3.2	3.2	3.2	3.5	3.5	3.5	6.75	6.75	6.75

Note: K refers to mounting hole diameter

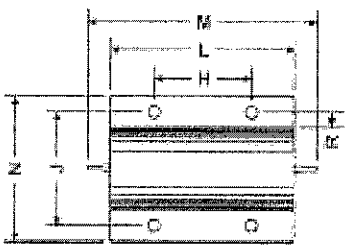
HSA5 - HSA50



2 x Mounting Hole

HSA5 - 2.4mm
HSA10 - 2.4mm
HSA25 - 3.3mm
HSA50 - 3.3mm

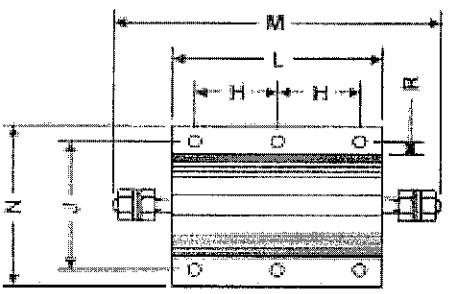
HSC75 - HSC150



4 x Mounting Hole

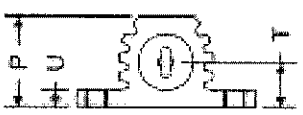
HSC75 - 4.4mm
HSC100 - 4.4mm
HSC150 - 4.4mm

HSC200+



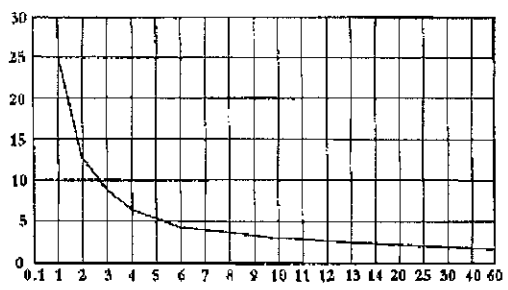
6 x Mounting Hole

HSC200 - 5.3mm
HSC250 - 5.3mm
HSC300 - 6.5mm



POWER OVERLOAD

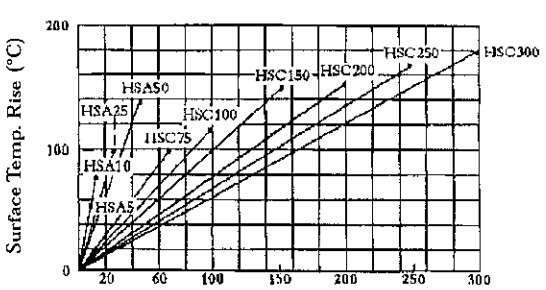
This graph indicates the amount that the rated power (at 20°C) of the standard HS series resistor may be increased for overloads of 100mS to 60S



Duration of Overload (seconds)

SURFACE TEMPERATURE RISE

For resistor mounted on standard heatsink, related to power dissipation.



Power Dissipation (Watts)

ISX TYPE 25 WATTS/50WATTS HIGH CREEP

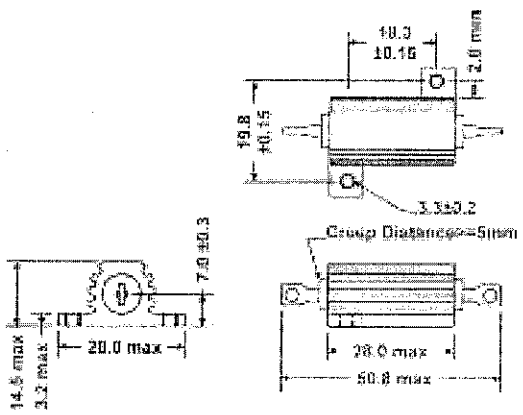
ower Dissipation on Water Cooled Heatsink: (Inlet Water Temperature (= 20°C)	25 Watts	50 Watts
esistance Range: (Tolerance ± 5% STD)	R05 to 36K	R05 to 86K
ability ΔR after 2000 hrs. @ 1½ hrs - ON, ½ hr - OFF	< = 2%	< = 2%
sulation Resistance @ 500V:	> 10,000 MΩ	> 10,000 MΩ
verload Resistance Change Δ R: 5 x Rated Power for 5 seconds	< = 1%	< = 1%
miting Element Voltage:	500V DC or AC rms	1250V DC or AC rms
olation Voltage:	3.5KV AC pk	3.5KV AC pk
mperature Coefficient:	< ± 50 ppm/°C	< ± 50 ppm/°C
nvironmental Category:	-55/200/56	-55/200/56

MECHANICAL

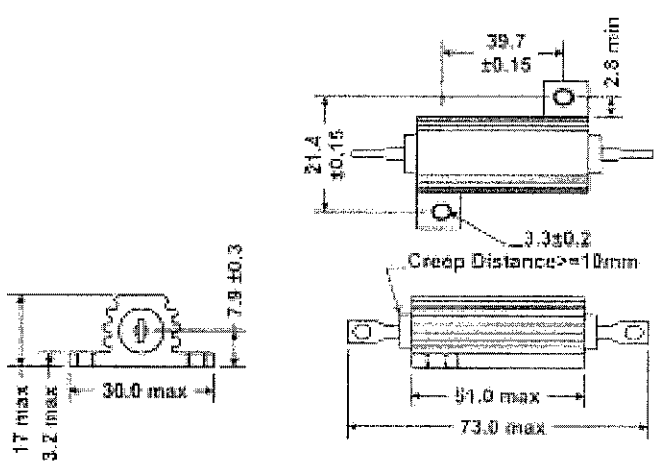
ore:	High Grade Steatite Ceramic
ap:	Stainless Steel
ement:	Ni/Cr
imary Insulation:	Epoxy Moulding
osecone:	Epoxy Moulding
ousing:	Anodised Aluminium

DIMENSIONS

ISX 25



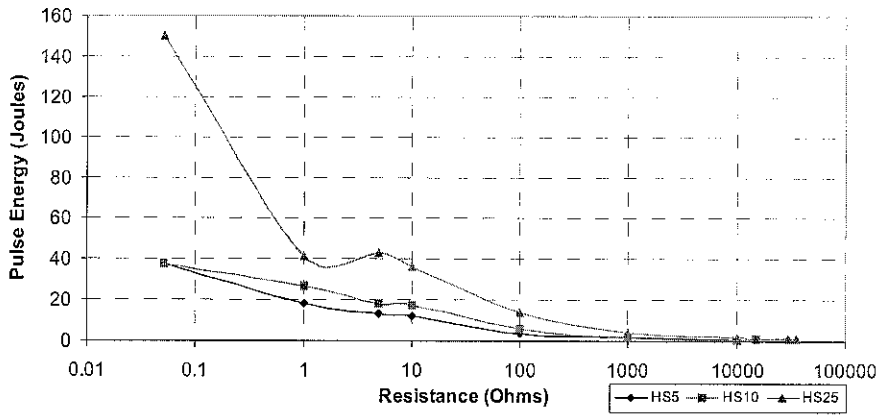
ISX 50



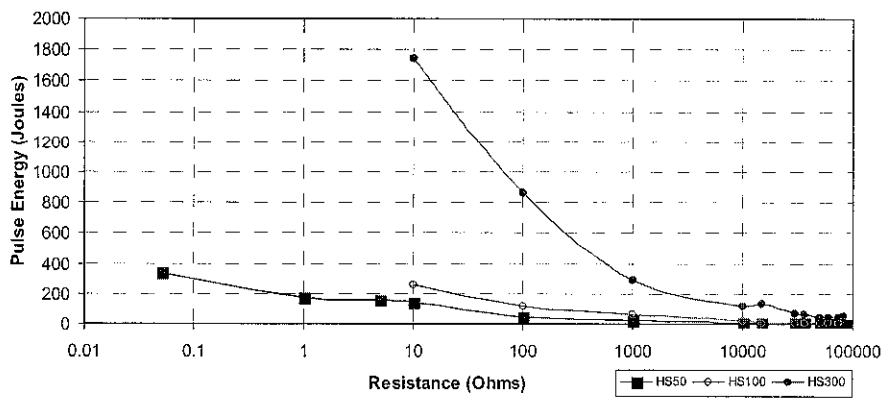
dimensions are nominal
in mm. unless otherwise
wn. Do not scale.

ULSE FORM GRAPHS FOR HSA, HSC AND HSX TYPES

Pulse Energy



Pulse Energy



IPV TYPE 500/1000 WATTS MINERAL FILLED

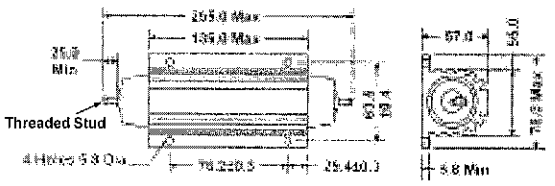
Ieggitt CGS is probably unique in offering an elegantly packaged resistor range with power dissipations up to 1000 watts, resistance nges to 50K and 12KV DC voltage proof in an elegant mineral filled aluminium case. These resistors have been specifically designed r the power generation industry but are increasingly finding applications in locomotive and other industrial markets where high ower, long life and exacting pulse requirements are key design parameters. Most resistors are tailored to user specifications and we fer a range of mounting patterns and terminal configurations.

LECTRICAL

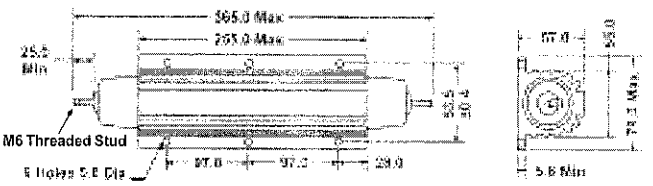
	HPV 500	HPV 1000
ower Dissipation on Water Cooled Heatsink: (Inlet Water Temperature (= 20°C)	500 Watts	1000 Watts (Max. Continuous)
esistance Range: (Tolerance ± 5% STD)	0R5 to 33K	1R0 to 50K
ability ΔR after 2000 hrs. @ 1½ hrs - ON, ½ hr - OFF	< = 2%	< = 2%
sulation Resistance @ 500V:	> 10,000 MΩ	> 10,000 MΩ
verload Resistance Change ΔR: 5 x Rated Power for 5 seconds	< = 1%	< = 1%
miting Element Voltage:	2.5KV AC rms	2.5KV AC rms (For continuous operation)
ılsed Voltage:	12KV peak	12KV peak
ılation Voltage:	4.8KV AC pk	4.8KV AC pk
ltage Proof:	6.8KV AC rms or 12KV DC	6.8KV AC rms or 12KV DC
mperature Coefficient:	< ± 100 ppm/°C	< ± 100 ppm/°C
ıvironmental Category:	-55/200/56	-55/200/56

IMENSIONS

HPV500



HPV1000

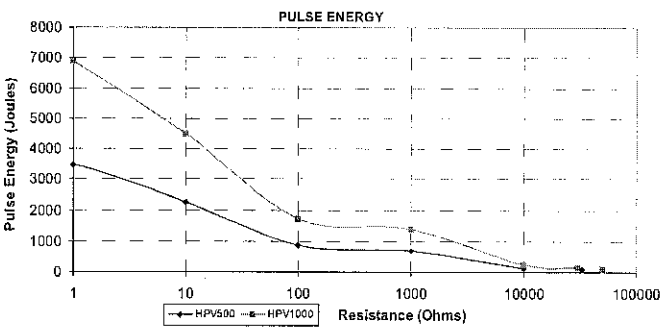


dimensions are nominal
l in mm. unless otherwise
wn. Do not scale.

ECHANICAL

ore:	High Grade Alumina
ıp:	Stainless Steel
ıd: (Threaded Terminals Only)	Stainless Steel
ement:	Ni/Cr
imary Insulation:	High Grade Alumina
osecone:	Silicone Moulding
ousing:	Aluminium Extrusion (Anodised)

ULSE FORM GRAPH



PECIAL DESIGN VARIANTS

Ohmic values from R01 dependent on size

Addition of tinned copper wire attached by high melt solder, wire supplied with or without insulation at length to suit customer.

Length of tag increased by 3mm. to provide additional hole 1.0mm. for voltage connector.

HS25 and HS50 manufactured with extended nosecones to improve creep distance.

Embedded wire terminals

HARACTERISTICS

aximium Overload
ır overloads of the order of 2 x power rating for 3 mins., 5 x power
:ing for 5 secs., or 25 x power rating for 1 second, change of resistance
less than 0.5% + 0.05 ohm maximum voltage must not exceed
aximum working voltage.

ong Term Stability
ır improvements in long term stability, resistors must be derated as
llows: for 50% of stated ΔR maximum dissipation must not exceed
% of rating; for 25% of stated ΔR maximum, dissipation must not
:eed 50% of the rating.

eat Dissipation
though the use of proprietary heatsinks with lower thermal resistance
acceptable, uprating is not recommended. The use of proprietory
atsink compound to improve thermal conductivity is recommended
r optimum performance of all sizes but essential for HSC200, HSC250,
SC300.

sulation Resistance
ry: 10,000 Megohm minimum. After moisture test: 1000 Megohm
inimum.

igh Ambient Power Dissipation
issipation derates linearly to zero at 250°C from 25°C

ecification
:mperature coefficient below 100R, 50ppm/°C.
:mperature coefficient above 100R, 30ppm/°C.
lerance, 5% standard; 10%, 3%, 2%, 1%, 0.5% & 0.25% available.
lerance for values below R10, 10% standard.

MATERIALS

Core
Ceramic, steatite or alumina depending on size.
Element
Copper nickel alloy or nickel chrome alloy.
Endcaps
Nickel iron or stainless steel.
Encapsulant
High temperature material moulding
Housing
Anodised aluminium
Stock
The HSA5, 10, 25 and 50 are stocked in selected values of the E24 series at 5% tolerance.

OW TO ORDER

HS	A	50	680R	J	X
COMMON PART	**MOUNTING STYLE**	**WATTAGE RATING AT 25°C WITH HEATSINK**	**RESISTANCE VALUE**	**TOLERANCE**	**RELEASE CONDITION**
HS - Standard KHS - Increased ielectric Strength NHS - Low nductive Winding	A - Single Opposing Mounting Feet B - Flange One Side C - Flange Two Sides X - High Creep (25 & 50 Watt only)	10 Watt = HSA5 16 Watt = HSA10 25 Watt = HSA25 50 Watt = HSA50 75 Watt = HSA75 etc....	0.1 ohm (100 mille ohms) R10 1 ohm (1000 mille ohms) 1R0 1K ohm (1000 ohms) 1K0	F - 1% G - 2% E - 3% J - 5% K - 10%	X - BS CECC No Letter - Commercial

OW TO ORDER HPV TYPES

s many applications require major or minor customisation Meggitt will normally allocate a R number special sequence to your requirement.
his is logged with drawings and maintained indefinitely to facilitate your re-order or spares requirements.
hese various specials may be low inductance types, various wire terminal types, special pulse application designs or various stud terminal types.

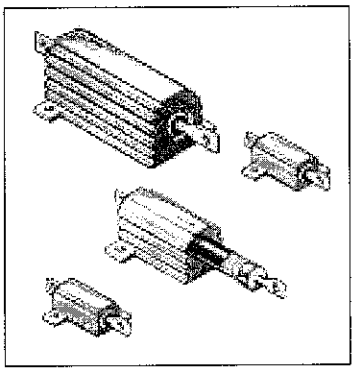
Meggitt Electronic Components Ltd. Ohmic House, Westmead Industrial Estate, Swindon, Wilts. SN5 7US
Telephone:(01793)487301(Admin.) (01793)611666 (Sales) EMail:sales@megelec.co.uk Fax:(01793) 611777

gh Power Resistors

aluminium housed for heatsinking

Key features

- **up to 300 watts with heatsink**
- **low ohmic values available**
- **CECC - BS approved**
- **non-inductive & tight tolerance available**
- **up to 2500 volts dc**
- **range of connectors**
- **custom designs welcomed**



Specification

Electrical

	HSA 5	HSA 10	HSA 25	HSA 50	HSC 75	HSC 100	HSC 150	HSC 200	HSC 250	HSC 300
CECC 40203-001	AA	BA	CA	DA						
Dissipation at 25°C (Watts)										
With Heatsink	10	16	25	50	75	100	150	200	250	300
Without Heatsink	5.5	8	12.5	20	45	50	55	50	60	75
Ohmc Value										
Min Value	R051	R051	R051	R051	R010	R010	R010	R010	R010	R010
Max Value	10K	15K	36K	86K	50K	75K	100K	50K	68K	82K
Max Working Voltage V (DC/AC RMS)	160	265	550	1250	1400	1900	2500	1900	2200	2500
Dielectric Strength V (AC Peak)	1400	1400	2500	2500	5000	5000	5000	5600	5600	5600
Stability % Resistance Change/1000Hrs	1	1	1	1	2	2	2	3	3	3
Surface Temperature Rise Mounted on Standard Heatsink °C per Watt	5.5	5.0	4.4	2.9	1.2	1.1	1.0	0.75	0.65	0.60
Standard Heatsink										
Area cm²	415	415	535	535	995	995	995	3750	4765	5780
Thickness mm	1	1	1	1	3	3	3	3	3	3
Mounting Style	<---------- 2 HOLE ---------->				<------ 4 HOLE ------>			<----- 6 HOLE ---->		
Approximate Weight Grams	5	10	16	35	90	120	180	475	600	700
Increased Dielectric Strength Option V (AC Peak)					KHSA25 3500			KHSA50 3500		

Power Resistors

e HS series

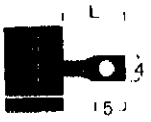
IS series is the 'flagship' ıct of the Meggitt onics power product . A major business, in this roduct, Meggitt are the ıg European supplier of ard and custom designed inium Clad Resistors, for al purpose use, power ies, generation and the ɔn industries. A particular ;itt strength in this area, is mised HS resistors where quantities are not required.

sales action desk (01793) 611666
sales fax line (01793) 611777

aluminium housed for heatsinking

Terminations

	Lmm
), 10	7
25, 50	10
75, 100, 150	8



Style	Lmm
HSC 200, 250, 300	25

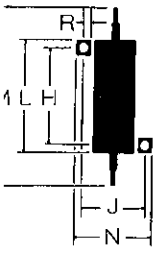
Dimensions

pe	HSA 5	HSA 10	HSA 25	HSA 50	HSC 75	HSC 100	HSC 150	HSC 200	HSC 250	HSC 300
.3	11.3	14.3	18.3	39.7	29.0	35.0	58.0	35.0	45.5	52.0
.3	12.4	15.9	19.8	21.4	37.0	37.0	37.0	57.2	57.2	59.0
2	2.4	2.4	3.3	3.3	4.4	4.4	4.4	5.3	5.3	6.5
x	17.0	21.0	29.0	51.0	49.0	65.5	98.0	90.0	109.0	128.0
ıx	30.0	36.5	51.8	72.5	71.0	87.5	122.0	143.0	163.0	180.0
.x	17.0	21.0	28.0	30.0	47.5	47.5	47.5	73.0	73.0	73.0
x	9.0	11.0	15.0	17.0	26.0	26.0	26.0	45.0	45.0	45.0
ı	1.9	1.9	2.8	2.8	5.0	5.0	5.0	5.6	5.6	6.0
5	3.4	5.2	7.2	7.9	11.5	11.5	11.5	22.2	22.2	22.2
(	2.5	3.2	3.2	3.2	3.5	3.5	3.5	6.75	6.75	6.75

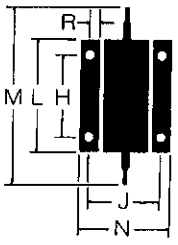
type HS series

Certain styles are approved to CECC specification, others are designed to conform to MIL, or customer specifications. We will be happy to advise on the use of resistors for pulse applications, and to supply further information for high voltage use, low inductive and low ohmic value components, alternative mountings and terminations. A full range of HS resistors, is available from Meggitt distributors.

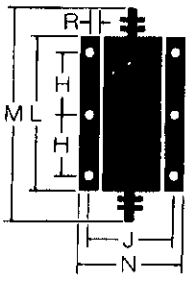
:SA5 to HSA50



HSC75 to HSC150



HSC200 to HSC300



How To Order

HS — A — 25

Common Part	Mounting Style	Size
HS - Standard KHS - High Voltage * NHS - Low Inductance Winding	A - Single Opposing Mounting Feet B - Flange One Side C - Flange Two Sides	HSA5 - 10 Watts HSA10 - 16 Watts HSA25 - 25 Watts etc .....

1R0 — J — X

Resistance Value			Tolerance	Release Condition
0.1 ohm	(100 milli ohms)	R10	F * 1%	X - BS CECC
1.0 ohm	(1000 milli ohms)	1R0	E - 3%	- - No Letter Commercial
1K ohm	(1000 ohms)	1K0	J - 5%	
			K - 10%	

* - KHS Applies to 25 Watt and 50 Watts Styles Only

Please Request Full Data Sheet L1000

MEGGITT ELECTRONIC COMPONENTS

ɔW TO ORDER

itary Type Designation: Styles CK05, CK06

· values, tolerances, voltages, sizes, configurations and lectrics not shown, contact AVX facilities directly information.

ɪt Number Example CK05 BX 104 K

ɪle

tage-Temperature Limits

pacitance Code

pacitance Tolerance

ɹ Part No. Codes

ɪle: **CK** = General purpose, ceramic dielectric, fixed capacitors.
05 = Remaining two numbers identify shape and dimension.

tage-Temperature Limits:
irst letter identifies temperature range.
B = -55°C to +125°C

econd letter identifies voltage-temperature coefficient.

Capacitance Change with Reference to 25°C		
Second Letter	**No Voltage**	**Rated Voltage**
X	+15, -15%	+15, -25%

. Fig. Capacitance and Multiplier:
Ɛirst two digits are the significant figures of capacitance. Ɪhird digit indicates the additional number of zeros. Ɛor example, order 100,000 pF as 104.

pacitance Tolerances: K = ±10%, M = ±20%

ɔkaging: CK05 1000 per bag
CK06 1000 per bag
Radial tape and reel packaging available upon request (2500 pcs./reel).

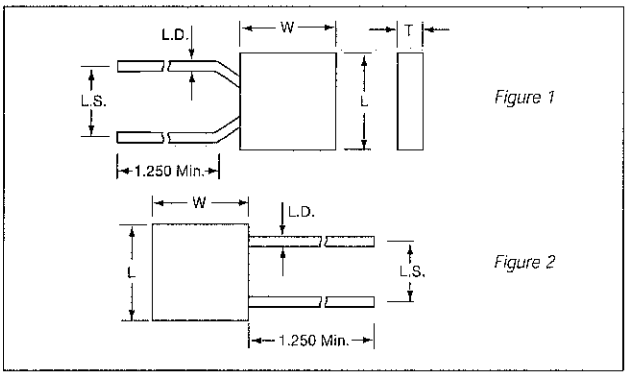


Figure 1

Figure 2

SIZE SPECIFICATIONS

Dimensions: Millimeters (Inches)

Case Size	Per MIL Spec	
MIL-C-11015	CK05 (Fig. 1)	CK06 (Fig. 2)
Length (L)	4.83±.25 (.190±.010)	7.37±.25 (.290±.010)
Width (W)	4.83±.25 (.190±.010)	7.37±.25 (.290±.010)
Thickness (T)	2.29±.25 (.090±.010)	2.29±.25 (.090±.010)
Lead Spacing (L.S.)	5.08±.38 (.200±.015)	5.08±.38 (.200±.015)
Lead Diameter (L.D.)	.64±.05 (.025±.002)	.64±.05 (.025±.002)

ary Part Number Identification CK05 and CK06

Military Type Designation	Capacitance (pF)	Capacitance Tolerance	WVDC
	CK05 (BX)		
CK05BX100_	10	K, M	200
CK05BX120K_	12	K	200
CK05BX150_	15	K, M	200
CK05BX180K_	18	K	200
CK05BX220_	22	K, M	200
CK05BX270K_	27	K	200
CK05BX330_	33	K, M	200
CK05BX390K_	39	K	200
CK05BX470_	47	K, M	200
CK05BX560K_	56	K	200
CK05BX680_	68	K, M	200
CK05BX820K_	82	K	200
CK05BX101_	100	K, M	200
CK05BX121K_	120	K	200
CK05BX151_	150	K, M	200
CK05BX181K_	180	K	200
CK05BX221_	220	K, M	200
CK05BX271K_	270	K	200
CK05BX331_	330	K, M	200
CK05BX391K_	390	K	200
CK05BX471_	470	K, M	200
CK05BX561K_	560	K	200
CK05BX681_	680	K, M	200
CK05BX821K_	820	K	200
CK05BX102_	1,000	K, M	200
CK05BX122_	1,200	K	100
CK05BX152_	1,500	K, M	100
CK05BX182K_	1,800	K	100
CK05BX222_	2,200	K, M	100
CK05BX272K_	2,700	K	100
CK05BX332_	3,300	K, M	100
CK05BX392K_	3,900	K	100
CK05BX472_	4,700	K, M	100
CK05BX562K_	5,600	K	100
CK05BX682_	6,800	K, M	100
CK05BX822K_	8,200	K	100
CK05BX103_	10,000	K, M	100
CK05BX123K_	12,000	K	50
CK05BX153_	15,000	K, M	50
CK05BX183K_	18,000	K	50
CK05BX223_	22,000	K, M	50
CK05BX273K_	27,000	K	50
CK05BX333_	33,000	K, M	50
CK05BX393K_	39,000	K	50
CK05BX473_	47,000	K, M	50
CK05BX563K_	56,000	K	50
CK05BX683_	68,000	K, M	50
CK05BX823K_	82,000	K	50
CK05BX104_	100,000	K, M	50

Add Capacitance Tolerance Letter K = ±10% or M = ±20%

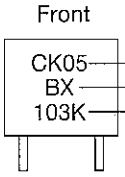
Military Type Designation	Capacitance (pF)	Capacitance Tolerance	WVDC
	CK06 (BX)		
CK06BX122K_	1,200	K	200
CK06BX152_	1,500	K, M	200
CK06BX182K_	1,800	K	200
CK06BX222_	2,200	K, M	200
CK06BX272K_	2,700	K	200
CK06BX332_	3,300	K, M	200
CK06BX392K_	3,900	K	200
CK06BX472_	4,700	K, M	200
CK06BX562K_	5,600	K	200
CK06BX682_	6,800	K, M	200
CK06BX822K_	8,200	K	200
CK06BX103_	10,000	K, M	200
CK06BX123K_	12,000	K	100
CK06BX153_	15,000	K, M	100
CK06BX183K_	18,000	K	100
CK06BX223_	22,000	K, M	100
CK06BX273K_	27,000	K	100
CK06BX333_	33,000	K, M	100
CK06BX393K_	39,000	K	100
CK06BX473_	47,000	K, M	100
CK06BX563K_	56,000	K	100
CK06BX683_	68,000	K, M	100
CK06BX823K_	82,000	K	100
CK06BX104_	100,000	K, M	100
CK06BX124K_	120,000	K	50
CK06BX154_	150,000	K, M	50
CK06BX184K_	180,000	K	50
CK06BX224_	220,000	K, M	50
CK06BX274K_	270,000	K	50
CK06BX334_	330,000	K, M	50
CK06BX394K_	390,000	K	50
CK06BX474_	470,000	K, M	50
CK06BX564K_	560,000	K	50
CK06BX684_	680,000	K, M	50
CK06BX824K_	820,000	K	50
CK06BX105_	1.0 mfd	K, M	50

Add Capacitance Tolerance Letter K = ±10% or M = ±20%

?KING

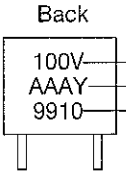
CK05/CK06

Front



Style
Temperature Characteristic
Capacitance Value
(3 digit code) and Capacitance Tolerance

Back



Voltage Rating
A for AVX; Plant I.D. (X); Lot Code (XX)
Date Code