COMPARATIVE STUDY OF COOLMOS AND MOSFET FOR HIGH FREQUENCY INVERTER DESIGN

By

SITI SAKINAH SARI'AT

FINAL REPORT

Submitted to the Electrical & Electronics Engineering Programme
in Partial Fulfillment of the Requirements
for the Degree
Bachelor of Engineering (Hons)
(Electrical & Electronics Engineering)

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CERTIFICATION OF APPROVAL

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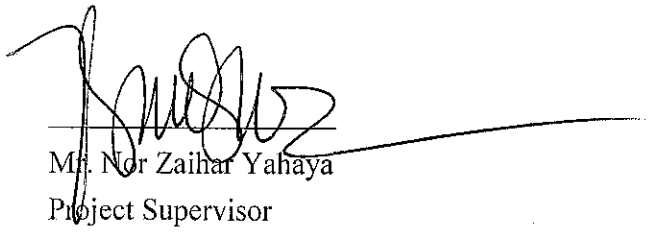
Approved:



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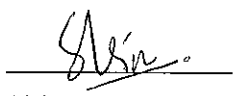
December 2005

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.



Siti Sakinah Sari'at

ABSTRACT

In this project, effectiveness performances of COOLMOS and MOSFET switches in a single phase full bridge high frequency inverter circuit are investigated and compared in terms of output voltage and current waveform, switching losses and efficiency of the circuit catering for Uninterruptible Power Supply (UPS) system. Recently, semiconductor field came out with the latest technology of MOSFET family known as COOLMOS which is specified by the manufacturers to have lower switching losses with greater efficiency at lower cost. Therefore, the superior performances of COOLMOS over MOSFET in a single phase full bridge high frequency inverter design for UPS application are to be verified. The project is executed using simulation in the Cadence PSpice 14.2 software as well as by experimentation on the Printed Circuit Board (PCB) layout. The layout of inverter circuit configuration is designed by using Multisim and transferred to the Ultiboard 2001 software. The simulation outcomes are confirmed to be as per theoretical study before comparing them with the experimentation results. From the simulation investigation of both switches, COOLMOS indicates better performances by having switching energy losses are reduced up to more than 50% compared to MOSFET and able to cater for high voltage application. Consequently from the experimentation the PCB layout, COOLMOS is validated to have superior performances compared to MOSFET in terms of experiencing lower switching energy losses.

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LIST OF ABBREVIATIONS

List of abbreviations used are as follows:

AC	Alternating Current
A/D	Analog to Digital
BJT	Bipolar Junction Transistor
COOLMOS	Cool Metal Oxide Semiconductor
D	Duty Ratio
DC	Direct Current
E	Switching Energy Losses
f	Frequency
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
S	Semiconductor Switch
UPS	Uninterruptible Power Supply
VSI	Voltage-Source inverter

CHAPTER 1
INTRODUCTION

1.1 Background of Study

In this project, a design for a 300W uncontrolled isolated inverter circuit is done for the conversion of energy from direct current (DC) power supply to alternating current (AC) power to be used in a high power UPS application. The configuration is achieved using a single phase full bridge high frequency inverter with MOSFET and COOLMOS acts as the switches. The switching frequency of this inverter circuit is selected to be 500 kHz since at this frequency the acoustic noise and distortion at the AC outputs can be eliminated. The inverter circuit is operated with a constant input of 150V-dc supply to fulfill the demands of a high rated voltage for the UPS application. The duty ratio of the switches is fifty percent (50%) as to generate an equal proportion of positive and negative cycle at the AC output waveforms.

Basically, this project is carried out by two students whereby the author is focusing on the effectiveness performances of COOLMOS switches in the single phase full bridge high frequency inverter design. Meanwhile, the investigation of MOSFET performances is done by the author's project partner, Nur Alina Jelani. The effectiveness performances of COOLMOS and MOSFET switches are investigated, analyzed and compared in terms of its output voltage and current waveform, switching losses as well as the efficiency of the inverter circuit. MOSFET is a commonly use power switches. Meanwhile, COOLMOS is the latest revolutionary technology specifically designed for a higher voltage application (> 600 Volts).

At the end of this project, the most efficient switches between COOLMOS and MOSFET performed in the inverter circuit for UPS application is concluded by comparing the switching energy losses as well as the efficiency.

1.2 Problem Statement

The reliability of power supply is very important since minor disturbances may cause severe damage to the electronic components. Power problems may cause unplanned shutdowns and leads to the important data losses. These problems will affect the profitability of an organization especially the manufacturing company. This issue might not be affected much on residential consumers but it becomes a major concern for the industrial consumers in a public service industry, government department, telecommunications and security establishments.

Power quality study has been widely done by various organizations and it reveals that the average computer system is subjected to 289 potentially damaging power disturbances per year [1]. Therefore, one of the best solutions to overcome this problem is by providing the system with highly reliable and capable UPS which will maintain a stable power supply regardless of the mains supply quality. Here, an inverter circuit which is part of the UPS system is studied in order to produce a highly reliable UPS system. Based on some researches, there have been many ways of approaches in the inverter circuit design as to provide an efficient AC outputs. One of the approaches having simple circuit configuration and highly efficient, but unsafe since the front-end and the inverter stages share the power switches without providing an isolation between the main line and the load [2]. However, there is an existing good dynamic response of inverter which offers isolation between main line, the battery set and the load but the circuit and operation topology is rather complex [3]. Isolation between the main line and the load is needed if the inverter circuit is operated at the DC power supply of higher than 60V mainly for the load protection purposes. Thus, in this project isolation transformer is implemented between the main line and the load while maintaining the simplicity of the circuit configuration.

Another solution to provide a highly reliable UPS system is by selecting the most efficient switches that has lower switching energy losses in the inverter circuit design. Therefore, a comparison study of COOLMOS and MOSFET performances shall be performed to choose the best switches to be used in the inverter circuit of UPS system. Previously, MOSFET is known to have low conduction losses. Meanwhile, COOLMOS is actually a high voltage of MOSFETs, 600V a recent new device based on concept called the super junction (SJ), [4].

1.3 Objectives and Scope of Study

The objectives of this project is to perform a comparison study between two semiconductor switches COOLMOS and MOSFET performances by using a single phase full bridge high frequency inverter circuit for UPS application as the medium. The inverter circuit is operated at an input of 150V-dc, switching frequency of 500 kHz and under fifty percent (50%) duty ratio. The performances of the switches is investigated and analyzed via simulations using Cadence PSpice 14.2 software and via hardware experimentation on the PCB layout. The effectiveness performances of COOLMOS and MOSFET switches in a single phase full bridge high frequency inverter circuit are investigated and compared in terms of output voltage and current waveform, switching losses as well as the efficiency.

1.3.1 Objectives

1. To construct a single phase full bridge high frequency inverter circuit by using COOLMOS as the switches with isolation in between the main line and the load while maintaining the simplicity of circuit configuration and operation.
2. To operate the single phase full bridge high frequency inverter circuit with a base parameters of input DC supply of 150V, switching frequency of 500 kHz and duty ratio of 0.5.
3. To perform a comparison study of COOLMOS and MOSFET performances as the switches in a high frequency inverter circuit via:

    a. Simulations using Cadence PSpice 14.2 software

    In the simulations, COOLMOS performances such as the resultant output voltage and current waveform, the switching energy losses and efficiency are investigated at varied input DC supply, duty ratio and switching frequency.

    b. Experimentation on the PCB layout

    In the experiments, COOLMOS performances such as the resultant output voltage and current waveform and the switching energy losses are investigated at an input DC supply of 150V, switching frequency of 500 kHz and duty ratio of 0.5.

1.3.2 Scope of Study

Basically, this project deals with the exploitation of power and analogue electronics area of specialization. The scope covers the understanding of inverter circuit design and operations, the characteristics of COOLMOS, and also incorporates of some relevant mathematical formula analysis. The scope also covers the interpreting of datasheet and specifications of components and hardware involved in the inverter circuit design. Lastly, the scope of study covers the knowledge on using Cadence PSpice, Multisim and Ultiboard 2001 software for simulation as well as for experiments implementation.

1.3.3 Gantt Chart

The process of completing this project is according to the activities planned in the Gantt chart. This is to ensure the project is successfully reached its goals within the time specified. The Gantt chart is as attached in Appendix 1.

CHAPTER 2
LITERATURE REVIEW AND THEORY

Inverter circuits are used to deliver power from a DC source to a passive or active load by means of using the gate-driven semiconductor devices as switches, which in this project COOLMOS and MOSFET. DC-AC inverters are used in applications where the only source available is a fixed DC source and the system needs an AC load such as aircraft power supplies and variable-speed AC motor drives. Each and every year, the number of researches and studies related on the latest advancement design of a high frequency inverter circuit is kept increasing. This is due to the high demand for DC-AC high frequency inverter circuit that produces a stable, reliable and efficient AC output for UPS application. Thus to fulfill the demand, a comparative study between COOLMOS and MOSFET performances in a high frequency inverter circuit design is carried out to ensure the UPS system able to produce a fixed AC frequency output even when the main power grid system is out.

2.1 Inverter Circuit Design

The full bridge circuit configuration for a voltage-source inverter under resistive and inductive (R-L) load is shown as in Figure 1.

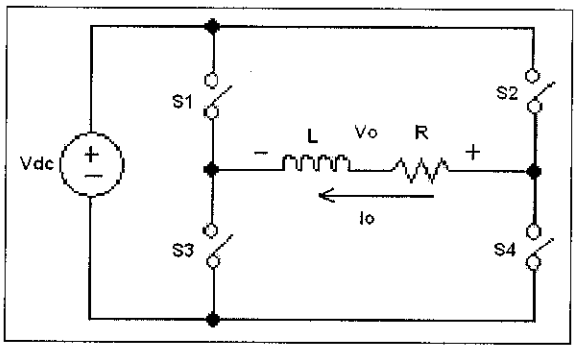


Figure 1 Single phase full bridge inverter circuit of R-L load

The inverter is normally employs a bidirectional switching device that can be gate-controlled to interrupt current flow. These switching devices are the gate-driven types such as Insulated-gate-bipolar transistors (IGBTs), Bipolar-junction-transistors (BJTs), MOSFETs or COOLMOS. The example of COOLMOS implementation as switches in the inverter circuit is shown as in Figure 2.

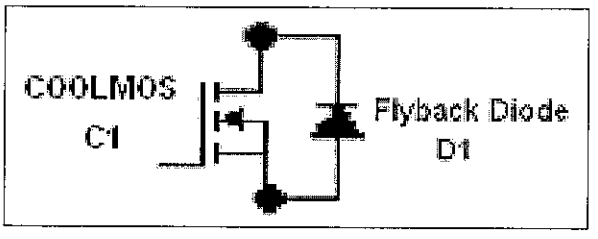


Figure 2 COOLMOS implementation as switches in an inverter circuit

The output voltage of inverter circuit depends on the duty cycle and switching sequences of S_1, S_2, S_3 and S_4. If S_2-S_3 and S_1-S_4 are switched on and off at a 50% duty cycle as shown in Figure 3, the output voltage, shown in Figure 4(a) is a symmetrical squarewave whose maximum and minimum voltage is equal to DC input supply. S_2-S_3 is turned on during the first half cycle of complete period, T. Meanwhile S_1-S_4 is turned on during the other half cycle of the period, T.

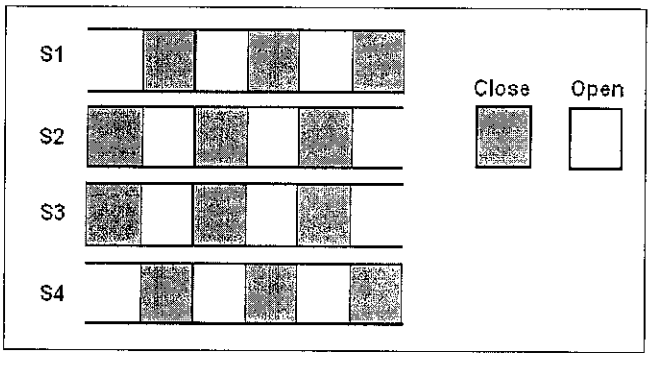


Figure 3 Switching sequences of full bridge inverter circuit

The voltage has two states of output which is positive and negative value of DC input voltage summarized as below:

$$V_o = +V_{dc} \text{ during } 0 < t < T/2$$

$$V_o = -V_{dc} \text{ during } T/2 < t < T$$

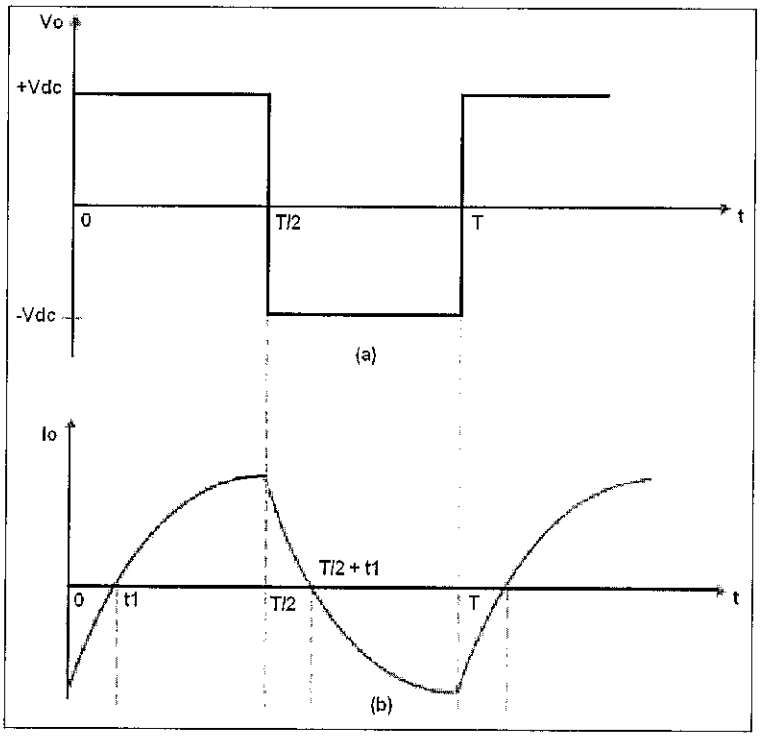


Figure 4 Output voltage and current waveform of inverter at 50% duty cycle, [5]

When S_2-S_3 is turned on, current is flowing from the positive DC input terminal to the load, thus the output voltage is equal to positive DC supply voltage. On the other hand when S_1-S_4 is turned on, current is now flowing from the negative terminal of DC input voltage to the load, therefore the output voltage is now equal to negative of DC supply voltage.

Presume the inverter operates in the steady state and its inductor current waveform is shown in Figure 4(b). For $0 \le t < t_1$, the inductor current is negative since during S_2-S_3 is on the current actually flows in the reverse direction through the flyback diode of the switches as shown in Figure 2. In the steady state operation, the following conditions must hold:

$$i_L(0) = -i_L(T/2)$$

$$i_L(0) = i_L(T)$$

The value of initial inductor current is calculated by using the given formula:

$$I_L(0) = -\frac{V_{dc}}{R}\frac{1-e^{-\frac{T}{2\tau}}}{1+e^{-\frac{T}{2\tau}}}$$

where $\tau = \frac{L}{R}$ and $T = \frac{1}{f}$

2.2 Characteristics of COOLMOS

A few characteristics of COOLMOS have been studied as to understand the internal structures and behaviors, advantages as well as the disadvantages of the switches in the inverter circuit operation. The characteristics of both switches are compared as listed in Table 1.

Table 1 Characteristics of COOLMOS

COOLMOS
➢ Blocking voltage V_{ds} of higher than 600V ➢ Periodic avalanche rated ➢ Extreme *dV/dt* rating ➢ Extremely fast and controllable switching ➢ Low on-state resistance by factor up to 7

In the semiconductor field, MOSFETs are known to have minimal resistance when the device is conducting and able to sustain high voltage when the device is off. It is widely used in various high frequency and low power applications as it is very easy to drive and switches fast. However, the switch has the limitation in a high voltage levels due to its poor conduction properties. High voltage application requires low doping concentration and reduces the thickness of the epitaxial layer, n^- in order to maintain the electric field below the semiconductor breakdown value.

Recently, the latest technology for high voltage power MOSFETs known as COOLMOS has been introduced. COOLMOS virtually combines the low switching losses of a MOSFET with the on-state losses of an IGBT. In the COOLMOS device, the drift region of the conventional power MOSFET is replaced by a "super-junction" which consists of the combination of n^- and p^- strips in parallel as shown in Figure 5.

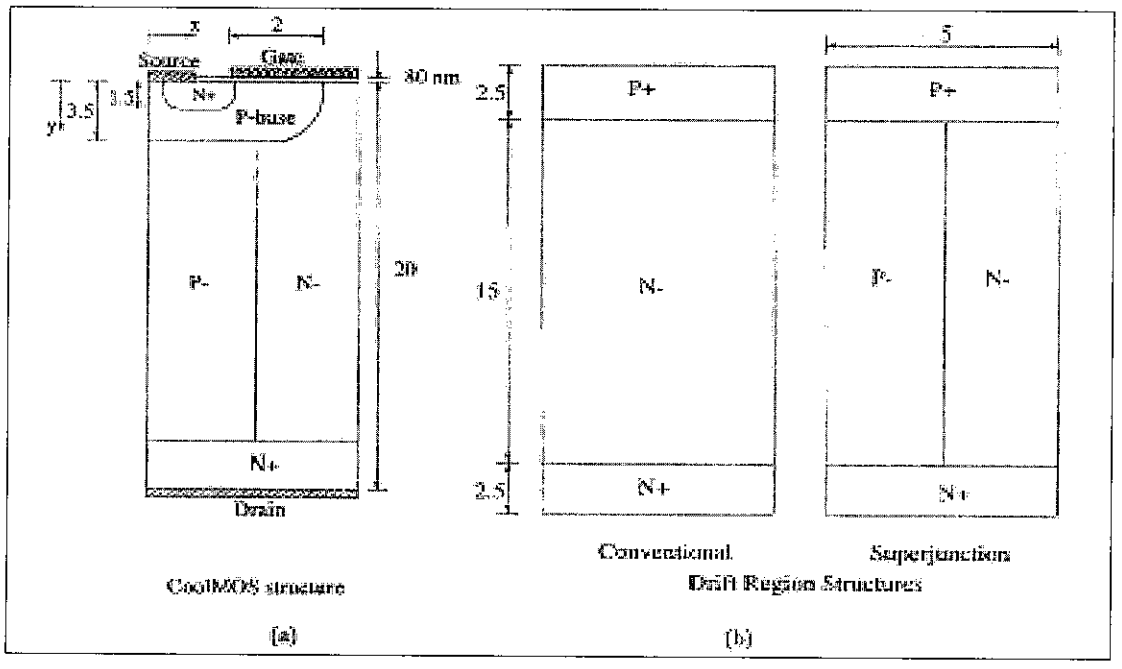


Figure 5 The COOLMOS and drift region structure, [6]

In the novel structure of COOLMOS, the n^- strip conducts the drain current when the device is on. Meanwhile, when the device is off the drain voltage, V_D appears as a reverse bias between the n^- and p^- strips. As a consequent, the drift zone is now completely depleted and acts like a voltage sustaining layer of a pin-structure. However, if the voltage is further increased, the electric field rises linearly without any further expansion of the space charge layer. Thus, no current flows through the layer. This behavior is characteristics for charge compensated devices and leads tremendously to lower losses. Therefore, the conduction losses of COOLMOS are reduced by a factor of 5 versus the conventional MOSFET.

Also, COOLMOS allows the increase of the n^- drift doping which permits a reduction of the conduction resistance up to 5-10 times compared to the conventional high voltage MOSFET. Moreover, the structure of COOLMOS offers an electric field expansion not only in the vertical direction as the conventional MOSFET, but also in the horizontal direction as well. Therefore, the breakdown voltage of COOLMOS can be increased by reducing the doping concentration and increasing the thickness of drift region.

The superior performance of COOLMOS over conventional MOSFET in terms of lower switching energy losses is illustrated as in Figure 6. This is because the generated energy which is converted into heat in every turn-on process increases with the chip area. Thus, it limits the minimum power losses in the inverter circuit topologies.

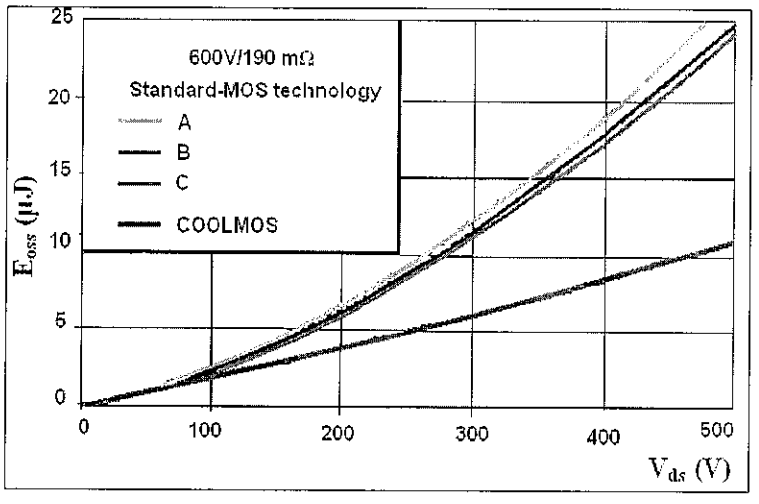


Figure 6 COOLMOS reduces the stored energy twice versus MOSFET, [7]

As shown in Figure 7, the gate to source threshold voltage of COOLMOS has been increased to improve the noise immunity margin in the bridge applications. The typical value of threshold voltage, $V_{gs(th)}$ is 4.5V (range 3.5V to 5.5V at 25°C). In spite of this, COOLMOS has already reaches its nominal $R_{DS\,(on)}$ at the gate voltage of 10V. The higher threshold voltage results in a better symmetry between turn-on and off behavior of the switches.

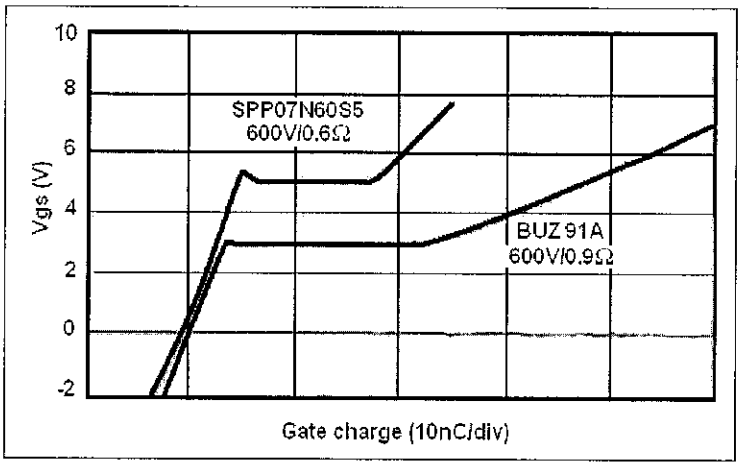


Figure 7 Gate charge characteristics of COOLMOS versus MOSFET, [7]

The following Figure 8 and 9 show the turn-on and off behavior of a COOLMOS with ohmic load respectively. The turn-off trend indicates no tail current, with a clearly visible of soft switching behavior up to a voltage of 50V. There is no carrier flows through the high field region during the turn-off of the device. Therefore, COOLMOS switch is insensitive to second breakdown phenomena and can be switched at a very high *dV/dt* rated.

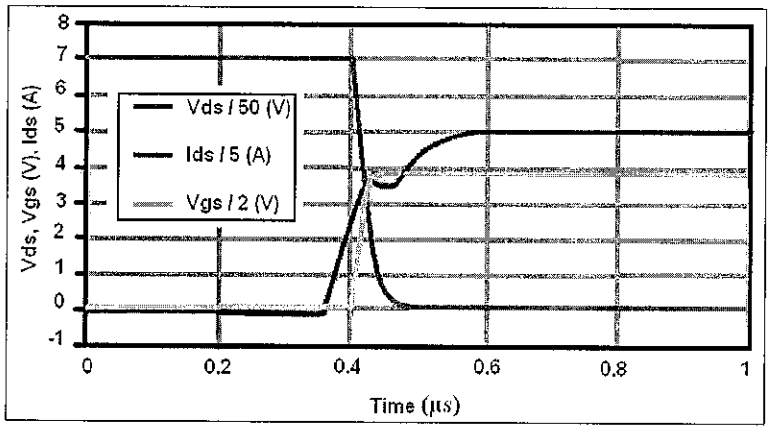


Figure 8 Turn-on behavior of COOLMOS with ohmic load, [7]

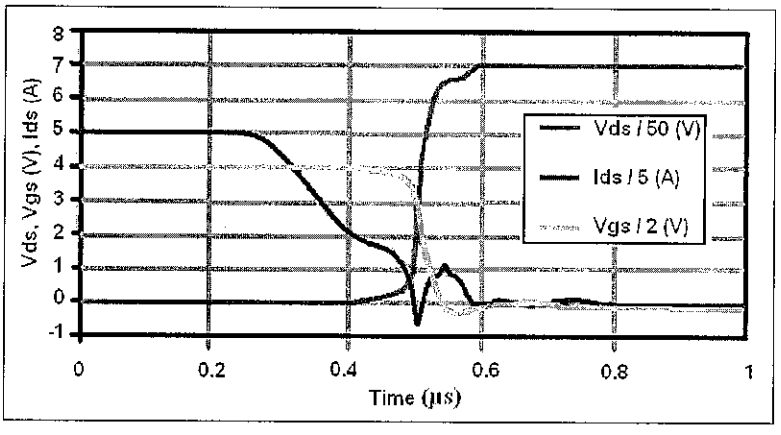


Figure 9 Turn-off behavior of COOLMOS with ohmic load, [7]

Overall, COOLMOS introduces a compensation structure in the vertical drift region to reduce its on-state resistance to one fifth of the conventional MOSFET for the same circuit configuration. As a result, COOLMOS has fastest and controllable switching speed for the same given circuit configuration [8].

CHAPTER 3
METHODOLOGY/PROJECT WORK

3.1 Methodology

The process of completing this project is referred to the following flow chart. During the first semester, the project goals are achieved via simulations. Meanwhile, at the second semester the project is executed by hardware implementation on PCB layout.

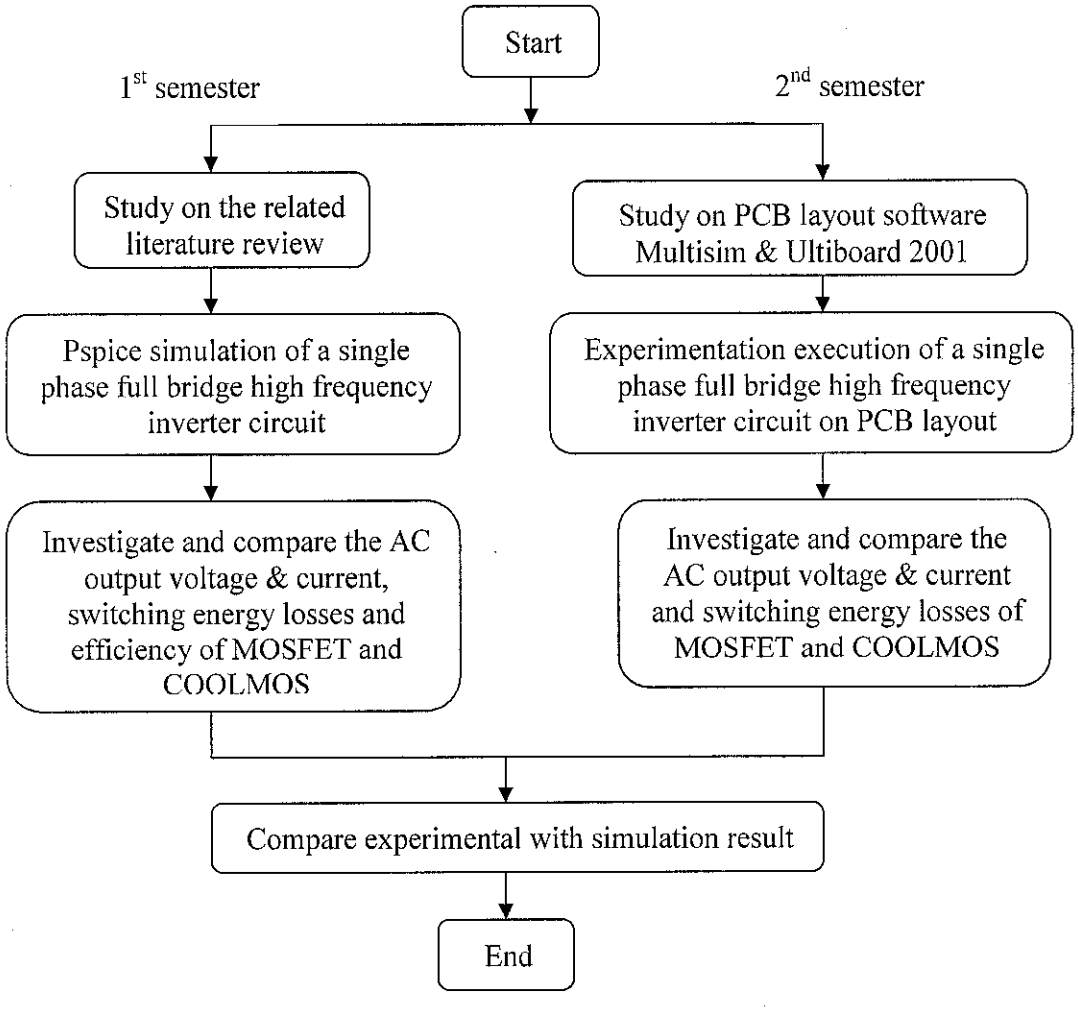


Figure 10 Project Process Flow

3.2 Procedure Identification

The entire procedures in completing this project are elaborated as follows:

1. Study on the related literature reviews:
   Numerous researches and studies have been done on the latest issue of high frequency inverter circuit design for UPS applications. Literature reviews are done to enhance the understanding on the project as well as to acquire the theoretical data and waveforms for the inverter circuit design. The researches include:

   a. Study on the technical papers related to various inverter circuit topologies, look into the major and recent issues of inverter circuit design for UPS application as well as familiarize with the characteristics of COOLMOS semiconductor switches in various application-wise. The technical papers are all obtained from the IEEE website.

   b. Study on the inverter circuit operation and its respective ac output voltage and current waveforms. The simulation output waveforms are to be verified with these theoretical output waveforms. Also, the calculation of initial inductor current is referred from Power Electronics Circuit text book written by Issa Batarseh.

   c. Research on the model number of COOLMOS for different manufacturers like International Rectifier (IRF), Infineon Technologies and Fairchild Semiconductor. The respective datasheets are collected and organized for future references in designing the inverter circuit. The importance of datasheets is to ensure that the simulation and experiment are executed without exceeding the maximum device rating.

   d. Study on the Cadence Pspice 14.2 software installation and the simulation method to analyze COOLMOS effectiveness performances in a high frequency inverter circuit. The manual of the software is referred to Pspice reference books [9, 10].

2. Design a single phase full bridge high-frequency inverter circuit using Cadence PSpice 14.2 software:

   a. Single phase full bridge high frequency inverter circuit with inductive-resistive (R-L) load is created in the Cadence Pspice software using COOLMOS as the switches. The inverter circuit is developed under the project design file of analog or mixed Analog to Digital (A/D) in order to simulate the inverter circuit. The inverter is having (R-L) load to comply with the industrial standard.

   b. The switching frequency of the switches is set to be at high-frequency of 500 kHz as to eliminate acoustic noise and distortion at the AC output. The DC input voltage is 150V, to cater the high rated voltage for UPS application. The inverter circuit is executed under 50% duty cycle to generate an equal proportion of positive and negative cycle at the AC output waveform.

   c. The components opted in the simulation are listed as below:

      i. Semiconductor switches:

         The process of getting the right model of COOLMOS is simply by doing trial and error simulations. Initially, the model from Infineon Technology is selected, but the simulation process dealt a lot with transient analysis problems. Therefore, the model from IRF manufacturer is opted as the switches in the simulation of inverter circuit since it experiences less transient analysis problems. The model of COOLMOS with its respective maximum voltage rating is shown as below:

         - COOLMOS Model: IRFBC40 ($V_{DSS} = 600V$)

         The datasheet for COOLMOS is referred for its maximum voltage rating before simulations are carried out, [11].

ii. Isolation transformer:

It is provided in between the main line and the load for protection purposes, in case of power failure, the load side is isolated.

- Isolation Transformer Model: TN33_20_11_2P90

iii. Loads:

The load consists of resistive-inductive, as it is practically use in the industry.

- Resistive Load: $R = 10\ \Omega$
- Inductive Load: $L = 18\ \mu H$

iv. Resistances at the input trigger pulse signal:

Small value of resistance is applied in between the input trigger pulse signal and the switches to protect the switches from high transient current.

- $R_1 = R_2 = R_3 = R_4 = 1\ \Omega$

v. Input trigger pulse signal:

Supposedly, the trigger pulse signal to turn-on COOLMOS is approximately 4V, however in the simulation the value does not sufficient to turn-on the switches thus the input trigger pulse signal is increased to 200V.

d. Parameter settings in the simulations are set to be as follows:

- Pulse Width, $PW = 1\ \mu s$, Period, $PER = 2\ \mu s$
- Time Delay, $T_D = 0\ \mu s$ for V_2 and V_3
- Time Delay, $T_D = 1\ \mu s$ for V_1 and V_4
- Rise Time, $T_R = 0.1\ \mu s$, Fall Time, $T_F = 0.1\ \mu s$
- Start saving data after = 1040 μs
- Maximum step size = 1 ns
- Transient point iteration limit = 1000

e. The inverter circuit is then simulated and the resultant output voltage and current waveform is compared with the theoretical waveforms. Once the output waveforms are verified, the effectiveness performances of COOLMOS in a high frequency inverter circuit are investigated in terms of the switching energy losses during turn-on and turn-off as well as the efficiency.

f. The investigation of COOLMOS performances in a high frequency inverter circuit is extended to different parameters as shown in Table 2.

Table 2 Varying parameters for comparative study of switches performances

Parameters	**Base**	**Varies**	
DC input voltage, V_{in}	150V	200V	400V
Switching frequency , f	500 kHz	1 MHz	5 MHz
Duty ratio, D	0.5	0.4	0.6

3. The simulation results:

The comparative study of COOLMOS and MOSFET for high frequency inverter design is done in terms of:

a. AC output voltage, V_o and current, I_o waveform

According to the voltage-source inverter (VSI) design, V_o is a function of inverter operation and the nature of the load can be observed from the load current, I_o. The voltage spike and leakage current is observed and analyzed from the resultant output waveforms if there is any.

b. Switching energy losses of COOLMOS and MOSFET

The switching energy losses are calculated as an area under the graph of power losses. The losses are investigated and compared during turn-on and turn-off mode of both switches. The switch with lesser switching energy losses is opted as the best switch in a high frequency inverter circuit.

c. Efficiency

The efficiency of the circuit is obtained by the ratio of resultant output power to input power.

4. Preliminary study on PCB layout software, Multisim & Ultiboard 2001

The studies are focused on the process of constructing a single phase full bridge inverter circuit using Multisim and transferred to Ultiboard 2001 to create the circuit routing.

5. Finalize the components for circuit construction:

The components selection is based on the simulation. The ratings and specifications of components are obtained from the simulation data operated at DC input voltage of 150V, switching frequency of 500 kHz and duty cycle of 0.5. However, the selection of components is affected by the limitation of cost and the availability in the market. The list and details of components are shown as in Table 3.

Table 3 List and details of components for experimentation

NO.	ITEM	ORDER CODE	NO. OF ITEM	PRICE
1	Resistor, 10Ω Wire-wound Aluminum Clad, 200W	272723	1	RM 100.02
2	Resistor, 1Ω Wire-wound Aluminum Clad, 100W	652453	4	RM 31.77
3	Inductor, 18 μH Inductor Series 2100	4981601	1	RM 13.03
4	COOLMOS, V_{DSS} = 600V, 1 MHz Model: IRFBC40	3572572	4	RM 12.96
6	Capacitor, 250VAC, 4700pF	3531892	1	RM 1.69
7	Capacitor, 200VDC, 100pF	286930	1	RM 0.99

6. Construction of inverter circuit on PCB layout:

   The steps involved in constructing an inverter circuit on PCB layout is elaborated as below:

   a. Design an inverter circuit using Multisim 2001 software

      The inverter circuit is designed by placing and connecting the respective components equivalent to the inverter circuit configuration done in the Cadence Pspice software. The corresponding model of the components is selected from the library folder to obtain the correct footprints. However, there are few components which do not have its model in the Multisim library, thus any components with the match footprints are selected.

   b. Transfer the inverter circuit from Multisim to Ultiboard 2001 software

      i. From Multisim, the inverter circuit file is transferred to Ultiboard 2001 software to develop circuit routing of the components connection.

      ii. The components are placed outside the board outline after netlist is imported from Multisim. Therefore, the components need to be arranged into a proper configuration manually. The components must be well arranged as it will be printed on the PCB layout.

      iii. A few factors need highly consideration in PCB design, such as to ensure that the PCB is a copper bottom design with a single layer. Furthermore, the trace width, drill hole diameter of the pads and the spacing between the components are also need to be properly designed.

      iv. Next, the function of auto-routing is activated to develop routing of traces between components. Any open traces ends and unused vias of the inverter circuit are deleted before exporting it to the Gerber file.

v. Finally, Gerber file is produced by selecting RS274X and NC Drill format and exporting the entire available layers list into the Gerber file format.

7. Experimentation execution on the PCB layout

a. Before the experiments are carried out, some of the components are soldered on PCB layout. The inverter circuit configuration on the PCB layout with the high rated resistors and wires is shown as in Figure 11.

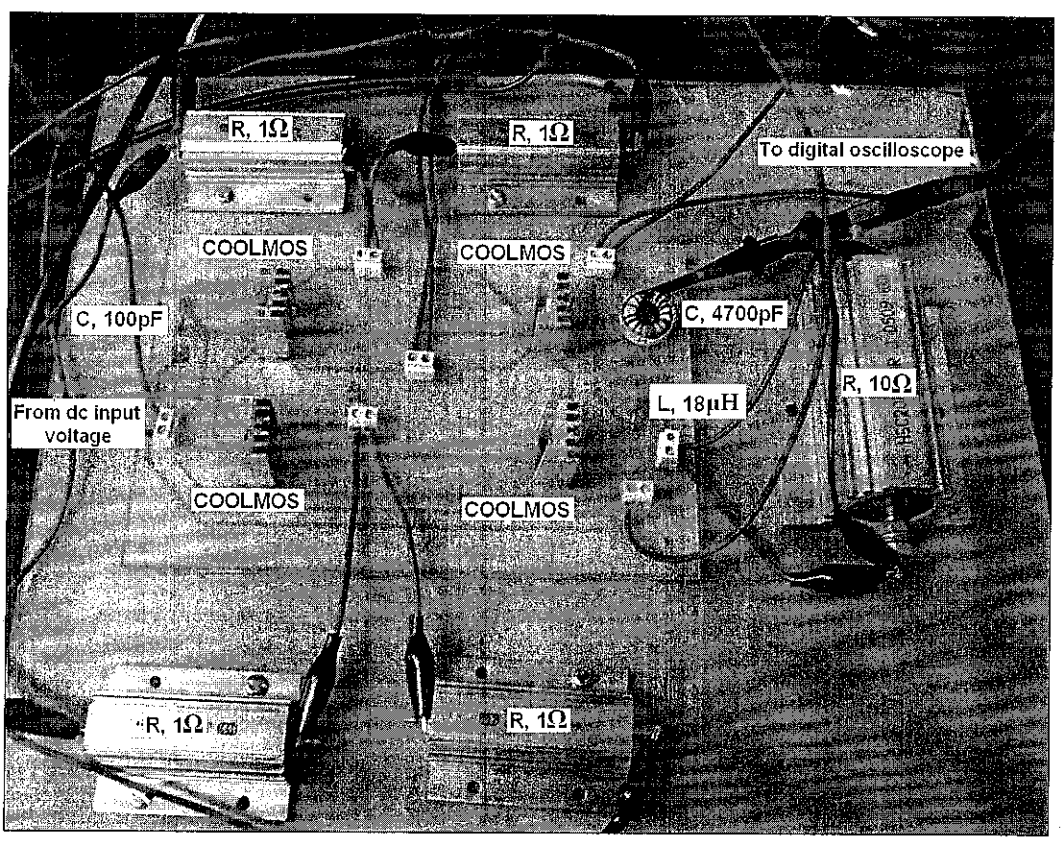


Figure 11 Inverter circuit configuration on PCB layout

b. The complete experimentation setup of this project is shown as in Figure 12. The hardware consists of three independent DC power supply which is connected in series to produce DC input voltage of 150V. Digital oscilloscope is used to capture the AC output voltage and current as well as the power losses waveform. Initially, two function generators are used to trigger two different pairs of switches in the full bridge inverter circuit. However, due to the synchronization difficulty, BJT switch is used to overcome this problem.

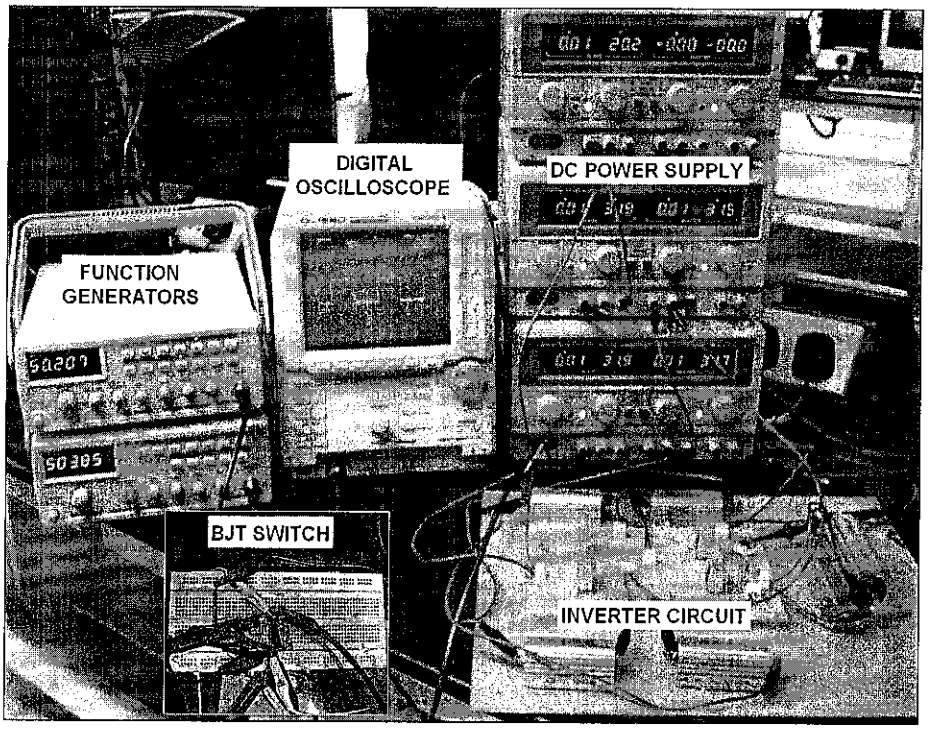


Figure 12 Experimentation setup of full bridge inverter circuit

c. An additional external circuit is constructed solely by using a BJT in order to invert the voltage waveform of input trigger signal supplied by the function generator. The illustration of the switching inversion mechanism is shown as in Figure 13.

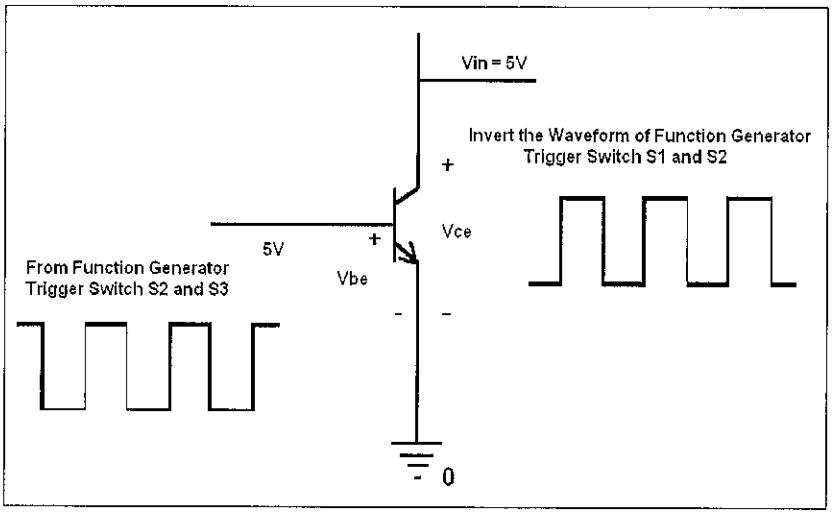


Figure 13 BJT switch to invert the trigger input signal

Based on the above figure, an input trigger signal of 5V from function generator is supplied in between the base and emitter terminal of BJT. This input trigger signal is used to trigger S_2 and S_3 switches of full bridge inverter circuit. When collector-emitter terminal of BJT is supplied with 5V input from DC power supply, the voltage waveform across collector-emitter terminal is now become the invert of input trigger signal from function generator. Therefore the voltage across collector-emitter terminal is used to trigger $S_1$and S_4 switches of full bridge inverter circuit.

d. The experiments are carried out only at the base parameters as shown in Table 4. At these fixed parameters, the AC output voltage and current as well as power losses waveforms are obtained for COOLMOS switches. The experimental results are to be compared with the simulation results. At the end of this project, switch with lesser switching energy losses and higher efficiency is concluded as the best switch to be used in a full bridge inverter circuit for UPS application.

Table 4 Base parameters use for experimentation on PCB layout

Parameters	**Base**
DC input voltage, V_{in}	150V
Switching frequency , f	500 kHz
Duty ratio, D	0.5

e. Getting the power losses waveform of COOLMOS

In the experiments, the waveform of power losses could not obtained directly since there is no power probe available in the laboratory. Therefore the following procedures, as shown in Figure 14 are used to obtain the power losses waveform.

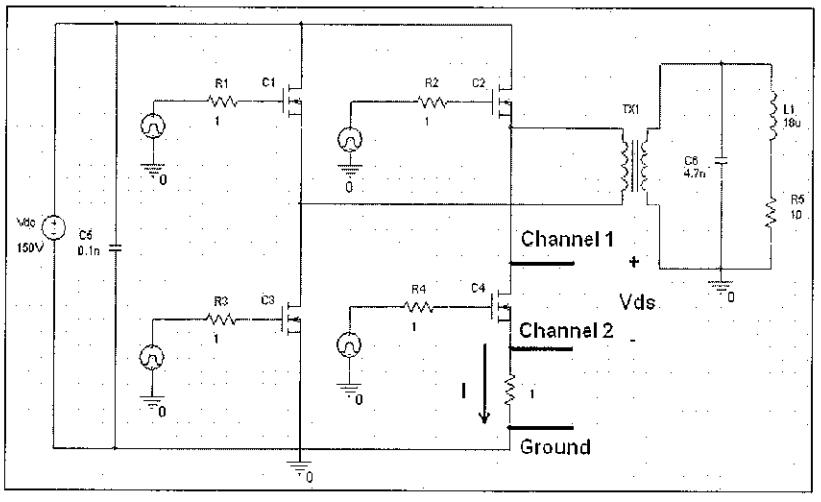


Figure 14 Circuit arrangement to get power losses waveform

The multiplication of voltage across drain-source, V_{ds} terminal of switch and current flows through 1Ω resistor gives the power losses of the switch. Two channels of digital oscilloscope are used for this purpose. Channel 1 is used to capture the voltage waveform of the switch. Meanwhile Channel 2 is used to obtain the current waveform flows through the switch. Then, the power losses waveform is obtained by multiplying the two channels using the MATH function available on the digital oscilloscope.

Theoretically;

Channel 1 : Voltage, V_{ds}

Channel 2 : Current, I

$$I = \frac{V}{R} = \frac{V}{1\Omega} = V$$

Power losses waveform = Channel 1 x Channel 2

= V x I

= W

3.3 Equipment & Tools

The major equipment and tools involved in this project are consists of:

1. Cadence Pspice 14.2 tools

   The software is used to simulate a single phase full bridge high frequency inverter circuit in order to investigate and compare the effectiveness performances of COOLMOS and MOSFET in the inverter circuit.

2. Multisim & Ultiboard 2001 tools

   The software is used in the process of constructing and fabricating the circuit layout of inverter circuit on the PCB for experimentation purposes.

3. Electrical & electronic devices

   a. DC Power Supply

      It is used to provide the inverter circuit with a DC input voltage supply of 150V.

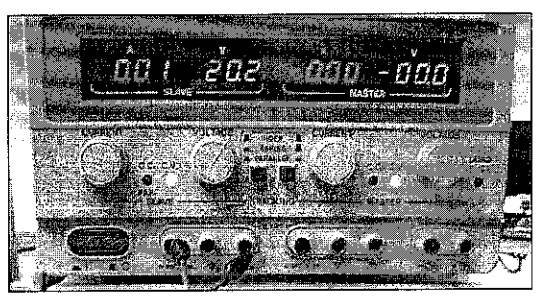


Figure 15 DC power supply

   b. Function Generator

      It is used to turn-on the switches with a switching frequency of 500 kHz

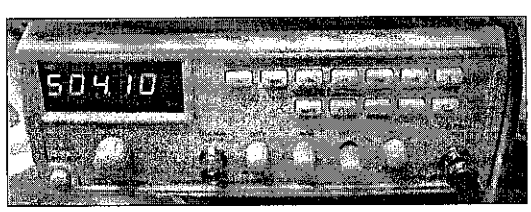


Figure 16 Function Generator

c. Digital Oscilloscope

It is used to capture AC output voltage and current as well as power losses waveforms.

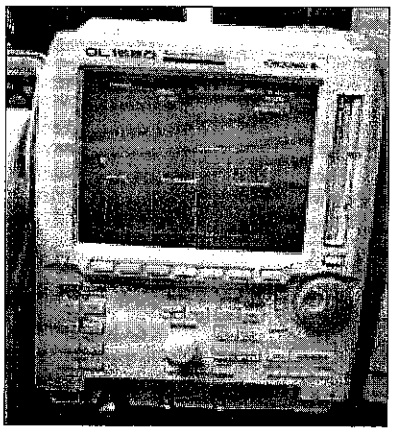


Figure 17 Digital Oscilloscope

CHAPTER 4
RESULTS AND DISCUSSION

A comparative study is performed both via simulation using Cadence PSpice and experimentation on PCB layout to investigate the output voltage and current waveform of a single phase full bridge high frequency inverter circuit using COOLMOS and MOSFET as the power switches. Also, the switching energy losses and efficiency of the switches are investigated and compared. Simulation is carried out by using the parameters as shown in Table 5.

Table 5 Parameters setting for simulation

▪ Switching frequency, f	= 500 kHz
▪ Duty ratio, D	= 0.5
▪ Period, T	= 2.0 μs
▪ Pulse width, PW	= 1.0 μs
▪ Time delay, TD (for V_2 and V_3)	= 0
▪ Time delay, TD (for V_1 and V_4)	= 1.0 μs
▪ Rise time, T_R and Fall time, T_F	= 0.1 μs
▪ Start saving data after	= 1040 μs
▪ Maximum step size	= 1.0 ns
▪ Transient point iteration limit	= 1000

In the simulation, the investigation of COOLMOS performances is performed at varied DC input voltage of 150V, 200V and 400V, switching frequency of 500 kHz, 1 MHz and 5 MHz as well as varying the duty ratio to 0.4, 0.5 and 0.6.

The simulation schematic diagram of a single phase full bridge high frequency inverter circuit with COOLMOS switches is shown in Figure 18.

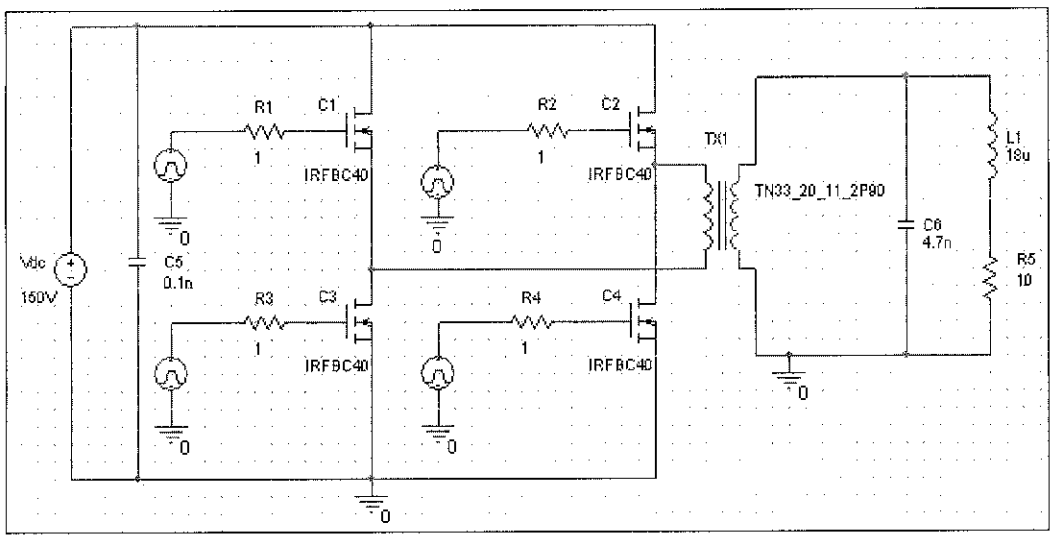


Figure 18 Single phase full bridge inverter circuit

The execution of experiment is performed on the PCB layout shown as in Figure 19 with its respective schematic layout shown in Figure 20. The components soldered on PCB layout of full bridge inverter is placed with high rated resistors on the acrylic board. From the experimentation, output voltage and current as well as power losses waveforms are obtained and compared with the simulation results.

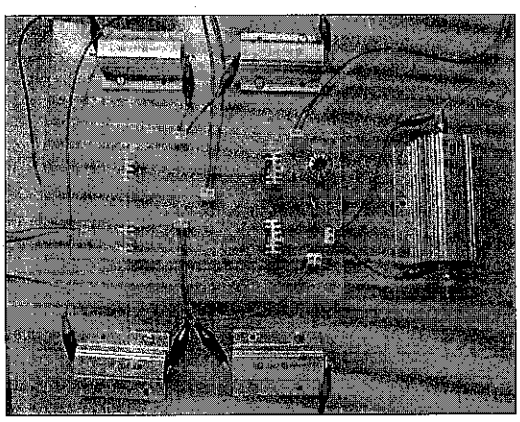


Figure 19 PCB layout

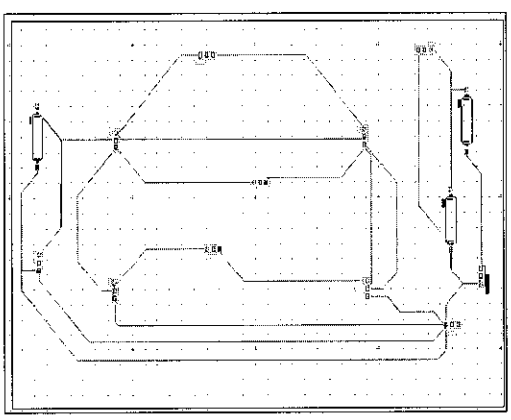


Figure 20 Schematic of PCB layout

4.1 Output Voltage and Current Waveforms

The simulation and experimental output voltage of a full bridge inverter circuit using COOLMOS switch is shown as in Figure 21 and 22. Meanwhile, the simulation and experimental output voltage of a full bridge inverter circuit using MOSFET switch is shown as in Figure 23 and 24 respectively, as taken from the investigation conducted by Nur Alina Jelani, [12]. The experimental output voltage waveform of both switches is obtained at 500ns/divison and 50V/division.

Simulation output voltage

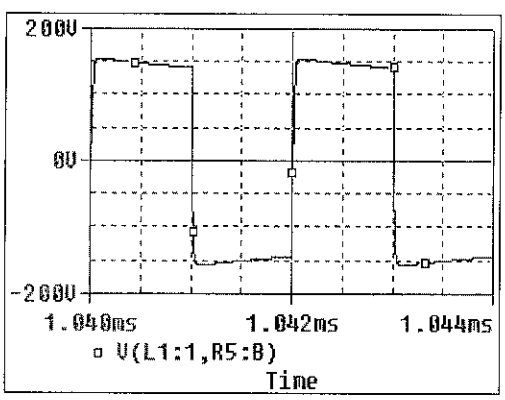


Figure 21 Simulation output voltage using COOLMOS switch

Experimental output voltage

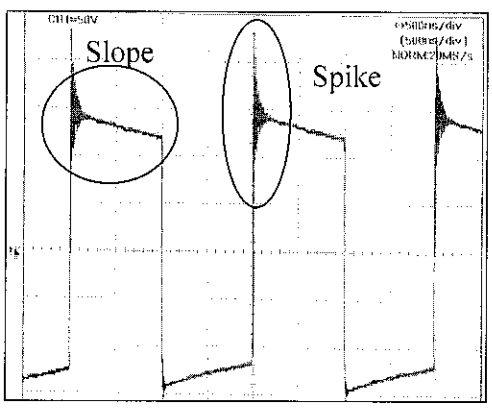


Figure 22 Experimental output voltage using COOLMOS switch (Scale on oscilloscope = X:500ns/div, Y:50V/div)

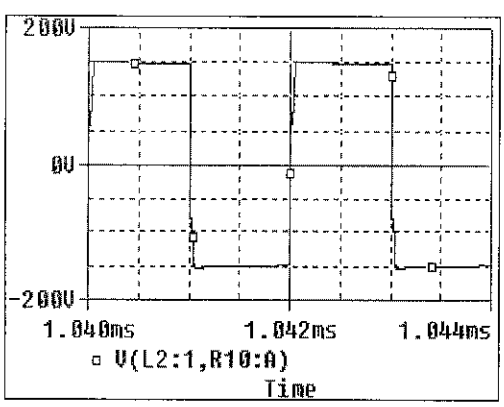


Figure 23 Simulation output voltage using MOSFET switch, [12]

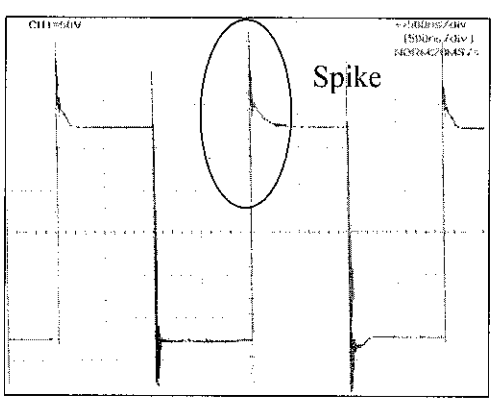


Figure 24 Experimental output voltage using MOSFET switch, [12] (Scale on oscilloscope = X:500ns/div, Y:50V/div)

It can be observed from Figure 21 and 22, the output voltage with COOLMOS switch is slant-wise due to the characteristics of COOLMOS of having an extreme *dV/dt* rated. However, the slant of experimental output voltage is more obvious compared to the simulation output voltage. As for MOSFET, the simulation and experimental output voltage is almost a perfect squarewave. From the experimental output voltage waveform of both switches, the voltage spike exists during turn-on and off the switches. This is due to the internal noise of the components in the inverter circuit itself.

Next, the simulation and experimental output current of a full bridge inverter circuit using COOLMOS switch is shown as in Figure 25 and 26 respectively. The simulation and experimental output current using MOSFET switch is similar as using COOLMOS. The experimental output current waveform of both switches is obtained at 400ns/divison and 2V/division.

Simulation output current

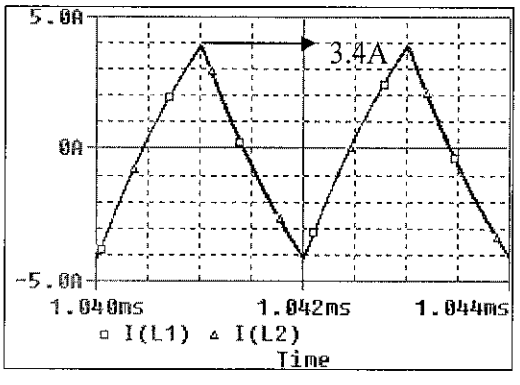


Figure 25 Output current using COOLMOS

Experimental output current

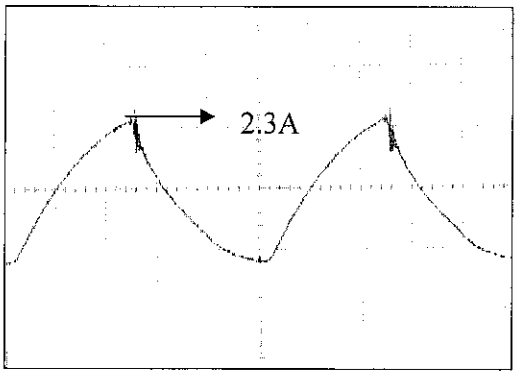


Figure 26 Output current using COOLMOS

(Scale on oscilloscope = X:400ns/div, Y:2V/div)

The simulation and experimental output current waveform for both switches are alike except the value of peak current. The simulation peak output current is 3.4A, while the experimental peak output current is 2.3A. This is due to the resistances in the wire connections as well as in the components of the inverter circuit itself.

Theoretically, the initial value of output current is calculated by the following formula:

$$Io = -\frac{Vdc}{R}\frac{1-e^{-\frac{T}{2\tau}}}{1+e^{-\frac{T}{2\tau}}} = -\frac{150}{10}\frac{1-e^{-\frac{2}{2(1.8)}}}{1+e^{-\frac{2}{2(1.8)}}} = -4.063A$$

where $T = \frac{1}{f} = \frac{1}{500k} = 2us$

$\tau = \frac{L}{R} = \frac{18u}{10} = 1.8us$

4.2 Switching Energy Losses

The simulation and experimental switching energy losses of COOLMOS switches during turn-on are shown in Figure 27 and 28 respectively. Meanwhile, the simulation and experimental switching energy losses of MOSFET are shown in Figure 29 and 30. The experimental switching energy losses for both COOLMOS and MOSFET are obtained at 200ns/divison and 5kV/division.

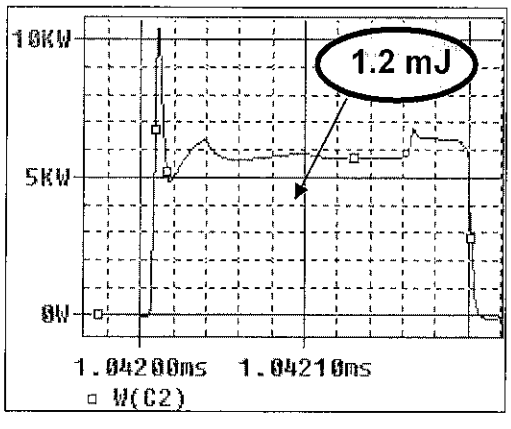


Figure 27 Simulation switching energy losses of COOLMOS during turn-on

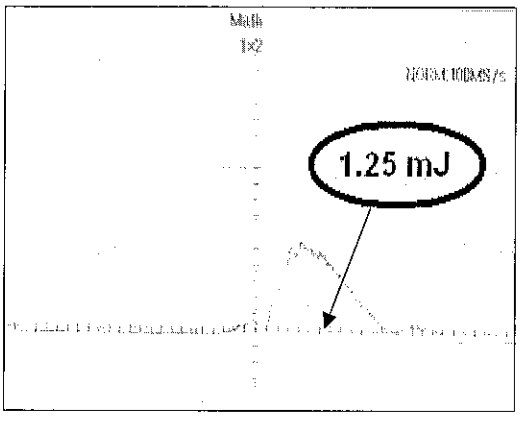


Figure 28 Experimental switching energy losses of COOLMOS during turn-on
(Scale on oscilloscope = X:200ns/div, Y:5kV/div)

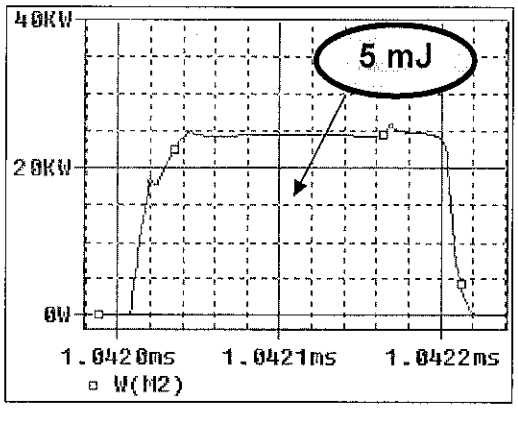


Figure 29 Simulation switching energy losses of MOSFET during turn-on, [12]

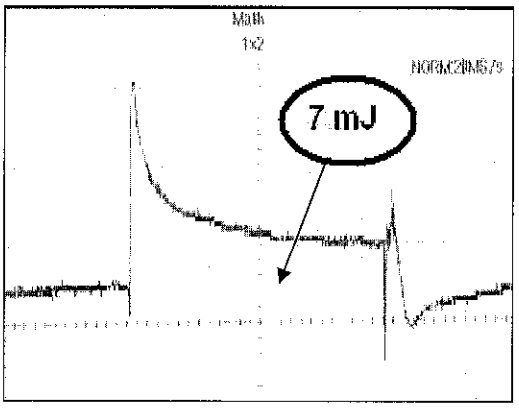


Figure 30 Experimental switching energy losses of MOSFET during turn-on, [12]
(Scale on oscilloscope = X:200ns/div, Y:5kV/div)

The switching energy losses are calculated as area under the graph of power losses waveform and the calculation is shown as below:

Calculation of simulation switching energy losses:

Switching energy losses = Area under the graph of power losses waveform
= Nos. of boxes x Time (x-axis) x Power (y-axis)

Switching energy losses of COOLMOS = 2.4 x 100 ns x 5 kW
= **1.2 mJ**

Switching energy losses of MOSFET = 2.5 x 100 ns x 20 kW
= **5 mJ**

Calculation of experimentation switching energy losses:

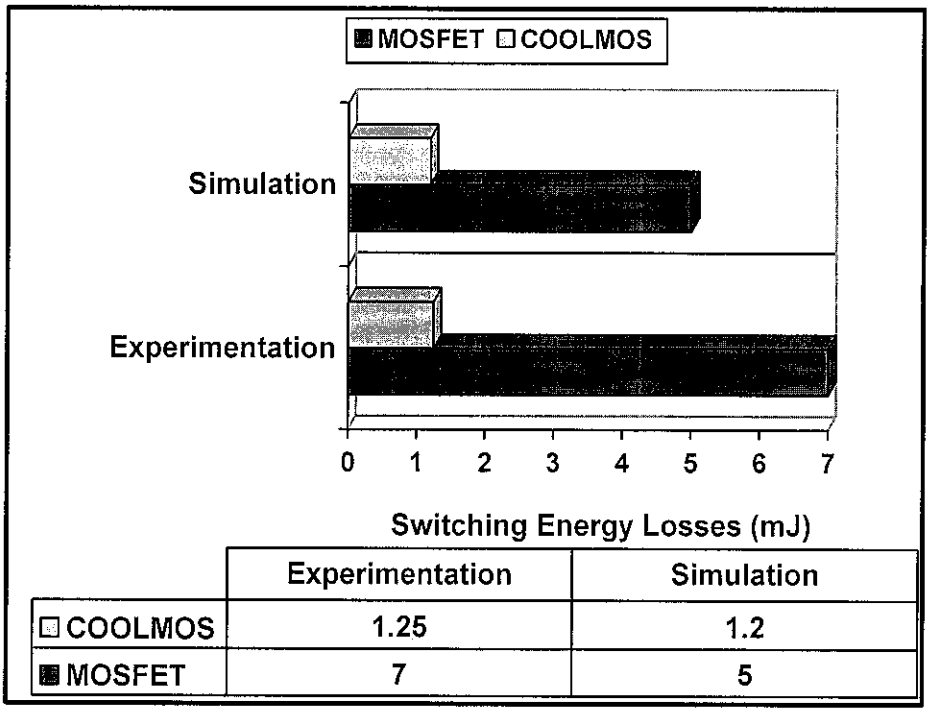
Switching energy losses = Area under the graph of power losses waveform
= Nos. of boxes x Time (x-axis) x Power (y-axis)

Switching energy losses of COOLMOS = 1.25 x 200 ns x 5 kW
= **1.25 mJ**

Switching energy losses of MOSFET = 7 x 200 ns x 5 kW
= **7 mJ**

The experimental switching energy losses for both switches is slightly higher than the simulation value due to a few factors such as the resistances of the PCB tracks and routing, as well as connection of high rated wires and digital oscilloscope probes. Nevertheless, COOLMOS produced 75% reduction of switching energy losses compared to MOSFET.

The comparison of simulation and experimental switching energy losses is represented in the bar chart as shown in Figure 31.



	Experimentation	Simulation
COOLMOS	1.25	1.2
MOSFET	7	5

Figure 31 Comparison of simulation and experimental switching energy losses

The simulation switching energy losses of COOLMOS and MOSFET switches during turn-off are shown in Figure 32 and 33 respectively.

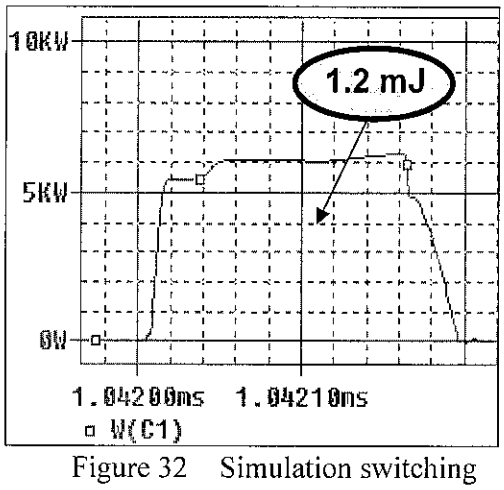


Figure 32 Simulation switching energy losses of COOLMOS during turn-off

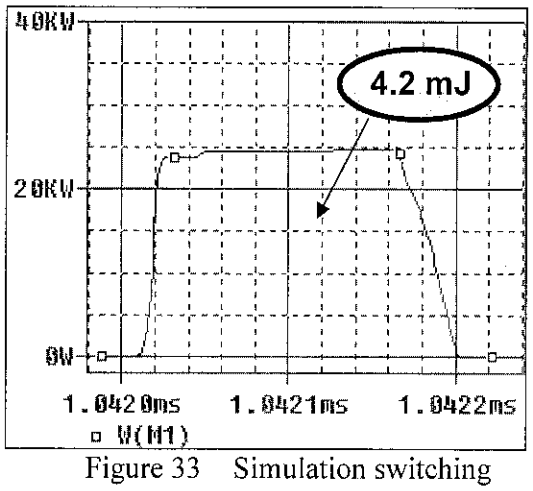


Figure 33 Simulation switching energy losses of MOSFET during turn-off, [12]

Calculation of simulation switching energy losses:

Switching energy losses = Area under the graph of power losses waveform
= Nos. of boxes x Time (x-axis) x Power (y-axis)

Switching energy losses of COOLMOS = 2.4 x 100 ns x 5 kW
= **1.2 mJ**

Switching energy losses of MOSFET = 2.1 x 100 ns x 20 kW
= **4.2 mJ**

As it can be seen from the power losses waveform, the switching energy losses of COOLMOS is reduced by 75% compared to MOSFET and the statement is verified by the above calculations.

4.3 Extra Simulation of COOLMOS and MOSFET at Varying Parameters

4.3.1 Varying f = 1, 5 & 10 MHz with constant V_{in} = 150V and D = 0.5

Two single phase full bridge high frequency inverter circuit each using either COOLMOS or MOSFET as the switches is simulated together to ease the comparison of their performances. Firstly, the simulation of the inverter circuit is operated at varied frequency of 1, 5 and 10 MHz. The output voltage and current waveforms at frequency of 1 and 5 MHz are attached as in Appendix 2. At a frequency of 5 MHz, the output voltage and current are having a slight distortion and at a frequency of 10 MHz, the resultant output voltage and current waveform of both switches are severe distorted as shown in Figure 34 and 35 respectively.

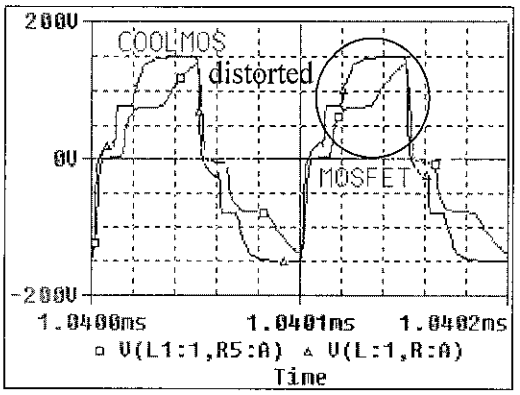


Figure 34 Simulation output voltage at f = 10 MHz

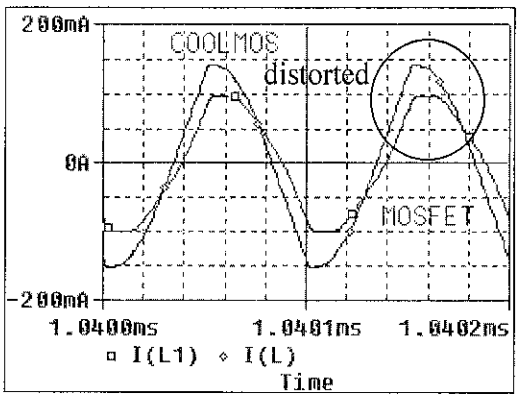


Figure 35 Simulation output current at f = 10 MHz

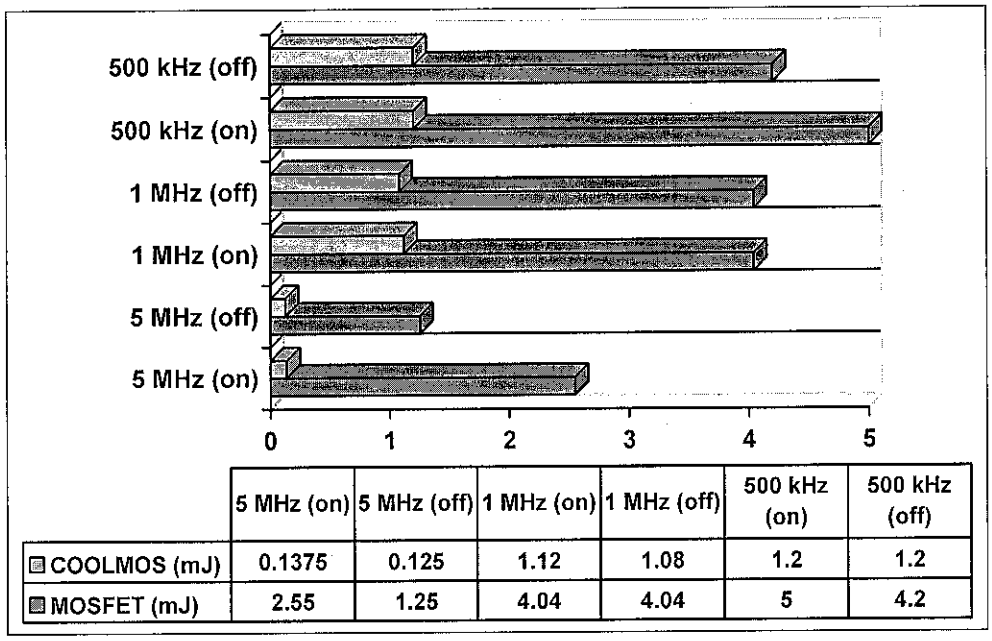
The severe distortion at the output voltage and current indicates that both switches are unable to operate properly at a frequency higher than 5MHz. The distortion is mainly caused by the internal structure of both switches which could not sustain a very high frequency, and thus highly degrades the performances of the inverter circuit. Therefore, the switching frequency of higher than 5 MHz is unacceptable in inverter circuit design for UPS application using COOLMOS and MOSFET as the switches.

The maximum value of output voltage and current at the respective three frequencies is listed as in Table 6. As seen from the table, the maximum value of output voltage and current reduces as the switching frequency of switches increases.

Table 6 Maximum output voltage and current at f = 500 kHz, 1 & 5 MHz

Switching Frequency, f	Maximum output voltage (V)		Maximum output current (A)	
	COOLMOS	MOSFET, [12]	COOLMOS	MOSFET, [12]
500 kHz	153.001	150.326	3.3908	3.2869
1 MHz	150.650	149.896	1.3659	1.3136
5 MHz	149.85	149.85	0.2677	0.3139

Next, the switching energy losses of COOLMOS and MOSFET are investigated and compared in bar chart as shown in Figure 36.



	5 MHz (on)	5 MHz (off)	1 MHz (on)	1 MHz (off)	500 kHz (on)	500 kHz (off)
COOLMOS (mJ)	0.1375	0.125	1.12	1.08	1.2	1.2
MOSFET (mJ)	2.55	1.25	4.04	4.04	5	4.2

Figure 36 Comparison of switching energy losses at f=500 kHz, 1 & 5 MHz

From the bar chart, it is obvious that the switching energy losses of COOLMOS in the full bridge inverter circuit are much lesser than MOSFET. The switching energy losses for both switches are decrease as the switching frequency increases. This is true based on the given relations of power, energy and frequency.

Given:

Power $= P$ (Watts)

Energy $= E$ (Joules)

Frequency $= f$ (Hertz)

Since $P = Ef$, therefore the frequency is given as $f = \frac{P}{E}$

Based on the equation above, the switching energy losses of the switches is inversely proportional to the switching frequency.

Overall, COOLMOS produced 75% reduction of switching energy losses compared to MOSFET during turn-on and off.

The efficiency of inverter circuit using COOLMOS and MOSFET as the switches is also taken into consideration. As seen in Figure 37, the efficiency of the full bridge inverter circuit is reduced as the switching frequency increases. However, the efficiency of the inverter circuit by using COOLMOS as the switches is still higher compared to MOSFET.

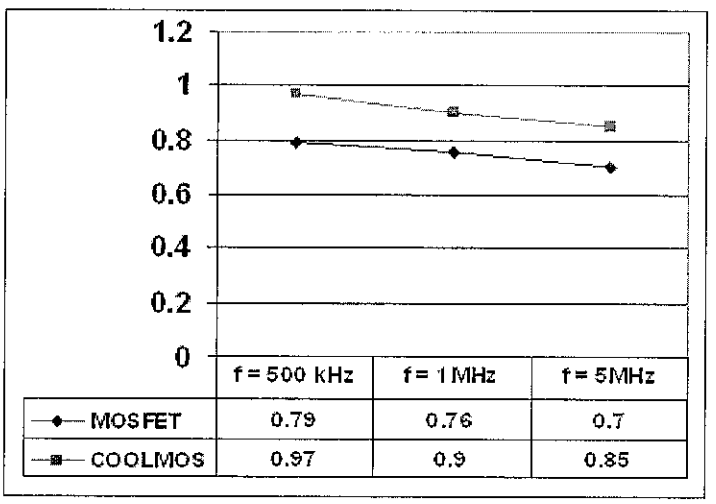


Figure 37 Efficiency of inverter circuit at f = 500 kHz, 1 & 5 MHz

4.3.2 Varying D = 0.4 & 0.6 with constant V_{in} = 150V and f = 500 kHz

Secondly, the effectiveness performances of COOLMOS and MOSFET in a single phase full bridge high frequency inverter circuit is further investigated by varying the duty ratio of the switches to 0.4 and 0.6. At the duty ratio of 0.4 and 0.6, the switch is turned-on 40% and 60% of the total one cycle period, T respectively. The respective output voltage and current waveforms are attached as in Appendix 2.

From Figure 38, it shows at the duty ratio of 0.4, the value of maximum positive output voltage is greater than the negative value. On the other hand, at the duty ratio of 0.6, the value of maximum positive output voltage is lower than the negative value as shown in Figure 39.

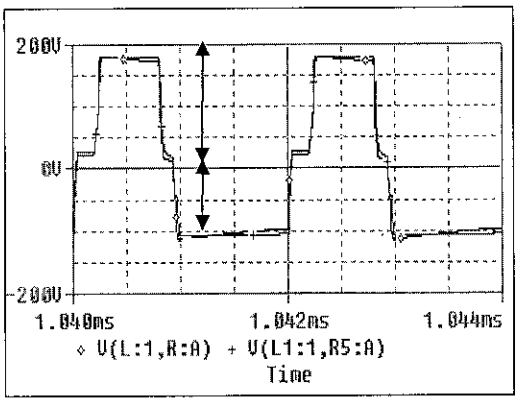


Figure 38 Simulation output voltage at $D = 0.4$

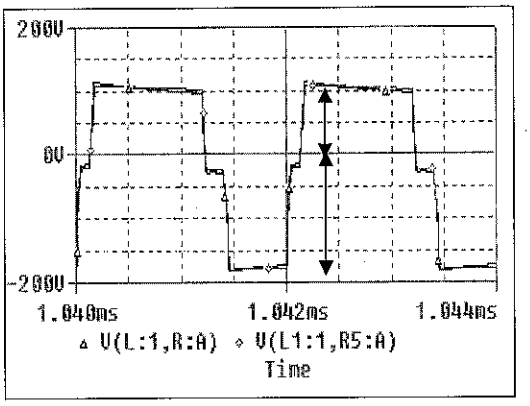


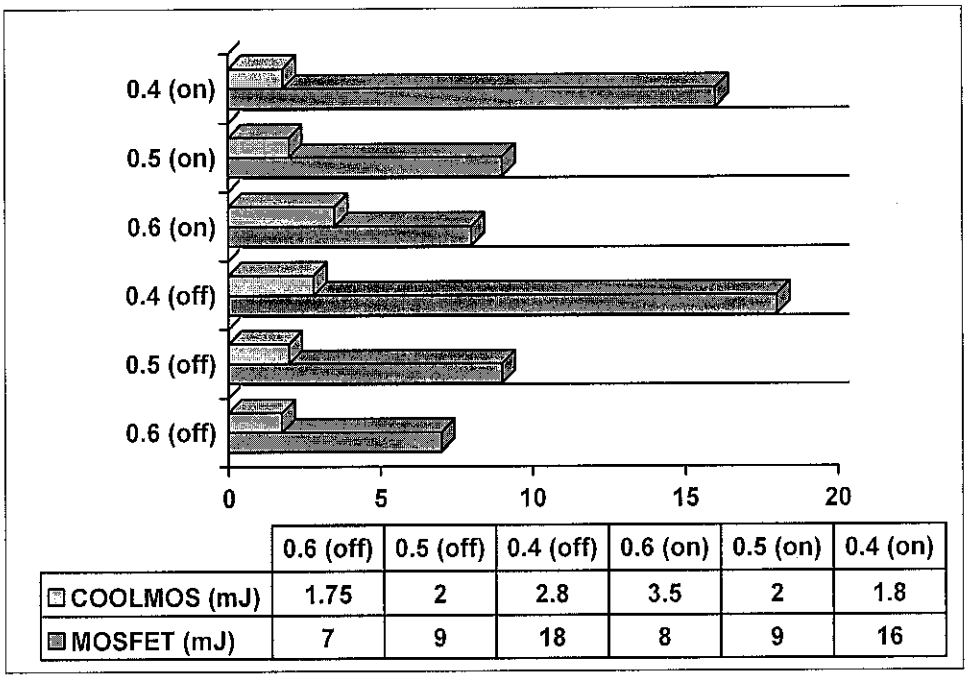
Figure 39 Simulation output voltage at $D = 0.6$

The maximum positive value of output voltage and current at the respective three duty ratios is listed as in Table 7. As seen from the table, the maximum positive value of output voltage becomes greater or lower than the DC input voltage depending on the duty ratio given.

Table 7 Maximum output voltage and current at $D = 0.4$, 0.5 & 0.6

Duty ratio, D	Maximum output voltage (V)		Maximum output current (A)	
	COOLMOS	MOSFET, [12]	COOLMOS	MOSFET, [12]
0.4	180.983	179.620	3.2630	3.2389
0.5	153.001	150.326	3.3908	3.2869
0.6	114.037	109.436	2.9268	2.8514

Next, the switching energy losses of COOLMOS and MOSFET are investigated and compared in bar chart as shown in Figure 40.



	0.6 (off)	0.5 (off)	0.4 (off)	0.6 (on)	0.5 (on)	0.4 (on)
COOLMOS (mJ)	1.75	2	2.8	3.5	2	1.8
MOSFET (mJ)	7	9	18	8	9	16

Figure 40 Bar chart of switching energy losses at $D = 0.4, 0.5$ & 0.6.

The relationship of switching energy losses and the duty ratio is given as below:

Given:

Pulse Width = PW (Seconds)

Duty Ratio = D

Time = T (Seconds)

Frequency = f (Hertz)

Power = P (Watts)

Energy = E (Joules)

Table 8 The relationship of switching energy losses and duty ratio

During turn-on	During turn-off
The pulse width is given as: $$PW = DT = \frac{D}{f} = \frac{D}{P/E}$$ Therefore, the switching energy losses is given as: $$E = \frac{PWxP}{D}$$	The pulse width is given as: $$PW = (1-D)T = \frac{(1-D)}{f} = \frac{(1-D)}{P/E}$$ Therefore, the switching energy losses is given as: $$E = \frac{PWxP}{(1-D)}$$

Based on the above relations, during switch turn-on, the switching energy losses of the switches is inversely proportional to the duty ratio. When the duty ratio increases, the switching energy losses decrease. However, for the COOLMOS switch, the value of switching energy losses increases as the duty ratio is increased. This is because the value of power losses increases at a higher duty ratio.

Meanwhile, during switch turn-off, supposedly the switching energy losses of the switches are directly proportional to the duty ratio. However, as seen from the bar chart, the value of switching energy losses is decreases with increasing duty ratio. This is due to the smaller power losses produced at a higher duty ratio.

Overall, COOLMOS produced 80% reduction of switching energy losses compared to MOSFET during turn-on and off.

4.3.3 Varying V_{in} = 200 & 400V with constant f = 500 kHz and D = 0.5

Thirdly, the effectiveness performances of COOLMOS and MOSFET in a single phase full bridge high frequency inverter circuit is investigated by varying the DC input voltage to 200V and 400V. At an input voltage of 200V, the maximum positive and negative output voltage is equal to the DC input voltage. The respective output voltage and current waveform at an input voltage of 200V is attached in Appendix 2. However, at an input voltage of 400V, the output voltage and current waveform of a full bridge inverter circuit using MOSFET switches are severely distorted as shown in Figure 41 and 42. This is because the internal structure of MOSFET has been damaged since its maximum rated voltage is exceeded (V_{DSS} = 250V).

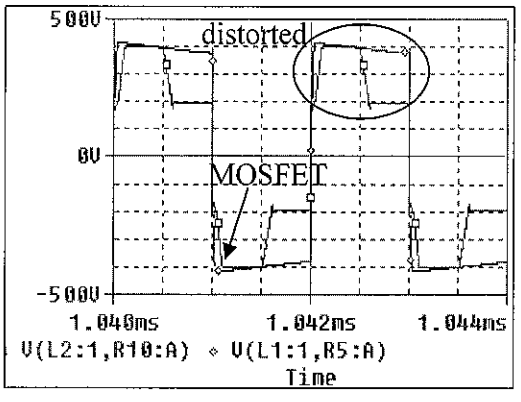


Figure 41 Simulation output voltage at V_{in} = 400V

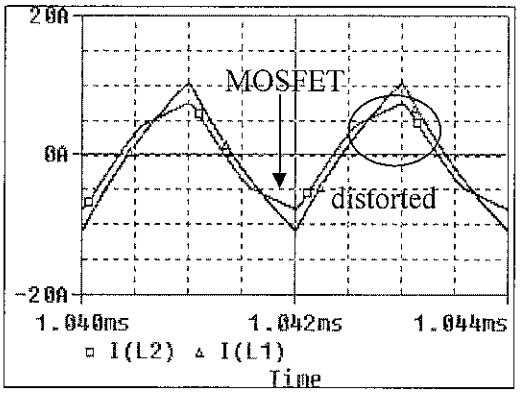


Figure 42 Simulation output current at V_{in} = 400V

The maximum positive value of output voltage and current at the respective three DC input voltages is listed as in Table 9. As seen from the table, the maximum positive value of output voltage is approximately equal to the DC input voltage.

Table 9 Maximum output voltage and current at V_{in} = 150, 200 & 400V

Input Voltage, Vin	Maximum Output Voltage (V)		Maximum Output Current (A)	
	COOLMOS	MOSFET, [12]	COOLMOS	MOSFET, [12]
150 V	153.001	150.326	3.3908	3.2869
200 V	204.923	201.317	4.4628	4.4149
400 V	410.249	-	8.9663	-

CHAPTER 5
CONCLUSIONS & RECOMMENDATIONS

5.1 Conclusions

Conclusively, the objective of this project in comparing the effectiveness performances of MOSFET (IRF644, V_{DSS} = 250V) and COOLMOS (IRFBC40, V_{DSS} = 600V) semiconductor switches in a single phase full bridge high frequency inverter circuit for UPS applications has been accomplished. The full-bridge inverter circuit is operated at an input voltage of 150V-DC and switching frequency of 500 kHz under fifty percent (50%) duty ratio. The effectiveness performances of both switches are investigated and compared in terms of output voltage and current waveform, switching losses as well as the efficiency of inverter circuit.

By simulation, COOLMOS shows superior performances of having 50% reduction of switching energy losses with greater efficiency at varied switching frequency, duty ratio and DC input voltage. COOLMOS advantage of having lower switching losses is verified experimentally. However, COOLMOS and MOSFET switches are unable to operate properly at a very high switching frequency (> 5 MHz) due to the limitation of their internal structure. Nevertheless, COOLMOS has an advantage in high voltage application since the breakdown voltage is higher compared to MOSFET. Therefore, it is worth to substitute the conventional MOSFET with COOLMOS in a high frequency inverter circuit design for UPS application to meet the needs of lower switching energy losses with greater efficiency at a lower cost.

5.2 Recommendations

A few recommendations for future works of this project are:

- It is better if the Electrical and Electronics engineering Final Year Project (EE FYP) committee could develop a systematic filing database of manual and procedures for software and equipments for the ease of students in executing a project.
- Further investigation on the internal structure of the switches to appreciate and gain better understanding on the switching behaviors.
- More parameters are to be investigated in verifying the superior performances of COOLMOS in different application-wise such as the heatsink design and total harmonic distortion.

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APPENDIX 1

GANTT CHART

Gantt Chart for Final Year Project 1, January Semester 2005

NAME : **Siti Sakinah Sari'at 2565**

FYP TITLE : **Comparative Study of COOLMOS and MOSFET for High Frequency Inverter Design**

NO.	DETAIL / WEEK	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1.0	*Selection of Project Topic*	▨													
	- Introductory FYP Briefing														
	- Approval on Project Title Selection and Synopsis														
2.0	*Preliminary Research work*	▨	▨	▨	▨										
	- Introduction														
	- Objective														
	- Project Planning														
	- List of References / Literature review														
3.0	*Submission of Preliminary Report*				O										
4.0	*Project Work*				▨	▨	▨	▨	▨	▨					
	- Reseacrh work of Reference / Literature														
	- Practical / Laboratory works														
5.0	*Submission of Progress Report*									O					
6.0	*Project Work Continue*									▨	▨	▨	▨		
7.0	*Submission of Interim Report Final Draft*												O		
8.0	*Oral Presentation*													O	
9.0	*Submission of Project Dissertation*														O

NOTE : O Milestone ▨ Process

Gantt Chart for Final Year Project 2, May Semester 2005

NAME :Siti Sakinah Sari'at 2565

FYP TITLE :Comparative Study of COOLMOS and MOSFET for High Frequency Inverter Design

NO.	DETAIL / WEEK	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
1.0	*Project Work Continue*	▨	▨	▨	▨																	
	- Familiarization with Multisim 2001 software																					
	- Selecting and purchasing the components																					
2.0	*Submission of Progress Report 1*				O																	
3.0	*Project Work*				▨	▨	▨	▨	▨													
	- Construction of inverter circuit on PCB																					
4.0	*Submission of Progress Report 2*								O													
5.0	*Project Work continue*								▨	▨	▨	▨	▨	▨								
	- Practical/Laboratory Work																					
	- Experimentation execution																					
6.0	*Submission of Draft Report*													O								
7.0	*Submission of Final Report (Soft Cover)*															O						
8.0	*Submission of Technical Report*															O						
9.0	*Oral Presentation*																			O		
10.0	*Submission of Final Report (Hard Cover)*																					O

NOTE : O Milestone ▨ Process

APPENDIX 2

EXTRA-INVESTIGATION SIMULATIONS

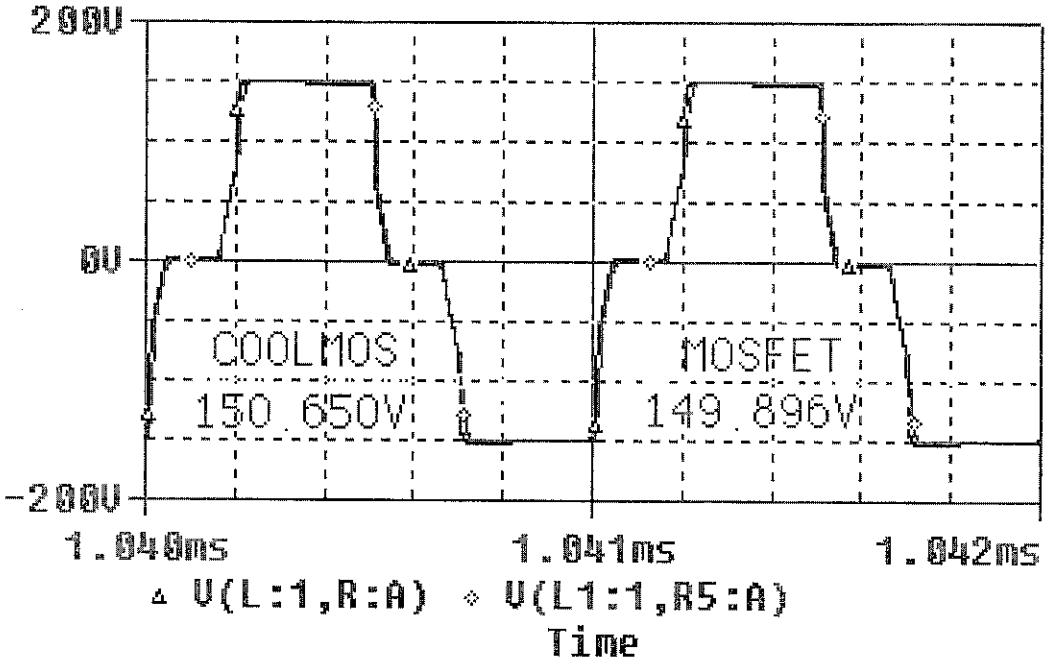


Figure 1 Output Voltage, V_o with V_{in} = 150V, f = 1 MHz and D = 0.5

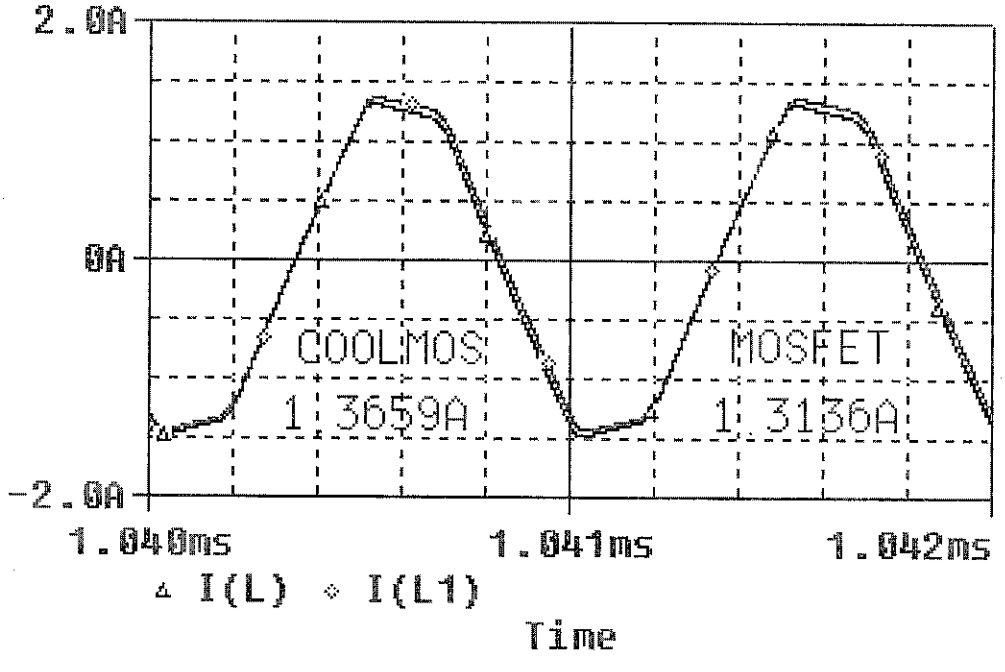


Figure 2 Output Current, I_o with V_{in} = 150V, f = 1 MHz and D = 0.5

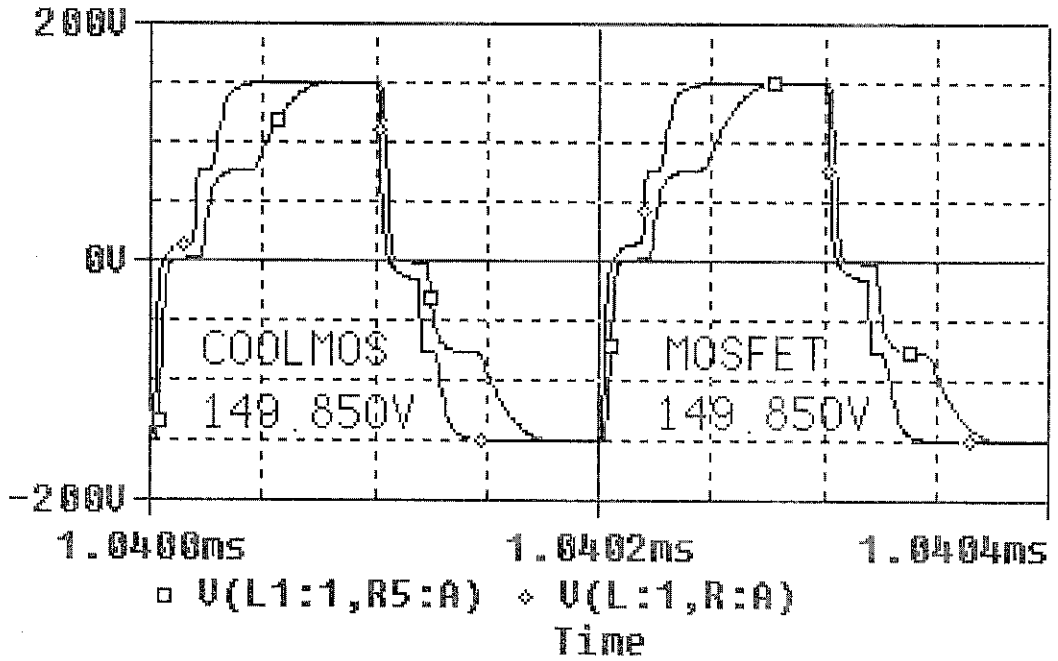


Figure 3 Output Voltage, V_o with V_{in} = 150V, f = 5 MHz and D = 0.5

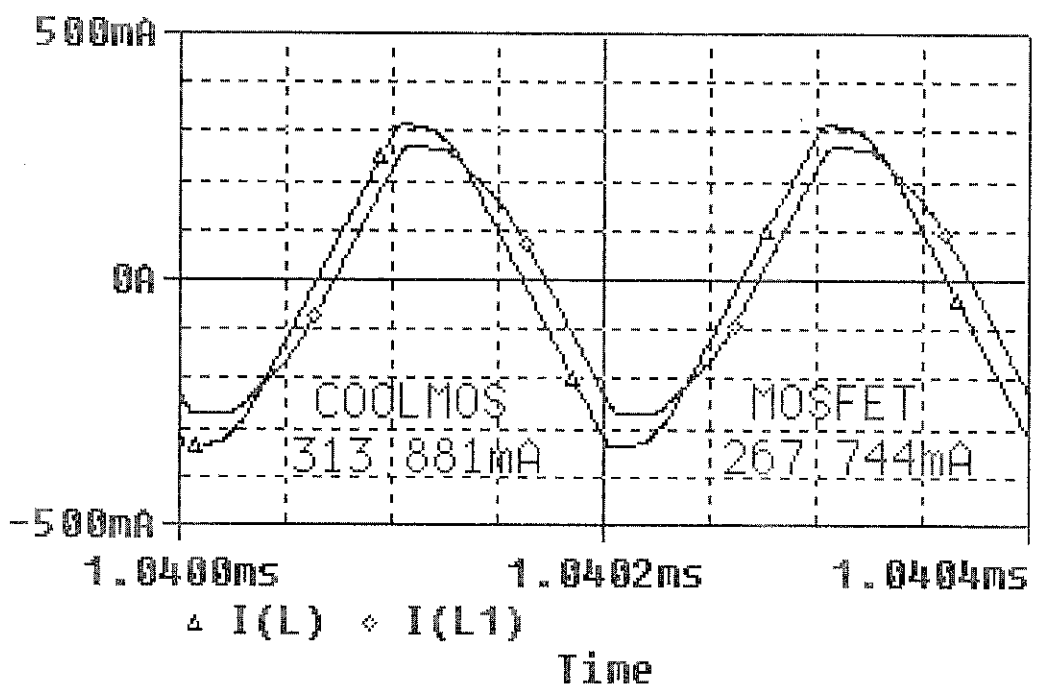


Figure 4 Output Current, I_o with V_{in} = 150V, f = 5 MHz and D = 0.5

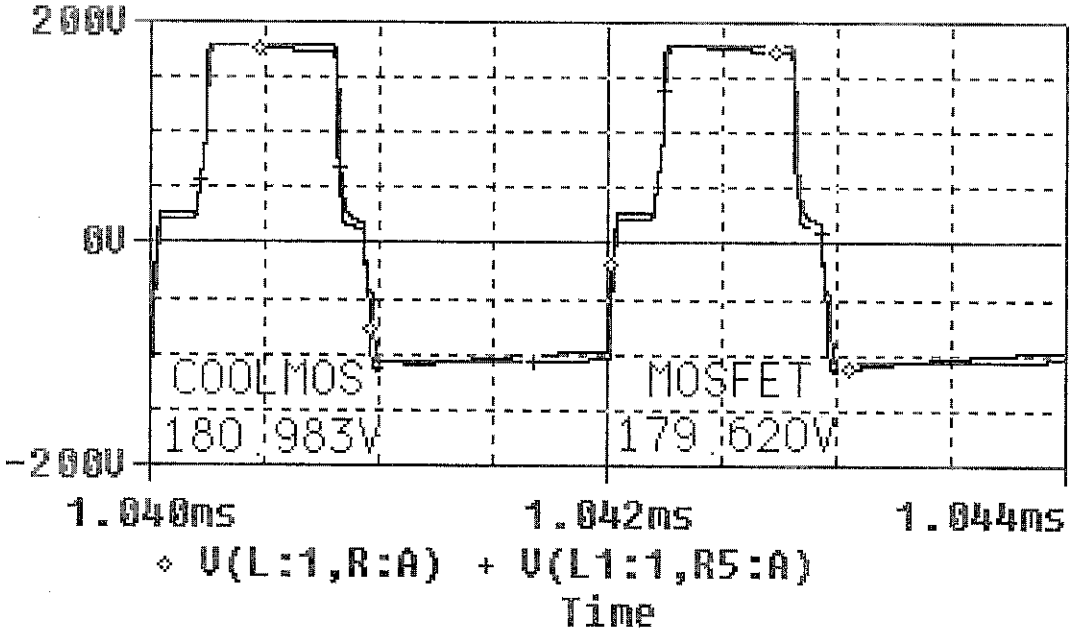


Figure 5 Output Voltage, V_o with V_{in} = 150V, f = 500 kHz and D = 0.4

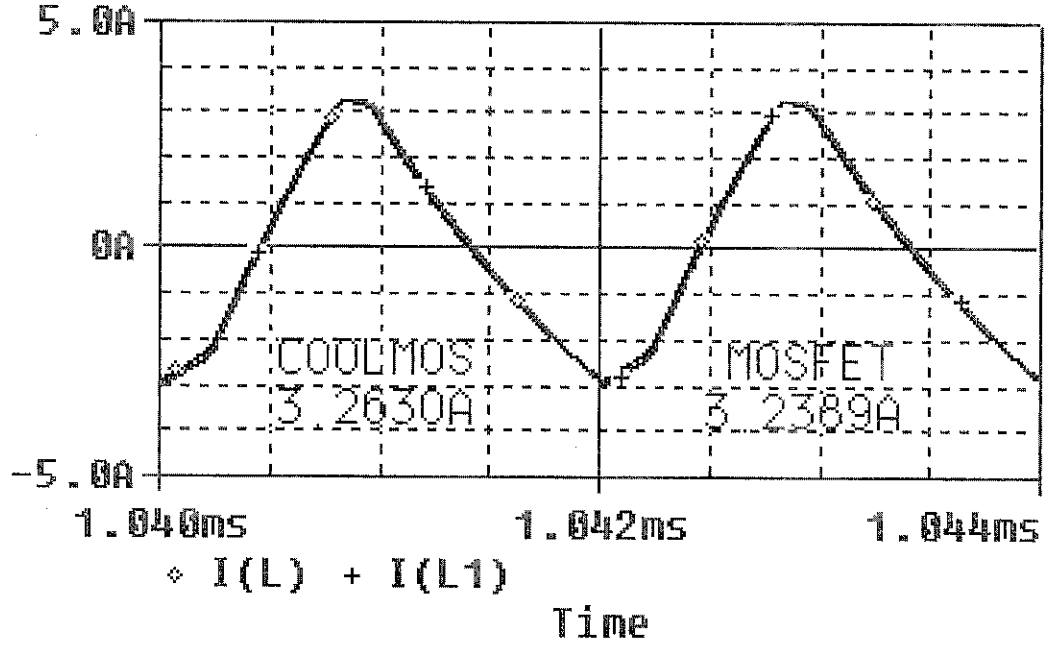


Figure 6 Output Current, I_o with V_{in} = 150V, f = 500 kHz and D = 0.4

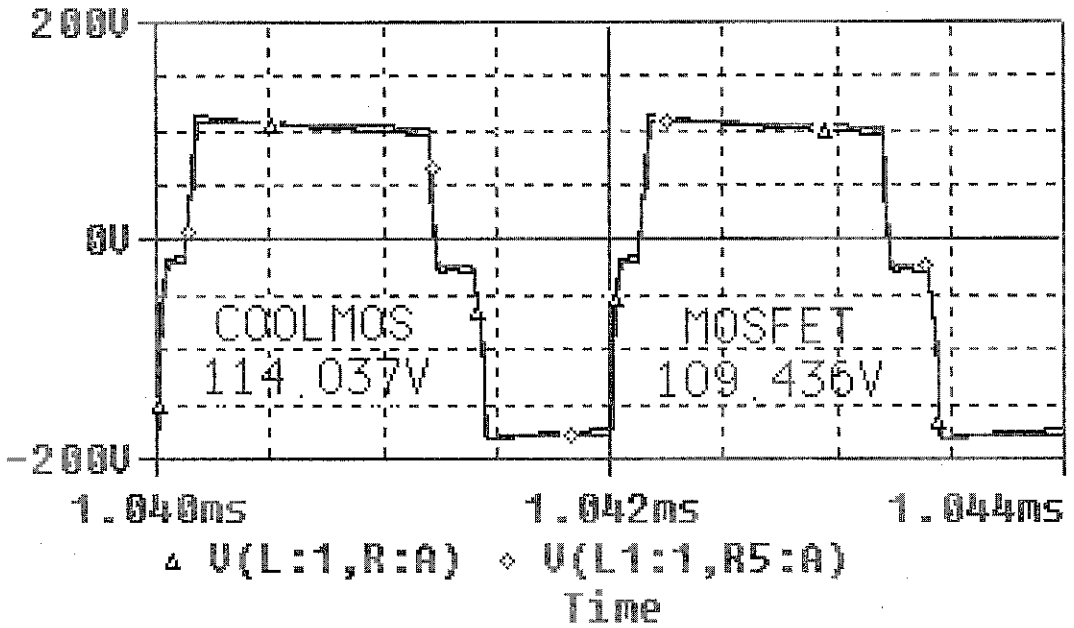


Figure 7 Output Voltage, V_o with V_{in} = 150V, f = 500 kHz and D = 0.6

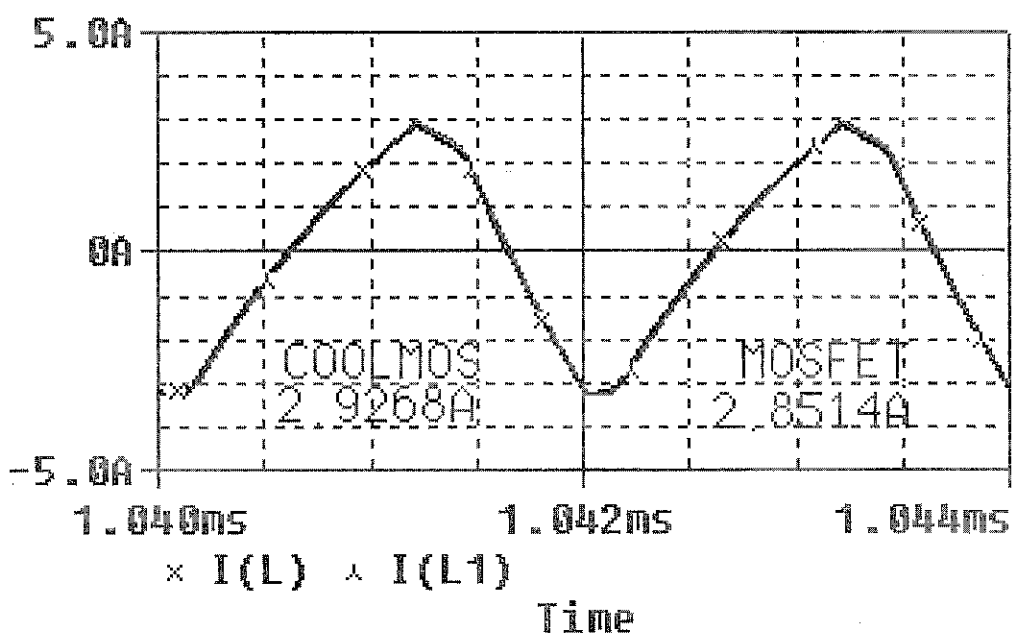


Figure 8 Output Current, I_o with V_{in} = 150V, f = 500 kHz and D = 0.6

APPENDIX 3

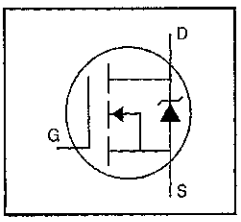
DATASHEETS

International IOR Rectifier

IRFBC40

HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements



V_{DSS} = 600V

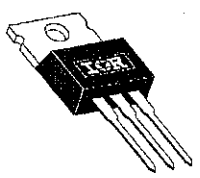
$R_{DS(on)}$ = 1.2Ω

I_D = 6.2A

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



TO-220AB

DATA SHEETS

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10 V	6.2	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10 V	3.9	
I_{DM}	Pulsed Drain Current ①	25	
P_D @ T_C = 25°C	Power Dissipation	125	W
	Linear Derating Factor	1.0	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	570	mJ
I_{AR}	Avalanche Current ①	6.2	A
E_{AR}	Repetitive Avalanche Energy ①	13	mJ
dv/dt	Peak Diode Recovery dv/dt ③	3.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	1.0	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	600	—	—	V	V_{GS}=0V, I_D= 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.70	—	V/°C	Reference to 25°C, I_D= 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	1.2	Ω	V_{GS}=10V, I_D=3.7A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS}=V_{GS}, I_D= 250μA
g_{fs}	Forward Transconductance	4.7	—	—	S	V_{DS}=100V, I_D=3.7A ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	100	μA	V_{DS}=600V, V_{GS}=0V
		—	—	500		V_{DS}=480V, V_{GS}=0V, T_J=125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS}=20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS}=-20V
Q_g	Total Gate Charge	—	—	60	nC	I_D=6.2A
Q_{gs}	Gate-to-Source Charge	—	—	8.3		V_{DS}=360V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	30		V_{GS}=10V See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	13	—	ns	V_{DD}=300V
t_r	Rise Time	—	18	—		I_D=6.2A
$t_{d(off)}$	Turn-Off Delay Time	—	55	—		R_G=9.1Ω
t_f	Fall Time	—	20	—		R_D=47Ω See Figure 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1300	—	pF	V_{GS}=0V
C_{oss}	Output Capacitance	—	160	—		V_{DS}=25V
C_{rss}	Reverse Transfer Capacitance	—	30	—		f=1.0MHz See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	6.2	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	25		
V_{SD}	Diode Forward Voltage	—	—	1.5	V	T_J=25°C, I_S=6.2A, V_{GS}=0V ④
t_{rr}	Reverse Recovery Time	—	450	940	ns	T_J=25°C, I_F=6.2A
Q_{rr}	Reverse Recovery Charge	—	3.8	7.9	μC	di/dt=100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is neglegible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

② V_{DD}=50V, starting T_J=25°C, L=27mH R_G=25Ω, I_{AS}=6.2A (See Figure 12)

③ I_{SD}≤6.2A, di/dt≤80A/μs, V_{DD}≤$V_{(BR)DSS}$, T_J≤150°C

④ Pulse width ≤ 300 μs; duty cycle ≤2%.

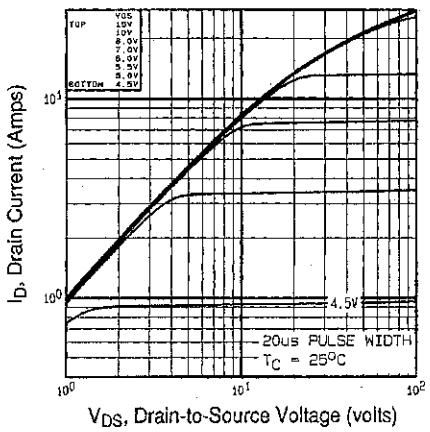


Fig 1. Typical Output Characteristics, T_C=25°C

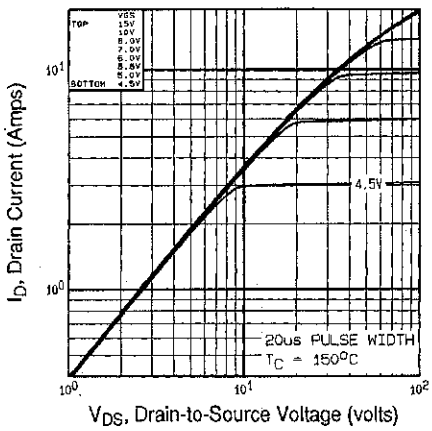


Fig 2. Typical Output Characteristics, T_C=150°C

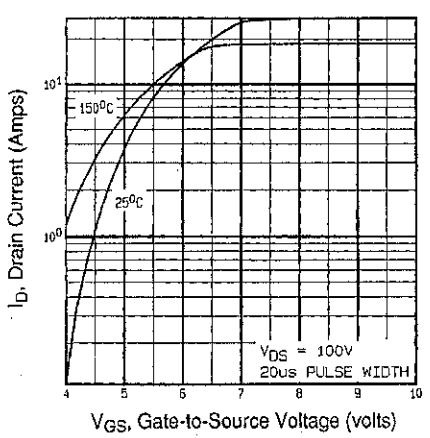


Fig 3. Typical Transfer Characteristics

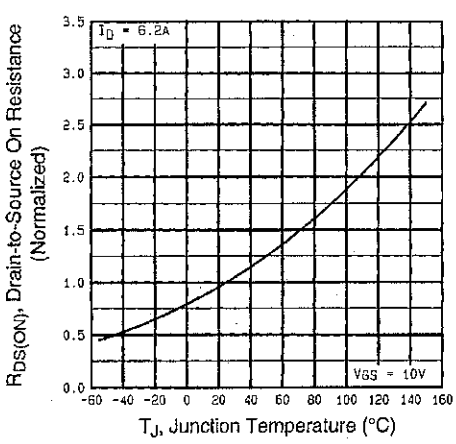


Fig 4. Normalized On-Resistance Vs. Temperature

DATA SHEETS

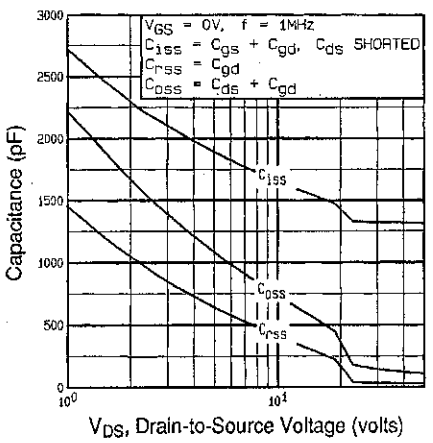


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

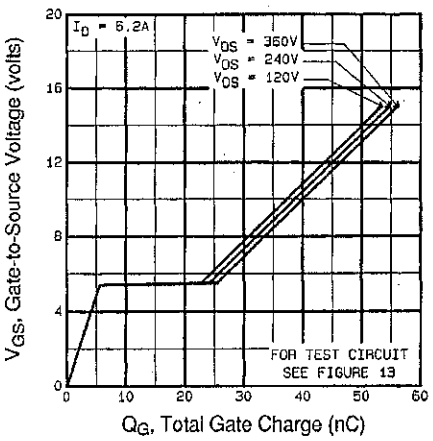


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

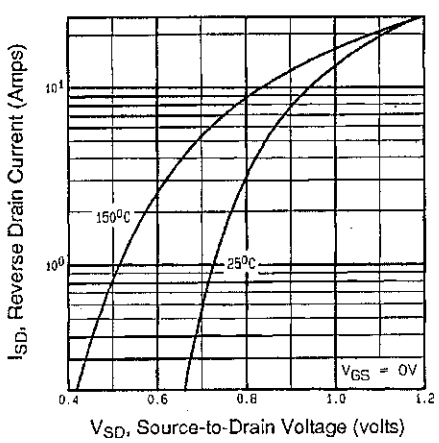


Fig 7. Typical Source-Drain Diode Forward Voltage

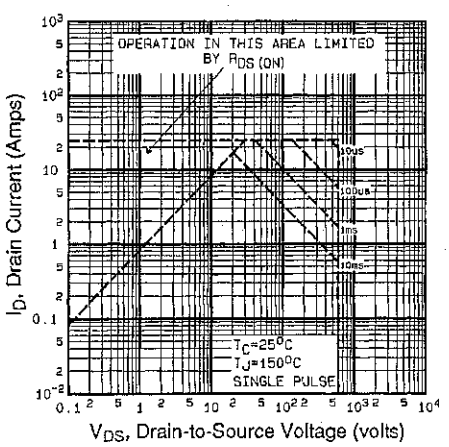


Fig 8. Maximum Safe Operating Area

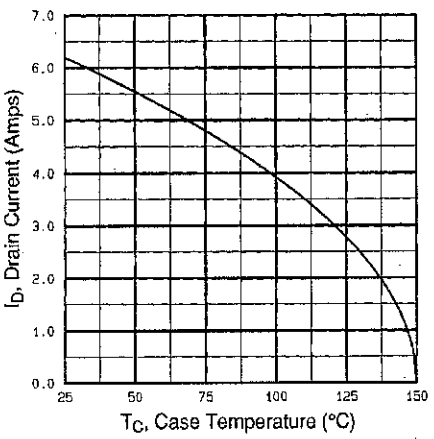


Fig 9. Maximum Drain Current Vs. Case Temperature

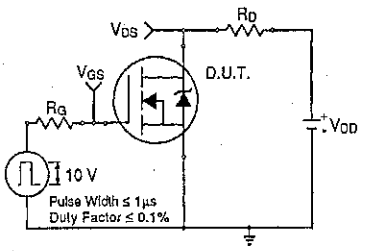


Fig 10a. Switching Time Test Circuit

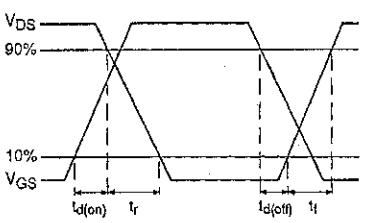


Fig 10b. Switching Time Waveforms

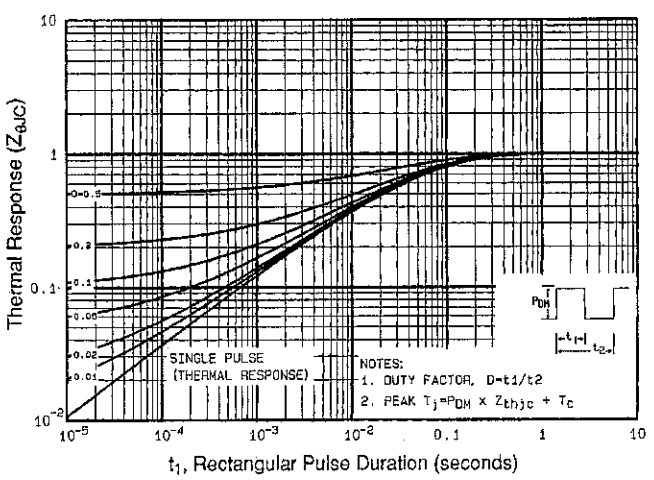


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

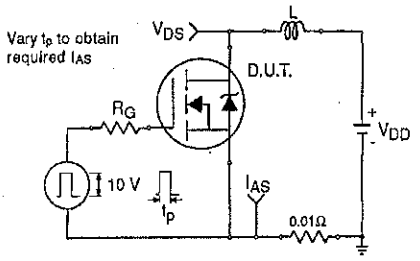


Fig 12a. Unclamped Inductive Test Circuit

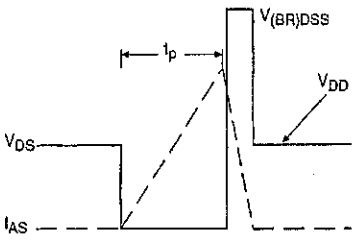


Fig 12b. Unclamped Inductive Waveforms

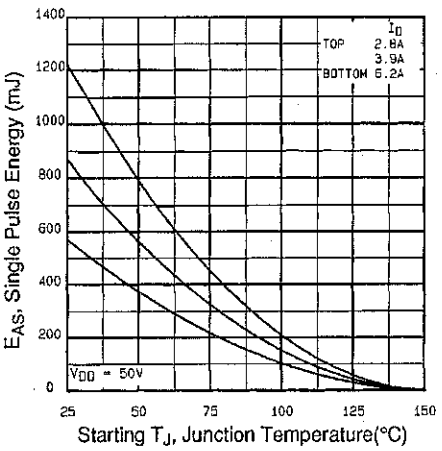


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

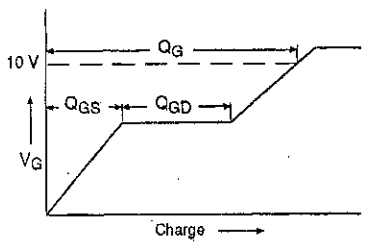


Fig 13a. Basic Gate Charge Waveform

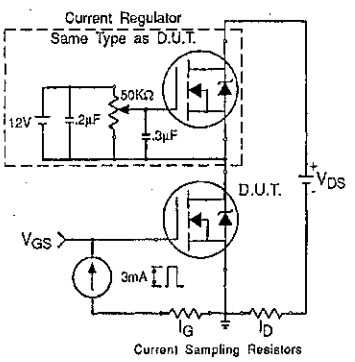


Fig 13b. Gate Charge Test Circuit

Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit – See page 1505

Appendix B: Package Outline Mechanical Drawing – See page 1509

Appendix C: Part Marking Information – See page 1516

Appendix E: Optional Leadforms – See page 1525

International
IOR Rectifier

W TO ORDER

tary Type Designation: Styles CK05, CK06

values, tolerances, voltages, sizes, configurations and ectrics not shown, contact AVX facilities directly nformation.

: Number Example CK05 BX 104 K

e

age-Temperature Limits

acitance Code

acitance Tolerance

Part No. Codes

e: **CK** = General purpose, ceramic dielectric, fixed capacitors.
05 = Remaining two numbers identify shape and dimension.

age-Temperature Limits:
rst letter identifies temperature range.
B = -55°C to +125°C

econd letter identifies voltage-temperature coefficient.

Capacitance Change with Reference to 25°C		
Second Letter	No Voltage	Rated Voltage
X	+15, -15%	+15, -25%

Fig. Capacitance and Multiplier:
irst two digits are the significant figures of capacitance. hird digit indicates the additional number of zeros. or example, order 100,000 pF as 104.

acitance Tolerances: K = ±10%, M = ±20%

kaging: CK05 1000 per bag
CK06 1000 per bag
Radial tape and reel packaging available upon request (2500 pcs./reel).

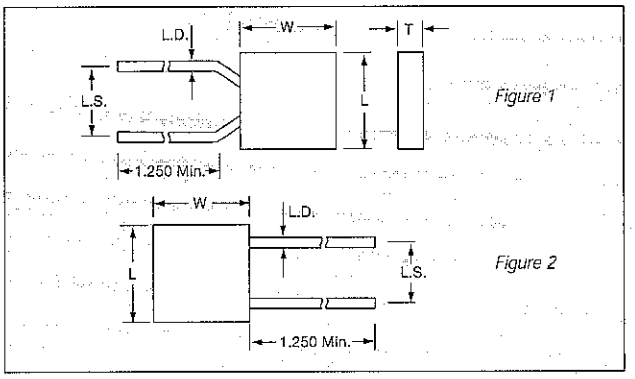


Figure 1

Figure 2

SIZE SPECIFICATIONS

Dimensions: Millimeters (Inches)

Case Size	Per MIL Spec	
MIL-C-11015	CK05 (Fig. 1)	CK06 (Fig. 2)
Length (L)	4.83±.25 (.190±.010)	7.37±.25 (.290±.010)
Width (W)	4.83±.25 (.190±.010)	7.37±.25 (.290±.010)
Thickness (T)	2.29±.25 (.090±.010)	2.29±.25 (.090±.010)
Lead Spacing (L.S.)	5.08±.38 (.200±.015)	5.08±.38 (.200±.015)
Lead Diameter (L.D.)	.64±.05 (.025±.002)	.64±.05 (.025±.002)

ry Part Number Identification CK05 and CK06

ilitary Type esignation	Capacitance (pF)	Capacitance Tolerance	WVDC
	CK05 (BX)		
05BX100_	10	K, M	200
05BX120K_	12	K	200
05BX150_	15	K, M	200
05BX180K_	18	K	200
05BX220_	22	K, M	200
05BX270K_	27	K	200
05BX330_	33	K, M	200
05BX390K_	39	K	200
05BX470_	47	K, M	200
05BX560K_	56	K	200
05BX680_	68	K, M	200
05BX820K_	82	K	200
05BX101_	100	K, M	200
05BX121K_	120	K	200
05BX151_	150	K, M	200
05BX181K_	180	K	200
05BX221_	220	K, M	200
05BX271K_	270	K	200
05BX331_	330	K, M	200
05BX391K_	390	K	200
05BX471_	470	K, M	200
05BX561K_	560	K	200
05BX681_	680	K, M	200
05BX821K_	820	K	200
05BX102_	1,000	K, M	200
05BX122_	1,200	K	100
05BX152_	1,500	K, M	100
05BX182K_	1,800	K	100
05BX222_	2,200	K, M	100
05BX272K_	2,700	K	100
05BX332_	3,300	K, M	100
05BX392K_	3,900	K	100
05BX472_	4,700	K, M	100
05BX562K_	5,600	K	100
05BX682_	6,800	K, M	100
05BX822K_	8,200	K	100
05BX103_	10,000	K, M	100
05BX123K_	12,000	K	50
05BX153_	15,000	K, M	50
05BX183K_	18,000	K	50
05BX223_	22,000	K, M	50
05BX273K_	27,000	K	50
05BX333_	33,000	K, M	50
05BX393K_	39,000	K	50
05BX473_	47,000	K, M	50
05BX563K_	56,000	K	50
05BX683_	68,000	K, M	50
05BX823K_	82,000	K	50
05BX104_	100,000	K, M	50

Add Capacitance Tolerance Letter K = ±10% or M = ±20%

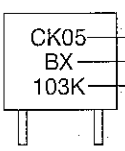
Military Type Designation	Capacitance (pF)	Capacitance Tolerance	WVDC
	CK06 (BX)		
CK06BX122K_	1,200	K	200
CK06BX152_	1,500	K, M	200
CK06BX182K_	1,800	K	200
CK06BX222_	2,200	K, M	200
CK06BX272K_	2,700	K	200
CK06BX332_	3,300	K, M	200
CK06BX392K_	3,900	K	200
CK06BX472_	4,700	K, M	200
CK06BX562K_	5,600	K	200
CK06BX682_	6,800	K, M	200
CK06BX822K_	8,200	K	200
CK06BX103_	10,000	K, M	200
CK06BX123K_	12,000	K	100
CK06BX153_	15,000	K, M	100
CK06BX183K_	18,000	K	100
CK06BX223_	22,000	K, M	100
CK06BX273K_	27,000	K	100
CK06BX333_	33,000	K, M	100
CK06BX393K_	39,000	K	100
CK06BX473_	47,000	K, M	100
CK06BX563K_	56,000	K	100
CK06BX683_	68,000	K, M	100
CK06BX823K_	82,000	K	100
CK06BX104_	100,000	K, M	100
CK06BX124K_	120,000	K	50
CK06BX154_	150,000	K, M	50
CK06BX184K_	180,000	K	50
CK06BX224_	220,000	K, M	50
CK06BX274K_	270,000	K	50
CK06BX334_	330,000	K, M	50
CK06BX394K_	390,000	K	50
CK06BX474_	470,000	K, M	50
CK06BX564K_	560,000	K	50
CK06BX684_	680,000	K, M	50
CK06BX824K_	820,000	K	50
CK06BX105_	1.0 mfd	K, M	50

Add Capacitance Tolerance Letter K = ±10% or M = ±20%

KING

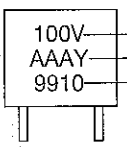
CK05/CK06

Front



Style
Temperature Characteristic
Capacitance Value
(3 digit code) and Capacitance Tolerance

Back

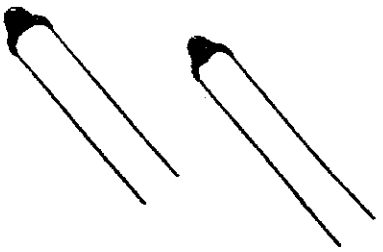


Voltage Rating
A for AVX; Plant I.D. (X); Lot Code (XX)
Date Code

CERAMIC CAPACITORS
MEDIUM VOLTAGE CAPACITORS 1KV to 6KVDC
E.I.A. CLASS II & III

murata

DE Series



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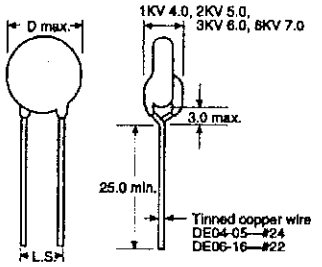
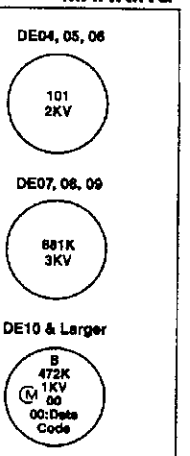


MARKING*



*Three-digit capacitance code for values of 100pF and larger. SL and F have no temperature characteristic marking.

PART NUMBERING SYSTEM

TYPE	LEADS	TEMP. CHAR.	CAPACITANCE	TOL.	VOLTAGE
DE04	05	B	101	K	1K

CAPACITOR TYPE AND SIZE

LEAD SPACING
05 = 5
07 = 7.5
10 = 10

TEMPERATURE CHARACTERISTICS
Class I: Per standard EIA specifications.
Class II & III:
TEMPERATURE RANGE: –25°C to +85°C
MAX. CAP. CHANGE OVER TEMP. RANGE:
B = ±10%
E = +20, –55%
F = +30, –80%

CAPACITANCE VALUE

CAPACITANCE TOLERANCE
J = ±5%
K = ±10%
Z = +80, –20%

VOLTAGE
Identified by a one-digit number

Note: B, E, F are JIS codes that are similar to EIA temperature characteristics Y5P, Y5U and Y5V respectively.

1KV – B

PART NUMBER	DIA (mm)	LS (mm)	CAP (pF)
DE0405B101K1K	4.5	5	100
DE0405B151K1K	4.5	5	150
DE0405B221K1K	4.5	5	220
DE0405B331K1K	4.5	5	330
DE0506B471K1K	5	5	470
DE0605B681K1K	6	5	680
DE0605B102K1K	6	5	1000
DE0805B152K1K	8	5	1500
DE0905B222K1K	9	5	2200
DE1006B332K1K	10	5	3300
DE1205B472K1K	12	5	4700
DE1510B682K1K	15	10	6800

2KV – B

DE0405B101K2K	4.5	5	100
DE0405B151K2K	4.5	5	150
DE0405B221K2K	4.5	5	220
DE0505B331K2K	5	5	330
DE0605B471K2K	6	5	470
DE0705B681K2K	7	5	680
DE0805B102K2K	8	5	1000
DE0905B152K2K	9	5	1500
DE1005B222K2K	10	5	2200
DE1205B332K2K	12	5	3300
DE1510B472K2K	15	10	4700

★3KV – B

PART NUMBER	DIA (mm)	LS (mm)	CAP (pF)
DE0507B101K3K	5	7.5	100
DE0507B151K3K	5	7.5	150
DE0507B221K3K	5	7.5	220
DE0607B331K3K	6	7.5	330
DE0707B471K3K	7	7.5	470
DE0807B681K3K	8	7.5	680
DE0907B102K3K	9	7.5	1000
DE1107B152K3K	11	7.5	1500
DE1307B222K3K	13	7.5	2200
DE1510B332K3K	15	10	3300

★6KV – B

DE0910B101K6K	9	10	100
DE0910B151K6K	9	10	150
DE0910B221K6K	9	10	220
DE0910B331K6K	9	10	330
DE1010B471K6K	10	10	470
DE1110B681K6K	11	10	680
DE1310B102K6K	13	10	1000

CERAMIC CAPACITORS
MEDIUM VOLTAGE CAPACITORS 1KV to 6KVDC
E.I.A. CLASS II & III

muRata

DE Series

1KV – E

DE0505E102Z1K	5	5	1000
DE0705E222Z1K	7	5	2200
DE0905E472Z1K	9	5	4700
DE1307E103Z1K	13	7.5	10000

2KV – E

DE0605E102Z2K	6	5	1000
DE0805E222Z2K	8	5	2200
DE1105E472Z2K	11	5	4700
DE1610E103Z2K	16	10	10000

3KV – E

DE0707E102Z3K	7	7.5	1000
DE1007E222Z3K	10	7.5	2200
DE1307E472Z3K	13	7.5	4700

6KV – E

DE1110E102Z6K	11	10	1000
DE1510E222Z6K	15	10	2200

1KV – F

DE0605F222Z1K	6	5	2200
DE0705F472Z1K	7	5	4700
DE1005F103Z1K	10	5	10000

2KV – F

DE0505F102Z2K	5	5	1000
DE0705F222Z2K	7	5	2200
DE0905F472Z2K	9	5	4700
DE1205F103Z2K	12	5	10000

Available as standard through authorized Murata Electronics Distributors.

CERAMIC CAPACITORS

SPECIFICATIONS: CLASS II & III

Test Conditions: Unless otherwise specified, measurements shall be made at +25°C, ±10°C, a relative humidity no greater than 75%, and normal atmospheric pressure.

Capacitance: Capacitance shall be within the specified limits when measured at, or corrected to, a temperature of +20°C, a VMS voltage between .05 and 5.0, and a frequency of 1KHz.

Dissipation Factor, or (Ratio of Equivalent Series Resistance to Reactance): Dissipation Factor shall not be greater than 2.5% for B and E characteristics, or greater than 5% for F.

Insulation Resistance: 10,000MΩ minimum when measured between terminals of capacitor 1 minute after application of a DC test voltage of 500 applied through a protective resistance which will limit the charging current to 50mA.

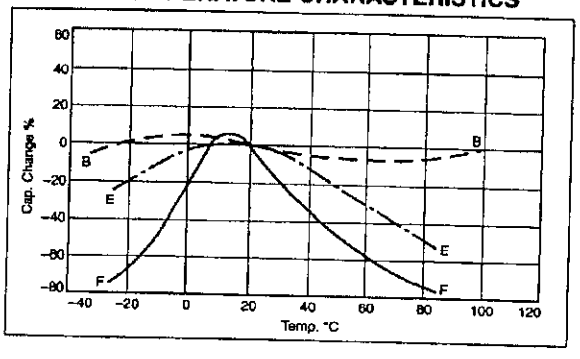
Dielectric Strength: Capacitors shall be subjected to a DC voltage equal to 200% of their rated working voltage. This voltage shall be applied for 5, ±1 seconds through a protective resistance that will limit the charging current to 50mA.

Humidity Resistance: After exposure for a period of 500 hours to an atmosphere of 95% relative humidity at a temperature of 40°C, capacitor shall have a minimum insulation resistance of 1,000MΩ.

Life: Capacitors shall be subjected to a DC voltage equal to 150% of the rated working voltage for 1,000 hours at +85°C. After this test, dissipation factor shall not be more than twice the stated initial value, and insulation resistance shall not be less than 2,000MΩ.

Encapsulation: Ceramic disc is coated in an epoxy resin which conforms to UL94V-0.

TYPICAL TEMPERATURE CHARACTERISTICS



e structure of the "Global Part Numbers" that have been adopted since June 2001 and the meaning of each code are described herein.
/ou have any questions about details, inquire at your usual Murata sales office or distributor.

art Numbering

ligh Voltage Ceramic Capacitors (250V-6.3kV)

Global Part Number) DE | B | B3 | 3A | 102 | K | N2 | A
❶ ❷ ❸ ❹ ❺ ❻ ❼ ❽

❶Product ID

Product ID	
DE	High-voltage (250V - 6.3kV) / Safety Standard Recognized Ceramic Capaictors

❸Series Category

Code	Outline	Contents
A	High-Voltage	Class1 (char. SL) DC1-3.15kV Rated
B		Class2 DC1-3.15kV Rated
C		Class 1,2 DC6.3kV Rated
H		High Temperature Guaranteed, Low-dissipation Factor (char. R, C)

rst three digit (❶Product ID and ❸Series Category) express "Series ame".

❹Temperature Characteristics

Code	Temperature Characteristics	Cap.Change or Temp. Coeff.	Temperature Range
B3	B	±10%	−25 to +85℃
E3	E	+20%,−55%	
F3	F	+30%,−80%	
C3	C	±20%	−25 to +85℃
		+15%,−30%	+85 to +125℃
R3	R	±15%	−25 to +85℃
		+15%,−30%	+85 to +125℃
1X	SL	+350 to −1000ppm/℃	+20 to +85℃

❺Rated Voltage

Code	Rated Voltage
2E	DC250V
2H	DC500V
3A	DC1kV
3D	DC2kV
3F	DC3.15kV
3J	DC6.3kV

❻Capacitance

xpressed by three figures. The unit is pico-farad(pF). The first nd second figures are significant digits, and the third figure xpresses the number of zeros which follow the two numbers. there is a decimal point, it is expressed by the capital letter "R". ı this case, all figures are significant digits.

❻Capacitance Tolerance

Code	Capacitance Tolerance
J	±5%
K	±10%
Z	+80%, −20%

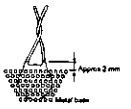
❼Lead Style

Code	Lead Style	Dimensions(mm)		
		Lead Spacing	Lead Diameter	Pitch of Components
A2	Vertical Crimp Long	5	ø0.6±0.05	—
A3		7.5		
A4		10		
B2	Vertical Crimp Short	5	ø0.6±0.05	—
B3		7.5		
B4		10		
C1	Straight Long	5	ø0.5±0.05	—
C3		7.5	ø0.6±0.05	
C4		10		
CD		7.5	ø0.5±0.05	
D1	Straight Short	5	ø0.5±0.05	—
D3		7.5	ø0.6±0.05	
DD		7.5	ø0.5±0.05	
N2	Vertical Crimp Taping	5	ø0.6±0.05	12.7
N3		7.5		15
N7		7.5		30
P2	Straight Taping	5	ø0.6±0.05	12.7
P3		7.5		15

❽Packaging

Code	Packaging
A	Ammo Pack
B	Bulk

■SPECIFICATION AND TEST METHOD

	Item		Specification		Testing Method
			Temp. Compensating	High Dielectric Constant	
1	Operating Temperature Range		−25 to +85℃	−25 to +85℃	—
2	Capacitance		Within the specified tolerance.	Within the specified tolerance.	The capacitance shall be measured at 20℃ with 1±0.2kHz (SL : 1±0.2MHz) and 5Vrms max.
3	Q Dissipation Factor (D. F.)		SL: C≧30pF : Q≧1000; C<30pF : Q≧400+20C[1]	B, E: D. F.≦2.5%; F: D. F.≦5.0%	Same condition as capacitance.
4	Insulation Resistance (I. R.)	Between Lead wires	10000MΩ min.	10000MΩ min.	The insulation resistance shall be measured with 500±50VDC within 60±5 sec. of charging.
5	Dielectric Strength	Between Lead wires	No failure.	No failure.	The capacitors shall not be damage when DC voltage of 200% of the rated voltage are applied between the lead wires for 1 to 5 sec. (Charge/discharge current≦50mA)
		Body Insulation	No failure.	No failure.	The capacitor is placed in the container with metal balls of diameter 1mm so that each lead wire, shortcircuited, is kept approximately 2mm off the balls as shown in the figure, and DC voltages of 1.3kV is applied for 1 to 5 sec. between capacitor lead wires and small metals. (Charge / discharge current≦50mA) 
6	Temperature Characteristic		T.C: SL; Temp. Coefficient: +350 to −1000ppm / ℃ (Temp. Range : +20 to +85℃)	T.C: B: within±10%; E: within$^{+20}_{-55}$%; F: within$^{+30}_{-80}$%	The capacitance measurement shall be made at each step specified in table. Capacitance change from the value of step 3 shall not exceed the limit specified. Step: 1: 20±2℃; 2: −25±3℃; 3: 20±2℃; 4: 85±2℃; 5: 20±2℃ Pre-treatment : Capacitor shall be stored at 85±2℃ for 1 hour, then placed at [2] room condition for 24±2 hours before initial measurements. (B,E,F)
7	Vibration Resistance	Appearance	No marked defect.	No marked defect.	The capacitor shall firmly be soldered to the supporting lead wire and vibration which is 10 to 55Hz in the vibration frequency range, 1.5mm in total amplitude, and about 1 minute in the rate of vibration change from 10Hz to 55Hz and back to 10Hz is applied for a total of 6 hours; 2 hours each in 3 mutually perpendicular directions.
		Capacitance	Within the specified tolerance.	Within the specified tolerance.	
		Q D. F.	SL: C≧30pF : Q≧1000; C<30pF : Q≧400+20C[1]	B, E: D. F.≦2.5%; F: D. F.≦5.0%	
8	Soldering Effect	Appearance	No marked defect.	No marked defect.	The lead wire shall be immersed into the melted solder of 350±10℃ (Body of ϕ5 and under : 270±5℃) up to about 1.5 to 2mm from the main body for 3.5±0.5 sec. (Body of ϕ5 and under : 5±0.5sec.) . Pre-treatment : Capacitor shall be stored at 85±2℃ for 1 hour, then placed at [2] room condition for 24±2 hours before initial measurements. (B,E,F) Post-treatment : Capacitor shall be stored for 1 to 2 hours at [2] room condition. (SL) Post-treatment : Capacitor shall be stored for 24±2 hours at [2] room condition. (B,E,F)
		Capacitance Change	SL: within±2.5%	B: within±5%; E: within±15%; F: within±20%	
		Dielectric Strength (Between lead wires)	Pass the item No. 5.	Pass the item No. 5.	
9	Humidity (Under Steady State)	Appearance	No marked defect.	No marked defect.	Set the capacitor for 500 $^{+24}_{0}$ hours at 40±2℃ in 90 to 95% humidity. Pre-treatment : Capacitor shall be stored at 85±2℃ for 1 hour, then placed at [2] room condition for 24±2 hours before initial measurements. (B,E,F) Post-treatment : Capacitor shall be stored for 1 to 2 hours at [2] room condition.
		Capacitance Change	SL: within±5%	B: within±10%; E: within±20%; F: within±30%	
		Q D. F.	SL: C≧30pF : Q≧350; C<30pF : Q≧275+$\frac{5}{2}$C[1]	B, E: D. F.≦5.0%; F: D. F.≦7.5%	
		I. R.	1000MΩ min.	1000MΩ min.	
10	Humidity Loading	Appearance	No marked defect.	No marked defect.	Apply the rated voltage for 500 $^{+24}_{0}$ hours at 40±2℃ in 90 to 95% humidity. (Charge / discharge current≦50mA) Pre-treatment : Capacitor shall be stored at 85±2℃ for 1 hour, then placed at [2] room condition for 24±2 hours before initial measurements. (B,E,F) Post-treatment : Capacitor shall be stored for 1 to 2 hours at [2] room condition. (SL) Post-treatment : Capacitor shall be stored at 85±2℃ for 1 hour, then placed at [2] room condition for 24±2 hours. (B,E,F)
		Capacitance Change	SL: within±7.5%	B: within±10%; E: within±20%; F: within±30%	
		Q D. F.	SL: C≧30pF : Q≧200; C<30pF : Q≧100+$\frac{10}{3}$C[1]	B, E: D. F.≦5.0%; F: D. F.≦7.5%	
		I. R.	500MΩ min.	500MΩ min.	
11	Life	Appearance	No marked defect.	No marked defect.	Apply a DC voltage of 150% of the rated voltage for 1000 $^{+48}_{-0}$ hours at 85±2℃. (Charge/discharge current≦50mA) Pre-treatment : Capacitor shall be stored at 85±2℃ for 1 hour, then placed at [2] room condition for 24±2 hours before initial measurements. (B,E,F) Pos-treatment : Capacitor shall be stored for 1 to 2 hours at [2] room condition. (SL) Pos-treatment : Capacitor shall be stored at 85±2℃ for 1 hour, then placed at [2] room condition for 24±2 hours. (B,E,F)
		Capacitance Change	SL: within±3%	B: within±10%; E: within±20%; F: within±30%	
		Q D. F.	SL: C≧30pF : Q≧350; C<30pF : Q≧275+$\frac{5}{2}$C[1]	B, E: D. F.≦4.0%; F: D. F.≦7.5%	
		I. R.	2000MΩ min.	2000MΩ min.	
12	Strength of Lead	Pull	Lead wire shall not cut off. Capacitor shall not be broken.		As a figure, fix the body of capacitor,apply a tensile weight gradually to each lead wire in the radial direction of capacitor up to 10N (1.0kgf) 5N (0.51kgf) for Lead diameter ϕ 0.5) and keep it for 10±1 sec. 
		Bending			Each lead wire shall be subjected to 5N (0.51kgf) 2.5N (0.25kgf) for Lead diameter ϕ0.5) weight and then a 90° bend, at the point of egress, in one direction, return to original position, and then a 90° bend in the opposite direction at the rate of one bend in 2 to 3 seconds.
13	Solderbility of Leads		Lead wire shall be soldered with uniformly coated on the axial direction over $\frac{3}{4}$ of the circumferential direction.		The lead wire of a capacitor shall be dipped into a methanol solution of 25wt% rosin and then into molten solder of 235±5℃ for 2±0.5 seconds. In both cases the depth of dipping is up to about 1.5 to 2mm from the root of lead wires.

[1] "C" expresses nominal capacitance value (pF) .

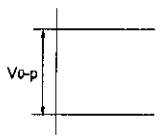
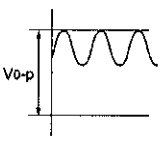
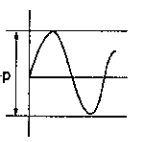
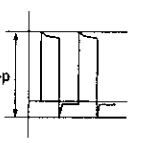
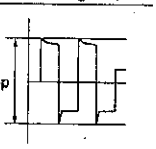
[2] "room condition" temperature : 15 to 35℃, humidity : 45 to 75%, atmospheric pressure : 86 to 106kPa

1. Operating Voltage

When DC-rated capacitors are to be used in AC or ripple current circuits, be sure to maintain the Vp-p value of the applied voltage or the Vo-p which contains DC bias within the rated voltage range.

When the voltage is started to apply to the circuit or it is stopped applying, the irregular voltage may be generated for a transit period because of resonance or switching. Be sure to use a capacitor within rated voltage containing these irregular voltage.

When using the low-dissipation DEA/DEH series in a high-frequency and high-voltage circuit, be sure to read the instructions in item 4.

Voltage	DC Voltage	DC+AC Voltage	AC Voltage	Pulse Voltage (1)	Pulse Voltage (2)
Positional measurement					

2. Operating Temperature and Self-generated Heat

Keep the surface temperature of a capacitor below the upper limit of its rated operating temperature range. Be sure to take into account the heat generated by the capacitor itself. When the capacitor is used in a high-frequency current, pulse current or the like, it may have the self-generated heat due to dielectric-loss.

The allowable frequency should be in less than 300kHz in sine wave. Applied voltage should be the load such as self-generated heat is within 5 °C in case of temperature characteristic SL and within 20°C for other temperature characteristic on the condition of atmosphere temperature 25 °C. When measuring, use a thermocouple of small thermal capacity-K of ø0.1mm and be in the condition where capacitor is not affected by radiant heat of other components and wind of surroundings.

(Never attempt to perform measurement with the cooling fan running. Otherwise, accurate measurement cannot be ensured.)

Before using the low-dissipation DEA/DEH series, be sure to read the instructions in item 4.

3. Fail-Safe

When capacitor would be broken, failure may result in a short circuit. Be sure to provide an appropriate fail-safe function like a fuse on your product if failure would follow an electric shock, fire or fume.

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4. Load Reduction and Self-generated Heat During Application of High-frequency and High-voltage

Since the heat generated by the low-dissipation capacitor itself is low, its allowable power is much higher than the general B characteristic. However, in case such an applied load that the self-heating temperature is 20°C at the rated voltage, the allowable power may be exceeded.

Therefore, when using the DEA/DEH series in a high-frequency and high-voltage circuit with a frequency of 1kHz or higher, make sure that the Vp-p values including the DC bias, do not exceed the applied voltage value specified in Table 1. Also make sure that the self-heating temperature (the difference between the capacitor's surface temperature and the capacitor's ambient temperature) at an ambient temperature of 25°C does not exceed the value specified in Table 1.

As shown in Fig. 2, the self-heating temperature depends on the ambient temperature. Therefore, if you are not able to set the ambient temperature to approximately 25°C, please contact our sales representatives or product engineers.

Failure to follow the above cautions (item 1 to 4) may result, worst case, in a short circuit and cause fuming or partial dispersion when the product is used.

<Table 1> Allowable Conditions at High-frequency

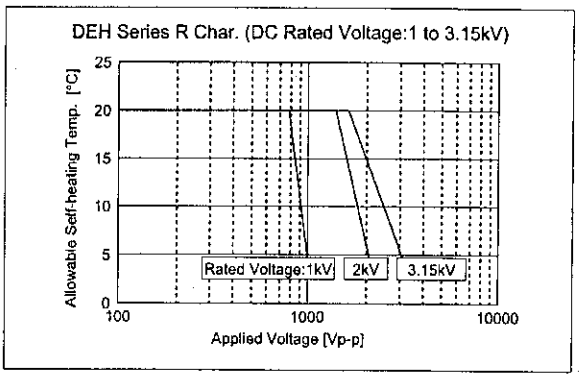
Series	Temp. Char.	DC Rated Voltage	Allowable Conditions at High-frequency *3		Operating Environment Temp. *2
			Applied Voltage (Max.)	Self-heating Temp. (25°C Ambient Temp.) *1	
DEH	R	250V	250Vp-p	10°C Max.	-25 to +85°C
	C	500V	500Vp-p	20°C Max.	
	R	1kV	800Vp-p	20°C Max.	
			1000Vp-p	5°C Max.	
		2kV	1400Vp-p	20°C Max.	
			2000Vp-p	5°C Max.	
		3.15kV	1600Vp-p	20°C Max.	
			3150Vp-p	5°C Max.	
DEA	SL	1kV	1000Vp-p	5°C Max.	
		2kV	2000Vp-p		
		3.15kV	3150Vp-p		

1 Fig. 1 shows the relationship between the applied voltage and the allowable self-heating temperature regarding 1 to 3.15kV rated voltage of the DEH series R characteristic.

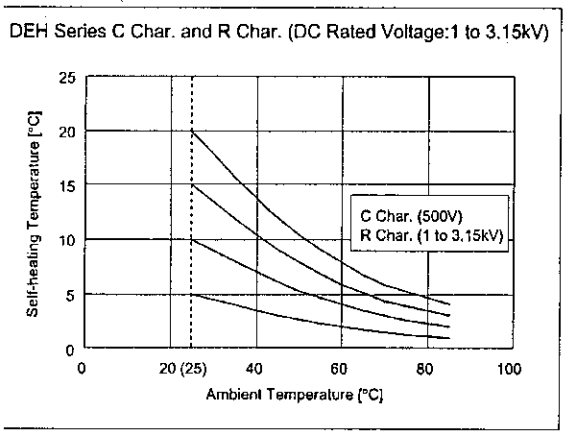
2 When the ambient temperature is 85 to 125°C, the applied voltage needs to be further reduced. If the DEA/DEH series needs to be used at an ambient temperature of 85 to 125°C, please contact our sales representatives or product engineers.

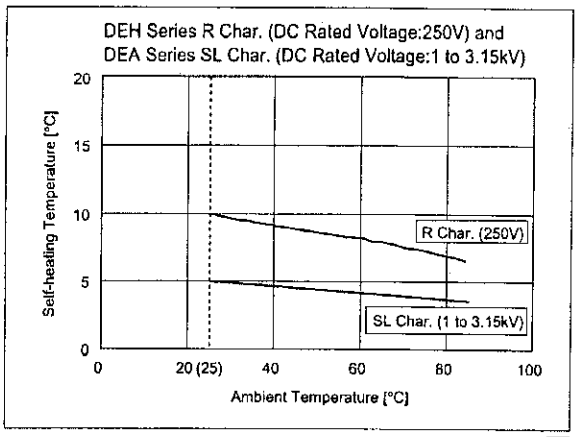
3 Fig. 3 shows reference data on the allowable voltage-frequency characteristic for a sine wave voltage.

<Fig. 1> Relationship Between Applied Voltage and Self-heating Temperature (Allowable Self-heating Temp. at 25°C Ambient Temp.)



<Fig. 2> Dependence of Self-heating Temperature on Ambient Temperature





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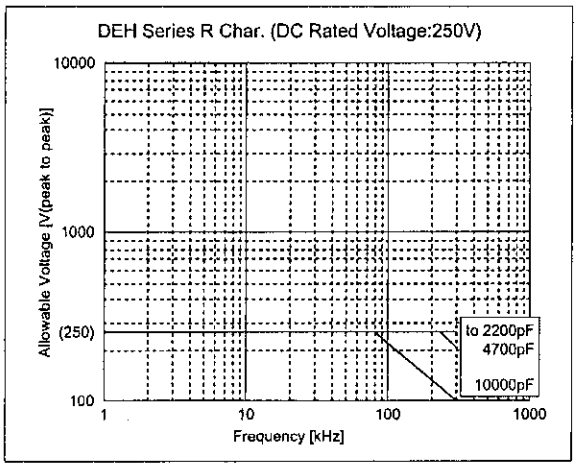
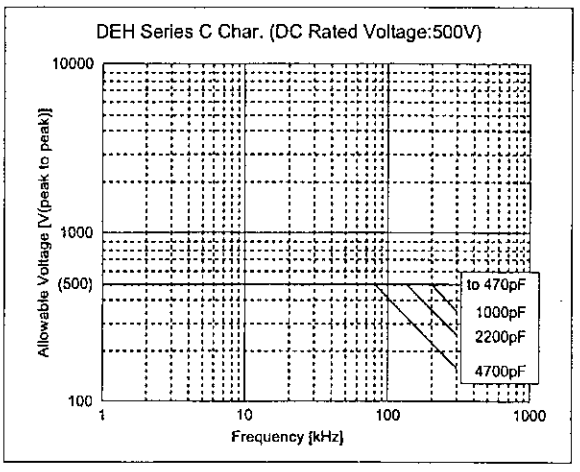
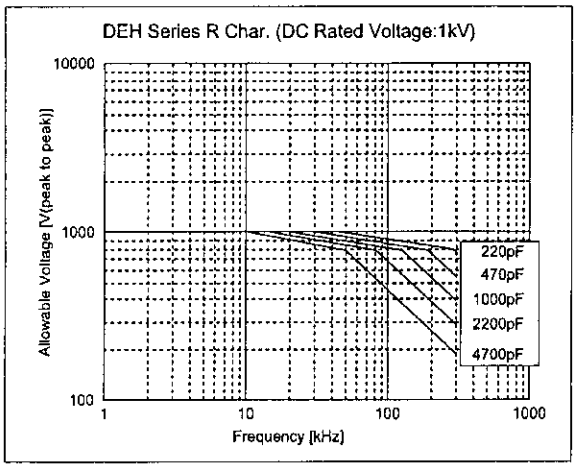
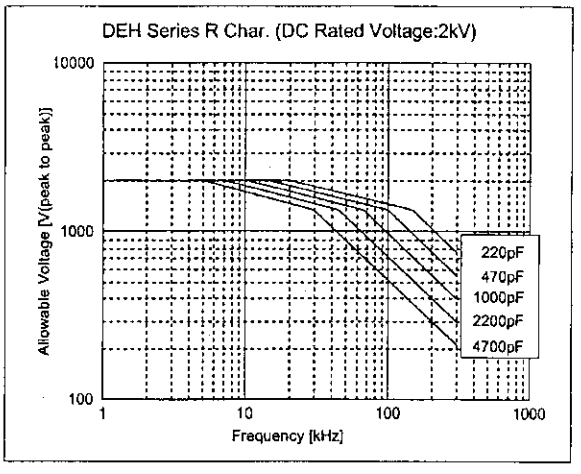
<Fig. 3> Allowable Voltage (Sine Wave Voltage) - Frequency Characteristic (At Ambient Temperature of 85°C or less)

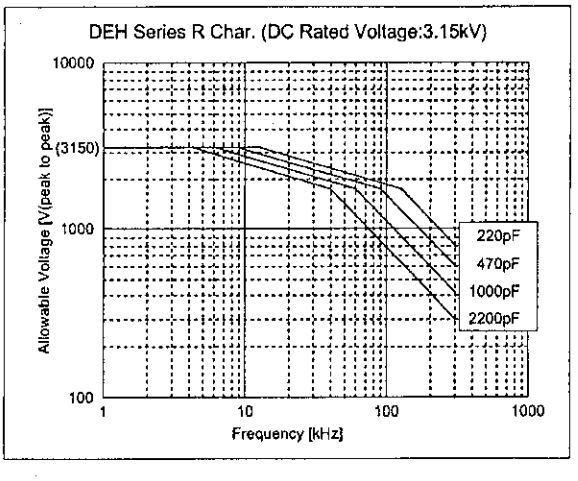
Because of the influence of harmonics, when the applied voltage is a rectangular wave or pulse wave voltage (instead of a sine wave voltage), the heat generated by the capacitor is higher than the value obtained by application of the sine wave with the same fundamental frequency.
Roughly calculated for reference, the allowable voltage for a rectangular wave or pulse wave corresponds approximately to the allowable voltage for a sine whose fundamental frequency is twice as large as that of the rectangular wave or pulse wave. This allowable voltage, however, varies depending on the voltage and current waveforms.
Therefore, you are requested to make sure that the self-heating temperature is not higher than the value specified in Table 1.











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<Fig. 3 (continue)> Allowable Voltage (Sine Wave Voltage) - Frequency Characteristic (At Ambient Temperature of 85°C or less)

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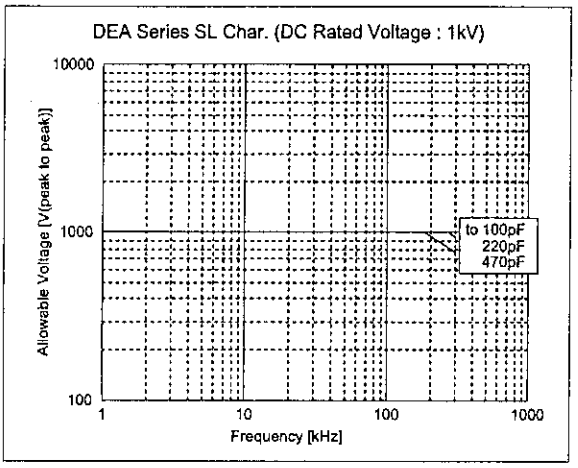
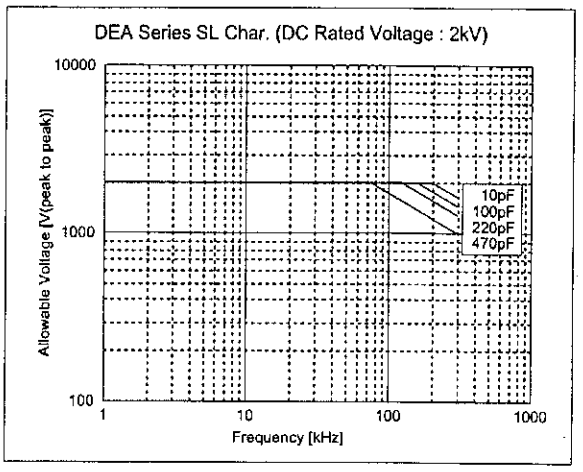
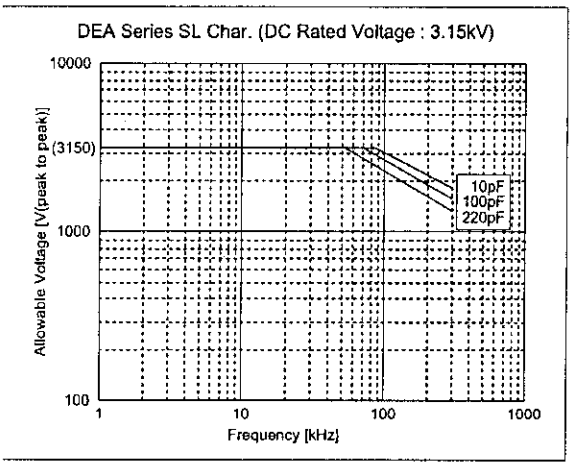
Roughly calculated for reference, the allowable voltage for a rectangular wave or pulse wave corresponds approximately to the allowable voltage for a sine wave whose fundamental frequency is twice as large as that of the rectangular wave or pulse wave.
This allowable voltage, however, varies depending on the voltage and current waveforms.
Therefore, you are requested to make sure that the self-heating temperature is not higher than the value specified in Table 1.







MEGGITT CGS

HIGH VOLTAGE RESISTORS
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ALUMNIUM CLAD RESISTORS
CURRENT SENSE RESISTORS

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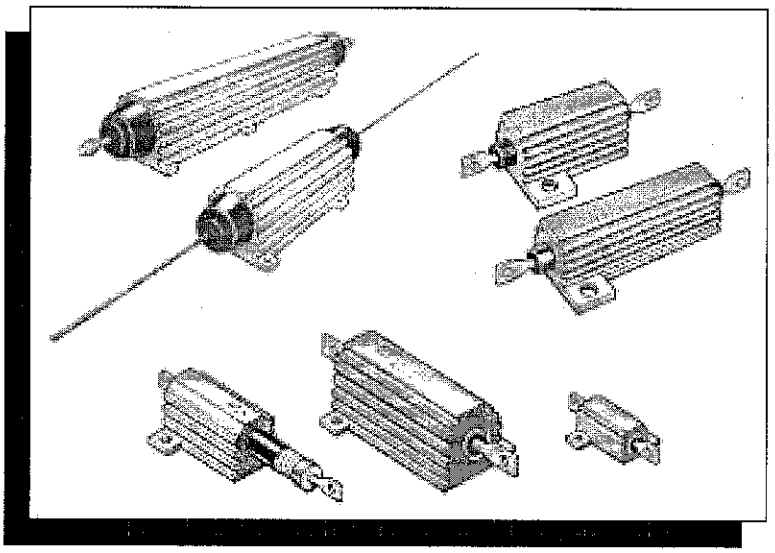

MEGGITT CGS
KEY FEATURES

- UP TO 1000 WATTS WITH HEATSINK
- LOW OHMIC VALUES AVAILABLE
- CECC - BS APPROVED
- NON INDUCTIVE + TIGHT TOLERANCE OPTIONS
- UP TO 2500 VOLTS DC
- RANGE OF CONNECTORS
- ATTRACTIVELY PRICED
- PROVEN RELIABILITY
- AVAILABLE IN DISTRIBUTION
- CUSTOM DESIGN OPPORTUNITIES WELCOMED

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FAX: (01793 611777)
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HS series is the 'flagship' product of the CGS product
e.
are the leading European supplier of standard and custom
ined Aluminum Clad Resistors for general purpose use,
er supplies, power generation and the traction industries.
latest introduction - the HSX offers increased creepage
ge by virtue of a remodelled and extended nose cone,
ng it entirely suitable for the latest VDE European Safety
irements.
HS is a range of extemely stable, high quality wirewound
ors capable of dissipating high power in a limited space
relatively low surface temperature. The power is rapidly
pated as heat through the aluminium housing to a
fied heatsink.

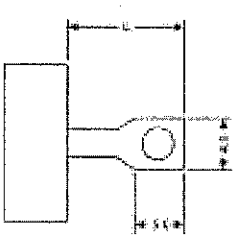
The resistors are made from quality materials for optimum reliability and stability.
Certain styles are approved to CECC specification, others are designed to conform to the relevent MIL, CGS or customer specification.
We will be happy to advice on the use of resistors for pulse applications, and to supply information for high voltage use, low ohmic value components, alternative mountings and terminations. For high power applications, a range of special designs are available, power dissipation up to 1000 Watts, insulated and designed to withstand 12KV impulse.

AND HSC TYPE 5 WATTS TO 300 WATTS

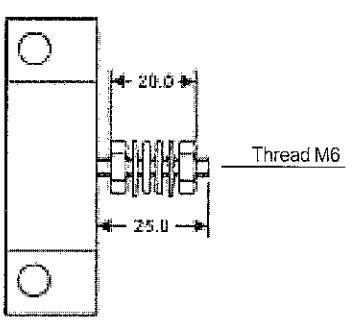
ype	HSA 5	HSA 10	HSA 25	HSA 50	HSC 75	HSC 100	HSC 150	HSC 200	HSC 250	HSC 300
C 40203 - 001	AA	BA	CA	DA						
ipation at 25°C (Watts)										
Heatsink	10	16	25	50	75	100	150	200	250	300
ıout Heatsink	5.5	8	12.5	20	45	50	55	50	60	75
ıic Value										
	R01 10K	R01 15K	R01 36K	R01 100K	R05 50K	R05 100K	R10 100K	R10 50K	R10 68K	R10 82K
. Working Voltage (DC/AC RMS)										
	160	265	550	1250	1400	1900	2500	1900	2200	2500
ectric Strength (AC Peak)										
	1400	1400	2500	2500	5000	5000	5000	5600	5600	5600
ility % Resistance										
ge, 1000 hrs.	1	1	1	1	2	2	2	3	3	3
ıce Temperature Rise Mounted on Standard Heatsink										
V	5.5	5.0	4.4	2.9	1.2	1.1	1.0	0.75	0.65	0.60
dard Heatsink										
cm^2	415	415	535	535	995	995	995	3750	4765	5780
‹ness, mm.	1	1	1	1	3	3	3	3	3	3
nting Style	← 2 Hole →				← 4 Hole →			← 6Hole →		
oximate										
ht, grams.	5	10	16	35	90	120	180	475	600	700
ɜased Dielectric Strength (AC Peak)						KHSA25			KHSA50	
						3500			3500	
ıinations										

Types HSA5 to HSC150

Type	L
HSA5, 10	7
HSA25, 50	10
HSA75, 100, 150	8



Types HSC200, 250, 300



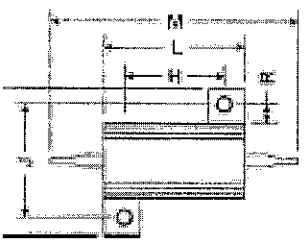
Faston connections available on request

MENSIONS (mm.)

HS Type	HSA 5	HSA 10	HSA 25	HSA 50	HSC 75	HSC 100	HSC 150	HSC 200	HSC 250	HSC 300
H ± 0.3	11.3	14.3	18.3	39.7	29.0	35.0	58.0	35.0	44.5	52.0
J ± 0.3	12.4	15.9	19.8	21.4	37.0	37.0	37.0	57.2	57.2	59.0
K ± 0.2	2.4	2.4	3.3	3.3	4.4	4.4	4.4	5.3	5.3	6.5
L Max.	17.0	21.0	29.0	51.0	49.0	65.5	98.0	90.0	109.0	128.0
M Max.	30.0	36.5	51.8	72.5	71.0	87.5	122.0	143.0	163.0	180.0
N Max.	17.0	21.0	28.0	30.0	47.5	47.5	47.5	73.0	73.0	73.0
P Max.	9.0	11.0	15.0	17.0	26.0	26.0	26.0	45.0	45.0	45.0
R Min.	1.9	1.9	2.8	2.8	5.0	5.0	5.0	5.6	5.6	6.0
T ± 0.5	3.4	5.2	7.2	7.9	11.5	11.5	11.5	22.2	22.2	22.2
U Max.	2.5	3.2	3.2	3.2	3.5	3.5	3.5	6.75	6.75	6.75

Note: K refers to mounting hole diameter

HSA5 - HSA50



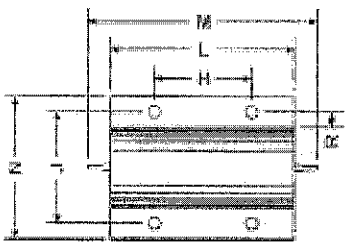
2 x Mounting Hole

HSA5 - 2.4mm
HSA10 - 2.4mm
HSA25 - 3.3mm
HSA50 - 3.3mm

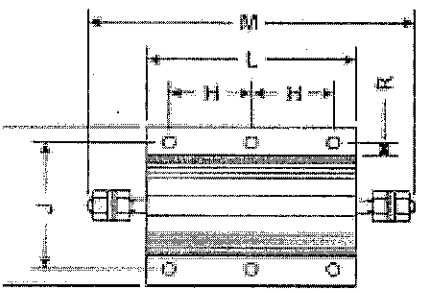
HSC75 - HSC150

4 x Mounting Hole

HSC75 - 4.4mm
HSC100 - 4.4mm
HSC150 - 4.4mm

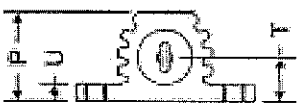


HSC200+



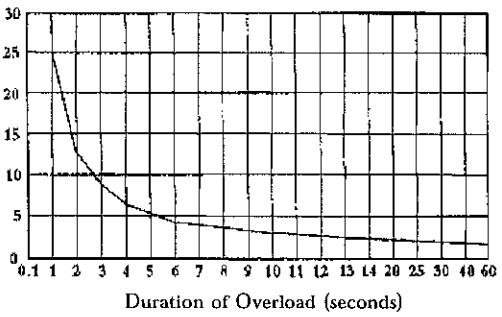
6 x Mounting Hole

HSC200 - 5.3mm
HSC250 - 5.3mm
HSC300 - 6.5mm



WER OVERLOAD

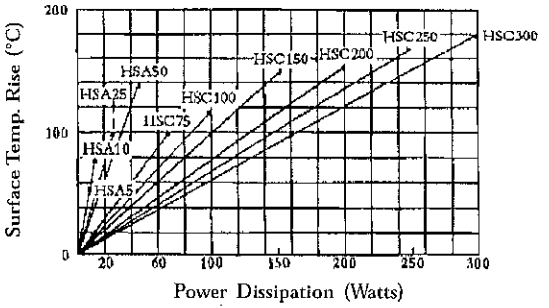
This graph indicates the amount that the rated power (at 20°C) of the standard HS series resistor may be increased for overloads of 100mS to 60S



Duration of Overload (seconds)

SURFACE TEMPERATURE RISE

For resistor mounted on standard heatsink, related to power dissipation.



Power Dissipation (Watts)

K TYPE 25 WATTS/50WATTS HIGH CREEP

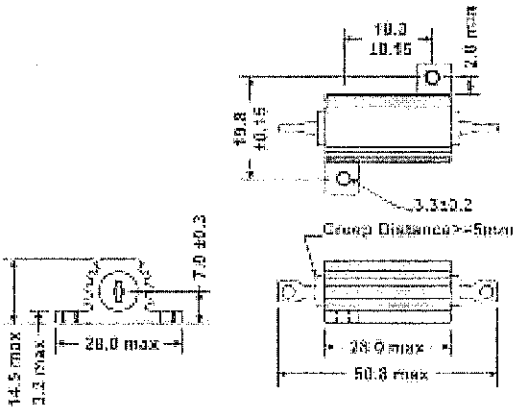
r Dissipation on Water Cooled Heatsink: (Inlet Water Temperature (= 20°C)	25 Watts	50 Watts
tance Range: (Tolerance ± 5% STD)	R05 to 36K	R05 to 86K
ity ΔR after 2000 hrs. @ 1½ hrs - ON, ½ hr - OFF	< = 2%	< = 2%
ıtion Resistance @ 500V:	> 10,000 MΩ	> 10,000 MΩ
load Resistance Change Δ R: 5 x Rated Power for 5 seconds	< = 1%	< = 1%
ing Element Voltage:	500V DC or AC rms	1250V DC or AC rms
ion Voltage:	3.5KV AC pk	3.5KV AC pk
ierature Coefficient:	< ± 50 ppm/°C	< ± 50 ppm/°C
onmental Category:	-55/200/56	-55/200/56

CHANICAL

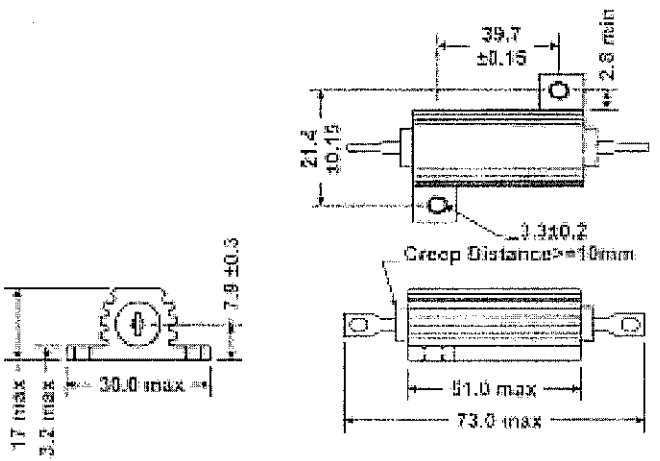
:	High Grade Steatite Ceramic
	Stainless Steel
ent:	Ni/Cr
ary Insulation:	Epoxy Moulding
cone:	Epoxy Moulding
ing:	Anodised Aluminium

MENSIONS

X 25



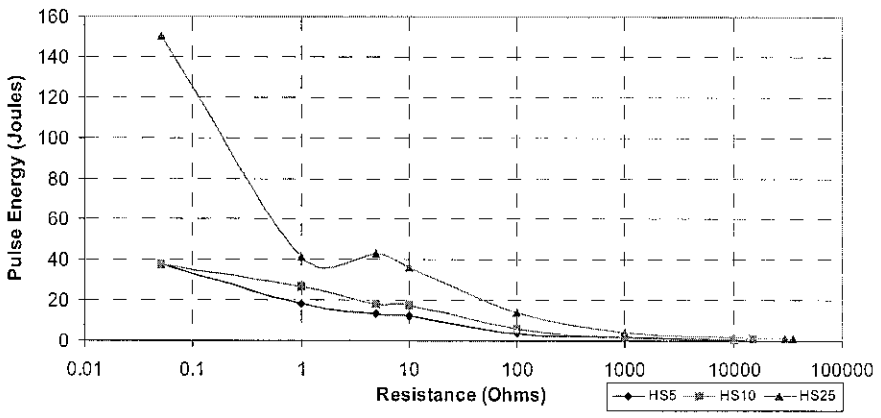
X 50



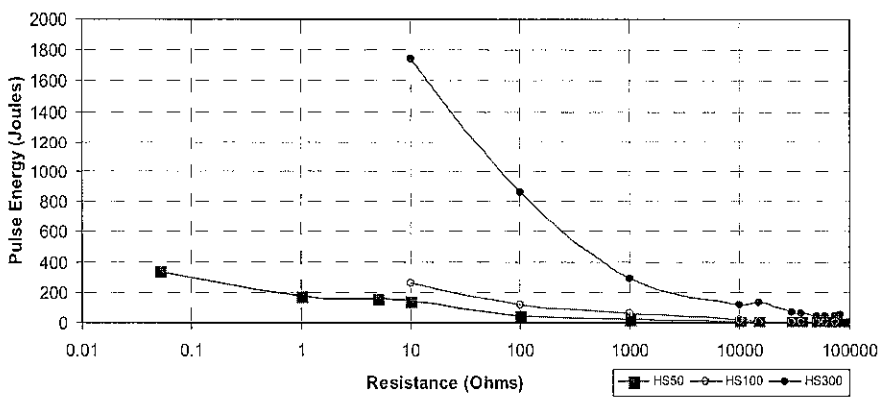
ensions are nominal
mm. unless otherwise
. Do not scale.

LSE FORM GRAPHS FOR HSA, HSC AND HSX TYPES

Pulse Energy



Pulse Energy



V TYPE 500/1000 WATTS MINERAL FILLED

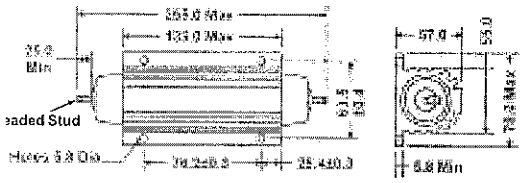
gitt CGS is probably unique in offering an elegantly packaged resistor range with power dissipations up to 1000 watts, resistance es to 50K and 12KV DC voltage proof in an elegant mineral filled aluminium case. These resistors have been specifically designed ne power generation industry but are increasingly finding applications in locomotive and other industrial markets where high er, long life and exacting pulse requirements are key design parameters. Most resistors are tailored to user specifications and we a range of mounting patterns and terminal configurations.

CTRICAL

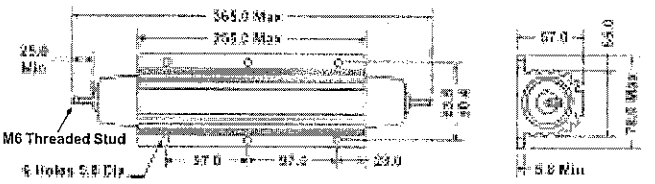
	HPV 500	HPV 1000
r Dissipation on Water Cooled Heatsink: (Inlet Water Temperature (= 20°C)	500 Watts	1000 Watts (Max. Continuous)
tance Range: (Tolerance ± 5% STD)	0R5 to 33K	1R0 to 50K
ity ΔR after 2000 hrs. @ 1½ hrs - ON, ½ hr - OFF	< = 2%	< = 2%
ition Resistance @ 500V:	> 10,000 MΩ	> 10,000 MΩ
oad Resistance Change ΔR: 5 x Rated Power for 5 seconds	< = 1%	< = 1%
ing Element Voltage:	2.5KV AC rms	2.5KV AC rms (For continuous operation)
d Voltage:	12KV peak	12KV peak
on Voltage:	4.8KV AC pk	4.8KV AC pk
ge Proof:	6.8KV AC rms or 12KV DC	6.8KV AC rms or 12KV DC
erature Coefficient:	< ± 100 ppm/°C	< ± 100 ppm/°C
onmental Category:	-55/200/56	-55/200/56

MENSIONS

HPV500



HPV1000

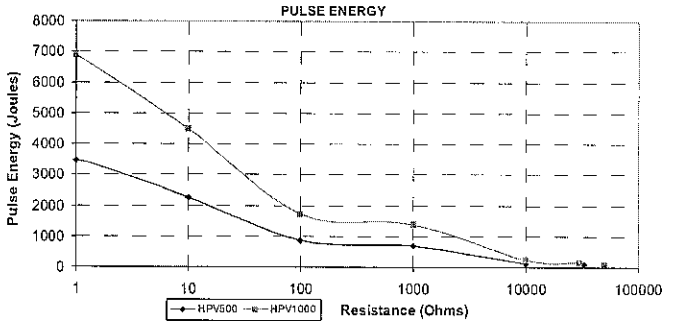


ensions are nominal
mm. unless otherwise
Do not scale.

CHANICAL

	High Grade Alumina
	Stainless Steel
(Threaded Terminals Only)	Stainless Steel
nt:	Ni/Cr
ry Insulation:	High Grade Alumina
one:	Silicone Moulding
ng:	Aluminium Extrusion (Anodised)

SE FORM GRAPH



CIAL DESIGN VARIANTS

hmic values from R01 dependent on size

ldition of tinned copper wire attached by high melt solder, wire supplied with or without insulation at length to suit customer.

ngth of tag increased by 3mm. to provide additional hole 1.0mm. for voltage connector.

S25 and HS50 manufactured with extended nosecones to improve creep distance.

nbedded wire terminals

ARACTERISTICS

imium Overload
overloads of the order of 2 x power rating for 3 mins., 5 x power g for 5 secs., or 25 x power rating for 1 second, change of resistance s than 0.5% + 0.05 ohm maximum voltage must not exceed mum working voltage.

g Term Stability
mprovements in long term stability, resistors must be derated as ws: for 50% of stated ΔR maximum dissipation must not exceed of rating; for 25% of stated ΔR maximum, dissipation must not ed 50% of the rating.

Dissipation
ough the use of proprietary heatsinks with lower thermal resistance eptable, uprating is not recommended. The use of proprietory ink compound to improve thermal conductivity is recommended otimum performance of all sizes but essential for HSC200, HSC250, 300.

lation Resistance
10,000 Megohm minimum. After moisture test: 1000 Megohm num.

Ambient Power Dissipation
pation derates linearly to zero at 250°C from 25°C

ification
erature coefficient below 100R, 50ppm/°C.
erature coefficient above 100R, 30ppm/°C.
ance, 5% standard; 10%, 3%, 2%, 1%, 0.5% & 0.25% available.
ance for values below R10, 10% standard.

MATERIALS

Core
Ceramic, steatite or alumina depending on size.

Element
Copper nickel alloy or nickel chrome alloy.

Endcaps
Nickel iron or stainless steel.

Encapsulant
High temperature material moulding

Housing
Anodised aluminium

Stock
The HSA5, 10, 25 and 50 are stocked in selected values of the E24 series at 5% tolerance.

W TO ORDER

HS	A	50	680R			J	X
MMON PART	**MOUNTING STYLE**	**WATTAGE RATING AT 25°C WITH HEATSINK**	**RESISTANCE VALUE**			**TOLERANCE**	**RELEASE CONDITION**
S - Standard S - Increased ctric Strength HS - Low ctive Winding	A - Single Opposing Mounting Feet B - Flange One Side C - Flange Two Sides X - High Creep (25 & 50 Watt only)	10 Watt = HSA5 16 Watt = HSA10 25 Watt = HSA25 50 Watt = HSA50 75 Watt = HSA75 etc....	0.1 ohm 1 ohm 1K ohm	(100 mille ohms) (1000 mille ohms) (1000 ohms)	R10 1R0 1K0	F - 1% G - 2% E - 3% J - 5% K - 10%	X - BS CECC No Letter - Commercial

W TO ORDER HPV TYPES

any applications require major or minor customisation Meggitt will normally allocate a R number special sequence to your requirement. is logged with drawings and maintained indefinitely to facilitate your re-order or spares requirements.
e various specials may be low inductance types, various wire terminal types, special pulse application designs or various stud terminal types.

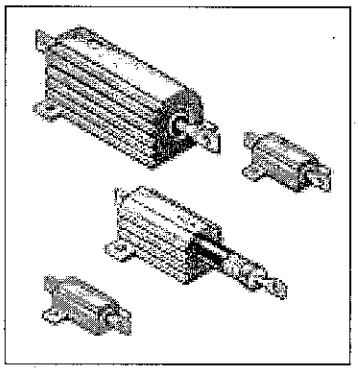
Meggitt Electronic Components Ltd. Ohmic House, Westmead Industrial Estate, Swindon, Wilts. SN5 7US
Telephone:(01793)487301(Admin.) (01793)611666 (Sales) EMail:sales@megelec.co.uk Fax:(01793) 611777

ıh Power Resistors

aluminium housed for heatsinking

Key features

- **up to 300 watts with heatsink**
- **low ohmic values available**
- **CECC - BS approved**
- **non-inductive & tight tolerance available**
- **up to 2500 volts dc**
- **range of connectors**
- **custom designs welcomed**



Specification

Electrical

	HSA 5	HSA 10	HSA 25	HSA 50	HSC 75	HSC 100	HSC 150	HSC 200	HSC 250	HSC 300
CECC 40203-001	AA	BA	CA	DA						
Dissipation at 25°C (Watts)										
With Heatsink	10	16	25	50	75	100	150	200	250	300
Without Heatsink	5.5	8	12.5	20	45	50	55	50	60	75
Ohmc Value										
Min Value	R051	R051	R051	R051	R010	R010	R010	R010	R010	R010
Max Value	10K	15K	36K	86K	50K	75K	100K	50K	68K	82K
Max Working Voltage										
V (DC/AC RMS)	160	265	550	1250	1400	1900	2500	1900	2200	2500
Dielectric Strength										
V (AC Peak)	1400	1400	2500	2500	5000	5000	5000	5600	5600	5600
Stability										
% Resistance Change/1000Hrs	1	1	1	1	2	2	2	3	3	3
Surface Temperature Rise Mounted on Standard Heatsink										
°C per Watt	5.5	5.0	4.4	2.9	1.2	1.1	1.0	0.75	0.65	0.60
Standard Heatsink										
Area cm^2	415	415	535	535	995	995	995	3750	4765	5780
Thickness mm	1	1	1	1	3	3	3	3	3	3
Mounting Style	<---------- 2 HOLE ---------->				<------ 4 HOLE ------>			<----- 6 HOLE ---->		
Approximate Weight										
Grams	5	10	16	35	90	120	180	475	600	700
Increased Dielectric Strength Option					KHSA25			KHSA50		
V (AC Peak)					3500			3500		

ower Resistors

HS series

series is the 'flagship'
: of the Meggitt
ıics power product
A major business, in this
duct, Meggitt are the
European supplier of
d and custom designed
ium Clad Resistors, for
purpose use, power
s, generation and the
industries. A particular
: strength in this area, is
ised HS resistors where
antities are not required.

ales action desk **(01793) 611666**
sales fax line **(01793) 611777**

aluminium housed for heatsinking

Terminations

	Lmm
10	7
50	10
100, 150	8

Style	Lmm
HSC 200, 250, 300	25

Dimensions

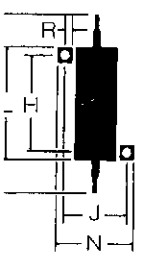
	HSA 5	HSA 10	HSA 25	HSA 50	HSC 75	HSC 100	HSC 150	HSC 200	HSC 250	HSC 300
	11.3	14.3	18.3	39.7	29.0	35.0	58.0	35.0	45.5	52.0
	12.4	15.9	19.8	21.4	37.0	37.0	37.0	57.2	57.2	59.0
	2.4	2.4	3.3	3.3	4.4	4.4	4.4	5.3	5.3	6.5
	17.0	21.0	29.0	51.0	49.0	65.5	98.0	90.0	109.0	128.0
	30.0	36.5	51.8	72.5	71.0	87.5	122.0	143.0	163.0	180.0
	17.0	21.0	28.0	30.0	47.5	47.5	47.5	73.0	73.0	73.0
	9.0	11.0	15.0	17.0	26.0	26.0	26.0	45.0	45.0	45.0
	1.9	1.9	2.8	2.8	5.0	5.0	5.0	5.6	5.6	6.0
	3.4	5.2	7.2	7.9	11.5	11.5	11.5	22.2	22.2	22.2
	2.5	3.2	3.2	3.2	3.5	3.5	3.5	6.75	6.75	6.75

Power Resistors

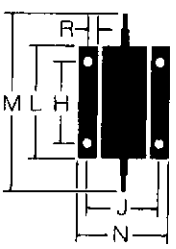
type HS series

Certain styles are approved to CECC specification, others are designed to conform to MIL, or customer specifications. We will be happy to advise on the use of resistors for pulse applications, and to supply further information for high voltage use, low inductive and low ohmic value components, alternative mountings and terminations. A full range of HS resistors, is available from Meggitt distributors.

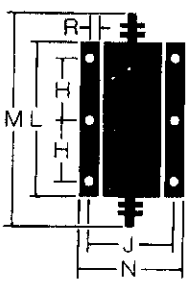
A5 to HSA50



HSC75 to HSC150



HSC200 to HSC300



How To Order

HS	A	25
Common Part	**Mounting Style**	**Size**
HS - Standard KHS - High Voltage * NHS - Low Inductance Winding	A - Single Opposing Mounting Feet B - Flange One Side C - Flange Two Sides	HSA5 - 10 Watts HSA10 - 16 Watts HSA25 - 25 Watts etc .....

1R0	J	X
Resistance Value	**Tolerance**	**Release Condition**
0.1 ohm (100 milli ohms) R10 1.0 ohm (1000 milli ohms) 1R0 1K ohm (1000 ohms) 1K0	F * 1% E - 3% J - 5% K - 10%	X - BS CECC - - No Letter Commercial

* - KHS Applies to 25 Watt and 50 Watts Styles Only

Please Request Full Data Sheet L1000

MEGGITT ELECTRONIC COMPONENTS