THE INVESTIGATION OF SWITCHING LOSSES IN A HIGH POWER FACTOR BUCK CONVERTER USING THE STATE OF THE-ART COOLMOS DEVICES

CHE SAROJA KATANI BINTI HUSIN

ELECTRICAL AND ELECTRONICS ENGINEERING
UNIVERSITI TEKNOLOGI PETRONAS
DECEMBER 2004

CERTIFICATION OF APPROVAL

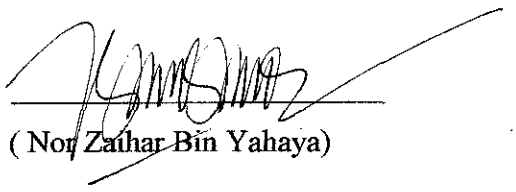
The Investigation of Switching Losses in a High Power Factor Buck Converter Using The State ofThe-Art CoolMos Device

by

Che Saroja Katani Binti Husin

A project dissertation submitted to the
Electrical & Electronics Engineering Programme
Universiti Teknologi PETRONAS
In partial fulfillment of the requirement for the
BACHELOR OF ENGINEERING (Hons)
(ELECTRICAL AND ELECTRONICS ENGINEERING)

Approved by,



(Nor Zaihar Bin Yahaya)

UNIVERSITI TEKNOLOGI PETRONAS
TRONOH, PERAK
December 2004

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

Che Saroja Katani Binti Husin

ABSTRACT

Switching losses is one of the phenomena that occur in power electronic fields, which cause the imperfection of the output waveform. There are lots of ways defined it encounter this problem such as snubber usage, tapped-inductor, MOSFETS and etc. In this century, semiconductor field came out with the revolution of the MOSFET, which is called CoolMOS in order to reduce the switching losses and give high efficiency. The CoolMOS become famous as it can reduce 80% reduction of switching losses and low cost. CoolMOS technology - developed for the production of charge-compensated devices - is presented. Due to its novel internal structure, the device offers a dramatic reduction in on-state resistance with a completely altered voltage dependence of the device capacitance. If the power factor is small which is below than 0.85, it causes large amount of power loss (Losses = I^2R) and power that should apply not achieved as target. In worst cases it causes equipment damaged and power supply trip. This will affect whole process especially for manufacturing company. Basically, this project needs to evaluate the performance of CoolMOS in improving the switching losses especially in Buck Converter. The main focus is on the parameters that contributing in developing high power factor. Its mean that selection of components used is very important such as inductor value. As conclusion, Buck converter is one of the best methods to investigate power factor correction. Moreover, CoolMOS device is a good device which should be varies its application in the future.

ACKNOWLEDGEMENT

The authors would like to thank numerous individuals for their tremendous support in performing this project. Deepest gratitude goes to the authors' supervisors; Mr. Nor Zaihar Bin Yahaya for their tremendous support through out the process. Millions of thanks to the technicians and friends, who have been very co-operative and understanding. The authors also would like to thank the lecturers of Electrical Engineering Program of UTP, who have been very helpful and resourceful while guiding us. Last but not least, I would like to thank all of our friends who have helped me in their own way.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLE

CHAPTER 1
INTRODUCTION

1.1 BACKGROUND OF PROJECT

A switching technique that improves performance of the high-power-factor buck converter by reducing switching losses is introduced. The losses are reduced by an enhancement of MOSFET devices, which is CoolMOS. A buck converter circuit consists only an inductor, a capacitor, a resistor, a power diode and a switch (CoolMOS) has inherent power factor correction properties and continuous input current (***Figure 1***). Moreover, this type of converter is a very attractive solution to implement power factor correction in many applications. By using buck converter, it causes low cost and simple circuit. This converter provides an output voltage (or bus voltage) lower than the peak line voltage, been very suitable for medium and low output voltage application.

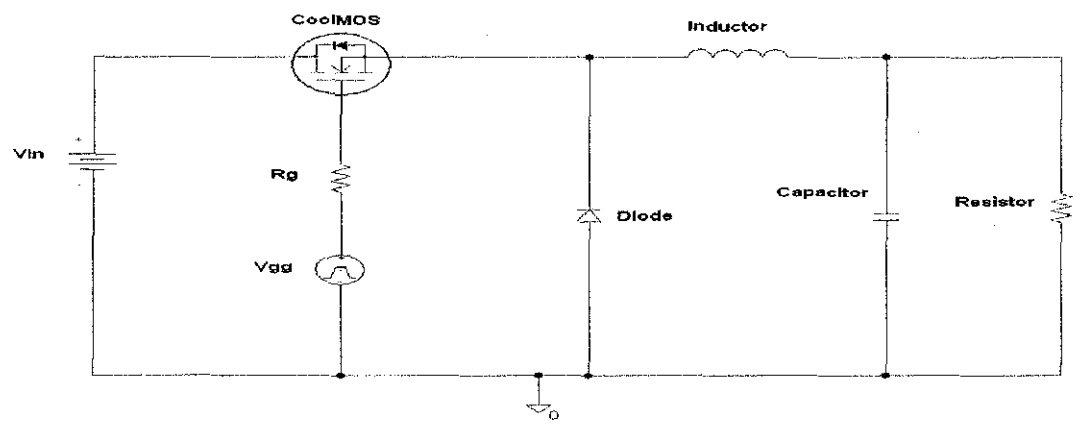


Figure 1: Basic circuit of Buck converter circuit

CoolMOS is a new revolutionary technology for high voltage power MOSFET. It has a few similarities with MOSFET but more advances in which MOSFET does not have capability to do it. The revolutionary CoolMOS power MOSFET family enables a significant reduction of conducting (up to 80%) and switching losses (up to 50%) in power electronic systems [1].

1.2 PROBLEM STATEMENT

Switching losses is one of the phenomena that occur in power electronic fields, which cause the imperfection of the output waveform. It is influence by many factors. One of them is power factor contribution to the circuit. Moreover, power factor problem also cause big issue especially to the power plant generator such as Tenaga Nasional Berhad (TNB). As a result, TNB took an action that the power factor must not less than 0.85. Penalty will be fined to those disobey that rule. For TNB itself, they took an action by adding up capacitor bank in order to recover that such of problem.

If the power factor is small which is below than 0.85, it causes large amount of power loss (Losses = I^2R) and power that should apply not achieved as target. In worst cases it causes equipment damaged and power supply trip. This will affect whole process especially for manufacturing company.

In order to avoid such as incident we have to make sure that power factor is always bigger than 0.85 which is optimized with the circuit constructed. The best parameter for power factor is almost to unity power factor which is equal to 1.To succeed in overcome this problem, we must be alert with capacitor and inductor value. Both are very important in contributing to achieve high power factor. Lastly, Buck converter circuit is the easiest circuit in order to perform this investigation.

1.3 PROJECT OBJECTIVE

Basically, this project needs to evaluate the performance of CoolMOS in improving the switching losses especially in Buck Converter. This includes research on power factor contribution in Buck Converter circuit. The main focus is on the parameters that contributing in developing high power factor. Its mean that selection of components used is very important such as inductor value. By conducting this investigation and research, it is hoped that these findings encourage further development of CoolMOS in encounter the switching losses in the Buck Converter circuit and at the same time able to upgrade the switching performance.

1.3.1 Objectives

The main objectives of this project are:

(a) To investigate the switching losses in Buck Converter.

(b) To monitor the influence of power factor correction to the Buck Converter circuit.

(c) To study on the characteristics of CoolMOS and MOSFET family.

(d) To be able to construct design circuit using CoolMOS in Buck Converter circuit

(e) To be able to do simulation on PCB.

(f) Produced a prototype of the circuits.

(g) Run a few experiments and able to prove the simulation is correct.

1.3.2 Scope of Study

In this study, the basic knowledge of power factor will be studied and practically using the a few software such as Pspice software to be able simulating the circuit. Besides, this investigation also will be focused on the effects of power factor in switching losses and also influence of the CoolMOS device in the circuit. In this research, power factor play important role and the characteristic of

CoolMOS need to study more deeply in order to make sure that all the components are attached together.

Besides, a prototype of the circuit needs to be constructed. New software like Multisim and Ultiboard used to evaluate the performances of switching losses by undergo some experiment using PCB.

1.3.3 Gantt Chart

Gantt chart is attached in **Appendix 1** and **Appendix 2** for the time frame.

CHAPTER 2

LITERATURE REVIEW AND THEORY

2.1 Buck Converter

Buck converter is a very attractive solution to implement power factor correction in many applications. By using buck converter, the standard can be met with a very simple and low cost circuit (***Figure 2***). This converter provides an output voltage (or bus voltage) lower than the peak line voltage, been very suitable for medium and low output voltage applications.

Thus, it has been proposed in hard requirements low output voltage power supplies based on two-stage conversion structures. Also, it has been proposed in the design of electronic ballast with power factor correction. The wide interest on the application of this converter has led to the development of an average small-signal model to become more easy and effective the design of the output voltage control loop [1].

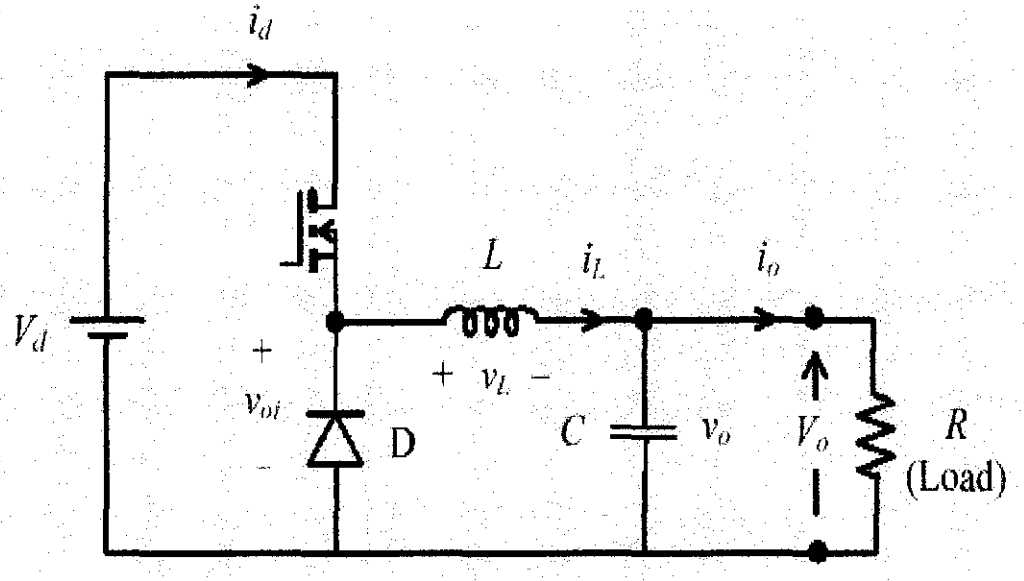


Figure 2: Buck converter circuit [2]

2.1.1 During Turn - on

Inductor voltage

$vL = Vg - v(t)$

Small ripple approximation:

$vL \approx Vg - V$

Knowing the inductor voltage, we can now find the inductor current via

$$vL(t) = L\left(\frac{diL(t)}{dt}\right)$$

Solve for the slope:

$\frac{diL(t)}{dt} = \left(\frac{vL(t)}{L}\right) \approx Vg - \frac{V}{L}$ The inductor current changes with an essentially constant slope

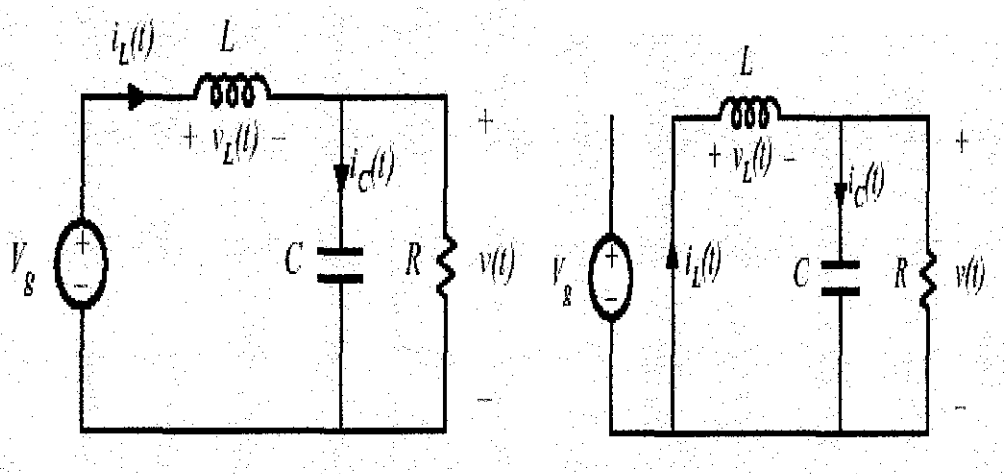


Figure 3: Switching characteristic of Buck Converter a) during Turn-on b) during Turn-off [3]

2.1.2 During Turn – off

Inductor voltage

$vL(t) = -v(t)$

Small ripple approximation:

$vL(t) \approx -V$

Knowing the inductor voltage, we can again find the inductor current via

$$vL(t) = L\left(\frac{diL(t)}{dt}\right)$$

Solve for the slope: $\frac{diL(t)}{dt} = \left(\frac{vL(t)}{L}\right) \approx -\frac{V}{L}$

The inductor current changes with an essentially constant slope.

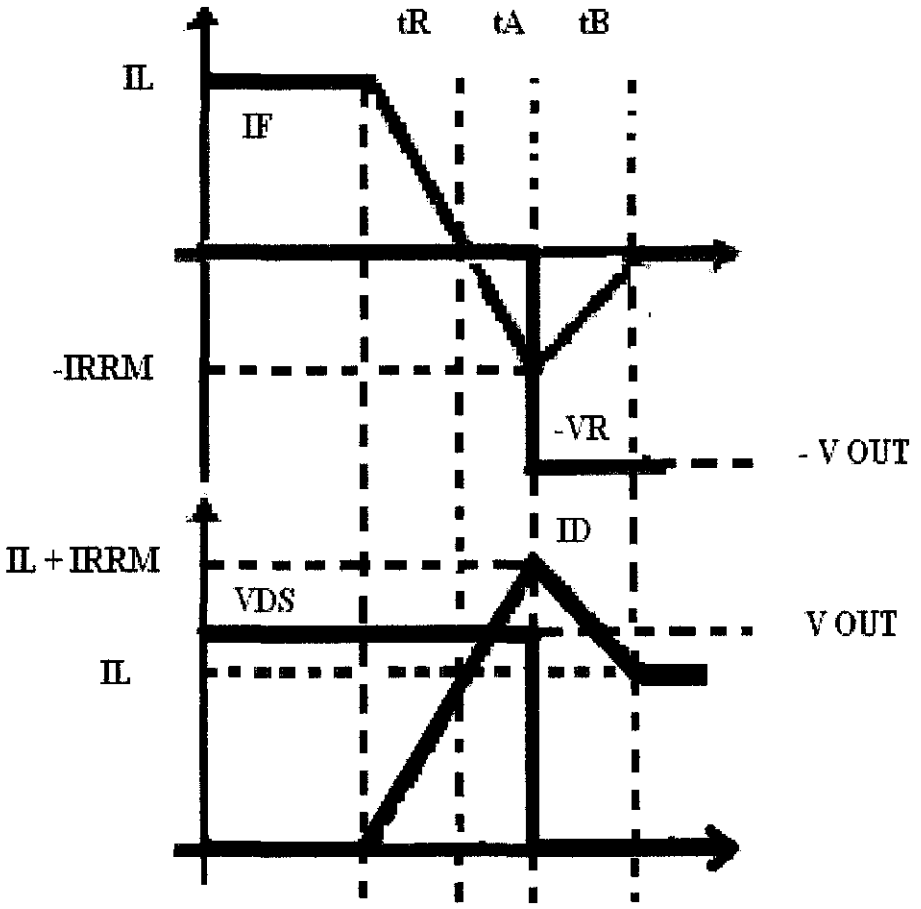


Figure 4: Idealized current and voltage waveforms; current commutates from diode to switch [4].

2.2 Power factor

The term power factor is borrowed from elementary AC circuit theory.

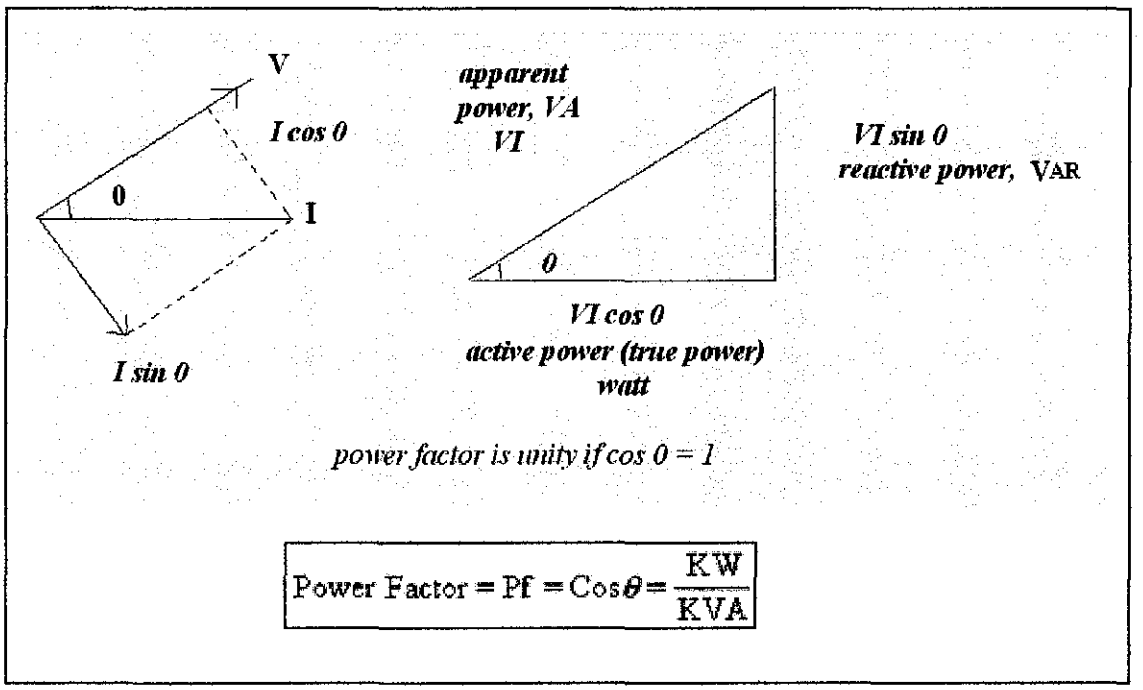


Figure 5: Calculation of Power Factor

Power factor is a quantity which has important implications when sizing a power supply system. Power is a measure of the delivery rate of energy and in DC (direct current) electrical circuits is expressed as the mathematical product of Volts and Amps (Power = Volts x Amps).

However, in AC (alternating current) power system, a complication is introduced; namely that some AC current (Amps) may flow into and back out of the load without delivering energy. This current, called reactive or harmonic current, gives rise to an "apparent" power (Volts x Amps) which is larger than the actual power consumed.

This difference between the apparent power and the actual gives rise to the power factor. The power factor is equal to the ratio of the actual power to the apparent power. Always a value between (0.0) and (1.0), the higher the number the greater / better the power factor. The bigger the power factor is the perfect the system is [5].

$$POWER\ FACTOR = \frac{Real\ Power}{Apparent\ Power}$$

2.2.1 Effects of Power Factor

1. **System Capacity** - Your kVA is the total power available. Your useful power kW = (kVA)(pf). The higher the system power factor, the more system capacity that is available. With more system capacity, voltage will remain more stable as loads are cycled on and off. Also more loads can be added to the system as needed.
2. **System Losses** - With a higher Power Factor, less current flows through your system. There is less power lost (I2R losses) to heating of cables, bus bars, transformers, panels, etc. These devices will run cooler and last longer too.
3. **Utility Charges** - Electric utilities must maintain a high Power Factor on their distribution system for efficiency. They will typically bill customers for a low Power Factor or they may bill on kVA demand, which Power Factor will affect. Most utilities that bill a Power Factor penalty require a user to maintain a 95% Power Factor to avoid penalty.

2.2.2 Advantages of Power Factor Correction:-

The main advantages of the Power Factor Correction are:

1. The electrical load on the Utility is reduced, thereby allowing the Utility to supply the surplus power to other consumers, without increasing its generation capacity.

2. Most of the Utilities impose low power factor penalties. By correcting the power factor, this penalty can be avoided.

3. High power factor reduces the load currents. Therefore, a considerable saving is made in the hardware cost, such as cables, switchgear, substation transformers, etc.

2.3 CoolMOS

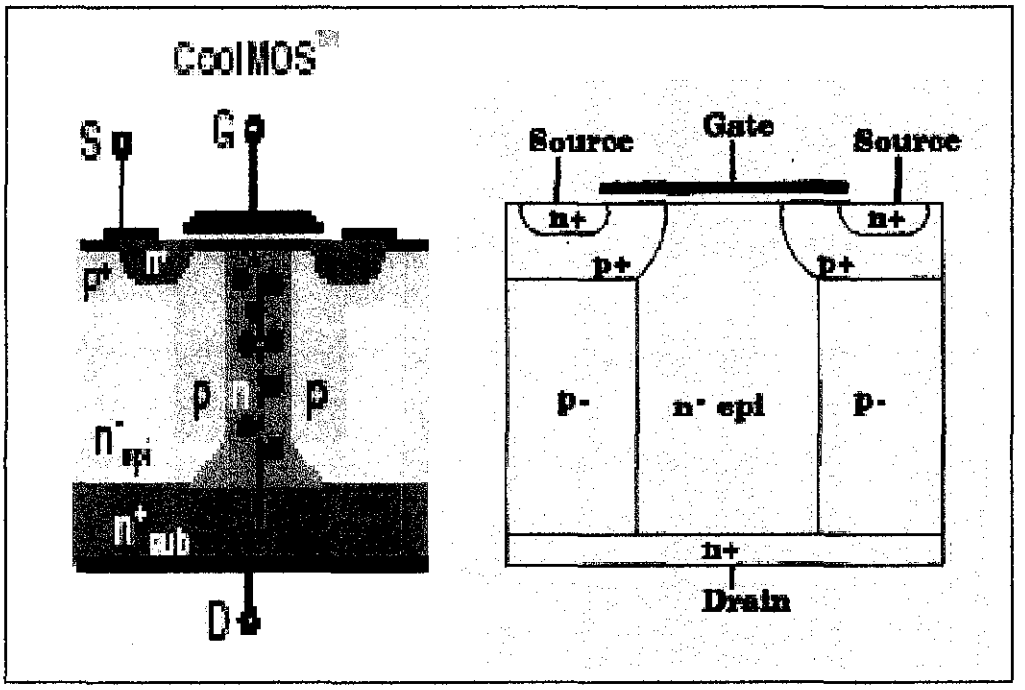


Figure 6: Cell structure of CoolMOS [6]

Characteristic of CoolMOS

- Blocking voltage Vds of 600V and 800V
- Lowest on -resistance reduced by a factor of up to 7 compared with standard devices
- Extremely fast controllable switching speed
- Ultra-low gate charge
- Avalanche-rated
- Compatible gate control

Benefits of CoolMOS

- Favorable for a wide range of application areas
- Highest conversion efficiency
- Lowest switching losses with adjustable EMI behavior
- Full rectangular SOA offers maximum system reliability
- Best with low driving ICs as well as for high–end solutions

COOLMOS™ DEVICE CONCEPT AND ON STATE RESISTOR

The CoolMOS™ concept (comparing to a conventional high voltage power MOSFET is shown in ***Figure 6***) offers here a new approach to overcome the challenge of the drift zone resistance. The electrical conductivity is provided by majority carriers only. There is no bipolar current contribution; the switching losses are hence equal to that of conventional MOSFETs. The conduction losses as shown in ***Figure 7*** have however been cut down by a factor of 5 versus this conventional technology. The doping of the voltage sustaining layer is rise by roughly one order of magnitude; additional vertical p-stripes are inserted into the structure, which compensate the surplus current conducting n-charge. When the transistor is reverse biased, a lateral electric field is built up, which drives the charge towards the contact regions. The space charge layer builds up along the physical pnjunction line and spreads at a voltage around 50V across the whole p-/n-striped structure. The drift zone is now completely depleted and acts like the voltage sustaining layer of a pin-structure. If the voltage is further increased, the electrical field rises linearly without any further expansion of the space charge layer. No current flows through the space charge layer.

Both carrier types are driven by very low electric fields within their columns towards the contacts. This behavior is characteristic for charge compensated devices and leads to extremely low losses. The breakdown voltage of the CoolMOS™ technology shows a significant dependence of the net charge balance. The net charge balance is the integral of the doping over the whole voltage sustaining layer normalized to the doping of the n-column.

A negative value indicates a surplus of pdoping. The maximum breakdown voltage is achieved, if the charge of the two opposite doped regions cancels each other out perfectly. A remaining net charge contributes to the vertical electric field, transforming the pin-structure in either pn-n or pp-n, respectively. The blocking voltage

therefore decreases. The width of this distribution at the specified blocking voltage limits the production window and is one of the CoolMOS™ main technological challenges.

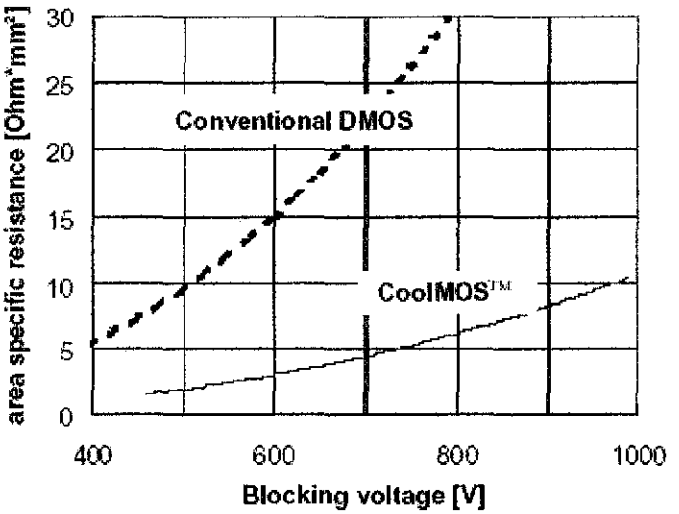


Figure 7: Comparison of the voltage dependency of the area specific R_{DSon}: CoolMOS vs. conventional power MOSFET

SWITCHING BEHAVIOUR

The equivalent circuitry of the Power diode like Schottky diode is an ideal diode with no switching losses and a capacitor in parallel. When switching the diode off only the voltage depended charging of the capacitor can be observed instead of a typical reverse recovery wave form. As expected there is also no dependence of this capacitive recovery charge (QC) from temperature, forward current or di/dt.

CoolMOS implements a compensation structure in the vertical drift region of a MOSFET in order to reduce the state resistance. Such a structure makes it possible to reduce the on-state resistance R_{dson} of a 600V MOSFET to one fifth of that of the conventional MOSFET for the same circuit. It also claimed that the CoolMOS achieves the fastest switching speed for the given circuit [7].

Characteristic of CoolMOS – SPB07N60C3:-

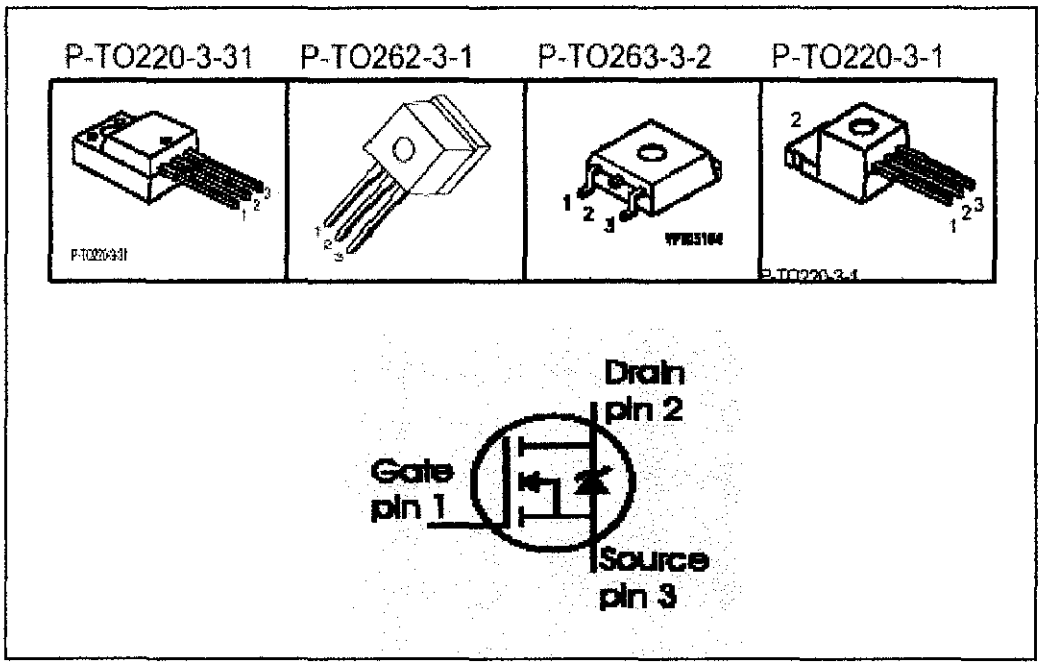


Figure 8: Layout of the CoolMOS – SPB07N60C3 [8]

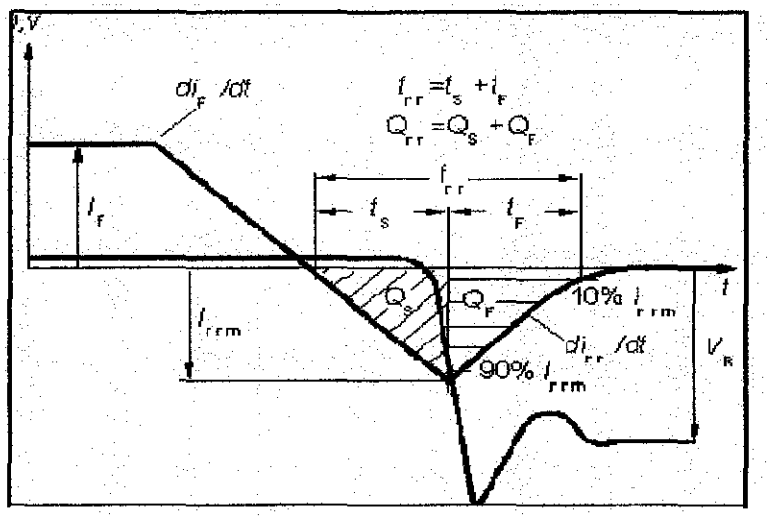


Figure 9: Expected diodes switching characteristics [9]

For more details of the specification of CoolMOS, SPB07N60C3 and also power diode, IDP06E60 can be referring to ***Appendix 4*** and ***Appendix 5***.

CHAPTER 3

METHODOLOGY

3.0 METHODOLOGY/PROJECT WORK

3.1 Procedure Identification

For the time being, the existence methodology is used and after analyze the data obtained, the methodology will be improved.

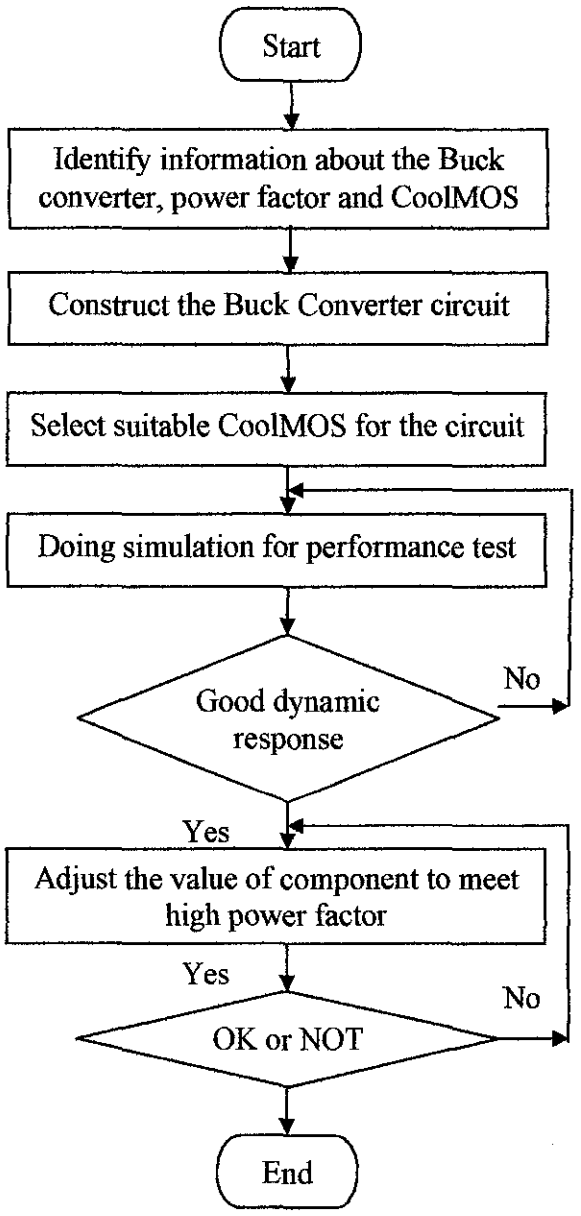


Figure 10: Flow diagram for semester 1

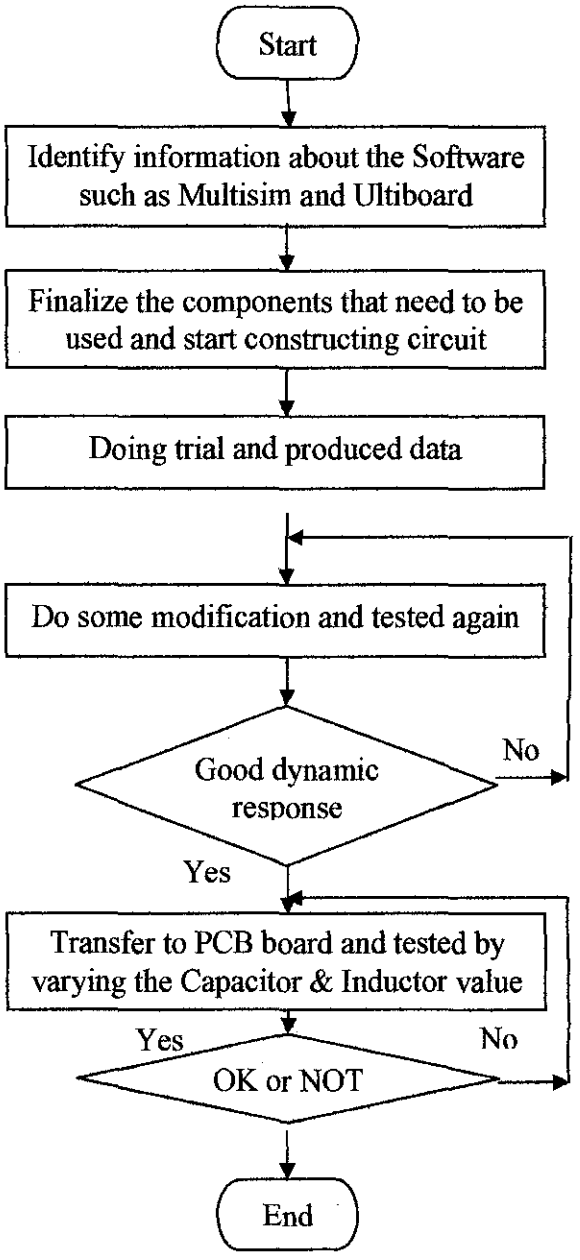


Figure 11: Flow diagram for semester 2

This project is divided into two phases which is one phases concentrate on the simulation of the circuit using Pspice and another phase focus on hardware implementation. During simulation phase, the circuit is running using the Pspice software to evaluate the performance of CoolMOS device and also the influence of power factor to the switching losses using Buck Converter circuit. In order to make the

simulation work out, there are lots of interface need to be done such as export the CoolMOS library and power diode library, setting on the parameters and time delay to use, the type of output that we need to achieve and etc.

3.1.1 Installation

The downloaded CoolMOS modeling package consists of the following files relevant to the PSpice simulator:

- ***.lib files comprising the PSpice code
- ***.slb files providing symbols for the models required by the graphic user interface (GUI) 'Schematics'. (In order to be usable in evaluation versions of the PSpice/Schematics system, each symbol library does not contain more than twenty symbols.)
- ***.olb files comprising symbols for the graphical user interface 'Capture'

If 'Schematics' is used as GUI, the ***.lib files must be installed via the 'Analysis → Library and Include Files' menu. Permanent installation via 'Add Library*' is recommended. The ***.slb files need to be installed via the menu 'Options → Editor Configuration →Library Settings'.

The installation in 'Capture' is similar. The ***.lib files must be included via the 'PSpice → Edit (New) Simulation Profile → Libraries'menu. Using the 'Add as Global' button will provide the CoolMOS models permanently. The symbol libraries (***.olb files) need to be included via 'Place → Part → Add Library' [10].

3.1.2 Typical Simulation Parameters

As PSpice was originally not designed for power electronics and highly non-linear Components, the standard simulation parameters (Simulation Setup/Options) are often not suitable. In common, the following typical values facilitate convergence:

ABSTOL= 1nA (maximum current accuracy)

CHGTOL= 1pC (maximum charge accuracy)

ITL1= 150 (maximum number of iterations for DC analyses without initial conditions)

ITL2= 150 (maximum number of iterations for DC analyses with initial conditions)

ITL4= 500 (maximum number of iterations for transient analyses time steps)

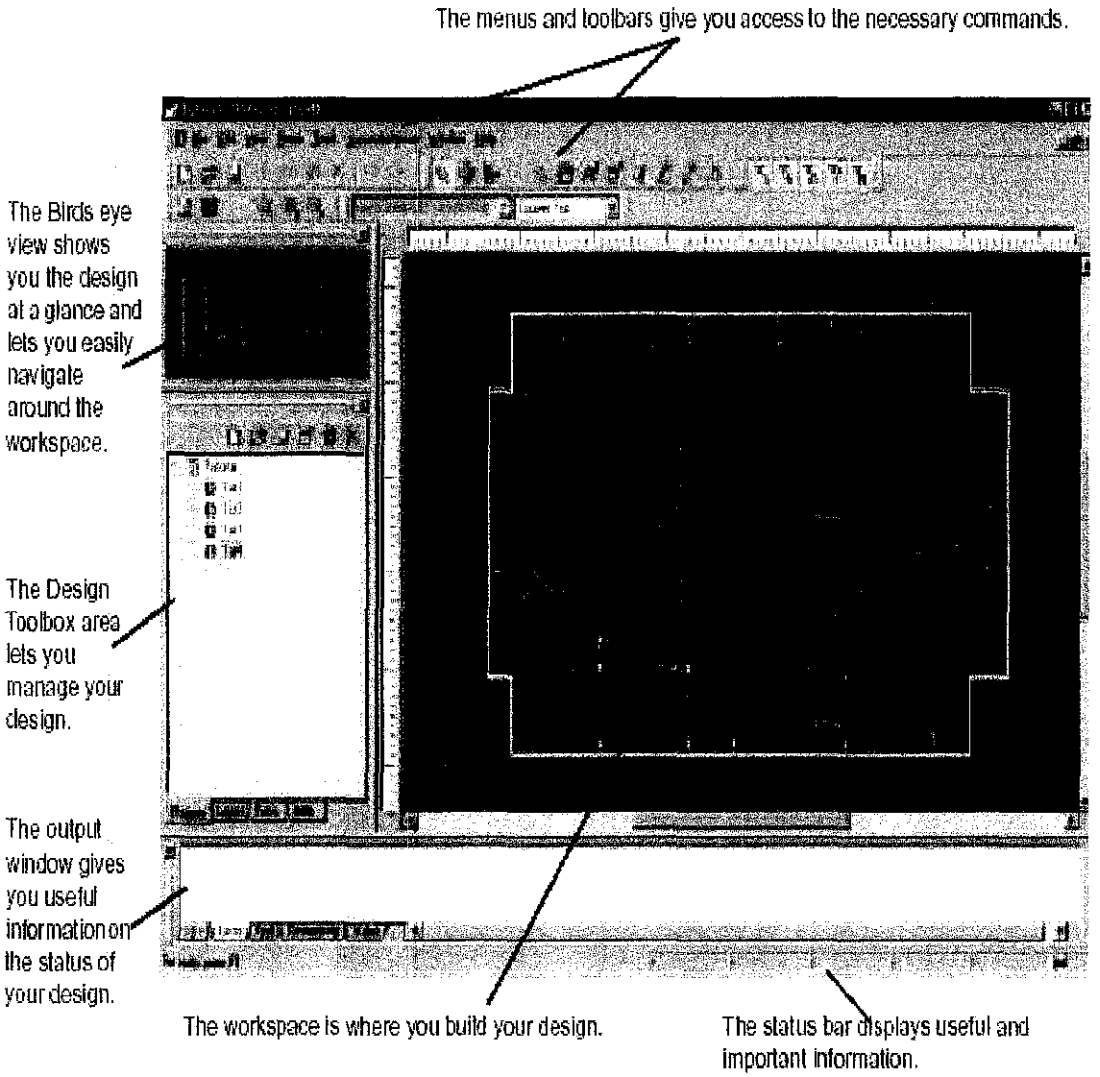
RELTOL= 0.01 (relative accuracy of voltages and currents)

The CoolMOS and power diode library can be found in infeneon website http://www.infineon.com/simulate or email to simulate@infineon.com.

This project is continuing for second phases where PCB is needed to conduct experiment on the Buck Converter circuit. In other to achieve the PCB, software like Ultiboard and Multisim is using to perform the arrangements and location of components before printed out the board.

The circuit has been modified in the simulation in order to meet the experimentation. New circuit and detail result is can be seen in the Chapter 4. In the same time, PCB board software in work up using the Ultiboard software. Using the manual the available on how to handle the software, make life easier. It may take a week to finish up the gerber file before hand in to the technician and sample layout can be seen as in ***Figure 12.***

Note The screen shown below is opened in Section 3.3 of this manual. When you open Ultiboard 2001, the default is no project open.



Note Your workspace will, by default, have a black background; however, for the purposes of this document, we show a white background.

Figure 12: Sample screen of Ultiboard 2001 software in order to work out the PCB

3.2 Tool required

3.2.1 Software

Pspice software simulation

Ultiboard 2001

3.2.2 Electronic components

a) Pulse-width modulating controller,
b) Transistor switch (CoolMOS) – SPB07N60C3,
c) Inductor – 0.4μH , 2.5μH , 4.25μH
d) Capacitor – 10 ηF
e) Power diode – IDP06E60
f) Resistor – 2 Ω , 10 Ω

Detail of list components can be referring to ***Appendix 3***.

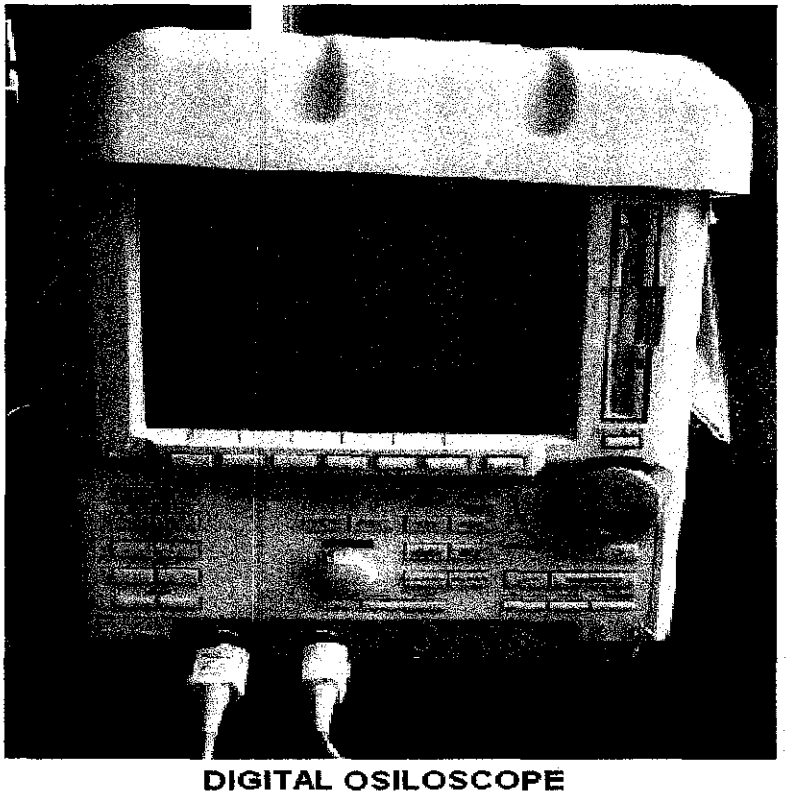
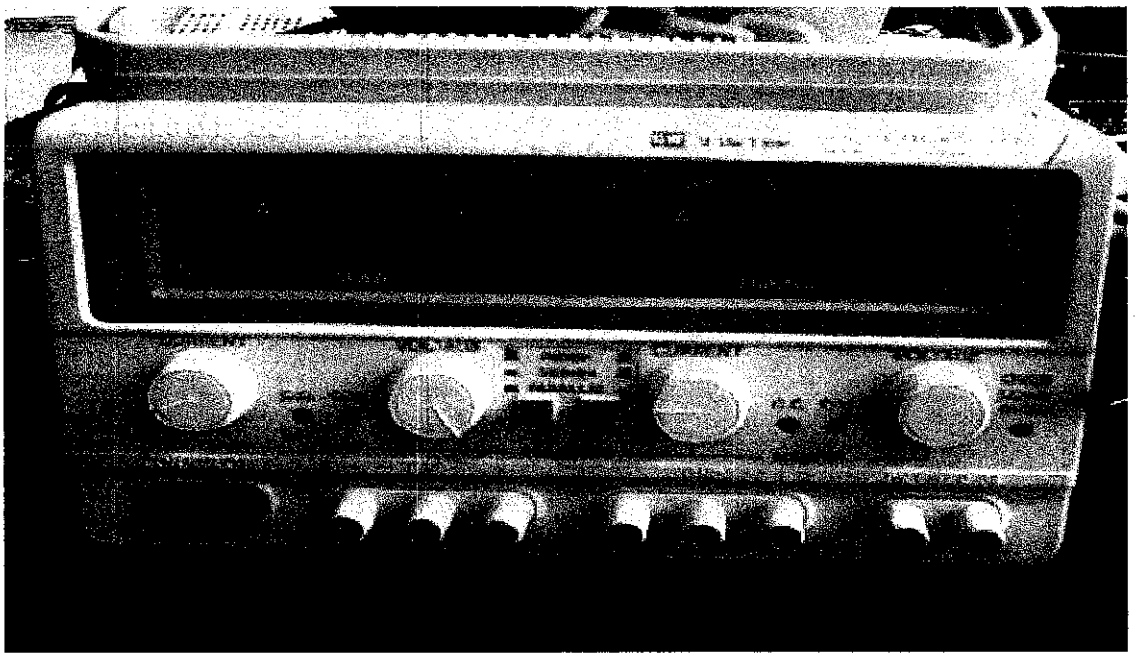


Figure 13: Digital oscilloscope for displaying the waveform

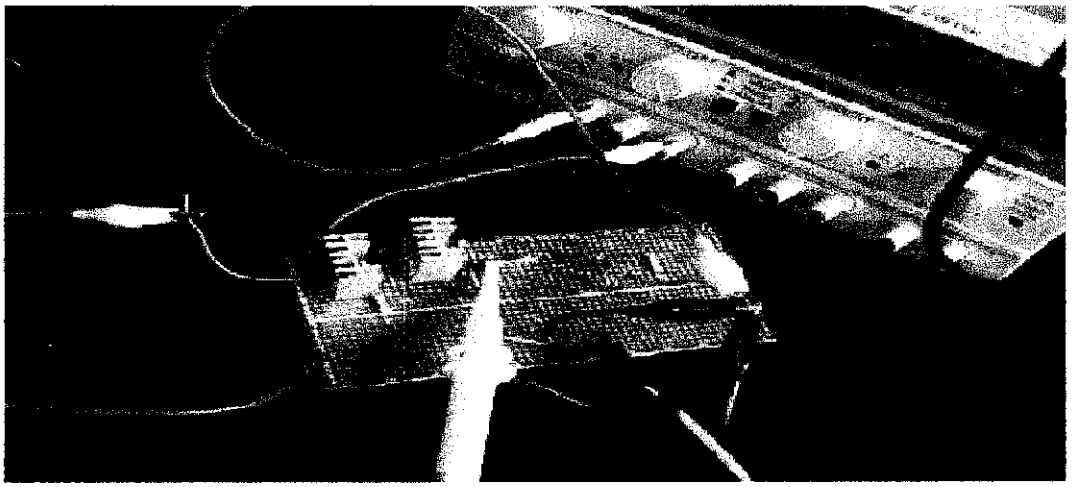
FUNCTION GENERATOR (V Pulse)

Figure 14: Function generator for triggered the V pulse



POWER SUPPLY

Figure 15: Power supply for input voltage



Measurement of the circuit during experiment

Figure 16: List of apparatus that used in the experiment

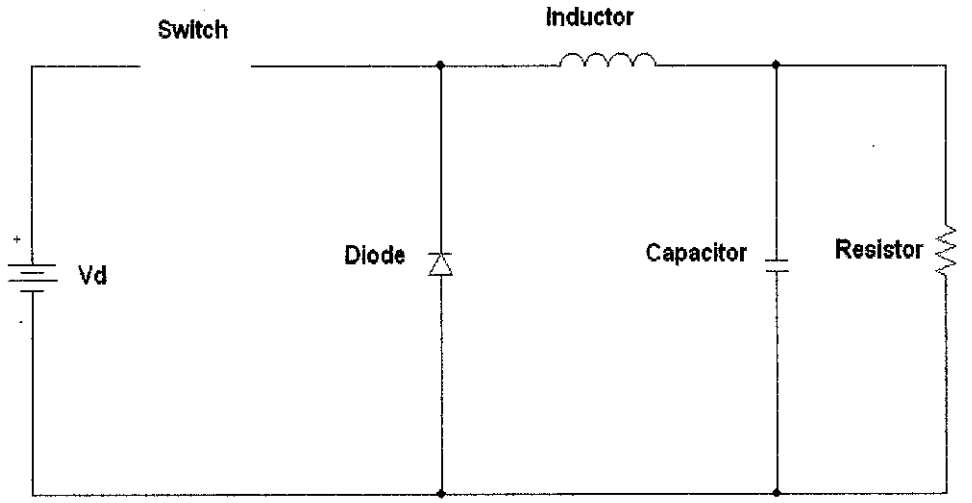
CHAPTER 4

RESULT AND DISCUSSION

4.0 RESULT

Results are divided into two sections which is simulation result and experimental result. Then, both of the results are compared to get the accuracy of the result.

Calculations for new inductor value:-



When inductor value, L = 0.4 μH:-

$$Xc = \frac{1}{\omega c} = \frac{1}{2\pi fc} = \frac{1}{2\pi(50kHz)(10\eta F)} = 318.31$$

$$XL = \omega L = 2\pi fL = 2\pi(50kHz)(0.4\mu H) = 0.1258$$

$$R = \frac{Xc \times R1}{R1 + Xc} = \frac{[(318.31)\times(2)]}{(2+318.31)} = 1.9875\Omega$$

$$z = \sqrt{R^2 + XL^2} = \sqrt{(1.9875^2)+(0.1258^2)} = 2\Omega$$

$$\theta = \tan^{-1}\left(\frac{XL}{R}\right) = \tan^{-1}\left(\frac{0.1258\Omega}{1.9875\Omega}\right) = 3.22^0$$

$$p.f = \cos\theta = \cos(3.22^0) = 0.998$$

When inductor value, L = 2.5 μH:-

$$Xc = \frac{1}{\omega c} = \frac{1}{2\pi fc} = \frac{1}{2\pi(50kHz)(10\eta F)} = 318.31$$

$$XL = \omega L = 2\pi fL = 2\pi(50kHz)(2.5\mu H) = 0.7854$$

$$R = \frac{Xc \times R1}{R1 + Xc} = \frac{[(318.31)\times(2)]}{(2+318.31)} = 1.9875\Omega$$

$$z = \sqrt{R^2 + XL^2} = \sqrt{(1.9875^2) + (0.7854^2)} = 2.137\Omega$$

$$\theta = \tan^{-1}\left(\frac{XL}{R}\right) = \tan^{-1}\left(\frac{0.7854\Omega}{1.9875\Omega}\right) = 21.56^0$$

$$p.f = \cos\theta = \cos(21.56^0) = 0.93$$

When inductor value, L = 4.25 μH:-

$$Xc = \frac{1}{\omega c} = \frac{1}{2\pi fc} = \frac{1}{2\pi(50kHz)(10\eta F)} = 318.31$$

$$XL = \omega L = 2\pi fL = 2\pi(50kHz)(4.25\mu H) = 1.3351$$

$$R = \frac{Xc \times R1}{R1 + Xc} = \frac{[(318.31)\times(2)]}{(2+318.31)} = 1.9875\Omega$$

$$z = \sqrt{R^2 + XL^2} = \sqrt{(1.9875^2) + (1.3351^2)} = 2.3943\Omega$$

$$\theta = \tan^{-1}\left(\frac{XL}{R}\right) = \tan^{-1}\left(\frac{1.3351\Omega}{1.9875\Omega}\right) = 33.891^0$$

$$p.f = \cos\theta = \cos(33.891^0) = 0.83$$

Table 1: Relationship between inductor value and power factor (currently)

Value of Inductor	Value of Power factor (cos θ)
0.4 μH	**0.998**
2.5 μH	**0.930**
4.25 μH	**0.830**

4.0.1 Result simulation

The simulation has been conducted using to compare the experiment result with the actual result. The input voltage been used is 50V as trial [11]. The details of the simulation result are as follow:-

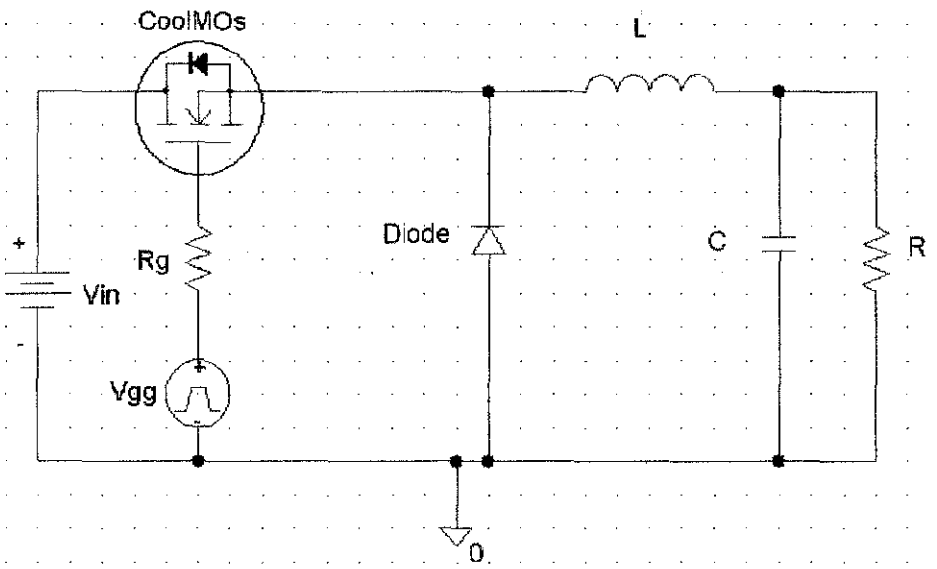


Figure 17: The circuit the have been modified for simulation used

This is the output waveform produced by the modified circuit.

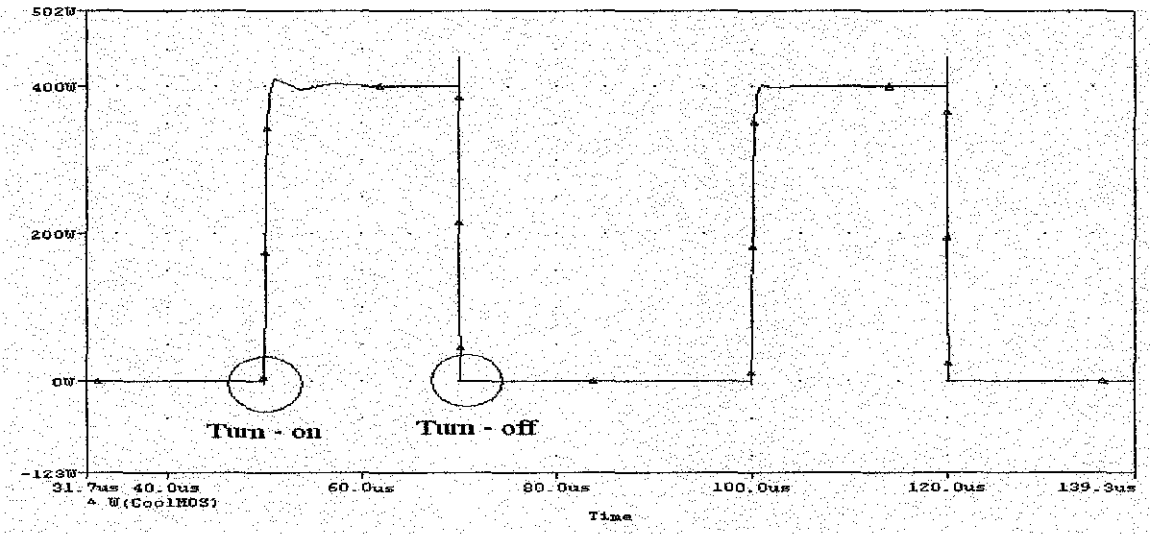


Figure 18: Waveform that show point of switching losses

Measurement for one power factor, pf which is 0.998:-

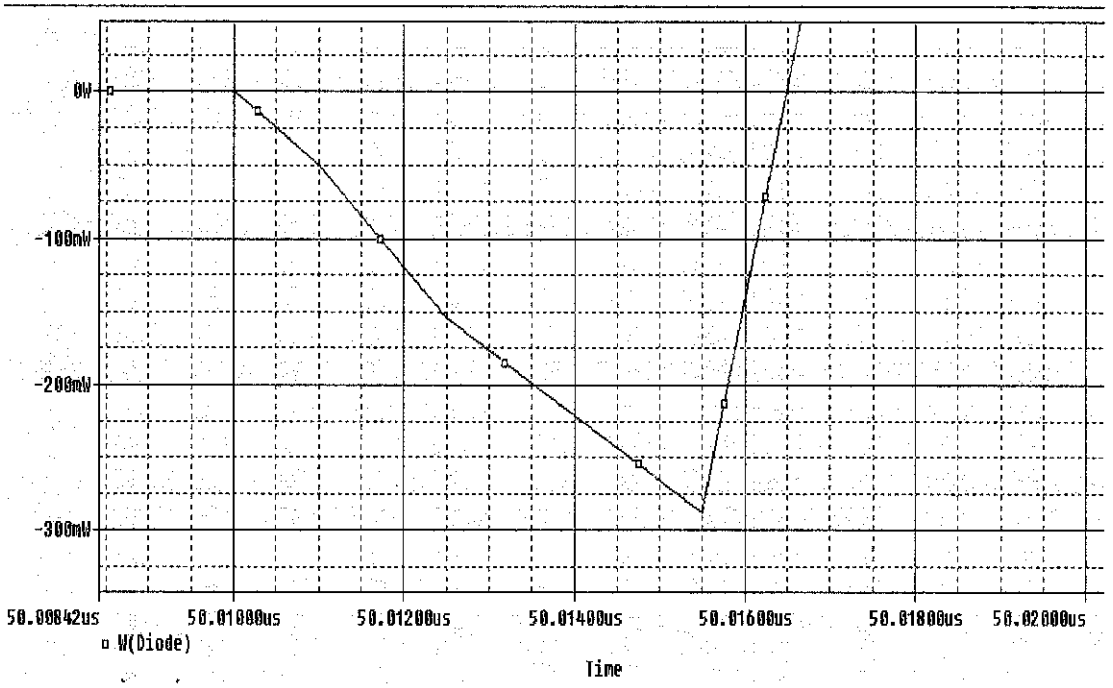


Figure 19: Region of switching losses during Diode during Turn-off

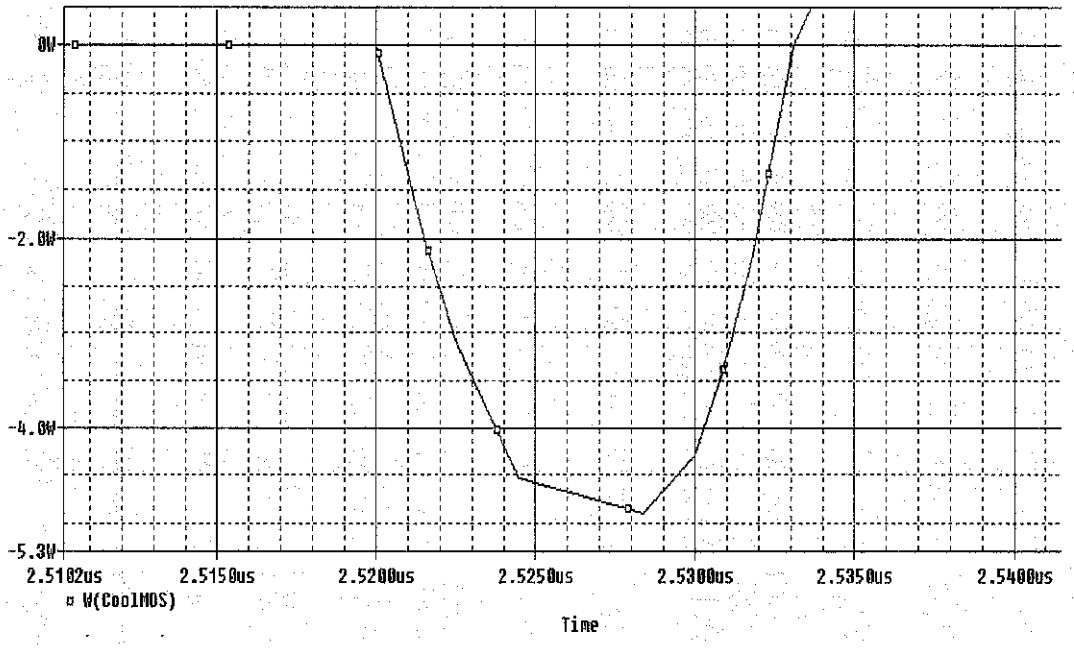


Figure 20: Region of switching losses during CoolMOS during Turn-on

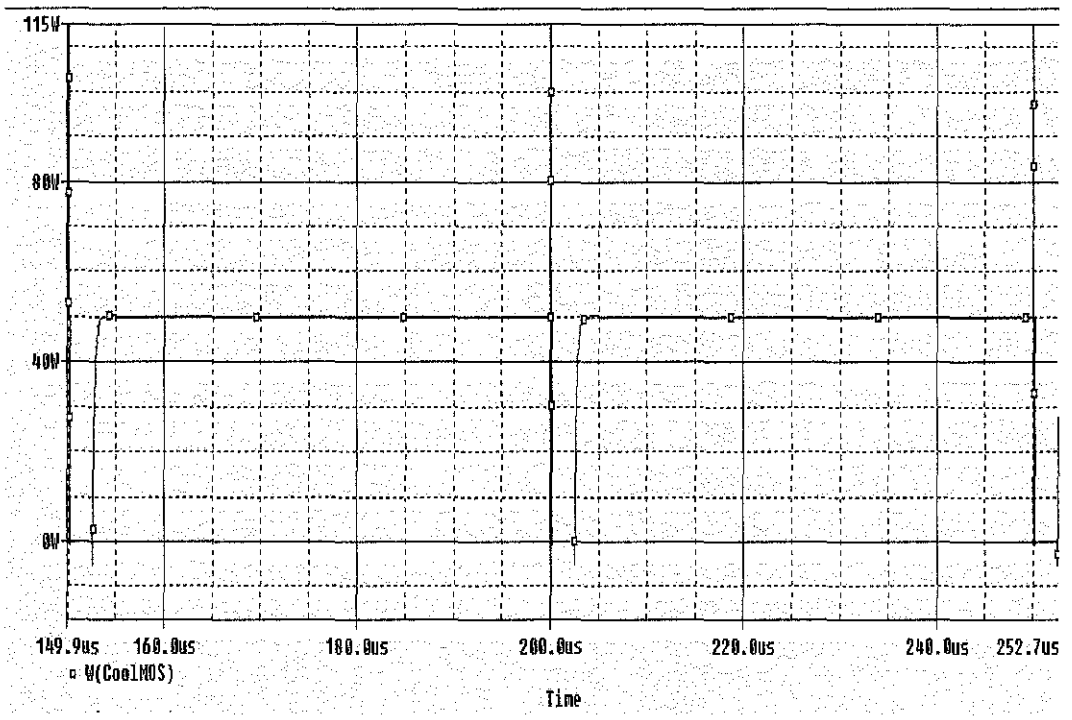


Figure 21: Waveform of CoolMOS during switching

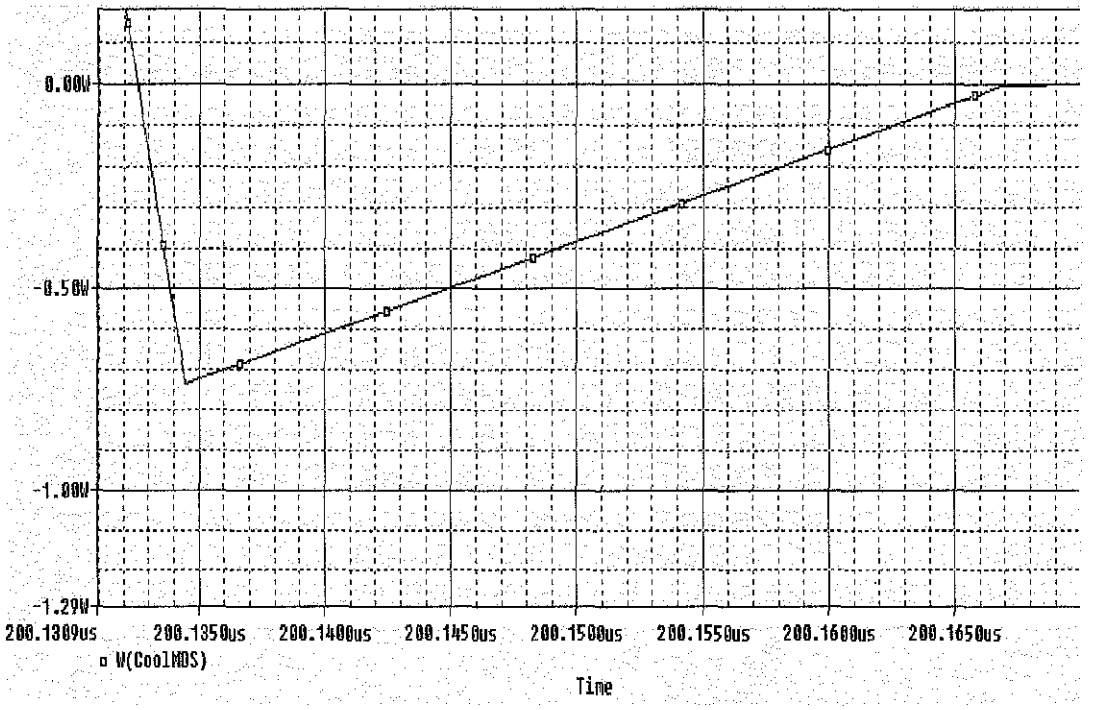


Figure 22: Region of switching losses during CoolMOS during Turn-off

Comparison waveform for three power factor using Buck converter circuit:-

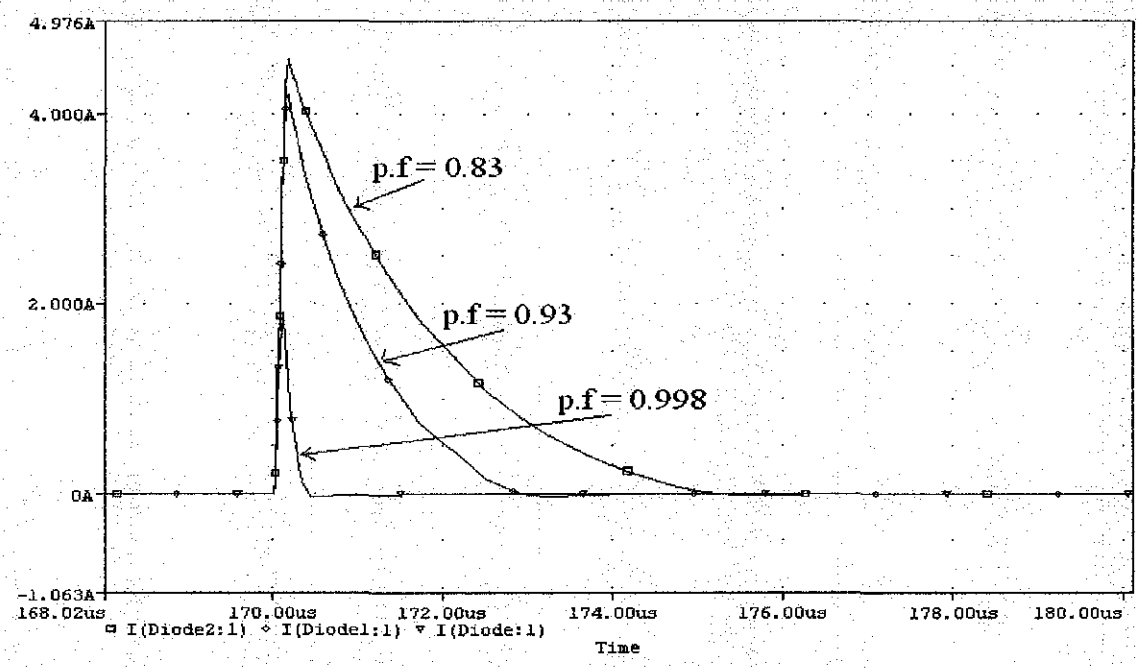


Figure 23: Comparison of waveform between low and high power factor

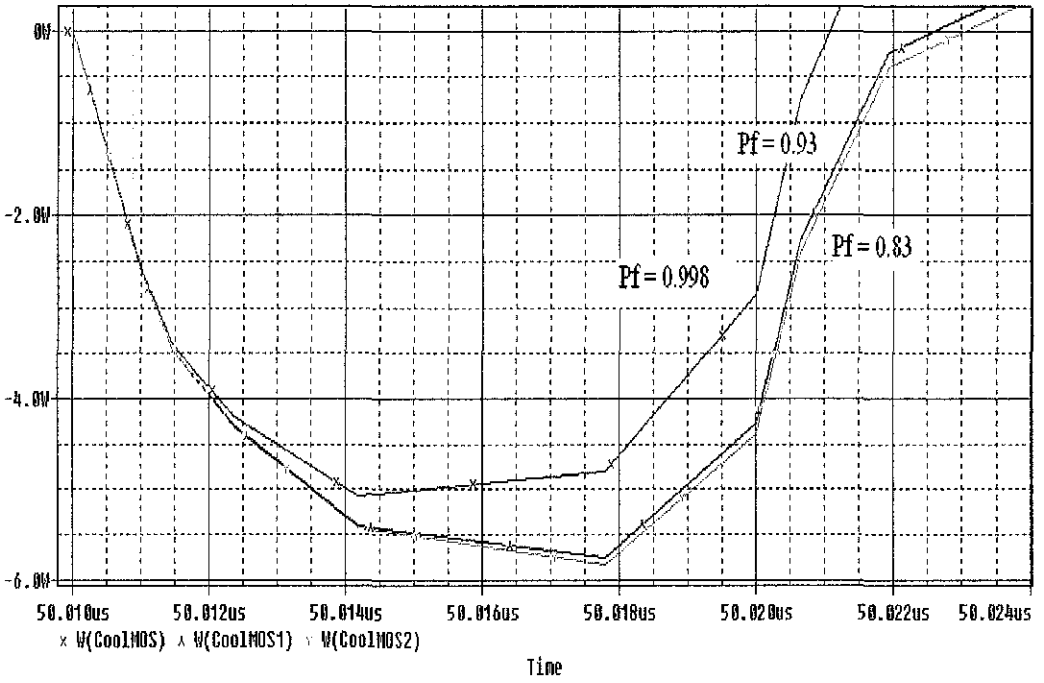


Figure 24: Region of switching losses during Turn – on (different power factor)

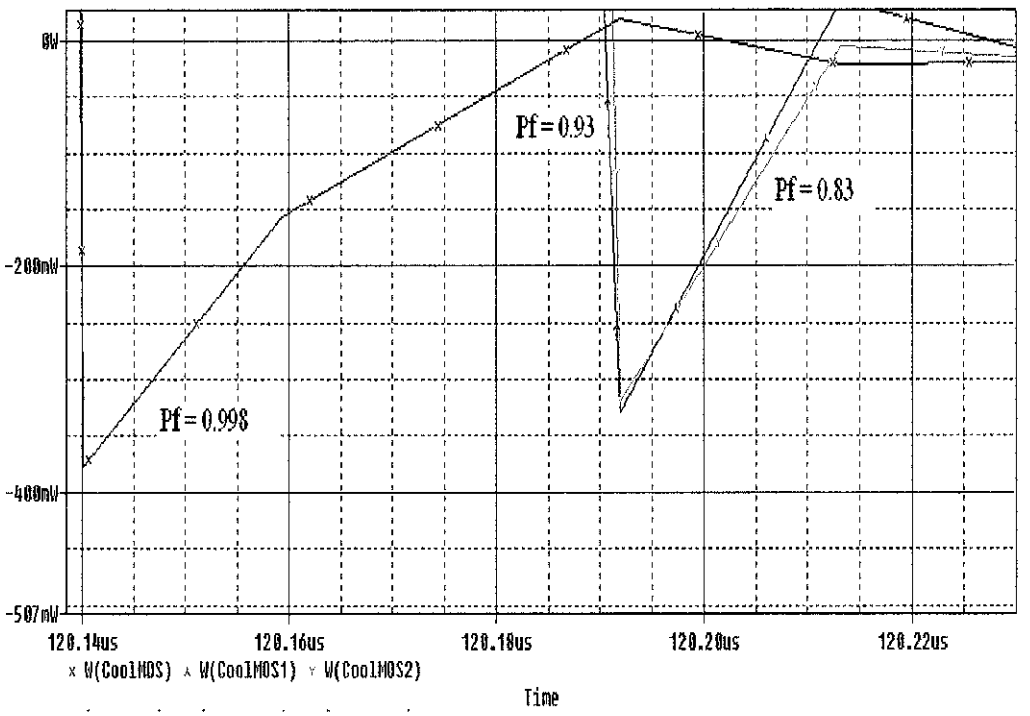


Figure 25: Region of switching losses during Turn – off (different power factor)

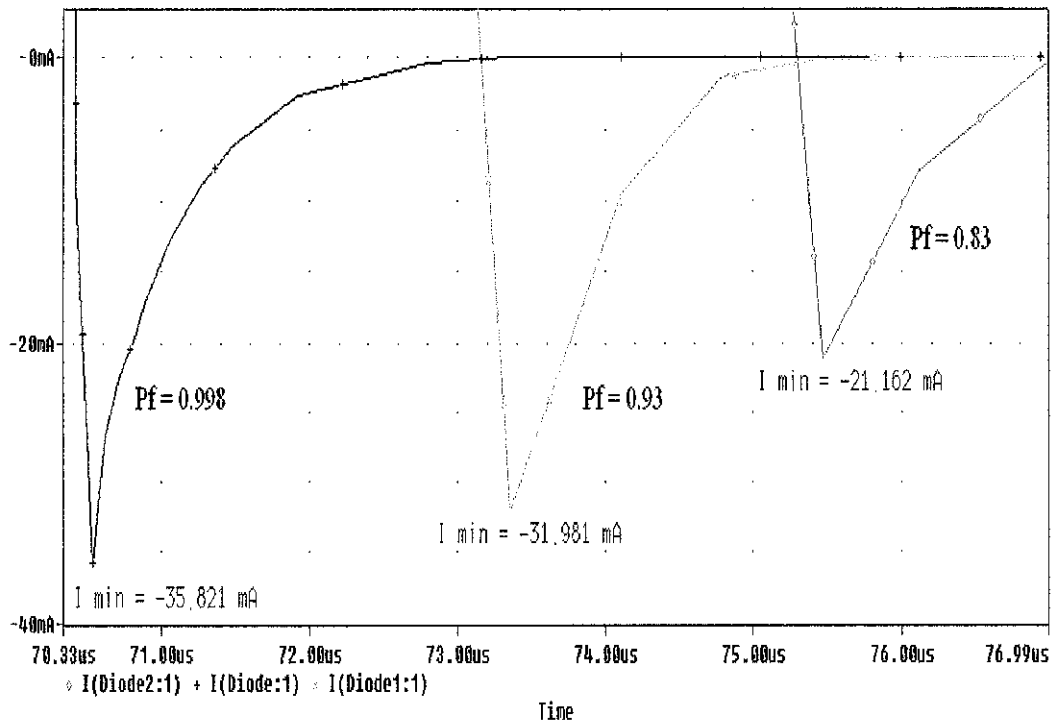


Figure 26: Waveform of Peak Reverse recovery Current (different power factor)

How to calculate the losses:-

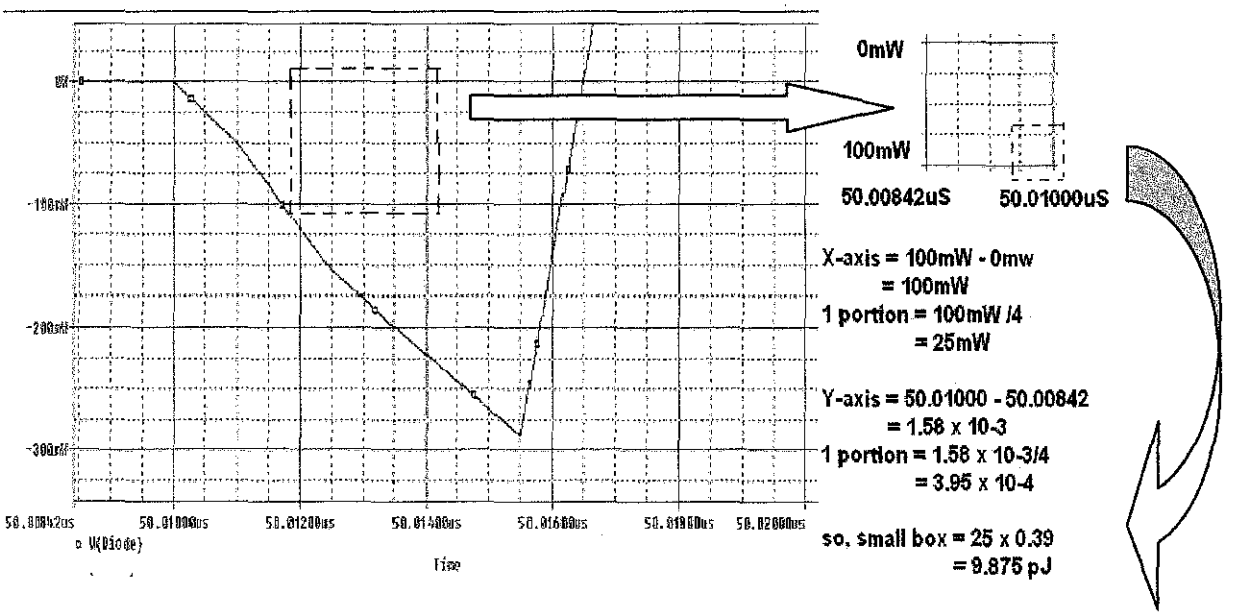


Figure 27 – Calculation of power losses

When we got the value of small box, we need to calculate total box under the region and calculate overall losses [11]. Let's say the total small box under the region is 50. So, overall losses are:-

Small box = 9.875 pJ with 50 box

Losses = 9.875pJ x 50

= 49.375 nJ

Table 2: Switching Losses produced by different power factor

Characteristics	*p.f = 0.998*	*p.f = 0.930*	*p.f = 0.830*
Peak Reverse Recovery Current (mA)	*-35.821*	*-31.981*	*-21.162*
CoolMOS Turn-on loss (nJ)	*56.75*	*67*	*67.75*

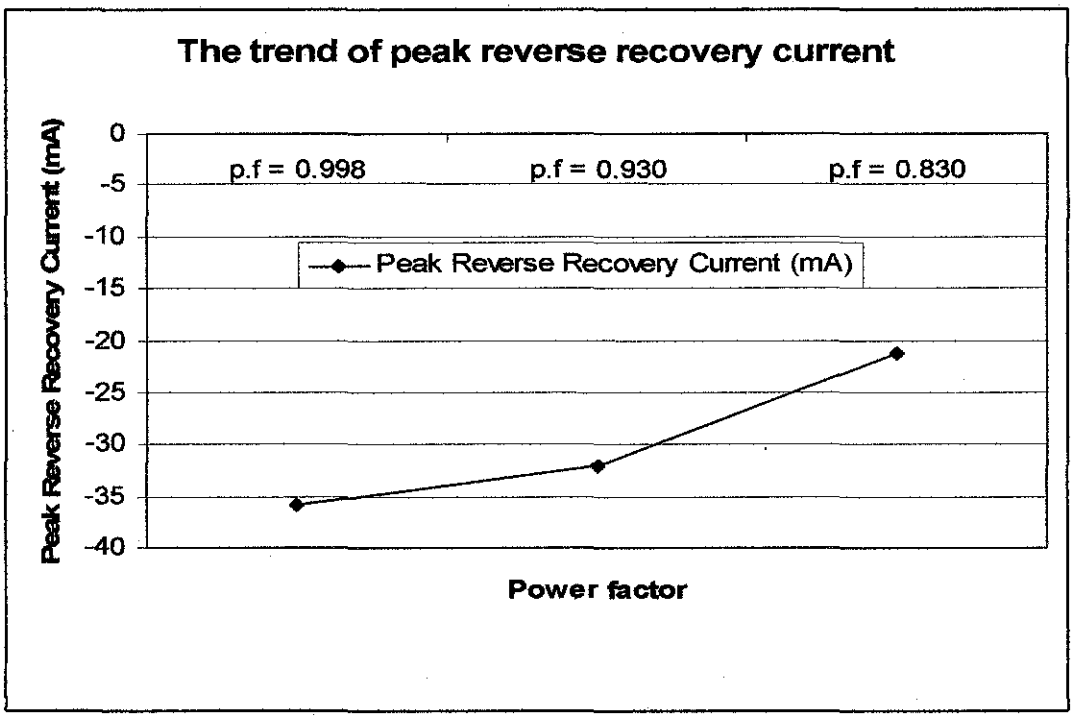


Figure 28: The trend of peak reverse recovery current

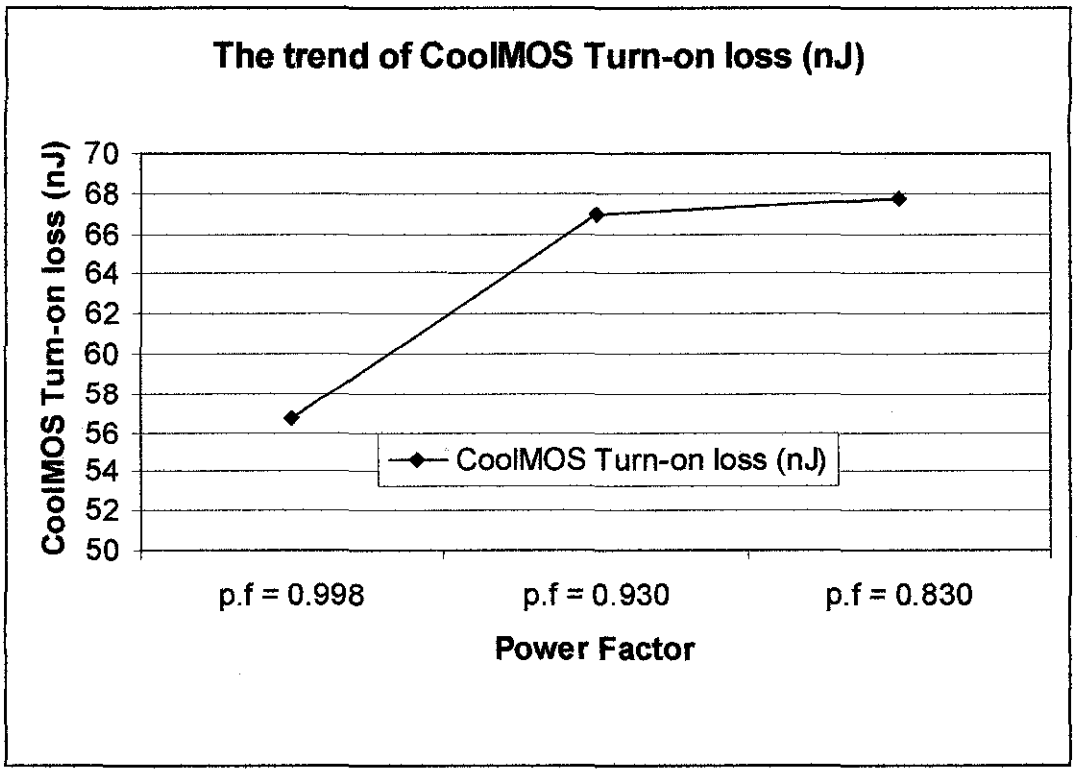


Figure 29: The trend of CoolMOS Turn – on loss (nJ)

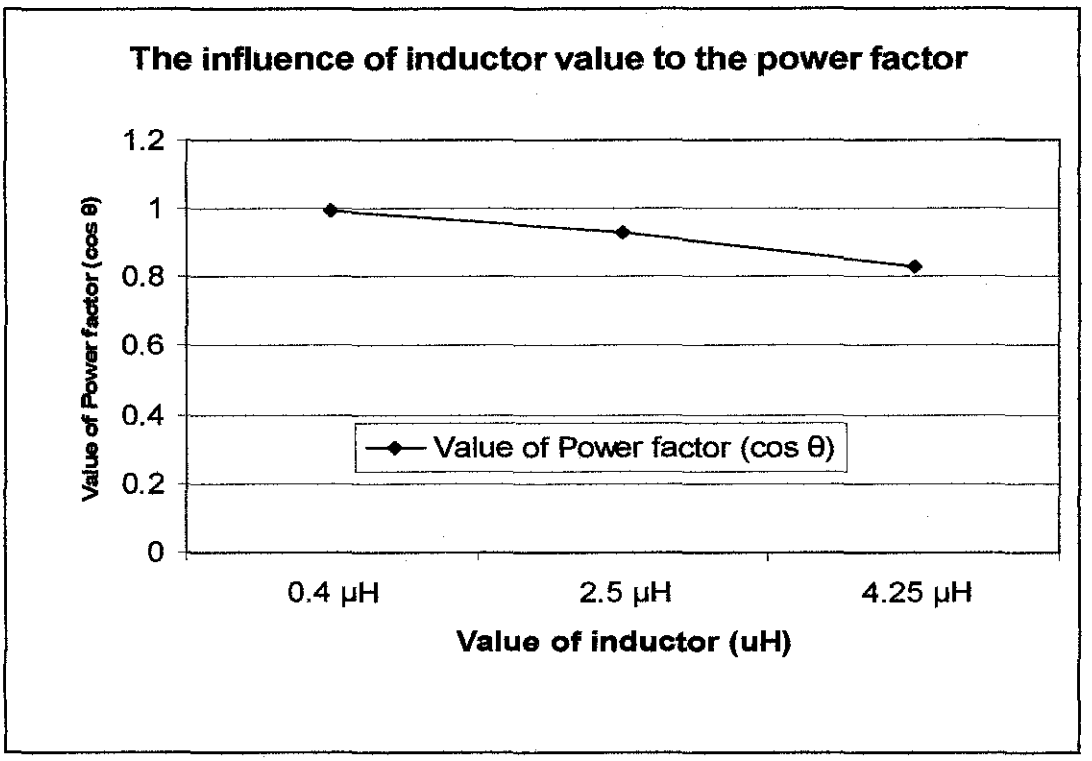


Figure 30: The influence of inductor value to the power factor

From the result above, as we increased the power factor, the switching losses is reduced. So, as conclusion the switching losses is perpendicular to the value of power factor.

4.0.2 Result experiments

After conduct the experiment, the result obtained is slightly different. The voltage input that used to trigger the CoolMOS is 50V. It is important to make sure that V pulse that triggered the CoolMOS is not very high. V pulse is between 3 to 10 V which is almost 40 KHz maximum. As the first stage, equipment problem appear where no current probe to measured the current drop in order to calculate the switching losses. Finally, that problem is overcome by putting extra resistor, 1 ohm along the measured junction.

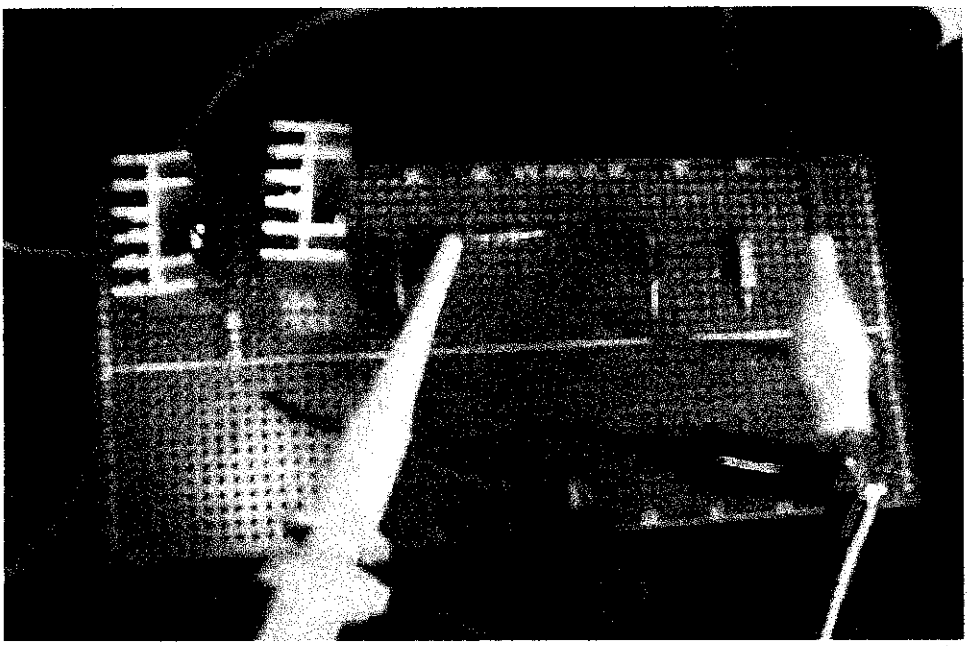


Figure 31: Layout of the circuit during experiment

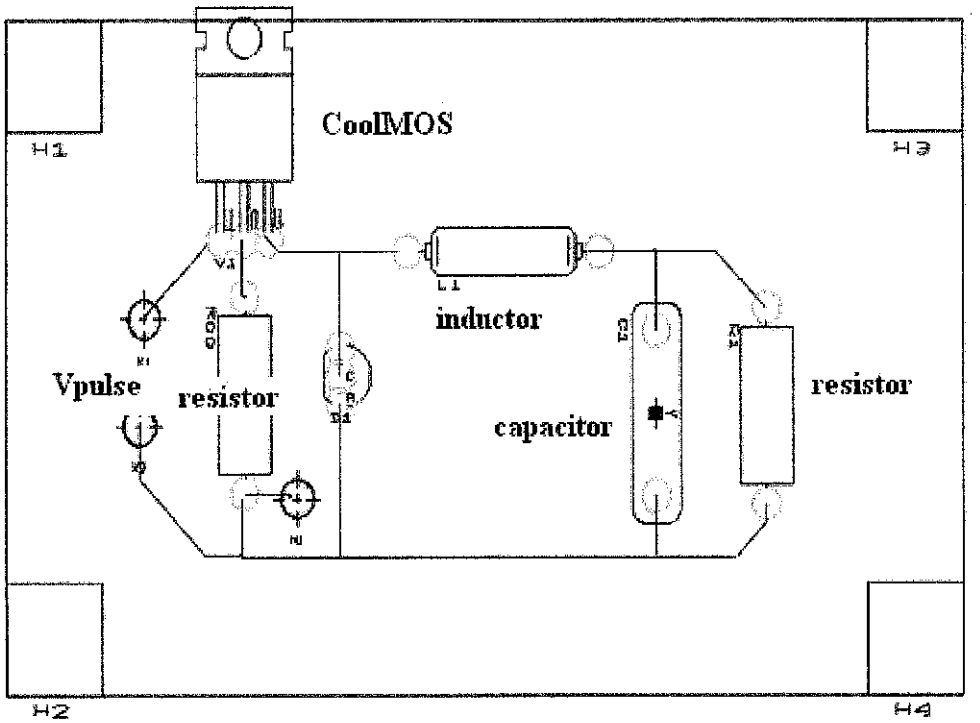


Figure 32: Layout of components using the Ultiboard

How to measure the switching losses:-

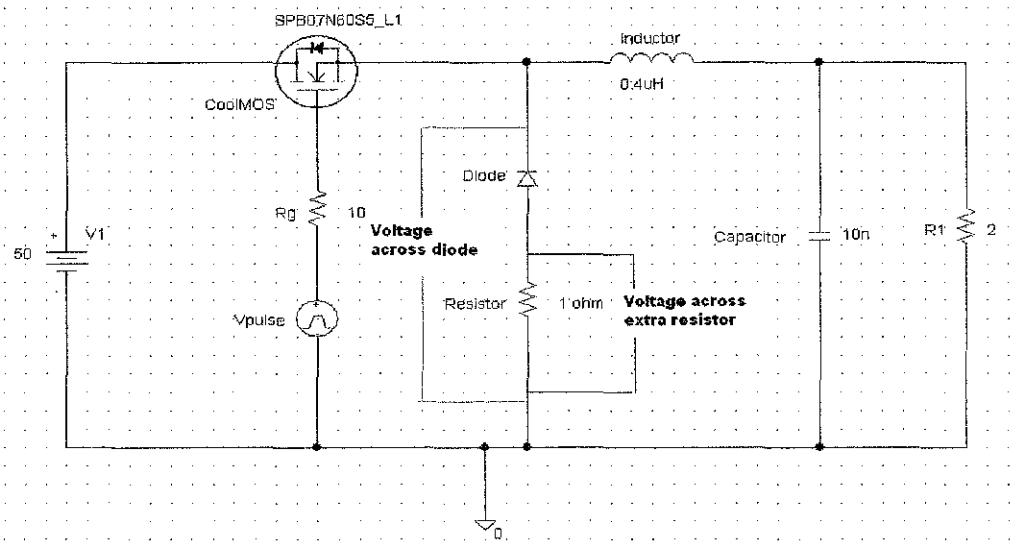


Figure 33: Circuit with extra resistor

First, we measured the voltage trough the extra resistor using channel 1 of the digital oscilloscope. Then, we measured the voltage across the diode using channel 2 of the digital oscilloscope. Finally, we multiply both channels to get the power losses along the diode. Lets say:-

$V = IR$

Resistor = 1 Ohm

So, $V = I$ *(1 Ohm)*

$V = I$, *current along the diode* ..... *(1)*

$P = IV$ ..... *(2)*

Substitute equation (1) into equation (2)

$P = IV$

So, the same procedure is applied to others in other to get the power losses.

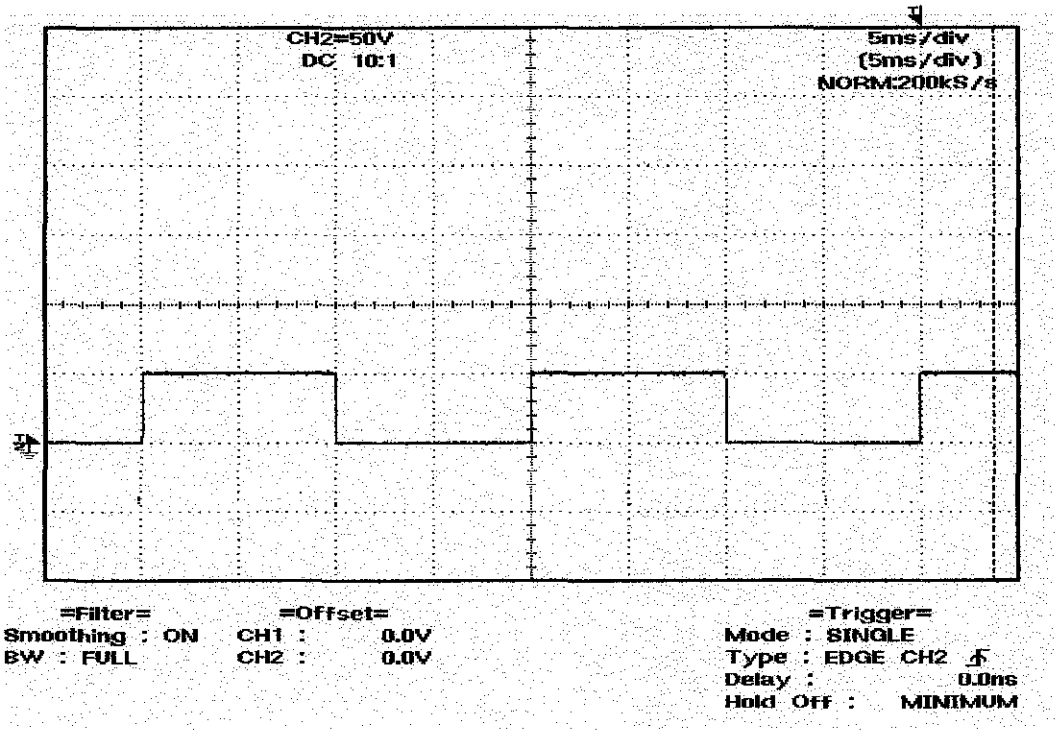


Figure 34: Waveform of the V pulse triggered to the CoolMOS

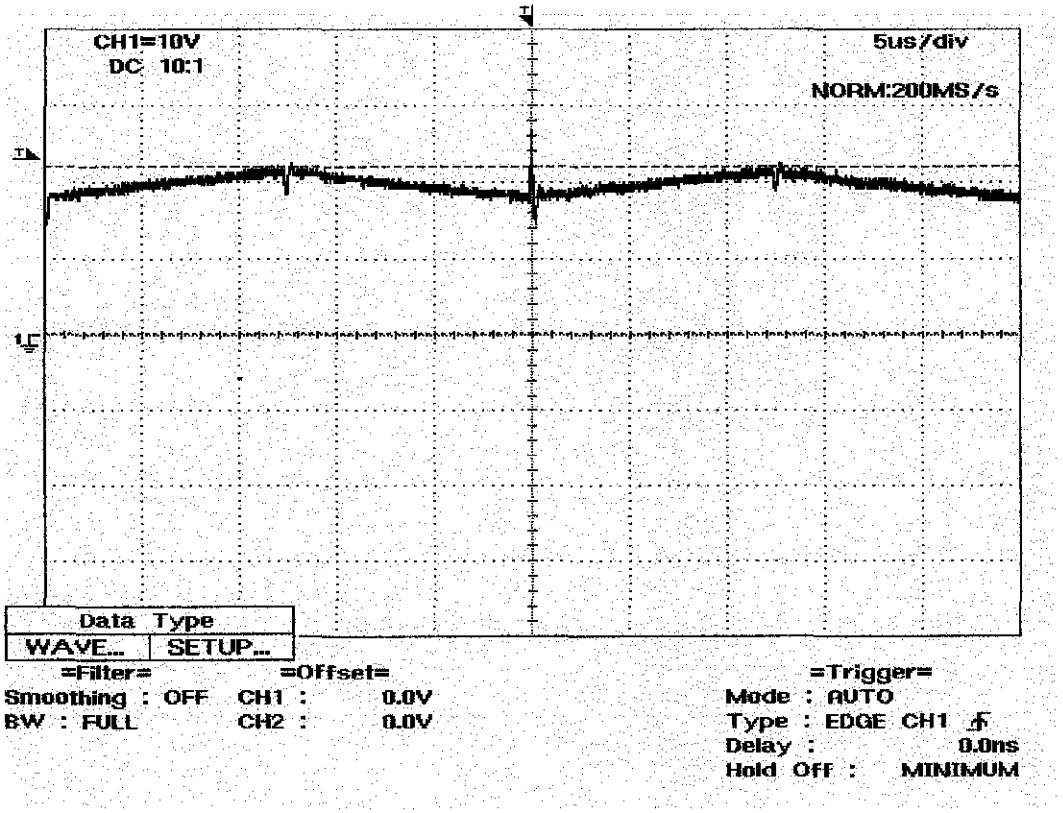


Figure 35: Waveform of the Voltage output

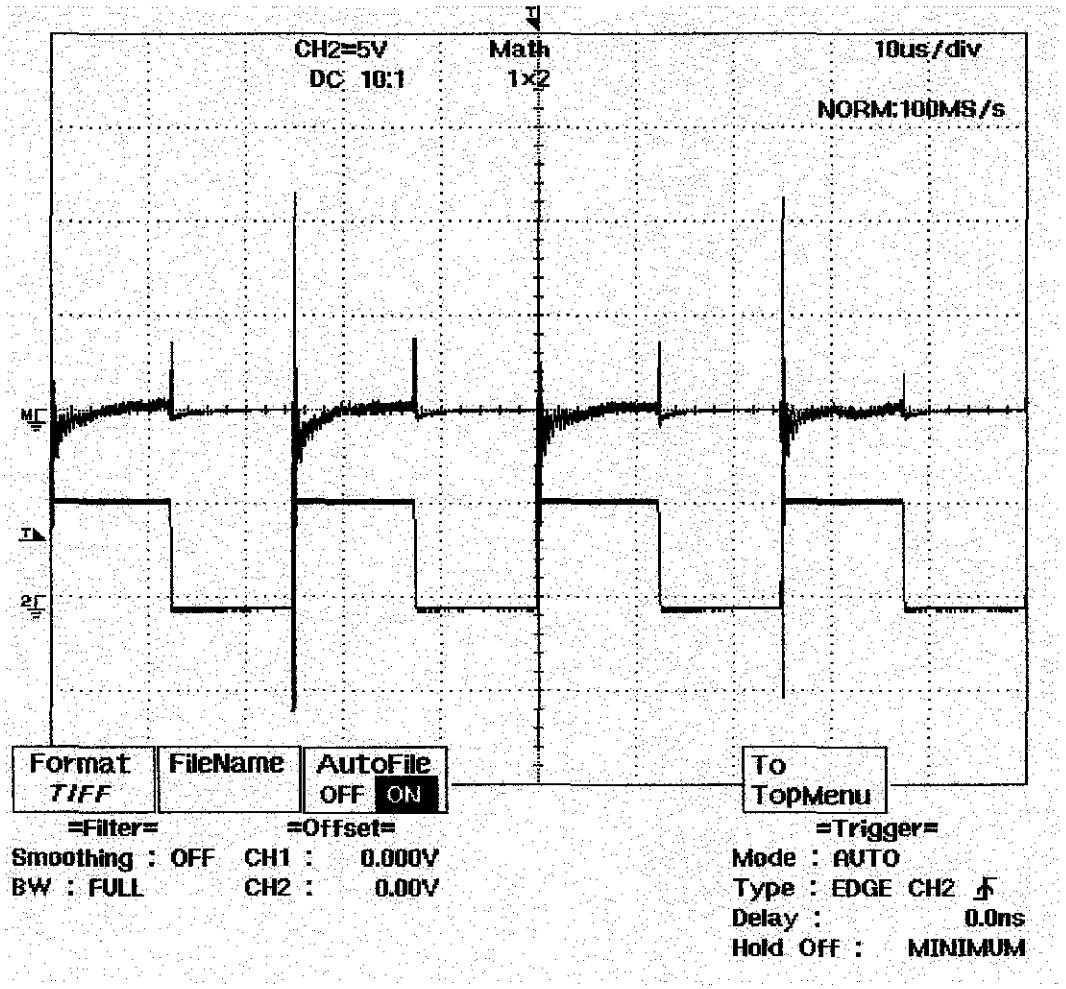


Figure 36: Waveform of Peak Reverse recovery Current (pf = 0.998)

Table 3: Switching Losses produced by different power factor (experiment)

Characteristics	*p.f = 0.998*	*p.f = 0.930*	*p.f = 0.830*
Peak Reverse Recovery Current (mA)	*-30.2*	*-25.4*	*-18.4*
CoolMOS Turn-on loss (nJ)	*53.7*	*62.8*	*65.9*

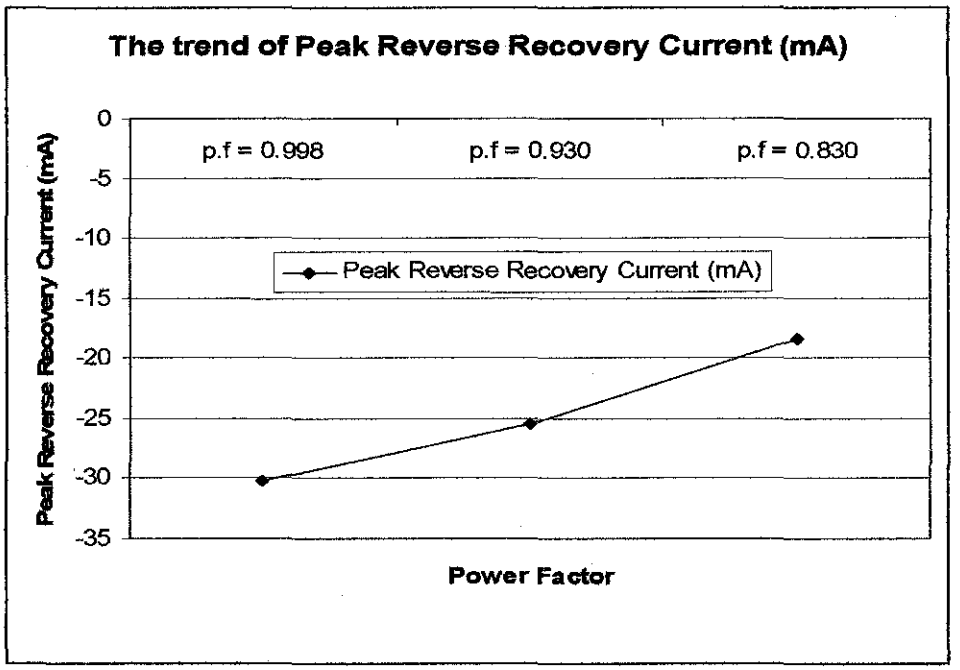


Figure 37: The trend of peak reverse recovery current (mA)

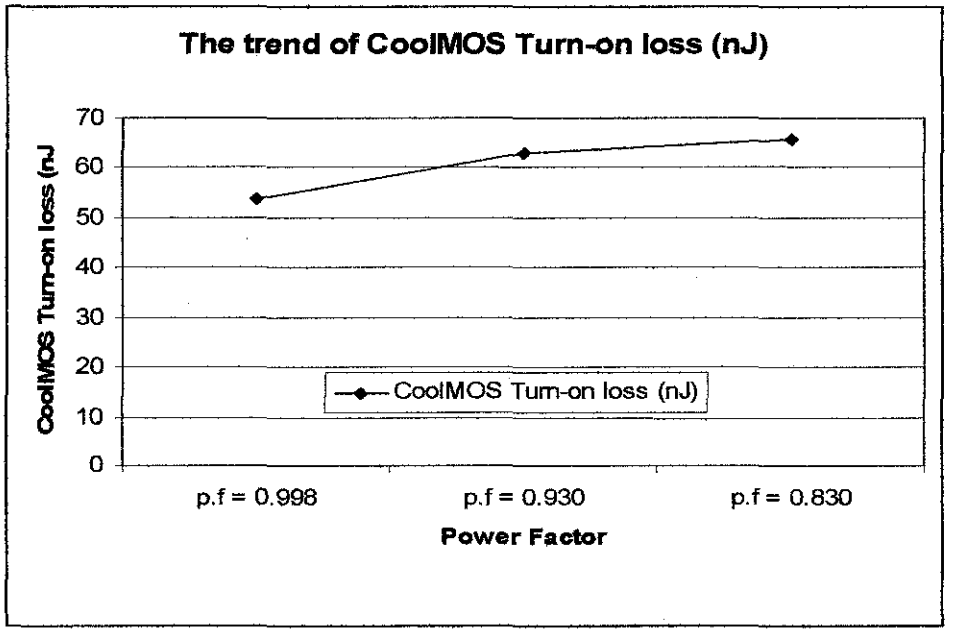


Figure 38: The trend of CoolMOS Turn – on loss (nJ)

4.0.2 Comparison results

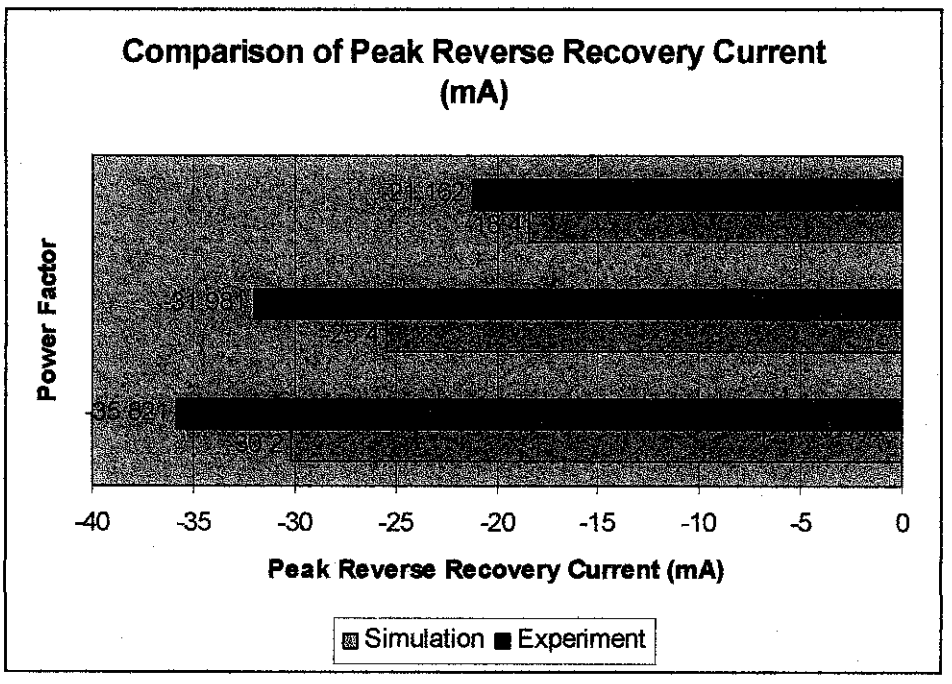


Figure 39: Comparison results of peak reverse recovery current (mA)

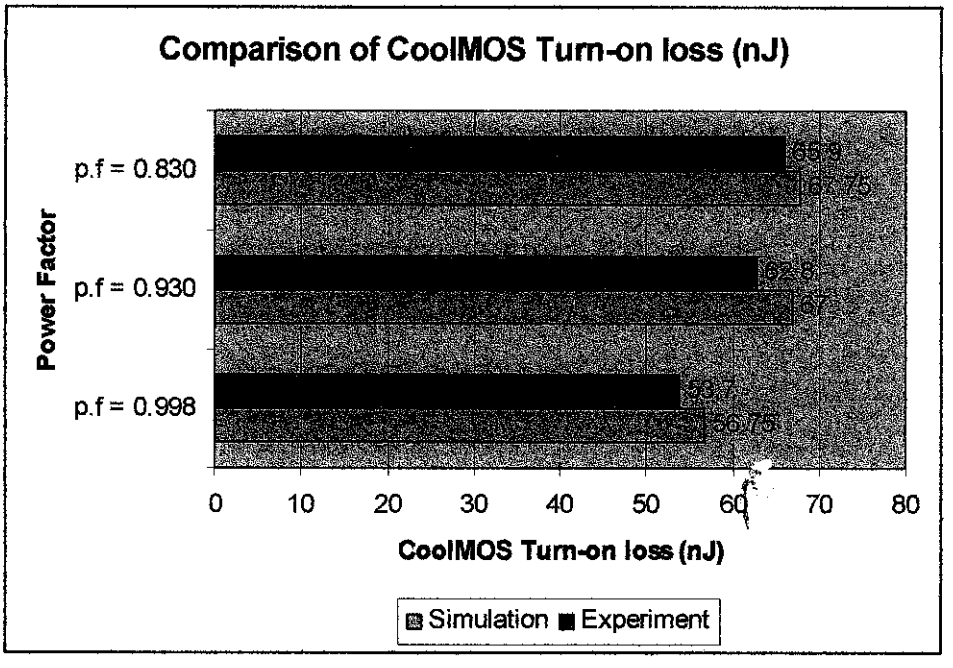


Figure 40: Comparison results of CoolMOS Turn – on loss (nJ)

4.0.4 Extra simulation between CoolMOS and MOSFET

This simulation done is to prove that CoolMOS is a good device in order to reduce the switching losses in Buck Converter circuit. Not only the value of inductor, the device use for switching also play important role in order to reduce the switching losses.

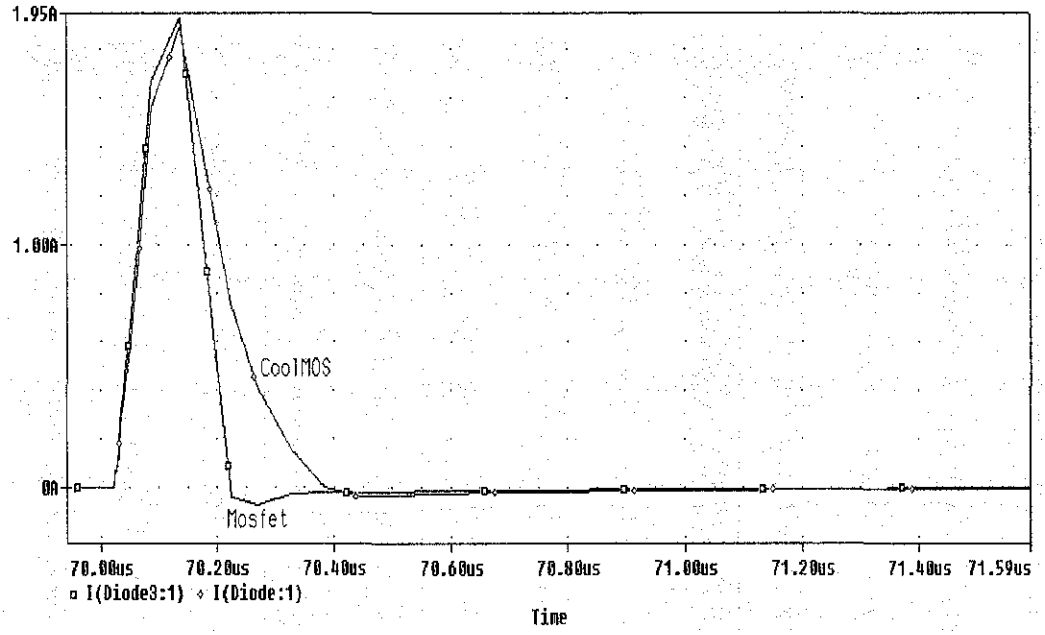


Figure 41: Comparison of waveform between MOSFET and CoolMOS

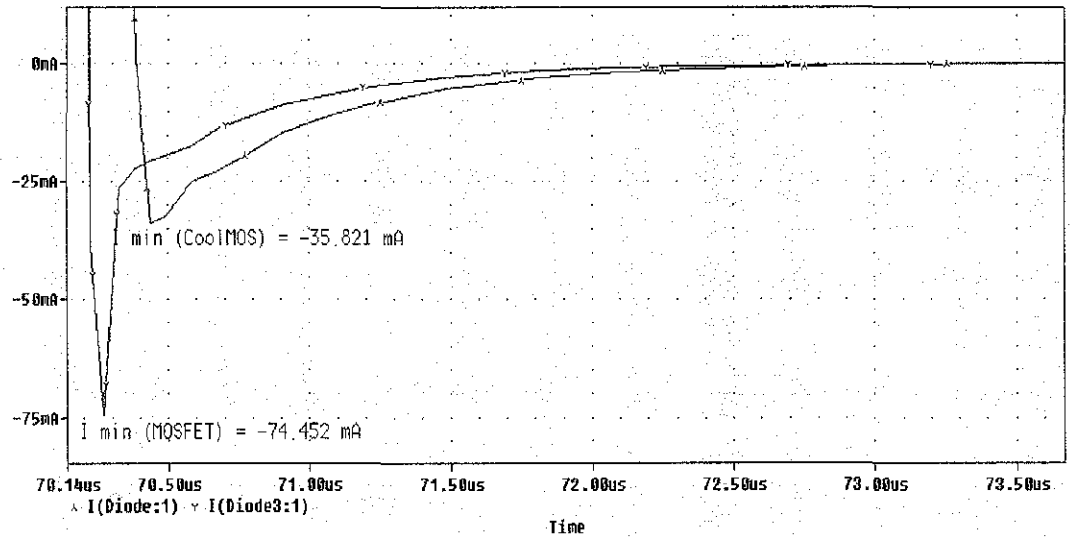


Figure 42: Waveform of Peak Reverse recovery Current

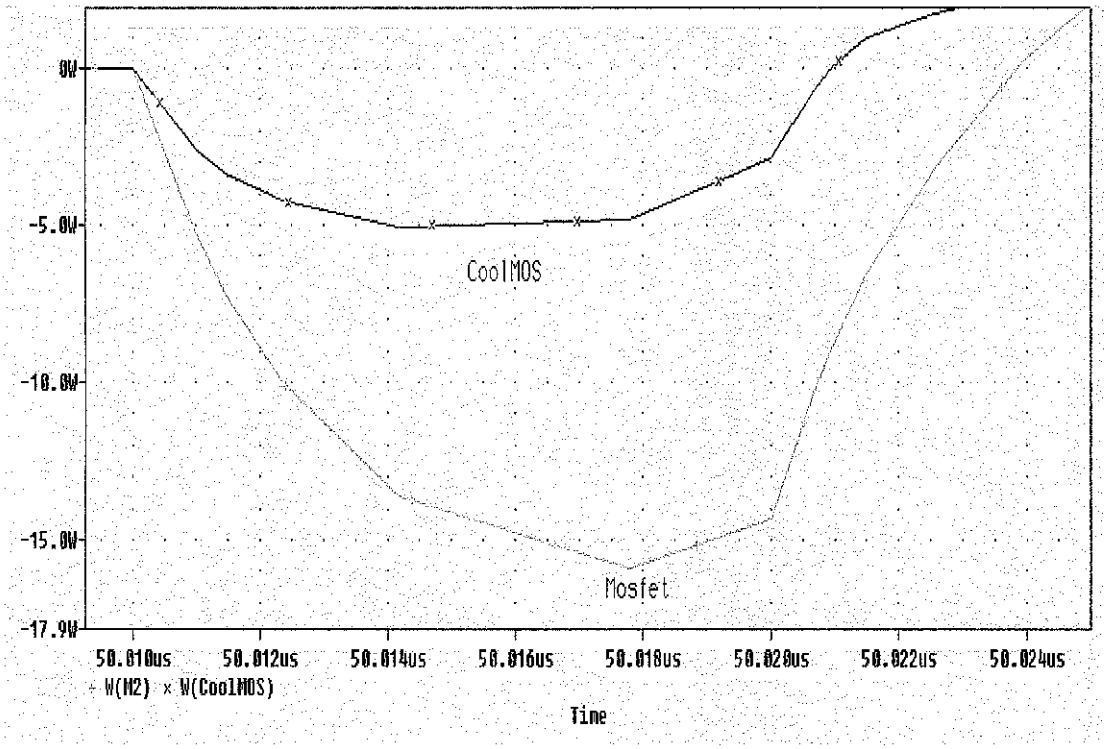


Figure 43: Region of switching losses during Turn – on

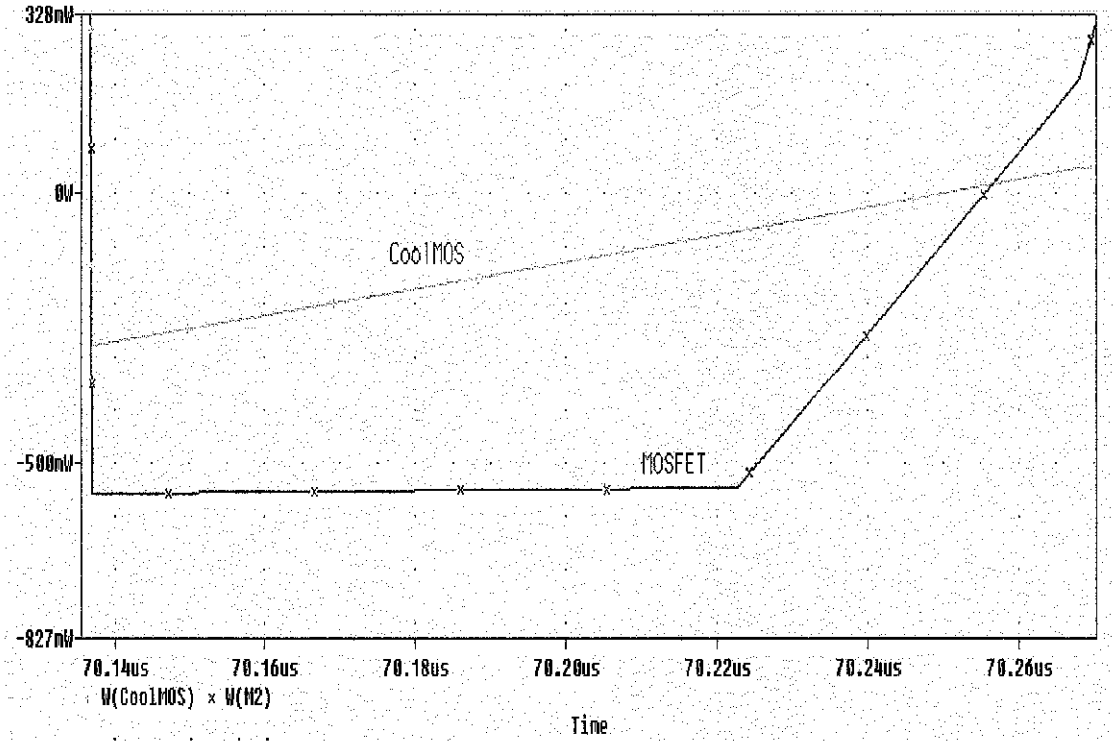


Figure 44: Region of switching losses during Turn – off

Table 4: Total switching Energy loss between CoolMOS and MOSFET

Characteristics		MOSFET
Peak Reverse Recovery Current (mA)		-74.452
Diode Turn-off (nJ)		5.6
CoolMOS / MOSFET Turn-on loss (nJ)		143

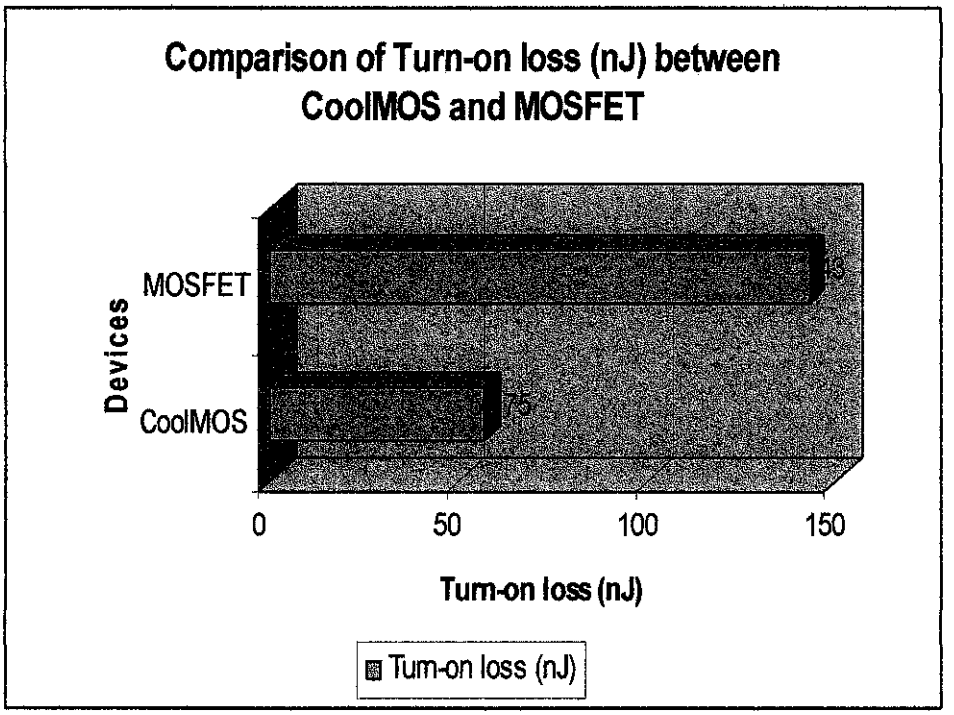


Figure 45: Comparison of Turn – on loss (nJ) between CoolMOS and MOSFET

4.1 DISCUSSION

From the results above, it can be seen that the experiment results meet the simulation results although there is slightly different of the figure obtained. May the accuracy of the probe influence the results obtained. It is proved that as we increase the value of power factor, the switching losses will reduced. Higher power factor contribute to the better efficiency of the system.

If power factor is 0.998, the peak reverse recovery current produces is -35.821 mA. But if the power factor is 0.830, the peak reverse recovery current produces is -21.162 mA. Moreover, if power factor is 0.998, the CoolMOS turn – on loss produces is 56.75 nJ. But if the power factor is 0.830, the CoolMOS turn – on loss produces is 67.75 nJ. It is proved that if we increase the power factor the losses will be reduce.

Moreover, CoolMOS perform much better compared to MOSFET. It can reduce almost 50% of switching losses compared to MOSFET. So, as conclusion, in order to achieve high power factor, value of inductor play important rule. As we reduce the value of inductor, power factor value will increase. In order to reduce the switching losses, selection of the value of power factor and switching devices will influences the trend of the losses produce.

CHAPTER 5

RECOMMENDATION

After conduct this project, I feel that it is still weaknesses which can be improved in the future. So, here, there a few recommendations:-

1) Use appropriate equipment during experiment such as current probe
2) Varies the scope of the project by doing comparison between CoolMOS and MOSFET and IGBT in order to prove that devices are the best among those.
3) Ordering of the components must be done earlier in order to avoid late delivery

CONCLUSION

Buck converter provides an output voltage (or bus voltage) lower than the peak line voltage, been very suitable for medium and low output voltage applications. This converter is very suitable in investigation this power factor correction. With the limit of power factor not less than 0.85, switching losses can be reduces by choosing the suitable value of inductor and capacitor in order to produce high power factor. If the power factor bigger and almost unity power factor (p.f = 1), the system become more perfect and the best.

Switching devices also important. CoolMOS is one of the best devices because it can reduce almost 50% of switching losses compared to MOSFET.

This project and research will exposed the student to the new development of MOSFETS and semiconductor industry; at the same time gain some knowledge on how to design the circuit of Buck Converter using CoolMOS. Indirectly, it practices us on how to be a good design engineer.

CHAPTER 6
REFERENCES

[1] Abraham I. Pressman, 1998, *"Switching Power Supply Design"*, New York Mc Graw-Hill, Second edition.

[2] Mohan,Undeland, Robbins, 2003, *"Power Electronics"* , John Wiley & Sons, Inc, Third edition.

[3] *Rochie Ligaya Libby, "Switching Characteristics of SiC Schottky diodes in a Buck – DC converter"*, Power Electronics Laboratory, Electrical and Electronics Engineering Department

[4] Udo Steinebrunner *"Fast, faster, fastest! Optimized diodes for switching applications"* by, IXYS Semiconductor GmbH, Lampertheim .

[5] "Power Factor Correction" home.earthlink.net/~jimlux/hv/pfc.htm , home.earthlink.net/~jimlux/hv/pfc.htm , www.ambercaps.com/ lighting/power_factor_correction_concepts.htm

[6] Second Generation of CoolMOSTM Fastest High Voltage Switch, Application Note, V1.0, Aug. 2000

[7] B.K.Bose, 1992, "Modern *Power Electronics Evolution, Technology and Applications"*, Institute of Electrical and Electronics Engineers, Inc

[8] "CoolMOS"www.ixys.com/99099.pdf , ww.infineon.com/cgi/ecrm.dll/ecrm/scripts/prod_cat.jsp?oid=-8176 , www.microcontroller.ru/components/infineon/cool_mos.pdf

[9] Issa Batarseh, 2004, *"Power Electronic Circuits"*, John Wiley & Sons, Inc.

[10] "PSpice Libraries for CoolMOS Power Transistors" http://www.infineon.com/simulate.

[11] Muhammad H. Rashid, Ph.D., 1996, "Power *Electronics Laboratory Using SPICE*", Institute of Electrical and Electronics Engineers, Inc.

CHAPTER 7

APPENDIXES

APPENDIX 1

Gantt chart of the project for semester 1

No.	Detail/ Week	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
		26/1 – 30/1	2/2 – 4/2	9/2 – 13/2	16/2 – 20/2	23/2 – 27/2	1/3 – 5/3	8/3 – 12/3	15/3 – 19/3	22/3 – 26/3	29/3 – 2/4	5/4 - 9/4	12/4 – 16/4	19/4 – 23/4	26/4 – 30/4	3/5 - 7/5	10/5 – 14/5	17/5 – 21/5	24/5 – 28/5	31/5 – 4/6
1	**Selection of Project Topic**	■																		
	-Propose Topic																			
	-Finalized topic selection																			
2	**Preliminary Research Work**		■	■																
	-Introduction																			
	-Objective																			
	-List of references/literature																			
	-Project planning management																			
3	**Submission of Preliminary Report**			●																
4	**Project Work**				■	■	■	■												
	-Reference/Literature																			
	-Practical/Laboratory Work																			
5	**Submission of Progress Report**								●											
6	**Project work continue**								■	■	■	■								
	-Practical/Laboratory Work																			
	- Simulation																			
7	**Submission of Interim Report Final Draft**												●							
8	**Submission of Interim Report**														●					
9	**Oral Presentation**																			●

● Suggested milestone

■ Process

□ Done Process

APPENDIX 2

Gantt chart of the project for semester 2

No.	Detail/ Week	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
		26/7 – 30/7	2/8 – 6/8	9/8 – 13/8	16/8 – 20/8	23/8 – 27/8	30/8 – 3/9	13/9 – 17/9	20/9 – 24/9	27/9 – 1/10	4/10 - 8/10	11/10 – 15/10	18/10 – 22/10	25/10 – 29/10	1/11 - 5/11	8/11 – 12/11	15/11 – 19/11	22/11 – 27/11	29/11 – 3/12	6/12 – 24/12
1	**Project Work Continue**																			
	-Ordering components																			
2	**Submission of Progress Report 1**				●															
3	**Project Work Continue**																			
	-Work on PCB																			
4	**Submission of Progress Report 2**								●											
5	**Project work continue**																			
	-Practical/Laboratory Work																			
	- Simulation																			
6	**Submission of Draft Report**												●							
7	**Submission of Final Report (Soft Cover**														●					
8	**Submission of Technical Report**																●			
9	**Oral Presentation**																		●	
10	**Submission of Final Report (Hard Cover)**																			●

● Suggested milestone

Process

Done Process

APPENDIX 3

List of components use

List of components use in experiment:-

Electronic components:-

a) Pulse-width modulating controller,

b) Transistor switch (CoolMOS) – SPB07N60C3,

rated - VDS @ Tjmax = 650 V

- ID = 7.3 A

c) Inductor – 0.4μH , 2.5μH , 4.25μH

d) Capacitor – 10 ηF

e) Power diode – IDP06E60

rated - V_{RRM} = 600 V

- I_F = 6 A

f) Resistor – 2 Ω (± 5%), 10 Ω (± 5%)

APPENDIX 4

Data sheet of CoolMOS – SPB07N60C3

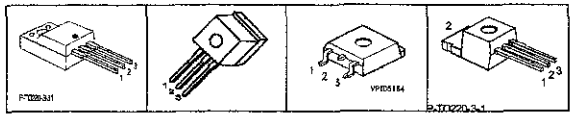
Cool MOS™ Power Transistor

V_{DS} @ T_{jmax}	650	V
$R_{DS(on)}$	0.6	Ω
I_D	7.3	A

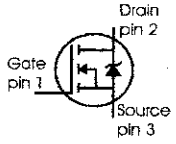
Feature

- New revolutionary high voltage technology
- Ultra low gate charge
- Periodic avalanche rated
- Extreme dv/dt rated
- High peak current capability
- Improved transconductance
- P-TO-220-3-31: Fully isolated package (2500 VAC; 1 minute)

P-TO220-3-31 P-TO262-3-1 P-TO263-3-2 P-TO220-3-1



Type	Package	Ordering Code	Marking
SPP07N60C3	P-TO220-3-1	Q67040-S4400	07N60C3
SPB07N60C3	P-TO263-3-2	Q67040-S4394	07N60C3
SPI07N60C3	P-TO262-3-1	Q67040-S4424	07N60C3
SPA07N60C3	P-TO220-3-31	Q67040-S4409	07N60C3



Maximum Ratings

Parameter	Symbol	Value		Unit
		SPP_B_I	SPA	
Continuous drain current	I_D			A
T_C = 25 °C		7.3	7.3[1)]	
T_C = 100 °C		4.6	4.6[1)]	
Pulsed drain current, t_p limited by T_{jmax}	$I_{D\ puls}$	21.9	21.9	A
Avalanche energy, single pulse	E_{AS}	230	230	mJ
I_D=5.5A, V_{DD}=50V				
Avalanche energy, repetitive t_{AR} limited by T_{jmax}[2)]	E_{AR}	0.5	0.5	
I_D=7.3A, V_{DD}=50V				
Avalanche current, repetitive t_{AR} limited by T_{jmax}	I_{AR}	7.3	7.3	A
Gate source voltage static	V_{GS}	±20	±20	V
Gate source voltage AC (f >1Hz)	V_{GS}	±30	±30	
Power dissipation, T_C = 25°C	P_{tot}	83	32	W
Operating and storage temperature	T_j, T_{stg}	-55...+150		°C

Infineon technologies

SPP07N60C3, SPB07N60C3
SPI07N60C3, SPA07N60C3

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain Source voltage slope	dv/dt	50	V/ns
V_{DS} = 480 V, I_D = 7.3 A, T_j = 125 °C			

Thermal Characteristics

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Thermal resistance, junction - case	R_{thJC}	-	-	1.5	K/W
Thermal resistance, junction - case, FullPAK	$R_{thJC\ FP}$	-	-	3.9	
Thermal resistance, junction - ambient, leaded	R_{thJA}	-	-	62	
Thermal resistance, junction - ambient, FullPAK	$R_{thJA\ FP}$	-	-	80	
SMD version, device on PCB:	R_{thJA}				
@ min. footprint		-	-	62	
@ 6 cm² cooling area [3)]		-	35	-	
Soldering temperature,	T_{sold}	-	-	260	°C
1.6 mm (0.063 in.) from case for 10s					

Electrical Characteristics, at T_j=25°C unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=0.25mA	600	-	-	V
Drain-Source avalanche breakdown voltage	$V_{(BR)DS}$	V_{GS}=0V, I_D=7.3A	-	700	-	
Gate threshold voltage	$V_{GS(th)}$	I_D=350µA, V_{GS}=V_{DS}	2.1	3	3.9	
Zero gate voltage drain current	I_{DSS}	V_{DS}=600V, V_{GS}=0V,				µA
		T_j=25°C	-	0.5	1	
		T_j=150°C	-	-	100	
Gate-source leakage current	I_{GSS}	V_{GS}=30V, V_{DS}=0V	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=4.6A				Ω
		T_j=25°C	-	0.54	0.6	
		T_j=150°C	-	1.46	-	
Gate input resistance	R_G	f=1MHz, open drain	-	0.8	-	

Electrical Characteristics, at T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Characteristics						
Transconductance	g_{fs}	$V_{DS}\geq 2*I_D*R_{DS(on)max}$, I_D=4.6A	-	6	-	S
Input capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V, f=1MHz	-	790	-	pF
Output capacitance	C_{oss}		-	260	-	
Reverse transfer capacitance	C_{rss}		-	16	-	
Effective output capacitance,[4] energy related	$C_{o(er)}$	V_{GS}=0V, V_{DS}=0V to 480V	-	30	-	
Effective output capacitance,[5] time related	$C_{o(tr)}$		-	55	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=380V, V_{GS}=0/13V, I_D=7.3A, R_G=12Ω, T_j=125°C	-	6	-	ns
Rise time	t_r		-	3.5	-	
Turn-off delay time	$t_{d(off)}$		-	60	100	
Fall time	t_f		-	7	15	
Gate Charge Characteristics						
Gate to source charge	Q_{gs}	V_{DD}=480V, I_D=7.3A	-	3	-	nC
Gate to drain charge	Q_{gd}		-	9.2	-	
Gate charge total	Q_g	V_{DD}=480V, I_D=7.3A, V_{GS}=0 to 10V	-	21	27	
Gate plateau voltage	$V_{(plateau)}$	V_{DD}=480V, I_D=7.3A	-	5.5	-	V

[1] Limited only by maximum temperature

[2] Repetitive avalanche causes additional power losses that can be calculated as $P_{AV}=E_{AR}*f$.

[3] Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical without blown air.

[4] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

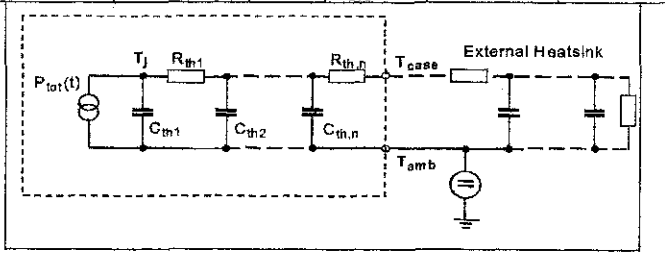
[5] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

Electrical Characteristics

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Inverse diode continuous forward current	I_S	T_C=25°C	-	-	7.3	A
Inverse diode direct current, pulsed	I_{SM}		-	-	21.9	
Inverse diode forward voltage	V_{SD}	V_{GS}=0V, $I_F=I_S$	-	1	1.2	V
Reverse recovery time	t_{rr}	V_R=480V, $I_F=I_S$, di_F/dt=100A/µs	-	400	600	ns
Reverse recovery charge	Q_{rr}		-	4	-	µC
Peak reverse recovery current	I_{rrm}		-	28	-	A
Peak rate of fall of reverse recovery current	di_{rr}/dt	T_j=25°C	-	800	-	A/µs

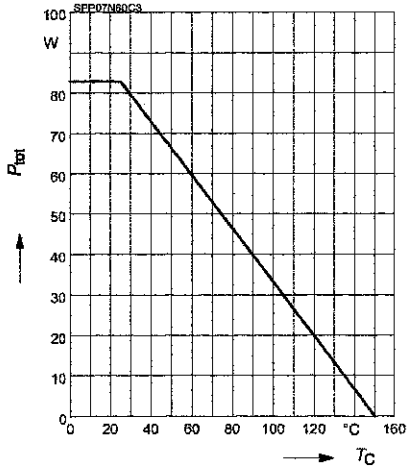
Typical Transient Thermal Characteristics

Symbol	Value		Unit	Symbol	Value		Unit
	SPP_B_I	SPA			SPP_B_I	SPA	
R_{th1}	0.024	0.024	K/W	C_{th1}	0.00012	0.00012	Ws/K
R_{th2}	0.046	0.046		C_{th2}	0.0004578	0.0004578	
R_{th3}	0.085	0.085		C_{th3}	0.000645	0.000645	
R_{th4}	0.308	0.195		C_{th4}	0.001867	0.001867	
R_{th5}	0.317	0.45		C_{th5}	0.004795	0.007558	
R_{th6}	0.112	2.511		C_{th6}	0.045	0.412	



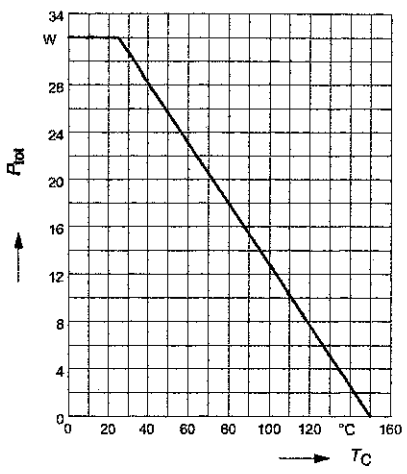
1 Power dissipation

$P_{tot} = f(T_C)$



2 Power dissipation FullPAK

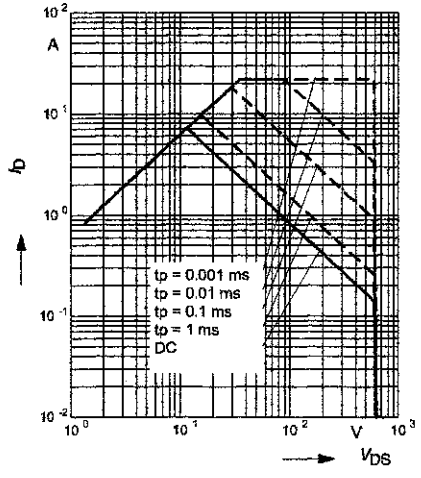
$P_{tot} = f(T_C)$



3 Safe operating area

$I_D = f(V_{DS})$

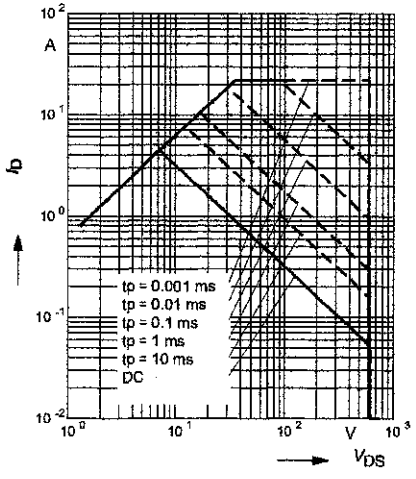
parameter : $D = 0$, T_C=25°C



4 Safe operating area FullPAK

$I_D = f(V_{DS})$

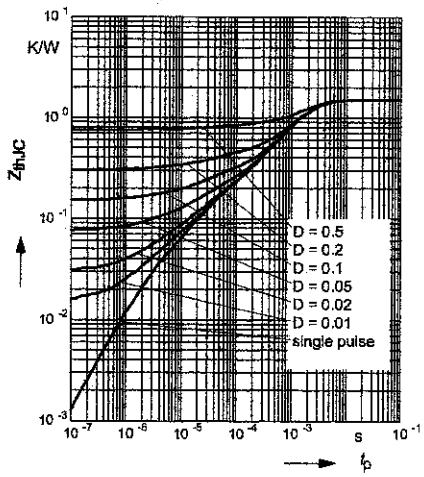
parameter: $D = 0$, T_C = 25°C



5 Transient thermal impedance

$Z_{thJC} = f(t_p)$

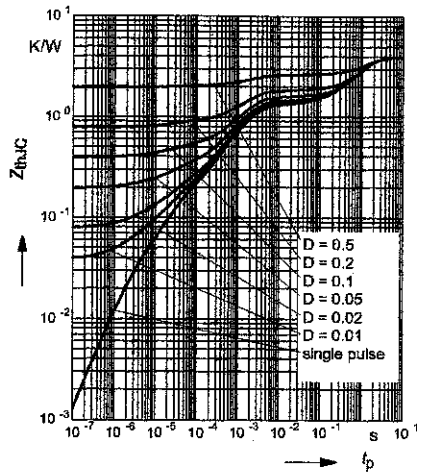
parameter: $D = t_p/T$



6 Transient thermal impedance FullPAK

$Z_{thJC} = f(t_p)$

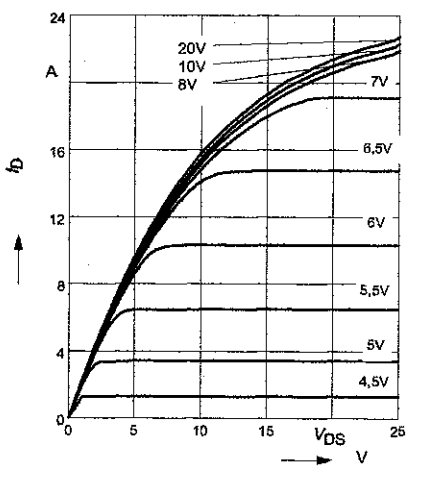
parameter: $D = t_p/t$



7 Typ. output characteristic

$I_D = f(V_{DS})$; T_j=25°C

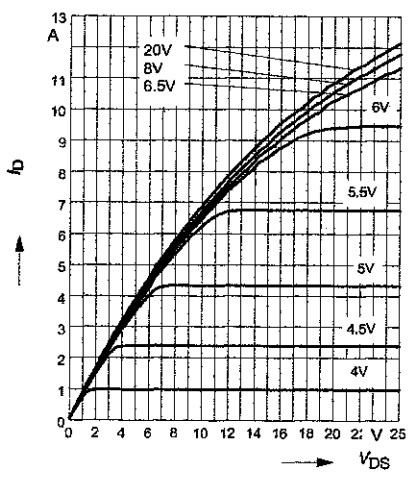
parameter: t_p = 10 µs, V_{GS}



8 Typ. output characteristic

$I_D = f(V_{DS})$; T_j=150°C

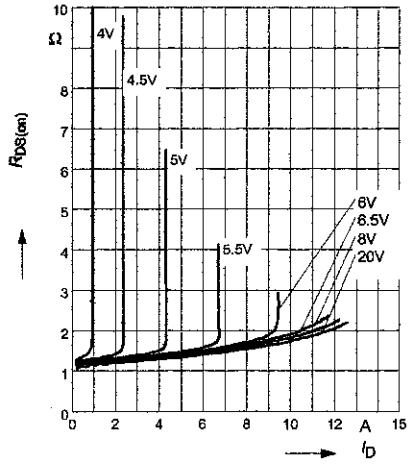
parameter: t_p = 10 µs, V_{GS}



9 Typ. drain-source on resistance

$R_{DS(on)}=f(I_D)$

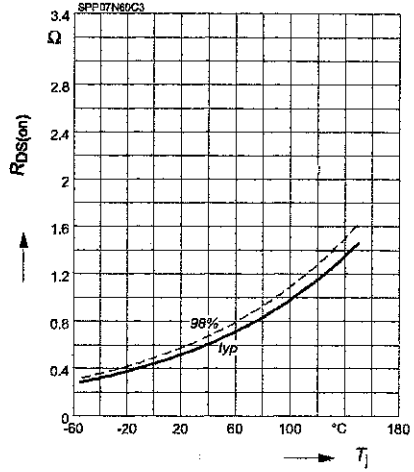
parameter: T_j=150°C, V_{GS}



10 Drain-source on-state resistance

$R_{DS(on)} = f(T_j)$

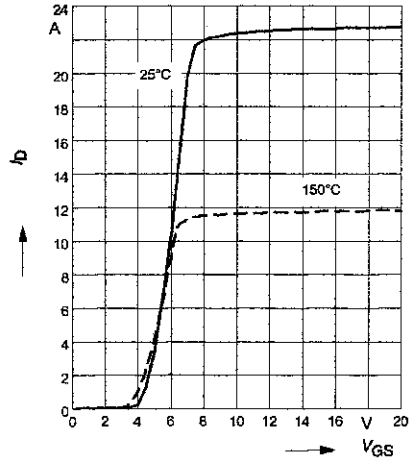
parameter : I_D = 4.6 A, V_{GS} = 10 V



11 Typ. transfer characteristics

$I_D= f(V_{GS})$; $V_{DS}\geq 2 \times I_D \times R_{DS(on)max}$

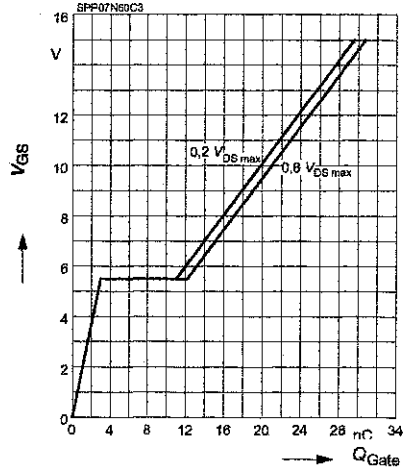
parameter: t_p = 10 µs



12 Typ. gate charge

$V_{GS} = f(Q_{Gate})$

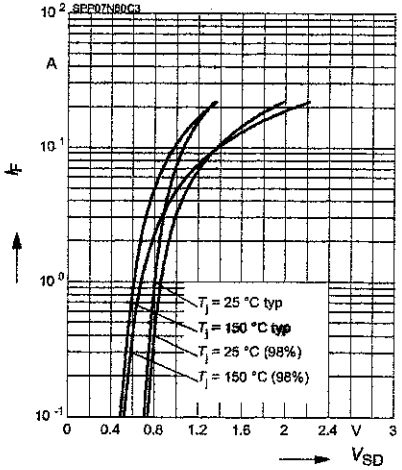
parameter: I_D = 7.3 A pulsed



13 Forward characteristics of body diode

$I_F = f(V_{SD})$

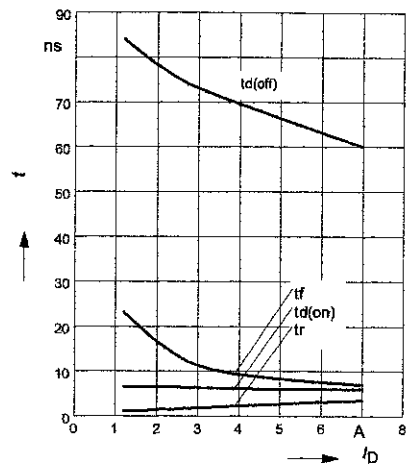
parameter: T_j , tp = 10 µs



14 Typ. switching time

$t = f(I_D)$, inductive load, T_j=125°C

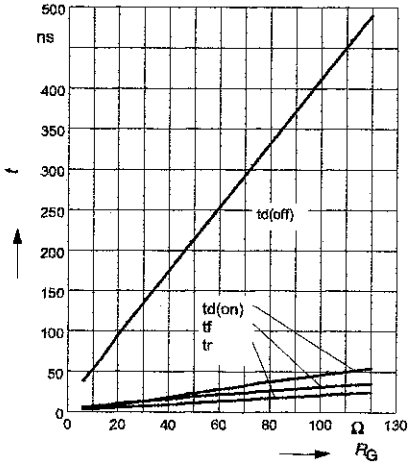
par.: V_{DS}=380V, V_{GS}=0/+13V, R_G=12Ω



15 Typ. switching time

$t = f(R_G)$, inductive load, T_j=125°C

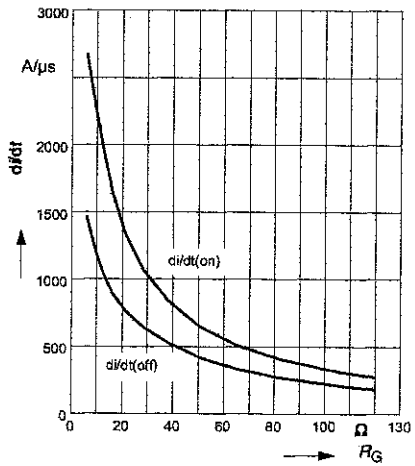
par.: V_{DS}=380V, V_{GS}=0/+13V, I_D=7.3 A



16 Typ. drain current slope

$di/dt = f(R_G)$, inductive load, T_j = 125°C

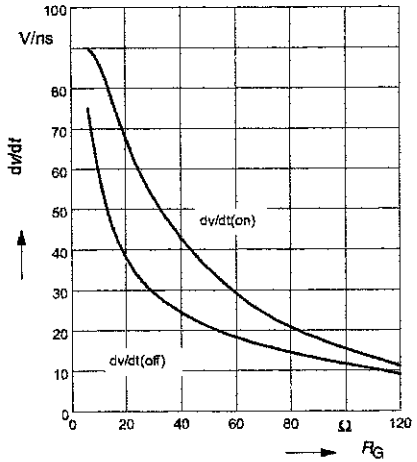
par.: V_{DS}=380V, V_{GS}=0/+13V, I_D=7.3A



17 Typ. drain source voltage slope

$dv/dt = f(R_G)$, inductive load, $T_j = 125°C$

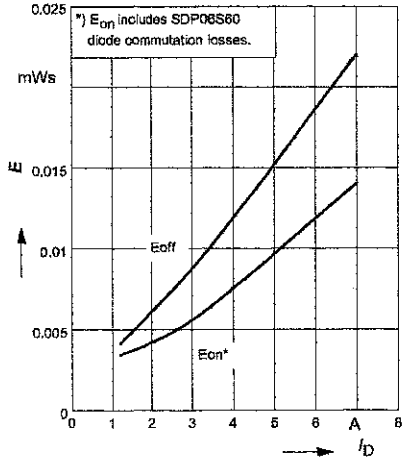
par.: V_{DS}=380V, V_{GS}=0/+13V, I_D=7.3A



18 Typ. switching losses

$E = f(I_D)$, inductive load, T_j=125°C

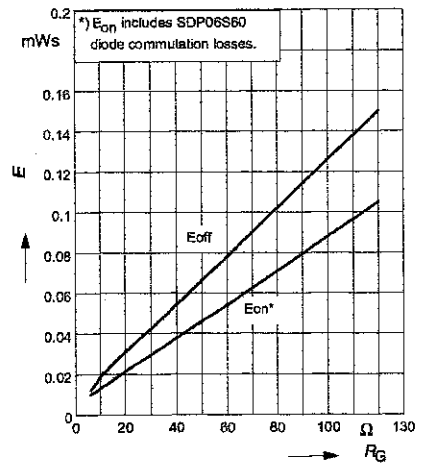
par.: V_{DS}=380V, V_{GS}=0/+13V, R_G=12Ω



19 Typ. switching losses

$E = f(R_G)$, inductive load, T_j=125°C

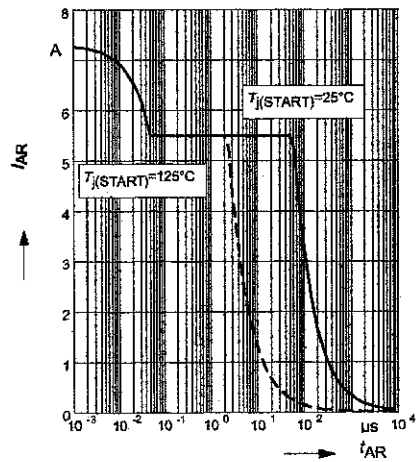
par.: V_{DS}=380V, V_{GS}=0/+13V, I_D=7.3A



20 Avalanche SOA

$I_{AR} = f(t_{AR})$

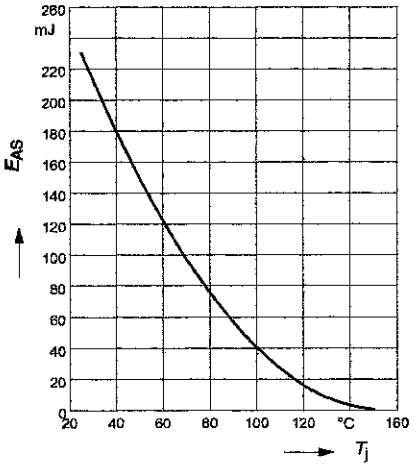
par.: $T_j \leq 150$ °C



21 Avalanche energy

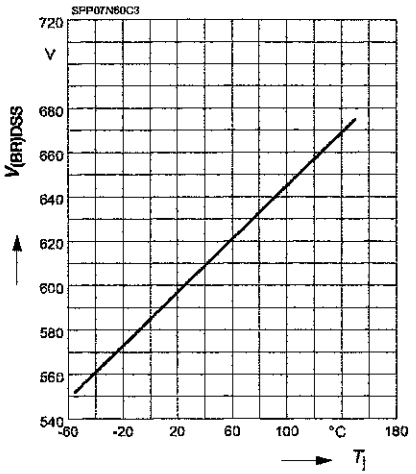
$E_{AS} = f(T_j)$

par.: I_D = 5.5 A, V_{DD} = 50 V



22 Drain-source breakdown voltage

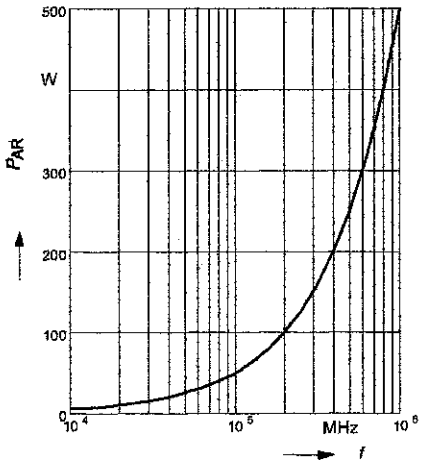
$V_{(BR)DSS} = f(T_j)$



23 Avalanche power losses

$P_{AR} = f(f)$

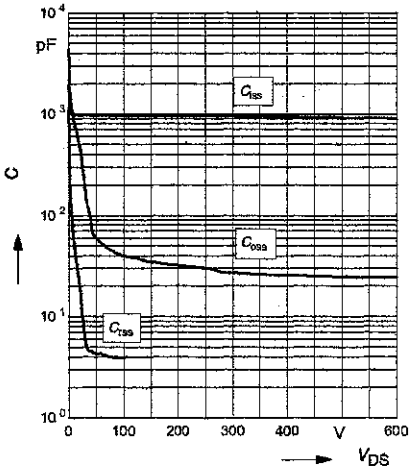
parameter: E_{AR}=0.5mJ



24 Typ. capacitances

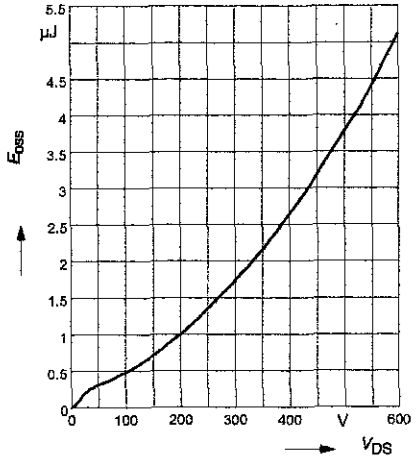
$C = f(V_{DS})$

parameter: V_{GS}=0V, f=1 MHz

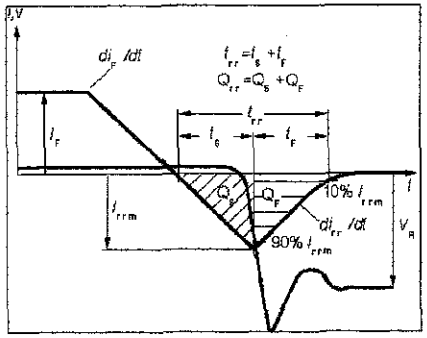


25 Typ. C_{oss} stored energy

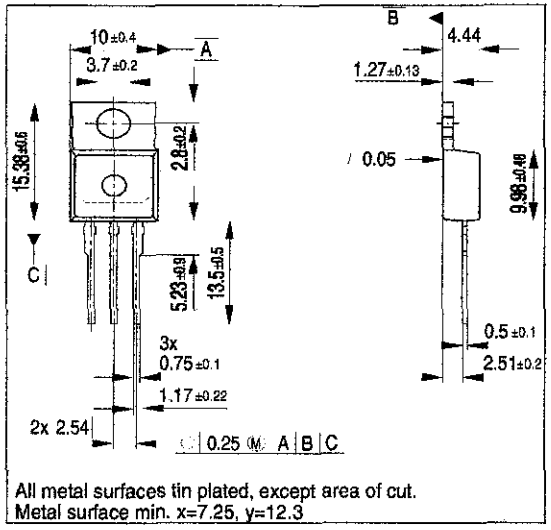
$E_{oss}=f(V_{DS})$



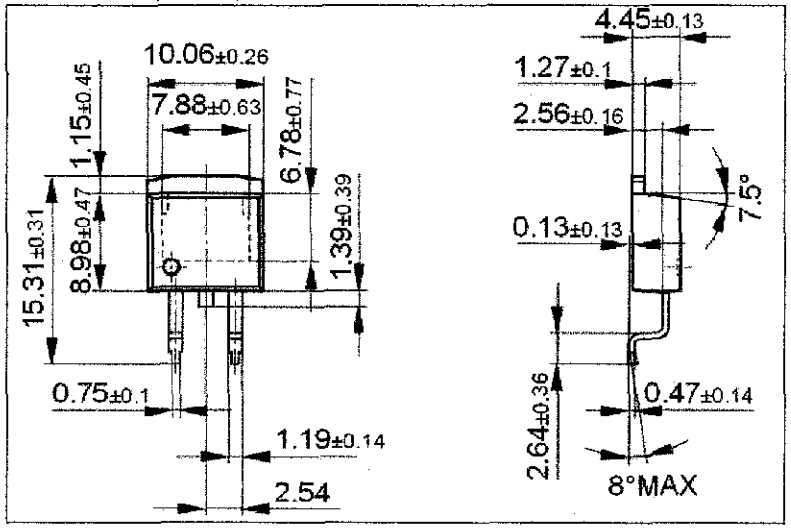
Definition of diodes switching characteristics



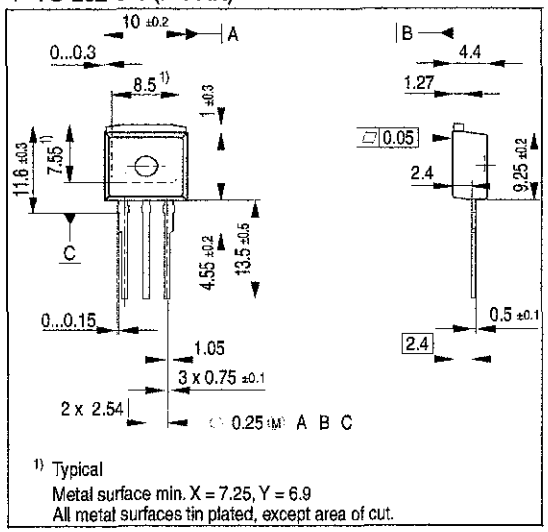
P-TO-220-3-1



P-TO-263-3-2 (D^2-PAK)

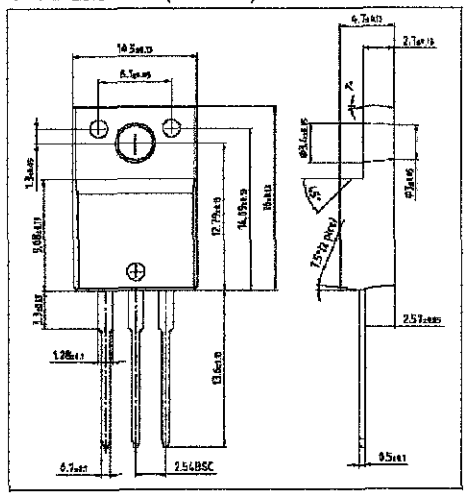


P-TO-262-3-1 (I^2-PAK)



1) Typical
Metal surface min. X = 7.25, Y = 6.9
All metal surfaces tin plated, except area of cut.

P-TO-220-3-31 (FullPAK)



Please refer to mounting instructions (application note AN-TO220-3-31-01)

Published by
Infineon Technologies AG,
Bereichs Kommunikation
St.-Martin-Strasse 53,
D-81541 München

Attention please!
The information herein is given to describe certain components and shall not be considered as warranted characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Infineon Technologies is an approved CECC manufacturer.

Information
For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Represnatives worldwide (see address list).

Warnings
Due to technical requirements components may contain dangerous substances.
For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

APPENDIX 5

Data sheet of Power Diode – IDP06E60

Fast Switching EmCon Diode

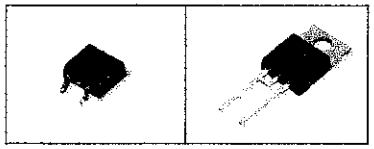
Feature

- 600 V EmCon technology
- Fast recovery
- Soft switching
- Low reverse recovery charge
- Low forward voltage
- 175°C operating temperature
- Easy paralleling

Product Summary

V_{RRM}	600	V
I_F	6	A
V_F	1.5	V
T_{jmax}	175	°C

P-TO220-3.SMD P-TO220-2-2.



Type	Package	Ordering Code	Marking	Pin 1	PIN 2	PIN 3
IDP06E60	P-TO220-2-2.	Q67040-S4480	D06E60	C	A	-
IDB06E60	P-TO220-3.SMD	Q67040-S4481	D06E60	NC	C	A

Maximum Ratings, at T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Value	Unit
Repetitive peak reverse voltage	V_{RRM}	600	V
Continous forward current	I_F		A
T_C=25°C		14.7	
T_C=90°C		10	
Surge non repetitive forward current T_C=25°C, t_p=10 ms, sine halfwave	I_{FSM}	29	
Maximum repetitive forward current T_C=25°C, t_p limited by T_{jmax}, D=0.5	I_{FRM}	22	
Power dissipation	P_{tot}		W
T_C=25°C		46.9	
T_C=90°C		26.6	
Operating and storage temperature	T_j, T_{stg}	-55...+175	°C
Soldering temperature 1.6mm(0.063 in.) from case for 10s	T_S	255	°C

Infineon technologies

IDP06E60
IDB06E60

Thermal Characteristics

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Characteristics					
Thermal resistance, junction - case	R_{thJC}	-	-	3.2	K/W
Thermal resistance, junction - ambient, leaded	R_{thJA}	-	-	62	
SMD version, device on PCB:	R_{thJA}				
@ min. footprint		-	-	62	
@ 6 cm² cooling area [1]		-	35	-	

Electrical Characteristics, at T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static Characteristics					
Reverse leakage current	I_R				µA
V_R=600V, T_j=25°C		-	-	50	
V_R=600V, T_j=150°C		-	-	500	
Forward voltage drop	V_F				V
I_F=6A, T_j=25°C		-	1.5	2	
I_F=6A, T_j=150°C		-	1.5	-	

[1] Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical without blown air.

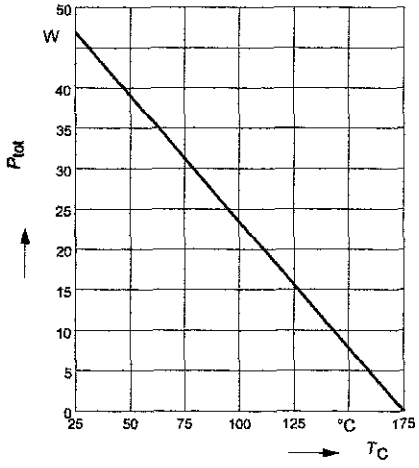
Electrical Characteristics, at T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Dynamic Characteristics					
Reverse recovery time	t_{rr}				ns
V_R=400V, I_F=6A, di/dt=550A/µs, T_j=25°C		-	70	-	
V_R=400V, I_F=6A, di/dt=550A/µs , T_j=125°C		-	100	-	
V_R=400V, I_F=6A, di/dt=550A/µs , T_j=150°C		-	105	-	
Peak reverse current	I_{rrm}				A
V_R=400V, I_F=6A, di/dt=550A/µs, T_j=25°C		-	6.5	-	
V_R=400V, I_F=6A, di/dt=550A/µs, T_j=125°C		-	7.4	-	
V_R=400V, I_F=6A, di/dt=550A/µs, T_j=150°C		-	7.9	-	
Reverse recovery charge	Q_{rr}				nC
V_R=400V, I_F=6A, di/dt=550A/µs, T_j=25°C		-	240	-	
V_R=400V, I_F=6A, di/dt=550A/µs, T_j=125°C		-	360	-	
V_R=400V, I_F=6A, di/dt=550A/µs, T_j=150°C		-	400	-	
Reverse recovery softness factor	S				
V_R=400V, I_F=6A, di_F/dt=550A/µs, T_j=25°C		-	4	-	
V_R=400V, I_F=6A, di_F/dt=550A/µs, T_j=125°C		-	4.8	-	
V_R=400V, I_F=6A, di_F/dt=550A/µs, T_j=150°C		-	4.9	-	

1 Power dissipation

$P_{tot} = f(T_C)$

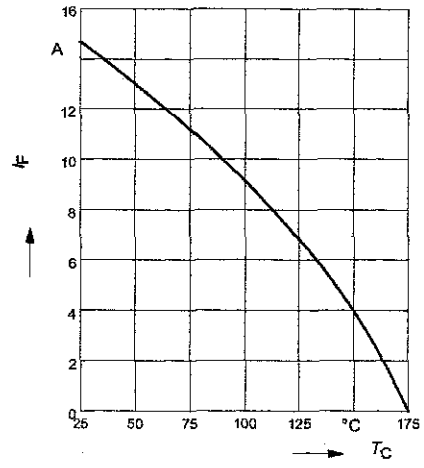
parameter: $T_j \leq 175$ °C



2 Diode forward current

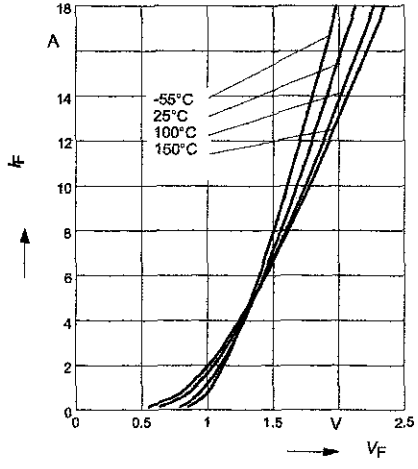
$I_F = f(T_C)$

parameter: $T_j \leq 175$°C



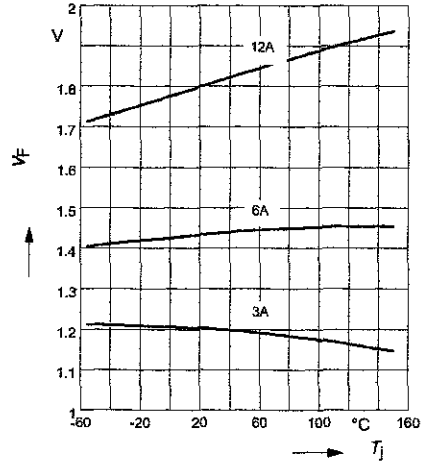
3 Typ. diode forward current

$I_F = f(V_F)$



4 Typ. diode forward voltage

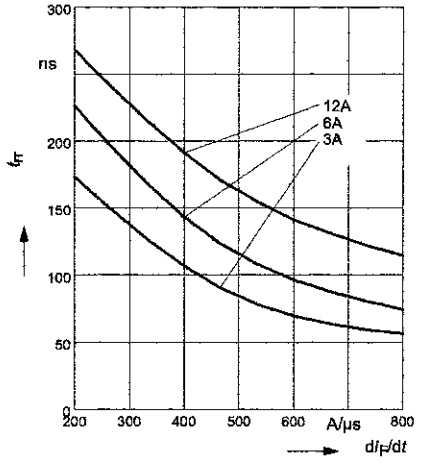
$V_F = f(T_j)$



5 Typ. reverse recovery time

$t_{rr} = f(di_F/dt)$

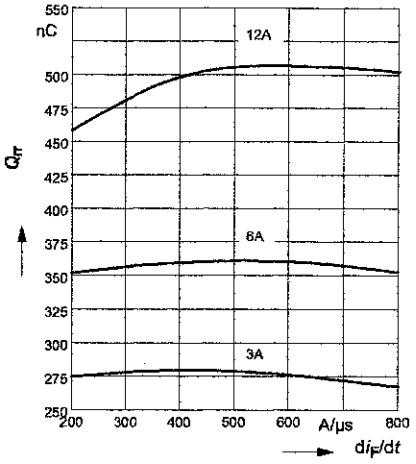
parameter: $V_R = 400V$, $T_j = 125°C$



6 Typ. reverse recovery charge

$Q_{rr} = f(di_F/dt)$

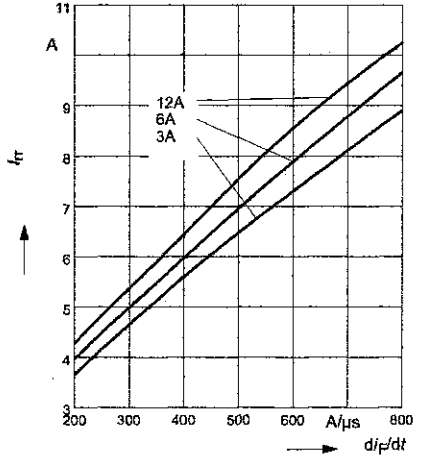
parameter: $V_R = 400V$, $T_j = 125\ °C$



7 Typ. reverse recovery current

$I_{rr} = f(di_F/dt)$

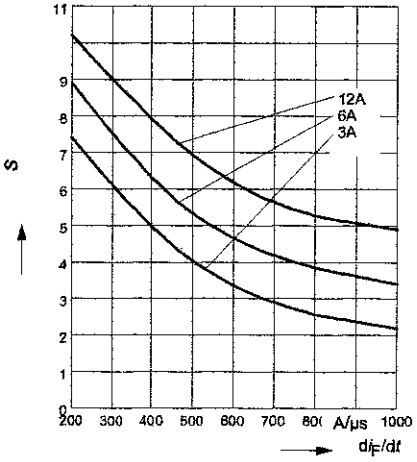
parameter: $V_R = 400V$, $T_j = 125°C$



8 Typ. reverse recovery softness factor

$S = f(di_F/dt)$

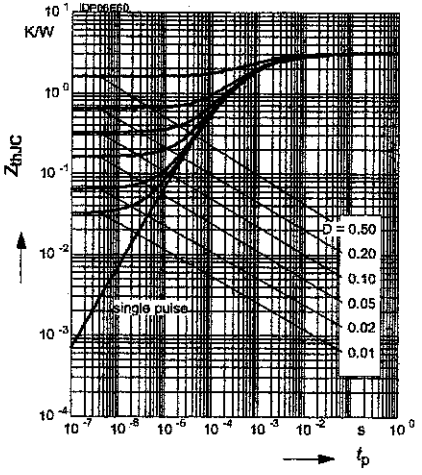
parameter: $V_R = 400V$, $T_j = 125°C$



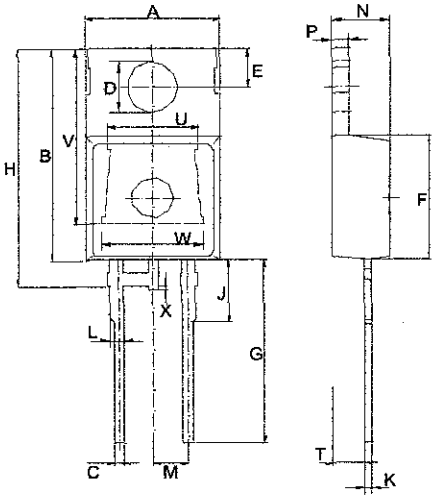
9 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

parameter : $D = t_p/T$

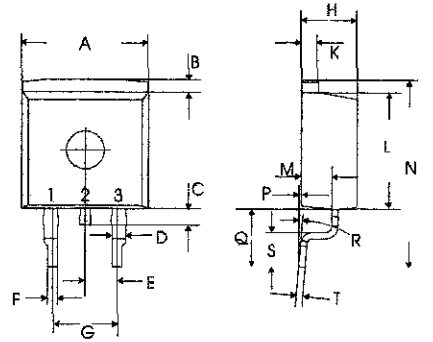


TO-220-2-2

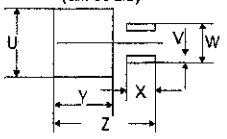


symbol	dimensions			
	[mm]		[inch]	
	min	max	min	max
A	9.70	10.10	0.3819	0.3976
B	15.30	15.90	0.6024	0.6260
C	0.65	0.85	0.0256	0.0335
D	3.55	3.85	0.1398	0.1516
E	2.60	3.00	0.1024	0.1181
F	9.00	9.40	0.3543	0.3701
G	13.00	14.00	0.5118	0.5512
H	17.20	17.80	0.6772	0.7008
J	4.40	4.80	0.1732	0.1890
K	0.40	0.60	0.0157	0.0236
L	1.05 typ.		0.41 typ.	
M	2.54 typ.		0.1 typ.	
N	4.4 typ.		0.173 typ.	
P	1.10	1.40	0.0433	0.0551
T	2.4 typ.		0.095 typ.	
U	6.6 typ.		0.26 typ.	
V	13.0 typ.		0.51 typ.	
W	7.5 typ.		0.295 typ.	
X	0.00	0.40	0.0000	0.0157

TO-220-3-45 (P-TO220SMD)



Footprint
(dif. scale)



symbol	dimensions			
	[mm]		[inch]	
	min	max	min	max
A	9.80	10.00	0.3858	0.3937
B	1.3 typ.		0.0512 typ.	
C	1.25	1.75	0.0492	0.0689
D	0.95	1.15	0.0374	0.0453
E	2.54 typ.		0.1 typ.	
F	0.72	0.85	0.0283	0.0335
G	5.08 typ.		0.2 typ.	
H	4.30	4.50	0.1693	0.1772
K	1.28	1.40	0.0504	0.0551
L	9.00	9.40	0.3543	0.3701
M	2.30	2.50	0.0906	0.0984
N	14.1 typ.		0.5551 typ.	
P	0.00	0.20	0.0000	0.0079
Q	3.30	3.90	0.1299	0.1535
R	8° max		8° max	
S	1.70	2.50	0.0669	0.0984
T	0.50	0.65	0.0197	0.0256
U	10.6 typ.		0.4252 typ.	
V	1.35 typ.		0.0532 typ.	
W	6.43 typ.		0.2532 typ.	
X	4.60 typ.		0.1811 typ.	
Y	9.40 typ.		0.3701 typ.	
Z	16.15 typ.		0.6358 typ.	

Published by
Infineon Technologies AG,
Bereichs Kommunikation
St.-Martin-Strasse 53,
D-81541 München

Attention please!
The information herein is given to describe certain components and shall not be considered as warranted characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Infineon Technologies is an approved CECC manufacturer.

Information
For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Represatives worldwide (see address list).

Warnings
Due to technical requirements components may contain dangerous substances.
For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

APPENDIX 6

Summary of results

SUMMARY OF RESULTS

Characteristics	p.f = 0.998	p.f = 0.930	p.f = 0.830
Peak Reverse Recovery Current (mA)	-35.821	-31.981	-21.162
Diode Turn-off (nJ)	14.4	16.9	18.2
CoolMOS Turn-on loss (nJ)	56.75	67	67.75

Table: Summary of Simulation results

Characteristics	p.f = 0.998	p.f = 0.930	p.f = 0.830
Peak Reverse Recovery Current (mA)	-35.821	-31.981	-21.162
Diode Turn-off (nJ)	15.3	15.8	20.1
CoolMOS Turn-on loss (nJ)	53.7	62.8	65.9

Table: Summary of Experimentation results