DESIGN COMMON MODE LOGIC (CML) FREQUENCY DIVIDER IN CMOS PORCESS TECHNOLOGY

By

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Dissertation submitted in Partial Fulfillment of
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CERTIFICATION OF APPROVAL

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Approved:

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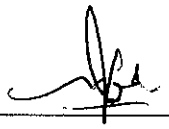
TRONOH, PERAK

June 2009

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.



Mastura binti Omar

ABSTRACT

The objective of this project is to design current mode logic (CML) frequency divider in CMOS technology. The current spikes that occur during transition between tacking and latch mode in transistor will degrade the performance of the frequency divider. The parasitic capacitances that exist in two transistor of tracking circuit directly contribute to the latch delay. The fundamental of this project is to understand the basic operation of CML of D Flip-flop based frequency divider. The new circuit which known as modified frequency divider is designed in order to overcome the current spike that occur during the transition between track and latch mode hence to reduce the rise time and fall time at the output. The modified frequency divider is able to reduce 20% up until 57.14% of the current spike that occurs during the transition between the track and latch mode. It also managed to reduce 11.76% up until 53.85% of the rise time and fall time at the output voltage hence reduce the latch delay.

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CHAPTER 1

INTRODUCTION

1.1 Background of Study

Background of Study of this project is divided by two PARTS. The first one is Introduction of Frequency Synthesizer and followed by Frequency Divider.

1.1.1 Introduction of Frequency Synthesizer

A frequency synthesizer is an electronic system that generates any range of frequencies from a single fixed timebase or oscillator [1]. It generates the frequencies that are exact multiply of a reference frequency. To synthesize new frequencies, the oscillator frequency can be added, subtracted, divided or multiplied [2].

There are three types of frequency synthesizers. There are direct analog synthesizer, direct digital synthesizer and phase locked looped (PLL) synthesizer. Direct analog synthesizer use four processes which are added, subtracted, divided and multiplied to synthesize new frequencies. Direct digital synthesizers synthesize waveforms and producing a number representing the phase of the synthesized signal of each reference period. Then it will convert each number to an analog output [2]. In this report, it will be more focus on PLL synthesizer.

The PLL synthesizer works by multiplying the reference frequency with a variable number. It is being done by dividing the output frequency by a variable number for adjusting the output frequency. After being divided the output frequency must be equal to the reference frequency [2].

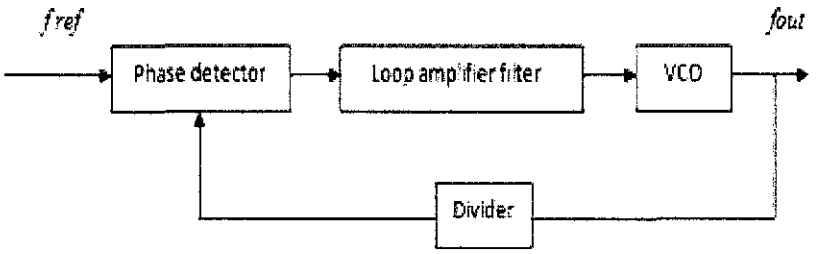

Figure 1: Basic PLL synthesizer

In Figure 1, the PLL synthesizer divides the frequency from Voltage Control Oscillator (VCO). VCO is an electronic oscillator design to be controlled in oscillation frequency by a voltage input and it convert back the voltage to frequency. PLL also control VCO so that the divided frequency is phase synchronized to a references frequency [2]. Most PLLs also include a divider between the oscillator and the feedback input to the phase detector to synthesize the frequency [3]. From here, the function of frequency divider in PLL is to synthesize the frequency by dividing the output frequency by variable number and will adjust the output frequency so that it is equal the reference frequency after division.

In digital wireless communication systems such as Global System for Mobile communications (GSM), Code Division Multiple Access (CDMA), PLL's are used to provide the Local Oscillator (LO) for up-conversion during transmission and down-conversion during reception. In most handphone, this function has been largely integrated into a single integrated circuit to reduce the cost and size of the handphone [3].

1.1.2 Frequency Divider

The frequency divider is an important part of PLL synthesizer. There are three popular types of frequency divider. They are injection-locked frequency dividers, regenerative frequency dividers and flip-flop-based frequency dividers. Flip-flop based frequency divider is digital frequency divider.

Flip-flop based frequency divider consist of two D latches in cascade and in negative feedback configuration at PLL [4]. The architecture is mainly a master-slave D flip-flop as shown in Figure 2.

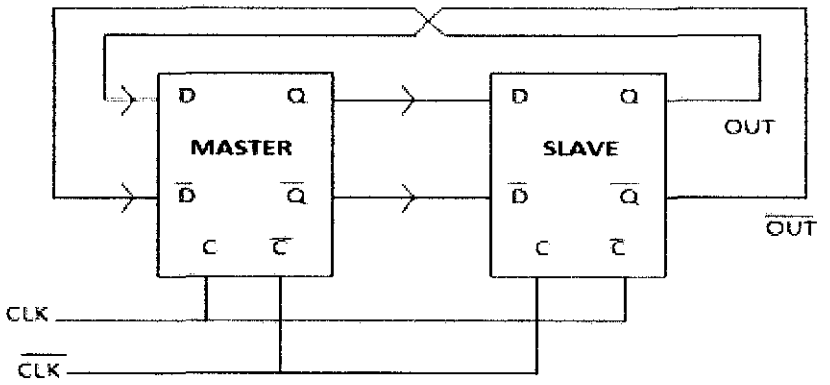

Figure 2: D flip flop master slave block diagram

The basic operation of master slave DFF is straightforward. The inverted output ($\overline{Q}$) is fed back to the input (D). The same clock is used to drive both level triggered DFF with opposite logic. The first DFF is called the master DFF while the second one is known as the slave DFF. Both of DD cannot be activated in the same time. Each positive input clock cycle is loaded into the DFF. On the next cycle, inverted output again is fed back to the input, which causes the output to toggle. The same event repeats for every two input clock cycle. Thus, output frequency is half of the input frequency and this is where the frequency division is achieved [5].

At transistor level, the flip-flop based frequency dividers are design using Current Mode Logic (CML) circuits. High speed based frequency dividers are normally implemented using CML. CML is a non-saturation, constant current, reduce swing logic that makes it enable to operate at high frequencies [6]. CML was first implemented using bipolar transistors and extended for application with MOS transistors. MOS current mode logic (MCML) circuits with constant bias currents are intended for accurate high-speed mixed signal application [7].

CML static frequency dividers are widely used in multi-gigahertz PLLs to divide the high frequency signal generated by the VCO into a signal with frequency lower enough to be handled by the following programmable frequency dividers implemented in CMOS logic.

CML circuit works by continuously toggling the output state after every clock cycle. This mechanism effectively causes the output to toggle between one and zero at a rate half that of the input clock and hence frequency division is achieved. A high-speed latch automatically results in a high-speed frequency divider [4]. From the previous findings, the high-speed latches are designed using current-mode logic (CML) circuits. Figure 3 shows the conventional CML latch topology.

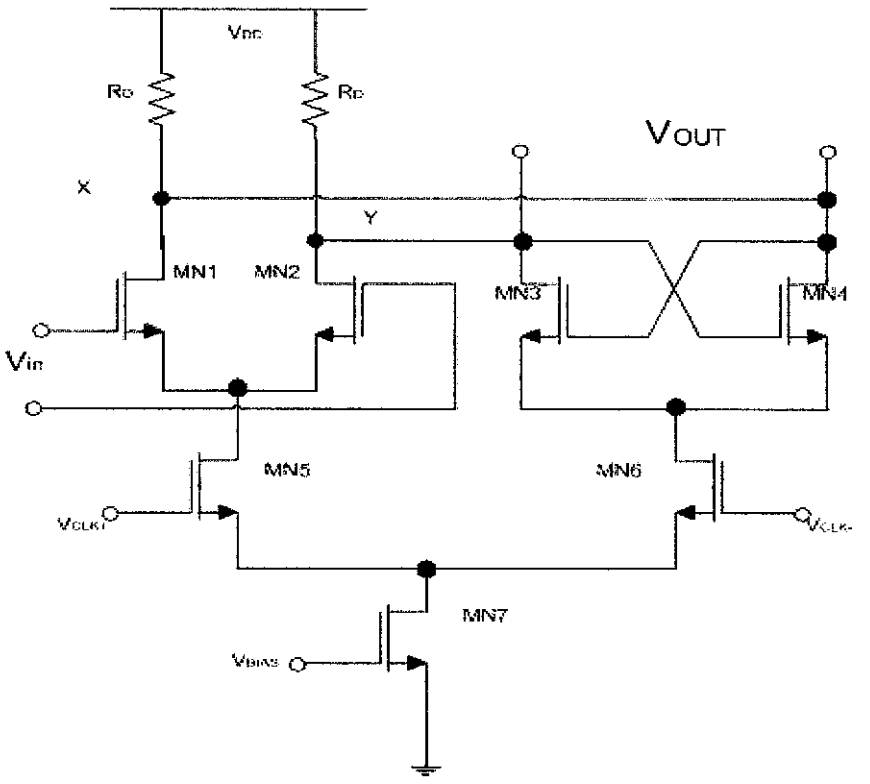

Figure 3: Conventional latch circuit

V_{in} actually represents the D and the $\overline{D}$ of DFF at the block diagram. While X represents the output Q and Y represents the inverter output $\overline{Q}$. V_{CLK+} and V_{CLK-} represent the clock.

The track and latch modes are determined by the clock signal input to a second differential pair, MN5 and MN6 [4]. When the signal V_{CLK} is "HIGH", the circuit operates in the tracking mode, where the tail current from MN7 flows entirely to the tracking circuit, MN1 and MN2, thereby allowing V_{OUT} to track V_{in} [4]. In the latch-mode, the signal V_{CLK} is held low and the tracking stage is disabled, whereas the latch pair is enabled storing the logic state at the output [4].

The basic CML static frequency divider is a divide by two cells. We need to cascade two CML circuit to realize the flip-flop based frequency dividers divide by two. As shown earlier by master slave DFF block diagram, the first CML will become the master and the second CML will become the slave.

1.2 Problem Statement

The conventional latch designs suffer from the current spikes due to a single tail current used for both tracking and latch circuits. The spike current happen because the transition between tracking and latch circuit happen very fast.These current spikes occur during the transition between tracking mode and latching mode. At ultra high-speed data-rates, the parasitic capacitances that exist in two transistor of tracking circuit will directly contribute to the latch delay and it also degrade the required minimum small-signal gain for a proper tracking operation [2]. All these effects will minimize the performance of the frequency divider.

1.3 Objective and Scope of Study

The objective of this project is to design CML frequency divider in CMOS technology based on D flip-flop circuit architecture to overcome the spike current problem during the transition between tracking mode and latching mode and also have smaller rise and fall time at the tracking mode. In this design, it will emphasize on the novel latch circuit which is shown in Figure 4.

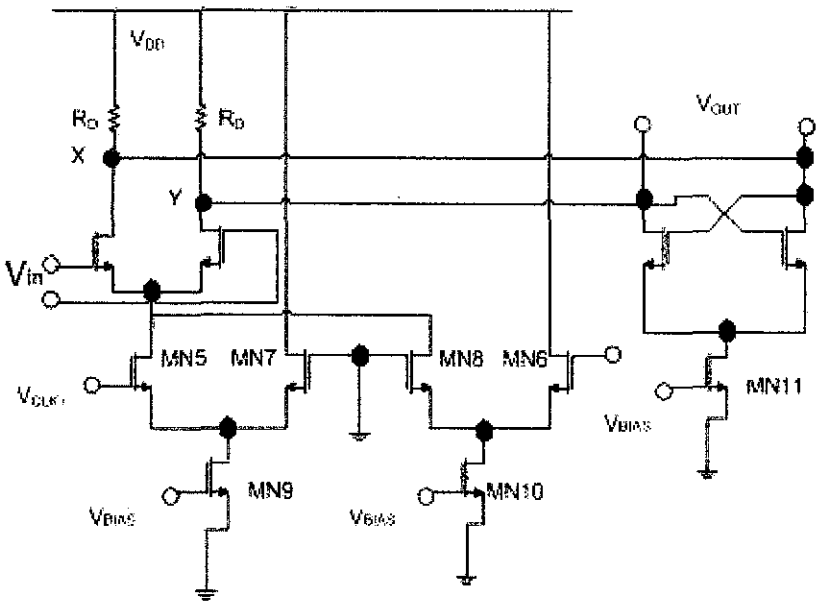

Figure 4: Novel latch circuit

The latch and tracking circuit use two distinct tails currents [4]. More details on this circuit operations will be discuss in Chapter 3. In order to achieve this objective, it is vital to understand the basic operation of frequency divider based on D flip-flop novel latch circuit architecture.

CHAPTER 2
LITERATURE REVIEW

2.1 Types of Frequency Divider

Based on Literature Review done, there are three popular types of frequency divider. There are Injection-locked frequency dividers, Regenerative Frequency Dividers and Flip-Flop-Based Frequency Dividers.

2.1.1 Injection-Locked Frequency Dividers

Injection-locked frequency dividers employ an oscillator whose centre frequency is locked to a harmonic of the incoming signal frequency. The input signal is injected through a voltage node of the oscillator. While achieving low-power operation, injection-locked frequency dividers exhibit a narrow lock-range [4].

2.1.2 Regenerative Frequency Dividers

Regenerative frequency dividers are realized by placing a mixer and a low-pass filter in a closed-loop feedback. A regenerative frequency divider exhibits a wider lock range at very high frequencies compared to an injection-locked counterpart, but utilizes many passive components in the process. Since frequency dividers are everywhere in modern high-speed systems, the excessive use of passive components is a disadvantage from overall chip-area and circuit matching considerations [4].

2.1.3 Flip-Flop-Based Frequency Dividers

The flip-flop-based frequency dividers are consists of two D latches in cascade, and in a negative feedback configuration. The digital operation of this type of dividers provides the advantage of suppressing the sensitivity to waveform distortions. Furthermore, the flip-flop-based dividers will achieve a wide bandwidth than other types of frequency dividers at low-to-medium range of frequencies. This approach also makes the signal levels compatible with the rest of the CML circuit blocks. High-speed flip-flop based frequency dividers are typically implemented using the current-mode-logic (CML) latches. Large frequency ranges (GHz) are not therefore uncommon in flip-flop-based frequency dividers that used CML logic style. However, a major disadvantage associated with conventional frequency dividers using CML style stems from the large load capacitances seen by the circuit blocks, which limit the maximum frequency of operation and fan-out capabilities [4].

2.2 Classification of Frequency Dividers

For this project, the Flip-Flop-Based Frequency Divider was chosen. The Flip-Flop-Based Frequency Dividers can be classified into two. There are asynchronous frequency divider and synchronous frequency divider.

2.2.1 Synchronous Frequency Divider

In synchronous dividers, all the flip-flops evaluate their respective states on the same clock edge. Synchronous dividers are inherently faster since changes in state occur almost simultaneously on the same clock edge but the division ratio is relatively low [8].

2.2.2 Asynchronous Frequency Divider

In asynchronous dividers, the clock signal triggers the first flip-flop and the output of the first flip-flop triggers the second flip-flop the change flows or ripples down the flip-flop chain. Asynchronous dividers also provide higher division ratios but they are slower because the changes from one flip-flop to the next do not arrive until the previous one has settled. Other than that, the output of the asynchronous dividers is not synchronized with the input clock signal and may contribute to the overall phase-noise [8].

2.3 Sizing the Transistors of the Frequency Divider

The size or Width over Length (W/L) ratio of the transistors play important role in determining the performance of frequency divider. In the frequency divider, there are three different circuits; there are the latch circuit, the track circuit and also full- rate clock. In sizing the transistor for the latch circuit, the track circuit and also full- rate clock have effect towards the performance of frequency divider.

2.3.1 Sizing the latch transistor

The cross-coupled transistor plays an important role in determining whether the divider structure will self oscillate. To increase the high speed operations of the divider, optimization is usually focused on reducing the size of these transistors. As the size is reduced, the circuit's poles move closer to the imaginary axis from the right half-plane [9].

2.3.2 Sizing the full-rate clock transistor

At high frequencies, it is important to maximise the energy coupled to the common source node for given external signal. So both sizing and biasing of the clock transistor are very important. As the size of full-rate clock transistor increased, the maximum voltage will decrease hence it will decrease the self oscillating frequency [9].

2.3.3 Sizing the track transistor size

The track transistor size has less effect on the other two parameters than the sizes of the other transistor [9].

CHAPTER 3

METHODOLOGY

3.1 Procedure Identification and Time Diagram for the project

Figure 5 below shows the procedure identification throughout this project.

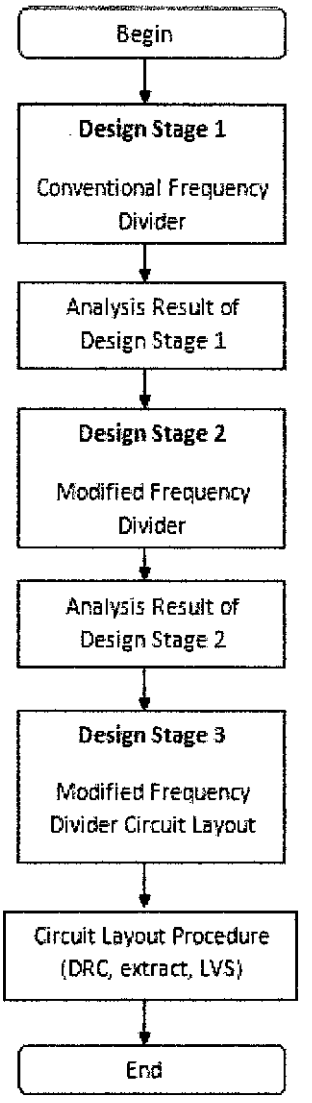

Figure 5: Procedure identification flow chart

Table 1 below shows the time diagram for this project.

Table 1: Time diagram for the project

Detail/Month	Aug	Sept	Oct	Nov	Dec	Jan	Feb	Mac	Apr
Design Stage One: Conventional Frequency Divider									
Analysis result Design Stage One									
Design Stage Two : Modified Frequency Divider									
Analysis result Design Stage Two									
Design Stage Three : Frequency Divider									
Analysis result Design Stage Two									

3.2 Design Stage 1: Conventional Frequency Divider

In the Design Stage One, first we need to design a conventional CML latch. Designing the conventional CML latch is a vital to make sure the flip flop based frequency divider is working. The conventional CML latch in Figure 3 is at the transistor level of the D flip flop while in Figure 6, it is at the logic gate level.

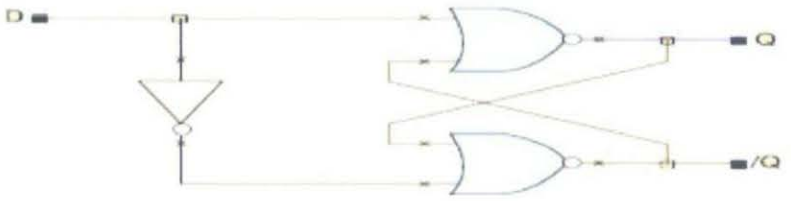

Figure 6: D Flip flop at logic level

The conventional CML latch is designed using Cadence Spectre IC design software. The design of conventional CML latch is very important because it is the crucial part of frequency divider. If this design part is not working well, it will affect the entire flip flop based frequency divider.

We need to cascade two conventional CML latch circuit to realize the flip-flop based frequency dividers. Figure 7 in the next page shows the two cascaded CML circuit in order to achieve conventional frequency divider.

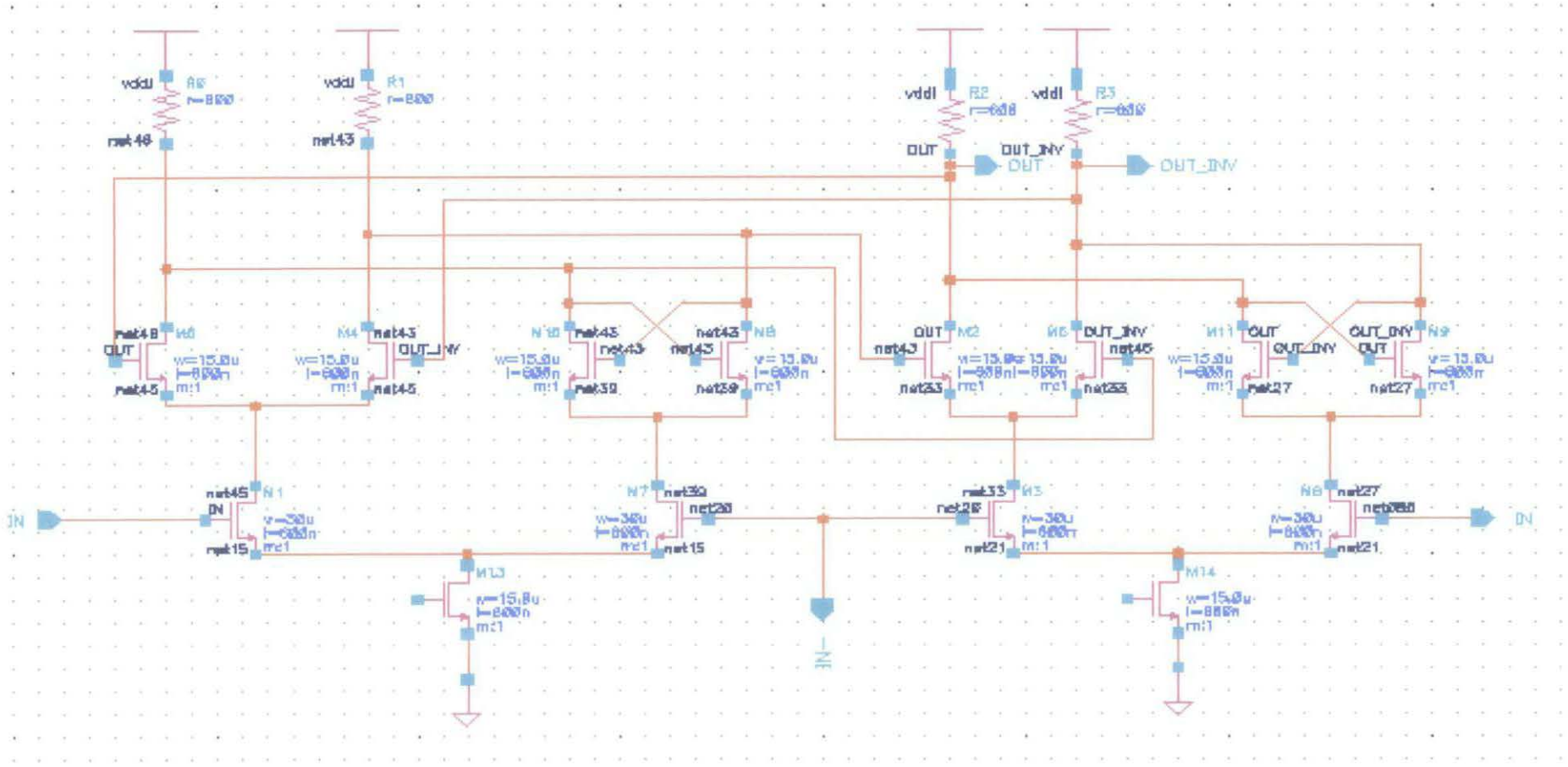

Figure 7: Conventional Frequency Divider

3.3 Design Stage Two: Modified Frequency Divider

To encounter the problems stated earlier, the modified frequency divider is designed so that the latch circuit and the tracking circuit will use two distinct tail currents as shown in Figure 8.

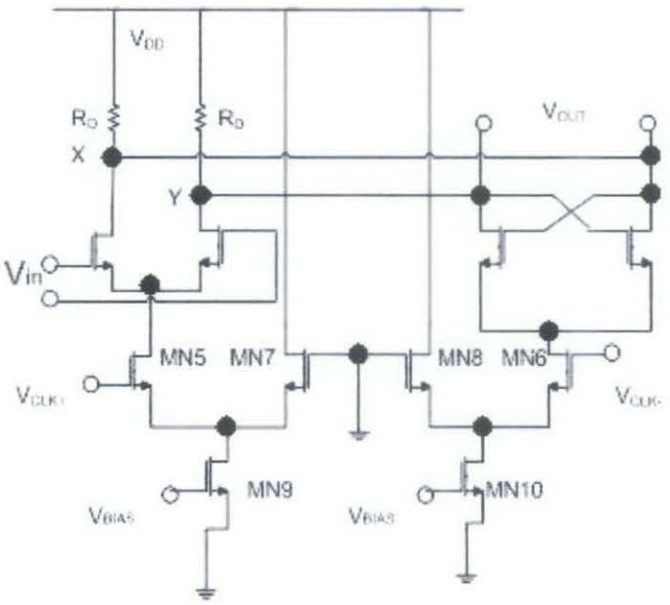

Figure 8: Modified CML Latch Circuit

There is another problem that causes a speed limitation on the proposed circuit as well as the conventional circuit. During each transition from the tracking mode (when V_{CLK} is "HIGH") to the latching mode (when V_{CLK} is "LOW"), the current tail of the cross-coupled pair (MN3 and MN4) must first recharge the capacitances of the cross-coupled pair as it starts drawing current from the output nodes, *X* and *Y*, and changing the logic state.

As for an alternative to the proposed circuit in Figure 8 is modified again so that the cross coupled pair having their own tail current. From that configuration, the latch cross-coupled pair always draws current from the nodes *X*, *Y* and there is no need for the charge to be built up during the latching phase. The new configuration known as Novel Latch circuit is shown in Figure 9.

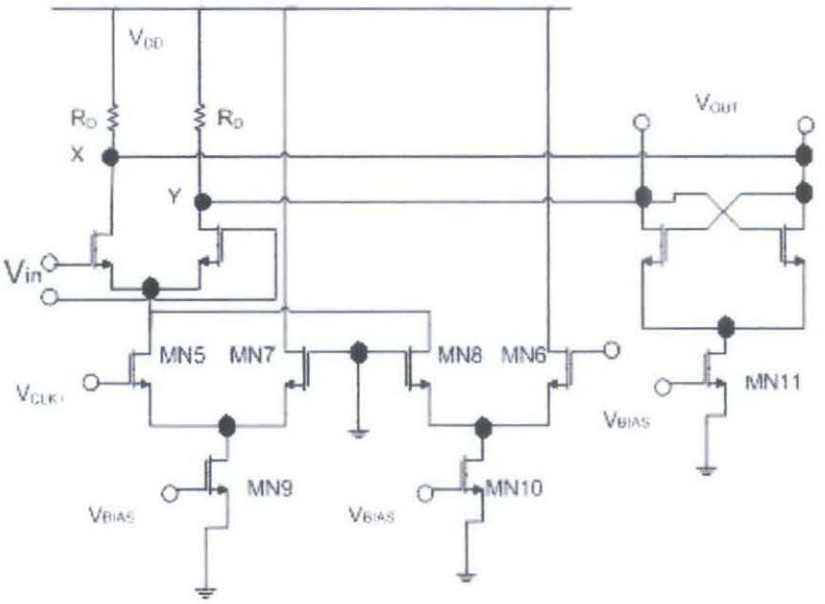

Figure 9: Novel Latch Circuit

To realize the flip-flop based frequency dividers we need to cascade two Novel CML latch circuit. Figure 10 in the next page shows the two cascade Novel CML circuit in order to implement the modified frequency divider.

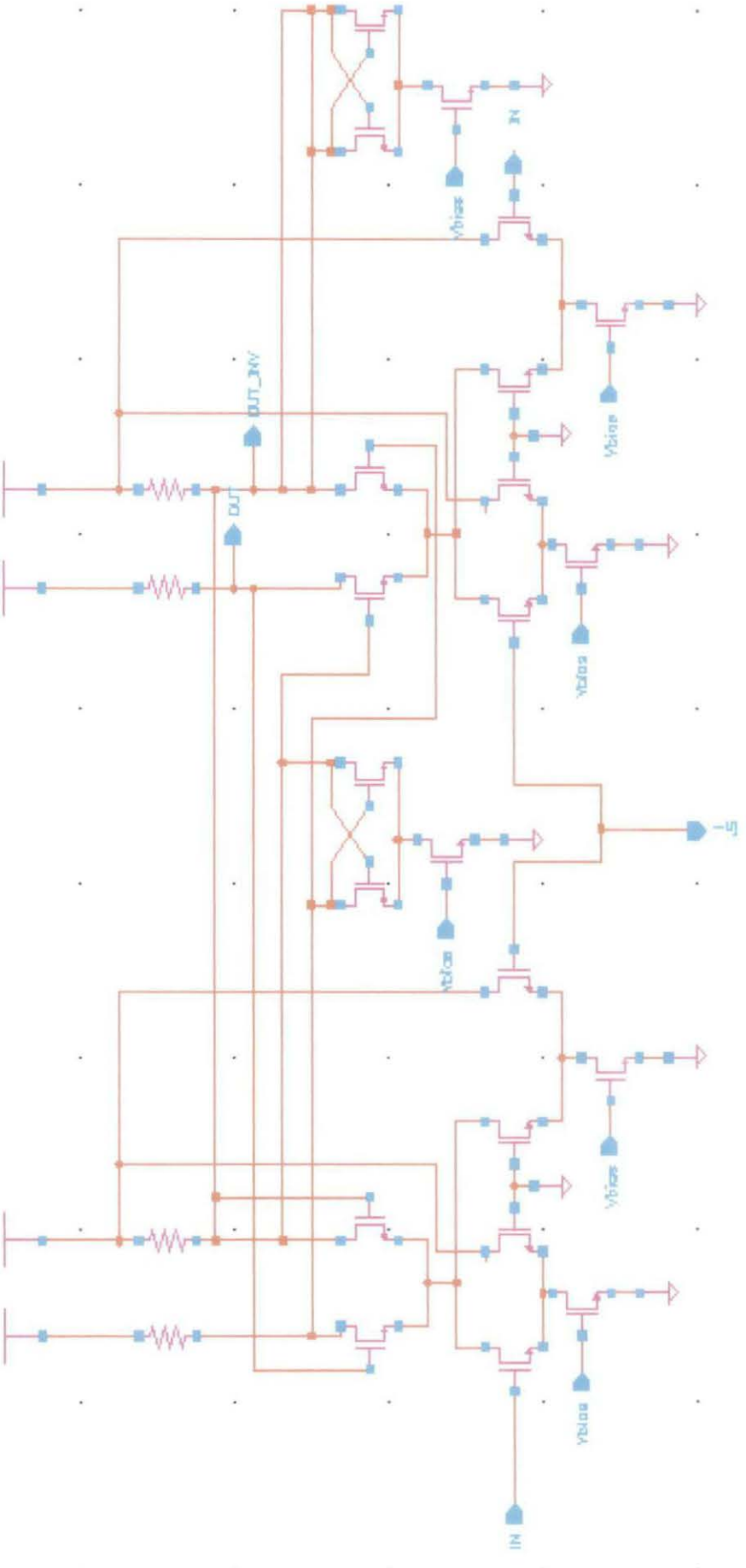

Figure 10: Modified Frequency Divider

3.4 Designing Parameter

Based on the literature review done, it can be said that the size of transistors play an important role towards the performance of frequency divider.

The conventional CML Latch and Combined Master Slave CML Latch are using design using Technology AMI06 or 0.6μm technology.

Since the value of length L is fixed because of the technology, we only can control the value of width W. The latch transistor size is determined according as follows;

$$\frac{W}{L} = \frac{15um}{0.6um} = 25$$

The full-rate clock transistor is determined according to as follows ratio;

$$\frac{W}{L} = \frac{30um}{0.6um} = 50$$

While for the track transistor size has less effect on the other two parameters than the sizes of the other transistor but it is designed to have the same size with the latch transistor.

V_{dd} is set to 3V and R_L is set to 600 Ω. While for V_{bias}, the value is set to 1.2V.

The frequency, f used for the flip flop based frequency divider is 500MHz. From here we can calculate the time, by referring the equation as follows.

$$f = \frac{1}{T}$$

Using the frequency value and the relationship of the frequency, f, the period T

$$500MHz = \frac{1}{T}; T = 2\text{ns}.$$

From here, we can calculate the rise time T_r and T_f fall time parameter that used in clock and data setting.

$$T_r = T \times 0.05$$

$$T_f = T \times 0.05$$

$$T_r = 2ns \times 0.05;\ T_r = 0.1ns$$

$$T_f = 2ns \times 0.05;\ T_f = 0.1ns$$

The properties of V_{in+} and V_{in-} are as shown in Table 1.

Table 2: Properties of V_{in+} and V_{in-}

PARAMETER	V_{in+}	V_{in-}
Voltage 1	2V	0V
Voltage 2	0V	2V
Rise Time	0.1ns	0.1ns
Fall time	0.1ns	0.1ns
Pulse Width	1ns	1ns
Pulse period	2ns	2ns

3.5 Design Stage Three: Modified Frequency Divider Layout.

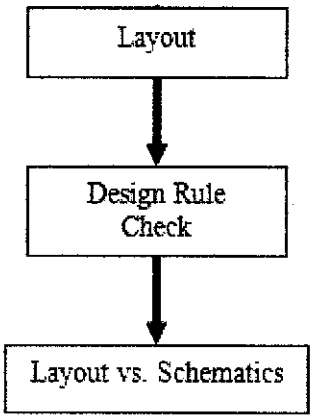

Figure 11: Layout Flow

In case we need to fabricate the modified frequency divider circuit, then the circuit must be layout. After completing the design and the simulation using Cadence Spectre Circuit Simulator, the circuit layout is carried out. Virtuoso Layout Editor is use to draw the layout of the modified frequency divider. The layout drawing of the circuit must be e verified by Design Rule Check (DRC). This is to ensure that the layout satisfied the rules such as Minimum Width Rules Minimum Space Rules Minimum Extension Rules and Overlap Rules. If the layout violates the rules, the error will appear. After that, the layout drawing must be compared to schematic through Layout Versus Schematic (LVS), since the schematic has been fully verified through the simulation process. Any inconsistency will lead to modifications on the layout, but sometimes, minor changes on the schematic were made as long as it does not alter any physical change. The layout drawing of modified frequency divider, verification of it by DRC and LVS will discuss in Chapter 4.

CHAPTER 4

RESULT AND DISCUSSION

4.1 The tail current of the transistor in the latch circuit

In this section, the simulation results of the tail current for both circuits are shown and discussed to see their performance.

4.1.1 The simulation results of the tail current

Figure 12 shows the simulation result of the tail current using the conventional frequency divider circuit at the frequency of 500 MHz. The conventional frequency divider exhibits about 0.7mA current spike. The simulation time is taken from 0 to 15ns.

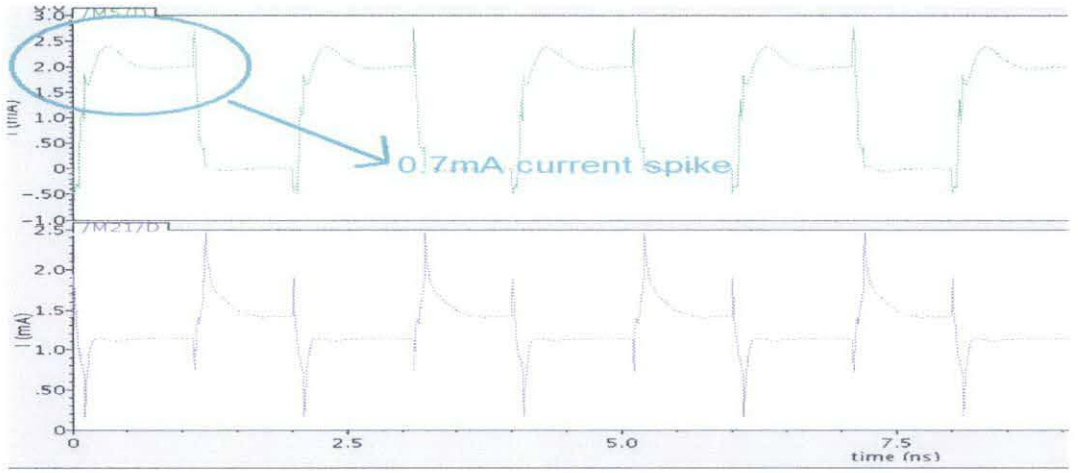

Figure 12: Tail currents of the conventional frequency divider.

Figure 13 shows the simulation result of at the tail current using the modified frequency divider. The two circuits are simulated at the frequency of 500 MHz to compare the performance. It is observed that the modified frequency divider exhibits about 0.3 mA current spike.

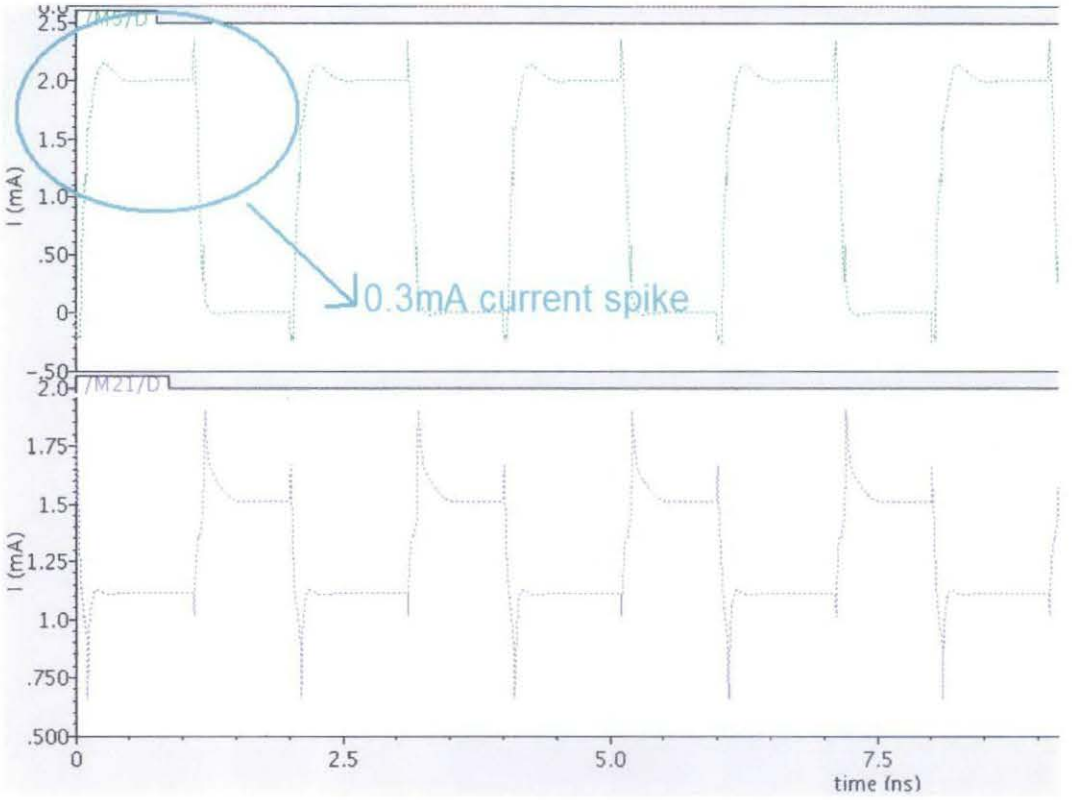

Figure 13: Tail currents of the modified frequency divider

4.1.2 Discussion of the simulation results of the tail current

Based on the simulation result of the tail current from the conventional frequency divider, it had been proved that earlier in the problem statement saying that conventional latch designs suffer from the current spikes due to single tail current used for both tracking and latch circuits.

From the simulation result, the spike current had been reduced in the modified frequency divider. The value of spike current of the modified frequency divider is 0.3 mA in comparison to the spike current from the conventional frequency divider which is 0.7 mA. Table 2 below shows the summary of the spike current for the conventional frequency divider and the modified frequency divider in the various frequency ranges from 500 MHz to until 2.5 GHz.

Table 3: Summary of spike current

Frequency, f (Hz)	Conventional frequency divider spike current, I (A)	Modified frequency divider spike current, I (A)	Percentage of reduce (%)
500M	0.7m	0.30m	57.14
750M	1.0m	0.50m	50.00
1G	1.3m	0.75m	42.30
2G	2.0m	1.60m	20.00
2.5G	7.5m	4.00m	46.67

The simulation results for the frequency other than 500MHz can be viewed on Appendix A. It can be concluded that the modified frequency divider had manage to reduce the spike current from 20 % to 57.14 %.

Although the main intention to design modified frequency divider is to overcome or eliminate the spike current that occurs during the transition from latch to track mode but due to the technology limitation attach might be the reason why we the spike current cannot eliminate the tail current to zero.

4.2 The output voltage of the frequency divider.

In this section, the simulation results of the output voltage for both circuits are shown and discussed to see their performance.

4.2.1 The simulation results of the output voltage

Figure 14 shows the simulation result of the output voltage using the conventional frequency divider taken with input frequency 500 MHz. It can be observed that there is a large ringing or oscillations at the output voltage. The rise and fall time for the conventional frequency divider is 3.9 ns.

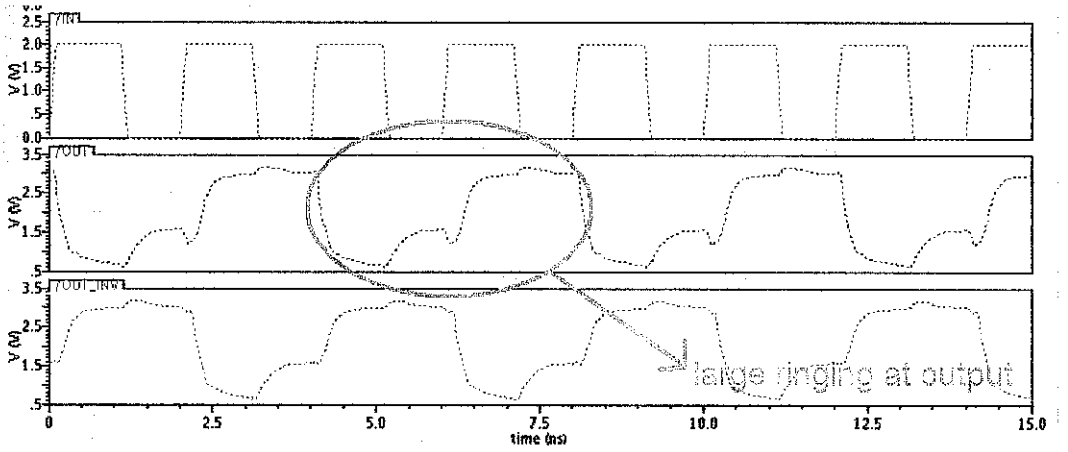

Figure 14: Output voltage of the conventional frequency divider.

Figure 15 shows the simulation result of the output voltage using the modified frequency divider circuit. To make the comparison sounds accurate, the result also taken at the frequency of 500MHz. It can be observed that the large ringing or oscillations that occurred on the conventional frequency divider much smaller in the modified frequency divider. The rise and fall time for the conventional frequency divider is 1.80 ns.

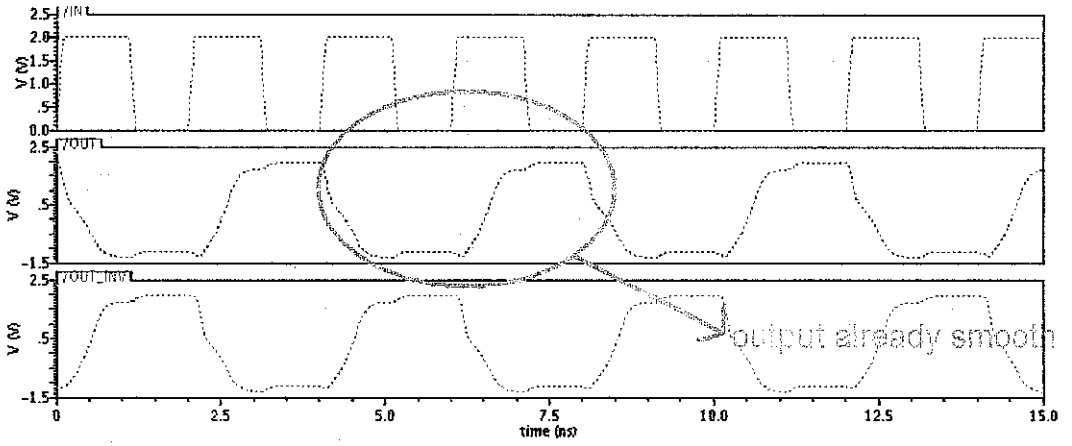

Figure 15: Output voltage of the modified frequency divider

4.2.2 Discussion of the simulation results of the output voltage of frequency divider

Based on the simulation of the output voltage using the conventional frequency divider, it can be observed that there is a large ringing output voltage which can lead to the operation failure of the frequency divider. At ultra high-speed data-rates, the parasitic capacitances that exist in two transistor of tracking circuit directly contribute to the latch delay. When the transistors are turned off, the current through parasitic inductance cannot drop to zero instantly and so it generates a large ringing at the output voltage. The large ringing output voltage also will cause failure to the operation of frequency divider [4].

From the simulation result, the rise and fall time at the output voltage had been reduced in the modified frequency divider. The value of the rise and fall time of the modified frequency divider is 1.80 ns in comparison to the conventional frequency divider which is 3.9 ns. Table 3 shows the summary of the spike current for the conventional frequency divider and the modified frequency divider in the various frequency ranges from 500 MHz until 2.5 GHz.

Table 4: Summary of rise and fall time

Frequency,*f* (Hz)	Conventional Frequency Divider rise and fall time, T (ns)	Modified Frequency Divider rise and fall time, T (ns)	Percentage of reduce (%)
500M	3.9	1.80	53.85
750M	2.5	2.00	20.00
1G	1.7	1.50	11.76
2G	0.8	0.40	50.00
2.5G	0.5	0.25	50.00

The simulation results of the output voltage for the frequency other than 500MHz can be viewed on Appendix B

Finally, it can be concluded that the modified frequency divider manage to reduce the fall time and rise time from 11.76 % to 53.85 %. The modified frequency divider had managed to reduce the fall time and rise time at the output voltage hence reduce the latch delay.

4.3 The input and output frequency divider.

To calculate the input and output frequency of the frequency divider, we can simply use the below formula;

$$f = \frac{1}{T}$$

f represent the frequency , while t represent the period of one complete cycle . For the input, the period of one complete cycle is 2 ns.

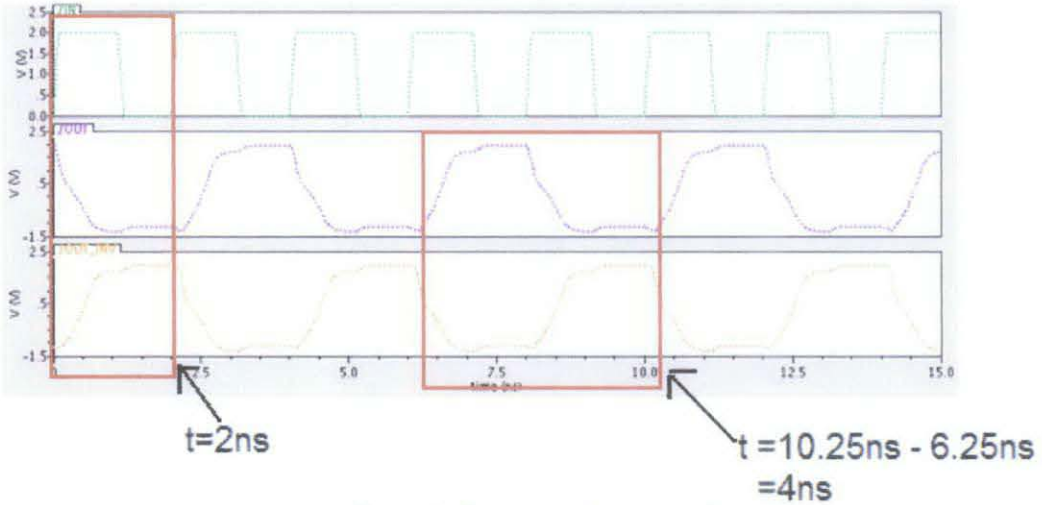

Figure 16: Period of input and output frequency

Hence the input frequency is 500 MHz. While for the output, the period of one complete cycle is 4 ns, therefore the output frequency is 250 MHz.

For this project, the frequency divider design is to divide by two. As shown in the previous page, the frequency divider managed to divide by two. There is another way to check whether the frequency divider manage to divide by two without calculating.

Since the output frequency must be half of the input frequency, the input period should twice the output period. This is shown in Figure 17

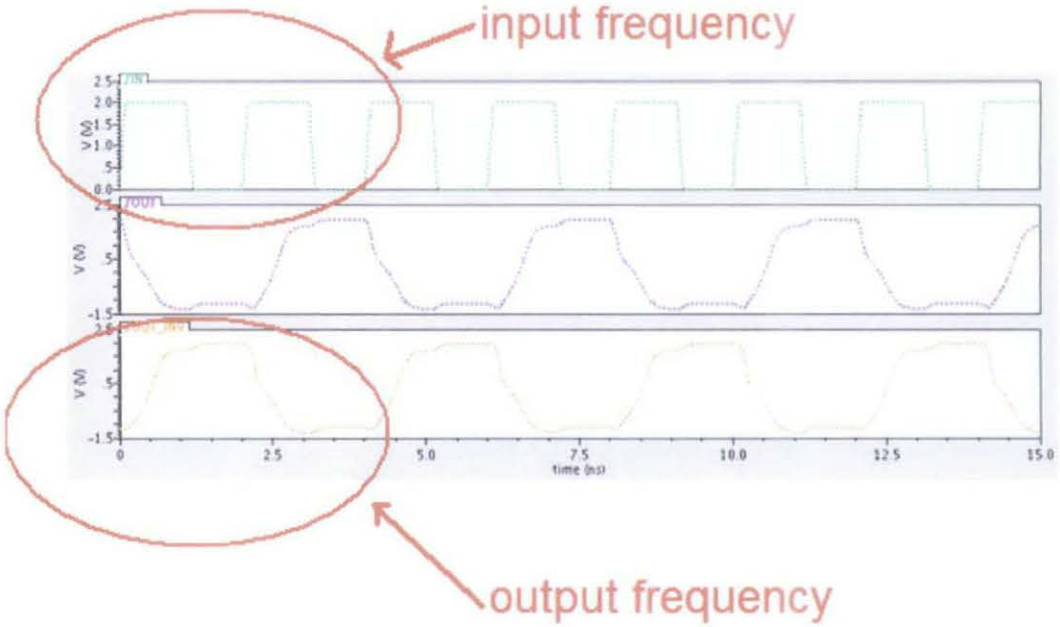

Figure 17: Input period should twice the output period

4.4 Layout of Modified Frequency Divider

The modified frequency divider has greater performance compare to the conventional frequency divider. This is shown throughout the simulation result that has been discussed earlier in this chapter. After succeed with simulation result, next we move on with the layout drawing of modified frequency divider. Since the frequency divider is obtained by combining two CML latches, we must draw the first latch. This is to ensure that if the first CML latch having problem, we can troubleshoot it. Figure 17 below shows the layout drawing of CML latch.

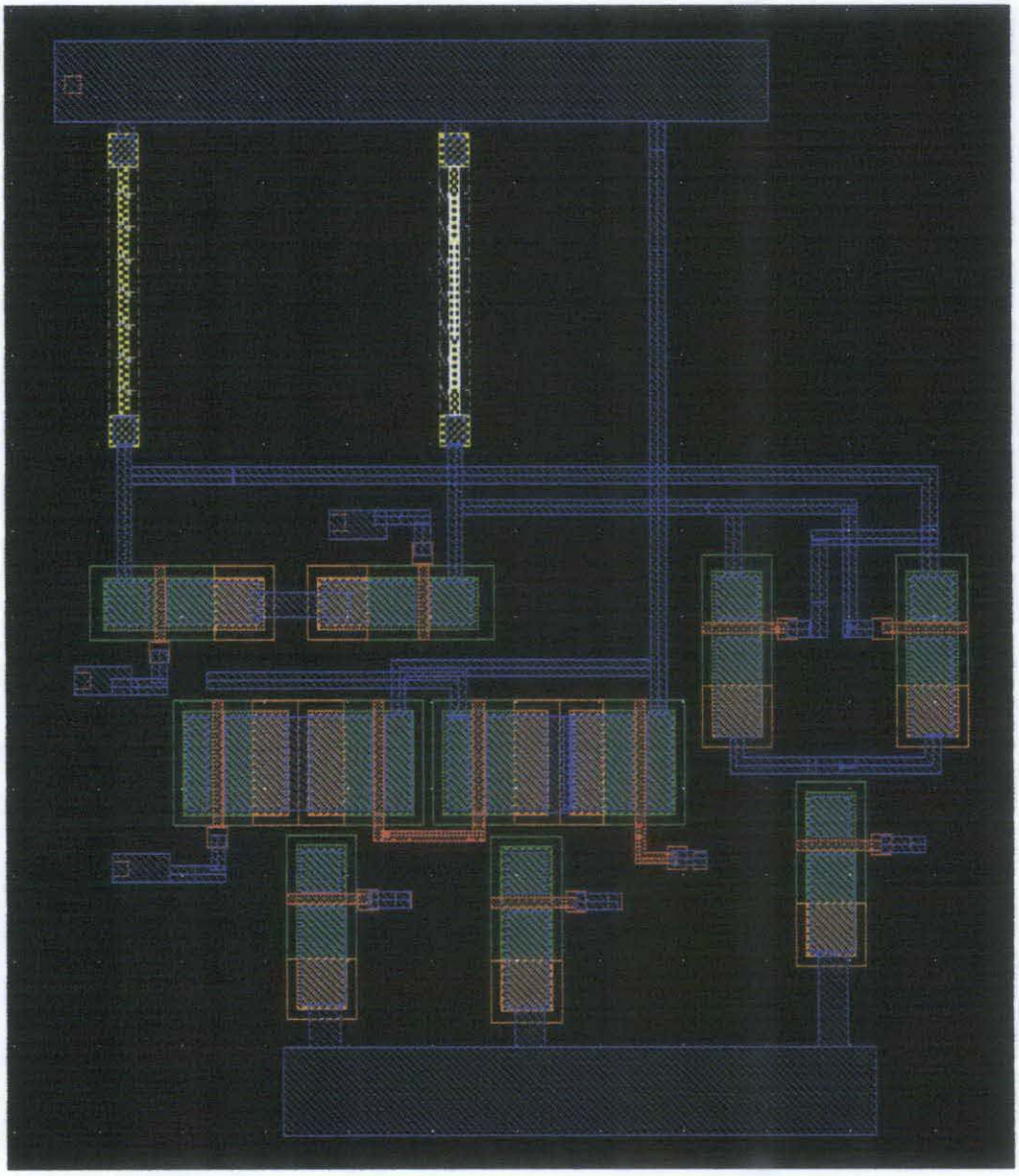

Figure 17: CML Latch layout.

4.4.1 *Design Check Rule (DRC)*

After finish draw the layout, next we move on to verify the layout using DRC. The layout drawing must follow the rules such as Minimum Width Rules Minimum Space Rules Minimum Extension Rules and Overlap Rules. Below is result of DRC.

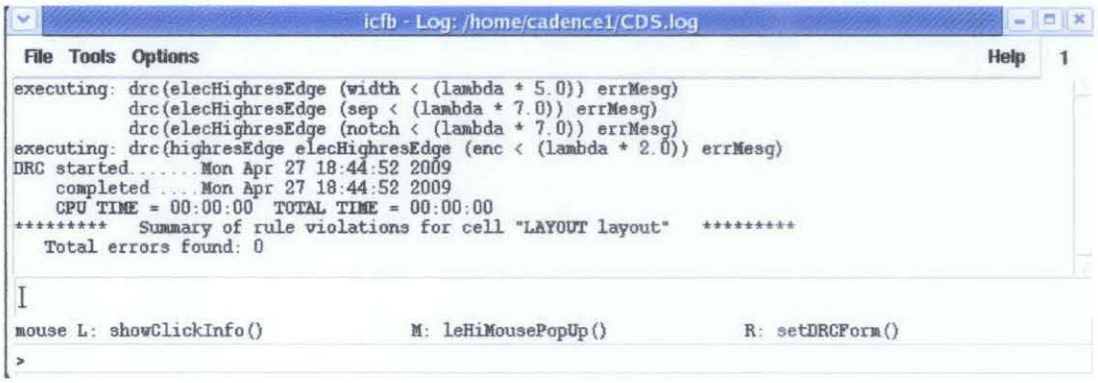

Figure 18: DRC of layout drawing.

4.4.2 *Extracted Layout*

Next we need to extract the layout drawing so that it can be used to compare with the schematic. Figure 19 shows the extracted of layout drawing.

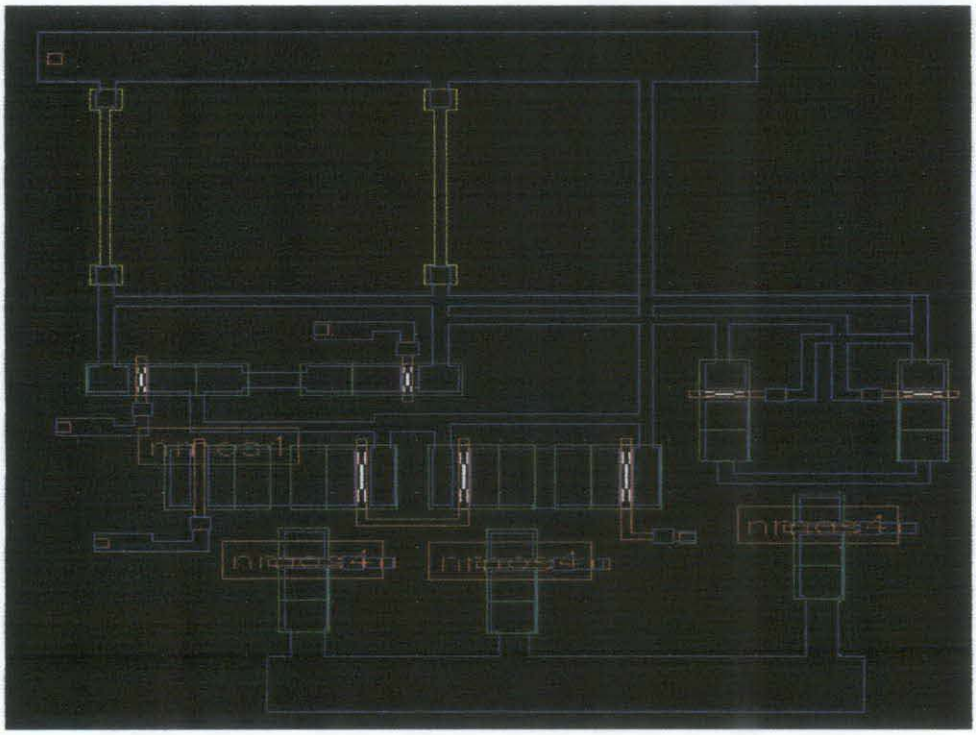

Figure 19: Extracted of layout

Unfortunately, the extracted layout appear a few errors as shown in Figure 20

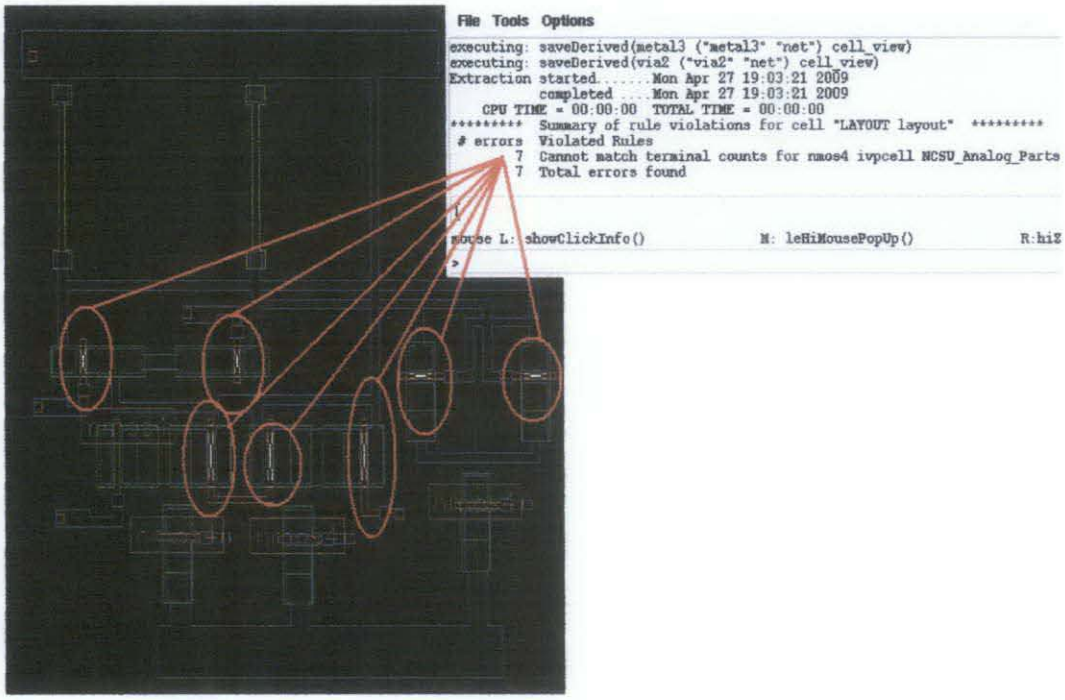

Figure 21: Error of extracted layout.

4.4.3 Layout versus Schematic

Although the layout appear few errors after extracted ,we can still to compare the layout with it's schematic using Layout Versus Schematic (LVS). The result of LVS is shown in Appendix C. Since during extract the layout already appear few errors,the LVS did not physically match.

4.3.4 Discussion of Layout.

The layout drawing manage to pass DRC but fail during the extracted.The errors appear are "Cannot match terminal counts for nmos4 ivpcell NCSU_Analog_Part". The errors happen most probably because of we cannot connect directly between the drain and source of transistor. To overcome this problem,the drawing layout technique must be master in order to avoid error in the future. Since the first CML Latch already facing problem and limitation of time to solve that problem,the second CML Latch cannot be proceed.

CHAPTER 5

CONCLUSION AND RECOMMENDATION

5.1 Conclusion

Based on the simulation results of conventional frequency divider and modified frequency divider, it can be conclude that the modified frequency divider manage to reduce 20 % to 57.14 % of the current spike that occurs during the transition between the track and latch mode. Due to the technology limitation, the current spike cannot be eliminated. The modified frequency divider managed to reduce 11.76 % to 53.85 % of the rise time and fall time at the output voltage hence reduce the latch delay.

Although the main intention to design modified frequency divider is to overcome or eliminate the spike current that occurs during the transition from latch to track mode but due to the technology that available to be used might be the reason why the spike current cannot be totally eliminated.

The modified frequency divider had managed to reduce the fall time and rise time at the output voltage hence reduce the latch delay.

Due to lack of skill in drawing the layout using Cadence Virtuoso Layout Editor, the layout was not able converted with zero errors. The errors appear during extracted the layout are "Cannot match terminal error counts for nmos4 ivpcell NCSU_Analog_Parts".The LVS also did not physically match due to previous error in extracted.

5.2 Recommendations

Since using 0.6μm CMOS Process Technology, the spike current can only be to reduce from 20 % up to 57.14 %.It is recommended that in the future, for this project to be conducted using smaller CMOS Process Technology in submicron ranges. Other than that, the frequency divider in this project is only able to divide by two. It is suggested in the future to design frequency divider that managed to reduce 100% spike current. The layout drawing skill must be mastered fully in order to overcome any error during the layout drawing.

REFERENCES

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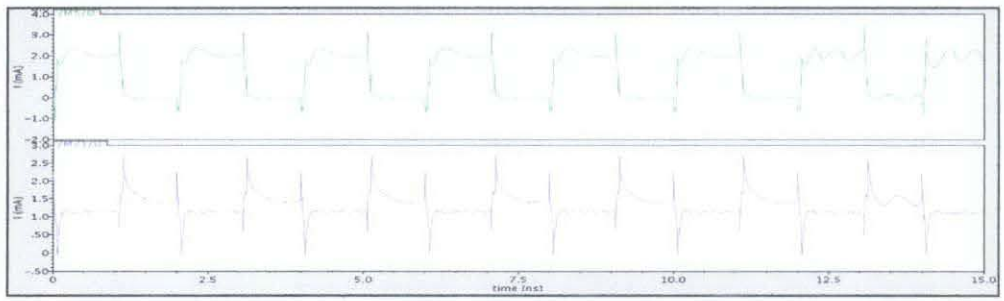
APPENDICES

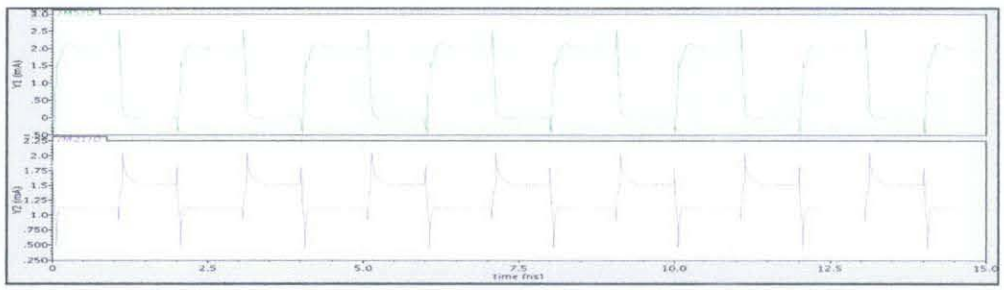
APPENDIX A

The Simulation Result of tail current

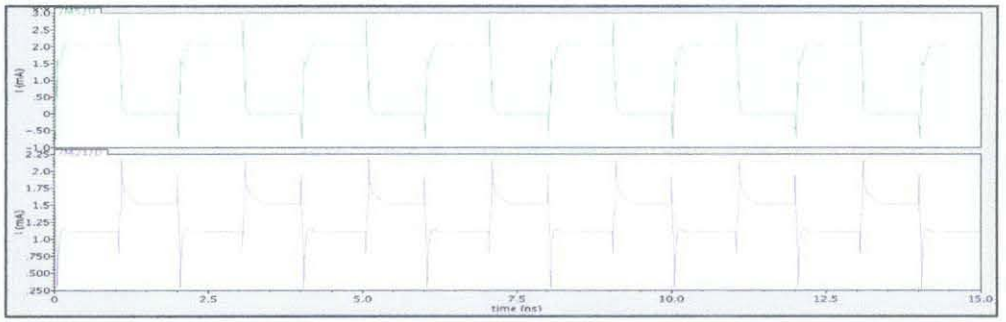
The results are arrange according to Combined Master Slave CML latch circuit and follow by Combined Master Slave Novel CML latch circuit.

At 750 Mhz;

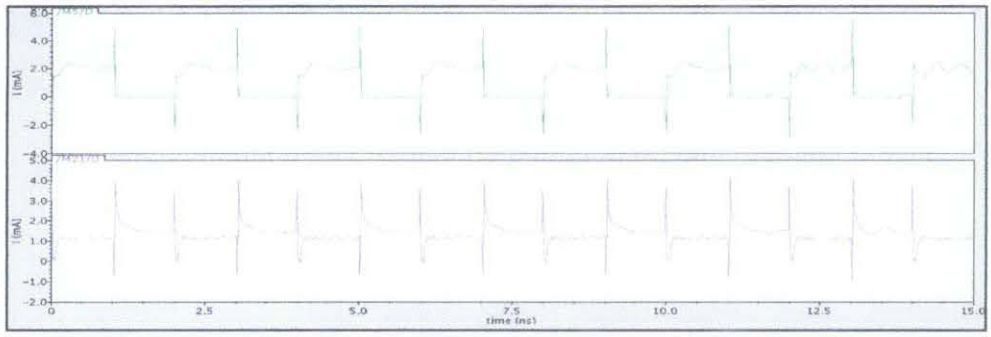


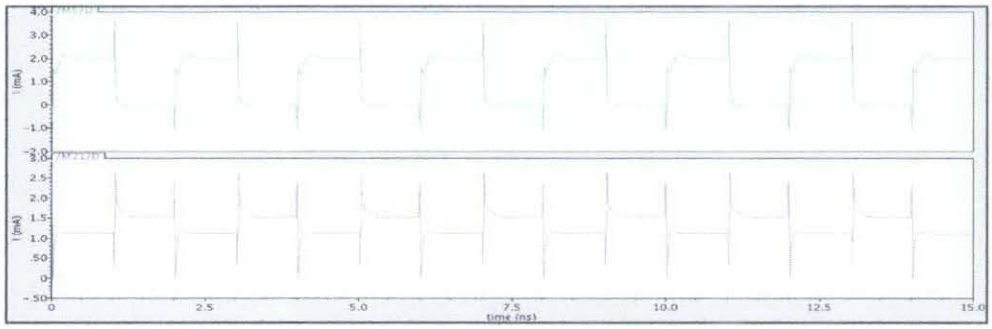


At 1 GHz;

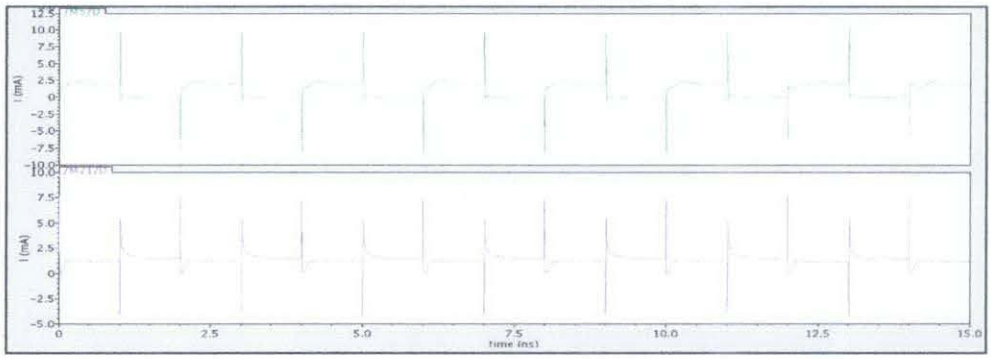


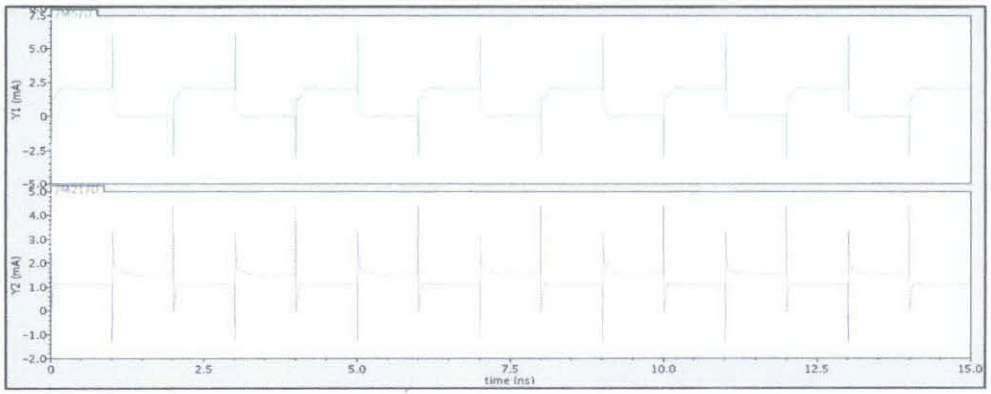
At 2 GHz;





At 2. 5 GHz;



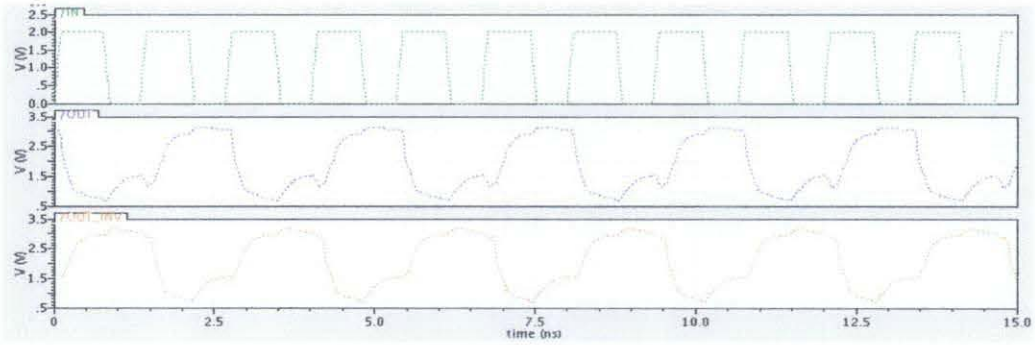


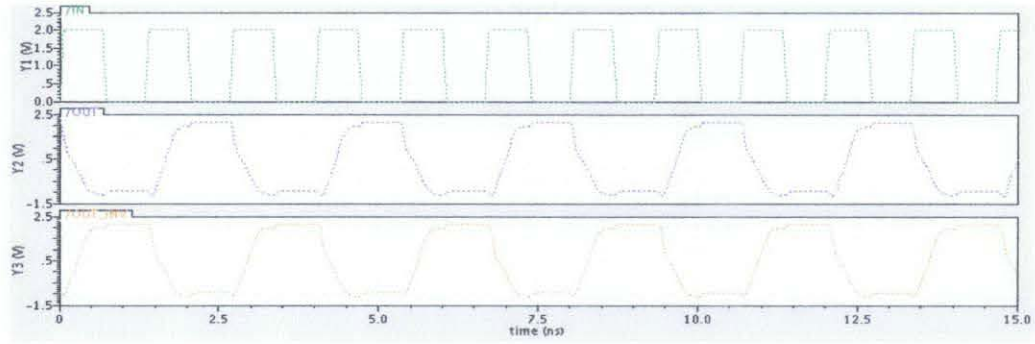
APPENDIX B

The Simulation Result of output frequency

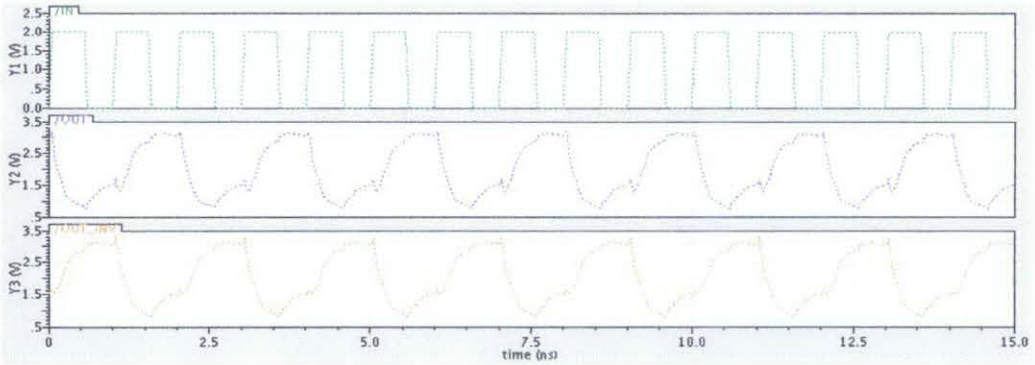
The results are arrange according to Combined Master Slave CML latch circuit and follow by Combined Master Slave Novel CML latch circuit.

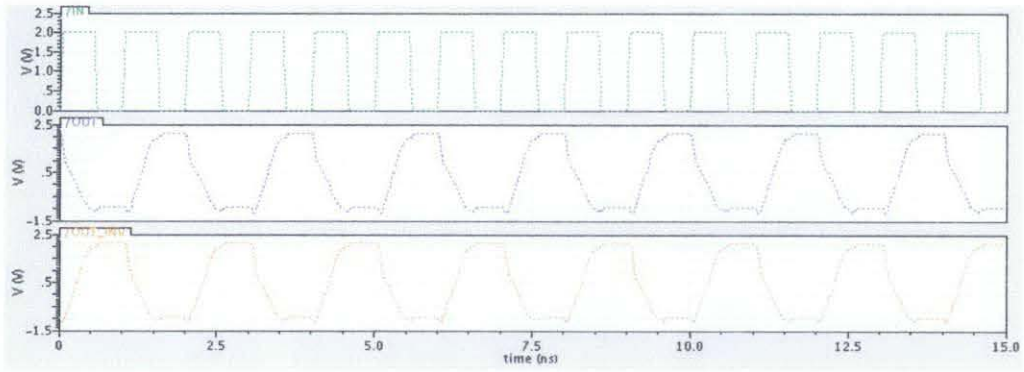
At 750 MHz;



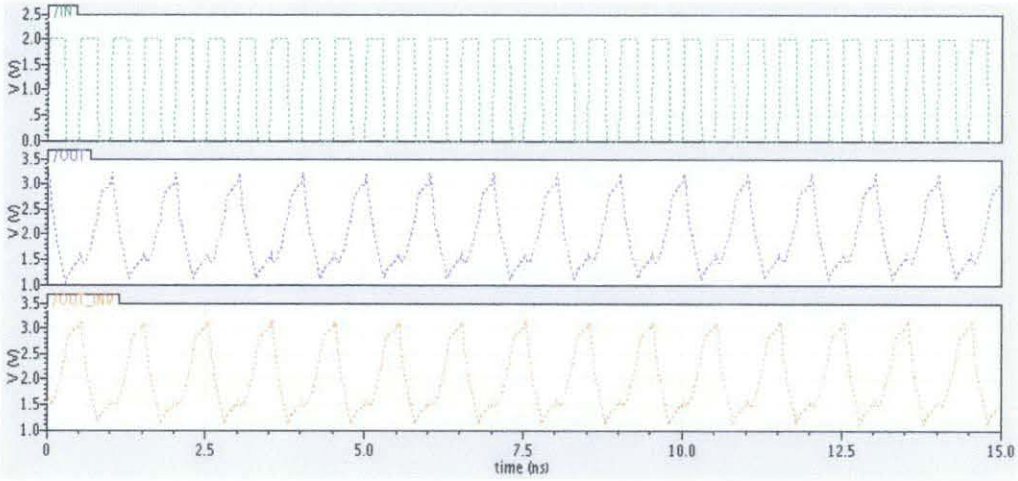


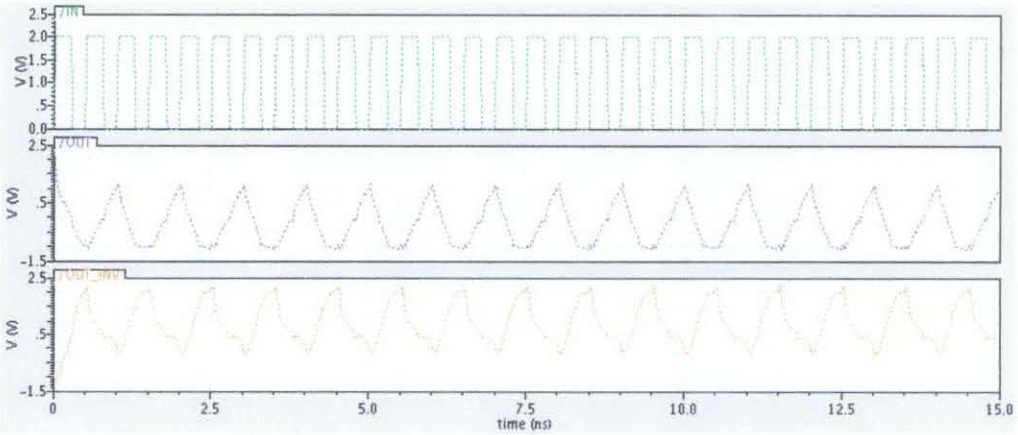
At 1 GHz;



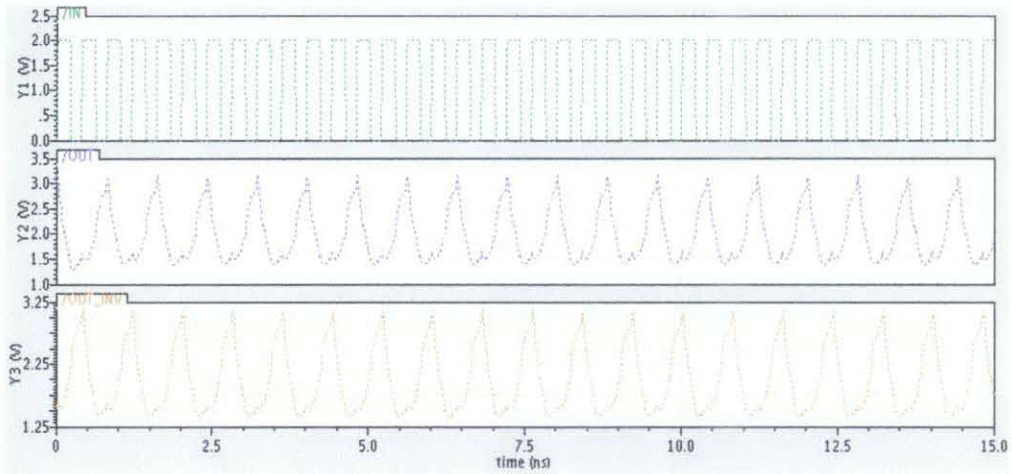

VIN
VOUT
V (V)
time (ns)
0
2.5
5.0
7.5
10.0
12.5
15.0

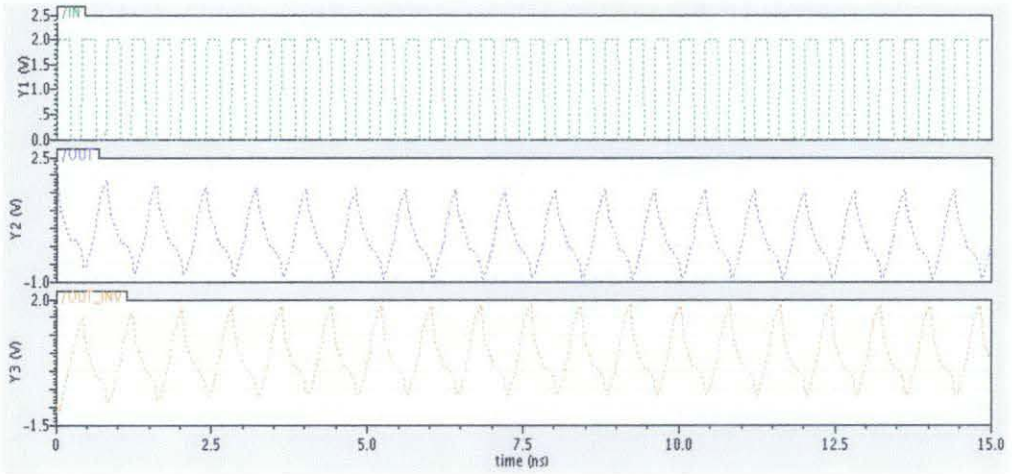
At 2 GHz;


VIN
VOUT
V (V)
time (ns)
0
2.5
5.0
7.5
10.0
12.5
15.0


VIN
VOUT
V (V)
time (ns)
0
2.5
5.0
7.5
10.0
12.5
15.0

At 2.5 GHz;


?IN
?OUT
?OUT_INV
Y1 (V)
Y2 (V)
Y3 (V)
time (ns)


?IN
?OUT
?OUT_INV
Y1 (V)
Y2 (V)
Y3 (V)
time (ns)

APPENDIX C

LVS result

/home/cadence1/LVS/si.out

File Help 24

```
@(#)$CDS: LVS.exe version 5.1.0 02/06/2007 19:59 (cicln01) $

Command line: /cadence_autofs/cadence_binary/IC5141ISR20070210/tools.lnx86/dfII/bin/32bit/LVS.exe -dir /home/cadence1/LVS -l -s -t /home/cadenc
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/cadence1/LVS/layout/netlist
       count
         14            nets
         8             terminals
         11            nmos

    Net-list summary for /home/cadence1/LVS/schematic/netlist
       count
         16            nets
         11            terminals
         2             res
         11            nmos

Devices in the netlist but not in the rules:
        res
Devices in the rules but not in the netlist:
        cap nfet pfet pmos nmos4 pmos4


        Device summary for layout
                  bad  total
        nmos       11     11


        Device summary for schematic
                  bad  total
        res         2      2
        nmos       11     11

The net-lists failed to match.

                            layout  schematic
                              instances
        un-matched            11      13
        rewired               0       0
        size errors           0       0
        pruned                0       0


        active                14      16
        total                 14      16

                              terminals
        un-matched            0       9
        matched but
        different type        0       0
        total                 8       11


Probe files from /home/cadence1/LVS/schematic

devbad.out:
The no. of lines exceeded than specified by the variable lvsLimitLinesInOutFile.
To see the complete information please see the file:
/home/cadence1/LVS/schematic/devbad.out

netbad.out:
The no. of lines exceeded than specified by the variable lvsLimitLinesInOutFile.
To see the complete information please see the file:
/home/cadence1/LVS/schematic/netbad.out

mergenet.out:
```

prunenet.out:

prunedev.out:

audit.out:

Probe files from /home/cadence1/LVS/layout

devbad.out:
The no. of lines exceeded than specified by the variable lvsLimitLinesInOutFile.
To see the complete information please see the file:
/home/cadence1/LVS/layout/devbad.out

netbad.out:
The no. of lines exceeded than specified by the variable lvsLimitLinesInOutFile.
To see the complete information please see the file:
/home/cadence1/LVS/layout/netbad.out

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out: