240VAC TO 110VAC VOLTAGE CONVERTER

By

IRMAN BAKTI BIN ALIAS

FINAL PROJECT REPORT

Submitted to the Electrical & Electronics Engineering Programme
In Partial Fulfillment of the Requirements
For the Degree
Bachelor of Engineering (Hons)
(Electrical & Electronics Engineering)

Universiti Teknologi Petronas
Bandar Seri Iskandar
31750 Tronoh
Perak Darul Ridzuan

CERTIFICATION OF APPROVAL

240VAC TO 110VAC VOLTAGE CONVERTER

by

IRMAN BAKTI BIN ALIAS

A project dissertation submitted to the
Electrical & Electronics Engineering Programme
Universiti Teknologi PETRONAS
in partial fulfillment of the requirement for the
Bachelor of Engineering (Hons)
(Electrical & Electronics Engineering)

Approved:

Mr. Lo Hai Hiung
Project Supervisor

Lo Hai Hiung
Lecturer
Elektrik & Elektronik Engineering
Universiti Teknologi Petronas
31750 Tronoh
Perak Darul Ridzuan, MALAYSIA
Tel: 05-368 7842
Fax: 05-368 7443
Email: lo_haihiung@petronas.com.my

UNIVERSITI TEKNOLOGI PETRONAS
TRONOH, PERAK

December 2005

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

Irman Bakti Bin Alias

ABSTRACT

The main task of this final year project is to design a household 240VAC to 110VAC voltage converter. This converter should be able to supply up to 400 Watts of power, enough to power up a normal household appliances such as vacuum cleaner. A voltage regulator must be included in the design to ensure the protection of any household appliances that uses this converter. This is important to ensure user safety when operating this converter and to protect the equipments that use this converter. The idea of designing this particular converter is by combining an AC-to-DC converter with a DC-to-AC inverter. Thus, the design must be reliable and efficient in term of power conversion. The cost of the design should be minimized since this type of converter is available in the market but the price is quite expensive. The main concern in this design is to minimize the cost needed to build this converter while maintaining its performance.

ACKNOWLEDGEMENTS

Firstly, I would like to express my sincere thanks to my supervisor Mr. Lo Hai Hiung, who has guided me in completing this project. Your supervision and leadership has been great in directing me through the correct path in completing this project. Additionally I would like to express my special thanks to Mr. Norzaihar Yahya who has guided me through the process in completing this project. I am also grateful to thanks all technicians who I worked with either directly or indirectly involve in this project. They had been kind and helpful in assisting me to carry out my work, and also in sharing their knowledge and experiences with me. I would also like to thank Universiti Teknologi PETRONAS (UTP) by providing the facilities such as internet services, information, books and also budget for this project. In addition my thanks also go to my parent who has supported me without any sign of exhaustion in doing this project. Thanks also to my friends who have help me to get information and help me throughout this period. The support and encouragement from the people above will always be a pleasant memory throughout our life.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

AC	-	Alternate current
BJT	-	Bipolar junction transistor
DC	-	Direct current
EWB	-	Electronic Workbench
IC	-	Integrated circuit
MOSFET	-	Metal-Oxide-Semiconductor Field-Effect-Transistor
PCB	-	Printed circuit board
PWM	-	Pulse width modulation
TNB	-	Tenaga Nasional Berhad
US	-	United States
UTP	-	Universiti Teknologi PETRONAS

CHAPTER 1

INTRODUCTION

Power processing has always been an essential feature for most electrical appliances. Differences in voltage and current requirements for different applications have led to design of dedicated power converters to meet those specific requirements. These power conversion devices are widely available in the market. There are 4 types of power conversion devices available in markets, which are AC-to-DC converter, DC-to-AC converter, AC-to-AC converter and DC to DC converter.

1.1 Problem Statement

Alternate current (AC) source is the most commonly used as an electrical source to power up most electrical appliances. In Malaysia, normal power source supplied by Tenaga Nasional Berhad (TNB) is a single-phase 240V 50Hz. Even though the main supply is from an AC source, some of electrical appliances have its own operating current and temperature. Therefore, the AC supply sometimes need to be manipulated to certain level or even rectify to direct current (DC) source to power up household appliances.

Normal household appliances have a different operating current and voltage. The main reason this 240VAC to 110VAC converter design is to satisfy the requirements of those appliances, which rated at 110VAC. This converter operates at lower level of current and voltage compare to normal power point available that supply 240VAC with 13 Amperes of current. Lower current produce in this particular converter is to ensure the safety of home user when operating those household appliances.

Since this type of converter is already available in the market, the main task is basically to reduce cost consumption in designing this type of voltage converter. The requirement in designing this converter is to be able to supply up to 400 Watts of power with a regulator to protect the equipments from any damage. The main usage of this converter is to power normal household appliances such as vacuum cleaner.

1.2 Project Objectives

The main objectives of this project are:

- To design a reliable 240VAC to 110VAC converter.
- To minimize cost in this converter.
- To ensure the converter able to supply up to 400W.

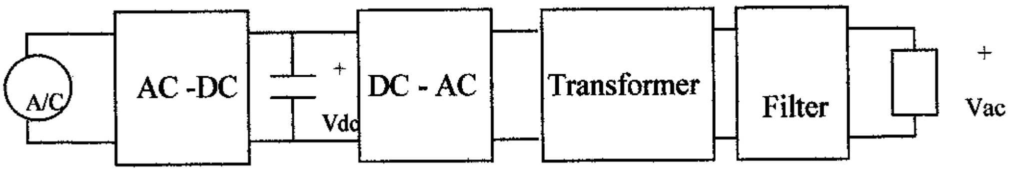
1.3 Scope of Work

This design involves several topics in power electronics field that need to be concerned. This design includes simulating and designing a converter, which uses a transformer as a voltage step up or step down and a combination of more than one type of voltage converter. The limitation in conducting this project is basically cost, time and knowledge. The prototype will be constructed by using fund provided by Universiti Teknologi PETRONAS.

CHAPTER 2

LITERATURE REVIEW

Block diagram below shows the combination of AC-to-DC converter with DC-to-AC converter in a power electronic circuit to form an voltage converter. [1]



2.1 AC-to-DC Converter (Rectifier)

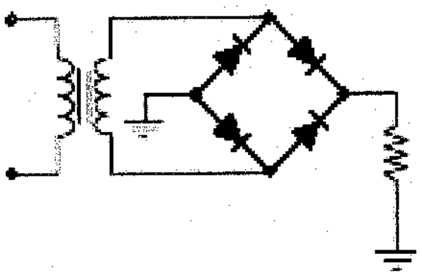


Figure 1: Bridge Rectifier

Rectifier circuit is normally used in power supply design. There were 3 types of AC-to-DC converter, which are half wave, full wave and bridge rectifier circuit. In this particular design, bridge rectifier circuit is most widely used in AC-to-DC converter. Figure 1 above shows the bridge rectifier circuit. In this rectifier circuit, a regulator circuit needs to be used to ensure voltage stability for safety purpose.

2.2 DC to DC Converter (Regulator)

There are three types of DC-to-DC converter which are buck converter, boost converter and buck boost converter.

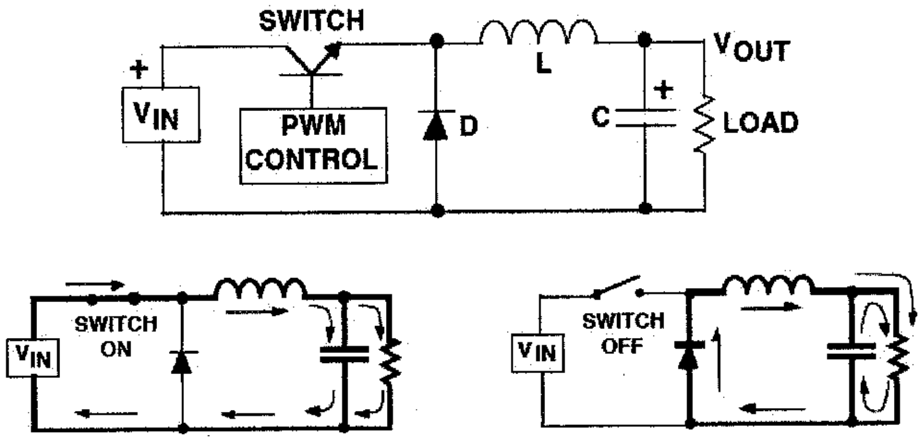


Figure 2: Buck Converter

Buck converter circuit is normally used to step down the dc voltage (V_{IN}) in the circuit by controlling the duty cycle, D of the switching devices. Buck converter provides control for duty cycle less than 0.5.

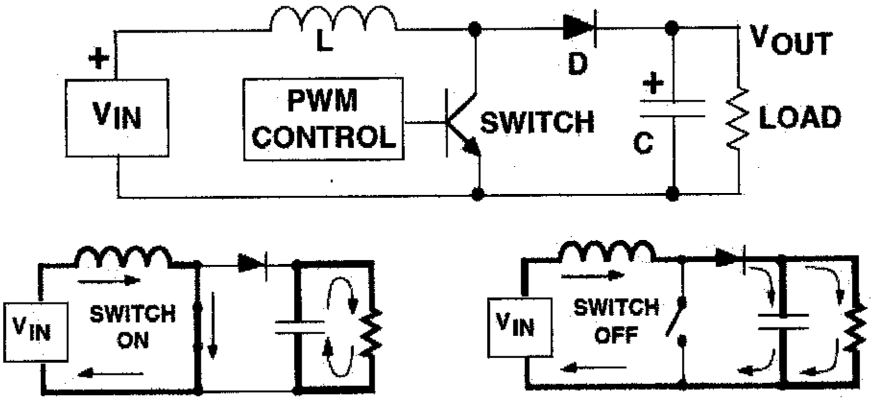


Figure 3: Boost Converter

Boost converter circuit is normally used to step up the dc voltage supply (V_{IN}) in the circuit by controlling the duty cycle, D of the switching devices. Boost converter provides control for duty cycle more than 0.5.

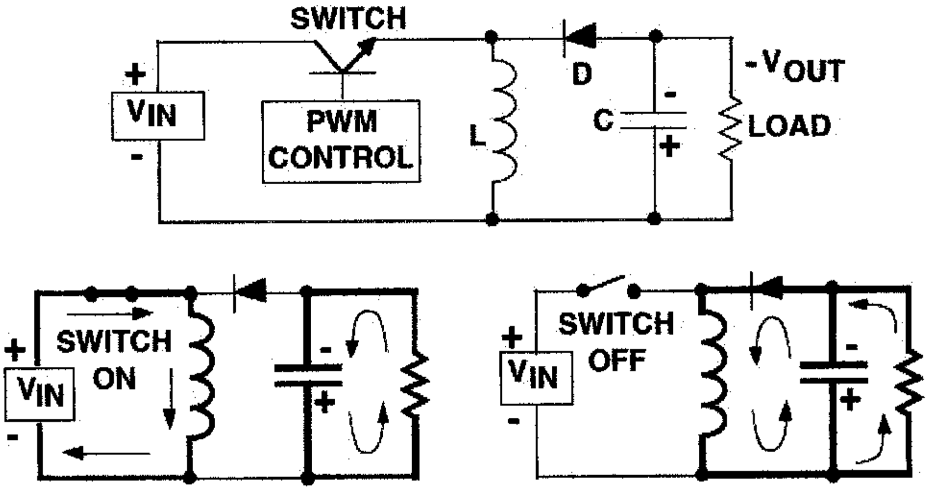


Figure 4: Buck Boost Converter

Buck Boost converter can perform either buck or boost operation with inverted polarity at the output voltage. The performance of the circuit can be change by controlling the switching devices duty cycle, D by using PWM controller.

2.3 DC-to-AC Converter (Inverter)

Inverter circuits have 3 types of configurations, which are biphase, half bridge and full bridge. This kind of circuit use fixed source of DC to produce symmetrical AC output voltages at fixed or variable frequency and magnitude. The frequency of the AC output can be controlled by the switching speed of the inverter circuit. [2]

2.4 Transformer

Transformer is used normally to step up or step down the voltage or current from an AC source.

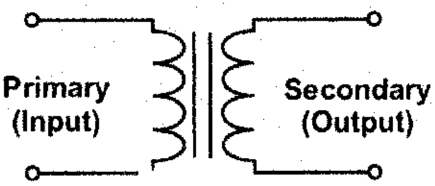


Figure 5: Transformer

Figure 2 shows the basic schematic symbol for the transformer. Note that it has two windings, the primary and the secondary. The input voltage is applied to the primary winding and the output voltage is taken from the secondary winding. The vertical lines between the windings represent an iron core transformer. Since the flux is constant for primary and secondary windings, the induced voltages will be proportional to the number of turns. Therefore,

$$\frac{V2}{V1} = \frac{N2}{N1} \quad [1]$$

Where;

V1 = Primary voltage

V2 = Secondary voltage

N1 = Primary turns

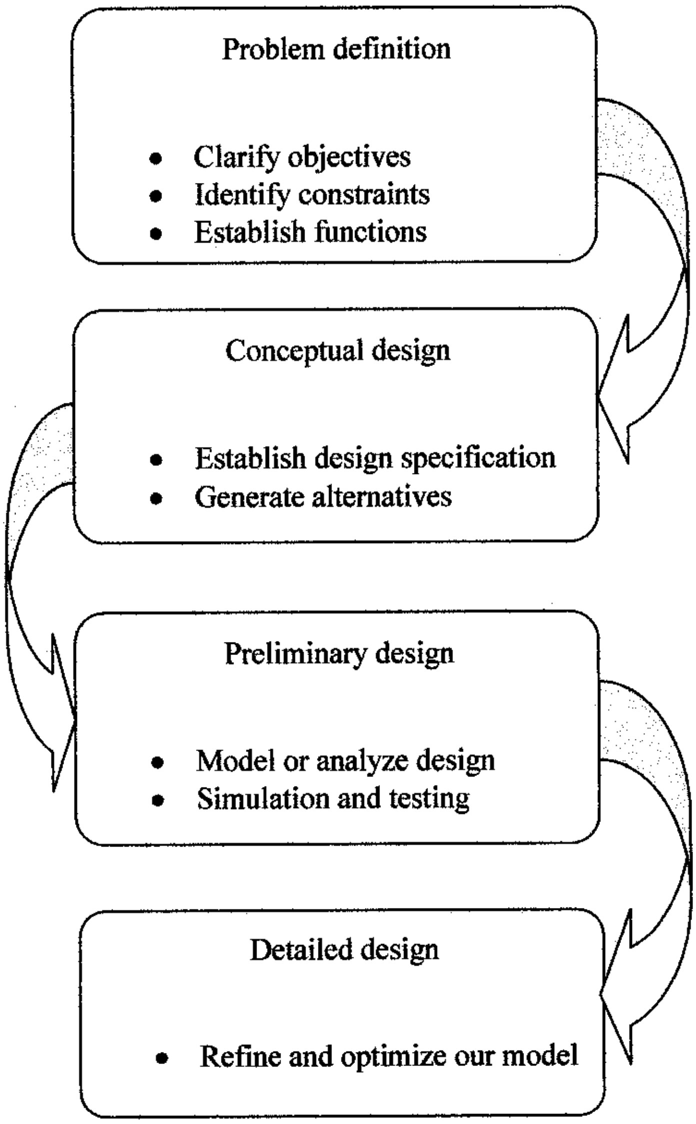
N2 = Secondary turns

Note that transformer chosen must fulfill the rated VA (apparent power). [4]

CHAPTER 3

METHODOLOGY

Procedure



Problem definition

- Clarify objectives
- Identify constraints
- Establish functions

Conceptual design

- Establish design specification
- Generate alternatives

Preliminary design

- Model or analyze design
- Simulation and testing

Detailed design

- Refine and optimize our model

3.1 PCB Design

MicroSim PCBoards was used to design a PCB layout. Then, the layout was transferred to Gerber file before submitted to the lab technician for PCB fabrication.

CHAPTER 4

CONCEPTUAL DESIGN

For AC-to-DC side, bridge rectifier (as shown in Figure 1) was selected as the suitable converter to be used in this project. For protection purposes, a fuse is added to separate a direct contact between the AC source and the transformer.

Boost regulator circuit (as shown in Figure 3) was selected to be the most suitable regulator in this project since this circuit can sustain high current. Previously, buck boost regulator was chosen but due to difficulty to find inductor for the circuit, boost converter was chosen in this project. The maximum and minimum current difference between those two regulators made the boost converter more relevant to be used in this project.

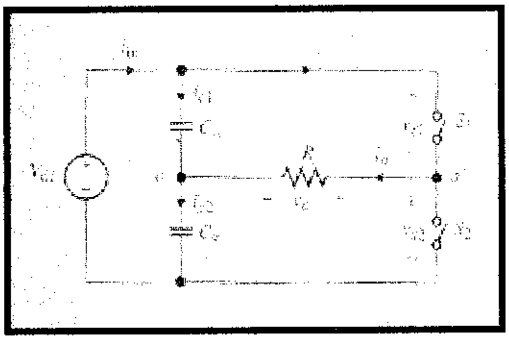


Figure 6: Half Bridge Inverter

A half bridge inverter circuit was chosen in this design. It was because this type of inverter is suitable for low power design, which is categorized below 800W. [3]

PWM using IC was chosen to be use in this project. One of the suitable IC's for this method was ICL8038. Below is one of the IC's that can be used as PWM.

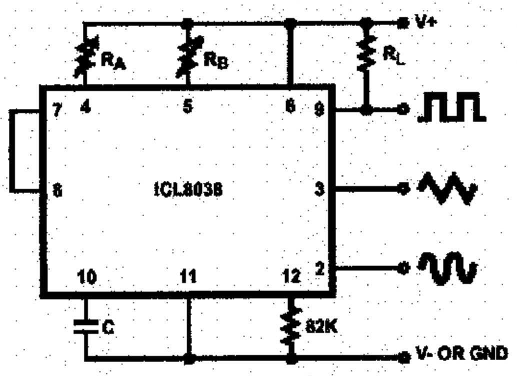


Figure 7: ICL8038

Set R_A equal to R_B for a regular triangle wave (equal rising and falling edges). The frequency of the triangle wave is $f = \frac{0.33}{R_A \times C}$

The capacitor value should be chosen at the upper end of its possible range. The waveform generator can be operated either from a single power supply (10V to 30V) or a dual power supply (+/-5V to +/-15V). The triangle wave swings from 1/3 of the supply voltage up to 2/3 of the supply voltage, so on a +12V single supply it would swing from 4V to 8V. [6]

As for the PWM controller, UC3825 was used in the boost converter circuit.

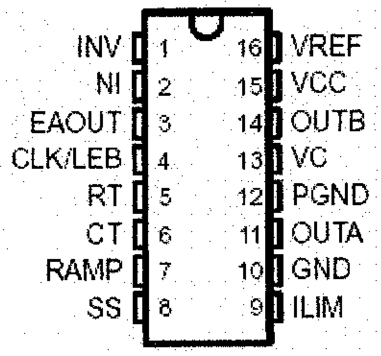


Figure 8: UC3825

The UC3825 provided closed loop operation through a proportional integral negative feedback from the output bus voltage to provide output voltage regulation. Figure 9 outlines how the voltage divider feedback functions in the boost circuit except in a simple form. R_1 and R_2 were chosen such that V_{out} would be 5.1V. The PWM will control the MOSFET by referring to the feedback in voltage mode. The value of Rt and Ct will be chosen as frequency, $f = \frac{1}{Rt \times Ct}$

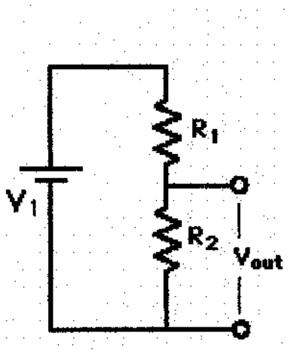
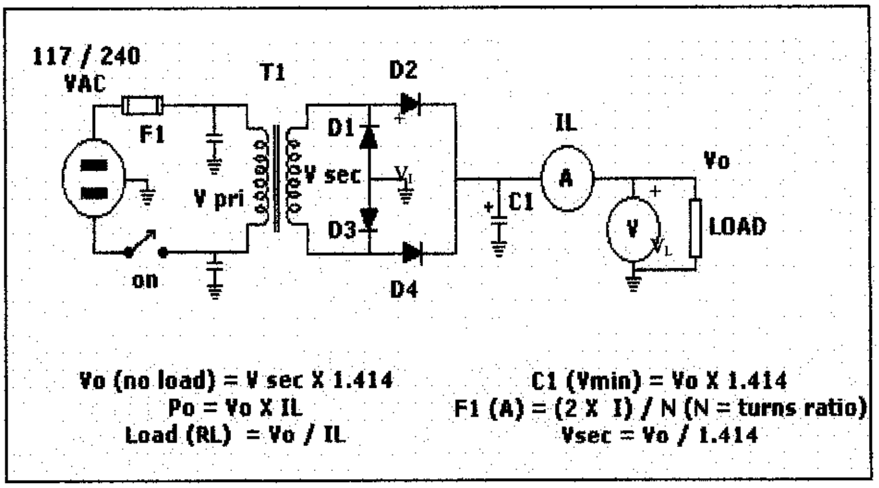


Figure 9: Voltage Divider

4.1 Calculation

4.1.1 Rectifier circuit (AC-to-DC)



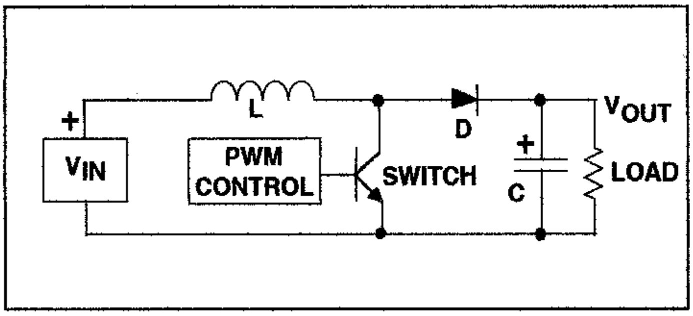
*1.1V voltage drop across bridge rectifier

$V_L = V_O \times 1.414 - 1.1V$

$= 60 \times 1.414 - 1.1V$

$= 83.75$ V [5]

4.1.2 Boost converter (DC to DC)



f = 100kHz

$V_{OUT} = 100V$

$V_{IN} = 83.75V$

$R = 22\Omega$

$$D = 1 - \frac{Vin}{Vout} = 1 - \frac{83.75}{100} = 0.1625$$

$$L_{CRI} = \frac{R\,(1-D)^2\,D}{2f} = \frac{22 \times (1-0.1625)^2 \times 0.1625}{2 \times 100k} = 12.54uH$$

$$L = 100{*}L_{CRIT} \sim 1.254mH$$

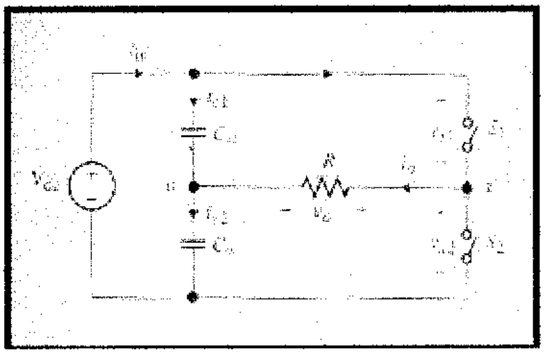
$$= 1mH$$

$$IL_{MAX} = Vin \times \left(\frac{1}{R(1-D)^2} + \frac{D}{2fL} \right) = 83.75 \times \left(\frac{1}{22 \times (1-0.1625)^2} + \frac{0.1625}{2 \times 100k \times 1m} \right) = 5.495A$$

$$IL_{MIN} = Vin \times \left(\frac{1}{R(1-D)^2} - \frac{D}{2fL} \right) = 83.75 \times \left(\frac{1}{22 \times (1-0.1625)^2} - \frac{0.1625}{2 \times 100k \times 1m} \right) = 5.359A$$

$$\Delta V_o / V_O = \frac{D}{RCf} = \frac{0.1625}{22 \times 220u \times 100k} = 0.00034$$

4.1.3 *Half bridge inverter (DC-to-AC)*



$$\text{Vo} = \frac{Vs}{2} = \frac{100V}{2}$$

$$= \underline{50\text{V}}$$

$$\text{R} = \frac{Vo^2}{Po} = \frac{50^2}{400W}$$

$$= \underline{6.25\Omega}$$

$$\text{Io} = \frac{Vo}{R} = \frac{50}{6}$$

$$= \underline{8.333\text{A}}$$

Po = IoVo = 8.333A x 50V

$$= \underline{416.67\text{W}}$$

CHAPTER 5

RESULTS

5.1 Simulation

Simulation was done in both *Electronic Workbench* (EWB) and *CADENCE PSpice*. Each circuit was simulated separately before combining all the circuits involve in the design. Simulation in EWB was using a buck boost converter while the simulation in *CADENCE PSpice* was using boost converter. The actual project design was using a boost converter circuit as simulation with *CADENCE PSpice*.

5.1.1 Electronic Workbench (EWB)

Based on data obtain in calculation, a simulation was done by using EWB to ensure the waveform of the output. Transformer was not used in this simulation since the suitable transformer was not found in the components directory.

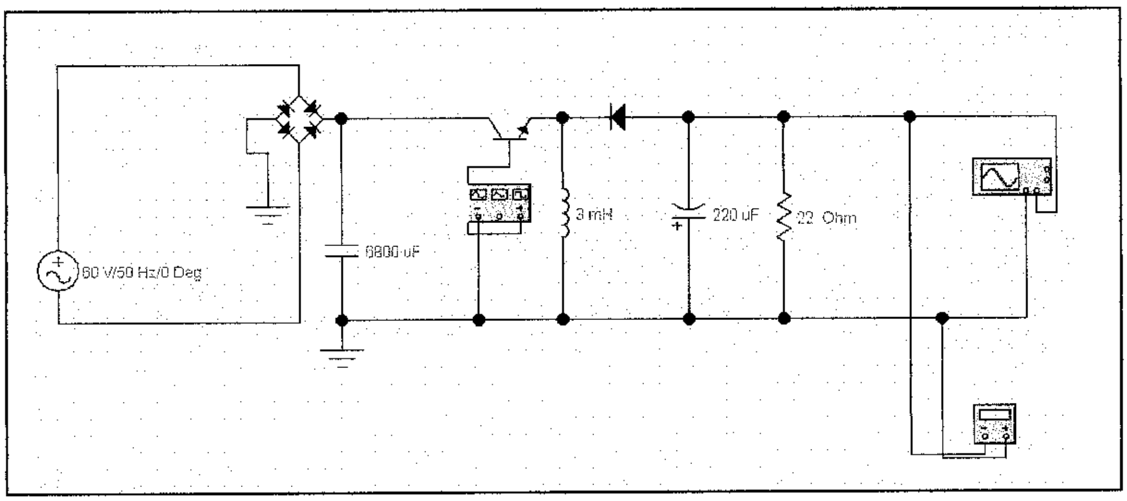
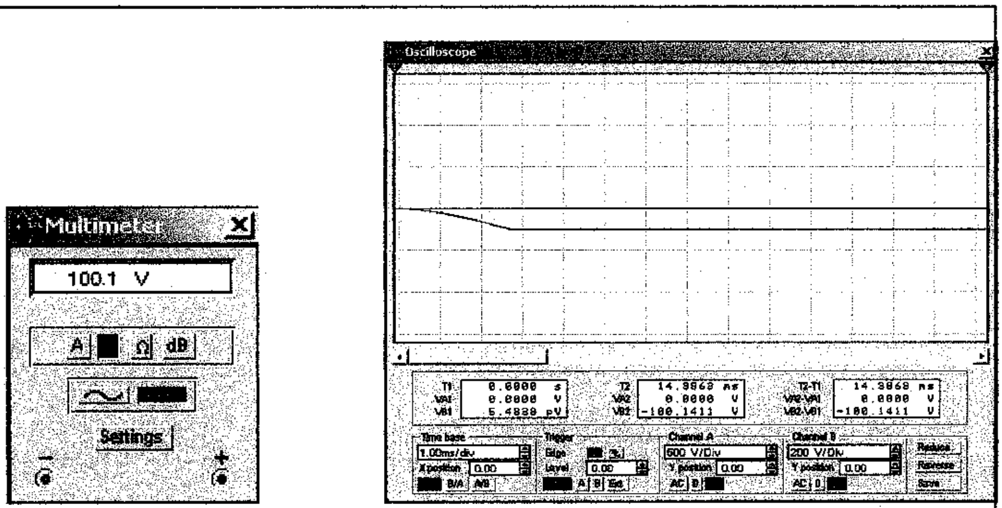


Figure 10: Buck Boost Converter Circuit (EWB)



100.1 V

T1 0.0000 s
VA1 0.0000 V
VB1 5.4828 pV
T2 14.3868 ns
VA2 0.0000 V
VB2 -100.1411 V
T2-T1 14.3868 ns
VA2-VA1 0.0000 V
VB2-VB1 -100.1411 V

Time base 1.00ms/div
X position 0.00
Level 0.00
Channel A 500 V/Div
Y position 0.00
Channel B 200 V/Div
Y position 0.00

Voltmeter

Oscilloscope

Figure 11: Buck Boost Converter Output (EWB)

Figure 10 shows the simulation done by using EWB. This simulation was done by combining the rectifier circuit with the switching regulator circuit. From the simulation, the output of the circuit was monitored using voltmeter and oscilloscope (as shown in Figure 11).

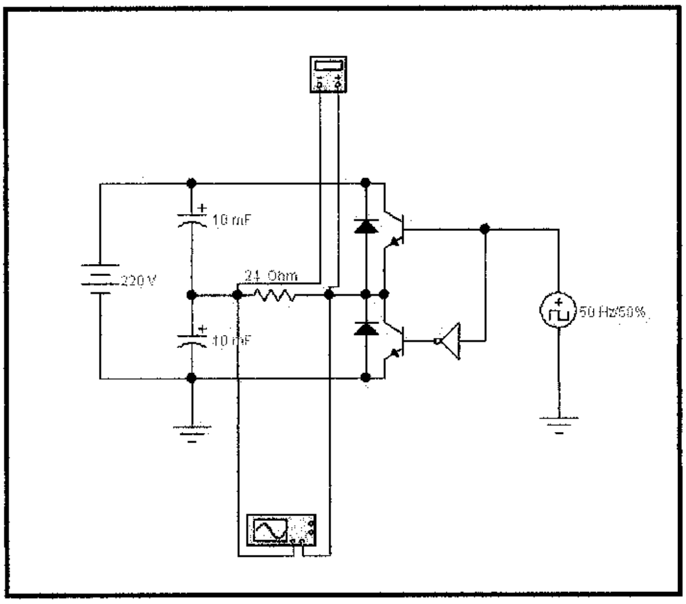
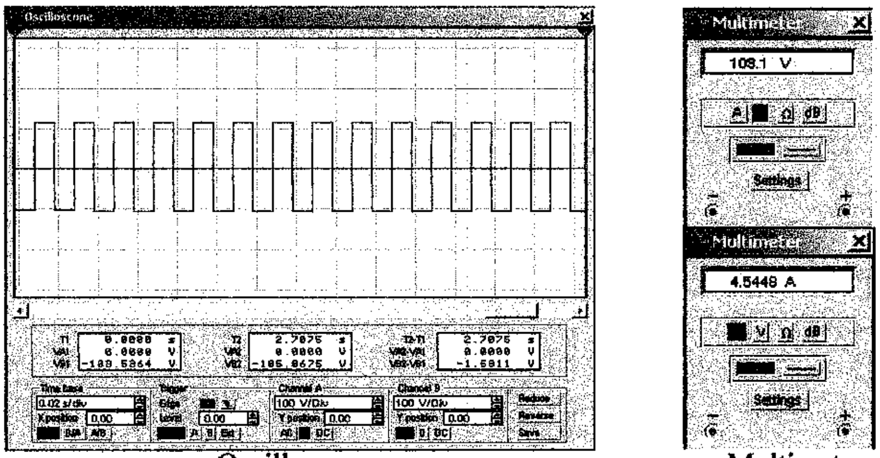


Figure 12: Half Bridge Inverter Circuit (EWB)



T1 0.0000 s
VA1 0.0000 V
VB1 -108.5364 V
T2 2.7075 s
VA2 0.0000 V
VB2 -105.8675 V
T2-T1 2.7075 s
VA2-VA1 0.0000 V
VB2-VB1 -1.5811 V
Time base 0.02 s/div
X position 0.00
Trigger Level 0.00
Channel A 100 V/Div
Y position 0.00
Channel B 100 V/Div
Y position 0.00

Oscilloscope

Multimeter 108.1 V

Multimeter 4.5448 A

Multimeter

Figure 13: Half Bridge Inverter Output (EWB)

Figure 12 shows the simulation of a half bridge inverter circuit. The output of the simulation was observed by using oscilloscope and multimeter as shown in Figure 13.

5.1.2 CADENCE PSpice

Simulation was also done by using *CADENCE PSpice* to obtain accurate value of output for each circuit and combination of all circuit. Figure 14 –21 shows the simulation done by using *CADENCE PSpice*.

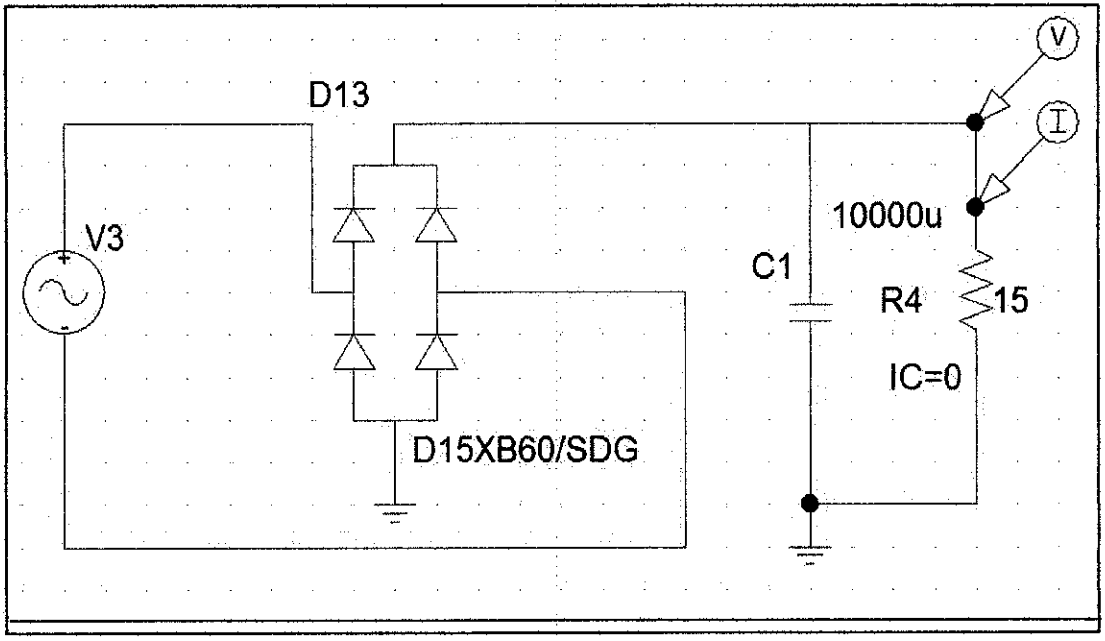


FIGURE 14: Full Bridge Rectifier Circuit

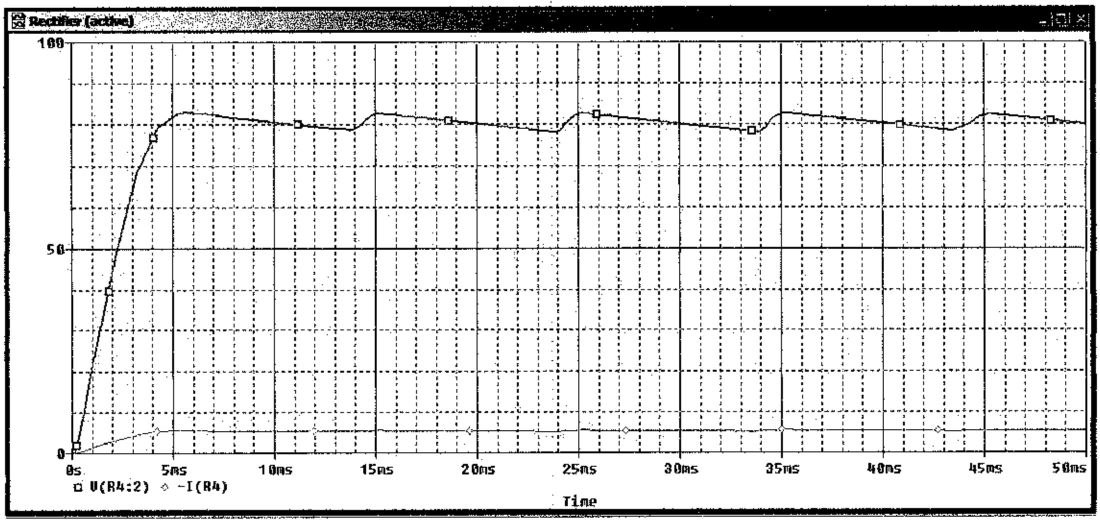


Figure 15: Full Bridge Rectifier Output

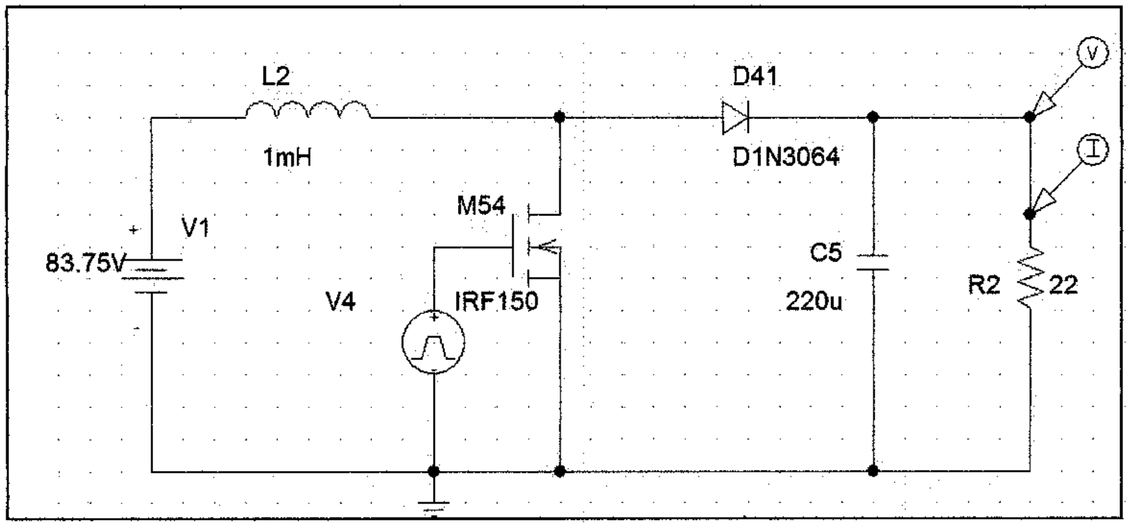


FIGURE 16: Boost Converter Circuit

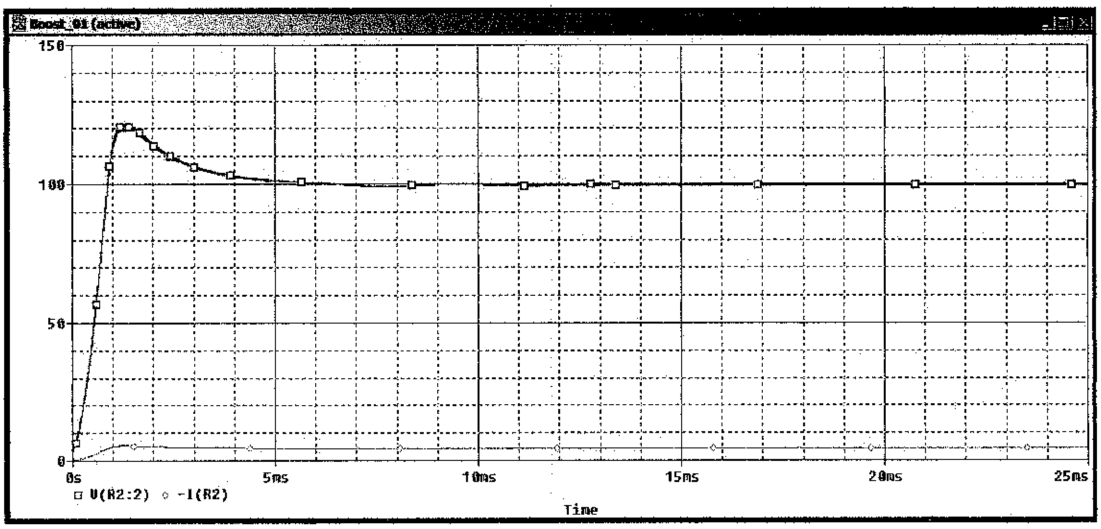


FIGURE 17: Boost Converter Output

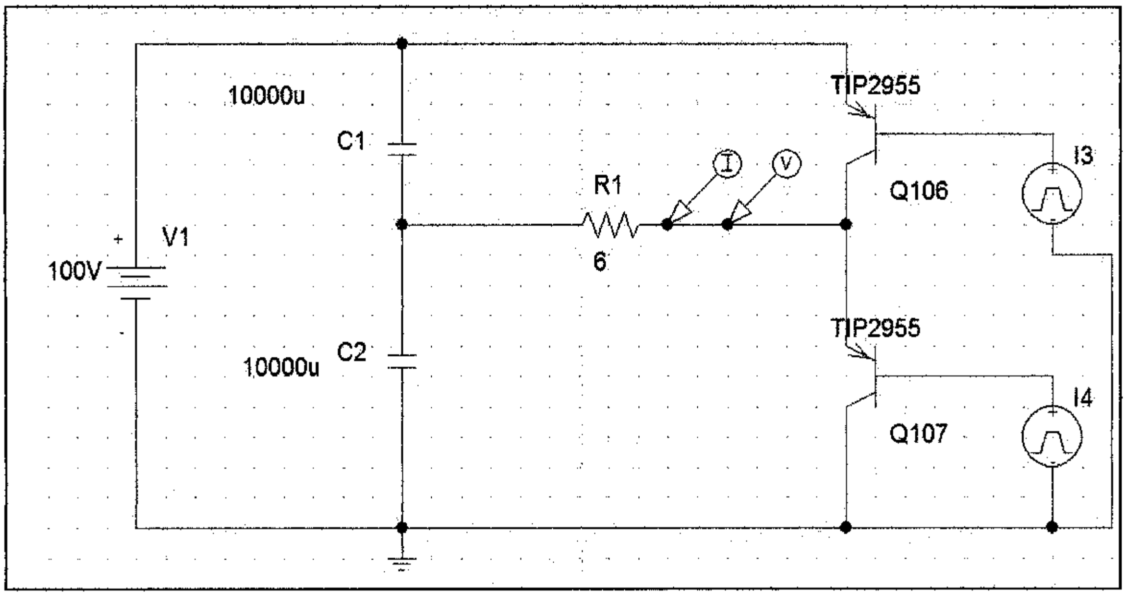


FIGURE 18: Half Bridge Inverter Circuit

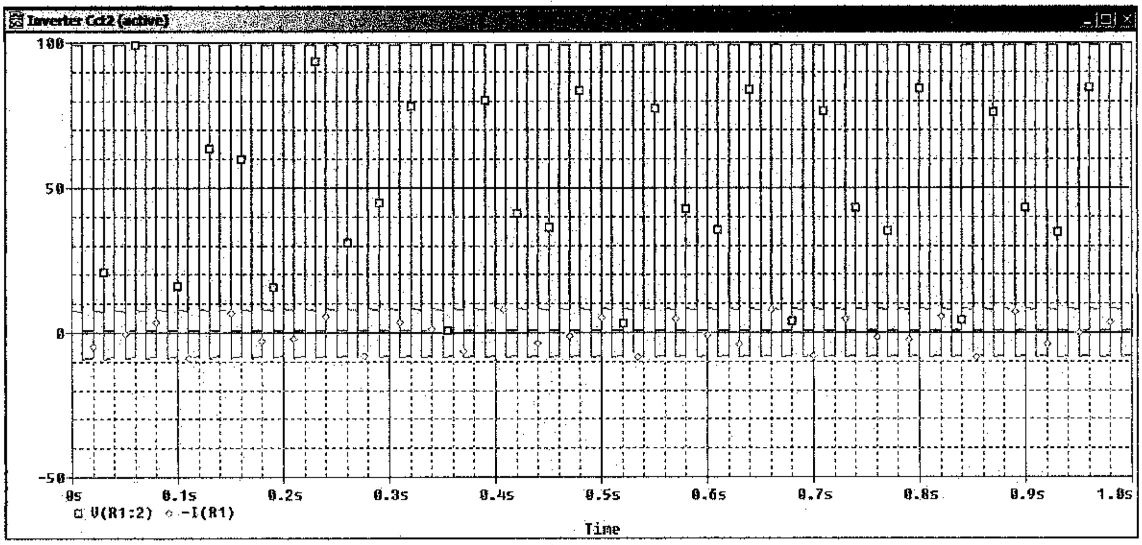


FIGURE 19: Half Bridge Inverter Output

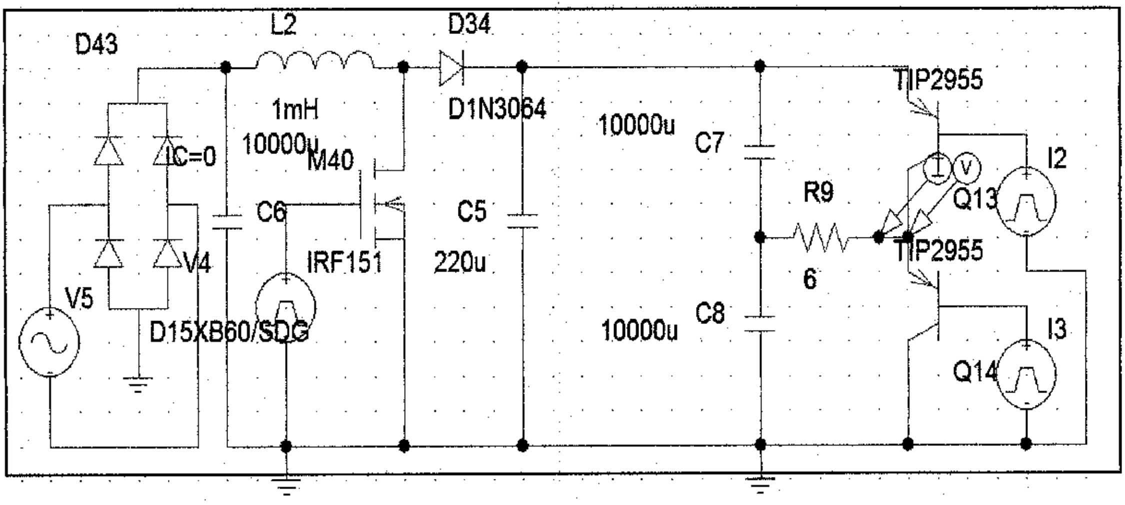


FIGURE 20: Combination Circuit

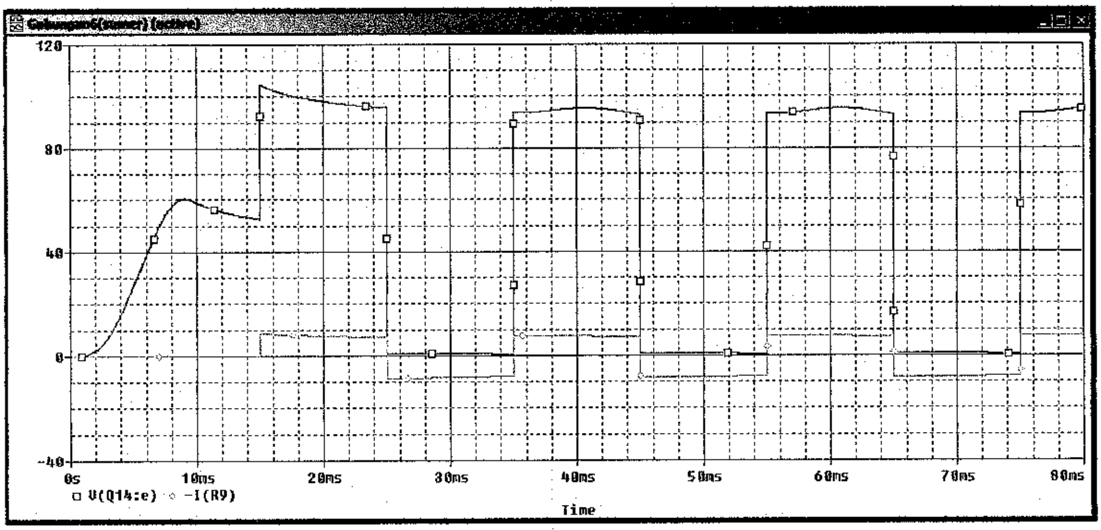


FIGURE 21: Combination Circuit Output

5.2 PCB Layout

Figure below shows the layout of the Printed Circuit Board (PCB) as design by using *MicroSim PCBoards* (as shown in Figure 22) and the actual PCB after fabrication (as shown in Figure 23).

Figure 22: Software PCB Layout

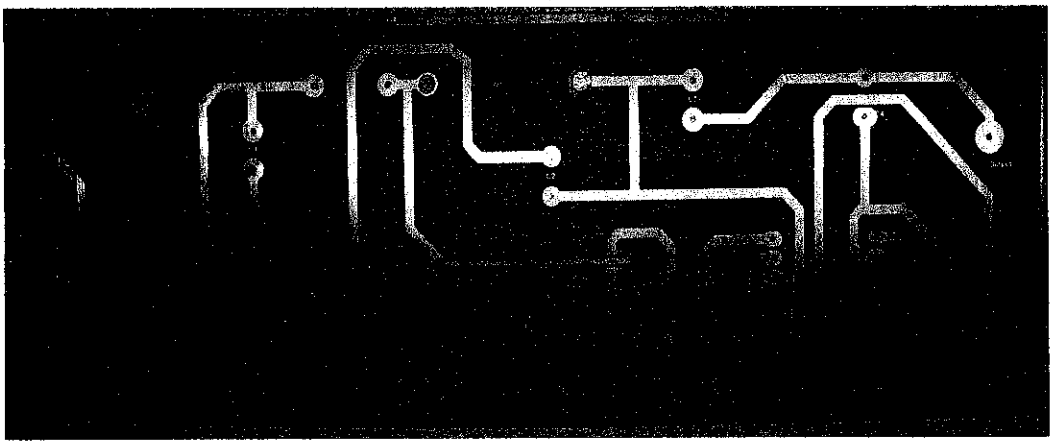


Figure 23: Actual PCB Layout

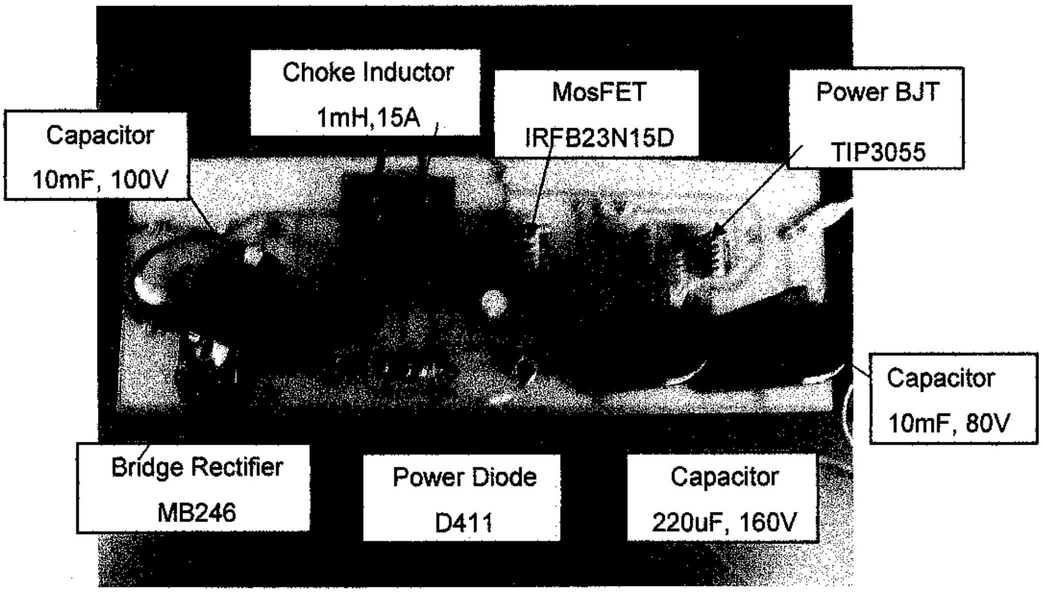


Figure 24: Prototype Layout

5.3 Experimentation Setup

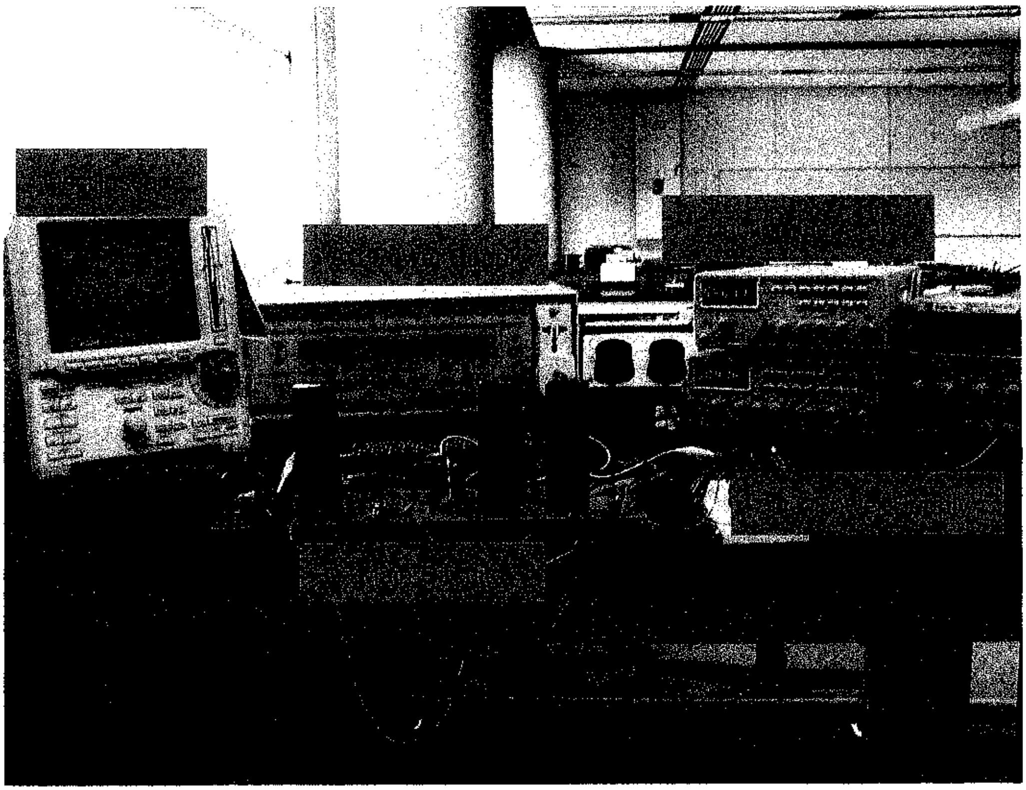


Figure 25: Testing the prototype

All those equipments as shown in Figure 25 were used to test the prototype. AC power supply to represent AC output from main socket, function generator and dc power supply to control the switching frequency and duty ratio for both power MOSFET and BJT while oscilloscope was used to capture the output during the test.

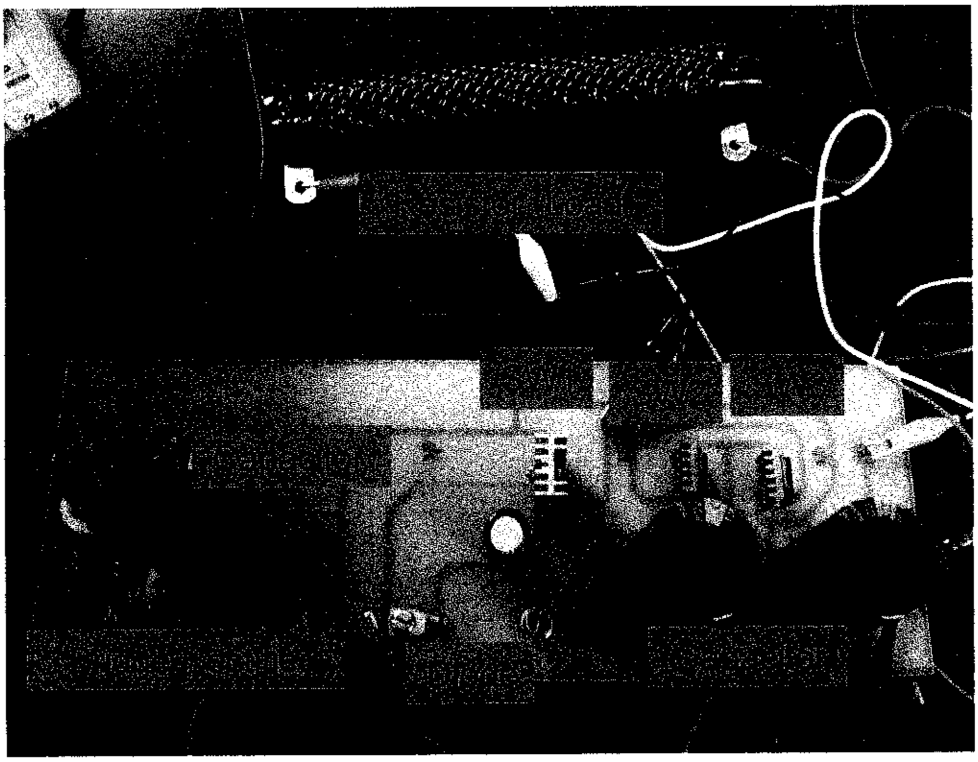


Figure 26: Main circuit during testing

One function generator was used to trigger SW1 and the other one was used to trigger SW2 and SW3. As SW2 and SW3 turn on alternately, an inverter was added to make sure SW2 and SW3 did not turn ON and OFF at the same time.

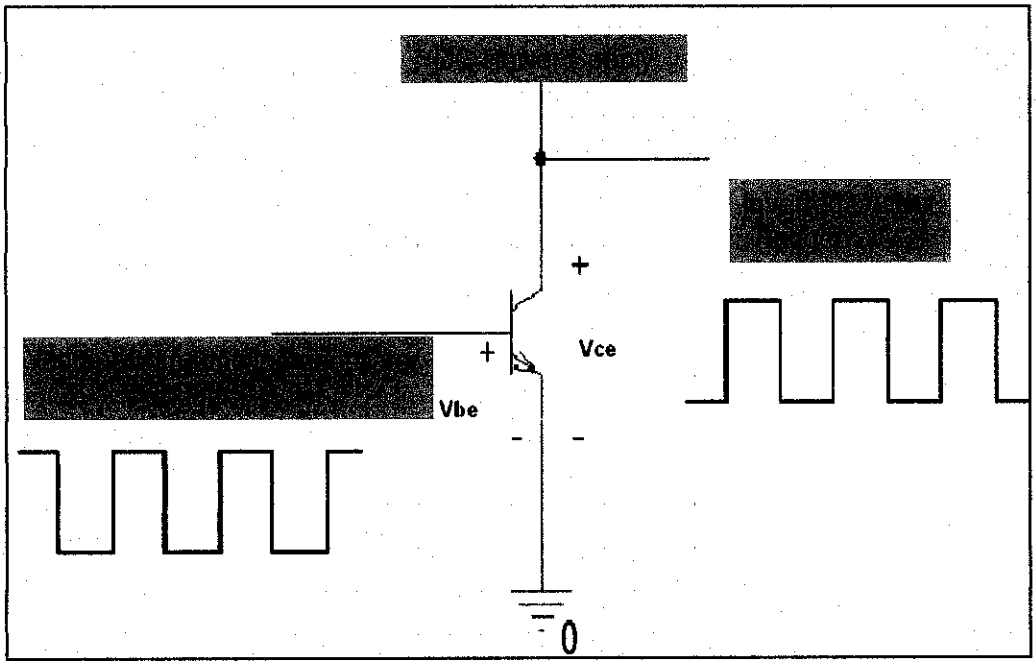


Figure 27: Inverter circuit operation

A power BJT was used in the external circuit to invert the output from function generator so that it can be used to trigger SW3. Output at resistor was captured and compared with simulation output (as shown in Figure 28). Since the prototype does not work perfectly, the circuit only produces output for a while before the inverter circuit is damaged.

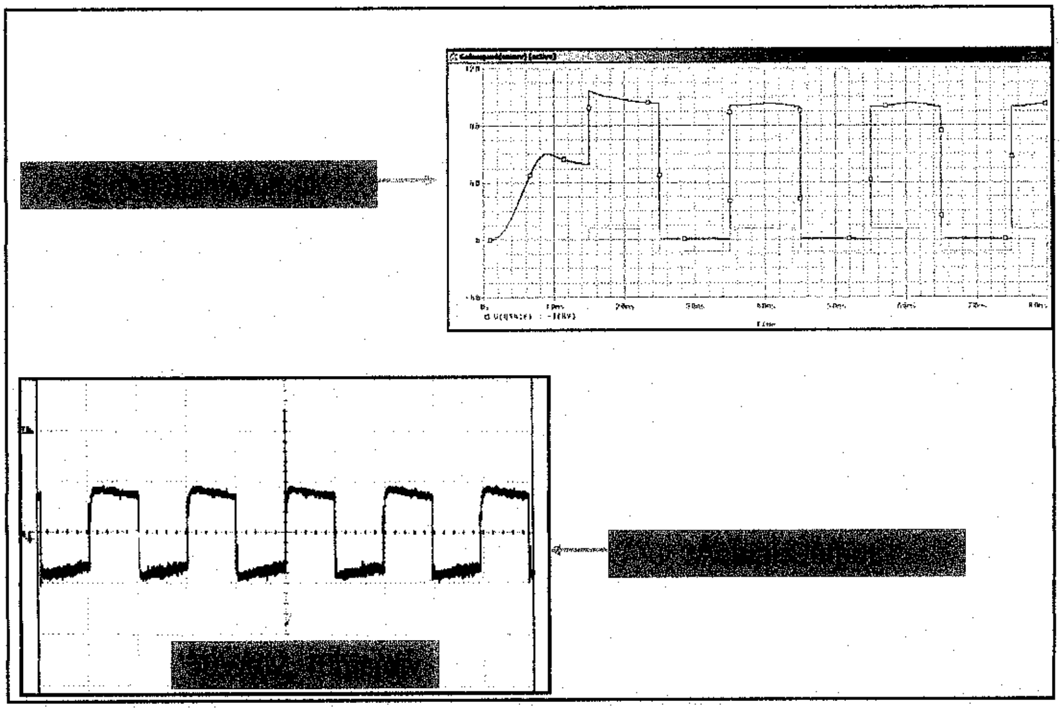


Figure 28: Output Comparison

5.4 Cost Analysis

Table 1: Cost Analysis

	Components	Model	Unit	Price per unit
1	Transformer	D4060	1	RM203.55
		D4064	1	RM203.55
2	Power MOSFET	IRFB23N15D	1	RM8.93
3	Power BJT	TIP3055	2	RM2.50
4	Bridge Rectifier	MB256	1	RM5.00
5	Capacitor	10 000uF, 80V	2	RM27.00
		10 000uF, 100V	1	RM45.00
		220uF, 160V	1	RM4.60
6	Power Diode	D411	1	RM29.19
7	Choke Inductor	1mH, 15A	1	RM55.11
8	PWM Controller	UC3825	1	RM14.99
9	IC Waveform Generator	ICL8038CCPD	2	RM27.86
10	Fuse	2A	1	RM0.35
Total Price				RM657.13

Comparing the price analysis with the product available in market, we can see the difference. Normally product available in market cost more than RM1000 per unit. Even though this cost analysis only include the main components without the finishing works cost. The price is still considered cheaper since the voltage converter circuit itself cost much lower than available product in market. This ensures that this voltage converter can be made cheaper than market prices.

CHAPTER 6

DISCUSSION AND CONCLUSION

6.1 Discussion

This project consists of three main circuits, which are rectifier circuit (AC-to-DC conversion), regulator circuit (DC to DC conversion) and inverter circuit (DC-to-AC conversion). Some of the components used in this power electronics circuit emit heat during operation. Heat sink is needed for such components to reduce losses and ensure safety of circuit operation. From literature review, these are a few components that may produce heat during operation:

1) Transformer
2) Power transistor / MOSFET
3) Capacitor

This components should not be place next to each other to prevent extreme heat transferred especially transformer and capacitor. It may damage the equipment or even worse can cause explode the equipment. So the PCB needs to be checked before soldering the components and before turning ON the circuit. The selections of components were made by going through datasheet and by using the results of simulation. From simulation the circuit should be working well. Since most of the components needed to complete this project need to be ordered from overseas such as UK and Singapore and the price for each component were quite expensive, some of the components were not bought to complete this project. It was because of the cost for this project has already exceeded the amount provided by UTP.

6.2 Conclusion

As a conclusion, it is possible to design a voltage converter that has the ability to supply up to 400W based on calculation and simulation. Main objectives have not been achieved successfully. Although it is possible to achieve in simulation, the prototype built for this project was still not fully functional. This problem occurs due to late components arrival and expensive cost for almost every component. The prototype does not function as simulation because of some components that need to be added in the actual circuit. The main challenge faced is the selection of suitable components in terms of cost and performance. Cost of the product can also be reduced by eliminating several components that is not critical in the circuit design. This voltage converter has proven to be safer as compared to direct AC source as it is isolated from the main source and the load. This will ensure that user will operate electrical appliances safely as compared to direct AC source. Besides that, user can directly used electrical appliances especially from United States by using the 240VAC to 110VAC converter without any modification to the equipment since United States uses 110VAC as their main AC source.

REFERENCES

1. Issa Batarseh, 2004, *Power Electronic Circuits,* United States of America, John Wiley & Son.
2. K. Kit Sum, 1984, *Switch Mode Power Conversion*, United States of America, Marcel Dekker.
3. Muhammad H.Rashid, 2004, *Power Electronics*, 3rd Edition, United States Of America, Prentice Hall.
4. The Basic Power Supply, http://www.technology.niagaraac,on,ca/courses/etec1120/Files/Unit12basicpsu.pdf , Niagara College, Canada.
5. Electronics Tutorial, http://www.electronics-tutorials.com/basics/basic-electronics.htm
6. PWM Signal Generators, http://homepages.which.net/~paul.hills/Circuits/Circuits.html
7. Electronic circuit 'Beans' collection, http://www.interq.or.jp/japan/se-inoue/e_ckt.htm.
8. Datasheet Archive, http://www.datasheetarchive.com/
9. RS Electronic Malaysia Catalogue, http://www.rsmalaysia.com
10. Farnell Components, http://www.farnell.com

APPENDICES

APPENDIX A
GANTT CHART

Gantt Chart for Final Year Project 2 January Semester 2005

Name: Irman Bakti Bin Alias 2550

No.	Detail/ Week	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	Resource Gathering	▨													
2	Prototype Construction		▨	▨	▨	▨	▨	▨	▨	▨	▨	▨			
3	Logbook (Weekly Report)			×	×										
3	Submission of Progress Report				×										
4	Test and verify prototype design					▨	▨	▨	▨	▨					
5	Submission of Progress Report 2								×						
6	Project work continue								▨	▨	▨	▨			
	- PCB Fabrication														
7	Submission of Dissertation Final Draft												×		
8	Oral Presentation													×	
9	Submission of Project Dissertation														×

× Milestone
▨ Process

APPENDIX B

LIST OF COMPONENTS

List of Components [8, 9 & 10]

No	Components	QTY	Description
1	Transformer	2	D4060 x 1 D4064 x1
2	Capacitor	4	10000uF(100V) x 1 220uF(160V) x 1 10000uF(80V) x 2
3	PWM	1	UC3825 x 1
4	IC Waveform Generator	1	ICL8038
5	Inductor	1	1mH, 15A
6	Switch	3	IRFB23N15D x 1 TIP3055 x 2
6	Power diode	1	D411 x 1
7	Fuse	1	2.0A

APPENDIX C

COMPONENTS DATASHEET

4000 RANGE 177-944

UL 506, CANADIAN NATIONAL STANDARD APPROVED

GENERAL SPECIFICATION

Input line voltage: see table.
Frequency: 50/60Hz. Operating Range 47 to 400Hz
Secondary voltage tolerance: Within 3% at normal input and full load.
Flash Tested at 4KV RMS.
Ambient plus temperature rise should not exceed 105°C.
Leads 150 mm long ±5mm PVC insulated
Allow 4mm over fixing kit

INPUT LINE VOLTAGE TABLE

Single primary 110V part number prefix "A"
Single primary 220V Part number prefix "B"
Single primary 240V Part number prefix "C"
Dual primary 120+120V Part number prefix "D"
Dual primary 110+110V Part number prefix "E"
Single primary 230V Part number prefix "F"
Dual primary 115+15V Part number prefix "H"
A range of single primaries 220V, 230V, 240V is available fully IEC 742, EN60/742, BS 3535 approved, see 5000 range data sheet.

ORDERING CODE EXAMPLE

D 4 012

Primary 120+120

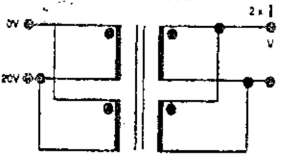
Approval UL 506

VA/Secondary 60 · 15+15

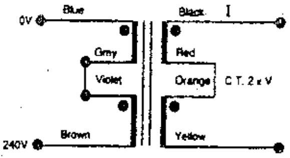
TRANSFORMER CONNECTIONS

Windings may be connected in parallel or series. If they are isolated from each other, the applied potential between them must not exceed 250V DC.

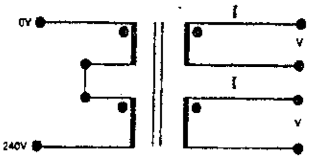
Primaries & Secondaries Parallel Connected



Primaries & Secondaries Series Connected



Primaries Series Connected Secondaries Independent



PERFORMANCE DETAILS

Temperature rise above ambient at maximum recommended continuous VA rating.

Load VA	Regulation %	Temp. Rise °C	Iron Loss W	Copper Loss W
30	16	50	0.40	4.8
60	13	50	0.9	7.8
100	10	50	1.2	10
160	9	56	2.0	14.4
230	8	56	2.75	18.4
330	7	58	3.4	23
530	6	60	5.0	32

Should it be preferable to operate the transformer at lower temperature rise with improved regulation the following table indicates temperature rise which can be expected under continuous conditions at lower VA ratings

Derated VA From	To	Regulation %	Temperature Rise °C
30	20	11	25
60	50	10	35
100	75	8	35
160	120	6	35
230	175	6	35
330	250	5	35
530	400	4	40

Type	Load VA	Secondary RMS Volts V	Secondary RMS Current A	Dimensions Dia. mm	Ht. mm	Weight kg Typical	Mounting
D4000	30	6+6	2.50	70	31	0.42	Dished Fixing Plate M5 Screw
D4001	30	9+9	1.67	70	31	0.42	
D4002	30	12+12	1.25	70	31	0.42	
D4003	30	15+15	1.00	70	31	0.42	
D4004	30	18+18	0.83	70	31	0.42	
D4005	30	22+22	0.68	70	31	0.42	
D4006	30	25+25	0.60	70	31	0.42	
D4007	30	30+30	0.50	70	31	0.42	
D4010	60	9+9	3.33	88	34	0.85	Dished Fixing Plate M6 Screw
D4011	60	12+12	2.50	88	34	0.85	
D4012	60	15+15	2.00	88	34	0.85	
D4013	60	18+18	1.67	88	34	0.85	
D4014	60	22+22	1.36	88	34	0.85	
D4015	60	25+25	1.20	88	34	0.85	
D4016	60	30+30	1.00	88	34	0.85	
D4017	60	110	0.55	88	34	0.85	
D4018	60	220	0.27	88	34	0.85	
D4019	60	240	0.25	88	34	0.85	
D4020	100	12+12	4.17	91	43	1.20	Dished Fixing Plate M6 Screw
D4021	100	15+15	3.33	91	43	1.20	
D4022	100	18+18	2.78	91	43	1.20	
D4023	100	22+22	2.27	91	43	1.20	
D4024	100	25+25	2.00	91	43	1.20	
D4025	100	30+30	1.67	91	43	1.20	
D4026	100	110	0.91	91	43	1.20	
D4027	100	220	0.45	91	43	1.20	
D4028	100	240	0.42	91	43	1.20	
D4030	160	18+18	4.44	113	44	1.90	Dished Fixing Plate M6 Screw
D4031	160	22+22	3.64	113	44	1.90	
D4032	160	25+25	3.20	113	44	1.90	
D4033	160	30+30	2.67	113	44	1.90	
D4034	160	35+35	2.29	113	44	1.90	
D4035	160	110	1.46	113	43	1.90	
D4036	160	220	0.73	113	44	1.90	
D4037	160	240	0.67	113	44	1.90	
D4040	230	25+25	4.60	120	51	2.67	Dished Fixing Plate M8 Screw
D4041	230	30+30	3.83	120	51	2.67	
D4042	230	35+35	3.29	120	51	2.67	
D4043	230	40+40	2.88	120	51	2.67	
D4044	230	110	2.09	120	51	2.67	
D4045	230	220	1.05	120	51	2.67	
D4046	230	240	0.96	120	51	2.67	
D4050	330	25+25	6.60	133	51	3.30	Dished Fixing Plate M8 Screw
D4051	330	30+30	5.50	133	52	3.30	
D4052	330	35+35	4.71	133	52	3.30	
D4053	330	40+40	4.13	133	52	3.30	
D4054	330	45+45	3.67	133	52	3.30	
D4055	330	110	3.00	133	52	3.30	
D4056	330	220	1.50	133	52	3.30	
D4057	330	240	1.38	133	52	3.30	
D4060	530	30+30	8.83	150	61	5.00	Dished Fixing Plate M8 Screw
D4061	530	35+35	7.57	150	61	5.00	
D4062	530	40+40	6.63	150	61	5.00	
D4063	530	45+45	5.89	150	61	5.00	
D4064	530	50+50	5.30	150	61	5.00	
D4065	530	110	4.82	150	61	5.00	
D4066	530	220	2.41	150	61	5.00	
D4067	530	240	2.21	150	61	5.00	

ALL DIMENSIONS ± 2mm

PD - 93894A

International
IOR Rectifier

SMPS MOSFET

IRFB23N15D
IRFS23N15D
IRFSL23N15D

HEXFET® Power MOSFET

Applications

- High frequency DC-DC converters

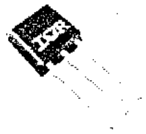
V_{DSS}	$R_{DS(on)}$ max	I_D
150V	**0.090Ω**	**23A**

Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current


TO-220AB
IRFB23N15D


D^2Pak
IRFS23N15D


TO-262
IRFSL23N15D

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	23	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	17	
I_{DM}	Pulsed Drain Current ①	92	
P_D @T_A = 25°C	Power Dissipation ⑦	3.8	W
P_D @T_C = 25°C	Power Dissipation	136	
	Linear Derating Factor	0.9	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	4.1	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torqe, 6-32 or M3 screw⑥	10 lbf•in (1.1N•m)	

Typical SMPS Topologies

- Telecom 48V input DC-DC Active Clamp Reset Forward Converter

Notes ① through ⑦ are on page 11

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	150	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.18	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.090	Ω	V_{GS} = 10V, I_D = 14A ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.5	V	V_{DS} = V_{GS}, I_D = 250μA
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V_{DS} = 150V, V_{GS} = 0V
		—	—	250		V_{DS} = 120V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 30V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -30V

Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	11	—	—	S	V_{DS} = 25V, I_D = 14A
Q_g	Total Gate Charge	—	37	56	nC	I_D = 14A
Q_{gs}	Gate-to-Source Charge	—	9.6	14		V_{DS} = 120V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	19	29		V_{GS} = 10V, ④
$t_{d(on)}$	Turn-On Delay Time	—	10	—	ns	V_{DD} = 75V
t_r	Rise Time	—	32	—		I_D = 14A
$t_{d(off)}$	Turn-Off Delay Time	—	18	—		R_G = 5.1Ω
t_f	Fall Time	—	8.4	—		V_{GS} = 10V ④
C_{iss}	Input Capacitance	—	1200	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	260	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	65	—		f = 1.0MHz⑥
C_{oss}	Output Capacitance	—	1520	—		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	—	120	—		V_{GS} = 0V, V_{DS} = 120V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	—	210	—		V_{GS} = 0V, V_{DS} = 0V to 120V ⑤

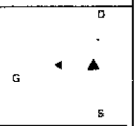
Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	260	mJ
I_{AR}	Avalanche Current①	—	14	A
E_{AR}	Repetitive Avalanche Energy①	—	13.6	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.1	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface ⑥	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient⑥	—	62	
$R_{\theta JA}$	Junction-to-Ambient⑦	—	40	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	23	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	92		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 14A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	150	220	ns	T_J = 25°C, I_F = 14A
Q_{rr}	Reverse RecoveryCharge	—	0.8	1.2	μC	di/dt = 100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

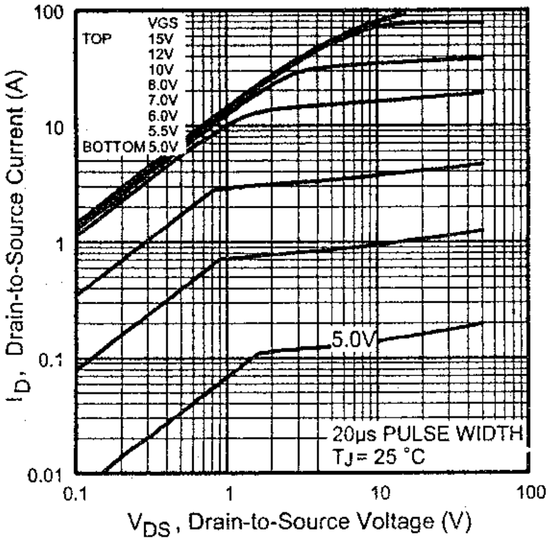


Fig 1. Typical Output Characteristics

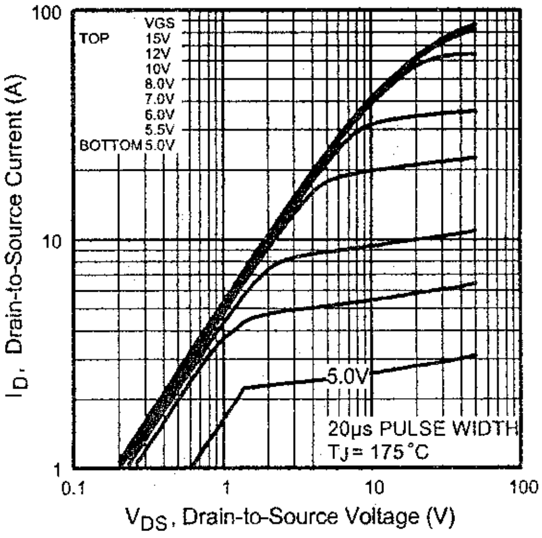


Fig 2. Typical Output Characteristics

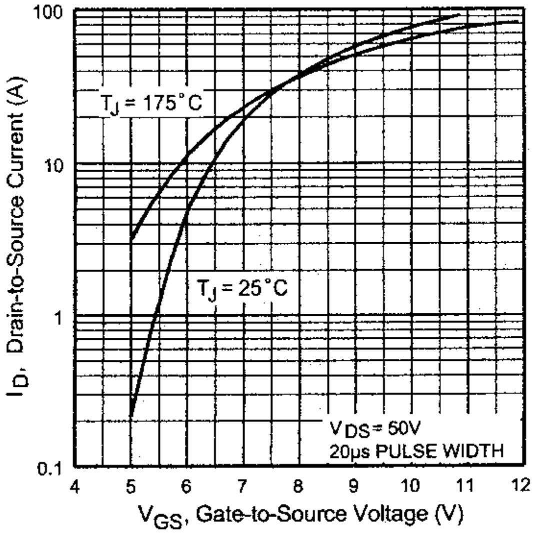


Fig 3. Typical Transfer Characteristics

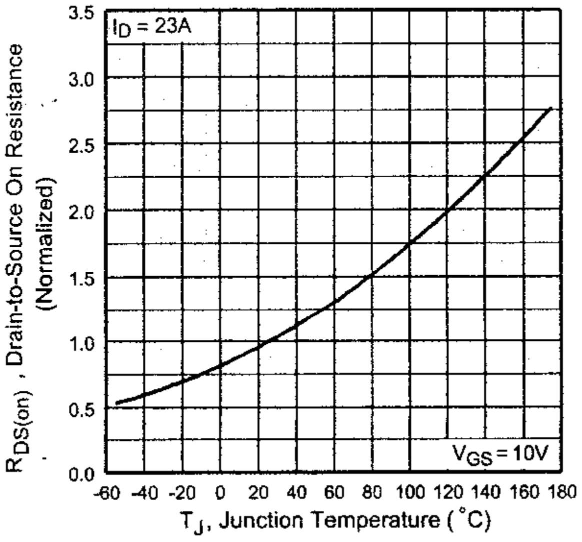


Fig 4. Normalized On-Resistance
Vs. Temperature

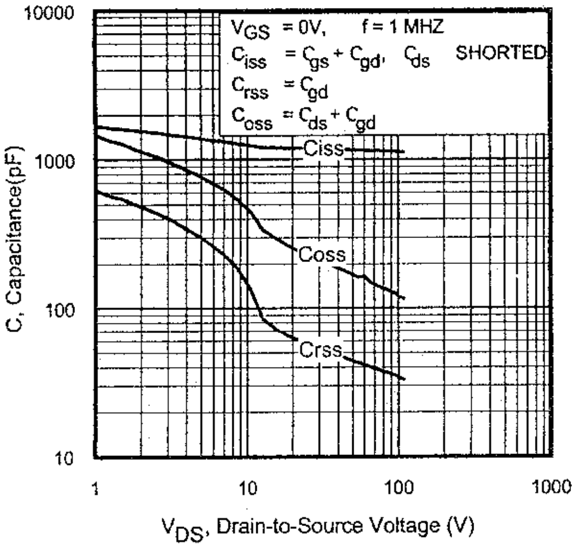


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

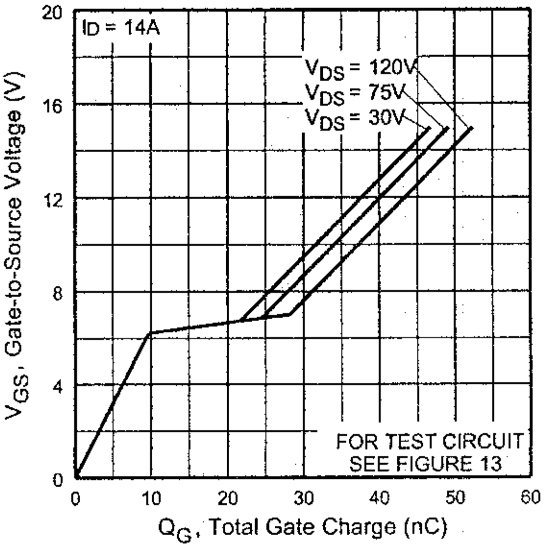


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

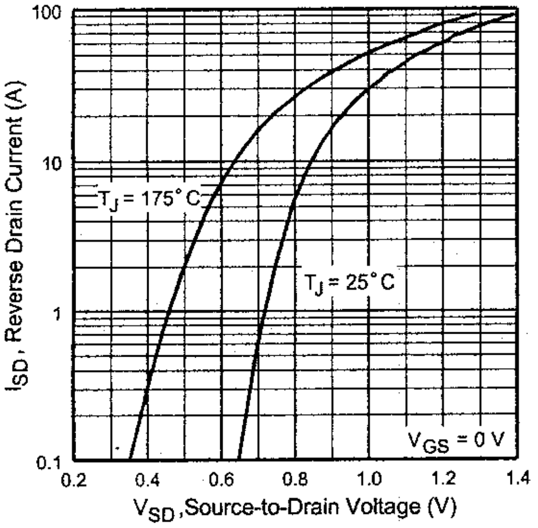


Fig 7. Typical Source-Drain Diode Forward Voltage

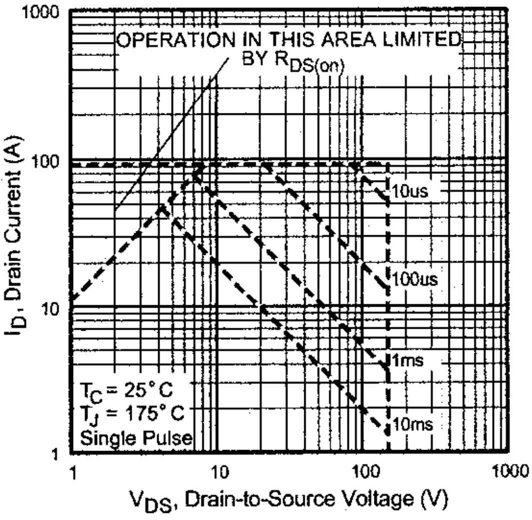


Fig 8. Maximum Safe Operating Area

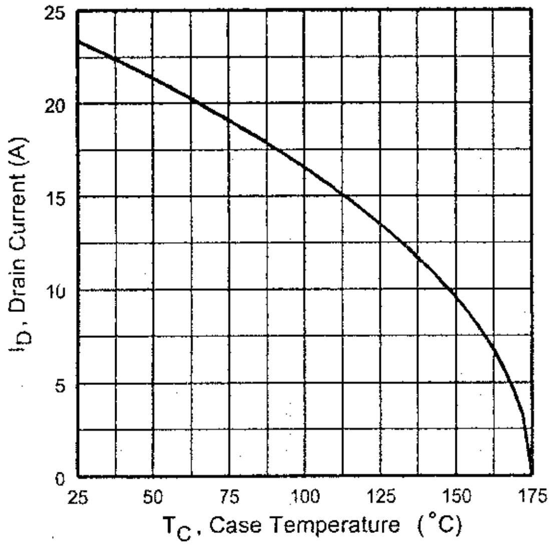


Fig 9. Maximum Drain Current Vs. Case Temperature

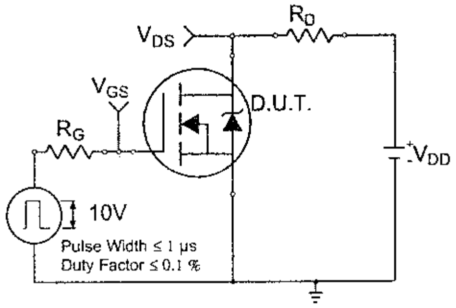


Fig 10a. Switching Time Test Circuit

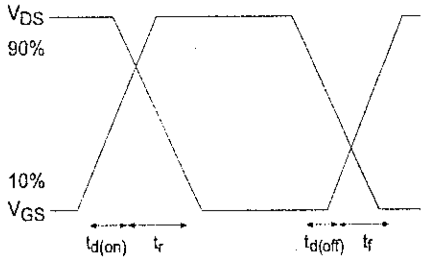
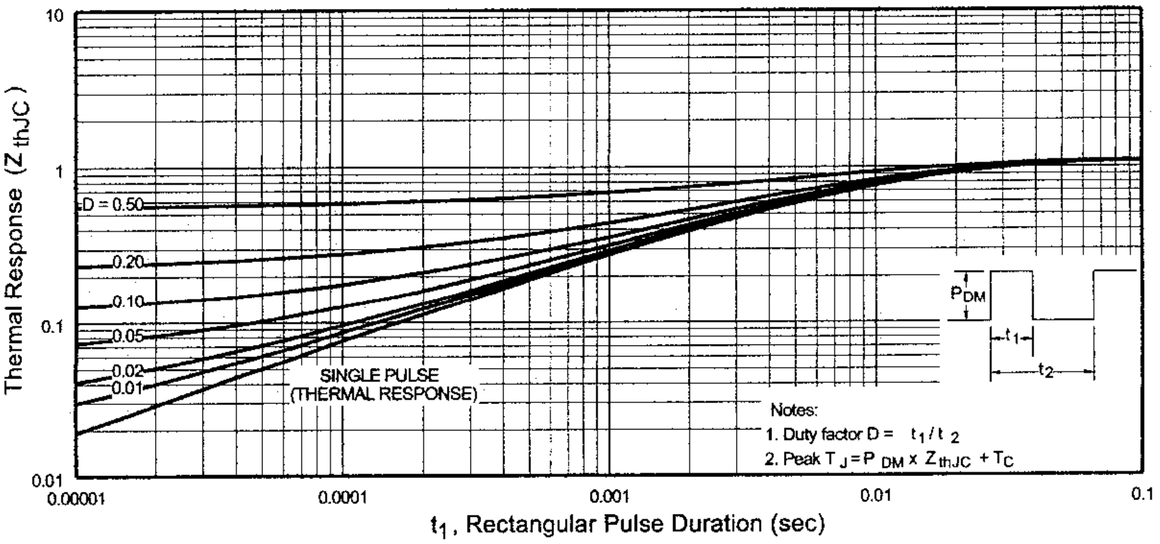


Fig 10b. Switching Time Waveforms



Notes:
1. Duty factor D = t_1 / t_2
2. Peak $T_J = P_{DM} \times Z_{thJC} + T_C$

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

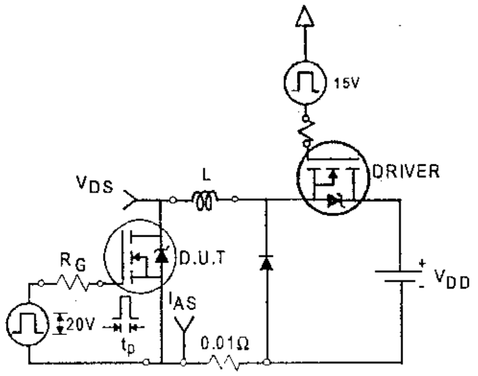


Fig 12a. Unclamped Inductive Test Circuit

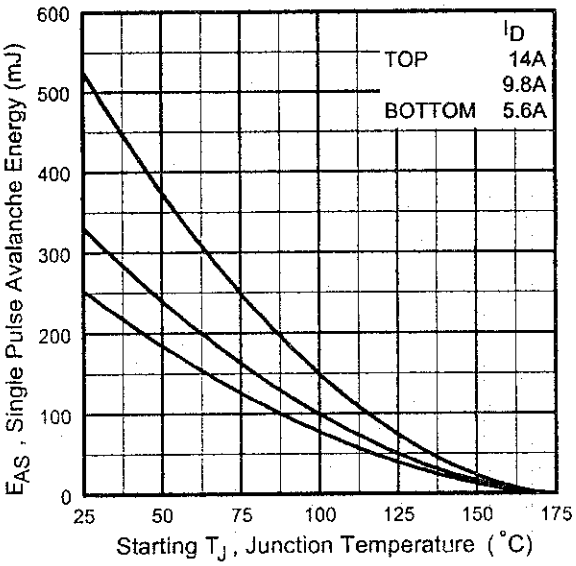


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

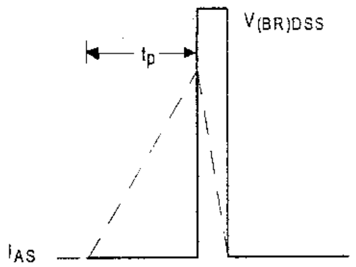


Fig 12b. Unclamped Inductive Waveforms

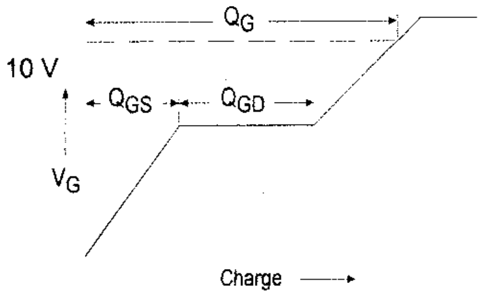


Fig 13a. Basic Gate Charge Waveform

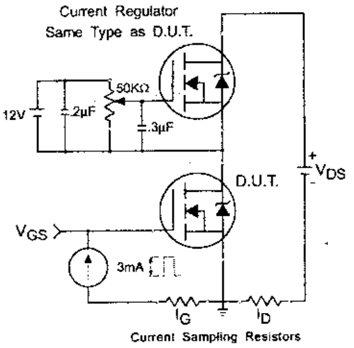
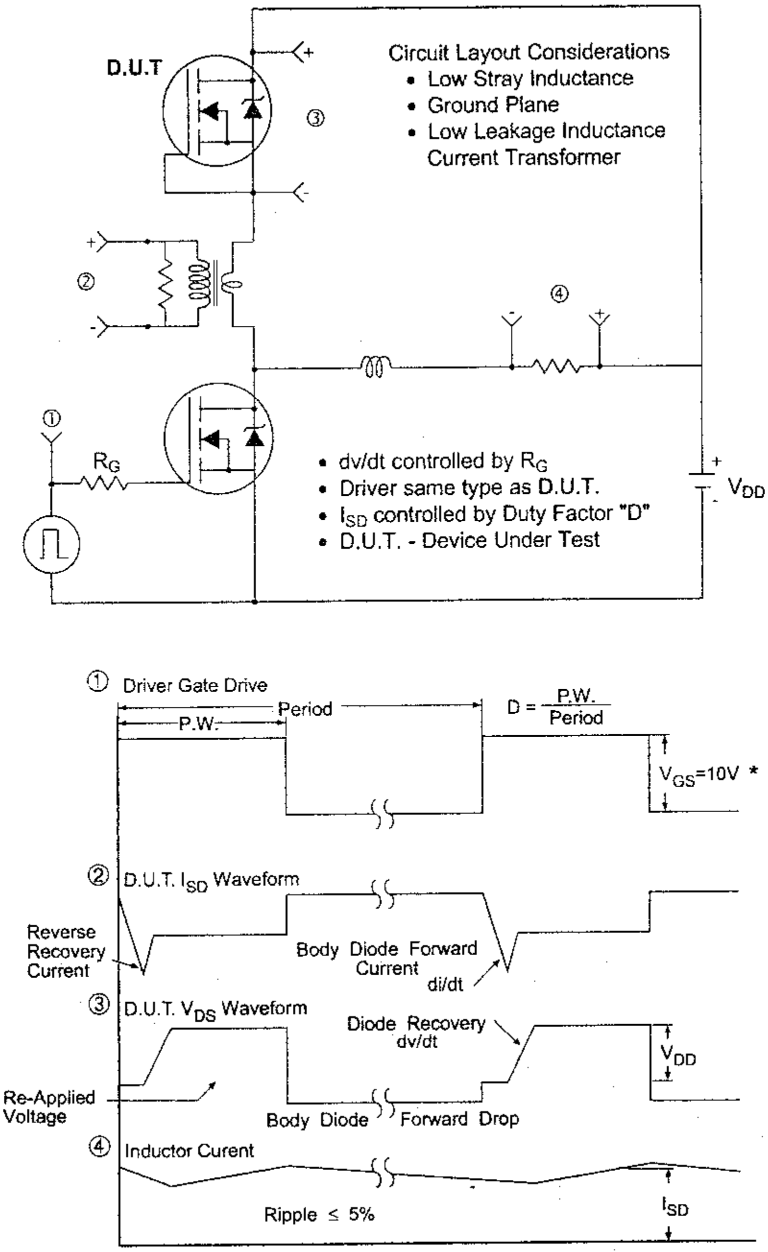


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit

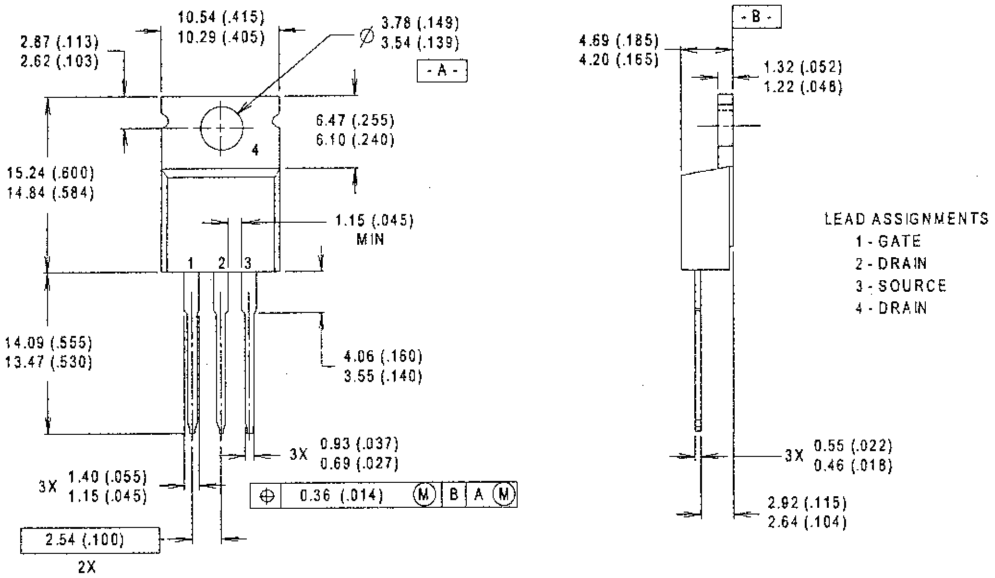


* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETs

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



LEAD ASSIGNMENTS
- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE
- 4 - DRAIN

NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.

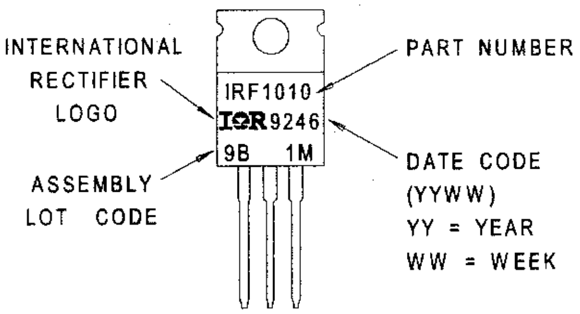
2 CONTROLLING DIMENSION : INCH

3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.

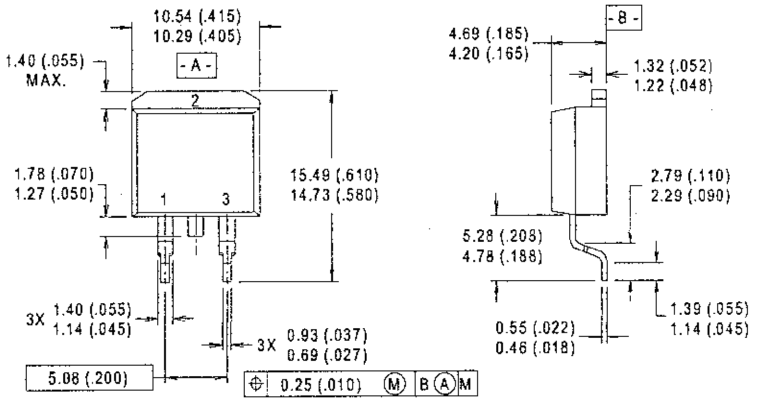
4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

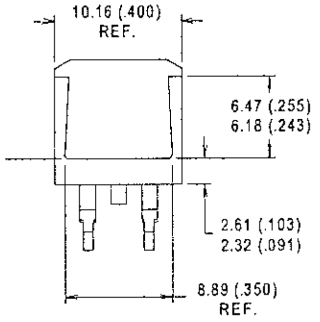
TO-220AB Part Marking Information

EXAMPLE : THIS IS AN IRF1010
WITH ASSEMBLY
LOT CODE 9B1M



D^{2}Pak Package Outline



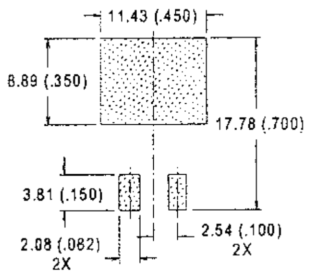


NOTES:

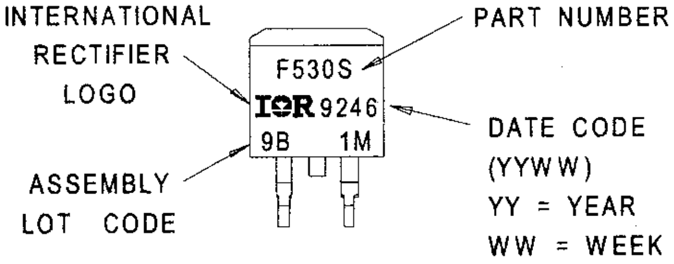
1 DIMENSIONS AFTER SOLDER DIP.
2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
3 CONTROLLING DIMENSION : INCH.
4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE

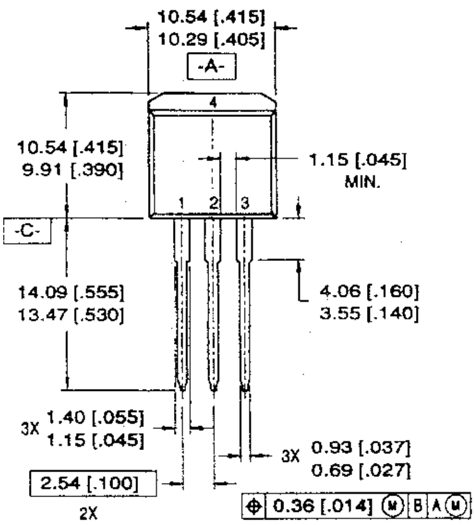
MINIMUM RECOMMENDED FOOTPRINT

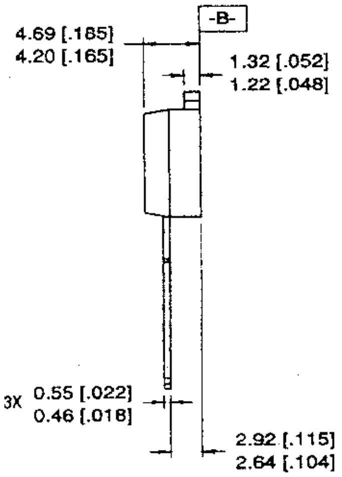


D^{2}Pak Part Marking Information



TO-262 Package Outline





LEAD ASSIGNMENTS

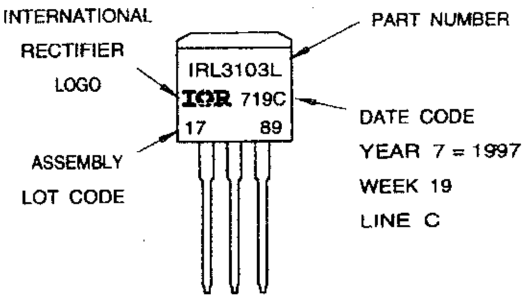
1 = GATE
2 = DRAIN
3 = SOURCE
4 = DRAIN

NOTES:

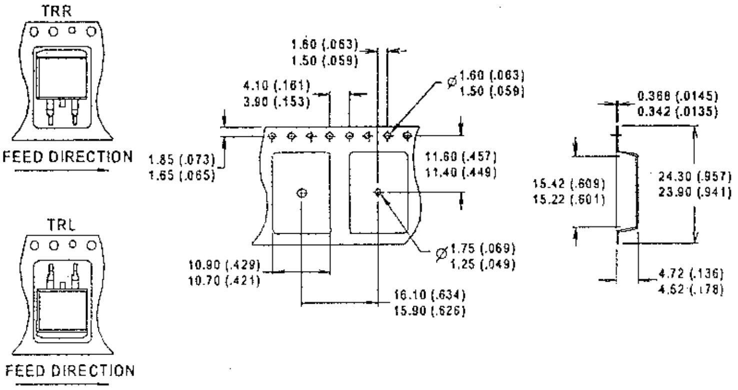
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

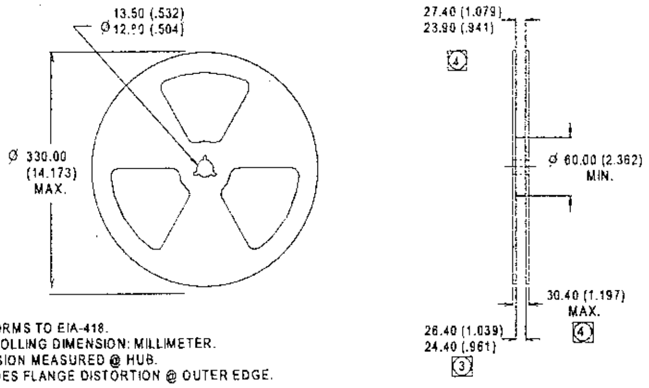
TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



D^2Pak Tape & Reel Information





NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3 DIMENSION MEASURED @ HUB.
4 INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting $T_J = 25°C$, $L = 2.7mH$
$R_G = 25\Omega$, $I_{AS} = 14A$.

③ $I_{SD} \leq 14A$, $di/dt \leq 240A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$,
$T_J \leq 175°C$

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

⑥ This is only applied to TO-220AB package

⑦ This is applied to D^2Pak, when mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR EUROPEAN REGIONAL CENTER: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN: 16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936

UNITRODE

UC1825
UC2825
UC3825

ligh Speed PWM Controller

EATURES

- Compatible with Voltage or Current Mode Topologies
- Practical Operation Switching Frequencies to 1MHz
- 50ns Propagation Delay to Output
- High Current Dual Totem Pole Outputs (1.5A Peak)
- Wide Bandwidth Error Amplifier
- Fully Latched Logic with Double Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Soft Start / Max. Duty Cycle Control
- Under-Voltage Lockout with Hysteresis
- Low Start Up Current (1.1mA)
- Trimmed Bandgap Reference (5.1V ±1%)

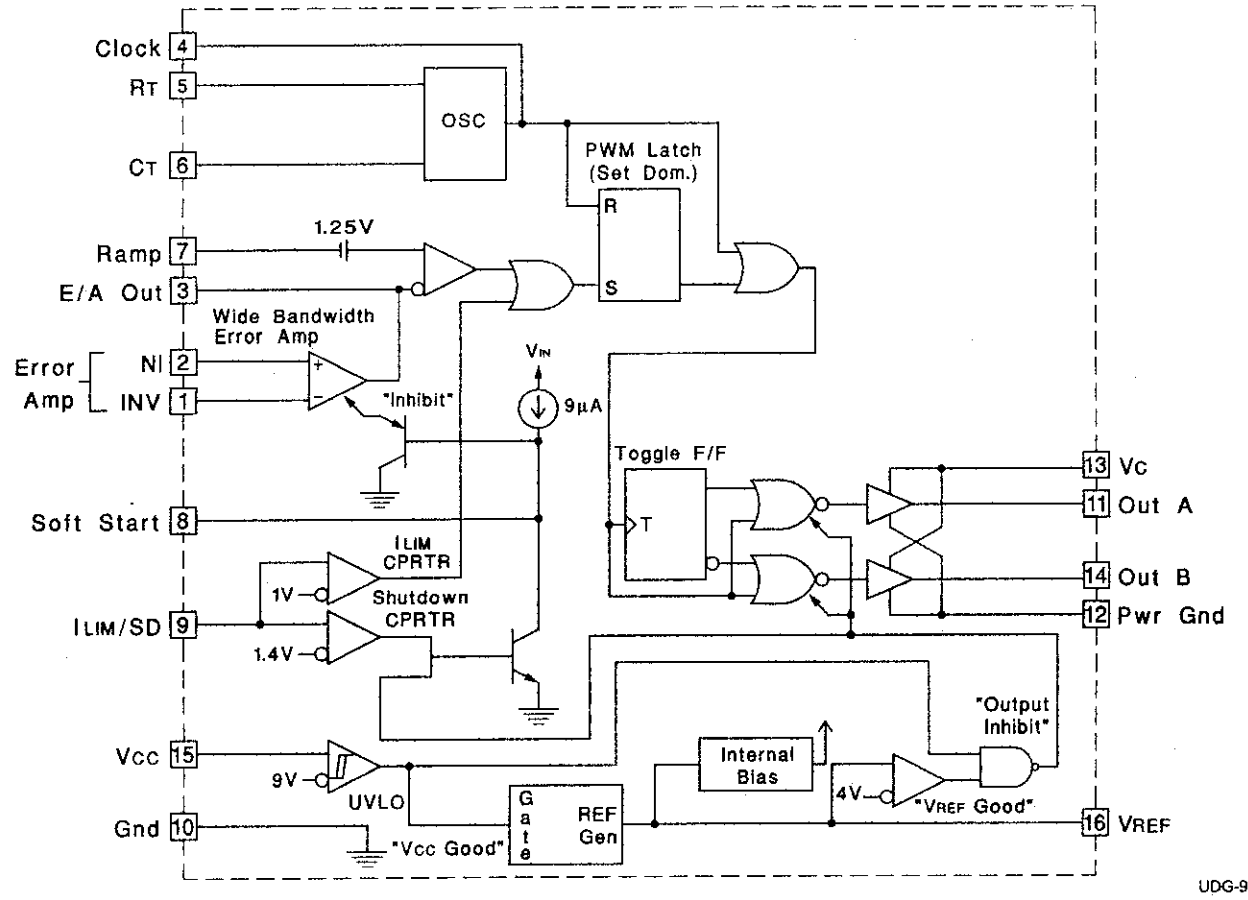
DESCRIPTION

The UC1825 family of PWM control ICs is optimized for high frequency switched mode power supply applications. Particular care was given to minimizing propagation delays through the comparators and logic circuitry while maximizing bandwidth and slew rate of the error amplifier. This controller is designed for use in either current-mode or voltage mode systems with the capability for input voltage feed-forward.

Protection circuitry includes a current limit comparator with a 1V threshold, a TTL compatible shutdown port, and a soft start pin which will double as a maximum duty cycle clamp. The logic is fully latched to provide jitter free operation and prohibit multiple pulses at an output. An under-voltage lockout section with 800mV of hysteresis assures low start up current. During under-voltage lockout, the outputs are high impedance.

These devices feature totem pole outputs designed to source and sink high peak currents from capacitive loads, such as the gate of a power MOSFET. The on state is designed as a high level.

LOCK DIAGRAM



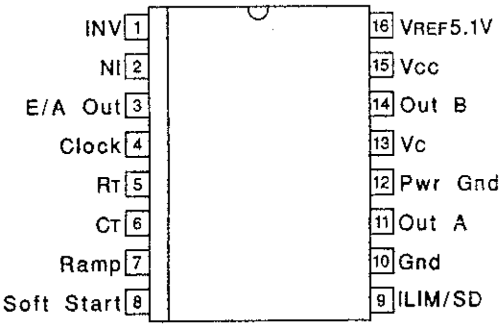
UDG-92030-2

BSOLUTE MAXIMUM RATINGS (Note 1)

ıpply Voltage (Pins 13, 15) 30V
ıtput Current, Source or Sink (Pins 11, 14)
. . . . 0.5A
ılse (0.5µs) 2.0A
ıalog Inputs
ins 1, 2, 7) . . . . -0.3V to 7V
in 8, 9) . . . . -0.3V to 6V
ock Output Current (Pin 4) . . . . -5mA
ror Amplifier Output Current (Pin 3) 5mA
ıft Start Sink Current (Pin 8) 20mA
scillator Charging Current (Pin 5) . . . . -5mA
ıwer Dissipation 1W
orage Temperature Range . . . . -65°C to +150°C
ad Temperature (Soldering, 10 seconds) . . . . 300°C

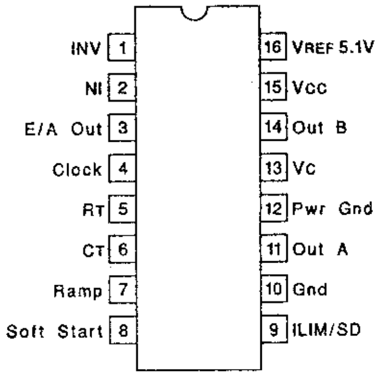
ıte 1: All voltages are with respect to GND (Pin 10); all currents are positive into, negative out of part; pin numbers refer to L-16 package.
ıte 3: Consult Unitrode Integrated Circuit Databook for thermal limitations and considerations of package.

OIC-16 (Top View)
W Package

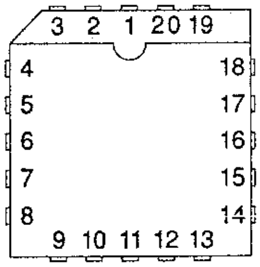


CONNECTION DIAGRAMS

DIL-16 (Top View)
J Or N Package



PLCC-20 & LCC-20
(Top View)
Q & L Packages



PACKAGE PIN FUNCTION	
FUNCTION	**PIN**
N/C	1
INV	2
NI	3
E/A Out	4
Clock	5
N/C	6
RT	7
CT	8
Ramp	9
Soft Start	10
N/C	11
ILIM/SD	12
Gnd	13
Out A	14
Pwr Gnd	15
N/C	16
Vc	17
Out B	18
Vcc	19
VREF 5.1V	20

LECTRICAL CHARACTERISTICS: Unless otherwise stated,these specifications apply for , $R_T = 3.65k$, $C_T = 1nF$, $V_{CC} = 15V$, $-55°C<T_A<125°C$ for the UC1825, $-40°C<T_A<85°C$ for the UC2825, and $0°C<T_A<70°C$ for the UC3825, $T_A=T_J$.

PARAMETERS	TEST CONDITIONS	UC1825 UC2825			UC3825			
		MIN	TYP	MAX	MIN	TYP	MAX	UNITS
eference Section								
Output Voltage	T_J = 25°C, Io = 1mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	10V < Vcc < 30V		2	20		2	20	mV
Load Regulation	1mA < Io < 10mA		5	20		5	20	mV
Temperature Stability*	TMIN < TA < TMAX		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation*	Line, Load, Temperature	5.00		5.20	4.95		5.25	V
Output Noise Voltage*	10Hz < f < 10kHz		50			50		µV
Long Term Stability*	T_J = 125°C, 1000hrs.		5	25		5	25	mV
Short Circuit Current	VREF = 0V	-15	-50	-100	-15	-50	-100	mA
scillator Section								
Initial Accuracy*	T_J = 25°C	360	400	440	360	400	440	kHz
Voltage Stability*	10V < Vcc < 30V		0.2	2		0.2	2	%
Temperature Stability*	TMIN < TA < TMAX		5			5		%
Total Variation*	Line, Temperature	340		460	340		460	kHz

.ECTRICAL CHARACTERISTICS ont.)

Unless otherwise stated,these specifications apply for , R_T = 3.65k, C_T = 1nF, V_{CC} = 15V, -55°C<T_A<125°C for the UC1825, –40°C<T_A<85°C for the UC2825, and 0°C<T_A<70°C for the UC3825, T_A=T_J.

PARAMETERS	TEST CONDITIONS	UC1825 UC2825			UC3825			
		MIN	TYP	MAX	MIN	TYP	MAX	UNITS
scillator Section (cont.)								
Clock Out High		3.9	4.5		3.9	4.5		V
Clock Out Low			2.3	2.9		2.3	2.9	V
Ramp Peak*		2.6	2.8	3.0	2.6	2.8	3.0	V
Ramp Valley*		0.7	1.0	1.25	0.7	1.0	1.25	V
Ramp Valley to Peak*		1.6	1.8	2.0	1.6	1.8	2.0	V
rror Amplifier Section								
Input Offset Voltage				10			15	mV
Input Bias Current			0.6	3		0.6	3	µA
Input Offset Current			0.1	1		0.1	1	µA
Open Loop Gain	1V < V_O < 4V	60	95		60	95		dB
CMRR	1.5V < V_{CM} < 5.5V	75	95		75	95		dB
PSRR	10V < V_{CC} < 30V	85	110		85	110		dB
Output Sink Current	$V_{PIN\ 3}$ = 1V	1	2.5		1	2.5		mA
Output Source Current	$V_{PIN\ 3}$ = 4V	-0.5	-1.3		-0.5	-1.3		mA
Output High Voltage	$I_{PIN\ 3}$ = -0.5mA	4.0	4.7	5.0	4.0	4.7	5.0	V
Output Low Voltage	$I_{PIN\ 3}$ = 1mA	0	0 .5	1.0	0	0.5	1.0	V
Unity Gain Bandwidth*		3	5.5		3	5.5		MHz
Slew Rate*		6	12		6	12		V/µs
WM Comparator Section								
Pin 7 Bias Current	$V_{PIN\ 7}$ = 0V		-1	-5		-1	-5	µA
Duty Cycle Range		0		80	0		85	%
Pin 3 Zero DC Threshold	$V_{PIN\ 7}$ = 0V	1.1	1.25		1.1	1.25		V
Delay to Output*			50	80		50	80	ns
oft-Start Section								
Charge Current	$V_{PIN\ 8}$ = 0.5V	3	9	20	3	9	20	µA
Discharge Current	$V_{PIN\ 8}$ = 1V	1			1			mA
urrent Limit / Shutdown Section								
Pin 9 Bias Current	0 < $V_{PIN\ 9}$ < 4V			15			10	µA
Current Limit Threshold		0.9	1.0	1.1	0.9	1.0	1.1	V
Shutdown Threshold		1.25	1.40	1.55	1.25	1.40	1.55	V
Delay to Output			50	80		50	80	ns
utput Section								
Output Low Level	I_{OUT} = 20mA		0.25	0.40		0.25	0.40	V
	I_{OUT} = 200mA		1.2	2.2		1.2	2.2	V
Output High Level	I_{OUT} = -20mA	13.0	13.5		13.0	13.5		V
	I_{OUT} = -200mA	12.0	13.0		12.0	13.0		V
Collector Leakage	V_C = 30V		100	500		10	500	µA
Rise/Fall Time*	CL = 1nF		30	60		30	60	ns
nder-Voltage Lockout Section								
Start Threshold		8.8	9.2	9.6	8.8	9.2	9.6	V
UVLO Hysteresis		0.4	0.8	1.2	0.4	0.8	1.2	V
upply Current Section								
Start Up Current	V_{CC} = 8V		1.1	2.5		1.1	2.5	mA
ICC	$V_{PIN\ 1}$, $V_{PIN\ 7}$, $V_{PIN\ 9}$ = 0V; $V_{PIN\ 2}$ = 1V		22	33		22	33	mA

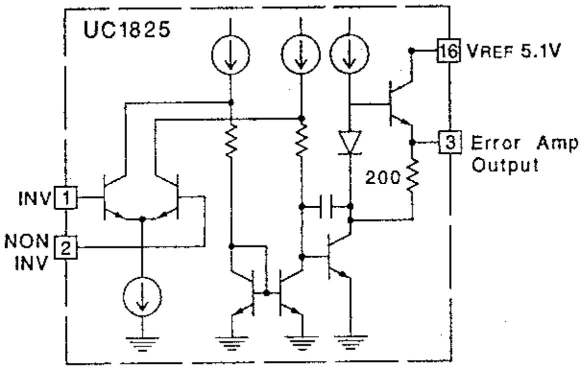
This parameter not 100% tested in production but guaranteed by design.

inted Circuit Board Layout Considerations

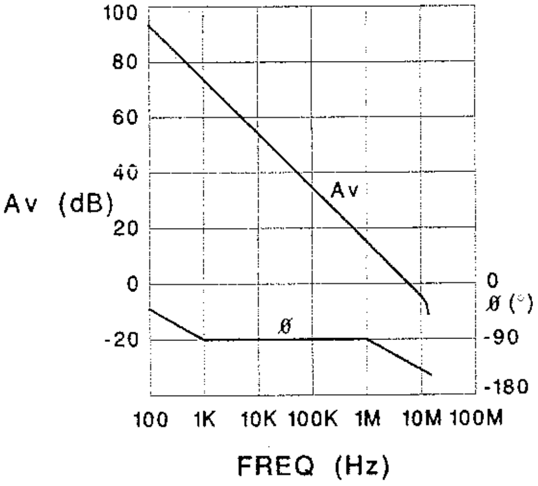
ɟh speed circuits demand careful attention to layout d component placement. To assure proper performance the UC1825 follow these rules: 1) Use a ground plane. Damp or clamp parasitic inductive kick energy from the te of driven MOSFETs. Do not allow the output pins to g below ground. A series gate resistor or a shunt 1 Amp Schottky diode at the output pin will serve this purpose. 3) Bypass VCC, VC, and VREF. Use 0.1µF monolithic ceramic capacitors with low equivalent series inductance. Allow less than 1 cm of total lead length for each capacitor between the bypassed pin and the ground plane. 4) Treat the timing capacitor, CT, like a bypass capacitor.

ror Amplifier Circuit

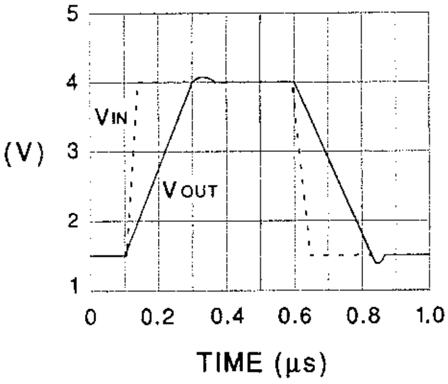
Simplified Schematic



Open Loop Frequency Response

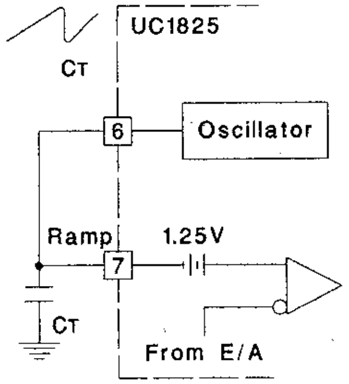


Unity Gain Slew Rate

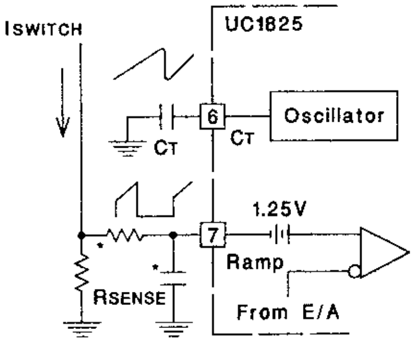


VM Applications

Conventional (Voltage Mode)

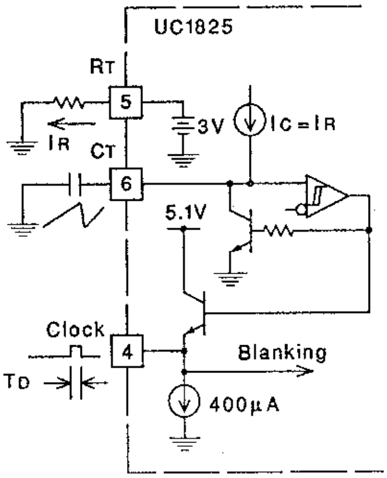


Current-Mode

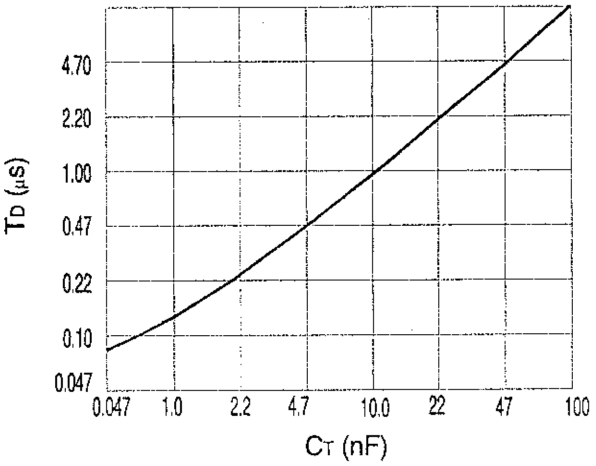


* A small filter may be required to suppress switch noise.

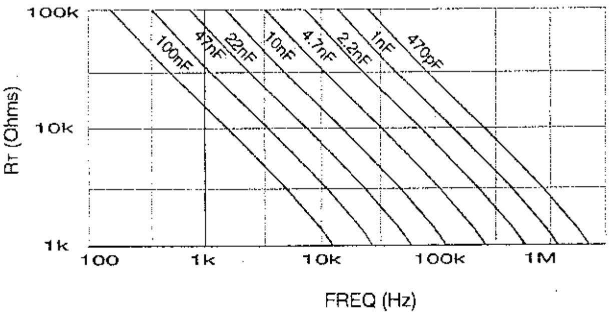
scillator Circuit



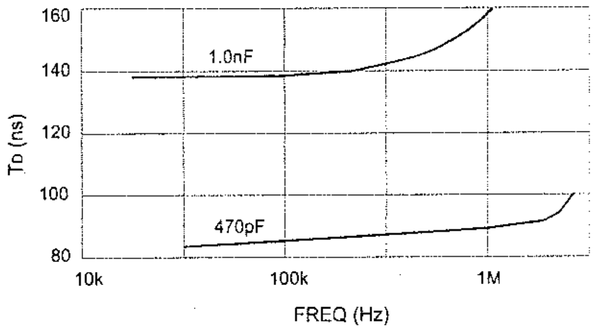
Deadtime vs CT (3k ≤ RT ≤ 100k)



Timing Resistance vs Frequency

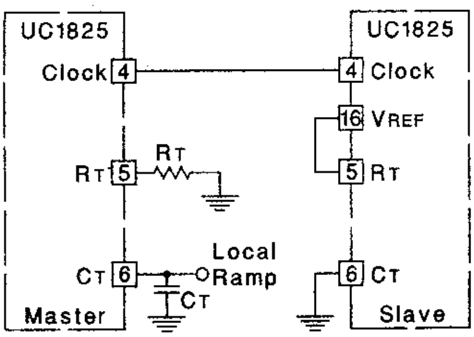


Deadtime vs Frequency

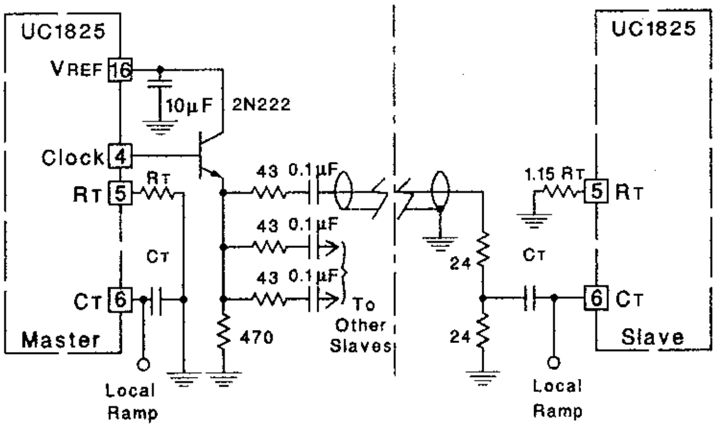


nchronized Operation

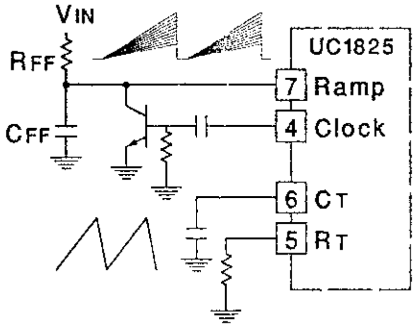
Two Units in Close Proximity



Generalized Synchronization

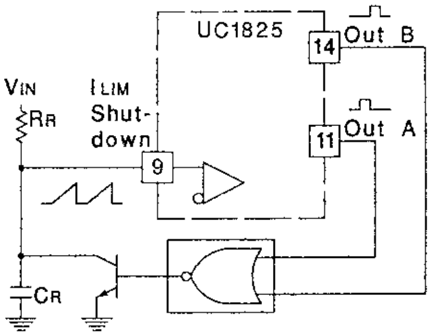


orward Technique for Off-Line Voltage Mode Application



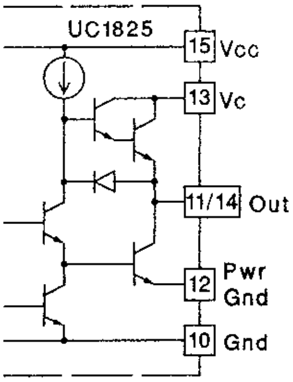
onstant Volt-Second Clamp Circuit

The circuit shown here will achieve a constant volt-second product clamp over varying input voltages. The ramp generator components, RT and CR are chosen so that the ramp at Pin 9 crosses the 1V threshold at the same time the desired maximum volt-second product is reached. The delay through the functional nor block must be such that the ramp capacitor can be completely discharged during the minimum deadtime.

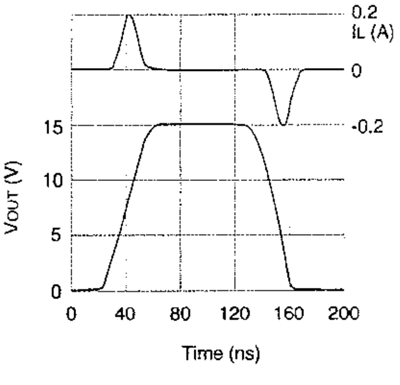


utput Section

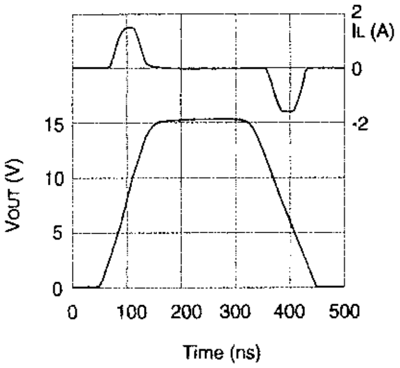
Simplified Schematic



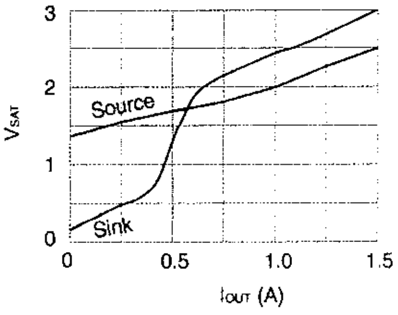
Rise/Fall Time (CL=1nF)



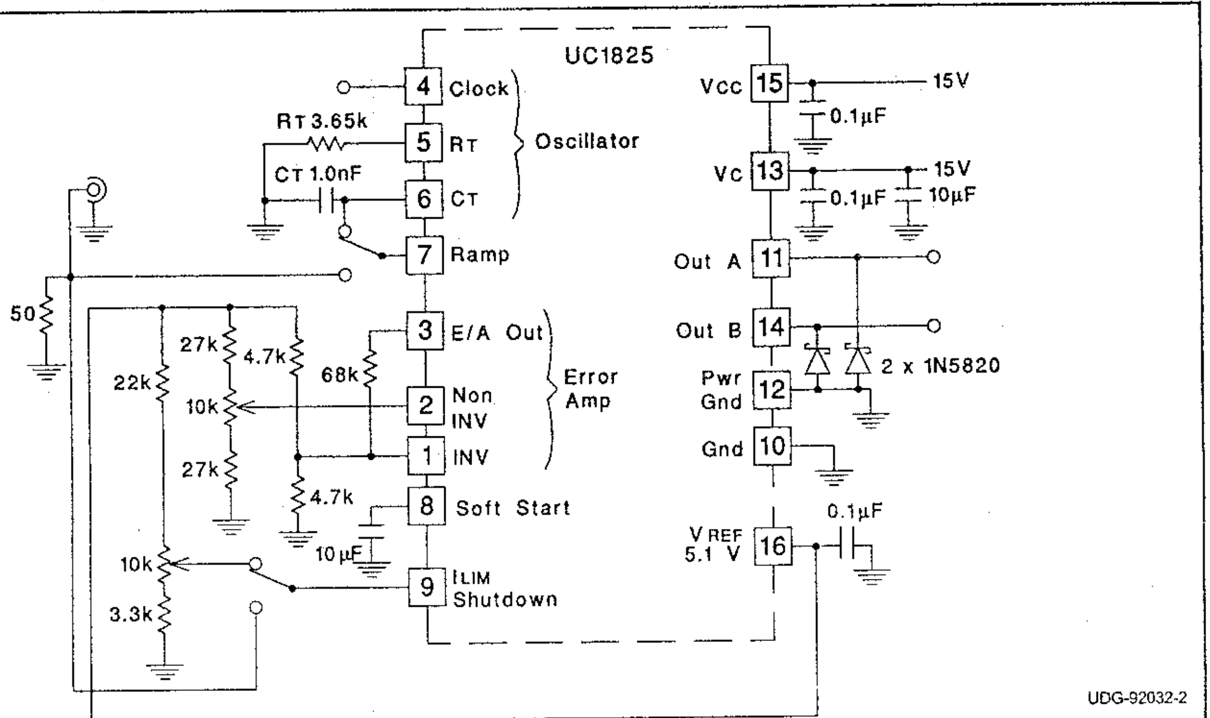
Rise/Fall Time (CL=10nF)



Saturation Curves



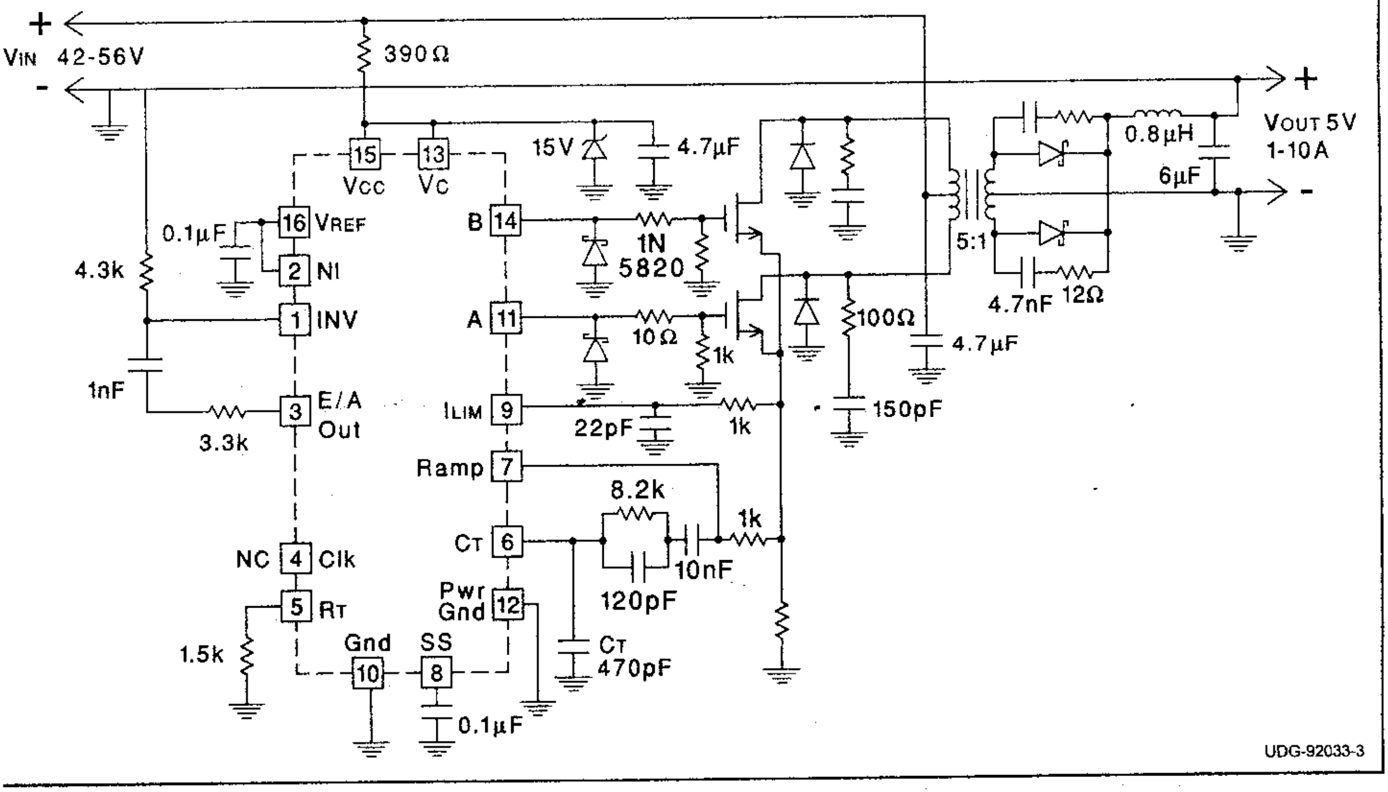
en Loop Laboratory Test Fixture



This test fixture is useful for exercising many of the UC1825's functions and measuring their specifications.

As with any wideband circuit, careful grounding and bypass procedures should be followed. The use of a ground plane is highly recommended.

esign Example: 50W, 48V to 5V DC to DC Converter - 1.5MHz Clock Frequency



intersil

ICL8038

Data Sheet | **September 1998** | **File Number 2864.3**

recision Waveform Generator/Voltage ontrolled Oscillator

e ICL8038 waveform generator is a monolithic integrated cuit capable of producing high accuracy sine, square, angular, sawtooth and pulse waveforms with a minimum of ternal components. The frequency (or repetition rate) can selected externally from 0.001Hz to more than 300kHz ing either resistors or capacitors, and frequency odulation and sweeping can be accomplished with an ternal voltage. The ICL8038 is fabricated with advanced onolithic technology, using Schottky barrier diodes and thin n resistors, and the output is stable over a wide range of nperature and supply variations. These devices may be erfaced with phase locked loop circuitry to reduce nperature drift to less than 250ppm/°C.

Features

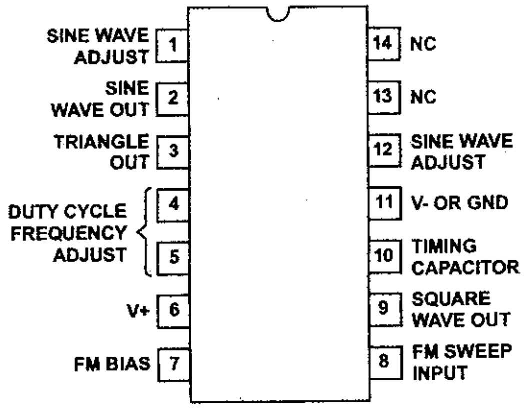
- Low Frequency Drift with Temperature . . . . . . 250ppm/°C
- Low Distortion. . . . . 1% (Sine Wave Output)
- High Linearity . . . . 0.1% (Triangle Wave Output)
- Wide Frequency Range . . . . 0.001Hz to 300kHz
- Variable Duty Cycle . . . . 2% to 98%
- High Level Outputs. . . . . TTL to 28V
- Simultaneous Sine, Square, and Triangle Wave Outputs
- Easy to Use - Just a Handful of External Components Required

rdering Information

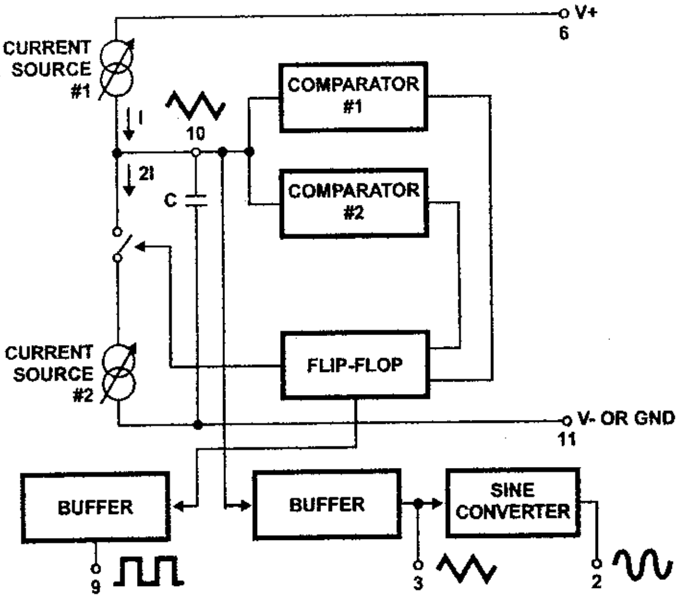
PART NUMBER	STABILITY	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
L8038CCPD	250ppm/°C (Typ)	0 to 70	14 Ld PDIP	E14.3
L8038CCJD	250ppm/°C (Typ)	0 to 70	14 Ld CERDIP	F14.3
L8038BCJD	180ppm/°C (Typ)	0 to 70	14 Ld CERDIP	F14.3
L8038ACJD	120ppm/°C (Typ)	0 to 70	14 Ld CERDIP	F14.3

inout

ICL8038
(PDIP, CERDIP)
TOP VIEW



Functional Diagram



solute Maximum Ratings

pply Voltage (V- to V+) 36V
ut Voltage (Any Pin) . . . . V- to V+
ut Current (Pins 4 and 5). 25mA
tput Sink Current (Pins 3 and 9) 25mA

erating Conditions

nperature Range
CL8038AC, ICL8038BC, ICL8038CC . . . . 0°C to 70°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	75	20
PDIP Package	115	N/A

Maximum Junction Temperature (Ceramic Package) . . . . .175°C
Maximum Junction Temperature (Plastic Package) . . . . .150°C
Maximum Storage Temperature Range . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C

Die Characteristics

Back Side Potential . . . . V-

UTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the ice at these or any other conditions above those indicated in the operational sections of this specification is not implied.

TE:

. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

ectrical Specifications

V_{SUPPLY} = ±10V or +20V, T_A = 25°C, R_L = 10kΩ, Test Circuit Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	ICL8038CC			ICL8038BC			ICL8038AC			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
upply Voltage Operating Range	V_{SUPPLY} V+	Single Supply	+10	-	+30	+10	-	+30	+10	-	+30	V
	V+, V-	Dual Supplies	±5	-	±15	±5	-	±15	±5	-	±15	V
upply Current	I_{SUPPLY}	V_{SUPPLY} = ±10V (Note 2)		12	20	-	12	20	-	12	20	mA
REQUENCY CHARACTERISTICS (All Waveforms)												
ax. Frequency of Oscillation	f_{MAX}		100	-	-	100	-	-	100	-	-	kHz
weep Frequency of FM Input	f_{SWEEP}		-	10	-	-	10	-	-	10	-	kHz
weep FM Range		(Note 3)	-	35:1	-	-	35:1	-	-	35:1	-	
M Linearity		10:1 Ratio	-	0.5	-	-	0.2	-	-	0.2	-	%
requency Drift with emperature (Note 5)	$\Delta f/\Delta T$	0°C to 70°C	-	250	-	-	180	-	-	120		ppm/°C
requency Drift with Supply Voltage	$\Delta f/\Delta V$	Over Supply Voltage Range	-	0.05	-	-	0.05		-	0.05	-	%/V
UTPUT CHARACTERISTICS												
quare Wave												
Leakage Current	I_{OLK}	V_9 = 30V	-	-	1	-	-	1	-	-	1	µA
Saturation Voltage	V_{SAT}	I_{SINK} = 2mA	-	0.2	0.5	-	0.2	0.4	-	0.2	0.4	V
Rise Time	t_R	R_L = 4.7kΩ	-	180	-	-	180	-	-	180	-	ns
Fall Time	t_F	R_L = 4.7kΩ	-	40	-	-	40	-	-	40	-	ns
Typical Duty Cycle Adjust (Note 6)	ΔD		2		98	2	-	98	2	-	98	%
riangle/Sawtooth/Ramp												-
Amplitude	$V_{TRIANGLE}$	R_{TRI} = 100kΩ	0.30	0.33	-	0.30	0.33	-	0.30	0.33	-	xV_{SUPPLY}
Linearity			-	0.1	-	-	0.05	-	-	0.05	-	%
Output Impedance	Z_{OUT}	I_{OUT} = 5mA	-	200	-	-	200	-	-	200	-	Ω

lectrical Specifications

V_{SUPPLY} = ±10V or +20V, T_A = 25°C, R_L = 10kΩ, Test Circuit Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	ICL8038CC			ICL8038BC			ICL8038AC			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
ine Wave												
Amplitude	V_{SINE}	R_{SINE} = 100kΩ	0.2	0.22	-	0.2	0.22	-	0.2	0.22	-	xV_{SUPPLY}
THD	THD	R_S = 1MΩ (Note 4)	-	2.0	5	-	1.5	3	-	1.0	1.5	%
THD Adjusted	THD	Use Figure 4	-	1.5	-	-	1.0	-	-	0.8	-	%

ΟTES:

. R_A and R_B currents not included.

. V_{SUPPLY} = 20V; R_A and R_B = 10kΩ, f ≅ 10kHz nominal; can be extended 1000 to 1. See Figures 5A and 5B.

. 82kΩ connected between pins 11 and 12, Triangle Duty Cycle set at 50%. (Use R_A and R_B.)

. Figure 1, pins 7 and 8 connected, V_{SUPPLY} = ±10V. See Typical Curves for T.C. vs V_{SUPPLY}.

. Not tested, typical value for design purposes only.

əst Conditions

PARAMETER	R_A	R_B	R_L	C	SW_1	MEASURE
upply Current	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Current Into Pin 6
weep FM Range (Note 7)	10kΩ	10kΩ	10kΩ	3.3nF	Open	Frequency at Pin 9
requency Drift with Temperature	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Frequency at Pin 3
requency Drift with Supply Voltage (Note 8)	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Frequency at Pin 9
ıutput Amplitude (Note 10)						
Sine	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Pk-Pk Output at Pin 2
Triangle	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Pk-Pk Output at Pin 3
eakage Current (Off) (Note 9)	10kΩ	10kΩ		3.3nF	Closed	Current into Pin 9
aturation Voltage (On) (Note 9)	10kΩ	10kΩ		3.3nF	Closed	Output (Low) at Pin 9
ise and Fall Times (Note 11)	10kΩ	10kΩ	4.7kΩ	3.3nF	Closed	Waveform at Pin 9
uty Cycle Adjust (Note 11)						
Max	50kΩ	~1.6kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 9
Min	~25kΩ	50kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 9
riangle Waveform Linearity	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 3
otal Harmonic Distortion	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 2

ΟTES:

. The hi and lo frequencies can be obtained by connecting pin 8 to pin 7 (f_{HI}) and then connecting pin 8 to pin 6 (f_{LO}). Otherwise apply Sweep Voltage at pin 8 ($^2/_3$ V_{SUPPLY} +2V) ≤ V_{SWEEP} ≤ V_{SUPPLY} where V_{SUPPLY} is the total supply voltage. In Figure 5B, pin 8 should vary between 5.3V and 10V with respect to ground.

. 10V ≤ V+ ≤ 30V, or ±5V ≤ V_{SUPPLY} ≤ ±15V.

. Oscillation can be halted by forcing pin 10 to +5V or -5V.

. Output Amplitude is tested under static conditions by forcing pin 10 to 5V then to -5V.

. Not tested; for design purposes only.

est Circuit

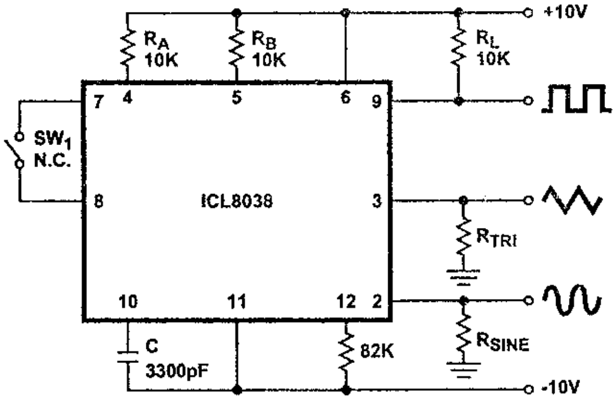
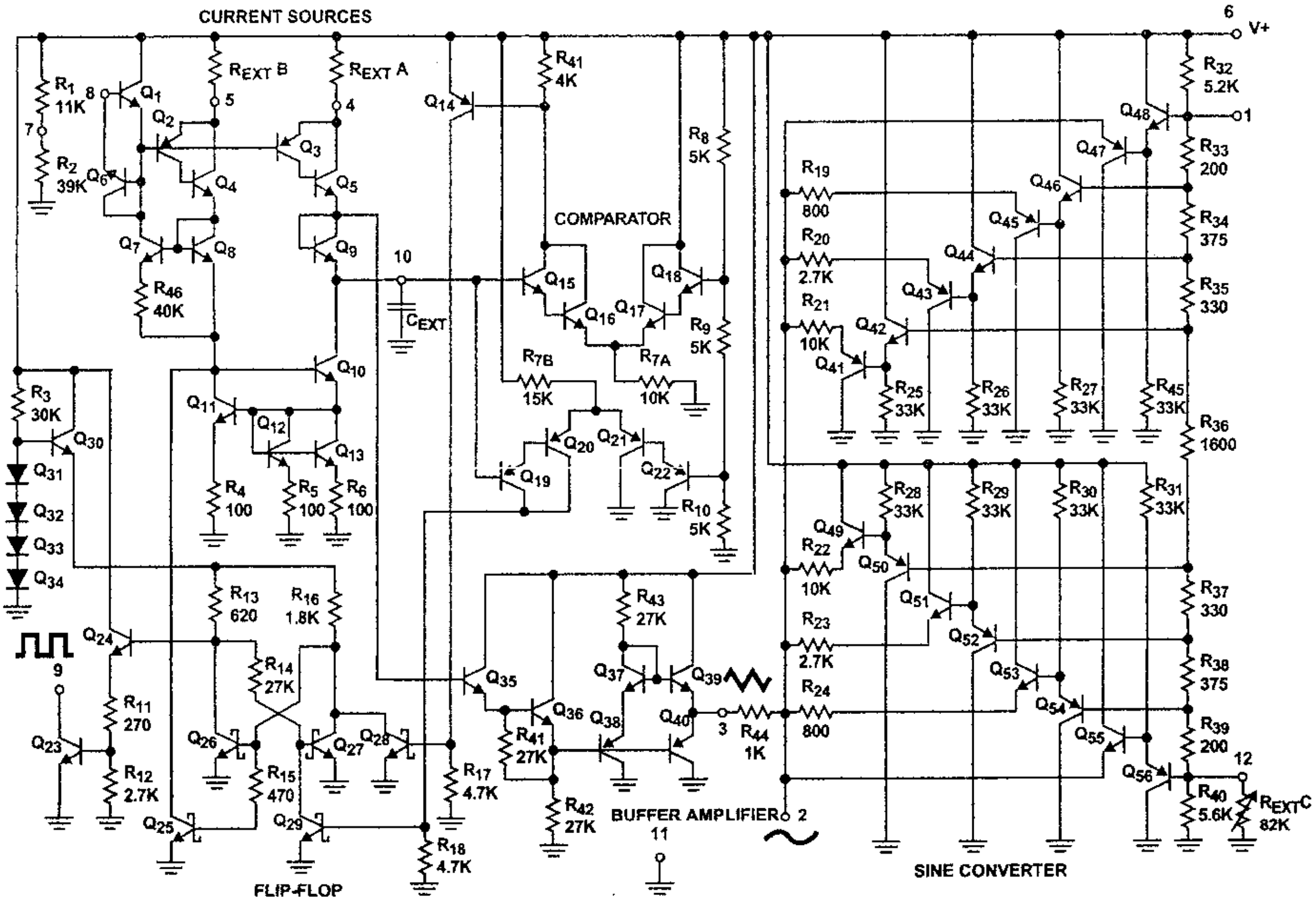


FIGURE 1. TEST CIRCUIT

etailed Schematic



pplication Information (See Functional Diagram)

ı external capacitor C is charged and discharged by two ırrent sources. Current source #2 is switched on and off by a ɔ-flop, while current source #1 is on continuously. Assuming at the flip-flop is in a state such that current source #2 is off, ıd the capacitor is charged with a current I, the voltage :ross the capacitor rises linearly with time. When this voltage aches the level of comparator #1 (set at 2/3 of the supply ıltage), the flip-flop is triggered, changes states, and leases current source #2. This current source normally ırries a current 2I, thus the capacitor is discharged with a net-current I and the voltage across it drops linearly with time. When it has reached the level of comparator #2 (set at 1/3 of the supply voltage), the flip-flop is triggered into its original state and the cycle starts again.

Four waveforms are readily obtainable from this basic generator circuit. With the current sources set at I and 2I respectively, the charge and discharge times are equal. Thus a triangle waveform is created across the capacitor and the flip-flop produces a square wave. Both waveforms are fed to buffer stages and are available at pins 3 and 9.

e levels of the current sources can, however, be selected er a wide range with two external resistors. Therefore, with two currents set at values different from I and 2I, an ymmetrical sawtooth appears at Terminal 3 and pulses h a duty cycle from less than 1% to greater than 99% are ailable at Terminal 9.

e sine wave is created by feeding the triangle wave into a nlinear network (sine converter). This network provides a creasing shunt impedance as the potential of the triangle ves toward the two extremes.

aveform Timing

e *symmetry* of all waveforms can be adjusted with the ternal timing resistors. Two possible ways to accomplish s are shown in Figure 3. Best results are obtained by eping the timing resistors R_A and R_B separate (A). R_A ntrols the rising portion of the triangle and sine wave and 1 state of the square wave.

e magnitude of the triangle waveform is set at $^1/_3$ $_{\text{UPPLY}}$; therefore the rising portion of the triangle is,

$$t_1 = \frac{C \times V}{I} = \frac{C \times 1/3 \times V_{SUPPLY} \times R_A}{0.22 \times V_{SUPPLY}} = \frac{R_A \times C}{0.66}$$

The falling portion of the triangle and sine wave and the 0 state of the square wave is:

$$t_2 = \frac{C \times V}{1} = \frac{C \times 1/3V_{SUPPLY}}{2(0.22)\frac{V_{SUPPLY}}{R_B} - 0.22\frac{V_{SUPPLY}}{R_A}} = \frac{R_A R_B C}{0.66(2R_A - R_B)}$$

Thus a 50% duty cycle is achieved when $R_A = R_B$.

If the duty cycle is to be varied over a small range about 50% only, the connection shown in Figure 3B is slightly more convenient. A 1kΩ potentiometer may not allow the duty cycle to be adjusted through 50% on all devices. If a 50% duty cycle is required, a 2kΩ or 5kΩ potentiometer should be used.

With two separate timing resistors, the frequency is given by:

$$f = \frac{1}{t_1 + t_2} = \frac{1}{\frac{R_A C}{0.66}\left(1 + \frac{R_B}{2R_A - R_B}\right)}$$

or, if $R_A = R_B = R$

$$f = \frac{0.33}{RC} \text{ (for Figure 3A)}$$

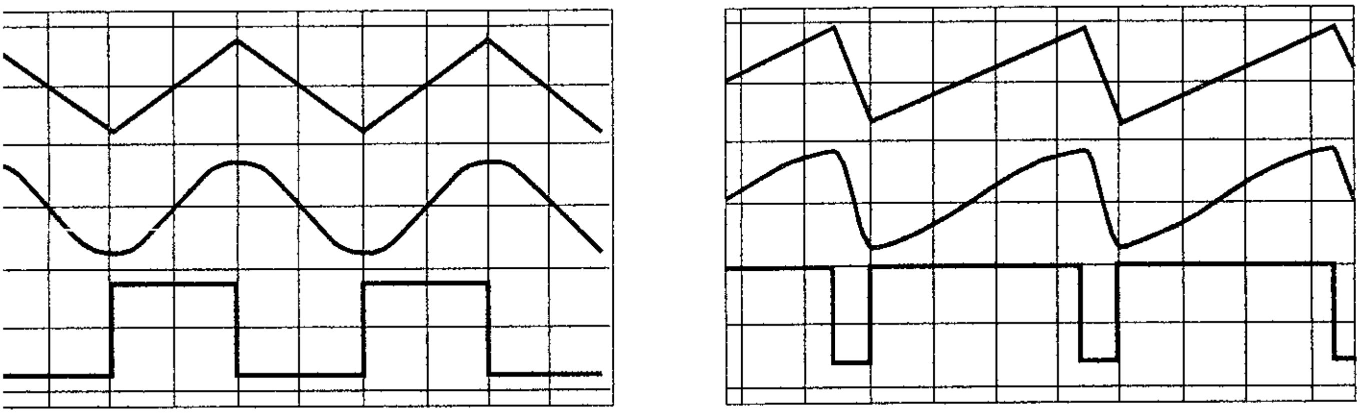


FIGURE 2A. SQUARE WAVE DUTY CYCLE - 50%

FIGURE 2B. SQUARE WAVE DUTY CYCLE - 80%

FIGURE 2. PHASE RELATIONSHIP OF WAVEFORMS

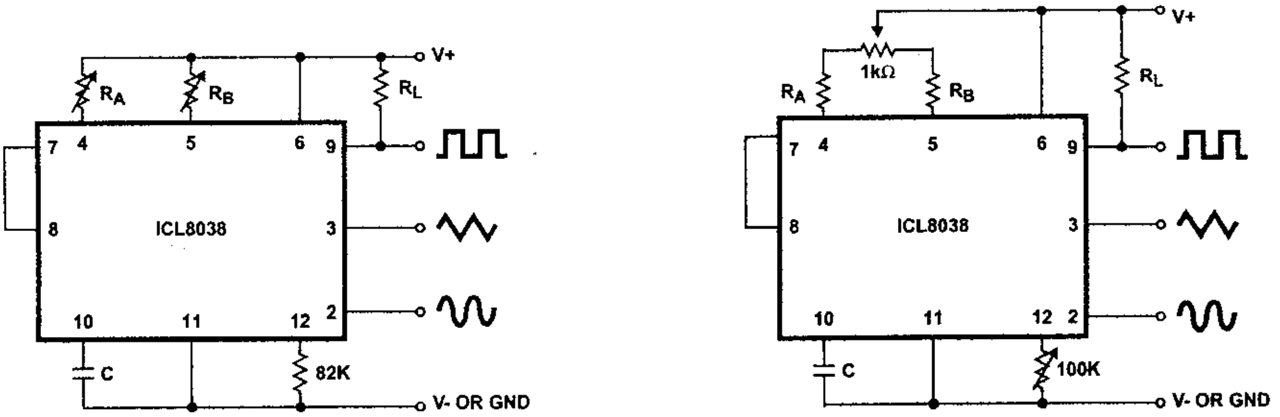


FIGURE 3A.

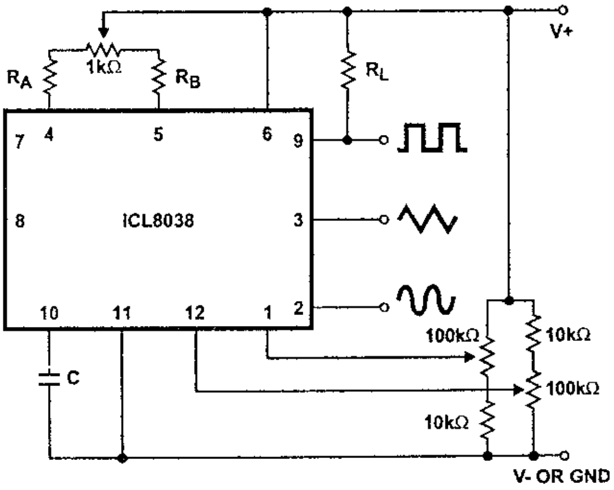
FIGURE 3B.

FIGURE 3. POSSIBLE CONNECTIONS FOR THE EXTERNAL TIMING RESISTORS

ither time nor frequency are dependent on supply voltage, ən though none of the voltages are regulated inside the əgrated circuit. This is due to the fact that both currents d thresholds are direct, linear functions of the supply tage and thus their effects cancel.

ducing Distortion

minimize sine wave distortion the 82kΩ resistor between ıs 11 and 12 is best made variable. With this arrangement tortion of less than 1% is achievable. To reduce this even ther, two potentiometers can be connected as shown in jure 4; this configuration allows a typical reduction of sine ve distortion close to 0.5%.



IGURE 4. CONNECTION TO ACHIEVE MINIMUM SINE WAVE DISTORTION

lecting R_A, R_B and C

r any given output frequency, there is a wide range of RC mbinations that will work, however certain constraints are ıced upon the magnitude of the charging current for timum performance. At the low end, currents of less than A are undesirable because circuit leakages will contribute ınificant errors at high temperatures. At higher currents › 5mA), transistor betas and saturation voltages will ntribute increasingly larger errors. Optimum performance l, therefore, be obtained with charging currents of 10μA to ıA. If pins 7 and 8 are shorted together, the magnitude of ᵌ charging current due to R_A can be calculated from:

$$= \frac{R_1 \times (V+ - V-)}{(R_1 + R_2)} \times \frac{1}{R_A} = \frac{0.22(V+ - V-)}{R_A}$$

R_1 and R_2 are shown in the Detailed Schematic.

A similar calculation holds for R_B.

The capacitor value should be chosen at the upper end of its possible range.

Waveform Out Level Control and Power Supplies

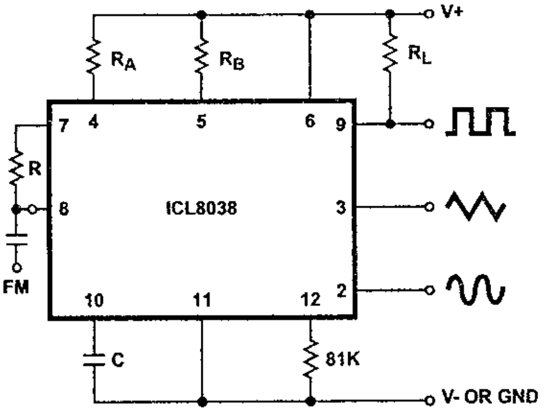
The waveform generator can be operated either from a single power supply (10V to 30V) or a dual power supply (±5V to ±15V). With a single power supply the average levels of the triangle and sine wave are at exactly one-half of the supply voltage, while the square wave alternates between V+ and ground. A split power supply has the advantage that all waveforms move symmetrically about ground.

The square wave output is not committed. A load resistor can be connected to a different power supply, as long as the applied voltage remains within the breakdown capability of the waveform generator (30V). In this way, the square wave output can be made TTL compatible (load resistor connected to +5V) while the waveform generator itself is powered from a much higher voltage.

Frequency Modulation and Sweeping

The frequency of the waveform generator is a direct function of the DC voltage at Terminal 8 (measured from V+). By altering this voltage, frequency modulation is performed. For small deviations (e.g. ±10%) the modulating signal can be applied directly to pin 8, merely providing DC decoupling with a capacitor as shown in Figure 5A. An external resistor between pins 7 and 8 is not necessary, but it can be used to increase input impedance from about 8kΩ (pins 7 and 8 connected together), to about (R + 8kΩ).

For larger FM deviations or for frequency sweeping, the modulating signal is applied between the positive supply voltage and pin 8 (Figure 5B). In this way the entire bias for the current sources is created by the modulating signal, and a very large (e.g. 1000:1) sweep range is created (f = 0 at V_{SWEEP} = 0). Care must be taken, however, to regulate the supply voltage; in this configuration the charge current is no longer a function of the supply voltage (yet the trigger thresholds still are) and thus the frequency becomes dependent on the supply voltage. The potential on Pin 8 may be swept down from V+ by ($^1/_3$ V_{SUPPLY} - 2V).



GURE 5A. CONNECTIONS FOR FREQUENCY MODULATION

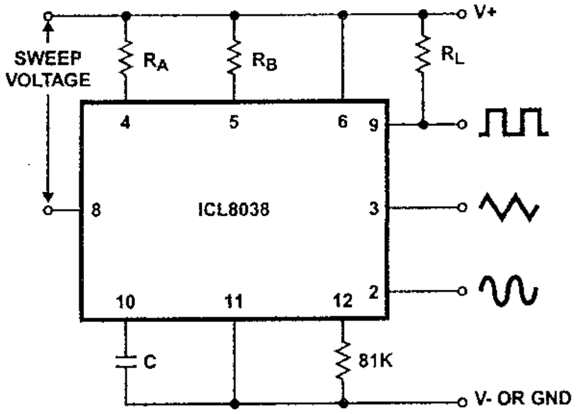


FIGURE 5B. CONNECTIONS FOR FREQUENCY SWEEP

FIGURE 5.

ypical Applications

ie sine wave output has a relatively high output impedance kΩ Typ). The circuit of Figure 6 provides buffering, gain id amplitude adjustment. A simple op amp follower could so be used.

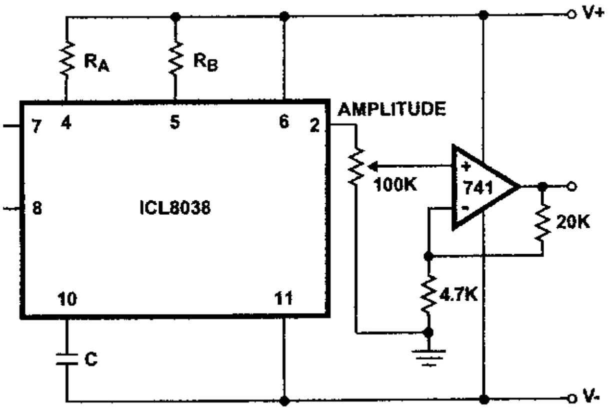


FIGURE 6. SINE WAVE OUTPUT BUFFER AMPLIFIERS

With a dual supply voltage the external capacitor on Pin 10 can be shorted to ground to halt the ICL8038 oscillation. Figure 7 shows a FET switch, diode ANDed with an input strobe signal to allow the output to always start on the same slope.

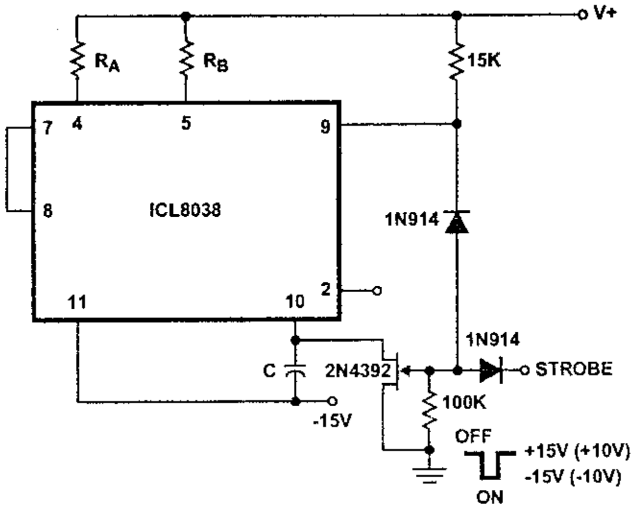


FIGURE 7. STROBE TONE BURST GENERATOR

To obtain a 1000:1 Sweep Range on the ICL8038 the voltage across external resistors R_A and R_B must decrease to nearly zero. This requires that the highest voltage on control Pin 8 exceed the voltage at the top of R_A and R_B by a few hundred mV. The Circuit of Figure 8 achieves this by using a diode to lower the effective supply voltage on the ICL8038. The large resistor on pin 5 helps reduce duty cycle variations with sweep.

The linearity of input sweep voltage versus output frequency can be significantly improved by using an op amp as shown in Figure 10.

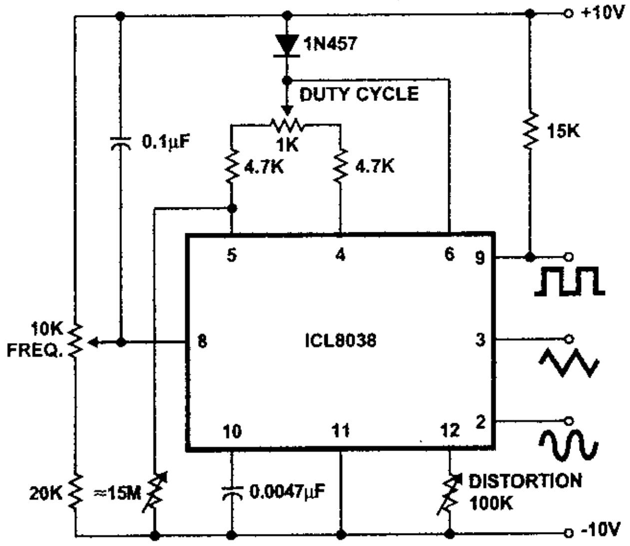


FIGURE 8. VARIABLE AUDIO OSCILLATOR, 20Hz TO 20kHzY

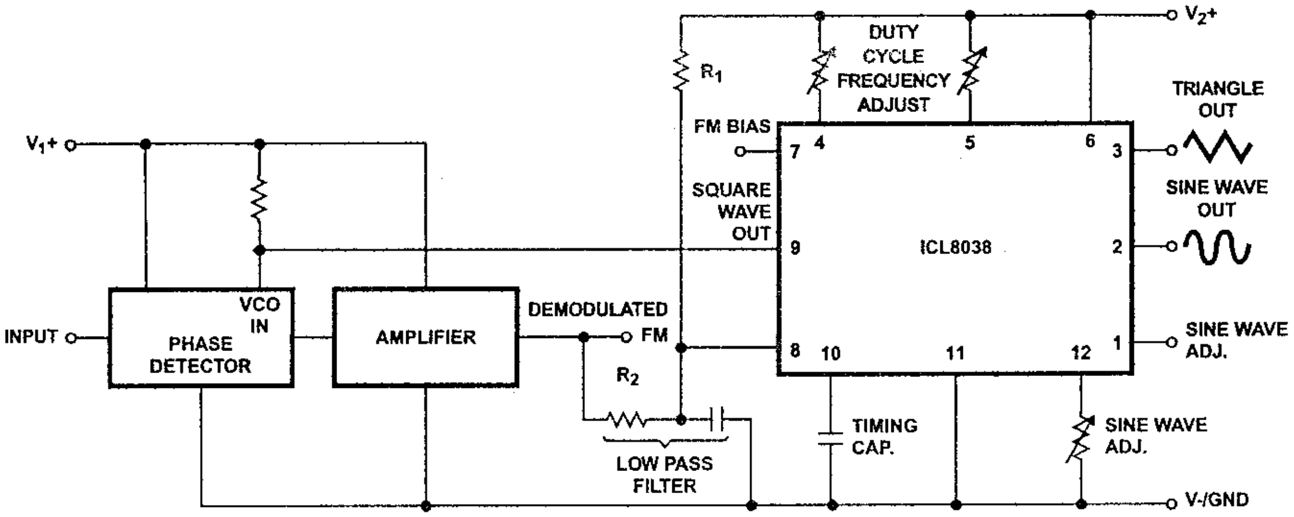


FIGURE 9. WAVEFORM GENERATOR USED AS STABLE VCO IN A PHASE-LOCKED LOOP

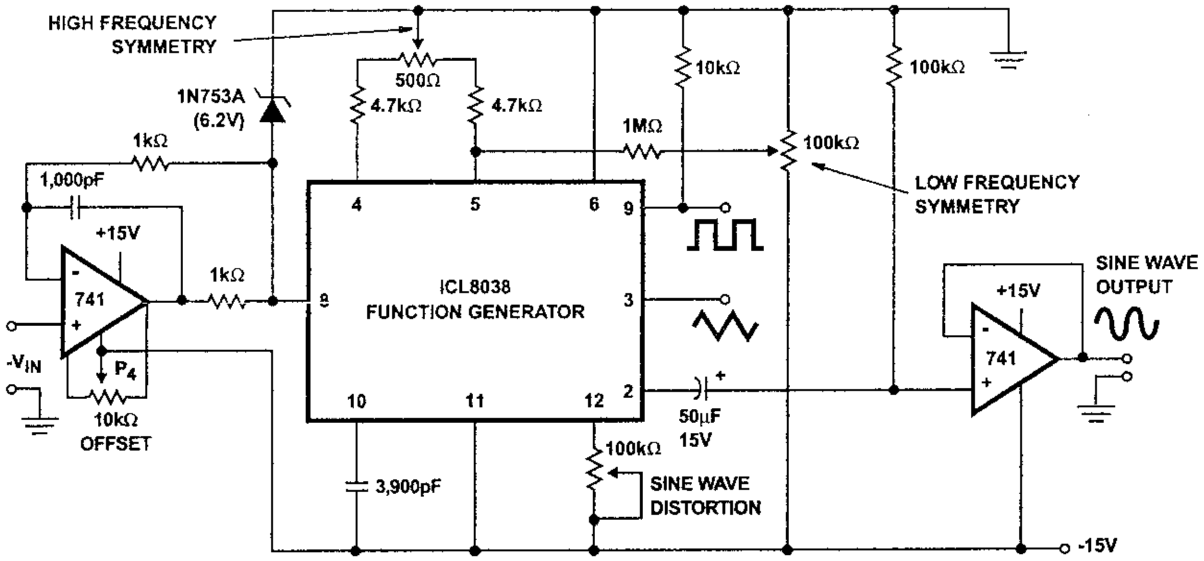


FIGURE 10. LINEAR VOLTAGE CONTROLLED OSCILLATOR

se in Phase Locked Loops

high frequency stability makes the ICL8038 an ideal ilding block for a phase locked loop as shown in Figure 9. this application the remaining functional blocks, the phase tector and the amplifier, can be formed by a number of ailable ICs (e.g., MC4344, NE562).

order to match these building blocks to each other, two eps must be taken. First, two different supply voltages are ed and the square wave output is returned to the supply of e phase detector. This assures that the VCO input voltage ll not exceed the capabilities of the phase detector. If a naller VCO signal is required, a simple resistive voltage vider is connected between pin 9 of the waveform nerator and the VCO input of the phase detector.

Second, the DC output level of the amplifier must be made compatible to the DC level required at the FM input of the waveform generator (pin 8, 0.8V+). The simplest solution here is to provide a voltage divider to V+ (R_1, R_2 as shown) if the amplifier has a lower output level, or to ground if its level is higher. The divider can be made part of the low-pass filter.

This application not only provides for a free-running frequency with very low temperature drift, but is also has the unique feature of producing a large reconstituted sinewave signal with a frequency identical to that at the input.

For further information, see Intersil Application Note AN013, "Everything You Always Wanted to Know About the ICL8038".

efinition of Terms

ipply Voltage (V_{SUPPLY}). The total supply voltage from · to V-.

ipply Current. The supply current required from the wer supply to operate the device, excluding load currents d the currents through R_A and R_B.

equency Range. The frequency range at the square wave tput through which circuit operation is guaranteed.

reep FM Range. The ratio of maximum frequency to nimum frequency which can be obtained by applying a eep voltage to pin 8. For correct operation, the sweep tage should be within the range:

3 V_{SUPPLY} + 2V) < V_{SWEEP} < V_{SUPPLY}

FM Linearity. The percentage deviation from the best fit straight line on the control voltage versus output frequency curve.

Output Amplitude. The peak-to-peak signal amplitude appearing at the outputs.

Saturation Voltage. The output voltage at the collector of Q_{23} when this transistor is turned on. It is measured for a sink current of 2mA.

Rise and Fall Times. The time required for the square wave output to change from 10% to 90%, or 90% to 10%, of its final value.

Triangle Waveform Linearity. The percentage deviation from the best fit straight line on the rising and falling triangle waveform.

Total Harmonic Distortion. The total harmonic distortion at the sine wave output.

ypical Performance Curves

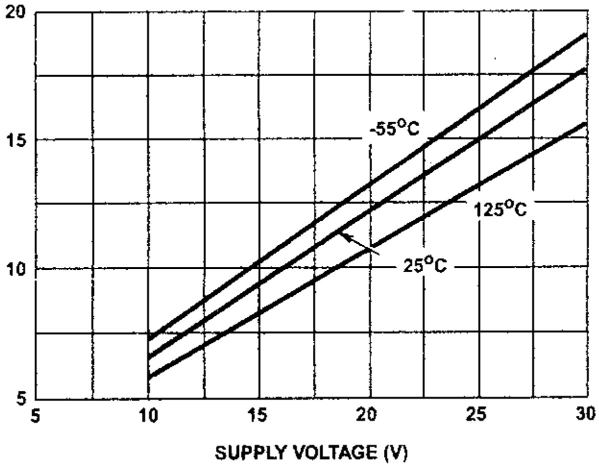


FIGURE 11. SUPPLY CURRENT vs SUPPLY VOLTAGE

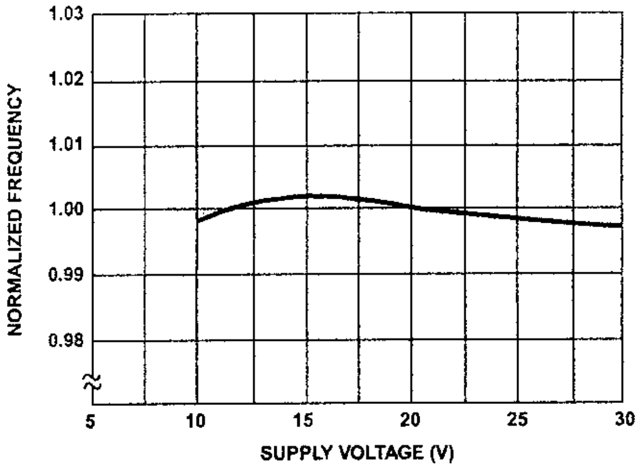


FIGURE 12. FREQUENCY vs SUPPLY VOLTAGE

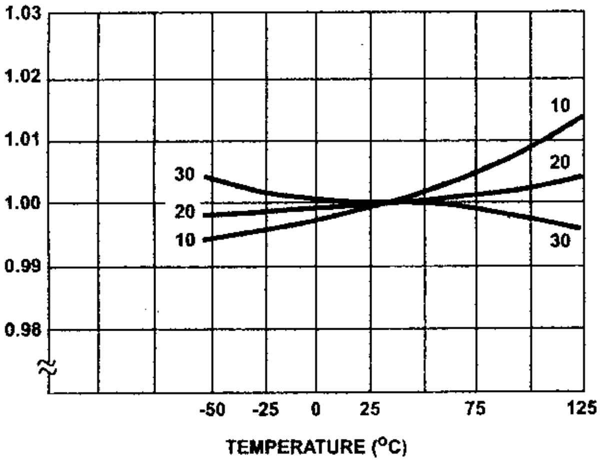


FIGURE 13. FREQUENCY vs TEMPERATURE

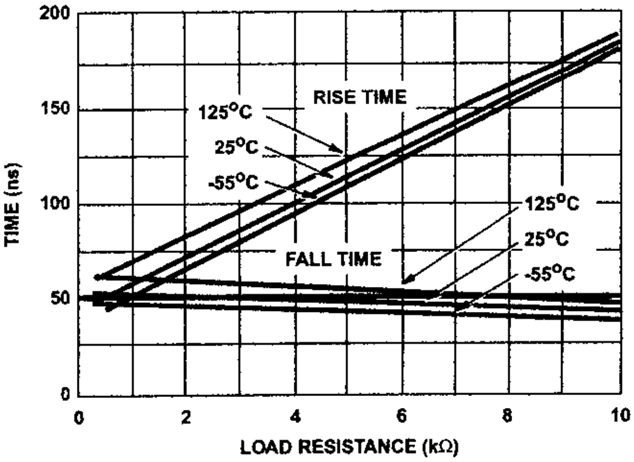
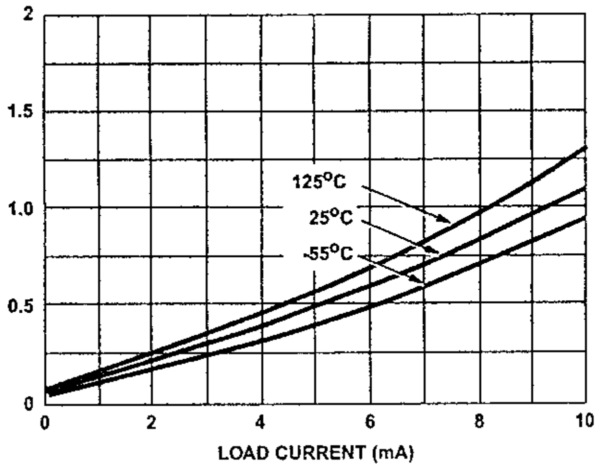


FIGURE 14. SQUARE WAVE OUTPUT RISE/FALL TIME vs LOAD RESISTANCE

ʼpical Performance Curves (Continued)



ƷURE 15. SQUARE WAVE SATURATION VOLTAGE vs LOAD CURRENT

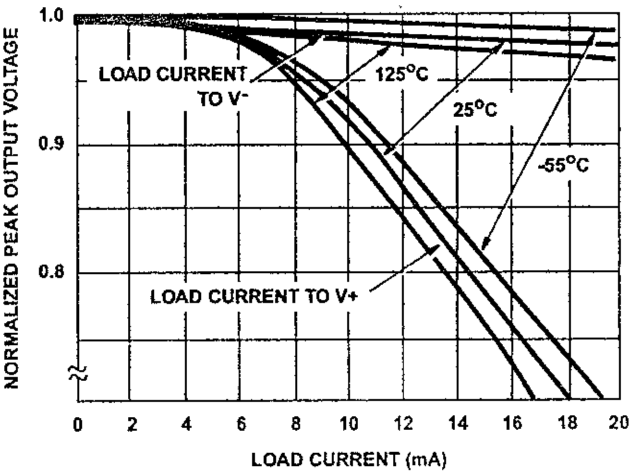
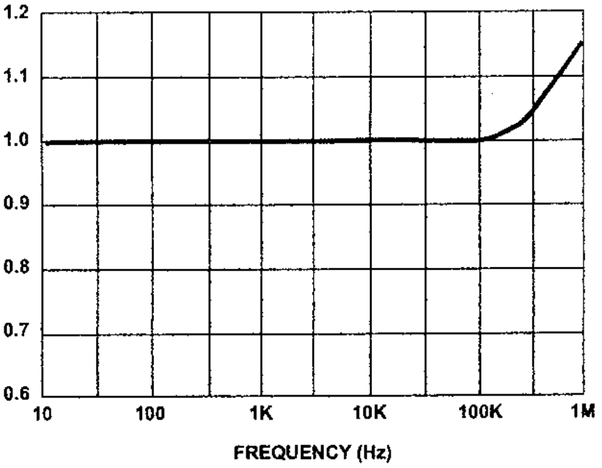


FIGURE 16. TRIANGLE WAVE OUTPUT VOLTAGE vs LOAD CURRENT



ƷURE 17. TRIANGLE WAVE OUTPUT VOLTAGE vs FREQUENCY

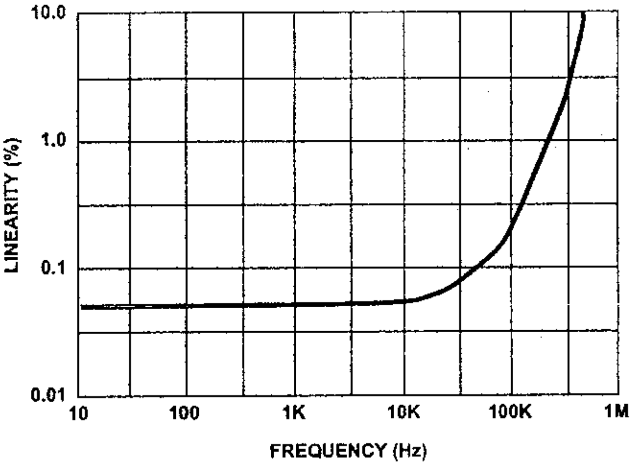
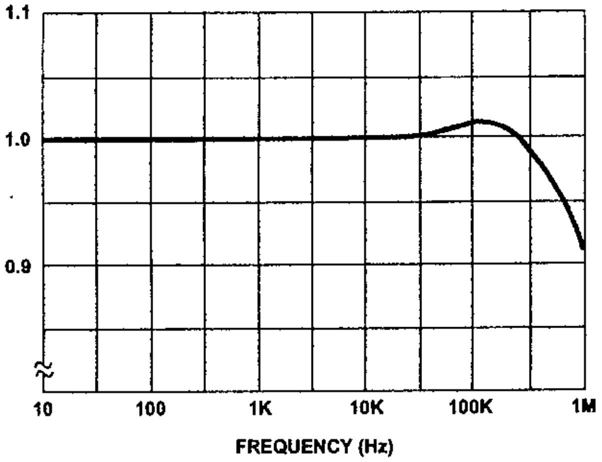


FIGURE 18. TRIANGLE WAVE LINEARITY vs FREQUENCY



ƷURE 19. SINE WAVE OUTPUT VOLTAGE vs FREQUENCY

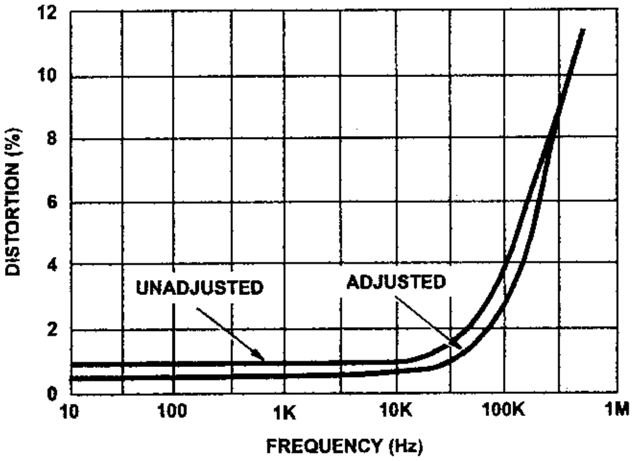


FIGURE 20. SINE WAVE DISTORTION vs FREQUENCY

TIP2955
TIP3055

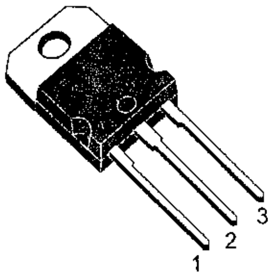
COMPLEMENTARY SILICON POWER TRANSISTORS

- STMicroelectronics PREFERRED SALESTYPES
- COMPLEMENTARY PNP - NPN DEVICES

DESCRIPTION

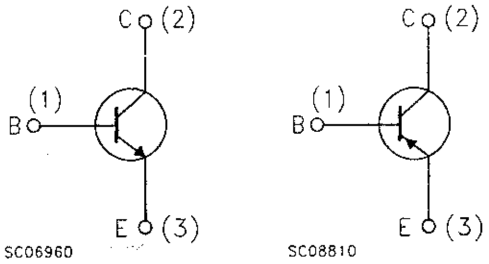
The TIP3055 is a silicon Epitaxial-Base Planar NPN transistor mountend in TO-218 plastic package. It is intented for power switching circuits, series and shunt regulators, output stages and hi-fi amplifiers.

The complementary PNP type is the TIP2955.



TO-218

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
		PNP	TIP2955	
		NPN	TIP3055	
V_{CBO}	Collector-Base Voltage ($I_E = 0$)		100	V
V_{CEO}	Collector-Emitter Voltage ($I_B = 0$)		60	V
I_C	Collector Current		15	A
I_B	Base Current		7	A
P_{tot}	Total Dissipation at $T_c \leq 25$ °C		90	W
T_{stg}	Storage Temperature		-65 to 150	°C
T_j	Max. Operating Junction Temperature		150	°C

For PNP types voltage and current are negative.

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case Max	1.4	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CEX}	Collector Cut-off Current (V_{BE} = -1.5V)	V_{CE} = 100 V V_{CE} = 100 V T_J = 150 °C			1 5	mA mA
I_{CEO}	Collector Cut-off Current (I_B = 0)	V_{CE} = 30 V			0.7	mA
I_{EBO}	Emitter Cut-off Current (I_C = 0)	V_{EB} = 7 V			5	mA
$V_{CEO(sus)}$*	Collector-Emitter Sustaining Voltage (I_B = 0)	I_C = 30 mA	60			V
$V_{CE(sat)}$*	Collector-emitter Saturation Voltage	I_C = 4 A I_B = 0.4 A I_C = 10 A I_B = 3.3 A			1 3	V V
V_{BE}*	Base-emitter Voltage	I_C = 4 A V_{CE} = 4 V			1.8	V
h_{FE}*	DC Current Gain	I_C = 4 A V_{CE} = 4 V I_C = 10 A V_{CE} = 4 V	20 5		70	
h_{fe}	Small Signal Current Gain	I_C = 1 A V_{CE} = 10 V f = 1 KHz	15			
f_T	Transition-Frequency	I_C = 0.5 A V_{CE} = 10 V f = 1 MHz	3			MHz
 t_{on} t_{off}	RESISTIVE LOAD Turn-on Time Turn-off Time	I_C = 6 A I_{B1} = - I_{B2} = 0.6 A R_L = 5 Ω $V_{BE(off)}$ = - 4 V		 0.5 0.9		 µs µs

∗ Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %
For PNP type, voltage and current value are negative.

TO-218 (SOT-93) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.7		4.9	0.185		0.193
C	1.17		1.37	0.046		0.054
D		2.5			0.098	
E	0.5		0.78	0.019		0.030
F	1.1		1.3	0.043		0.051
G	10.8		11.1	0.425		0.437
H	14.7		15.2	0.578		0.598
L2	–		16.2	–		0.637
L3		18			0.708	
L5	3.95		4.15	0.155		0.163
L6		31			1.220	
R	–		12.2	–		0.480
Ø	4		4.1	0.157		0.161