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"NEGATIVE BIAS TEMPERATURE INSTABILITY STUDIES FOR ANALOG SOC CIRCUITS"

by

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NEGATIVE BIAS TEMPERATURE INSTABILITY STUDIES FOR ANALOG SOC CIRCUITS

by

MOHD AZMAN ABDUL LATIF

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DECLARATION OF THESIS

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ABSTRACT

Negative Bias Temperature Instability (NBTI) is one of the recent reliability issues in sub threshold CMOS circuits. NBTI effect on analog circuits, which require matched device pairs and mismatches, will cause circuit failure. This work is to assess the NBTI effect considering the voltage and the temperature variations. It also provides a working knowledge of NBTI awareness to the circuit design community for reliable design of the SOC analog circuit. There have been numerous studies to date on the NBTI effect to analog circuits. However, other researchers did not study the implication of NBTI stress on analog circuits utilizing bandgap reference circuit. The reliability performance of all matched pair circuits, particularly the bandgap reference, is at the mercy of aging differential. Reliability simulation is mandatory to obtain realistic risk evaluation for circuit design reliability qualification. It is applicable to all circuit aging problems covering both analog and digital. Failure rate varies as a function of voltage and temperature. It is shown that PMOS is the reliability-susceptible device and NBTI is the most vital failure mechanism for analog circuit in sub-micrometer CMOS technology. This study provides a complete reliability simulation analysis of the on-die Thermal Sensor and the Digital Analog Converter (DAC) circuits and analyzes the effect of NBTI using reliability simulation tool. In order to check out the robustness of the NBTI-induced SOC circuit design, a burn-in experiment was conducted on the DAC circuits. The NBTI degradation observed in the reliability simulation analysis has given a clue that under a severe stress condition, a massive voltage threshold mismatch of beyond the 2mV limit was recorded. Burn-in experimental result on DAC proves the reliability sensitivity of NBTI to the DAC circuitry.

ABSTRAK

Suhu Bias Negatif Ketakstabilan (NBTI) adalah salah satu isu keboleharapan terkini dalam litar CMOS ambang sub. Kesan NBTI pada litar analog, yang memerlukan pasangan dan ketidakpadanan peranti dipadankan, akan menyebabkan kegagalan litar. Kerja ini adalah untuk menilai kesan NBTI khususnya voltan dan suhu. Ia juga menyediakan pengetahuan kerja NBTI kesedaran kepada masyarakat reka bentuk litar untuk reka bentuk dipercayai litar analog SOC. Terdapat banyak kajian sehingga kini berkenaan dengan kesan NBTI litar analog. Walau bagaimanapun, penyelidik lain tidak mengkaji implikasi tekanan NBTI atas litar analog yang menggunakan litar rujukan bandgap. Prestasi keboleharapan semua litar pasangan yang sepadan, khususnya rujukan bandgap, pada rahmat penuaan kebezaan. Simulasi Keboleharapan adalah wajib untuk mendapatkan penilaian risiko yang realistik untuk reka bentuk keboleharapan kelayakan litar. Ianya menyebabkan kepada litar semua penuaan masalah yang merangkumi kedua-dua analog dan digital. Kadar kegagalan berbeza-beza sebagai fungsi voltan dan suhu. Ia menunjukkan bahawa PMOS peranti mudah terpengaruh kebolehpercayaan dan NBTI mekanisme kegagalan yang paling penting untuk litar analog dalam sub-mikrometer teknologi CMOS. Kajian ini menyediakan simulasi keboleharapan analisis lengkap Sensor terma-mati dan Penukar Analog Digital (DAC) litar dan menganalisis kesan NBTI menggunakan keboleharapan alat simulasi. Dalam usaha menguji keteguhan reka bentuk NBTI yang disebabkan oleh litar SOC, percubaan membakar dalam telah dijalankan ke atas litar DAC. Kemerosotan NBTI yang diperhatikan dalam analisis simulasi keboleharapan telah memberi petunjuk bahawa di bawah keadaan tekanan yang teruk, voltan yang signifikan ambang ketidaksepadanan yang melebihi had 2mV dicatatkan. Membakar dalam keputusan uji kaji pada DAC mengesahkan sensitiviti kebolehpercayaan NBTI kepada reka bentuk litar DAC.

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LIST OF ABBREVIATIONS

ADC	Analog Digital Converter
ADI	Assembly Die Inventory
ATE	Automated Tester Equipment
BI	Burn-In
BIT	Burn-In Time
CMOS	Complementary Metal Oxide Semiconductor
CRT	Cathode Ray Tube
CTAT	Complementary To Absolute Temperature
DAC	Digital-to-Analog-Converter
DDR	Double Data Rate
DFT	Design-For-Test
DNL	Differential Non Linearity
DPM	Defect Per Million
DRAM	Dynamic Random Access Memory
EM	Electro Migration
EOL	End-Of-Life
FN	Fowler Nordheim
FIT	Failure-In-Time
HCI	Hot Carrier Injection
HDMI	High Definition Multimedia Interface
HTOL	High Temperature Operating Lifetest
HVM	High Volume Manufacturing
IC	Integrated Circuit
IM	Infant Mortality
INL	Integral Non Linearity
LSB	Least Significant Bit
LVDS	Low Voltage Differential Signaling

MSB	Most Significant Bit
MTBF	Mean Time Between Failure
NBTI	Negative Bias Temperature Instability
PBIC	Post Burn-In Check
PC	Personal Computer
PLL	Phase Locked Loop
PoF	Physics Of Failure
PROCHOT	Hot Processor
PTAT	Proportional To Absolute Temperature
PVT	Process Voltage Temperature
RSSS	Slow Process Corner
RFFF	Fast Process Corner
SOC	System-On-Chip
TDDB	Time Domain Dielectric Breakdown
TSMC	Taiwan Semiconductor Manufacturing Corporation
TTM	Time-To-Market
TTTT	Typical Process Corner
USB	Universal Serial Bus
ULSI	Ultra Large Scale Integration
UWB	Ultra Wide Band
VESA	Video Electronics Standards Association
VLSI	Very Large Scale Integrated
WLBI	Wafer Level Burn-In

CHAPTER 1

INTRODUCTION

1.1 Background

Over the last decade, the semiconductor industry has observed an exceptional market growth and the world is in the process of witnessing a continuous technology progression. Today, semiconductor devices, containing millions of transistors, can be easily found in various home appliances like IPOD players, GPS receivers, cell phones, and even rice-cookers. The industry's emphasis from military defense markets which require high reliability performance has shifted now to the mainstream and commercial and consumer markets in which time-to-market (TTM) and functionality are now today's top priorities. Marketing pressure and aggressive competition drive the manufacturers to keep introducing new materials, processes, devices and products. Many aspects of semiconductor design and manufacturing are experiencing drastic changes that may impact the high level of reliability that customers have been experiencing in the past. Designers are under intense pressure to have their designs work at the first time with a decent reliability. They need to balance the trade-off between performance and reliability to meet the needs of different market segments [5]. As the device complexity is increasing and the gap between normal operating and extreme test conditions is narrowing, manufacturers see these issues as big challenges. Hence, both designers and manufacturers need to work hand-in-hand to develop an accurate reliability or aging simulation and prediction tools in order to achieve the reliability performance goal covering both circuit level and system level [6].

Reliability or sometime called aging is the probability that a component can survive without failure under stated conditions for a stated period of time while taking into account various uncertainty sources such as the material properties, and the volume of the components. Due to this uncertainties, the reliability simulators or aging simulators have become an essential tool which is integrated into the design simulation/flow. These simulators have successfully modeled some critical failure mechanisms in today's electronic devices, such as Negative Bias Temperature Instability (NBTI), Time Domain Dielectric Breakdown (TDDB), electro-migration (EM) and Hot Carrier Injection (HCI). The expectation from the simulation output is that these failure mechanisms will be modeled until the end-of-life and will guarantee at least a minimum of the expected use-conditions for the electronic devices to operate. Throughout the years, there has been a significant amount of simulation work that focuses on individual reliability issues and their impact on semiconductor industry. Li, *et al.* [7] developed compact modeling of MOSFET wearout mechanisms for circuit-reliability simulation. Yan,*et al.* [8] developed reliability simulation and circuit-failure analysis in analog and mixed-signal applications. Sapatnekar *et al.* [9] have confirmed that the effect of NBTI relaxation under ac operations has been analytically modeled. In addition, Kufluoglu *et al.* [4] have addressed both PMOS-level measurement delay artifacts and real-time degradation/recovery calculation through a robust and accurate simulation approach. Huard *et al.* [10] have demonstrated the powerful abilities of a practical design in reliability (DiR) methodology in providing quantitative reliability assessment for CMOS designs by taking into account both the HCI and NBTI degradations.

The gate dielectrics breakdown mode also shifts from the clear cut hard breakdown detection to the noisy soft breakdown issue [11–13]. Hence, new reliability models are needed. At the same time, an issue which has been not so critical in the past, has begun to show substantial impact, such as the NBTI issue. Therefore, new modeling methods and understandings are mandatory. With alternative gate dielectrics introduction, new issues associated with these materials and device structures are also raised. Traps inside the bulk dielectrics and near the interface cause instability to the threshold voltage of complementary metaloxidesemiconductor (CMOS) and impose new risk to the

reliability of devices [14]. These issues are becoming even worse for system-on-chip (SOC) applications whereby most of the circuit blocks (digital and analog) are fabricated on the same chip. As a result, these issues need to be studied in detail before fully incorporating new process technology recipe for SOC products.

When the failure rate of CMOS VLSI circuits is too high to be acceptable, a passive improvement of the reliability statistical properties of the existing population can be achieved by burning the product prior to shipment. Burn-in stresses are commonly performed on products, particularly on SRAM array to accelerate the fabrication process failure mechanism and to screen out design flaws. Under sub-micron process technology node, the most possible implication to the burn-in stress is NBTI [5]. A. Krishnan *et al.* [15] from TI have explored the burn-in implications for SRAM circuits. Their approach has demonstrated that the NBTI-induced Vcc_{min} increase during burn-in is of the order of the NBTI-induced V_t shift.

1.2 Thesis Objectives

This work focuses on studying the effect of NBTI on analog circuit reliability. This main motivation of this study is because NBTI has emerged as a threat for future process technologies. NBTI effect prevents the device from operating at low voltage and causes higher power dissipation. There has been numerous studies to date on the NBTI effect to analog circuits. However, other researchers did not study the implication of NBTI stress on analog circuits utilizing bandgap reference circuit. The analog circuits investigated are namely the on-die thermal sensor and the Cathode-Ray Tube (CRT) Digital-to-Analog-Converter (DAC).

In order to investigate this reliability challenge at the circuit level, an accurate NBTI mode and a simulation tool for end-of-life or aging estimation are used. The simulation tool integrates the physics of-failure (PoF) approach and the statistical approach. Given the Process, Voltage, and Temperature (PVT) dependence of NBTI effect, and the significant amount of PVT variations in Nano-scale CMOS, it is critical to study

the effects of PVT variations and the NBTI effect for circuit analysis. For this specific work, the main focus is primarily on the voltage and temperature effects to the circuit degradation. Process variation effect will be studied in the future work. By taking reliability awareness into practical manner, it allows circuit designers to perform quick and efficient circuit reliability analysis and hence, to develop practical guidelines for reliable SOC circuit designs.

The final objective of the work is to study and to verify the reliability of the analog SOC circuit. A burn-in experiment is conducted to verify the robustness of the NBTI-induced CRT DAC circuit design.

1.3 Thesis Outline

This thesis is composed of 5 chapters. After the introduction, Chapter 2 discusses the reliability modeling for Analog Circuit Design. It describes the three most critical intrinsic failure mechanisms: NBTI , Hot Carrier Injection (HCI), and Time Domain Dielectric Breakdown (TDDB), respectively. The physics of failure behind these failure mechanisms as well as the physical and statistical models will be covered. Chapter 3 introduces the Analog Circuit in SOC applications particularly on the bandgap reference circuit on key electronic applications in SOC design.

Chapter 4 discusses the reliability simulation focusing on two case studies. This chapter focuses on an in-depth reliability simulation on analog circuits. The first case study is related to the on-die thermal sensor. The second case study deals with the data converters particularly DAC. Both analog components are mostly relying on the bandgap reference circuit. Therefore, the use of a bandgap reference circuit for these circuit applications needs a fully integrated voltage reference with a continuous-time output that exhibits a tight voltage spread and low thermal drift in production.

Chapter 5 describes the burn-in (BI) experiment conducted on the DAC component. It is critical to determine the validity and the robustness of this DAC component since its

applications require extreme levels of matching requirements. Hence, it is very critical to verify the reliability modeling of the induced mismatch for this particular circuit since most of studies to date confirm that even a small shift in matching devices can cause significant reliability concern.

Chapter 6 concludes this thesis by summarizing its most important contributions to the findings. It also provides recommendations for future work.

CHAPTER 2

RELIABILITY MODELING, MECHANISMS AND STRESSES

The progression of deep submicron process technologies coupled with the reduction of Complementary Metal Oxide Semiconductor (CMOS) physical geometries have revealed many new technical challenges in predicting circuit lifetimes and securing sufficient reliability margins. One of the criteria of reliable IC production ramps is being able to fabricate a product that is capable of sustaining its intended functionality for guaranteed time under stated usage conditions. The fundamental concept of reliability modeling for analog circuit design is described in Section 2.1. NBTI, which is one of the key recent reliability mechanisms in today's deep sub micron process technologies, is compared with other failure mechanisms in Section 2.2. Burn-in stress test is discussed in Section 2.3. Finally, some other reliability stresses are discussed in Section 2.4.

2.1 Reliability Modeling for Analog Circuit Design

Quality and reliability are among the two critical criteria in any products introduced regardless of the type of components. Quality is the fraction that works near time zero when customer first uses and tests the product. Reliability is the fraction that works after some time in the customer's hands. Reliability can be defined as the probability that an item will continue to perform its intended function without failure for a specified period of time [16]. For instance, it is expected that the cars, computers, electrical appliances, lights, televisions, etc. to function whenever they are required, day after

day, year after year. When they fail the results can be catastrophic and as a result, it could be costly. More often, repeated failure leads to annoyance, inconvenience and a lasting customer dissatisfaction that can play havoc with the responsible company's marketplace position.

Under recent fabrication process technologies, the microchips are formed from millions of transistors which make it a challenge to predict reliability. Therefore, a statistical method is found to be the most effective tool to predict microchip reliability [7]. The existing reliability simulation for microchip only models the failure at the end-of-life [2, 7]. That is basically after the fact that the suspected aging mechanisms are determined to be the dominator. This approach does not take into account the random defects after burn-in stress which may have been seen in the field.

Silicon and package reliability are the two key components that use Failure-In-Time (FIT) as a measurement. FIT is defined as a rate of the number of expected silicon defects per billion part hours [6]. For each component multiplies by the number of devices in a system, a FIT is determined for an estimation of the predicted system reliability. A predicted FIT given by the industry to the customers has some key parameters associated with it. Based on recent predicted FIT, the specifications consists of voltage, frequency, heat dissipation, etc. As a result, the Mean Time Between Failures (MTBF) is defined as a simulation model for a system reliability. MTBF for the complete system is produced by a summation of the FIT rates for each of the component.

A FIT is determined by equation (2.1) in [8] in terms of an acceleration factor, A_F, as

$$FIT = \frac{\#defects}{\#tested * hours * A_F} \times 10^9 \tag{2.1}$$

where the number of defects, (#defects) that can be expected in one billion device-hours of operation. FIT is statistically projected from the results of accelerated test procedures.

There are two methods in characterizing the reliability models. The first method is by device and the second method is by product.

1. Device Characterization - It is characterized using single-device test structures. The advantage of characterizing using this approach is due to better physical understanding and better control of stress during stress tests. On the other hand, the disadvantage of this approach is that it needs to be scaled to product with scaling and the use condition models.

2. Product Characterization - It is characterized by testing the complete units. The advantage of this approach is that it will produce an accurate model for the whole products and it will not require scaling factor. On the other hand, the disadvantage of this approach is that it will have less physical understanding and less precise control of stresses.

   In some mechanisms, device and product characterizations do occur. This event typically exists on the analog circuit.

2.2 Failure Mechanisms

To ensure critical components such as microprocessor, and other products, are sufficiently reliable, the reliability models predicts time-to-failure (TTF) due to known failure mechanisms and failure rates in the field. These two factors needs to be assessed if they are below the established goals set by the quality and reliability engineer. The most significant failure mechanism in the recent process technologies is NBTI [6, 8, 17–19].

2.2.1 Negative Bias Temperature Instability (NBTI)

In the modern semiconductor industry, statistical analysis and the black box knowledge behind the understanding of how complicated systems interact will become increasingly critical specifically as we enter the new paradigm of mega scale integration and SOC

semiconductor production. For the next generation of SOC and semiconductor products, there is a new series of challenges ahead of us to overcome [5]. Those challenges have critical effect to product yield and reliability, design-for-test (DFT), and the depth of process integration. NBTI, gate oxide leakage current, and power consumption are some of the key reliability problems affecting the semiconductor industry today. As CMOS devices are getting scaled and the chip density starts to increase, the probability of a circuit encountering lethal accelerated NBTI degradation increases [20]. As device channel length is shrinking over time, the defect interactions and the process variations become alarming when the electrical output characteristics are investigated [21]. According to Jha N.K. et al. [17], NBTI can pose a serious reliability concern as a small variation in the bias currents of analog circuits, such as the digital-to-analog-converter (DAC), can cause significant gain errors. At the end, as the SOC complexity and the integration increase, the NBTI impact to the yield is also expected to climb due to the shift in parametric behavior [22, 23].

2.2.1.1 NBTI Origin

Process technology is experiencing a continuous momentum in transistor enhancement with reduced channel length. Due to this effect, NBTI stress has become one of the most significant reliability concerns and this is crucial in determining the CMOS device lifetime expectancy [24]. NBTI occurs in the PMOS devices stressed with the negative gate bias at elevated temperature. This event occurs at the gate oxide silicon interface where the interface traps are formed [5, 6]. This interface trap formation is getting aggravated at the elevated temperatures. An increase in the threshold voltage, V_t and a decrease in the drain current, I_{DSAT} are the symptoms of the NBTI parametric manifestation especially in analog circuits [25–29]. NBTI occurs mostly under the condition where the gate is on but there is no current flowing through the channel, similar to the case of a CMOS inverter. Some low level degradations occur even when the drain current is flowing. Consider the voltage waveforms of a CMOS inverter as illustrated by Figure 2.1.

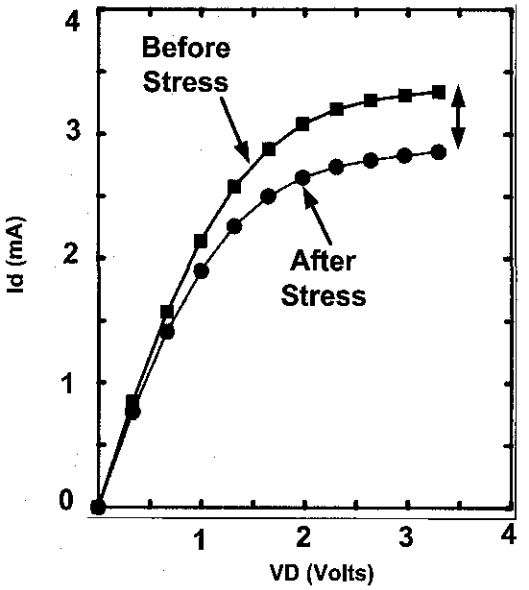

Figure 2.1: CMOS Inverter Voltage Waveforms

As illustrated in Figure 2.1, NBTI occurs during CMOS circuit operation when the PMOS transistor is fully turned on [30]. NBTI occurs for a substantially longer period of time when the circuit is not switching and is essentially static.

NBTI happens when the trivalent silicon atoms pairs with the silicon and the hidrogen, (Si_3-Si-H) bonds at the silicon to the gate oxide, (Si-SiO_2) interface are broken by cold holes. The left sketch in Figure 2.2 shows that these holes develop in the inversion layer and cause hydrogen to be released. The build up of the dangling bonds causes them to act as interface traps, Si-(N_{it}), where the interface state, (N_{it}), indicates no presence of SiO_2 molecule. The NBTI failing rate goes up as the gate voltage goes down [5, 31]. As the nitrogen concentration in the oxide is increased to raise the gate dielectric constant, NBTI degradation also increases [5, 31]. At a given voltage across gate to source,V_{gs}, and with increasing voltage across the bulk junction, V_{sb}, more N_{it} issues are created as Si-O bonds are broken by hot holes. The issue causes a severe damage to N_{it} and shifts from the drain end toward the center of the channel, and both the transconductance (g_m) degradation and threshold voltage (V_t) shifts are aggravated [31].

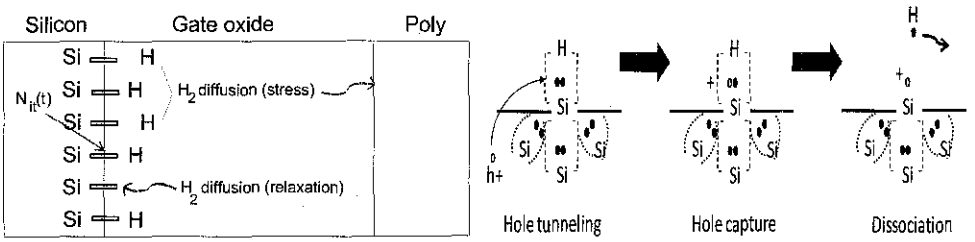

Figure 2.2: Schematic description of the NBTI event (left) and possible mechanism for breaking interfacial Si-H bonds by inversion-layer holes (right).

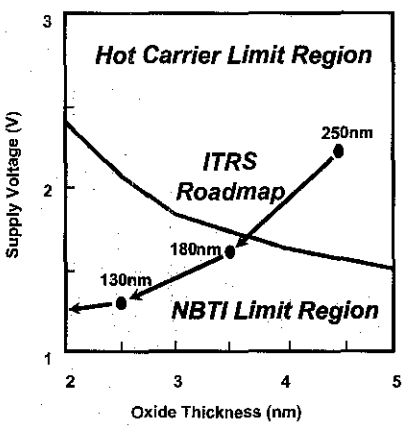

Figure 2.3: NBTI trend increases as the technology nodes goes with the narrower channel length [3]

It was reported based on data collection across different technology nodes that under the legacy process technology, Hot Carrier Injection (HCI) was the limiting factor [5, 6, 8, 17, 19, 23, 32]. However, this is not the case anymore under today's trend. Under recent sub micron CMOS process technology, NBTI has emerged as a major reliability concern. Figure 2.3 reveals that NBTI trend is becoming alarming as the technology node goes with the narrower channel length. It is noted that the narrower channel length and high-K metal gate (HKMG) material may help to alleviate NBTI problem [18]. However, the NBTI problem still exists even in today's process technology.

Therefore, an efficient analysis for resilient designs must be seriously considered. NBTI effect strongly depends on Voltage (VCC), Temperature (T), and Duty Cycle (DC) [5, 6, 8, 17, 19, 23, 32]. These factors change from time to time, from technology node to technology node.

NBTI degradation aggravates at high temperatures, causing a huge shift in the threshold voltage. Furthermore, over long periods of time, this V_t shift can potentially cause PMOS devices causing it to degrade. This is in contrast with other failure mechanisms such as the hot carrier injection phenomena whereby it happens for a short period of time during rapid switching transitions [30]. Hence, NBTI degradation is expected to be the most contributing factor for degradation to happen during the device operation [33]. NMOS transistors are far less affected because interface states and fixed charges are of opposite polarity and eventually cancel each other. Taking into account the positive fixed charge density, the trap charge density is added for a PMOS and subtracted for an NMOS transistor. This difference is illustrated in [5] by equation 2.2 below.

$$\Delta V_t(PMOS) = -\frac{Q_{it}+Q_f}{C_{ox}}, \Delta V_t(NMOS) = -\frac{Q_{it}-Q_f}{C_{ox}} \tag{2.2}$$

Equation 2.2 above illustrates the NBTI induced shift in threshold voltage for both PMOS and NMOS transistors as a function of fixed charge density and interface trap density. Both device types exhibit negative shifts in threshold voltage during a state of inversion; however, this further shows PMOS transistors are more severely affected by NBTI degradation.

The NBTI phenomenon is increasingly alarming due to the fact that the degradation mechanism occurs when the PMOS transistor is effectively biased with a negative gate voltage. This negative bias causes the PMOS transistor to be inverted. Figure 2.4 elaborates the static stress modes for a PMOS transistor. NBTI degradation is not dependent on the conduction current. Hence, this static stress mode assures uniform NBTI degradation across the channel of the transistor.

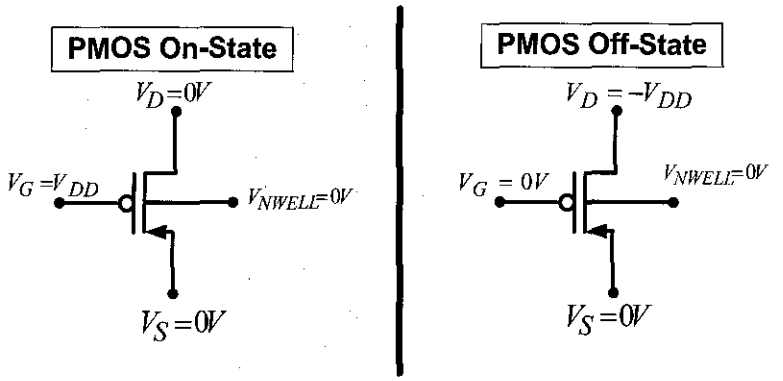

Figure 2.4: PMOS Stress Modes

The threshold voltage shift caused by NBTI is primarily dependent on several parameters namely temperature, voltage and stress time [19, 34–37]. The temperature is generally within the range of 100-250°C, followed by the oxide electric fields whose value generally below 6 MV/cm [17]. Any NBTI parameters described above which may perform below the expected value will result to the event of hot carrier degradation instead. These parameters are comparable to those seen during the burn-in test of a device. As a matter of fact, these values are also encountered by many high-performance ICs during normal operations.

In order to boost the circuit performance especially on SOC, designers must scale transistor oxide, width, length and thickness together [38]. This is to ensure that the channel resistance performance is retained from one technology node to the next generation. With the aggressive reduction of oxide thickness, less voltage must be applied to the gate in order to sustain reliability. This threat leads to the need to lower the threshold voltage value. During the NBTI stress, the hole concentration is higher near the gate edge and gate-source/drain overlap region than in the channel region [39]. The NBTI degradation near the gate edge is caused by reactions between holes and oxide defects through a combination of routine use conditions (electric field, current, and temperature). This results in unsaturated dangling electron bonds, also referred to as interface traps [18]. NBTI causes an analog circuit to fail due to the fact that analog operations require higher accuracy of matched device pairs. Even small mismatches induced by NBTI may result in circuit failure [17].

2.2.2 Other CMOS Defect Models

In addition to the progressive parametric degradation caused by NBTI, which is described as the primary reliability mechanism, the circuit designers must also address the integrity of the transistor dielectric itself. In the course of a circuit operation, this can cause the circuit to fail. This phenomenon is typically referred to as Time Dependent Dielectric Breakdown (TDDB). The third critical reliability mechanism occurs during the device switching in CMOS which is commonly referred to as Hot Carrier Injection (HCI).

2.2.2.1 Time Dependant Dielectric Breakdown (TDDB)

Time Dependant Dielectric Breakdown (TDDB) is a wear-out phenomenon of silicon dioxide, SiO_2 the thin insulating layer between the control gate and the conducting channel of the transistor. SiO_2 has a bulk resistivity of approximately 10^{15} Ω - cm and a dielectric breakdown strength of approximately 10^7 *V/cm*. This makes it the key factor of the success in the CMOS technology due to its process advantage and high quality. Technology scaling has driven the thickness of SiO_2), t_{ox} down to the fundamental limiting point of 1.2 nm. The oxide thickness of thinner than 1 nm is no longer insulated while oxide thickness of below 1 nm may never find extensive use in CMOS technology. This is because of excessively high oxide currents caused by TDDB [40]. Gate dielectric is the critical part of a MOS device. Gate oxide failure usually results from TDDB. This dielectric failure happens when there is a formation of conductive path in the dielectric, which causes shorting of the anode and the cathode [7]. Both PMOS and NMOS may suffer from TDDB event if both transistors are continuously stressed and biased by the gate. As a result it will lose the control of channel current flow between the drain and the source with a gate electronic field.

2.2.2.2 *Hot Carrier Injection (HCI)*

When a MOS transistor is in saturation, the electric field across the pinch-off region may be high enough that carriers gain enough energy to excite electron-hole pairs. The electron-hole pairs become components of the drain and substrate currents. The holes (electrons) usually flow towards the p-substrate (N-well) in an N-channel (P-channel) device, increasing the substrate currents. This scenario will have higher chances of producing latch-up event. The excited electrons (holes) that reach the drain cause an increase in I_{DSAT}. In other words, it will cause a weak avalanche event. However, the reliability concern is that part of the hot electron can penetrate the gate oxide.

The P-channel transistors are usually less susceptible to the hot electron degradation due to the holes lower mobility, and higher effective mass. Electrons that penetrated the gate oxide remain trapped there (in normal operating conditions). The hot electron effect is accumulative. The negative trapped charge in the oxide, which is near the drain of an NMOS transistor causes an increase in V_t there. The hot electron effect result is a degradation in the NMOS I_{DSAT} due to the higher effective V_t. It means the circuits slow down due to the fact that the hot electron degradation has a negative feedback behavior. Hot electron degradation is a long term reliability concern. The device life time that the industry guarantees is 100Khr of constant operation at the worst case conditions. However, this extreme condition is still within the industrial specification. That means when a device frequency is tested after fabrication, the hot electron degradation with time must be taken into account.

2.3 Burn-In Stress Test

2.3.1 Introduction

In the competitive environment of semiconductor manufacturing, accurate power dissipation and reliability prediction result in significant time-to-market and profitability improvement. Prediction quality depends on the manufacturers ability to characterize

process-related instabilities and defects in a given design. When the failure rate of CMOS VLSI circuits is too high to be acceptable, a passive improvement of the reliability statistical properties of the existing population can be achieved by burning-in the product prior to shipment.

Burn-in is a process of subjecting a device to elevated temperatures and voltages to promote early life failures of components or boards/systems in an effort to assure that outgoing Defect Per Million (DPM) targets are met. Burn-in is an obligatory part of microprocessor manufacturing and assures that reliability goals are achieved. It is a critical step in the microprocessor reliability provision during High Volume Manufacturing (HVM). Every new product requires burn-in hardware configuration and capacity planning before the product data are made available.

Burn-in stress test is an event when the device is exercised at elevated voltage and temperature from the start, which is typically at time zero. The main purpose is to screen assembly defects or to screen infant mortality defects going through a set of functional tests. Burn-in gives a clearer picture of unit's defects types hence determining the source of defects. The duration of burn-in stress will help filtering out defects with other early failure issues.

Burn-in is a process of subjecting a device to elevated temperature and voltage. The primary goal of burn-in is to accelerate particle defects and processing problems to failure. In other words, it weeds out Infant Mortality (IM) in the reliability bathtub curve. Figure 2.5 shows that at 30 days, burn-in stress will screen out infant mortality failures to guarantee product reliability in the first 30 days. Then the flat line is a constant failure rate, known as random failures. The right most of the bathtub curve is where failure rate begins to increase after 7 years of lifetime due to wearout.

Burn-in time (T), voltage (V) and temperature (T) conditions are process dependent. The health and stability of the fabrication process are also key factors. In the product qualification flow and initial production flow, units are tested at Raw Class location before burn-in stress. Raw Class is the first location of test. The purpose of running this test is to screen out potential assembly defects. Testing the units at raw class ensures

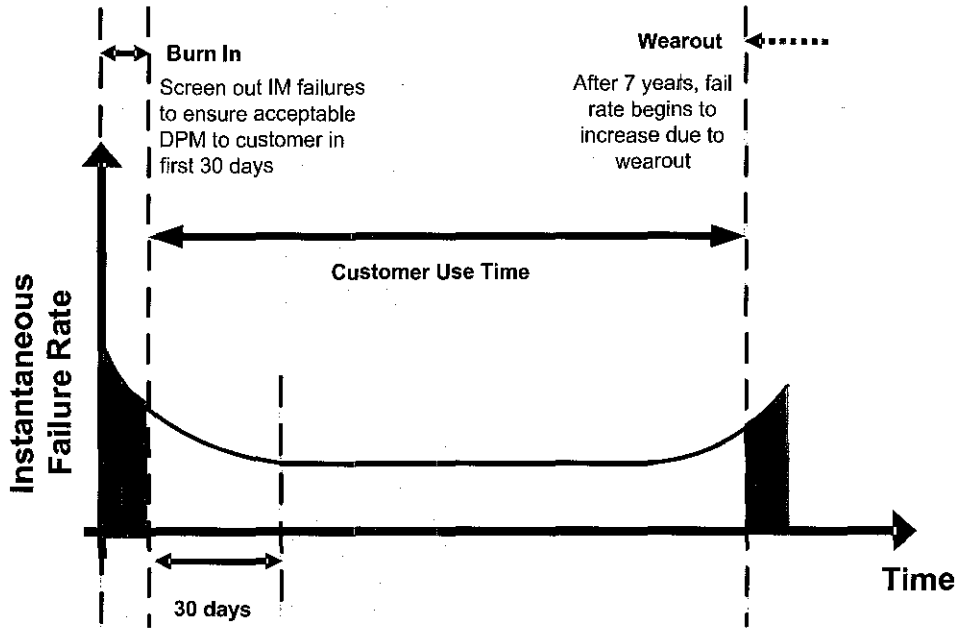

Figure 2.5: Bathtub curve

that post burn-in socket failures can be attributed strictly to burn-in induced failure mechanisms. Screening out defects prior to burn-in allows for what is referred to as clean burn-in.

In the production ramp flow as illustrated in Figure 2.6, units are burned in directly after assembly. This process is referred to as direct burn-in. Most of the semiconductor products undergo some amount of burn-in in all manufacturing flows before being shipped to customers.

The rationale behind burn-in is to apply elevated temperature and voltage stress in order to screen out parts with defects which would otherwise manifest as infant mortality.

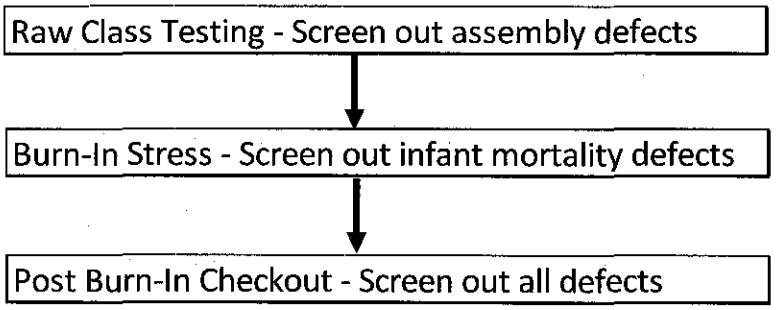

Figure 2.6: Typical manufacturing production flow

2.3.2 Analog versus Digital Burn-In

In digital circuits,the distribution of voltage across gate and source, V_{gs} stress is performed by dynamically toggling all transistor nodes between 0 and 1. Monitoring signal propagation through functional blocks has been used as an empirical indicator of both liveness, as well as the necessary toggle coverage. One of the main requirements of burn-in set by the industrial standard is to obtain at least an 80% toggle coverage. In other words, at least 80% of the transistors of the device will, at some point during the test, be placed into both on and off states. However, it does not guarantee that toggle coverage goals are being met, and therefore by extension, does not guarantee the distribution of V_{gs} stress.

Due to the signal propagation being associated with toggle coverage, and by extension to voltage stress in digital circuits, burn-in strategies for analog circuits presently in use across the industry are expected to be similar to digital burn-in strategies. It is for this reason that significant effort has been extended in trying to overcome the challenges of achieving analog signal propagation during burn-in. However, signal propagation is not necessarily an indicator of toggle coverage. Moreover, toggle coverage often has no meaning in analog circuits because the signal voltage levels do not swing between logic levels in normal operation. Therefore, the actual voltage stress in analog circuit must be carefully studied and understood. This is with the assumption that all on-chip

voltage regulators have been bypassed, or reprogrammed, so that external increases in power supply voltage are directly applied to target circuit power rails.

2.3.3 Wafer Level Burn-In stress (WLBI)

The Wafer Level Burn-In (WLBI) is used to improve package-level burn-in yield and to avoid unnecessary packaging of bad chips. Furthermore, some of the failing parts may be repairable. With WLBI, the chips are contacted directly on the wafer. In contrast to burn-in after packaging, WLBI does not require individual burn-in boards or special component sockets for the various package types. That enables considerable cost savings, especially when many different types of packages are manufactured.

However, because WLBI is generally performed on the production tester, the duration of burn-in needs to be very short. Also, the temperature is restricted to be well below package-level burn-in. Therefore, the voltage is usually increased above the package-level burn-in voltage and special measures are taken to obtain better efficiency in terms of duty cycle factor than in package-level burn-in.

2.3.4 High Temperature Operation Life (HTOL)

The purpose of High Temperature Operation Life (HTOL) test is to determine the effects of burn-in bias at elevated temperature stress conditions on solid-state devices over time. It stresses all the burn-in patterns at the maximum VCC instead of the burn-in voltage at much higher burn-in junction temperature, typically at 125°C. The setting is quiet similar to the extended life test but with an aggressive temperature acceleration. It is primarily being run for device reliability evaluation.

2.4 Summary

Reliability simulation and modeling concept have been discussed. NBTI phenomena and its sensitivity in comparison to other reliability failure mechanisms such as HCI and TDDB are presented and discussed. It is noted that NBTI event has been a major threat to the SOC design especially the analog circuit design.

NBTI causes analog circuits to fail because analog operations require higher accuracy of matched device pairs. Even small mismatches induced by NBTI may result in a circuit failure. In SOC design, where most of the circuit blocks (digital and analog) are fabricated on the same chip for SOC applications, it is very critical to design right at the first time.

Burn-in as one of the key reliability stress tests has been proven to be the key component in ensuring the reliability robustness of a product. Some other reliability stress tests are also being discussed. The study has found that all of these tests are having similarities in terms of verifying the reliability concerns.

In the next chapter, the band gap reference circuit, which requires extreme accuracy, and its applications are presented.

CHAPTER 3

BANDGAP REFERENCE AND ITS APPLICATIONS

The circuit performance is a function of environment where the circuit is being used. Therefore, it is critical to minimize the effect of the environment. The environment in this context is particularly the Process, the Voltage Supply and the Temperature (PVT). Bandgap reference circuit has been widely used to stabilize any circuit variables especially analog circuits applications. In this chapter, this special reference circuit is studied in detail. In order to minimize the cost for the overall work, a voltage reference circuit is desired to be designed and drawn with minimal area while minimizing the burn-in board cost associated with external chip power delivery or filtering components. Therefore, eliminating the need for on-die voltage regulation and eliminating calibration or trimming to achieve an absolute accuracy performance that is tighter than the external board voltage regulator is of interest. This aspect is important for overall area optimization of the chip IO ring since several IO circuits may be implemented with a bandgap reference voltage. Due to this fact, some key applications utilizing the bandgap reference in SOC design are described in Section 3.2. The bandgap reference sources of error are explained in Section 3.3.

3.1 Bandgap Reference Circuit

Highly accurate voltage reference circuits are required for a variety of precision analog circuit applications including data converters, voltage regulators, thermal sensors, biasing for Phase Locked Loop (PLL), and I/O interfaces such as Universal Serial Bus 2.0

(USB2^{TM}), Low Voltage Differential Swing (LVDS) and High-Definition Multimedia Interface (HDMI) transmitters. The use of a voltage reference circuit for these circuit applications generally require a fully integrated voltage reference with a continuous-time output that exhibits a tight voltage spread and low thermal drift in production [41].

Figure 3.1 shows the basic circuit diagram of the CMOS bandgap circuit. The bandgap voltage output, V_{BG}, indicated in [42] with op-amp offset is given by the equation (3.1):

$$V_{BG} = V_{BE3} + [\frac{R4}{R3}][\frac{KT}{q} \ln \frac{A1}{A2} - V_{OS}] \tag{3.1}$$

The voltage, V_{BE3}, is the diode voltage, T is temperature, K is Boltzmanns constant, q is the electron charge, V_{OS} is the input referred amplifier offset, and A1/A2 is the ratio of the two diode voltages. Resistor R4 has been designed to be equal to R5. The bandgap voltage output, V_{BG}, given by Equation 3.1 shows that the bandgap voltage output is strongly dependent on the op-amp offset. Since the op-amp offset term is effectively multiplied by a constant that depends on the ratio of resistances R4 and R3, the offset of the op-amp is typically the main contributor to the bandgap absolute output voltage varying from part-to-part due to random mismatch. A similar equation applies to the low-voltage bandgap circuit architecture [1, 43].

In order to minimize cost especially for a low power product, a bandgap voltage circuit is desired to be designed and drawn with minimal area while minimizing board cost associated with external chip power delivery or filtering components. The filtering components are created by adding an external capacitor to the output to create a low-pass filter. This circuit's output noise can be further reduced by adding another capacitor as a passive low-pass filter. Therefore, eliminating the need for on-die voltage regulation and eliminating calibration or trimming to achieve an absolute accuracy performance that is tighter than the external board voltage regulator is of interest. This aspect is important for overall area optimization of the chip I/O ring since several I/O circuits may be implemented with a bandgap reference voltage. In addition, the voltage reference

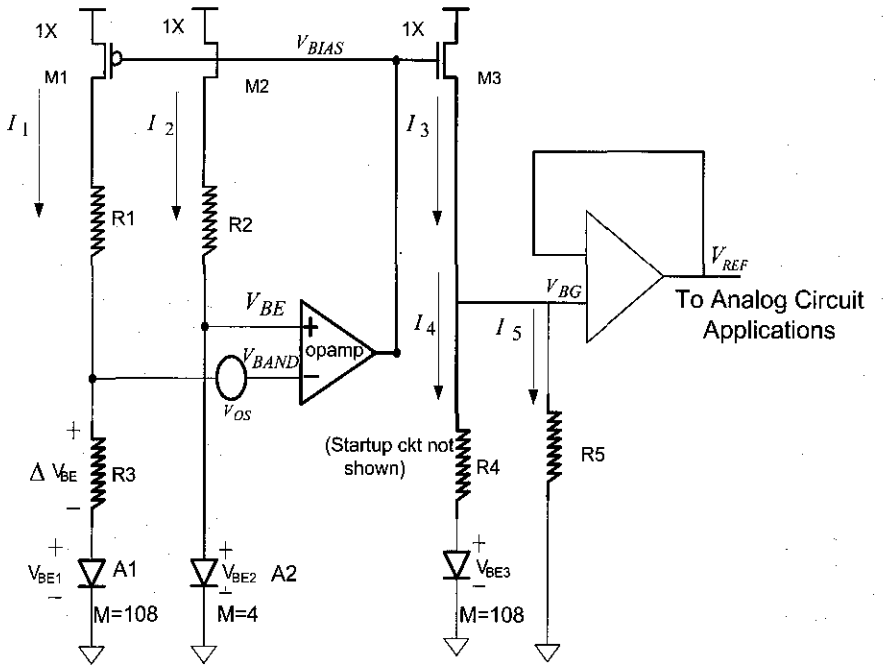

Figure 3.1: Basic CMOS Bandgap Reference Circuit.

circuit may also be required to start-up and be operational while circuits such as a PLL may be acquiring lock or I/O circuits to reach their state of operation. Therefore, it is desirable that the integrated voltage reference circuit is a self-contained, asynchronous and self-starting circuit that does not depend on schemes where the voltage reference must first be adjusted or calibrated prior to the I/O becoming functional.

3.2 Key applications utilizing Bandgap reference in SOC Design

Many system-on-chip (SOC) applications such as Universal Serial Bus 2.0 (USB2^{TM}), Low Voltage Differential Swing (LVDS) and High-Definition Multimedia Interface (HDMI) transmitters require precision analog circuit applications like the Digital Analog Converter (DAC), the Analog Digital Converter (ADC), the Phase-Locked Loop (PLL) and the on-die thermal sensor. In order for these applications to operate at the highest degree of voltage accuracy, they require the use of a bandgap reference circuit.

3.2.1 DAC Circuit

Many applications especially SOC, comprise of the Digital-Analog-Converter (DAC) as well as the Analog-Digital-Converter (ADC). These converters are used for communication with the external world [44]. The typical 8-bit DAC, used to produce the signals required to drive the RGB guns of a computer monitor, are usually current source based circuits. The currents produced are usually converted to voltage through a simple resistive termination found at each end of the cable that connects the monitor to the DAC inside the computer. The digital to analog transformation produced by the DAC is generally covered by a set of specifications described in terms of voltage.

Since the introduction of the IBM PC in 1980, the changes and advances in raster based display systems have been rapid and continual. Those aspects of the basic raster display system related to the DAC specifications are introduced and are still being used in the high speed applications.

The typical DAC used in video display is designed to be linear to the Least Significant Bit (LSB). There are several major issues in testing the DAC to this level of resolution. Many of the traditional DAC specifications are not typically used in the TV/Video/Cathode Ray Tube (CRT) DAC marketplace. For instance, there are usually no harmonic distortion or signal-to- noise ratio type specifications stated, as these are generally reserved for high performance audio DAC [45].

The architecture and technology options as illustrated in Figure 3.2 have shown that CMOS current-steering DAC architectures are the top choice for high speed performance and SOC applications due to their lower cost and lower power consumption in the SOC integration with the digital circuits. Furthermore, they are more linear than the famous resistor-string DAC's and they are intrinsically faster converter. [29, 46–48].

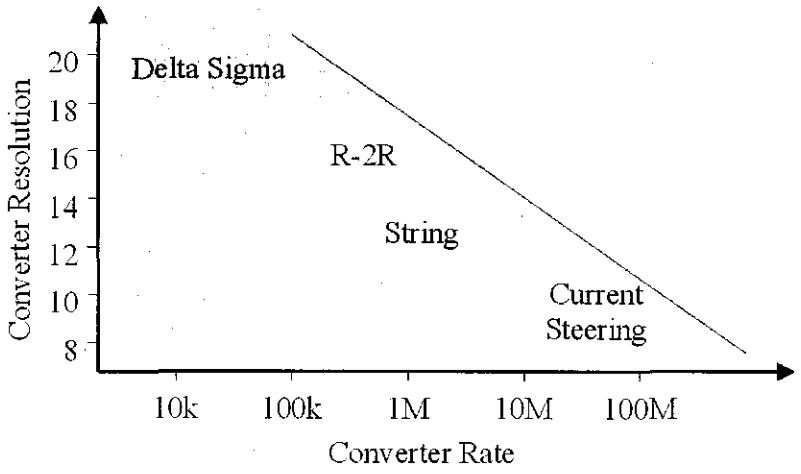

Figure 3.2: Architecture and techology comparisons of various DAC selections.

3.2.1.1 Output Voltage Compliance

This parameter is generally stated as a Compliance-Voltage Range (-0.5V to 1.5V) which represents the maximum range of the output terminal voltage over which a current source DAC will maintain its specified current-output characteristics. This then reflects the basic ability of the current sources within the device to maintain their currents within a stated range, regardless of their summed output terminal voltage, and any supply voltage variations.

3.2.1.2 Output Current

This parameter is also stated as a compliance type. It describes the typical full scale current at 700 mV with the standard 75 ohm doubly terminated load (37.5 ohms total) used on Video Electronics Standards Association (VESA) compliant video DAC [45]. The doubly terminated load implementation is to ensure maximum stability and performance, it is important to use both a source termination resistor and an end termination resistor. The typical voltage value would equate to having all the current sources ON and driving a maximum current of 18.67 mA through 37.5 ohms. The min / max values would be those expected as a result of any variation of actual device performance or

supply voltage. The design of the DAC usually incorporates an array of constant current sources whose sum total is used to produce the varying analog signal.

The current range of the individual current sources used in the design is not usually stated for specification purposes but is essential if special test mode techniques are employed that would make it possible to turn ON each current source individually. This individual current source test mode can be extremely valuable for design validation and manufacturing testing. It could be used as a means of measuring each current output and checking to see it falls within the range that supports the stated Full Scale Range.

One difficulty with this measurement originates from the fact that the DAC outputs are usually doubly terminated to ground with 75 ohm resistors and this converts the current into voltage and unless the termination can be disconnected from ground, the current being produced by each current source is not easily measurable by instrumentation.

3.2.1.3 DAC Resolution and Accuracy

Generally, the most important performance specifications of a DAC concern resolution and accuracy [8]. Resolution refers to the number of unique voltage or even current levels that the DAC is capable of producing. For typical 8-bit current source based DAC, they ideally would produce 256 unique current values for each digital code possible. Inherent in the specification of resolution, is the property of monotonicity. The output of a monotonic converter always changes in the same direction for an increase in the applied digital code. The quantitative measure of monotonicity is referred to as Differential Non Linearity (DNL) in terms of the step size.

Generally, the static absolute accuracy of a DAC can be described in terms of three fundamental kinds of errors: offset errors, gain errors, and linearity errors. Of these, linearity error is the most important, as usually in most cases, offset and gain errors can be adjusted or compensated for, in the end-use application. Linearity errors are more

difficult and expensive to deal with in terms of added compensation at the final PC video sub-system level. Offset and Gain errors are typically referred to as end-point errors.

3.2.1.4 Full Scale Error

Full Scale Error refers to any error found in the voltage or the current produced by the DAC with all bits activated as "1". This then equates to twice the value of the DACs Most Significant Bit (MSB) value. In a 4 Bit DAC it would be 2 times whatever the code 1000 (MSB-LSB) is ideally designed to produce. For a simple binary encoding, a linear correspondence exists between the input codes and the output levels. The equation referred in [45] for an N-bit DAC can be described in equation (3.2):

$$V_O = V_{FS} * \sum_{i=1}^{N} b_i/2^i \tag{3.2}$$

Note this equation reflects the fact that V_{FSR} is different from V_{11} by 1 LSB.

- b_i = logic levels of the binary input bits (Example: 0010 = 2) .
- N = number of input bits (Example: 4 input DAC, N = 4) .
- V_{FSR} = Voltage Out Full Scale Reference = V_{FS+} - V_{FS-}
- V_{11} = Voltage Out all bits On (all 1s code).
- V_O = Voltage Out all bits Off (all 0s code).

Figure 3.3 is an example of the offset error alone. The actual transfer function differs from the ideal by +2 LSBs for each code. If present, such an offset error could be detected at each code. But, it is often only measured at the all 0s code because of the possibility that some amount of gain error, as depicted in Figure 3.4, could also be present [45].

Figure 3.4 reflects what can happen if only positive or negative gain error is present. Gain error is usually expressed as a percentage, as it can affect each code by the same percentage amount. Hence gain error by itself is undetectable at the all 0s code, but

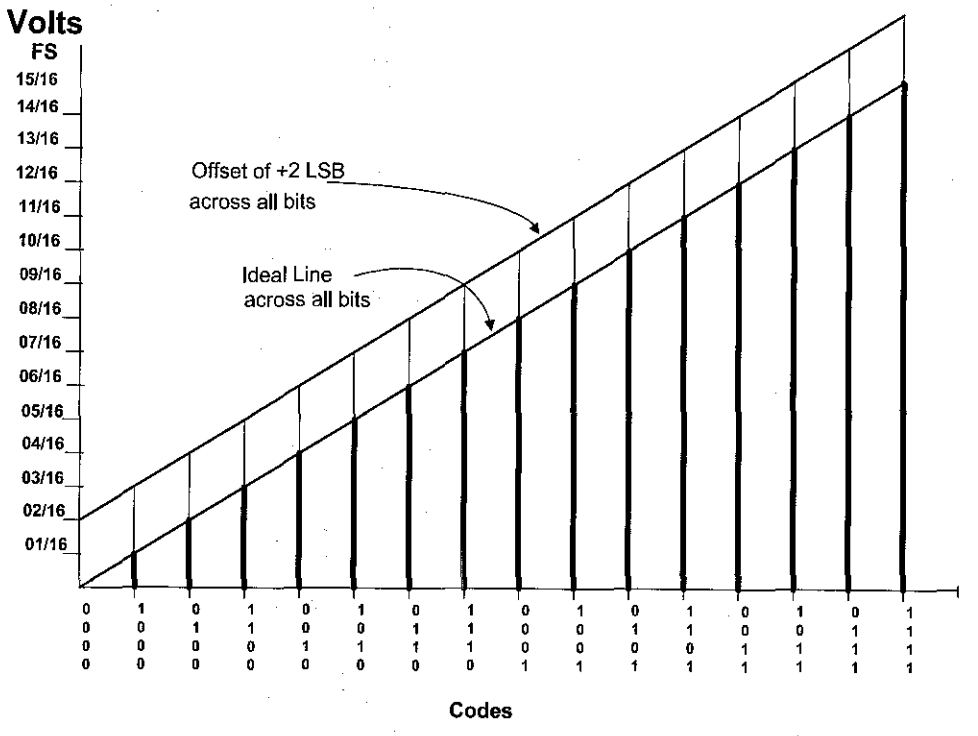

Figure 3.3: 4-Bit DAC Offset error transfer function.

is detectable at the all 1s code or (Full-Scale -1 LSB) level. Figure 3.4 reflects a +/- 5 percent gain error.

Gain error is determined by first determining the offset error, then by measuring the all 1s output voltage level (which is 1 LSB $<$ V_{FSR}) the full-scale reference voltage as indicated in [45] using equation (3.3).

$$ErrorPercent = [(V_{11} - V_{os})/V_{FSR}(1 - 2 - n)] - 1 \quad (3.3)$$

- V_{FSR} = Voltage Out Full Scale Reference
- V_{11} = Voltage Out all bits on (all 1s code).
- V_{os} = Voltage Measured Offset

The resolution and accuracy of the DAC are very critical to the applications. The Absolute Accuracy Error of a DAC is the difference between the actual analog output and the ideal output expected with a given applied digital code. This error is usually

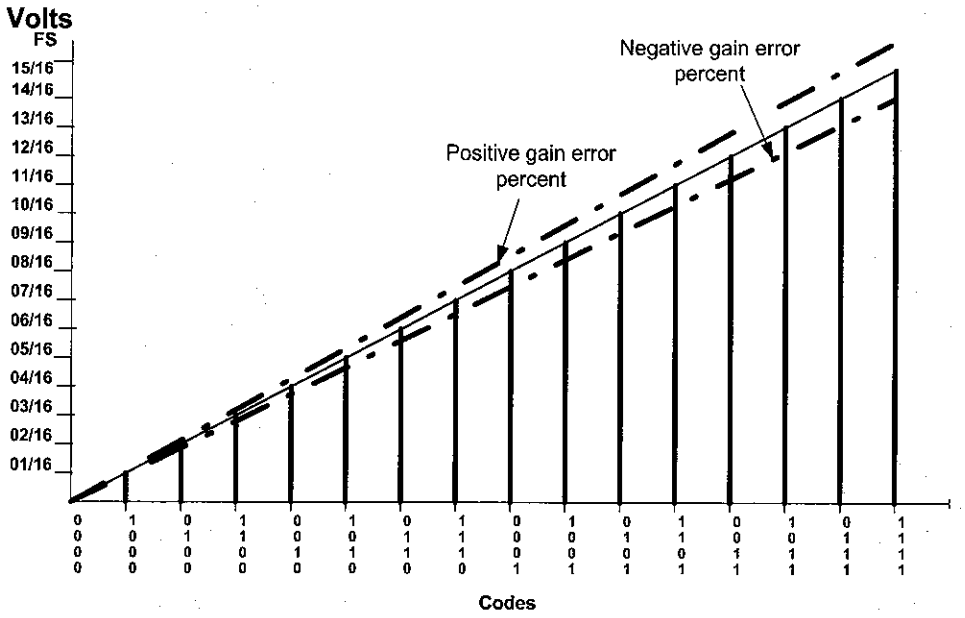

Figure 3.4: 4-Bit DAC Gain Error transfer function.

commensurate with the DAC resolution such as less than 2 -(n+1) or 1/2 LSB of full scale [9].

3.2.1.5 DAC Linearity (INL / DNL)

The description of Linear specifications can be broken into two major categories:

1. Integral Linearity Error or Integral Non-linearity (INL) - It is referred also to as Relative Accuracy as covered in the gain error. It refers to the maximum deviation, at any point on the transfer function curve of the output level, from its theoretical ideal value. This is ideally a straight line between zero volt and full scale ref.

2. Differential Linearity Error (DNL) - The maximum deviation of an actual analog output step, between adjacent input codes, from the ideal step value of + 1 LSB (or $+V_{FSR}/2n$). If the DNL error is more negative than -1 LSB, the DACs transfer function is non-monotonic. As for the DNL, if the error is -1 LSB, the adjacent

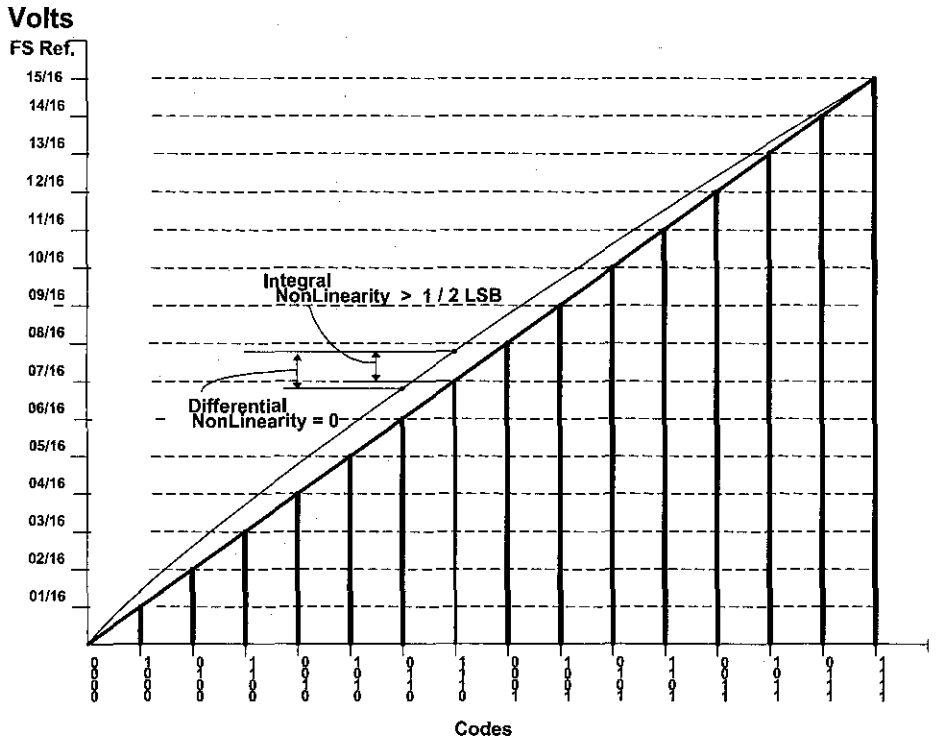

Figure 3.5: Examples of DNL and INL transfer funtion.

output step was equal to zero. A non-monotonic DAC would be one that actually exhibits a lower output value at code N then it did for code N-1. Its transfer function's slope between these two points would be negative. Refer to Figure 3.5.

3.2.2 ADC circuit

The Analog-to-Digital-Converters (ADC) are important interface circuit blocks between analog signals and digital codes which are commonly used in the electronic applications, such as data acquisition, telecommunication, precision industrial measurement, and consumer electronics [30, 49]. As a critical part, the reliability of the ADC performance strongly affects the accuracy of the overall system. Two key performance parameters for ADCs are resolution and speed. Recently, the demand for high sampling rate (more than 1 Gs/s) increases in disk operating system (DOS) and Ultra Wide Band (UWB) system [30]. Flash ADCs are most suitable to meet the requirement of

high conversion rate with the simplest and fastest architecture. Moreover, by using the deep-sub-micrometer technology, the high conversion rate can be achieved.

Similar to the DAC functional criteria, ADC also requires a higher degree of accuracy of voltage reference circuit. This criteria is the most critical part of analog circuit design. To be specific, this is a key factor in defining the precision of a high resolution ADC system. For example, a previous study done on a 14-bit ADC design has shown that ADC requires a significant resolution in order for the thermal sensor to operate. In the study, a temperature coefficient of 0.6 ppm/°C over a range of 100°C is quoted to be a requirement for the operation provided that one LSB variation is allowed [49]. Thus, due to its precise characteristics by utilizing the bandgap reference for biasing, the ADC has been widely used as compared to DAC design due to its better linearity performance.

3.2.3 PLL Circuit

Clock generation using Phase Locked Loop (PLL) in today's micro-processor products requires a lot of effort in the design and validation phases to guarantee wide operating range and good clock quality. Process scaling creates new challenges for analog circuits such as the PLL, making the silicon characterization phase a very critical task.

PLL design issue is mainly related to jitter performance. Jitter is mainly caused by the digital noise on a SOC. To be specific, jitter issue will aggravate the PLLs to cause power supply and substrate noise issues. Figure 3.6 shows the bandgap reference connection to the PLL. Due to being prone to the jitter issue, a voltage regulator V_{ref} is used to provide stable, PVT-insensitive and clean power-supply for PLL. This technique reduces the jitter problem and minimizes the noise. The bandgap reference plays a key role in finding not only the voltage drop across a forward biased diode but also the slope of the current-voltage curve of a forward biased diode levels. In other words, bandgap reference in the PLL design is used to set the voltage and to bias the current. Typically, the voltage drop is pretty stable and it is not influenced by process drifts. As a result,

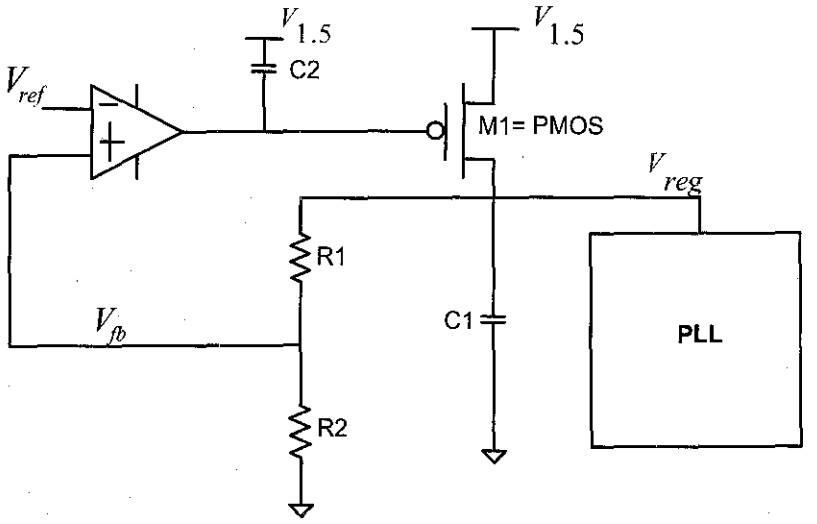

Figure 3.6: Bandgap reference usage on PLL design.

this factor helps in generating a stable reference voltage in a PLL design. It is noted that as the temperature of the diode increases, the voltage drop across a forward biased diode decreases. Therefore, it can be concluded that the voltage difference between two diodes is directly proportional to the absolute temperature.

The bandgap reference requires the use of a higher power supply. Typically the power supply range of the bandgap reference is between 1.2 V to 1.8 V. The V_t mismatch in the bandgap amplifier input dominates the overall regular mismatch. The aim is to have about 3mV offset at the amplifier which is about 20 mV variation at the output. The goal is to have less than 25 mV variation which is 1 sigma variation from the device mismatch whereas the goal for the PVT variation especially at the diodes is about +/- 5 mV.

The bandgap reference is hard to stabilize over the wide I_{load} and C_{load} ranges. Hence, the NMOS source-follower output stage requires more headroom so that it will have faster response and easier to stabilize. As for the PMOS common-source output stage, the goal is to ensure it can handle larger current loads to produce larger V_{gs}.

3.2.4 Thermal Sensor Circuit

Early generations of the thermal sensor designs were limited to off-die solutions, such as heat-sinks or fans. But as microprocessor's power density increased, the off-die schemes were no longer successful in maintaining the die temperature large scale to high volume digital CMOS processes [42]. Today's microprocessors are starting to implement the on-die thermal sensor. The on-die thermal sensor will help reducing the power consumption of the overall temperature system at a minimum [50, 51]. Since, thermal sensor errors are customer noticeable, the high degree of linearity is needed for the thermal sensor to work in a real digital application. There are two key features that act as indicators. The too hot scenario will cause high fan noise, low battery life, premature throttling and in worst case, system shutdown. On the other hand, the too cold event will produce reliability concern and hence will cause overheating [42].

To ensure to maintain the standard of the accuracy measurement, the bandgap voltage reference [8] is used to interface with the on-die thermal sensor circuit. The bandgap voltage reference is used to generate a variable-slope Proportional-To-Absolute-Temperature (PTAT) voltage (V_{ref}) from a ΔV_{be} loop to compare with the temperature dependent diode voltage (V_{be}) for temperature comparison. One voltage is a reference to the throttling temperature and, another set is referred to the catastrophic temperature.

The diode voltage (V_{be}) will produce a negative temperature coefficient. When the two voltages reach the same value or level, the comparator shuts-off. This will cause the programmed temperature to be reached at the desired level. The PTAT slope as a function of temperature, is adjusted by looking into the DAC which controls the current gain. Since the PTAT voltage is not skewed but reversed, an intrinsic non-linearity is revealed. This event happens because any PTAT voltage is centered at 0°K, as described in [43] in equation (3.4) to equation (3.6) for bandgap voltage reference.

$$V_{bg} = V_{be} + A * V_T \tag{3.4}$$

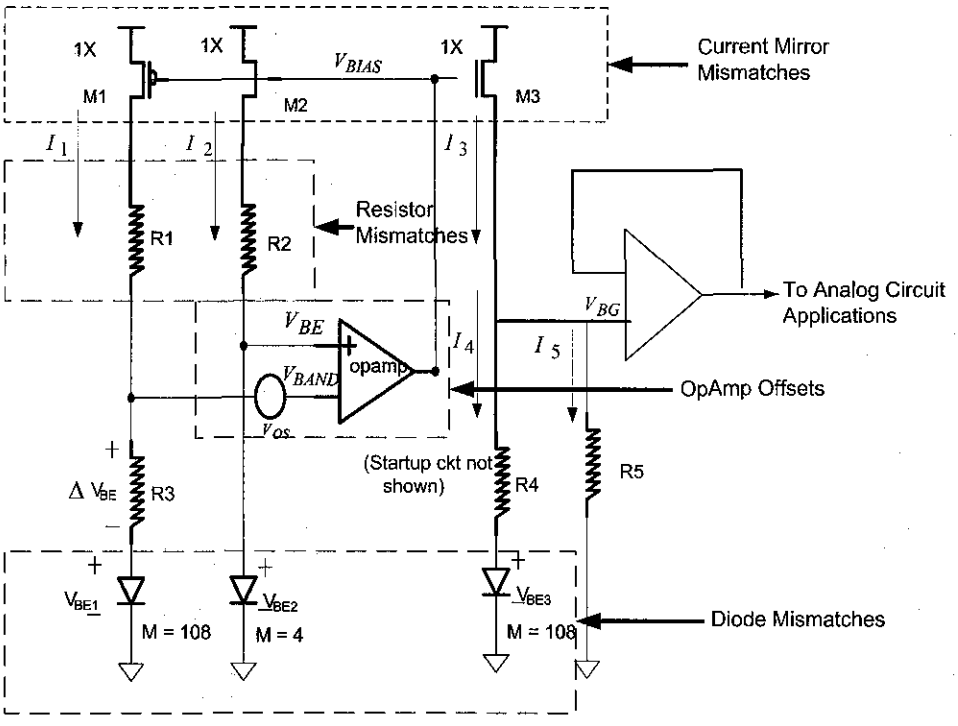

Figure 3.7: Bandgap reference sources of error.

where:

$$V_{be} = N * V_T * ln[\frac{I_c}{I_d} + 1] \tag{3.5}$$

$$V_T = K * T/q \tag{3.6}$$

3.3 Sources of error in bandgap reference

The sources of error in reference circuits, which are extremely vital components must be thoroughly studied. This is due to the fact that the shrinking voltages will cause severe performance inaccuracy. Their relative impact on the reference voltage is particularly essential in the design phase. Therefore, bandgap reference circuits, which play a critical role in today's high-performance wireless and mobile systems, must carefully put a special attention to these errors.

The basic topology of the circuit used for the analysis of error sources in bandgap references is shown in Figure 3.7. The figure shows the building blocks for the typical bandgap reference circuits. The expressions for each sources of error in the reference voltage of this circuit are described in sections 3.3.1 through 3.3.5

3.3.1 Mismatch in current mirror

Mismatch in the current mirror occurs from the variations of the ratio of the current mirror. This variation may happen from various factors such as threshold voltage (V_t) mismatch, width over length (W/L) mismatch, lambda effects of the MOS devices, diode mismatch and resistor mismatch [52].

3.3.2 Mismatch in resistor

In this context, resistor mismatch refers to the polysilicon resistors. This type of resistor uses a silicide block to exhibit high linearity especially to have a high degree of accuracy which is typically around 1%. It has low capacitance to the substrate and has relatively small mismatches. Some studies have proven that the linearity of this resistor in fact much depends on their length, L and width, W [52, 53]. This criteria is necessary for an accurate measurement and modeling for high precision applications.

3.3.3 Mismatch in resistor tolerance

A tolerance is defined as the deviation of any parameter from its nominal value. As a matter of fact, the main contributor of a huge deviation of resistor tolerance, which can be as high as 20%, is the process variation. This variation affects the V_{BE} parameter by changing the PTAT current flowing in the R1 and R2 resistors. Assume the δ_{RA} is the fractional deviation of the resistors tolerance, then the relationship for the error in V_{ref} is given by the equation (3.7):

$$\Delta V_{ref} = -V_t * \delta_{RA} \tag{3.7}$$

3.3.4 Mismatch in operational amplifier

This error has been identified based on some studies as the most sensitive component to mismatch [52]. Some studies have discovered that the phase margin during the op-amp operation causes low yield in the production [54, 55]. In addition, some previous studies have confirmed that op amp is the major contributor to the reliability issue [56, 57]. Efforts have been made to improve the existing op amp performance such as to resize the devices and to increase the phase margin by certain allowable percentage, like 18% while maintaining sufficient margin for Direct Current (DC) gain.

3.3.5 Mismatch in diodes

Diode mismatch is typically caused by the process variation related to the semiconductor fabrication process. The consequence of having a diode mismatch will significantly impact the performance of the particular circuit and hence, will result in a reduced yield of a particular product.

For the specific circuit diagram in Figure 3.7, the two diodes V_{BE1} and V_{BE2} are meant to help minimizing the output voltage swing on the current mirror (M1 and M2). The same thing happens on the other diode V_{BE3} whereby the purpose is to reduce the output voltage swing on the transistor M3.

3.4 Summary

Bandgap reference definition and the nature of its application are discussed. Key applications utilizing bandgap reference in SOC design such as the DAC, ADC, PLL and the on-die thermal sensor circuit are fundamentally described.

It is noted that all applications use the bandgap reference due to the need to have a higher degree of accuracy of voltage reference circuits. The use of a voltage reference circuit for these circuit applications generally require a fully integrated voltage reference with a continuous-time output that exhibits a tight voltage spread and low thermal drift in production.

Various sources of error are noted related to the bandgap reference. Current-mirror mismatch, which causes a mismatch in the collector currents of the bipolar transistors in the core of the bandgap reference, is the dominant source of error. This mismatch is a combination of various errors, namely, V_t mismatch, W/L mismatch, lambda effects of MOS devices, diode mismatch and resistor mismatch.

In the next chapter, the actual reliability simulation and analysis with NBTI-induced of the on-die thermal sensor and DAC circuits are presented.

CHAPTER 4

RELIABILITY SIMULATION

During the circuit performance, the transistor performance especially the key parameters like the drain current, I_{ds}, and the threshold voltage, V_t, will degrade over time. Due to this event, it is very important to develop a reliability simulation. This simulation will estimate this degradation based on the transient simulation of a circuit also known as stress simulation. It will also evaluate the impact of this degradation on circuit performance also known as playback simulation. In this chapter, the choice of the reliability simulator and its key methodology is described. Two case studies,namely the On-die Thermal Sensor and the DAC are described in terms of their voltage and temperature sensitivities in Section 4.4 and Section 4.5 respectively.

4.1 Introduction

With the continued downscaling of feature sizes in digital integrated circuits, the variation of device parameters has become a major concern. During manufacturing, variations of process parameters are inevitable. Hence, performance parameters like power consumption or operating frequency differ from the values they were designed for. After manufacturing the circuit performance degrades over time due to several aging effects that cause a drift of device parameters. These effects must be considered during a timing analysis of an aged circuit. Hot Carrier Injection (HCI) and Negative Bias Temperature (NBTI), previously discussed in the chapter 2, are considered to be the most critical aging effects in current technologies due to process drift. NBTI degrades

PMOS transistor characteristics and its impact can be best modeled by an increase in the magnitude of the threshold voltages. HCI degrades the drain current of both, PMOS and NMOS, transistor types. The traditional approach in a digital design flow to handle reliability concerns, brought up by uncertainties of device parameters, is to introduce safety margins. Those safety margins tend to increase in newer technologies because the relative parameter variations caused by process variations are increasing. Furthermore, an increased impact of aging effects on circuit performance can be observed. This increased impact of aging effects can be explained by the following two reasons; First, the degradation is dependent on the strength of the electric fields occurring in a device. For several technology generations, the feature sizes have been scaled more aggressively than the supply voltage, resulting in an increased drift due to higher electric fields. Second, the sensitivity of a logic gate delay according to a drift of threshold voltage increases with lower supply voltage. Hence, newer technologies are more sensitive to a threshold voltage drift.

Reliability device simulator has become a critical component of the design process. The reliability simulation has successfully demonstrated the model in most of the significant physical failure mechanisms such as TDDB, NBTI, EM and HCI. These failure mechanisms are modeled throughout the circuit design process to ensure that at least the system can operate for a minimum expected useful life [2].

4.2 Choice of Reliability Simulator

A reliability simulator is a tool or software package used for verification of the reliability modeling, which behaves or operates as if the model is a functional system when provided with a set of input stimulus. Several reliability simulators have been developed due to the criticality of ensuring an accurate modeling of major degradation mechanisms such as negative bias temperature instability, hot-carrier injection, and electro-migration. To choose a suitable simulator for this project, a few popular choices are considered, such as Berkeley Reliability Tools (BERT), AgingSim, RelXpert and Foundry DC Calculator.

Table 4.1: Comparison of various reliability simulators [1, 2].

Available Tools	Attributes	Applicability	Disadvantage	Comments
AgingSim	Quasi-static calculations	Intel Process Only	Not applicable for foundry process	Intel Tool
RelXpert	Quasi-static calculations	All Processes	Expensive, requires significant effort and time for deployment	Outsource Tool
BERT	Quasi-static calculations	All Processes	Excessive computational work	Outsource Tool
Foundry DC Calculator	DC Calculations only	Foundry Process	Inaccurate for AC estimations	Outsource Tool

While all the reliability simulators are very powerful and popular, licensing, the ease for debug and the compatibility with other validation languages become the decisive factors.

After some investigation and research, it is understood that most of the simulation tools are not able to support the work. BERT tool, which is an industry simulator, is not able to support the work due to excessive computational and experimental work. The RelXpert tool, which is widely known in the industry, is expensive and requires significant effort and time for deployment. Lastly, the Foundry DC Calculator is only applicable for the Taiwan Semiconductor Manufacturing Company (TSMC) process and it is understood that the tool produces inaccurate simulations for AC estimations.

Table 4.1 summarizes the comparison among various simulators. Looking at the advantages of AgingSim, it becomes clearer for the AgingSim to be adopted for this work.

AgingSim is used to predict changes in device and circuit performance over a product's lifetime. It further allows the simulation of post-degraded circuits to ensure that circuit designs meet reliability requirements at end-of-life [6, 58]. The framework of aging circuit design methodology discussed in this chapter is shown in Figure 4.1. The AgingSim will be run to cover the variations in Process, Voltage and Temperature (PVT).

Analog circuit designers should already have the skills to design the circuit that meets the design specification at the beginning of the design stage. Now circuit designers need to move one step further to include device aging impact into consideration, so that the circuit can still meet the specification at End-Of-Life (EOL). This can only be

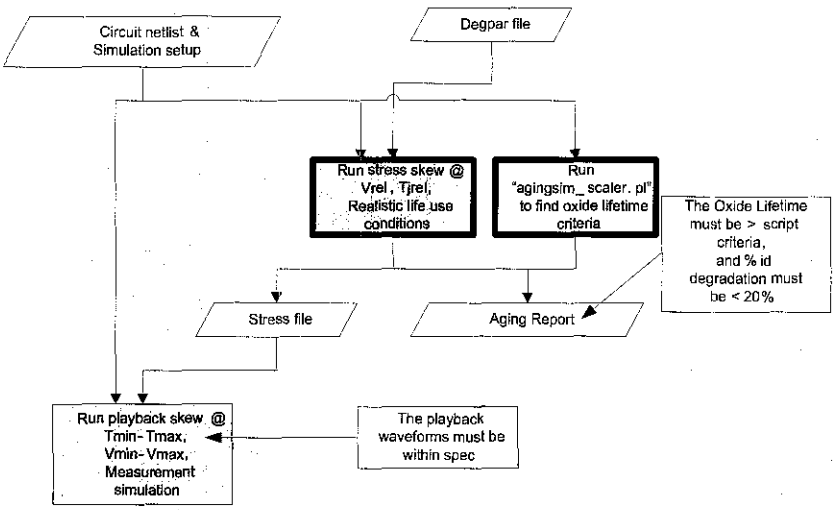

Figure 4.1: Reliability simulation flow

achieved by running all necessary reliability simulations, and it must be a standard part of any special circuit design procedures and be thoroughly reviewed [6].

Usually, for quality and reliability requirements such as hot electron, self-heat, electro-migration, latch-up, etc, these failure mechanisms can checked and fixed after the designs or even after circuit layouts are done. However, special attention needs to be paid for issues such as NBTI degradation, in particular the special circuits. Any thermal sensor issues require changes in circuit schemes, and the late identification of possible issues will cause negative consequences. Designers need to consciously pay attention to the transistor NBTI degradation during the design phase to make conscious choices to minimize the circuit sensitivity to NBTI.

For analog circuits, which is sensitive to within die variances, AgingSim provides the aging diagnosis capability. AgingSim can be used to study the impacts of aging differentials only, or can add the aging differentials on top of various process variances at time zero to obtain the realistic performance distribution or failure rate of the circuit at end of life. AgingSim must be performed to obtain a realistic risk evaluation for the reliability qualification of the circuit design. Without thorough reliability awareness, the analog circuits are susceptible to mismatches and thus impact the overall circuit performance [6].

The effectiveness of the reliability simulator specifically for this project has been proven and verified across major process technologies since the early 250nm until the recent sub-micron process technology such as the 14nm technology. Major mainstream CPU have used this reliability simulator effectively particularly for speed path analysis. During the early development of the simulation tool, it was hard to correlate the results. For example, many CPU products were attempting to approximate burn-in data to 7 year simulations. It was found that the results will correlate when the users use the correct inputs. Across many process technologies, this reliability simulator has been experiencing major improvements. Truly, this reliability tool can predict correct behavior as compared to post-stress silicon behavior.

4.3 Methodology

The first step in the simulation methodology of this case study is to enable reliability analysis of the analog SOC particularly the on-die thermal sensor and the DAC due to NBTI-induced circuit aging. Large magnitudes of voltage and temperature variations can occur even during several instants of microprocessor execution, leading the motivation to study this reliability failure mechanisms even deeper [59].

This simulation study gives an opportunity for observing voltage and temperature variations. The methodology is event-driven, where at each workload arrival or finish, NBTI as part of the critical reliability failure mechanisms is invoked. Depending on the way the circuit designers define the reliability model, the simulation result can be varied by varying the voltage and temperature knobs; this results in a significant NBTI degradation. Hence, voltage and temperature are sampled at each workload event and the corresponding NBTI failure rate is computed.

Reliability simulator estimates the transistor performance such as I_{DSAT} and V_t degradation based on the transient simulation of a circuit under stress. It evaluates the impact of this degradation on circuit performance under playback simulation. Reliability simulator not only models Negative Bias Temperature Instability (NBTI) but also

models Hot Carrier Injection (HCI) and other devices reliability modes. The simulator uses a combination of other simulators to complete the whole AgingSim.

For a specific NBTI mechanism, the physical model of the simulator is based on equations (4.1),(4.2),(4.3) and (4.4). This equation as explained in [1] shows the threshold voltage shift of PMOS transistor with different design parameters.

$$TTF(s) = MTTF * f(V_{TP}, L) * A \tag{4.1}$$

$$A = exp(-\gamma * E) * B \tag{4.2}$$

$$B = exp[\frac{E_a}{k} * [\frac{1}{T_j + 273} - \frac{1}{398}] * C]^{\beta} \tag{4.3}$$

$$C = \frac{[}{\delta V_{TP}} * FC \tag{4.4}$$

The parameters in (4.1),(4.2),(4.3) and (4.4) are as follow:

- E is electric field (V/T_{ox}) across gate oxide
- T_j is the junction temperature
- $MTTF$ is mean time to failure
- $TTF(s)$ is scaled time to failure in seconds because of voltage and temperature scaling
- $F(V_{tp}, L)$ is geometry scaling function for aging
- E_a is thermal activation energy
- FC is V_t shift defined as failure criterion for modeling.
- β is the process dependent variables.

The shift in V_t, the threshold voltage for a time varying waveform, as elaborated in [1] can be calculated using the quasi-static time integral in (4.5).

$$TTF = \frac{1}{\frac{1}{t'} * \int \frac{dt}{TTF(t)}} = \frac{1}{Avg(1/TTF(t))} \tag{4.5}$$

In stress mode, the reliability simulator calculates the transistor V_t shift, using the complete simulated waveform and equations (4.1), (4.2), (4.3) and (4.4). In playback mode, the simulator re-runs spice simulations with a degraded threshold voltage to calculate the shift in delay after aging.

It is noted that even though NBTI degradation occurs under elevated voltage and temperature, the NBTI phenomena do show some levels of relaxation [4]. There are two types of relaxation that need to be seriously considered for the circuit reliability modeling.

1. Fast relaxation : This relaxation occurs as soon as the stress is removed. It is responsible for reduced AC degradation even after accounting for the transistor ON time. However, this relaxation mode is not covered in this reliability simulation.

2. Extended relaxation : This relaxation occurs as the device is kept unbiased. This reliability tool has already accounted for this relaxation mode into the simulation. Most of the aging data have already been accounted for this relaxation since the devices are tested much later after they have been removed from stress.

   Because of the above two relaxation modes, a device under continuous usage may suffer a higher degradation than what the reliability simulation predicts. Figure 4.2 illustrates the two relaxation modes.

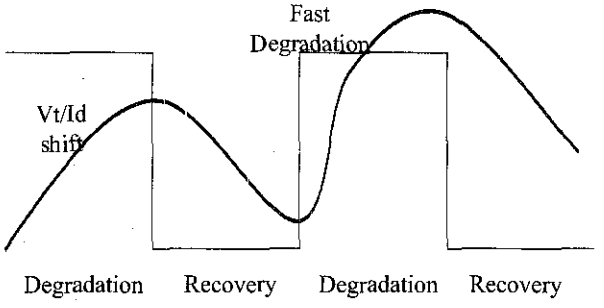

Figure 4.2: NBTI periodic stress and relaxation [4].

4.3.1 Assumptions of the reliability simulation model

Reliability simulation models are often used to extrapolate failure rates. Therefore, it is very important to validate whether the models chosen are consistent with whatever data are available. This section describes several assumptions used to ensure the model used for this case study is acceptable.

1. Constant failure rate assumption: According to J. Bernstein *et al.* [60], it is critical to use an exponential distribution for a complex electronic application to estimate the overall failure rate. Even though most of the key circuit reliability failure mechanisms such as NBTI, TDDB and HCI do not correlate with the exponential distributions, it is justified to use this assumption due to the criticality of such events to occur. J. Bernstein *et al.* [60] in their comprehensive reliability modeling development also have demonstrated that it is not necessary to figure out the distribution for each of the failure mechanism's failure rate. In addition, an article by Reliasoft has a similar argument that implies the urgency to run reliability simulation under the actual usage conditions. Several mathematical models have been developed, implemented and well explained but the benefits are far from what have been gained in the actual usage conditions [61] . Both statements suggest that the failure rate for each of the failure mechanisms will be averaged out in order to produce a constant level of the failure rate based on realistic usage conditions.

2. Equal contribution assumption: This assumption is subjected to the failure analysis results which leads to determining the actual distribution of field failures. J. Bernstein *et al.* [60] commented that this assumption is about how the device is designed properly as minimum reliability failure mechanism as possible. Due to the reliability awareness, electronic components are now designed at the reasonable cliff of the design specifications. When any potential failure mechanism arises, specific design and manufacturing techniques will be developed to mitigate the risk of the failure. This assumption is the extension of the first assumption whereby not even one failure mechanism dominates. All are equally likely and the resulting failure distributions are similar to the constant rate processes.

3. Proportional acceleration assumption: It is shown by J. Bernstein *et al.* [60] that the constant failure rate-based reliability for electronic components allows the manufacturer to test parts under accelerated conditions on condition that all failure mechanisms are accelerated in approximately the same proportion. Data extrapolation can be done once the result of the failure rate is available taking into account factors such as applied voltage, temperature, and speed of the devices. However, the drawback is that the accelerated stress test may cause reliability problems if this assumption is wrong. Therefore this assumption needs to be thoroughly analyzed and done right at the first time.

4. Linear superposition assumption: System failure rate is linearly modeled as a sum of individual failure mechanisms. This assumption is not taking the consideration of interactions with different reliability failure mechanisms. For example, NBTI may overlap with the HCI event, but the interrelation is too complicated and is typically insignificant and negligible.

5. Technology dependence assumption: All model parameters for each failure mechanism are dependent on process technology. For different process technologies, model parameters typically vary, but for the same process technology, they are assumed to be constant. This assumption allows technology and circuit designers to mitigate the risk of the proven model parameters by characterizing with typical

sample structures to determine the robustness of each model parameter. Furthermore, both technology and circuit designers can use these extracted model parameters to estimate the failure rate of by the same process technology.

4.3.2 Stress Mode

A "Stress" Mode is used to calculate the amount of device degradation after arbitrary periods of time. During this mode, the AgingSim will calculate device degradation during a short transient simulation and extrapolate the degradation out to the desired degradation time. This mode is run under the assumption that the signal from the short transient simulation is repeated throughout the entire degradation time. At the end of the stress mode, the simulation will create an age report containing the end-of-life degradation values for each transistor.

4.3.3 Playback Mode

Unlike "Stress" mode, the "Playback" mode is used to simulate degraded circuit performance based on Stressing Mode results.

In general, the AgingSim flow allows circuit designers to define the "Stress" and "Playback" corner list in the global corner definition file which can be used by all the circuit designers who are working on the same interface design or reused for other project. In the design flow, circuit designers can define a normal corner list together with the "Stress" and the "Playback" corner list in the script to kick off the regression in parallel. Hence, the final result table will display all the normal corners and AgingSim corner's run results for comparison. This table is needed in order to quickly identify any circuit performance issues.

4.4 Case Study 1 : On-Die Thermal Sensor Reliability Prediction

The on-die thermal sensor has performed a simple but important task for many generations of Intel processors. Its purpose is to monitor the junction temperature on-die and to determine whether the operating temperature has exceeded the pre-programmed the hot processor (PROCHOT) reference temperature. This thermal management feature allows the system designer to design cooling solution based on real-life power consumption, not peak power. Should the junction temperature (T_j) rise above the PROCHOT trip point, the processor throttles its frequency and voltage in an effort to maintain a T_j at or below the trip point.

To demonstrate good and consistent linearity across voltage and temperature, the on-die thermal sensor has been selected as a vehicle in this case study. The key motivation is to observe how severe is the NBTI mechanism affecting the on-die thermal sensor performance.

4.4.1 On-Die Thermal Sensor Design

Temperature monitoring sensors can be categorized either as off-die or on-die whereby they are either built-in or embedded into the silicon design.Off-chip techniques can be further sub-classified as based either on the contact methods or the non-contact methods. Example of the usage of contrast materials such as liquid crystals, phosphorus or the use of Atomic Force Microscopes. In contrast, the non-contact methods include infrared thermography, reflectometric and interferometric techniques. Since all these techniques require a direct optical access to the silicon die, they are usually restricted to failure analysis [62].

On-die thermal sensors have a silicon area overhead but they provide significant flexibility for the test procedure, allowing both laboratory and in-field testing. The built-in thermal sensor output can be proportional to the absolute temperature or could be proportional to the difference of temperature at two points of the silicon surface.

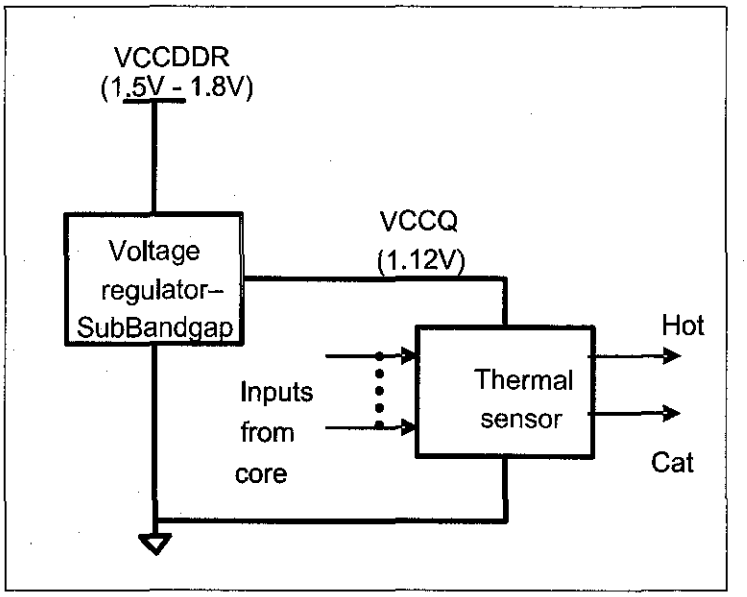

Figure 4.3: Thermal Sensor Block Diagram.

Thus, implying the need for two temperature transducers, and relative temperature measurement [63].

On-die thermal sensors are preferred over off-die ones because of their fast response, low cost and the fact that they can be designed for low area and low power overhead [62]. However, the drawback is that they have additional design constraints such as CMOS process technology compliance, unregulated power supply and calibration limitations. Also, in an on-chip thermal sensor, the reference will be susceptible to the same inputs as the sensor. Built-in/on-chip thermal sensors can be classified on the basis of their output type, circuit type and process technology [42].

The block diagram of the on-die thermal sensor circuit used in this case study is shown in Figure 4.3. The circuit consists of the thermal sensor and a voltage regulator with a Double Data Rate (DDR) power supply (VCCDDR) of 1.5V-1.8V. The output stage logic power voltage (VCCQ) of 1.12V supplies the thermal sensor.

The thermal sensor allows the system designer to design a cooling solution based on the real-life power consumption, not the peak power. If the junction temperature, T_j, rises above the hot trip point, the micro-processor throttles its frequency and voltage

in an effort to maintain T_j at or below the trip point. Another output from the thermal sensor is the catastrophic shutdown (Cat). This is a feature that prevents permanent damage to the micro-processor should hot thermal management fail allowing the micro-processor to go into thermal runaway. It accomplishes this by disabling all clocks and asserting a special thermal sensor signal, which will cause the system to collapse the Vcc supply and prevent leakage from heating the processor further. The Cat event indicator must trigger below the threshold where damage occurs to the micro-processor, but above the hot trip point.

Bandgap voltage reference, as illustrated in Chapter 3, Figure 3.1, is a high-performance analog circuit for applications in a host of analog, digital, and mixed-signal integrated systems [1]. For all these applications, the accuracy of the bandgap reference voltage is crucial as it can severely limit system functionality. This is especially very important in the case of sensitive blocks like thermal sensors [52]. The thermal sensor is an on-die analog circuit used by microprocessors for clock throttling, thermal catastrophic protection, and power management. Unlike thermal diodes, with no external pin limitation, thermal sensors can be placed in multiple locations within a microprocessor to capture the within-die temperature profile [54]. However, on-die thermal sensors usually have poorer accuracy than the external temperature sensing chips used by thermal diodes, which are fabricated on the trailing edge analog CMOS processes [42].

The DAC based circuits rely on the comparison of a PTAT voltage and a complementary to absolute temperature (CTAT) base-emitter voltage for temperature measurement, without the need of an accurate ADC [64]. They are relatively simple to implement but are difficult to deliver with good quality over a wide temperature operating range [51].

The circuit as illustrated in Chapter 3, Figure 3.1 generates a variable-slope PTAT voltage (V_{REF}) from a ΔV_{BE} loop and compares it against the diode voltage (V_{BE}). The V_{BE} has a negative temperature coefficient so when the two voltages reach the same level, a comparator trips, indicating that the programmed temperature has been reached [65]]. PTAT slope as a function of temperature is adjusted using current DAC

with variable gain M. Since the PTAT voltage is not shifted but rotated, intrinsic non-linearity is introduced. This occurs because any PTAT voltage is pivoted at 0°K, as described in [42] in the following equation for V_{REF} [66].

$$V_{REF}(T) = M[\frac{nKT}{q}\ln N - V_{off}]\frac{R_{VREF}\Big|_{T-T0}}{R_b\Big|_{T-T0}} \tag{4.6}$$

$$V_{SBG} = [\frac{R5}{R4+R5}]V_{BE3} + [\frac{R5R4}{R3(R4+R5)}][\frac{KT}{q}\ln\frac{A1}{A2} - V_{OS}] \tag{4.7}$$

If R5=∞, then I4=I3

$$V_{SBG} = V_{BE3} + [\frac{R4}{R3}][\frac{KT}{q}\ln\frac{A1}{A2} - V_{OS}] \tag{4.8}$$

$$V_{SBG} = V_{BE3} + I3I4 \tag{4.9}$$

Equation (4.6) is based on the schematic of the thermal sensor circuit as illustrated in Chapter 3, Figure 3.1. All transistors are sized and biased such that they are operating in saturation region. Transistor M1 provides a bias for the current mirror PMOS transistors (M2 and M3). The drain current of the current mirror PMOS transistors (I2 and I3) drives the diode connected to the op-amp, generating voltage difference of V_{BE} and V_{BAND}. The output of the op-amp is connected to M3 which then connects to the thermal sensor circuit. Equation 4.7 to 4.9 compares the PTAT (V_{REF}) against the V_{BAND} voltage, which is obtained by placing a diode and a resistor (GB N_{Well}) in series. The diode voltage (V_{BE}) has a negative temperature coefficient and the resistor has a positive temperature coefficient but not as large as that of the V_{BE} in absolute value. Thus, the total temperature coefficient for V_{BAND} is still negative since V_{BE} dominates. When the two voltages are crossed, a comparator will trip, indicating that the programmed temperature has been reached.

4.4.2 AgingSim Process Step

NBTI simulation is performed using the AgingSim tool covering electrical over-stress analysis and statistical simulations. The AgingSim and analysis are done in Cadence Analog Artist environment based on the circuit as illustrated in Chapter 3, Figure 3.1. For this case study, the NBTI behavior of the thermal sensor circuit under normal and extreme conditions was simulated. Thermal sensor AgingSim was run in a 3-Step Process.

1. Generate a fresh (non-degraded) waveform at the typical circuit operating condition (VCC and Temperature).

2. Turn on the AgingSim Stressing Mode to calculate the amount of degradation on each transistor. This was done at a slightly higher voltage and temperature to get a more conservative estimate of the degradation.

3. Turn on the AgingSim Playback Mode to simulate the degraded waveform, using the degradation calculated in the Stressing Mode. This was done at the operating conditions used for the fresh simulation (step 1), in order to make the comparison between fresh and degraded waveforms.

Out of these three steps, step 3) is the most general representation in which the stressing mode simulation does not have to be at the same conditions as the fresh and degraded simulations. If quality and reliability specifies that the Stressing Mode can be run at the normal operating condition (same as fresh and degraded simulations), then steps 1 and 2 can be combined into a single operation. In this case study, the fresh curve was generated at the same time as the age report.

AgingSim playback mode analysis was done under the following conditions on three standard corners.

1. RSSS refers to a slow corner
2. TTTT refers to a typical corner
3. RFFF refers to a fast corner

The simulation, which covers these three process corners, uses the pre-layout schematics with proper loading. For this analysis, the circuit was aged for 7 years life time to check the thermal sensor circuit functionality and the effect of NBTI degradation under burn-in mode conditions. Table 4.2 shows the AgingSim parameter settings at time zero, stressing and playback modes. In order to guarantee a good coverage of reliability analysis, a process skew is almost mandatory. The skewing of the process corners means the difference in propagation delay times between corresponding outputs on any two like devices when both devices operate under identical conditions. Process skew quantifies skew due to process variation in the manufacturing process (skew caused by lot-to-lot variation). It excludes variations in supply voltage, operating temperature, output loading, input edge rate, input frequency, etc. Hence, process skew is an output skew over several devices covering slow, typical and fast corners in all 3 different modes. For the fresh mode, the stress voltage is at 1.8V nominal whereas for the burn-in and age modes, the stress voltage is elevated at 2.5V. As for the temperature, the difference between the fresh and the burn-in mode is by 10°C. Last but not least, the fresh mode is obviously defined to be time zero, the burn-in mode is at 500hrs and the Age mode is simulated to 7 years lifetime. These parameters were used for the AgingSim of the on-die thermal sensor.

The result in Table 4.3 revealed that under burn-in condition, the thick gate oxide in the thermal sensor circuit block has bigger lifetime prediction margin which is until 1000 years of operation. As a matter of fact, the lifetime of the thick gate oxide at time zero and after burn-in stress remains the same. On the other hand, the thin gate oxide has shorter lifetime prediction, which can only survive between 11.5 days for NMOS thin gate oxide to 1.85 months for PMOS thin gate oxide. This analysis has proven that the thick gate oxide reliability is more robust as compared to the thin gate oxide reliability.

To further zoom into a specific thermal sensor block AgingSim analysis, the matched devices were analyzed and a slightly different degradation behavior was observed. The degradation of the matched devices in V_{REG} Operational Amplifier (Op Amp) was reported having slightly different degradation percentage between 0.36% and 1.73% as

Table 4.2: AgingSim Settings across 3 different modes.

Parameters	Fresh	Burn In (Stressing Mode)	Age (Playback Mode)
Stress Skew	Slow,Typical, Fast	Slow,Typical, Fast	Slow,Typical, Fast
Stress Voltage	1.8V	2.5V	1.8V
Temperature	100'C	110"C	110'C
Use time	Time 0	500 hrs	7 years

Table 4.3: AgingSim - Post Stress Result.

Paramater		Fresh Condition	Burn-in Condition
Gate Oxide Lifetime			
	Thin N	232 Yrs	11.5 Days
	Thin P	188 Yrs	1.85 Months
	Thick N	1000 Yrs	1000Yrs
	Thick P	1000 Yrs	1000Yrs
	Pass/Fail	Pass	Pass

indicated in Table 4.4. These two matched devices were expected to have similar I_{dsat} percentage but transistor M1213 had about 1.73% degradation. After thorough investigation on the specific node, the degradation was deemed acceptable to be below the allowable percent degradation. The goal was set to be below 10% degradation.

AgingSim covers a range of process, voltage and temperature (PVT) and therefore it is very crucial to perform analog aging verifications across multiple PVT conditions.

Table 4.4: Matched devices in Op Amp.

Oxide Lifetime	percent Id (%)	Idmax (mA)	Vt shift (V)	Vt mismatch (mV)	Node
1000y	2.29E-32	0.03073			M1220
1000y	2.15E-32	0.0303			M1221
1000y	2.047	-0.05951	-0.01179	2.329	M1210
1000y	2.047	-0.05952	-0.01179	2.329	M1211
1000y	2.047	-0.06136	-0.002071	2.329	M1215
1000y	0.3612	-0.02976	-0.009918	0.9102	M1212
1000y	1.726	-0.02946		1.99	M1213
1000y	6.07E-33	0.02945			M1225
1000y	2.05E-33	0.02939			M1226
1000y	0	0.02943			M1224
1000y	0	0.0294			M1227
1000y	0	0.04549			M1228
1000y	0	0.06141			M1229
1000y	5.35E-22	0.352			M1230
1000y	0	0.352			M1231
1000y	0	0.06031			M1232

In special circuits like thermal sensors, NBTI can pose a serious reliability concern as even a small variation in bias currents can cause significant gain errors [67].

4.4.3 Voltage Sensitivity Analysis

Higher voltage difference between gate and source will result in a higher degradation. As explained in the theory [19, 68], this is a result of the higher electric field causing a larger number of interface traps. According to Schroder et al. oxide electric field enhances NBTI and causes certain key process parameter to be shifted [5]. This scenario is determined by measuring the time-to-fail (TTF).

TTF in [5, 18] is a function of the following relationship:

- When the stress voltage, V_{stress}, increases, the TTF decreases.
- When the difference between the nominal voltage, VCC, and V_t increases, the TTF goes down.
- Last but not least, as the temperature goes up, the TTF will be on the opposite direction.

The worst case situation is when the unit is operated or is kept at a high voltage most of the time, but operated at low voltage sometimes [32].

Figure 4.4 shows the thermal sensor voltage output comparison between the before-stressed and the after-stressed simulations. Looking at the waveforms, the simulations clearly show that any mismatch developing by the thermal sensor circuit shifts the output characteristic by roughly the amount of the threshold voltage difference. The post stressed simulation represents after 7 years, which is a typical product lifetime. Of note, it was observed that the thermal sensor DC output characteristic shifted to right side of the before-stress curve. The implication of the degradation is that it lower the drive current, I_d and hence, slowing down the circuit operation.

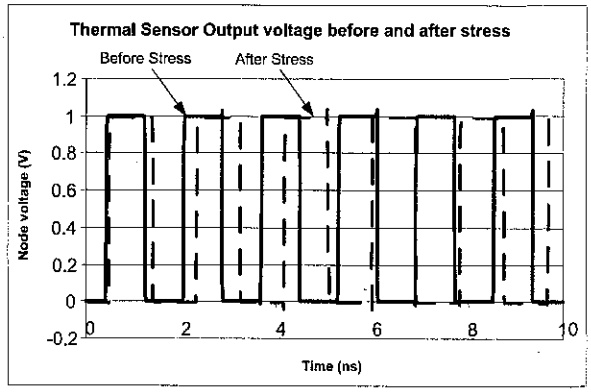

Figure 4.4: AgingSim Voltage variations.

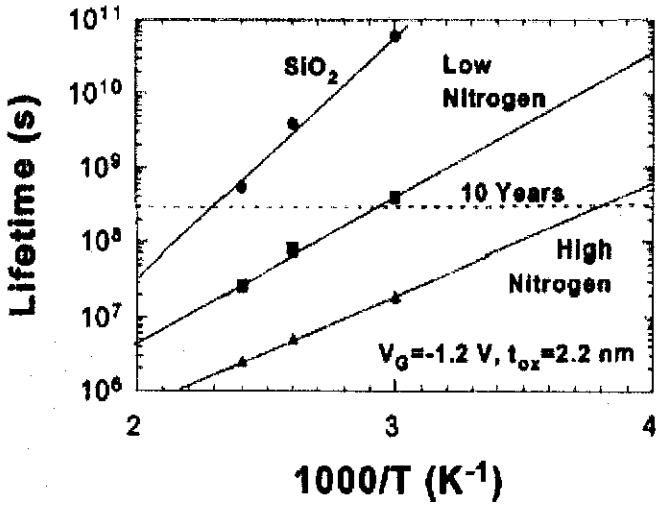

Figure 4.5: Lifetime as a function as temperature [5].

4.4.4 Temperature Sensitivity Analysis

Higher temperature stress significantly enhances NBTI effects. (Proportional to $\sim T^4$) [18]. Figure 4.5 shows the relation between NBTI lifetime and nitrogen concentration in the gate insulator. The increase in nitrogen concentration, which suppresses boron penetration for the scaling-down gate insulator of PMOS transistor, causes the degradation of NBTI characteristics. As indicated in [18], there are 3 key equations that show the temperature relationships to the NBTI. Equation (4.10) shows the interface trap density is inversely proportional to the oxide thickness t_{ox} while Equation (4.11) reveals the fixed oxide charge is independent of t_{ox}. The relationship between Equation (4.10) and

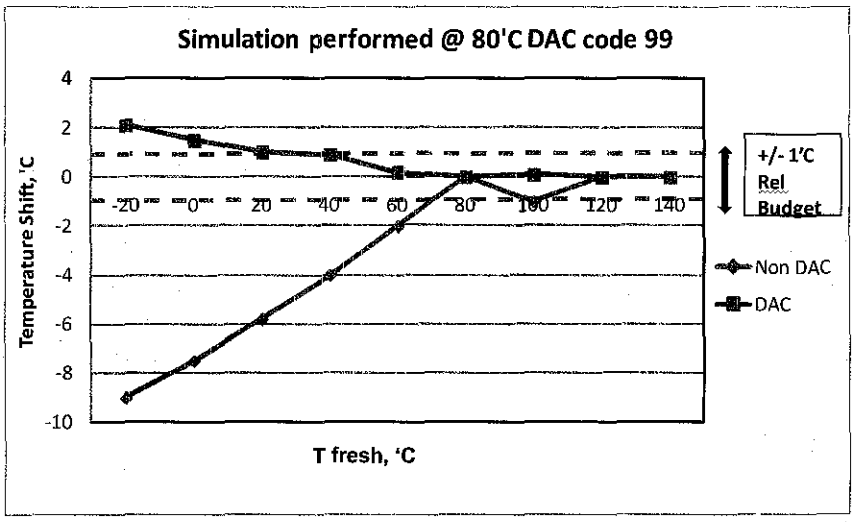

Figure 4.6: AgingSim considering temperature variation.

(4.11) suggest that NBTI is worse for thinner oxides. However, this is not always observed because NBTI is highly dependent on the process conditions. Equation (4.12) shows the dependence of V_t shift on inverse of the stress temperature (1/T). As a result, NBTI degrades more severely the higher the temperature. High performance microprocessors and SOCs can have hot spots in a circuit design leading to large temperature gradients across a chip.

$$\Delta N_{it} \propto \exp \frac{0.2}{kT} \tag{4.10}$$

$$\Delta Nf \propto \exp \frac{-0.15}{kT} \tag{4.11}$$

$$\Delta V_t = f(\Delta N_{it}, \Delta N_f) \tag{4.12}$$

where:

1. N_{it} is the interface states
2. N_f is the fixed oxide charge

Figure 4.6 shows the AgingSim temperature profile of the thermal sensor circuit. The line points and the dotted points were used to compare between the DAC circuit and the non-DAC circuit building block that connects to the thermal sensor circuit. The temperature difference (-30°C~130°C) resulted in an aging difference of up to ±1°C between the lowest temperatures to the highest.

It is important to know accurately what each unit is going through, from a temperature perspective, at each burn-in session. This can be achieved through the thermal sensor and a proper calibration of the thermal sensor at a unit level. Hence, it is critical to observe that NBTI is highly sensitive to the operating temperature. The amount of degradation observed is strongly dependent on the temperature of the chip [36].

4.5 Case Study 2 : Digital Analog Converter Reliability Prediction

The function of the DAC circuit is to drive an analog signal where the luminance of the signal is coded as the output voltage swing [69]. It is a key circuit to the graphics engine which is used to drive a cathode-ray tube (CRT) type analog display. The CRT DAC is a precision analog circuit that requires thorough characterization since many of the performance aspects of the CRT DAC are not feasible or cost-effective to be tested during high volume manufacturing. The CRT DAC performance is critical since its performance directly affects the display quality and since poor visual quality can lead to eye fatigue.

To demonstrate a good and consistent performance across voltage and temperature, the CRT DAC has been selected as a second vehicle in this case study. The key motivation is to observe the severity of the NBTI mechanism affecting the CRT DAC performance.

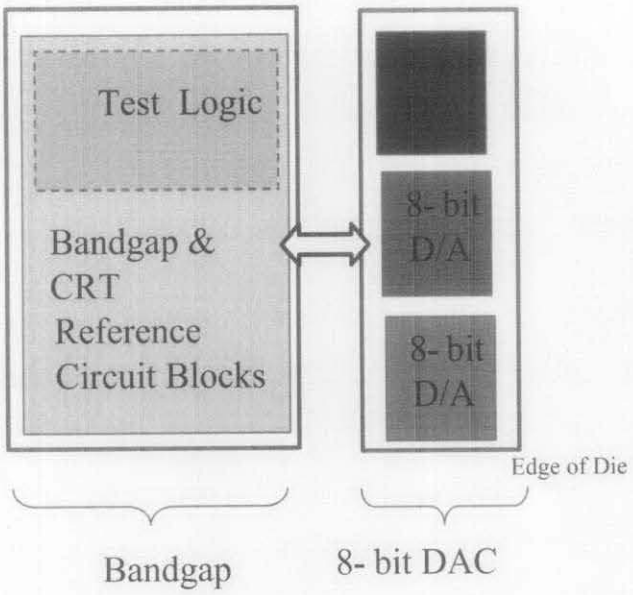

Figure 4.7: The 8-bit CRT DAC block diagram.

4.5.1 Digital Analog Converter Design

Even though a device pair mismatch of 1 mV to 2 mV may seem to be insignificant, certain special circuits do require absolute levels of matching. One of the examples is a DAC circuit. A DAC requires extreme level of matching [8]. The typical 8 Bit CRT DAC used to produce the signals required to drive the RGB guns of a CRT-based PC monitor are usually current source based circuits. Figure 4.7 shows the high level block diagram showing the bandgap interface with the 8-bit CRT DAC.

Memory controller chip designs that integrate a graphic engine to support enhanced video applications have become an important feature as well as a major cost reduction aspect for the PC platform. Future chip designs will continue to integrate a graphic engine on-die to provide original equipment manufacturers the flexibility to design cost-effective PC platforms without the need for an external video card. It is therefore essential to perform a thorough characterization of the video DAC for each chip product that integrate the graphics engine.

The performance of the DAC is critical for achieving excellent video quality. The required accuracy of the DAC is based on the differential gain and the phase distortion

specifications for TV. The architecture is designed as a current-steering architecture to achieve high accuracy and low distortion of the analog video signal from the motherboard ground level, i.e. zero volts, to the maximum nominal analog video signal swing of 1.3 V. The digital input to each DAC is latched on the rising edge of each clock and converted to an analog current. For a given digital input, the current source outputs are either summed together and directed to the output pin or directed to the motherboard ground plane by the differential current switches. An analog video voltage is created from the DAC output current flowing into the termination resistors. The video level specifications for the various video formats along with the effective load termination determine the required output current of the DAC circuit. The Least Significant Bit (LSB) output voltage is a function of the video format supported and normally ranges between 684 μV to 1.27 mV above the motherboard ground.

Knowing the circuit mismatch sensitivity on this special circuits, paired devices are typically designed using longer dimensions, i.e. the L and W values of the CMOS transistors. The main purpose is to minimize process variation and to meet the desired initial matching characteristics and requirements.

To meet the minimum requirement for 10-bit accuracy, the digital input word must have an error less than 50 percent of the LSB. To calculate the sensitivity of a device mismatch, the Integral Non-Linearity (INL) can be used as an example. The INL is defined in [17] as the maximum deviation from the ideal DC transfer curve, and for an N-bit DAC, it can be expressed as equation (4.13)

$$INL \approx \sqrt{2^{N-1}} * \Delta I_d / I_d * LSB \tag{4.13}$$

4.5.2 AgingSim Process Flow

NBTI simulation for the DAC circuit is done through AgingSim covering electrical over-stress analysis and statistical simulations. The AgingSim and analysis are done in

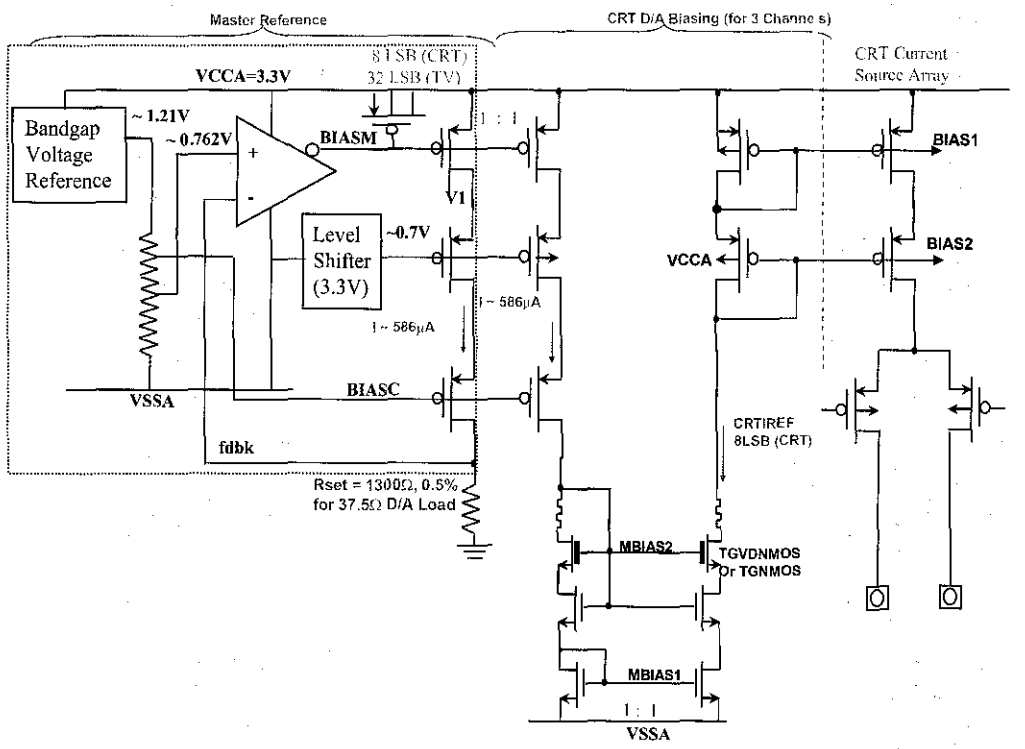

Figure 4.8: Simplified circuit diagram of 8-bit CRT DAC [1].

Cadence Analog Artist environment based on the circuit in Figure 4.8. For this case study, the NBTI behavior of the DAC circuit under normal and extreme conditions was simulated, similar to simulation conducted on the first case study explained in Section 4.4.2.

DAC AgingSim was also run in a 3-Step Process.

1. Generate a fresh (non-degraded) waveform at the typical circuit operating condition (VCC and Temperature). In DAC case, the nominal voltage and temperature are set at 3.3V and 100°C respectively.

2. Turn on the AgingSim stressing mode to calculate the amount of degradation on each transistor of the current source and the differential switch. This was done at 4.6V and 110°C to get a more conservative estimate of the degradation.

Table 4.5: AgingSim parameters across three different conditions

Parameters	Fresh	Burn In (Stressing Mode)	Age (Playback Mode)
Stress Skew	Typical	Typical	Typical
Stress Voltage	3.3V	4.6V	3.3V
Temperature	100'C	110"C	110'C
Use time	Time 0	500 hrs	7 years

3. Turn on the AgingSim playback mode to simulate the degraded waveform, using the degradation calculated in the stressing mode. This was done at 3.3V and 100°C for the fresh simulation (step 1), in order to make the comparison between fresh and degraded waveforms.

Similar to the simulation run on the first case study, step 3 is determined to be the most general representation in which the stressing mode simulation does not have to be at the same conditions as the fresh and degraded simulations. If quality and reliability specifies that the stressing mode can be run at the normal operating condition, which is the same as fresh and degraded simulations, then steps 1 and 2 can be combined into a single operation. In this case study, the fresh curve was generated at the same time as the age report.

AgingSim playback mode analysis was done under the typical corner (TTTT). The analysis was done by invoking the DAC schematics layout with proper parameters loaded. For this analysis, the circuit was aged for 7 years life time to check the DAC circuit functionality and the effect of NBTI degradation under burn-in mode conditions. Table 4.5 shows a comparison among three different conditions.

4.5.3 DAC Circuit Design

Under a specific DAC block AgingSim analysis, the analysis is primarily focused on the matched devices in Figure 4.9. After a thorough analysis is done, the matched devices reveal a slightly different degradation behavior. Ultimately, the DAC design is

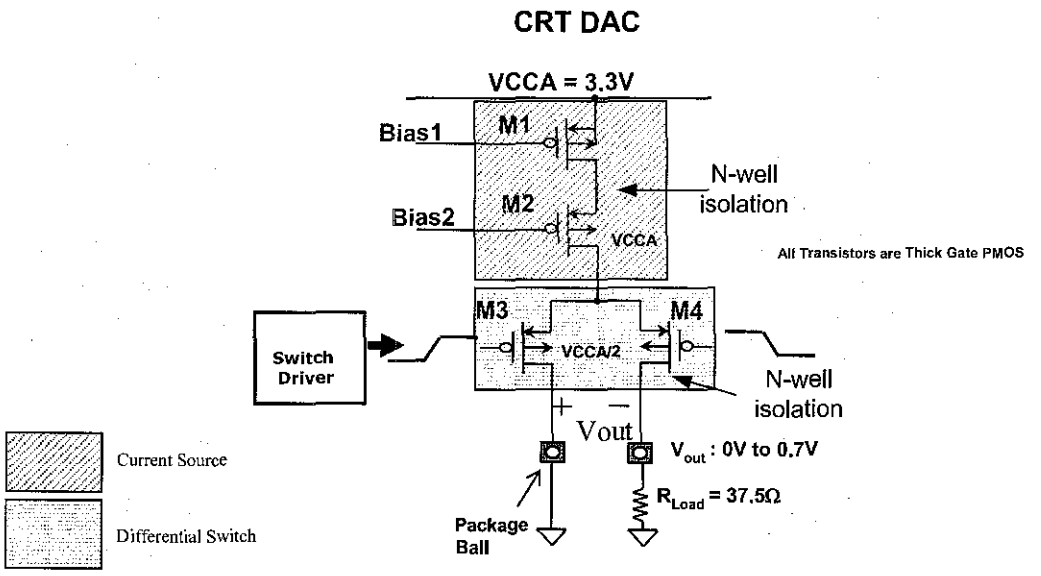

Figure 4.9: Circuit diagram of the current source/differential switch for the CRT DAC [1].

composed of parallel current switches. This so-called CRT DAC is widely used in the high speed applications specifically for its speed and linearity. The circuit is referenced to an analog power supply, which consists of an array of PMOS current sources and differential current switches.

This analog power supply of the CRT DAC operates at 3.3V nominal voltage. This voltage operates in 90nm process technology. It has been proven based on industry specification that the 90nm CRT DAC has sufficient headroom in terms of the circuit performance degradation in the used model of 7-year lifetime [1].

Since the supply voltage was chosen to be 3.3V, the DAC transistors were implemented with thick-gate oxide PMOS transistors to prevent electrical over-stress on the oxide for long term reliability and to minimize the effects of gate leakage current [70]. The PMOS transistor selection over the NMOS transistor was chosen to minimize the effect of substrate noise on the DAC LSB output. The current source and the differential switch transistors are isolated from the substrate by the n-well as indicated in Figure 4.9.

The current sources of the transistor M1 are implemented with a cascode transistor M2 to increase the output resistance which is important for the INL performance [71]. A cascode is a two-stage amplifier composed of a transconductance amplifier followed by a current buffer. Biasing transistors that are drawn with relatively large dimensions at V_{gs} and V_{ds} voltages a few hundred milli-volts above the threshold voltage typically result in lower output resistance compared to larger biasing voltages. The differential switch M3 and M4 is implemented with the thick gate oxide PMOS transistors that are driven by a custom designed master-dual-slave flip flop [1]. The lower voltage potential of the flip-flop/switch driver cell is clamped to a diode voltage drop to minimize the output voltage swing on the differential current switch transistors (M3/M4). The edge rate of the flip-flop/switch driver is designed to be fast to minimize jitter. However, the coupling of charge via parasitic capacitance with fast edge rates can result in excessive "glitches" at the output of the DAC. Output glitches or signal-feed-through from the flip-flop driver of the output of the DAC is one of the major components that degrade the dynamic performance of the DAC.

Based on the simulation result, it is observed that the $\mathbf{I}_{dsat}$ and the V_t degradations of both the matched devices M1 and M2 pairs and the differential switch M3 and M4 pairs at 3.3V nominal condition were comparable. However at 4.6V burn-in condition, the degradation of the matched devices M1 and M2 pairs was reported having higher V_t mismatch as high as 5.2mV above the DAC specification of 2mV or below as indicated in Table 4.6. As a result, the high V_t mismatch may cause the DAC operation to malfunction.

Hence, it is very critical for circuits such as DAC to have an accurate modeling of reliability induced mismatch. Even though we may think that the 2mV of V_t mismatch is insignificant, this type of special analog circuit like the current steering DAC requires a high degree of matching.

Table 4.6: AgingSim result comparing current source/differential pairs at 3.3V and 4.6V

Aging Simulation - Burn In mode @ 3.3V (V nominal)			
Transistor	Pair	idsat (%)	Vt mismatch (mV)
M1	Current Source	2.157	0.902
M2	Current Source	2.157	0.902
M3	Differential	2.047	0.731
M4	Differential	2.047	0.731

Aging Simulation - Burn In mode @ 4.6V (1.4X V nominal)			
Transistor	Pair	idsat (%)	Vt mismatch (mV)
M1	Current Source	1.905	5.239
M2	Current Source	1.905	5.239
M3	Differential	2.039	2.059
M4	Differential	2.039	2.059

4.5.4 Voltage Sensitivity Analysis

As discussed in the first case study, it is noted that the higher voltage difference between the gate and the source of a transistor will result in a higher NBTI degradation. Therefore, for the second case study on the CRT DAC, the scenario will be even worse due to the extreme level of matching required for the DAC to operate at its best.

Based on the AgingSim procedure explained in the Section 4.4.3, the percentage increase in NBTI degradation is very significant as the voltage supply increases. The scaled time dependencies of a PMOS transistor at different operating voltages are shown in Figure 4.10. The degradation in Figure 4.10 is extrapolated by scaling the gate voltages to the typical analog operating voltages.

The extrapolation is done by [6] using equation (4.14).

$$\Delta V_t = A * e^{\beta V_G} * e^{\frac{-E_a}{KT}} * t^n \tag{4.14}$$

where:

- A (Gain) = 1
- E_a = 0.145 eV

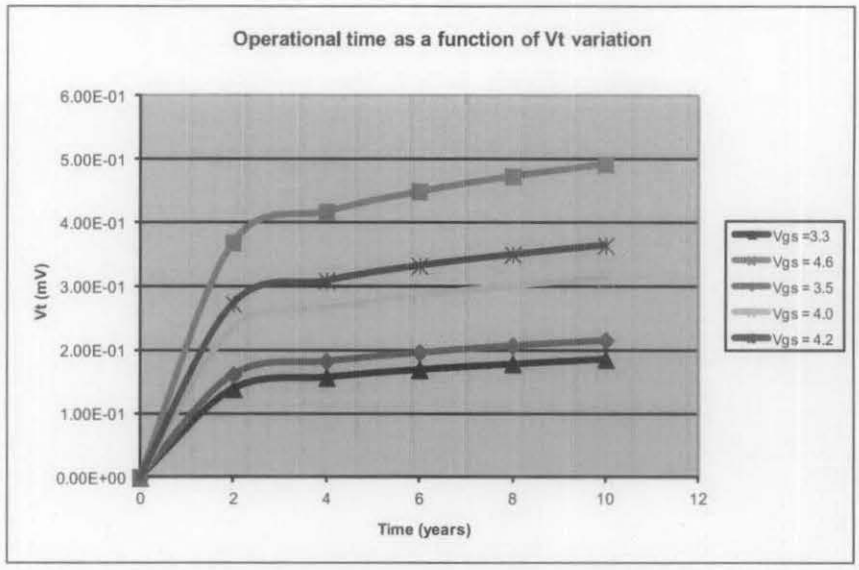

Figure 4.10: Threshold voltage variation as a function of operational time

- $\beta = 0.75$
- K (Boltzmann constant) = 8.61E-05
- T (Temperature in Celcius) = 95°C

Equation (4.14) is derived and formulated by taking into account the hole density and the hole tunneling effect to NBTI. Based on this formula, this tunneling effect is proportional to the exponential of the activation energy, E_a.

4.5.5 Temperature Sensitivity Analysis

The graph shown in Figure 4.11 is an example of the temperature profile in a burn-in oven. The left most and right most points are used to signify the two different batches of samples used for the burn-in experiment.

The temperature difference (85°C~125°C), will result in an aging difference of up to 70% between the lowest temperature to the highest.

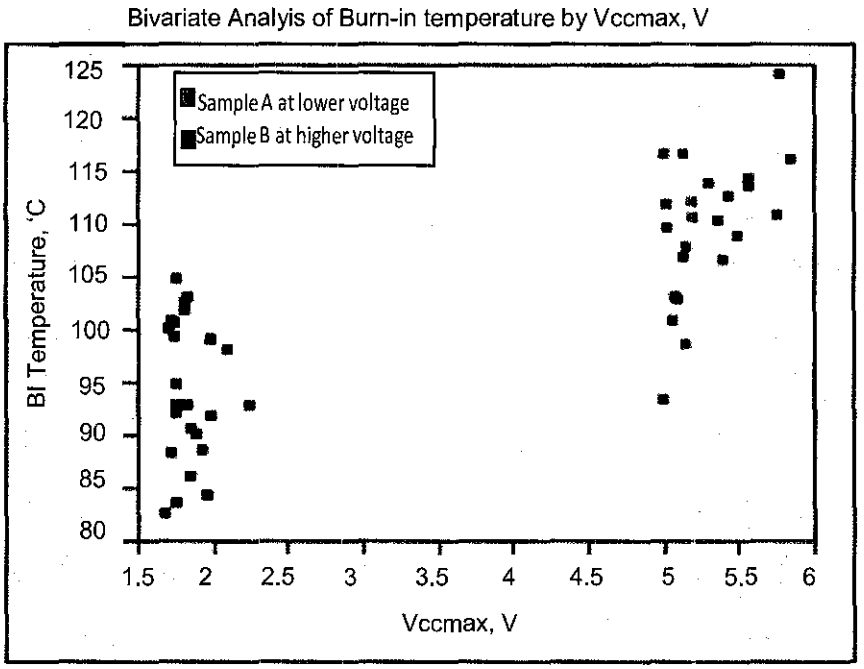

Figure 4.11: Temperature variation as a function of Vccmax

It is important to know accurately what each unit is going through, from a temperature perspective, at each burn-in session. This can be achieved through die level information from the thermal sensor whereby the temperature measurement of the unit can be taken real time.

Hence, a proper calibration is essential and for this matter it is very necessary to track the measurement via the thermal sensor, at a unit level. The use of a more accurately controlled temperature environment such as the standard burn-in oven is critically needed to minimize the temperature variation. This is because of the fact that NBTI itself is dependent on the temperature [18].

4.6 Summary

Reliability Simulator is treated as a proxy for circuit robustness. Hence, it is a very critical tool in today's circuit design which can effectively predict changes in device

and circuit performance over a product lifetime. It further allows the simulation of post-degraded circuits to ensure circuit designs meet the reliability requirements at end-of-life.

The two case studies presented in this chapter were only focusing on voltage and temperature sensitivities. Based on the simulation done on the on-die thermal sensor circuit, it is observed that higher voltage and temperature will result in higher NBTI degradation. Further analysis reported on the specific internal circuit inside the thermal sensor confirmed as a non-reliability concern because the percentage degradation is within an acceptable range.

On the other hand, the second case study on the DAC circuit appears to be very critical due to its high degree of matching requirements. The analysis shows that the degradation reported on the simulation was much above the typical 2 mV range. This is due to the stress voltage condition which was set beyond the typical 1.4X nominal voltage.

In the next chapter, the actual burn-in stress experiment on a specific DAC circuit was conducted to prove its reliability robustness.

CHAPTER 5

BURN-IN STRESS ON DIGITAL-ANALOG-CONVERTER (DAC)

Burn-in stress is one of the key elements in evaluating the reliability robustness of circuit devices. Therefore, it is very critical to develop a burn-in hardware early enough so that the experiment can be planned upfront.

In this chapter, a special burn-in experiment on the DAC circuit is described in great detail. Then, a special burn-in test modes, test patterns as well as special use conditions are explained. Last but not least, the result of the DAC burn-in experiment is discussed in section 5.6.

5.1 Introduction

In the previous chapter, the focus was primarily on the analog circuit aging simulations and their sensitivity across product designs. In order to verify the circuit reliability of the design, the aim of this chapter is to discuss the burn-in stress that was performed on the DAC interface.

Reliability and product yield have been playing key roles affecting today's semiconductor manufacturing bottom line [72]. NBTI has emerged as the dominant PMOS device failure mechanism in the nanometer VLSI era. The extent of NBTI degradation of a PMOS device increases dramatically at elevated operating temperatures and supply voltages. Unfortunately, both these conditions are concurrently experienced by

a VLSI chip during the process of burn-in testing. Therefore, burn-in testing can potentially cause significant NBTI degradation of the chip which can require designers to incorporate reliability mechanisms in their design simulations.

Burn-in stress is an integral part of today's semiconductor industry back-end test methodology and is used primarily to screen out the infant mortality regime of the traditional Bath-tub Failure Rate curve as shown in Figure 5.1. These latent defects or sometimes called as early life failures are attributable to intrinsic gross faults within the bought-in components, assembly errors and faults induced in components by inappropriate handling such as the ESD damage. Burn-in can reduce the cost of repair by weeding out potential defective parts before they get assembled into boards. Burn-in stress is also used for product reliability risk assessment which translates into Defect Per Million (DPM). This activity refers to early Infant Mortality (IM) fails according to the first regime of the Bath-tub curve as illustrated in Chapter 2, Figure 2.5.

An extended burn-in or life testing is used to predict long term reliability. These long term reliability failures are measured in Failure In Time (FIT) rate. It is a measurement of the number of failures that can be expected in one billion (10^9) device-hours of operation. Burn-in is used on rogue or excursion materials to help in risk assessment and decision making of ship or no-ship of products.

Product defects are accelerated by applying elevated temperature and voltage levels during the burn-in process, while the specified burn-in time (BIT) is optimized to achieve the outgoing quality goals without significant over stress to the product.

This work does not cover all product burn-in designs or circuit blocks but instead the focus is only on the DAC interface.

The details of how much voltage stress is required at each circuit node can vary with products requirements. The classifications of some digital or analog circuits, simply because they fall within such block boundaries in a design hierarchy, can also cloud the issue. For example the Double Data Rate (DDR) interface has both digital and analog circuits. Depending on which design block, the voltage acceleration coverage clearly

vary across designs and test methods. Therefore, it is very critical to run thorough circuit aging simulation since inadequate voltage acceleration coverage is always a possibility like the DAC circuit.

5.2 DAC Burn-In Conditions

The typical lifetime of a desktop computer or a netbook is less than 7 years [6]. Hence, the usage conditions are very much important especially for the end users to comply so that they do not exceed the limits defined by the design specifications. Due to this requirement, there are design rules developed for the product/process design which are intended to prevent both the circuit designers and the end-users from over-stressing the devices. In this context, the focus is on the DAC device.

Failure acceleration is accomplished by two factors, the voltage and the temperature. Higher junction temperature will accelerate chemical reaction, diffusion defects, and contamination decomposition while elevating operating voltage will accelerate the gate oxide defects, particle defects, and Inter-Layer Dielectric (ILD) defects [73].

The Voltage Acceleration Factor equation follows the Arrhenius equation [73] and is defined by equation (5.1).

$$V_{AF} = e^{C(V_2 - V_1)} \tag{5.1}$$

where V_2 is the stress VCC at the stress level, V_1 is a nominal VCC, and C is a constant that is technology (gate oxide) dependent.

Temperature Acceleration Factor equation as explained in [73] is defined by equation (5.2)

$$T_{AF} = e^{E_a/k*(1/T1 - 1/T2)} \tag{5.2}$$

where:

- E_a is the defect activation energy. The value is typically 0.3 to 1.0 eV, depending on the defect mechanisms.
- T1 and T2 are the use junction and the stress junction temperature, both in degree Kelvin (C+273)
- k is a Boltzmann constant = 8.617x10-5 eV/deg K

The total acceleration A between two Voltage/Temp conditions is then the multiplicative product of the two factors, as shown in equation (5.3).

$$A_{21}(i) = e^{Q_i/k*(1/T1-1/T2)+C_i(V_2-V_1)} \tag{5.3}$$

where:

- T_2, V_2, T_1, V_1 are operating temperatures (in degree Kelvin) and voltages at conditions 2 and 1, respectively.
- k = 8.61 x 10-5 eV/K is Boltzmann constant
- Q_i (eV) is the thermal activation energy for mechanism i
- C_i (volts-1) is the voltage acceleration constant for mechanism i

In actual fact, separate failure mechanisms may have different acceleration factors but in practice during the infant mortality baseline generation, composite voltage and temperature acceleration factors are calculated.

In this work, the voltage supply of interest is the analog CRT DAC power supply, VCCA. The nominal voltage for this power supply is 3.3V. Table 5.1 shows the calculated acceleration factors using the Arrhenius equation for the device used in this research.

5.3 DAC Burn-In Stress Test Mode

The standard burn-in method focuses on voltage and temperature as the primary latent defect accelerants. However, for the purpose of this experiment, the burn-in stress was

Table 5.1: Calculated acceleration factors.

Parameters	Nominal Conditions	Burn In conditions
Voltage (VCCA CRT DAC)	3.3V	4.6V
Temperature	80	100

Acceleration Factor	Burn In Conditions
Voltage Acceleration Factor, VAF	43095.76
Temperature Acceleration Factor, TAF	0.24
Total Acceleration Factor, A	10357.43

run on a special procedure. This new procedure is to implement an on-die clock with a temperature control diode to speed up the Burn-in test modes. As the frequency is increased, the internal junction temperature is elevated to meet the required stress temperature, without raising the surrounding ambient temperature.

During the Burn-In test mode, all clocks will run at 20 MHz as long as the part is running below a threshold temperature detected by the on-die thermal sensors. This 20 MHz clock is achieved by using two 10 MHz clocks, each 90 degrees phase shifted. When the thermal sensor detects that the part is too hot, all clocks will slow down to 1 MHz. But when the thermal sensor detects a catastrophic condition, all of the clocks will be stopped and the part will go into IDDQ (leakage) test mode.

The Burn-in test mode exercises all the basic components of the DAC design (decoders, band-gap voltage generator, constant current source, etc.). This test mode should provide the needed Burn-In toggle coverage on the DAC outputs by producing a full staircase ramp and the full output voltage swing of 0V to 0.7V on these buffers.

The DAC burn-in Test Mode simply muxes the outputs of an 8-bit counter into the DACs 8-bit decoders. Thus on a per clock basis the DAC are stepped through all 256 possible digital codes in sequence. This produces a staircase (saw-tooth) waveform with the DAC Test[3:0] bits in Figure 5.2. All 3 DAC channels will produce a triangle pattern ranging from code 0 to code 255. This "triangle" pattern will have an increase of 1 LSB testing both the up and down directions. With this test mode activated, the DAC's internal 8-bit up/down counter is enabled and produces a triangular input data pattern. The waveform will ramp from 00 to FF and then will ramp from FF to 00 hex, which is

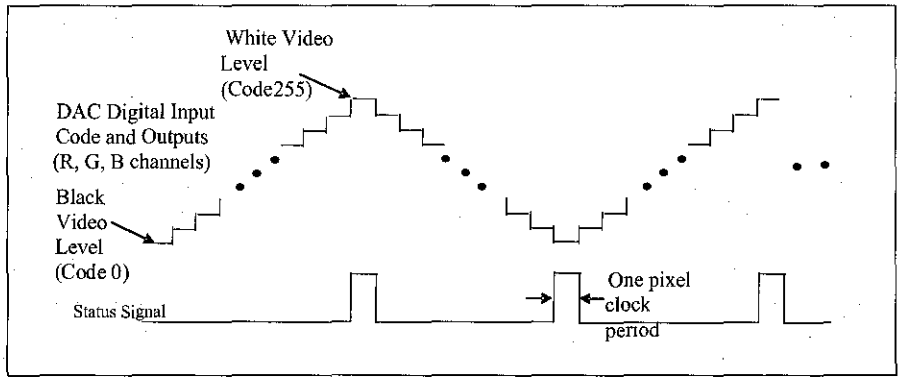

Figure 5.1: The pulse width of the status signal of the Burn-In monitor output pin.

muxed to the inputs of all three DAC channels. This operation isl repeated throughout the whole period of the burn-in operation. This operation provides full burn-in toggle coverage of the CRT DAC for burn-in testing. As the 8-bit counter reaches its terminal count value, either FF or 00 hex, a status signal from the video DAC embedded block transitions. At the completion of the count, the MSB of the counter is sent out through the Burn-In monitor output pin.

5.4 Burn-In System

Burn-in is an integral part of semiconductor companies back end test methodology and is used primarily to screen out the infant mortality section of the traditional Bathtub Failure Rate curve in Figure 5.1.

Product defects are accelerated by applying elevated temperature and voltage levels during the burn-in process. Typically, the burn-in stress is done by loading the samples into the burn-in oven utilizing the burn-in boards. During the burn-in operation, the burn-in oven supplies the elevated voltages to the samples while maintaining the oven at elevated temperature. The values of the voltage and temperature vary from product to product due to the nature of the fabrication process technology envelope. During the burn-in process, the electrical bias applied is either static or dynamic, depending on the

failure mechanism being accelerated. However, the burn-in experiment performed on the DAC interface was run on a special burn-in system.

Just like a TV or cable box at homes heats up when running, this special burn-in system relies on the heat-up process to facilitate a self initiated burn-in instead of requiring an oven. Once the oven is eliminated, traditional batch-based handling equipment can be streamlined and faster asynchronous continuous flow can be implemented.

The key advantage of this special system is that it can measure silicon stress more accurately. Working with smaller transistors at higher power and lower voltage required a new burn-in process. For this specific work, the burn-in equipment was specifically designed to burn-in test the lower power (0-75 Watt) products that do not require a specific cooling solution. For this work, the CRT DAC is already part of the device which has the ability to heat itself up to the desired burn-in test temperature. This capability is one of the Design-For-Test (DFT) features used for most of Intel products. The device is capable of regulating and holding its temperature by modulating the speed of a forced-air cooling fan and the core speed of the device. Hence, this work took the advantage of the given DFT feature to complete the CRT DAC burn-in activities.

5.5 DAC Burn-In Experiment

Burn-in usually employs exposing the device to extremes of temperature and voltage for a specified period of time and monitoring the health of the part at Post Burn-In Check (PBIC). The PBIC test should include a test that checks the DAC burn-in test mode and a set of tests that check the DACs functionality. Due to the ATE tester limitations, it would be difficult to create a test that has enough resolution that could detect minor variations in the DAC performance induced by the burn-in.

This burn-in experiment is not meant to screen out the infant mortality behavior. Instead, the main purposes of this experiment are the following:

- To ensure no product specific issues which could show a high risk parametric shift (Example : Pin signal is out of specification or new circuitry with critical timings is not being checked on or prior to the productions)
- To ensure the product design follow all design rules for that particular fabrication process.
- To provide a measure of device reliability and Negative Bias Temperature Instability degradation (NBTI) concern.
- To ensure the outgoing quality is within the specification limit throughout the product life cycle.

For a specific DAC burn-in experiment, 300 units from 3 fabrication lots were run through the experimental flow whereby the wafers were then sent into assembly die inventory (ADI) where it waited for the final assembly and testing. The overall Burn-In experimental flow is illustrated in Figure 5.3.

The Raw Class 1 (RC1) is a high temperature test. The main objective of doing raw class testing is to screen out assembly related defects. Next, these units were subjected to burn-in stress for 30 minutes and completed by Post Burn-In Check (PBIC). Similar process took place until all units completed the cumulative 168-hour burn-in. The main purpose of this work is not looking at these 300 experimental units but rather to sample out 25 good units for a specific DAC burn-in characterization. Out of all 25 units, 1 unit from each fabrication lot was marked separately to be treated as the control unit. The idea was that these control units are to be tested first and the data to be taken in a separate log file for comparison purposes, while the rest of the units will be tested after each of the burn-in readouts at a hot temperature of 115°C.

With regards to the test contents of the ATE testers, a series of electrical measurements (timing and parametric shift) are taken at different stages. A total of 25 good units from 3 qualification lots will incur burn-in stress for 12 cumulative hours with readouts taken at time zero, 30 minutes, and 12 cumulative hours. The readouts will

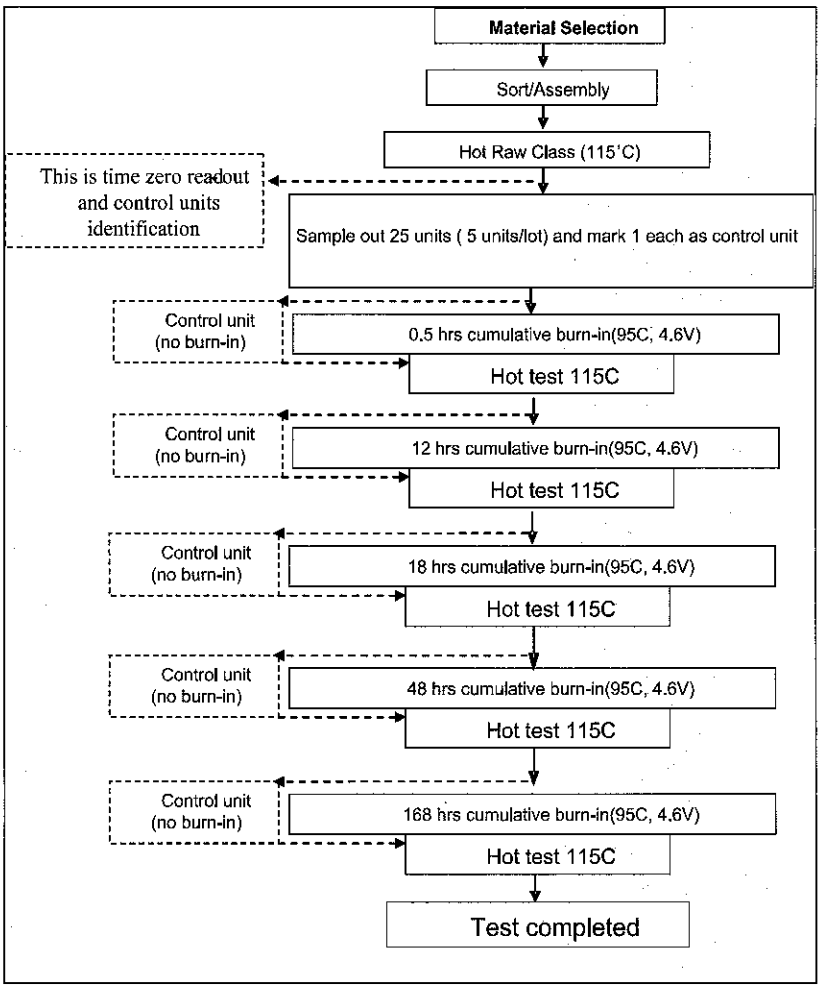

Figure 5.2: DAC Burn-In Experimental Flow.

consist of AC and DC testing with pins and parameters chosen to provide test coverage to all buffers and pin types.

The aim of the test results is to collect data based on the following parameters:

- Differential Non-Linearity (DNL)
- Integral Non-Linearity (INL)
- Gain Error
- Offset Error
- Output Current

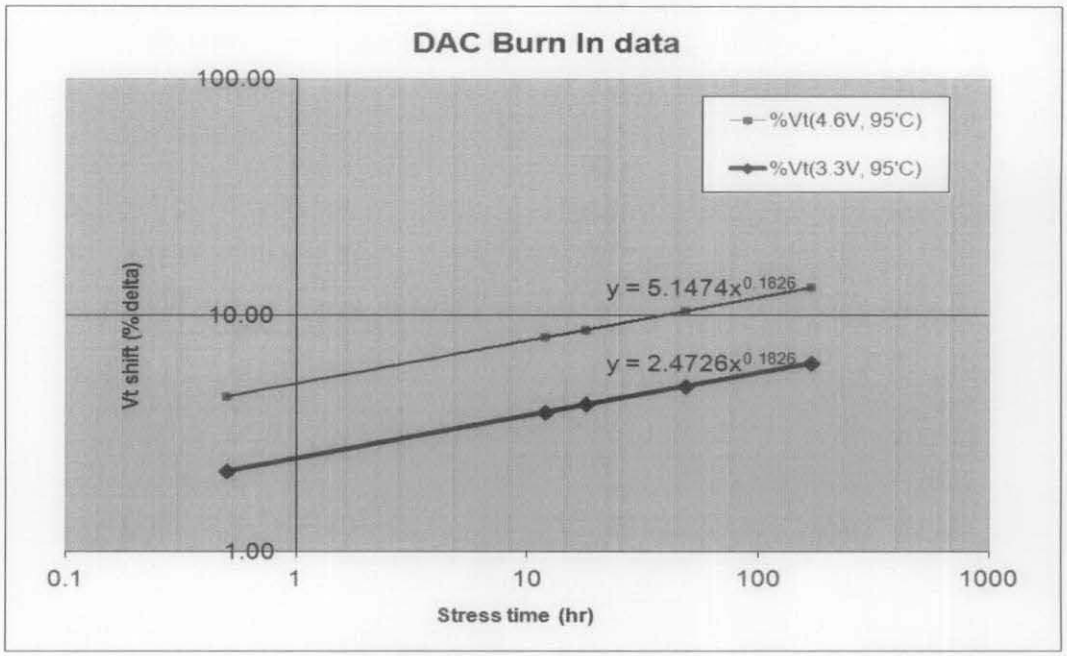

Figure 5.3: DAC burn-in comparison, 3.3V vs 4.6V

5.6 DAC Burn-In Result

Figure 5.4 summarizes the DAC burn-in result. The work was conducted on two legged burn-in experiment. The first leg was run under nominal voltage of 3.3V while the second leg was done under elevated burn-in voltage of 4.6V. Based on the graph plotted, it clearly shows that the higher voltage difference between gate and source will result in a higher degradation.

As explained in the theory in Section 2.2.1.1, this is a result of the higher oxide electric field causing a larger number of interface traps. Oxide electric field enhances NBTI. NBTI is very sensitive to electric field as shown in the Figure 5.5, in terms of the applied gate voltage for two different oxide thicknesses [5]. According to Ogawa et al. the interface trap and fixed charge generation show an $E_{ox}{}^{1.5}$ dependence [74]. NBTI performance is judged by the extrapolating time-to-failure (TTF) to a typical percentage of parameter shift.

TTF is a function of the following:

- Vstress (↑ means ↓ TTF)

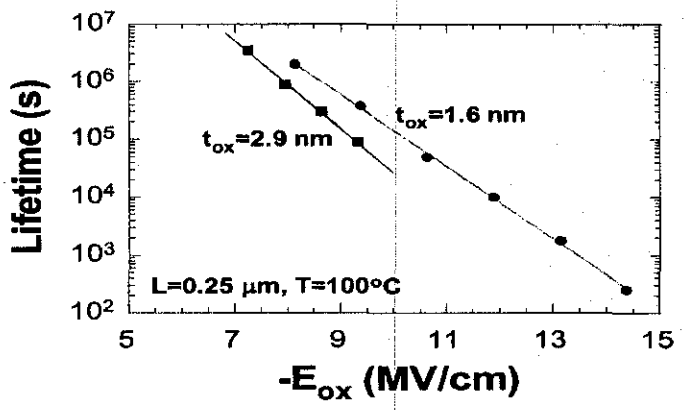

Figure 5.4: Lifetime as a function of gate voltage. Data after Schroder et al.[5].

Table 5.2: Summary of 168 hours (7 years) Burn-In experiment of DAC

Items	Pre Burn-In	Post Burn-In	Percent Change
DNL mean	0.185 LSB	0.197 LSB	6.48%
INL mean	0.235 LSB	0.246 LSB	4.68%
Gain Error	3.585V	2.500V	43.50%
Offset Error	0.000344V	0.000361V	4.90%
Output Current	59 mA	60.2 mA	2%

- Vcc - Vt (↑ means ↓ TTF)

DAC or even ADC are the key components of data-acquisition systems. They act as communication blocks for both analog and digital blocks [11]. In principle, when the digital input is given to a DAC, it will provide an accurate output voltage. In practice, the accuracy of the output voltage is subject to the offset and the gain errors from the DAC building block and other devices in the signal chain. Hence, in order to verify the robustness of the DAC performance after burn-in stress, the key DAC parameters, which are critical to extreme matching are measured. These measurements were taken after the last burn-in readout of 168-hours under a severe stress condition of 4.6V. The key test results measured before and after the burn-in stress are summarized in Table 5.2.

Based on the test results measured, the gain error measurement after the post burn-in stress was the only parameter that has a significant spike as compared to the rest of

Table 5.3: The Vout data taken before and after Burn-In stress

Input code	Vout @ pre Burn-In	Vout @ post Burn-In
0	0.000	0.000
1	0.167	0.239
2	0.333	0.478
3	0.500	0.717
4	0.667	0.956
5	0.833	1.195
6	1.000	1.434
7	1.167	1.673
8	1.333	1.912
9	1.500	2.151
10	1.667	2.390
11	1.833	2.629
12	2.000	2.868
13	2.167	3.107
14	2.333	3.346
15	2.500	3.585

the key parameters. A significant increase in the gain error of 43.5% was observed. The ideal situation is that the DAC's gain error has to be zero. The gain measurement was collected on the ATE tester. The pre burn-in is assumed to be an ideal case with zero gain error. Table 5.3 shows that as the DAC input code increases, the output voltage increases accordingly to 2.5V (V_{ref}).

The post burn-in Vout was measured at the ATE tester and the Vout values increased by ~43.5% compared to the typical gain error percentage of less than ~20%. The gain was calculated as A_V= 3.585/2.5 = ≈1.43406667. Hence, the gain error percentage is ≈43.5%. Figure 5.6 shows the DAC transfer functions of ideal (pre burn-in) vs actual DAC (post burn-in).

In this specific case, the gain error has created a span greater than the desired ideal case. The transfer function is modeled as a typical straight line as commonly described by $y = mx + c$ equation, where:

- y is the output of the DAC
- m is the slope of the transfer function
- x is the input of the DAC

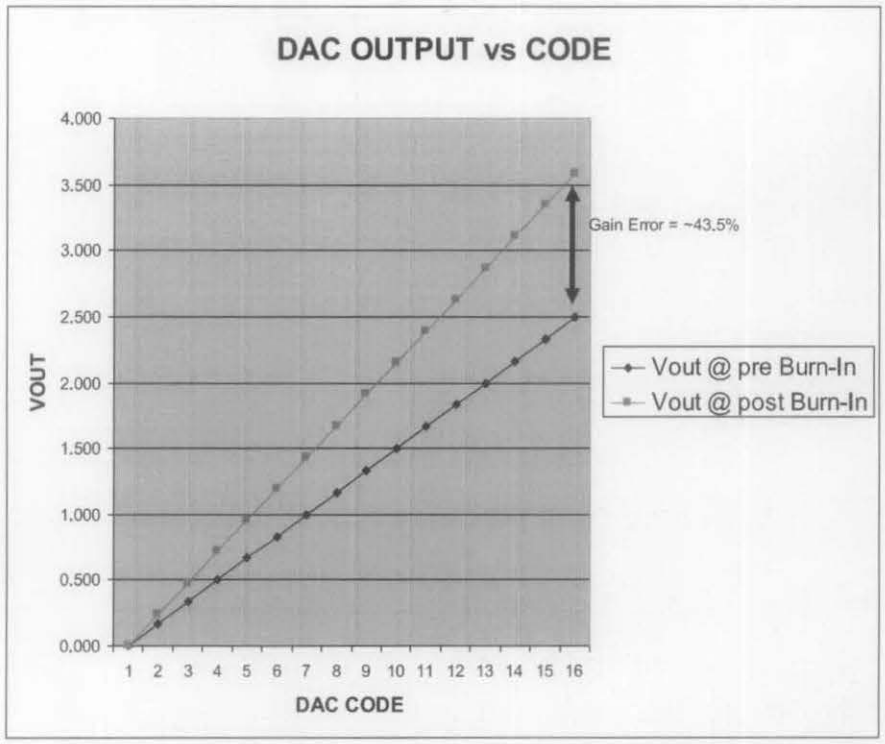

Figure 5.5: DAC characteristic showing an excessive gain error of 43.5%

- c is the offset voltage

Typically, an ideal DAC has a gain, m, of 1 and an offset, c, of 0 and hence the output tracks the input in a precise linear manner. However, for the real DAC, it has non-ideal gain and offset values which normally can be compensated once the values are determined.

For the data taken in this burn-in experiment, the design is based on an 8-bit DAC with a 0V to 2.5V nominal output span. When the digital input is set to a full scale, a 3.585V output is measured.

From this data, the actual gain error, measured in percentage, can be determined by multiplying the output voltage at post burn-in by the output voltage at pre burn-in, 3.585V/2.5V = $\approx$1.43406667. The gain error is calculated with the assumption that the offset error is zero while the span error is measured at 850 mV, giving an actual span of 3.585V.

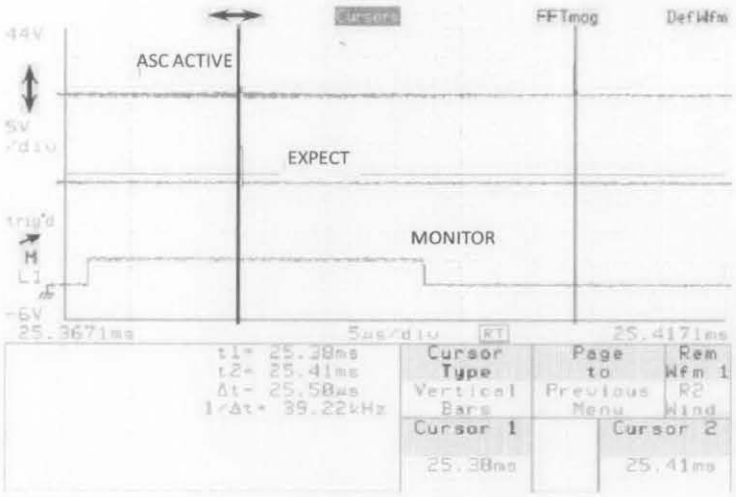

Figure 5.6: DAC Output signal during burn-in.

5.7 Correlation of Simulation and Experimental Work

To validate the actual performance of the CRT DAC design, a customized burn-in hardware was developed to specifically stress the CRT DAC components only. Burn-in is usually run at a low frequency, 20 MHz. The burn in test mode exercises all the basic components of the DAC design such as the decoders, band-gap voltage generator, constant current sources etc. This test mode should provide the needed toggle coverage on the DAC outputs by producing a full staircase ramp and the full output voltage swing of 0V to 0.7V on these buffers.

Data shown here was taken on the burn-in board (BIB) at VCC = 4.6V (burn-in voltage for DAC) with device case temperature of 95°C and driver data rate of 20 MHz. The DAC BIST output can be seen on the monitor output signal (MONITOR) of each device. Figure 7 shows a small section of the DAC output seen on MONITOR. Auto Signal Check (ASC) is active twice during this section and is looking for one high and one low. Since the MONITOR and the EXPECT (simulation data) match while ASC is active, Auto Signal Check will pass. MONITOR can be found on the rear edge connector of the BIB. ASC active and expect can be found on test turrets towards the rear of the BIB.

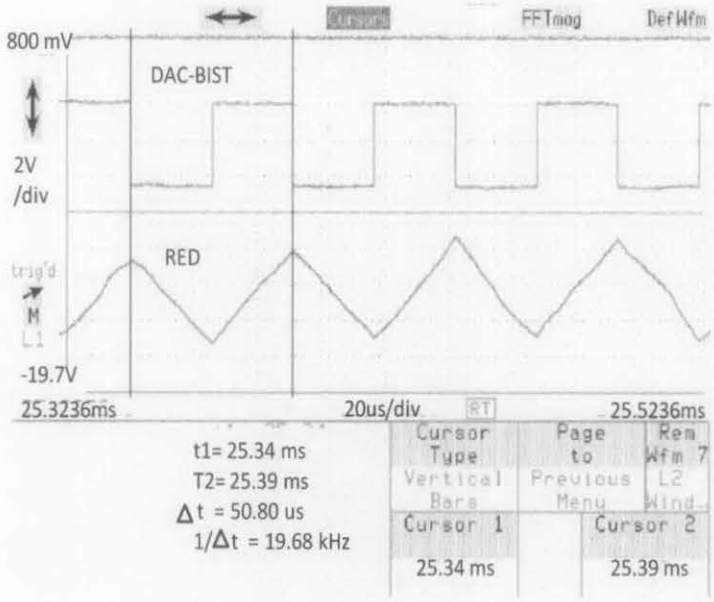

Figure 5.7: RGB Output signal during burn-in.

Figure 8 shows a screen capture of the monitor output during DAC BIST, and the output of one of the RGB pins. The RGB outputs can be found on the 3 socket resistors comprised of Red (pictured below), Green, and Blue.

5.8 Summary

In a nutshell, burn-in stress is one of the key elements to verify circuit reliability specifically the analog devices/circuits.

A special burn-in condition which includes its test modes, test patterns, and use conditions were set-up. The data after the burn-in stress was collected and compared with the pre-stress data.

Due to the sensitivity of the DAC functionality, some key DAC parameters were monitored and compared between pre and post stress. It is observed that a gain error is the only parameter which is susceptible to elevated use conditions.

The last chapter comprises two sections. Section 6.1 gives the conclusion of this work and Section 6.2 proposes ideas for future work.

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

Developing an efficient reliability simulator covering Process, Voltage and Temperature variations (PVT) is deemed compulsory in order to deliver highly reliable products in the SOC business where less customer complaints related to reliability are expected. To take the leading role in technology and market without sacrificing reliability, circuit designers must be equipped with accurate reliability modeling and simulation tools to help control the reliability from the very beginning design stage to the final qualification.

The main objective of this work is to study the NBTI failure mechanism and its sensitivity in the two critical analog devices, comparing the aging simulation result to the actual burn-in experiment.

This last chapter comprises two sections. Section 6.1 provides the conclusion of this work and Section 6.2 gives an overview of the future work related to this paper.

6.1 Conclusion

As discussed in Section 2.2.1, the NBTI failing mechanism in specific analog circuit blocks particularly the DAC can cause errors. For this work, specific SOC analog circuits have been thoroughly investigated, verified and found some important issues in relation to the NBTI issues.

The work can be separated into 2 main sections.

6.1.1 Voltage and temperature variation in NBTI Model for Circuit Design

Previous work on the NBTI effect to the analog circuits has given some general ideas on the impact to the circuit performance at different operating conditions. Running reliability simulation across PVT is mandatory to ensure all process corners and conditions are fully validated and verified.

This work has been successfully conducted by comparing the simulation result to the actual silicon performance. However, the interest of the work is to look only at voltage and temperature sensitivities. Simulation results on both case studies depend on the nature of the NBTI event.

For example, the on-die thermal sensor simulation results revealed that the NBTI degradation observed based on the simulation analysis has proven to be non-significant to cause an error to the thermal sensor functionality. This initial finding of this work titled ***"A case study for reliability-aware in SOC analog circuit design"*** was presented as an oral presentation in IEEE International Conference on Intelligent and Advanced Systems (ICIAS) conducted in Kuala Lumpur in June 2010.

The second case study on the DAC shows a different result. This is due to the higher degree of matching accuracy required for the DAC to perform at its design specification. The NBTI degradation observed in the simulation analysis revealed that under a severe stress condition like 40% increase in the nominal voltage supply, a significant voltage threshold mismatch of beyond the 2mV limit was recorded. This work with the title ***"NBTI-induced 8-Bit DAC circuit mismatch in System-On-Chip (SOC)"*** was presented as an oral presentation in IEEE 3rd Asia Symposium on Quality Electronic Design (AsQED) held in Kuala Lumpur in July 2011.

6.1.2 A special Burn In experiment looking into NBTI reliability sensitivity

A burn-in experiment was performed to verify the reliability sensitivity of the DAC design. Burn-in stress plays an important role in verifying the robustness of circuit

design. A defect after burn-in stress can cause performance degradation and can slow down the circuit operation.

Through this special burn-in experiment on the DAC circuit, it is proven that elevating both voltage and temperature at the extreme conditions can cause critical DAC parameters to be malfunctioned. In this case, the voltage was elevated to 1.4X nominal supply voltage while the temperature was set at 90-100°C. The gain error was determined to be at the upper extreme reading, 43.5% to be exact.

In summary, the reliability simulation demonstrated a shift of the threshold voltage, V_t on the CRT DAC specifically at the current source array component, implying the existence of NBTI mechanism. Correlations between reliability simulations and the burn-in systems were attempted, which are critical in characterizing the key components of the DAC design specifically the current source array circuit. This attempt provides high confidence in the reliability model and the simulation developed. As a result, the actual burn-in stress conducted on the CRT DAC shows variations in the biasing currents due to NBTI, which resulted in a gain error. This paper sheds some light for the next generation SOC products to perform an accurate reliability simulation modeling and to correlate with burn-in systems in order to minimize reliability induced mismatch.

NBTI is one of the most important sources of failures affecting transistors. The question that may arise is that what needs to be done once NBTI effects are known. Some possible methods are introduced to reduce the effect of NBTI.

1. Simulation - This method, as discussed in this thesis, mitigates NBTI by running circuit level simulation using AgingSim to verify the NBTI impact. By running AgingSim, the outlier of the NBTI paths can be fixed real time.

2. Test Guardband - This method mitigates NBTI by introducing a fixed percentage of the maximum frequency (Fmax) buffer between the test and the usage frequency (i.e. test at 3.4 GHz, higher than the specification frequency of 3.2Ghz). In addition to this method, some investments need to be put on the table. As the mean and the sigma of NBTI percentage increases, more Fmax buffer is needed.

3. Aging heuristics - This method mitigates NBTI by applying delay penalty to compensate for circuits with higher NBTI percentage. By using heuristics, time can be reduced when solving problems. At the same time, this method ensures good design practice.

4. Dynamic VCC and Bus-ratio adjustment - This method is still under feasibility study. The method adjusts the dynamic VCC and the bus-ratio during the usage conditions based on the Intra-Die Variation Probe (IDVP) degradation as an indicator.

6.2 Future Work

Since this paper has focused on the voltage and the temperature effect to the NBTI event, the future work will be focusing on the effect of process variation. Some initial works have started and the work title ***"IDVP (Intra-Die Variation Probe) for System-on-Chip (SOC) Infant Mortality Screen"*** has been presented as an oral presentation in the IEEE International Symposium on Circuits and Systems (ISCAS) which was held in Rio de Janeiro, Brazil in May 2011. Another work, which is also related to the process variation effect, titled ***"A Case Study of Process Variation Effect to SOC Analog Circuits"*** has been published in the IEEE Recent Advances in Intelligent Computational Systems (RAICS) which was held in Trivandrum, India in September 2011.

Recent sub-micron process technology scaling leads the urgency to build an efficient methodology of characterizing and modeling the process variation effect, for example, the threshold voltage, V_t. This is one of the key process parameters that must be extensively modeled and validated for accurate circuit performance. Furthermore, this requirement is even more critical for analog applications which demand an ability to match devices precisely.

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LIST OF PUBLICATION

The research work in this thesis was presented and published in official proceedings of rigorously referred conferences through the following research papers:

1. Abdul Latif, M.A., Zain Ali, N.B., Hussin, F.A. "**A Case Study for Reliability-Aware in SOC Analog Circuit Design,**" In IEEE International Conference on Intelligent and Advanced Systems (ICIAS), Kuala Lumpur, June 2010.

2. Abdul Latif, M.A., Zain Ali, N.B., Hussin, F.A. "**IDVP (Intra-Die Variation Probe) for System-on-Chip (SOC) Infant Mortality Screen**," In IEEE International Symposium on Circuits and Systems (ISCAS), Rio De Janeiro, Brazil, May 2011.

3. Abdul Latif, M.A., Zain Ali, N.B., Hussin, F.A. "**NBTI-induced 8-Bit DAC Circuit Mismatch in System-On-Chip (SOC),**" In IEEE Asia Symposium on Quality Electronic Design (ASQED), Kuala Lumpur, July 2011.

4. Abdul Latif, M.A., Zain Ali, N.B., Hussin, F.A. "**A Case Study of Process Variation Effect to SOC Analog Circuits,**" In IEEE Recent Advances in Intelligent Computational Systems (RAICS), Trivandrum, India, September 2011.

APPENDIX A

DAC BURN-IN PLAN

The burn-in board matrix is customized specifically to stress the DAC circuit. The original intent of building the burn-in board was to use for a specific product sample but for this special experiment, the emphasis is on stressing the DAC circuit. Trace impedance of all channels is controlled to allow operation of the signals operating at 10 MHz, low frequency. The output monitor signal (DAC out) is to be brought out to the burn-in board edge connector for the BI socket through a 100 ohm series resistor. The purpose is to facilitate the debug of DAC burn-in.

This special DAC BI is structurally exercised with DAC power supply at elevated voltage of 4.6V (VCC DAC). Other power supplies which are not to the interest of this experiment are core power supplies at 1.6V (VCC Core) and I/O power supplies at 2.5V (VCC I/O) The reference voltages are set to 1/2 VTT, 1/2 VDD, or 2/3 VCC depending on the interfaces. A dedicated burn-in system supply is used for the 4.6V source. A resistor divider is used to acquire proper reference source. The BI frequency under BI mode is 10 MHz. Each of the product samples is laid to support single voltage supply requirement.

A series of inexpensive discrete components is mounted on a burn-in board (BIB) to stimulate, and monitor a new on-die burn-in stress mode for DAC. This is to make each burn-in board a self-contained independent stress module. To accomplish this; the Design-For-Test (DFT) mode is entered using a strapped pull-up resistor to a power plane in conjunction with toggling the input signals. The on-burn-in board circuits will include two signals, which will be tapped off of a crystal using an RC time constant to supply input stimulus to a discrete 16-bit shift register, this will provide 900 phase shifted clocks to the device. These clocks will vary the sample product's operational frequency and junction temperature. Monitoring will use blinking Light Emitting Diodes (LED), which will give a visual reference that the DAC burn-in mode is operating properly.

BI testing is enabled when the video DAC is programmed for the triangle pattern mode with a special DAC input pin. The way the pin works is tracked by its bit from 0 to bit 2.

With this test mode activated, the video DAC internal 8-bit up/down counter is enabled and produces a triangular input data pattern (ramp 00 to FF and than ramp FF to 00 hex and repeat) that is muxed to the inputs of all three DAC channels.

This provides full-toggle coverage of the video DAC for burn-in testing. As the 8-bit counter reaches its terminal count value, either FF or 00 hex, a status signal from the video DAC embedded block transitions.

A special indicator signal will be the key to indicate the status bit intended for end of burn-in testing.

There are two flavors for executing this DAC test mode, the burn-in mode which also requires the PLL to be turned off and placed in the 1X bypass mode, and the mode which is the default DAC burn-in test mode that depends on the PLLs.

DAC burn-in is activated by setting test selects and strobing test enable when hardware test mode has been activated.

Once activated the following test mode conditions are applied:

- All clocks are ungated. (open)
- All scan-out buffers and the burn-in monitor output buffer are enabled.
- The Linear Feedback Shift Register (LFSR) monitor buffer is enabled. LFSR is a shift register whose input bit is a linear function of its previous state.
- The remaining buffers are tristated.
- The pull-ups and pull-downs are turned off.
- All clamps are turned off.

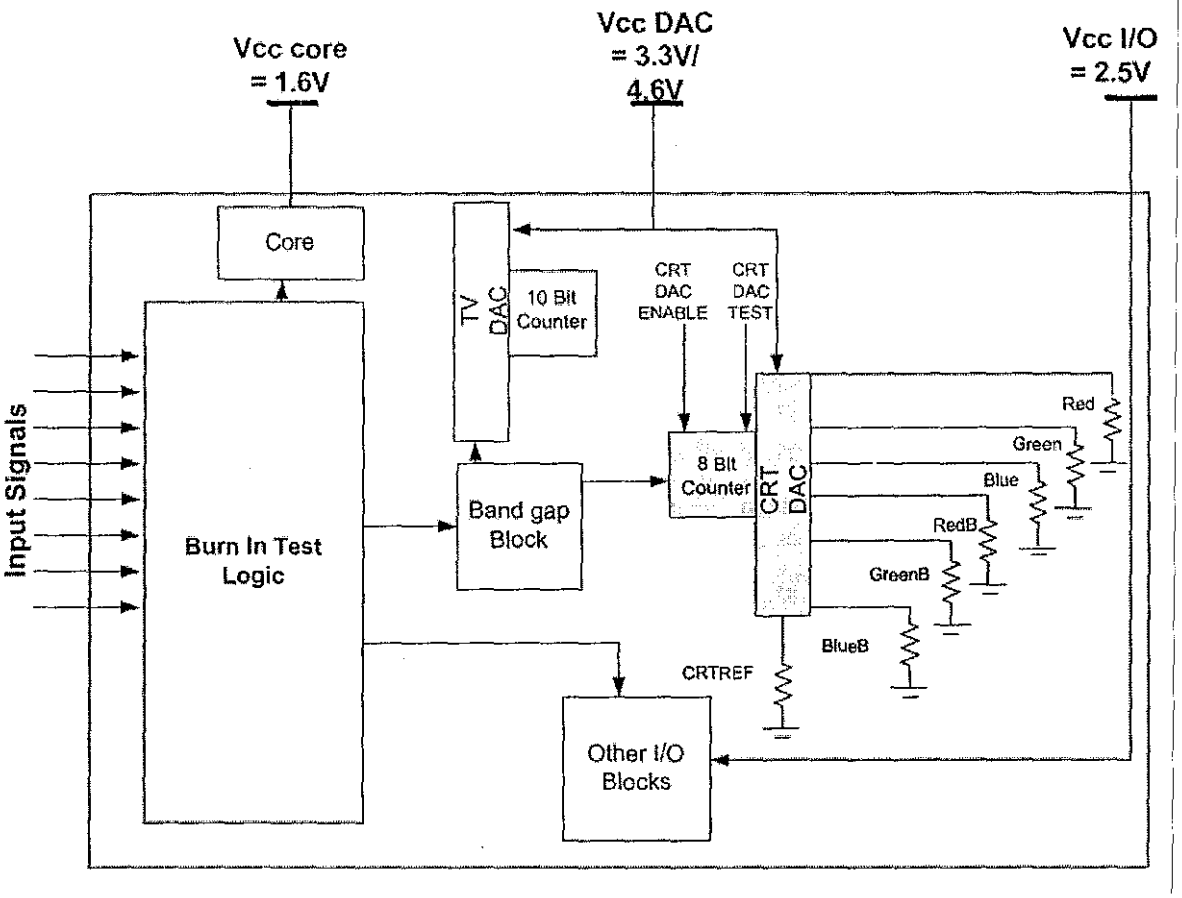

Figure A.1: Burn In Architecture

The tri-state buses are grounded. This mode is not cumulative. Figure A.1 shows a high level DAC specific BI block diagram.