DESIGN OF
LOW POWER
MOBILE TRANSMITTER

By

LEE WAI MUN

DISSERTATION

Submitted to the Electrical & Electronics Engineering Programme
in Partial Fulfillment of the Requirements
for the Degree
Bachelor of Engineering (Hons)
(Electrical & Electronics Engineering)

Universiti Teknologi Petronas
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CERTIFICATION OF APPROVAL

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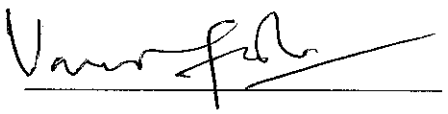
Approved:



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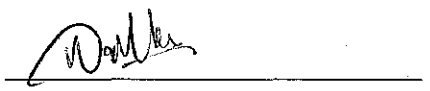
June 2005

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.



Lee Wai Mun

ABSTRACT

The objective of this project is to design a power amplifier for a new two way mobile radio product being launched by Motorola. Two-way mobile radio consists of a transmitter, receiver and a voltage-controlled oscillator. Mobile radios usually have transmitter whose power output ranges from 1 W to 50 W. Design of transmitter line-up for mobile radio involves the design of appropriate matching network for driver and power amplifier. The power and voltage control of these devices are equally important. Designing a mobile radio transmitter is regarded tricky due to difficulty in getting a robust transmitter that is stable with minimum oscillation.

In this work, the design is attempted using Advanced Design Simulator (ADS). The design simulation provides accurate simulation on harmonic filter and antenna switch. 50 ohm matching networks have also been designed and simulated using ADS and it gives close approximation to the specifications. The radio has since been prototyped and tested. The evaluation and testing of the radio has been carried out and it satisfies the specifications that are set by the Telecommunication Industry Association (TIA). Some minor optimization has also been performed to improve the radio performance. Eventual product is a transmitter line up that function well today.

ACKNOWLEDGEMENTS

I would like to take the opportunity here to express my deepest gratitude to the following personnel for the successful completion of this final year project in one year time.

- Dr. Varun Jeoti, Associate Professor of Electrical & Electronic Engineering Department, UTP
- Mr. G.S.Kok, Senior Engineering Manager, Motorola Penang
- Mr. Jalmi Jalil, Engineering Section Manager
- Engineers from ELM team of Motorola Penang
- All lecturers, staff and technicians of UTP

Thank you!

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LIST OF ABBREVIATIONS

A	-	Ampere
ADS	-	Advance Design Simulator
AS	-	Antenna Switch
GHz	-	Giga Hertz
ELM	-	Entry Level Mobile
FGU	-	Function Generating Unit
FYP	-	Final Year Project
HF	-	Harmonic Filter
I/O	-	Input/Output
LO	-	Local Oscillator
MHz	-	Mega Hertz
Mic	-	Microphone
NWA	-	Network Analyzer
PA	-	Power Amplifier
PTT	-	Push to Talk
RF	-	Radio Frequency
Rx	-	Receiver
S-parameter	-	Scattering Parameter
TIA	-	Telecommunication Industry Association
Tx	-	Transmitter
UHF	-	Ultra High Frequency
VCO	-	Voltage Controlled Oscillator
VHF	-	Very High Frequency
VSWR	-	Voltage Standing Wave Ratio
W	-	Watt

CHAPTER 1
INTRODUCTION

1.1 Background

Mobile radio is the wireless two-way radio being used widely in public transport and commercial sector. It is mostly installed in vehicles. It utilizes the supply from the car battery. Mobile two-way radio is a half-duplex radio where it allows transmission in one direction at one time. The radio circuitry consists of four major sections. They are transmitter, receiver, function generating unit and antenna switch. The transmitter of the mobile radio is usually designed to cater high level of power transmission due to the need for long distance of transmission. The power level of mobile radio ranges from 25W to 40W. The main function of the transmitter is to amplify the input audio signal and radiate the signal to space through the antenna. During amplification through stages, the noise and small signal will be amplified as well. Meanwhile, the harmonics generated by the power amplifier needs to be taken care of. Harmonics could produce spurious problem during transmission. Improper matching network in transmitter stage could create the so-called oscillation that may cause instability to the system.

Two-way radio consists of four main portions, namely, transmitter, antenna switch, receiver and function generating unit (FGU). The latter two portions have been completed by the engineers in Motorola, Penang. The transmitter design in this project covers the transmitter and antenna switch/harmonic filter. This is a project in collaboration with Motorola, Penang. Meanwhile, it has helped to develop a two-way radio in this new range of frequency

This final year project (FYP) is a two semester project where the first semester was focused on the simulation of the line up, power and voltage control simulation using Advanced Design Simulator software. The work of second semester mainly revolved around on board measurement, prototyping of the two way radio and testing and evaluations of the prototyped radios. Optimization and some troubleshooting skills were acquired in this project as well.

1.2 Problem Statement

Very High Frequency (VHF) 216 MHz ~ 247MHz is a relatively new band of frequency being studied in Entry Level Mobile (ELM) team, Motorola Penang. The future mobile radio based on this frequency band needs to be designed in order to accommodate the demand of users. Since it is a relatively new band, the design of the circuitry the radio needs to be studied in order to benchmark the radio architecture. The current VHF band and UHF band radio can be used as reference in the design. The transmitter line up is one of the major radio circuitry. Throughout the design, a number of design parameters specifications need to be met in order to achieve the design objective. Transmitter design was conventionally designed by using hands on practical on the current radio board. Upon done with feasibility study, they will decide on the radio topology to be used. Then they will perform tweaking on the transmitter line up in order to achieve the goals of power and current. However, this method may not yield the desired result as luck and experience plays the important role here. Due to inconsistency in this method, simulation using ADS software was much desirable. En route to design the transmitter for this band, ADS simulation was extensively used. Successful ADS simulation on transmitter line up may be helpful in the design of radio of other bands.

In practice, the simulation result has discrepancy with the actual on board measurement. ADS software is considered as one of world most powerful RF design software. However, the simulation result still carries certain extent of difference compared with actual on board result. Due to this reason, we faced a problem after the radio has been prototyped. The response of the radio is not as encouraging as expected from ADS. This prompted to a optimization to fine tune the radio.

On top of that, in real life, the component has tolerance to certain limit. Since the line up consists of a number of RLC, the tolerance of each component contributed to the overall discrepancy that we can see from the ADS simulation and on board result. This is one of the challenges we faced in the design as ADS result can only serve as starting approximation.

The performance of the radio is a subjective issue as different people define the output quality differently from one person from the other. With the TIA specifications, the performance of the radio can be evaluated in an objective manner. This leads to a series of testing and evaluation. The result has been compared with the specifications and analyzed. Learning and practicing these testing methods and understand the significance of each is another challenge in this project.
ADS provide powerful simulation in impedance matching. However, the theory behind impedance matching is not well understood. Thus, this prompted to a detailed study on impedance matching. This study is practically helpful in understanding what matching is and how it is done.

Meanwhile, the absence of the Power Amplifier (PA) model in the simulation software prompted an interest in the modeling of the device in order to achieve a better simulation result by using ADS. Modeling of a power amplifier requires a great deal of effort on understanding the device parameters and its characteristic. Meanwhile, the current model that exists in ADS is reviewed as well in order to know the kind of model they use in ADS.

1.3 Objectives and Scope of Study

The objectives of the project are as followed.

- To design a transmitter chain
  - ✓ that provides a 25W power with a 13.8V with a **current goal of < 6.5A** and meet the 0.25uW of radiated and conducted spur emission up to 1GHz and 2.5uW level up to 4GHz.
  - ✓ That operates through +80 deg C to -40 deg C at operating supplies of 10.88V to 16.32V with a power leveling specification of -3dB +2dB.
  - ✓ That is unconditionally stable to a load mismatch of Voltage Standing Wave Ratio (VSWR) of 4:1 over voltage and temperature extremes
  - ✓ That does not exceed the die temperature limit and the whole system not allowed to exceed the safety temperature limits when test through a 7+1 hour EIA Key down test
- To prototype the 220MHz range two-way radio
- To evaluate and test the performance on the transmitter of the radio
- To optimization and improve the performance of transmitter

The main scope of this project is on the mobile RF two way radio transmitter lines up design and configuration. The scopes may involve several perspectives below.

- ➢ RF analogue communication design
- ➢ Utilization of Advanced Design System software in RF design
- ➢ Simulation and hand on practical on transmitter line up design
- ➢ RF testing and evaluation
- ➢ LDMOSFET modeling study
- ➢ Linearization study

CHAPTER 2
LITERATURE REVIEW

2.1 Two Way Radio System and Operation

The radio being designed for this project is a two way mobile type of radio where the transmit power can go up to 25W. This radio is mainly built to cater the need from commercial consumers like the transport industry, manufacturing and construction sectors. With the high power capability, it could transmit and receive a signal at the distance of radius up to 5kms.

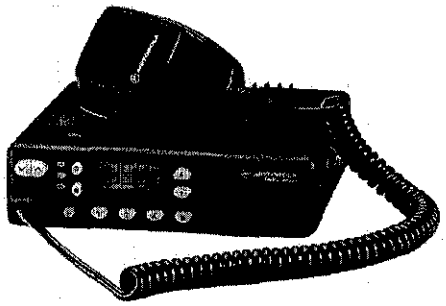


Figure 1 Two Way Mobile Radio

Two-way radio communication can be divided into analog and digital radio. The choice of the radio is largely dependent on the use of the consumers, the facilities that are available and the cost. The project here is design of a mobile radio which is from the family of analog radio. The use of digital signal processor is the key to differentiate the radio family, analog or digital. In this two-way mobile radio, it uses mainly the analog signal processor to process the signal. The digital signal processor is not used. The major components in the circuitry are RLC (resistor, inductor and capacitor).

2.1.1 Two way radio System

The two way radio uses frequency modulation scheme to carry the signal and radiate to a certain distance away. The carrier generated by the function generating unit was frequency modulated with the signal received from the users. The signal propagation is of type line of sight transmission like the figure shown below.

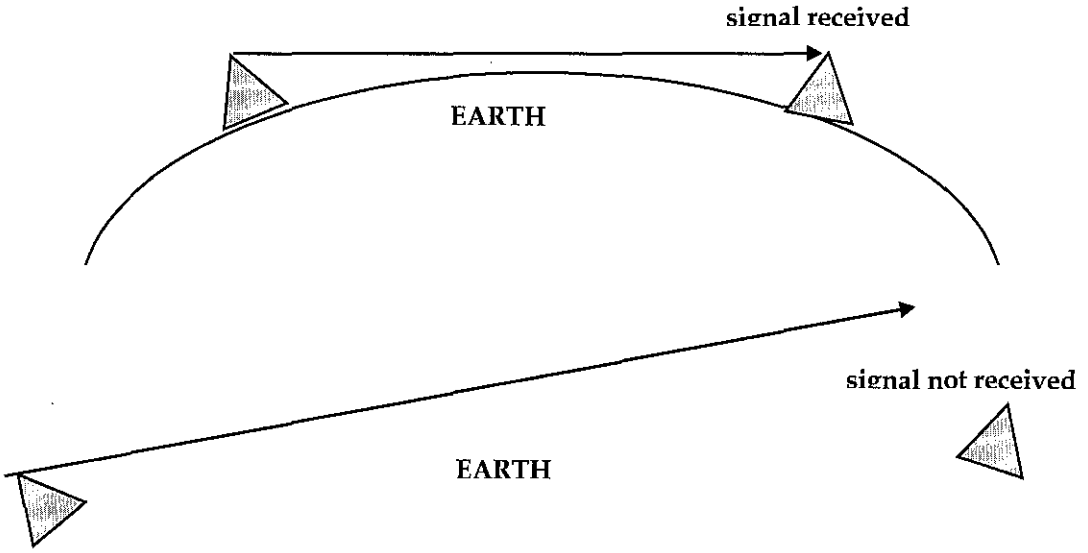


Figure 2 Line of Sight Propagation.

The range of transmission is mainly dependent on the power of transmission and the frequency of transmission. The signal received and transmitted is dependent on the surrounding condition and the frequency of operation. The rules of thumb of choice of frequency are as below.

- As the frequency increases, range decreases but so does the ambient noise
- Reflections from buildings increases with frequency

The relationship of frequency and the operation Excellencies can be seen from the table 1.

	LOW BAND	VHF	UHF	800 MHz
Interference	**Severe**	**Minimum**	**None**	**None**
Antennas	**Long**	**Short**	**Short**	**Short**
Gain	**Low**	**High**	**High**	**High**
Rural Range	**Excellent**	**Good**	**Fair**	**Fair**
Suburban Range	**Good**	**Excellent**	**Good**	**Fair**
Urban Range	**Poor**	**Good**	**Excellent**	**Excellent**

Table 1 Relationship of frequency and operation

Two-way radio communication can be one of three modes as listed below.

- Unit to unit
- Dispatch mode
- Repeater

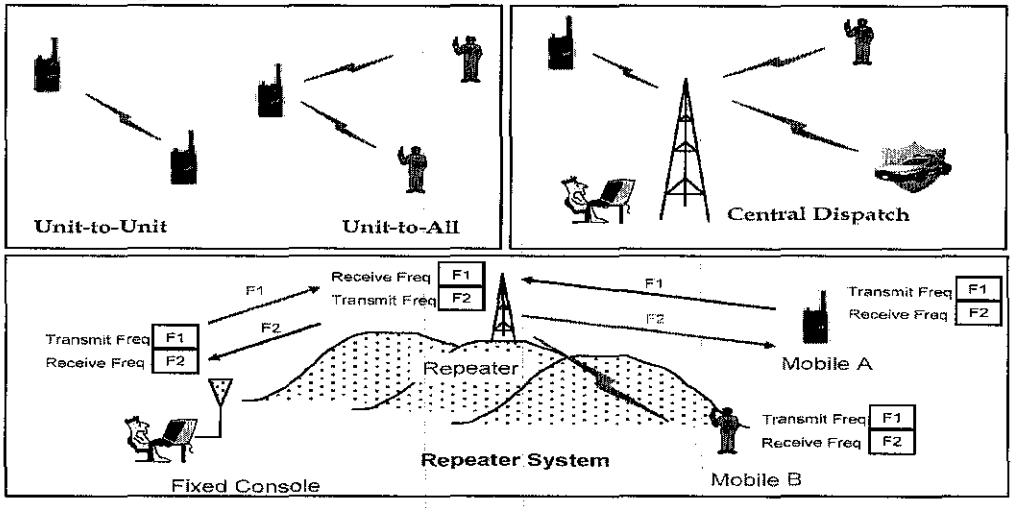


Figure 3 Mode of transmission

2.2 Mobile Two-way radio transmitter

Upon research and literature performed, there are several criteria that the transmitter of design needs to achieve. The transmitter chain needs to provide a 25W power with a 13.8V with a current goal of < 6.5A. This transmitter chain will be required to operate through +80 deg C to -40 deg C at operating supplies of 10.88V to 16.32V with a power leveling specification of -3dB +2dB. The transmitter will also need to be unconditionally stable to a load mismatch of VSWR=4:1 over voltage and temperature extremes. The PA will not be allowed to exceed its die temperature and the whole system not allowed to exceed the safety temperature limits when test through a 2+1 hour EIA Key down test. The safety feature to be incorporated must be activated and the need to ensure that the temperature cutback is operating when the excessive temperature is pick up. The transmitter will need to meet the 0.25uW radiated and conducted emission up to 1GHz and 2.5uW level up to 4 GHz.

The literature material showed that the transmitter line up for this VHF (216MHz to 247 MHz) band transmitter could be up banded from radio design of 146MHz to 174MHZ range. The topology could be used as reference in designing this VHF radio transmitter line up. The transmitter line up consists of three main amplification stages, namely pre driver, driver and power amplifier stage. In designing this line up, the input/output matching play critical role in order to achieve the criteria as stated in the pervious pages.

Upon reviewing the RF design materials, the architecture and various topologies of the mobile radio were learnt. The basic architecture of the radio was shown in the figure 4 below.

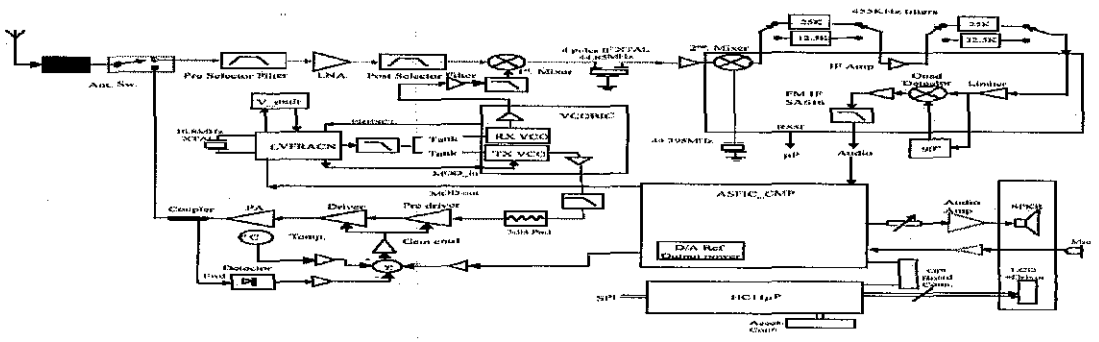


Figure 4 Mobile radio architecture

The transmitter line up consists of the 3 amplification stages: predriver, driver and power amplifier. The signal passes through these stages and gets amplified before it radiates out through antenna. The block diagram below in figure 5 shows the gain when signal passes through the stages.

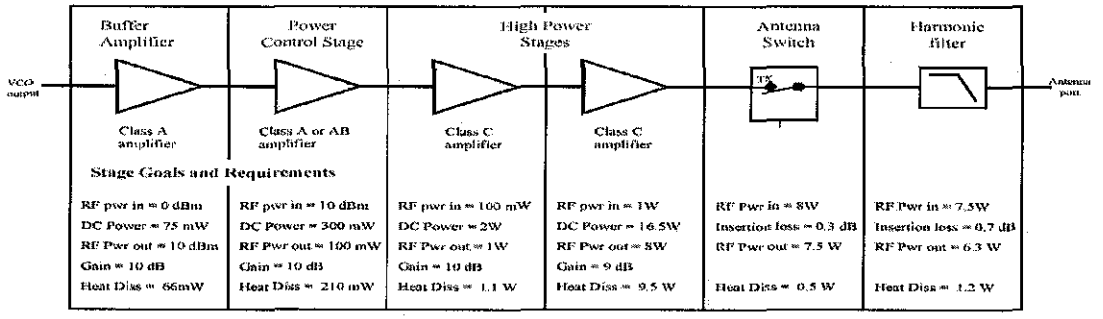


Figure 5 Transmitter line up

The project will involve designing the circuitries utilizing Advance Design Simulator or equivalent for sub-circuit simulation and optimization. Final proto-type realization for verification will be performed. Eventual result of this project is the mobile radio with the transmitter with the capability of transmitting at low power at VHF 220MHz range.

2.3 LDMOSFET Modeling Study

LDMOSFET- Laterally Diffused MOSFET is a widely used power amplifier. It is widely used in base station applications below a couple of GHz range as well as many other RF and microwave applications. However, due to its wide range of frequency range and power, the LDMOSFET model in simulation software is rarely developed. The existing high power amplifier model in simulation software has disadvantages like poor inter-modulation distortion prediction, lack of dynamic self-heating effect, complex extraction routines and so on.

In this project, the power and current cannot be simulated due to inexistence of the power amplifier model in ADS. Due to this reason, there is a need to develop a model in the simulation software. However, developing a new model of transistor in simulation software is not an easy task. Transistor has a wide range of model and the model is largely dependant on the simulation software requirement and preference. The model can be a BSIM4, Level 1, 2 or 3, HSPICE and so on. In Cadence PSPICE, usually they implement Level 3 modeling. In ADS, it gives the option to the user to model the transistor. It enables modeling using BSIM, Level 1, 2 or 3 and HSPICE.

Developing a model in ADS or other simulation software is a tough challenge but it can be very useful and time-saving in PA and transmitter design. Modeling of the device cannot be done without some good understanding of the modeling techniques and transistor characteristics. The main literature is some technical paper attached with this progress report. The study on the characteristics of PA and modeling techniques are the objectives of this project since modeling the device may take more than 2 semesters to complete and require great deal of effort in doing.

2.4 TIA/EIA testing and Evaluation

According to the Telecommunication Industry Association, two way radios are put under scrutiny in its performance by setting out a set of testing and specifications. This is carried out in order to evaluate the performance of the radio in an objective manner. The testing and specifications are set by acquiring the requirements from various users (manufacturing, construction, rescue team, public transportation and so on). The test is carried out to simulate to investigate the radio performance. Here is the list of testing and their significance. However, the procedures of the testing and detailed specifications are not shown due to confidentiality of the contents.

2.4.1 Transmit power and current

The carrier power output rating is the power available at the output terminal of the transmitter.

2.4.2 Transmit frequency error

The frequency error of the transmitter is the difference between the measured carrier frequency in the absence of modulation and the nominal frequency of the transmitter.

2.4.3 Transmit harmonic distortion

The Tx audio distortion is the voltage ratio, usually expressed as a percentage of the rms value of the undesired signal of the transmitter's demodulated output to the rms value of the complete signal at the output of the transmitter's demodulator.

2.4.4 Transmit Hum and Noise

The Tx Hum and Noise is the ratio of the standard test modulation to the residual frequency modulation measured by the test receiver. This is to be performed with any audio compression / expansion circuit disabled.

2.4.5 Conducted Spur

The Tx conducted spur emission is the unwanted that is generated or amplified in a transmitter and appear at the transmit antenna terminal.

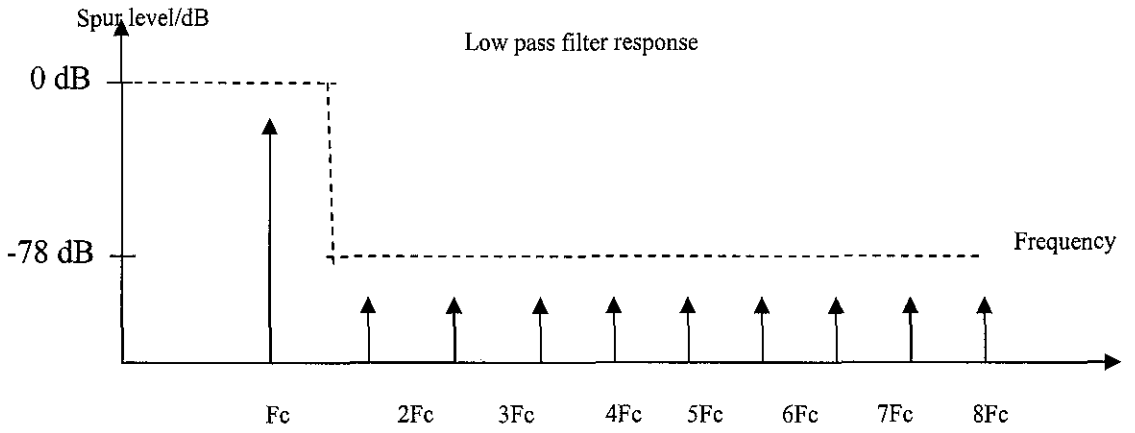


Figure 6 Conducted Spur at Fcs

The figure 6 shows the harmonics level that is generated from the transmitter. The spur at Fc is used for transmission while the rest are suppressed by HF/AS.

2.4.6 TIA Key Up/Down Safety Evaluation

This test is conducted to evaluate the safety aspect of the radio. Since the power output of the radio can go up to 30W, the power dissipation is of great concern. Thus, this test is needed to check the temperature of the radio at different section of the radio, like power amplifier, driver, crystal and chassis. The radio will be undergone a key up of 1 minute and key down of 4 minute continuously for 7 hours and followed by one hour of 5 minute of key up and 10 minute of key down. This is to check the temperature compensation loop is working.

2.4.7 Load Pull

Radio is subjected to a Voltage Standing Wave Ratio (VSWR) load pull during transmit state. The spectrum of the transmit signal is observed during the pull. This is done to simulate the real time situation where the radio is being used in real life. The existence of spur at non-frequency of operation is observed.

CHAPTER 3
METHODOLOGY

3.1 Methodology

There are software simulation and hardware approach to this project. The software simulation part has been completed in first semester while the hardware implementation of hardware has been conducted this semester. The flow chart in the figure 9 details the procedure in conducting this project

3.1.1 Feasibility Study (FYP I)

- Deals with the applicability of the use of upper or lower band radio to be used as reference in the design of transmitter of the band of interest.
- Study was on VHF and UHF radio topology and its potential up/down-band to 220 MHz was studied.
- Meanwhile, study has been conducted on the component devices and performed some preliminary calculation, shown in section 4.1 of this report.
- Outcome- UHF low power transmitter line up has been chosen as the topology for this project with its superior performance in power and current.

3.1.2 Circuit Design (FYP I)

- Design and simulate the circuit using ADS
- Developed the transmitter line up by using ADS
- Output- The circuit of the output matching network has been developed and the simulation has been performed. It shows fifty ohm matching.
- Refer to Appendix B for more ADS information.

3.1.3 On board measurement (FYP II)

- This approach is to implement the design on a PCB board and evaluate the performance
- Provide comparison between real circuit response with the result obtained from ADS

3.1.4 Optimization (FYP II)

- Upon getting the appropriate design, the ADS can be used to further improve the design through this optimization
- Use to improve the design in order to pass the specifications by bigger margin.
- Upon prototyping, the radio is tested. If any failure in term of design, optimization will be carried out on board. This could be done by using ADS as well, if a good correlation is achieved.

3.1.5 Prototyping (FYP II)

- Generate the circuit board that contains the RLC components and layout that was designed in the previous design stage
- Produce the circuit board that will be used for testing and evaluation.
- This has been done with the help of Motorola manufacturing line.

3.1.6 Testing and Evaluation (FYP II)

- The prototyped radio has been gone through testing that is set by the authority of telecommunication, TIA (Telecommunication Industry Association)
- The further details of testing and specifications can be seen in the section 2.4 and the test setup in figure 7.
- Beside of TIA testing, the radio has gone through a safety test that investigates the safety aspect of the radio.
- The load pull test has been conducted as well in order to investigate the impact of load pull to the radio operation. The test setup for load pull is shown in figure 8.

Transmit Test Setup

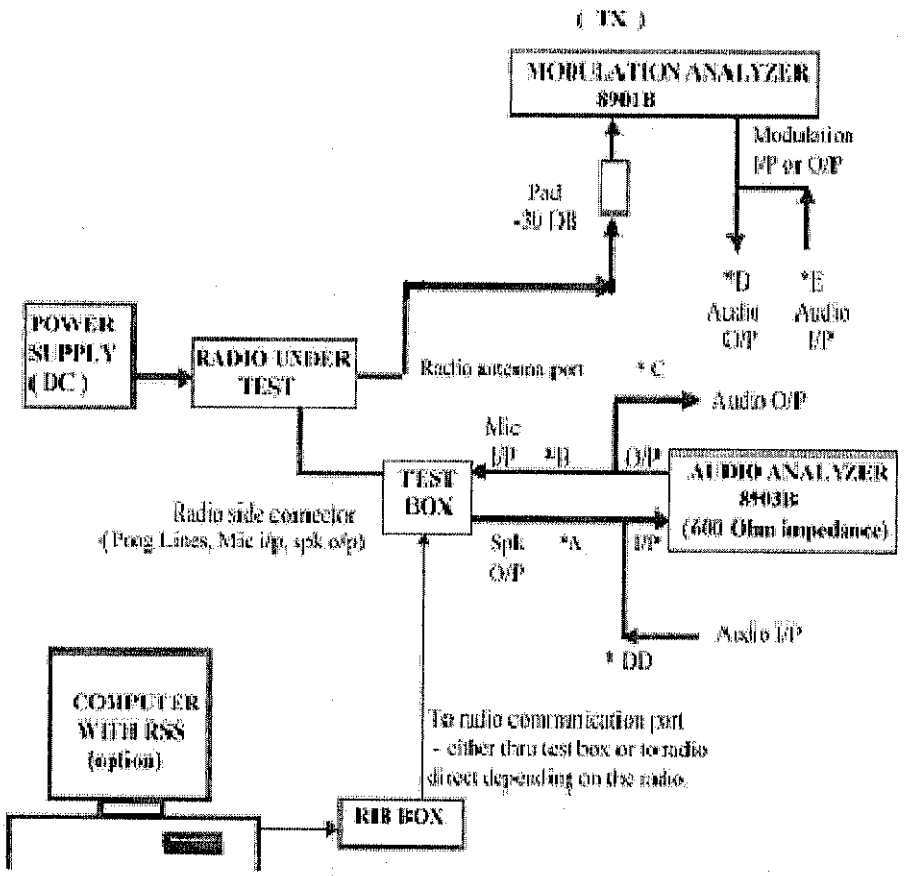


Figure 7 Transmit test setup

Load Pull test setup

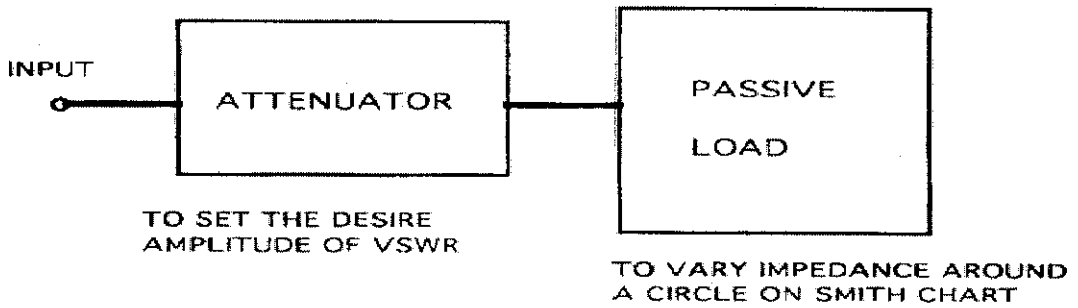


Figure 8 Load Pull test setup

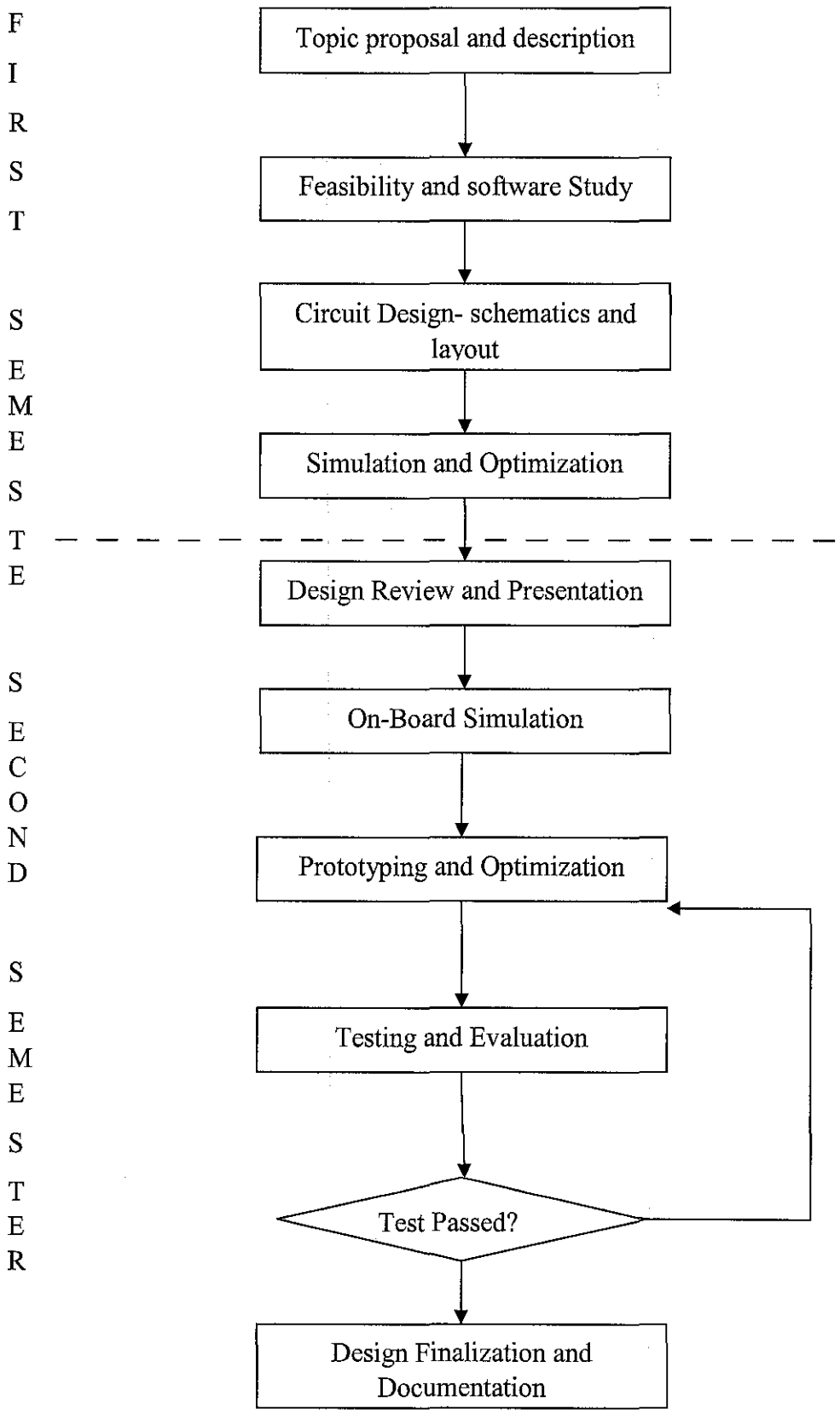


Figure 9 Project Flow Chart

CHAPTER 4
RESULT AND DISCUSSION

Over the two semesters, the project has been successfully completed. The transmitter line up that can operate in the 216-247 MHz range has been designed and prototyped. These sections will discuss the whole project design and result of the project.

4.1 Feasibility Study and Result

The project started off by conducting a preliminary calculation on the power that we can obtain from the current transmitter line up topology. Currently, for mobile radio, three stages amplification is performed. Table 2 shows the preliminary calculation. From here, we know that the current line up is capable of producing the desired power using the devices below.

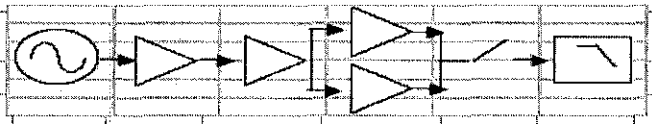
Preliminary Calculation TX Line Up Input data in Green								
		VCO	C65	MRF1518	MRF1535	AS	HF	Reserve Power
Reserve Power Condition								
RF Power In	Watts		0.002	0.5	5	50	46.5	
	dBm		3	27	37	47	46.7	
RF Power Out	Watts	0.002	0.5	5	50	46.5	42	> 37.5
	dBm		27	37	47	46.7	46.2	> 45
Gain	dB	-	25	10	10	0.5	0.5	

Table 2 Preliminary Power Calculation

The study on the current radios topology has been performed in order to benchmark a current working radio transmitter topology that can be utilized in this project. Upon research and some testing, it seems that UHF 350 MHz range radio was best suit for the use in this project. The main reason that drove me to this conclusion was the ability of the transmitter of this radio to produce output power of 20W at 220MHz range even though the matching network is matched for 350MHz range. Here is some data collected to strengthen my finding, shown in table 3.

From VHF 136MHz band radio

Frequency MHz	P max W	I rated A
136	52.6	5.42
148	55.9	5.44
162	56	4.63
216	6.5	2.2
229	2.52	1.76
247	0.9	1.1

From UHF 350MHz band radio

Frequency MHz	Pmax W	I rated A
350	47.7	4.4
365	44.6	4.5
380	36.3	4.5
216	18.5	3.65
229	16	3.5
247	15.6	3.41

Table 3 VHF 136MHz and UHF350MHz power measurement

From the comparison above, it clearly proved that the 350MHz matching network and transmitter line up gave us a closer starting design approximation to my project. However, it doesn't mean VHF range is not suitable for this project. The data above gave the information that the matching in UHF 350MHz is closer to our design than VHF. Using the UHF, we can get the matching for 220MHz band in an easier manner. Thus, the UHF 350 MHz transmitter topology has been chosen

4.2 Transmitter line up ADS simulation by using S-parameter from datasheet

In transmitter line up, the three main devices which are power amplifier (PA), pre-driver and driver. These three devices are operating in non linear region. In this region, their behaviors are unpredictable because the harmonics that are produced by the devices in this region. The S-parameter is provided by the manufacturer in the datasheet (see appendix G). This parameter was obtained through experiment conducted by the manufacturer at a particular voltage and biasing current. The output power is high, about 35 W. Thus, based on this S-parameter, the transmitter line up simulation by ADS should be feasible. Thus far, this approach has achieved the followings. Due to time constraint, only the output matching of the PA has been simulated. The interstate matching will adopt the current UHF 350 MHz radio configurations.

4.2.1 Schematic drawing

The transmitter line up simulation was first time being approached as, conventionally, hands on was performed to get the appropriate matching and result. Thus, the whole transmitter line up needs to be drawn on ADS platform. This started with a 50 ohm termination point from VCO input and passed through pre-driver, interstate matching, driver, interstate matching and finally PA and 50 ohm output termination.

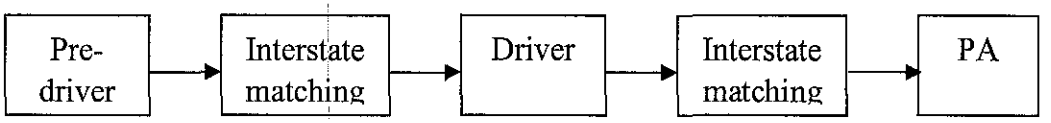


Figure 10 Transmitter Line Up

The schematic was shown in the appendix A and the current UHF band 1 transmitter lines up was shown in comparison. (Note: UHF band 1 and UHF 350 MHz have the same transmitter topology)

4.2.2 Transmission line up modeling

Real PCB board contains h substrate that may affect the system significantly if the radio is operating at high frequency in MHz range. Thus, the transmission

line of the real board should be taken into consideration as well in order to achieve good accuracy in simulation result. Correlation has been done in order to ensure the simulation result close to the actual on board result. The measurement was taken by measuring the length and width of the transmission line or known as runner. The measurement result was then entered into the ADS transmission line model. H-substrate of the PCB board depends on the material it was made of. Thus, data needs to be obtained from the vendor and the data was inserted into the ADS model as well. By doing that, the transmission line losses and characteristics will be similar to the one on board. This could produce a better and more correlated ADS simulation result.

4.2.3 Device modeling

The ADS do not have their library or simulation model of PA, pre-driver and driver. Thus, these devices need to be modeled for this simulation purpose. ADS have the capability of reading S-parameter files, in touchstone form. The file is known as s2p file. From the datasheet, the S-parameter file was generated by keying in the data from datasheet. Then, this file was linked to the 2 ports data item in ADS. Thus, when this data item with the file was used, it behaves as the device since the data item now is operating with the s-parameter of the device. Some simulations on this data item were done here and the result compromised to the data from datasheet.

I_{DQ} = 250 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\lvert S_{11}\rvert$	$\angle\phi$	$\lvert S_{21}\rvert$	$\angle\phi$	$\lvert S_{12}\rvert$	$\angle\phi$	$\lvert S_{22}\rvert$	$\angle\phi$
50	0.89	−173	8.496	83	0.014	−26	0.76	−170
100	0.90	−175	3.936	72	0.014	−14	0.79	−170
150	0.91	−175	2.429	63	0.011	−23	0.82	−170
200	0.92	−175	1.627	57	0.010	−44	0.86	−170
250	0.94	−176	1.166	53	0.007	−16	0.88	−170
300	0.95	−176	0.886	49	0.006	−44	0.91	−171
350	0.96	−176	0.686	48	0.005	36	0.92	−170
400	0.96	−176	0.568	44	0.005	−1	0.94	−171
450	0.97	−176	0.457	44	0.004	49	0.94	−172
500	0.97	−176	0.394	44	0.003	−51	0.95	−171
550	0.98	−176	0.332	42	0.001	31	0.95	−173
600	0.98	−177	0.286	41	0.013	99	0.94	−173

Table 4 S-parameter of MRF 1535T1

The table 4 shows the S-parameter of the PA MOSFET device, MRF1535T1, at biasing current of 250 mA and V of 12.5 V. This is the table that was created in the file that was linked to the ADS data item. When this item was read, the s-parameter as in the table will be used to generate the corresponding IC device behavior. The PA model, which has been modeled using the s-parameter method, has been implemented in the matching network circuit. The simulation has been performed together with the matching network in order to get a 50 ohm output matching. The details of the simulation and schematics are shown in section 4.2.4: Simulation and Optimization.

4.2.4 Simulation and Optimization

Thus far, only simple simulation on the two port item has been performed and the result was shown. The whole transmitter line up will be simulated in order to see the simulation result. The matching network were formulated and simulated. The result will be shown in and the related issues will be discussed.

Output Matching Network- The output matching network for the power amplifier has been attempted and simulated. The PA is represented by a block with the s2p touchstone format file while the whole line up has been drawn in the schematic in ADS platform, as shown in figure 11. The matching network is developed to match the output impedance of the PA to 50 ohm to ensure full power transmission. The simulation has been conducted and the result was shown in figure 12. The smith chart, tables and graphs show that in the 216 to 247 MHz range, the impedance was close to 50 ohm. Since the band of frequency in the passband is relatively large, it is hard to get an exact 50 ohm matching throughout the band. However, this close simulation result could provide a good first time approximation in the matching network design. Perhaps, some optimization will be required when the design has been implemented on board.

Output matching Simulation

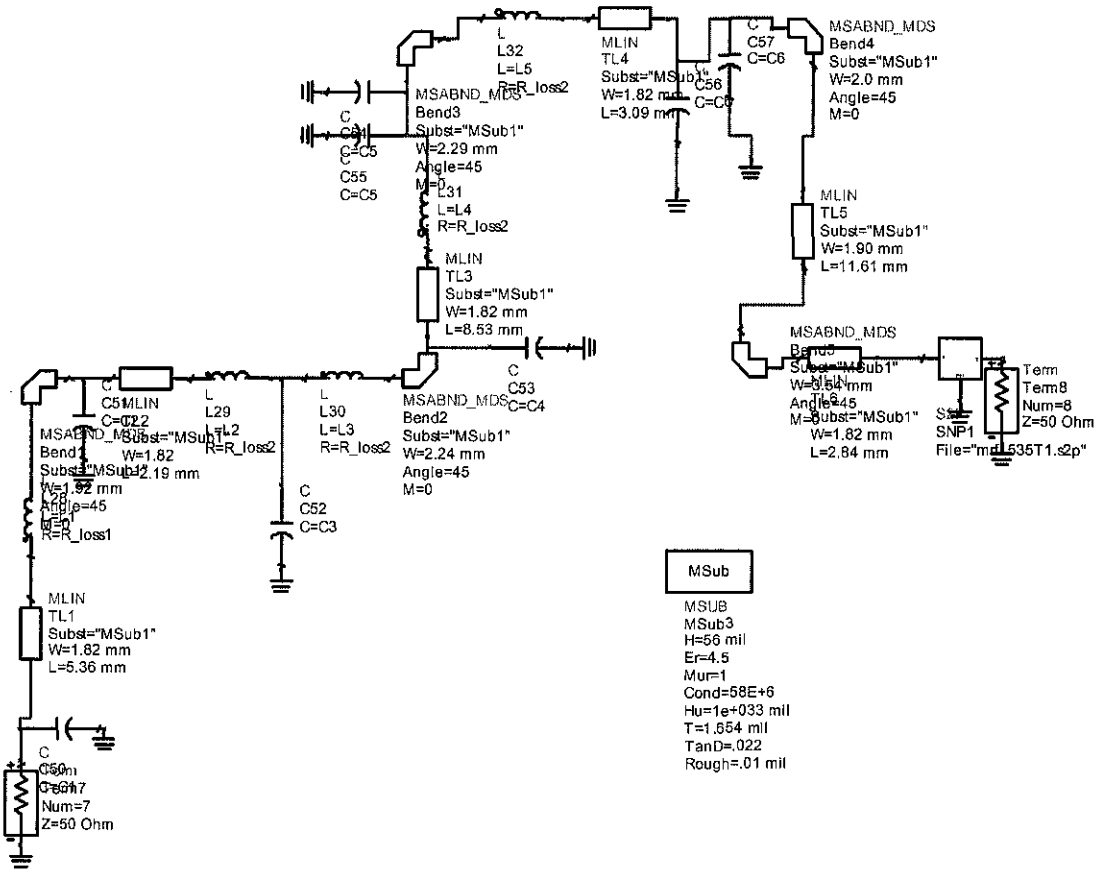
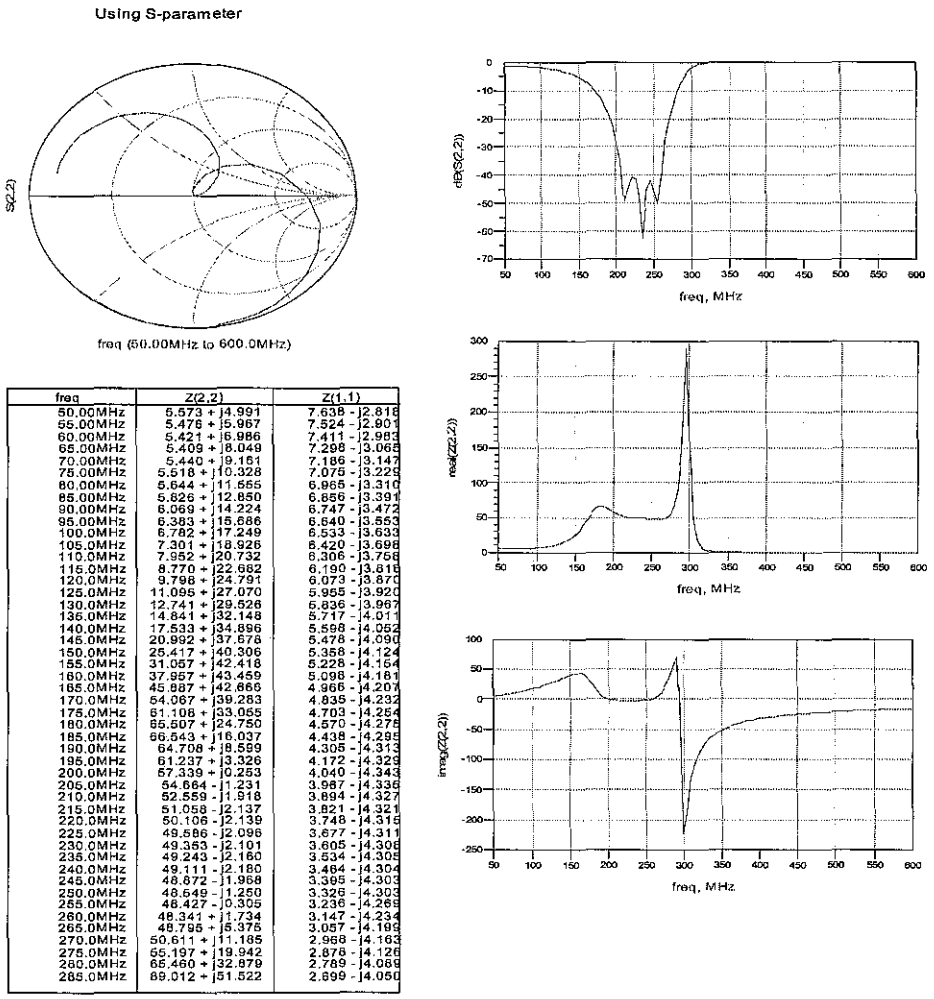


Figure 11 Output matching network of final PA

The schematic in figure 11 shows the line up of the final PA stage output matching network. The data item on the right contains the S-parameter which characterizes the PA device. The topology of line up above was based on the topology used in UHF band 1 radio transmitter. The transmission line in the figure 11 above was measured on board by using clipper and the characteristic of the board was obtained from vendor. The coil being used in the figure 11 above was a model formed by senior engineer Motorola. When we zoom into the coil, it is actually consists of inductor, resistor and coupling capacitor. Thus far, only ADS have the ability to simulate multi layer circuitry like the case here.



freq	Z(2,2)	Z(1,1)
50.00MHz	5.573 + j4.991	7.638 - j2.818
55.00MHz	5.476 + j5.967	7.524 - j2.901
60.00MHz	5.421 + j6.986	7.411 - j2.983
65.00MHz	5.409 + j8.049	7.298 - j3.065
70.00MHz	5.440 + j9.151	7.186 - j3.147
75.00MHz	5.518 + j10.328	7.075 - j3.229
80.00MHz	5.644 + j11.555	6.965 - j3.310
85.00MHz	5.826 + j12.850	6.856 - j3.391
90.00MHz	6.069 + j14.224	6.747 - j3.472
95.00MHz	6.383 + j15.686	6.640 - j3.553
100.0MHz	6.782 + j17.249	6.533 - j3.633
105.0MHz	7.301 + j18.926	6.429 - j3.698
110.0MHz	7.952 + j20.732	6.306 - j3.756
115.0MHz	8.770 + j22.682	6.190 - j3.815
120.0MHz	9.798 + j24.791	6.073 - j3.870
125.0MHz	11.095 + j27.070	5.955 - j3.920
130.0MHz	12.741 + j29.526	5.836 - j3.967
135.0MHz	14.841 + j32.148	5.717 - j4.011
140.0MHz	17.533 + j34.896	5.598 - j4.052
145.0MHz	20.992 + j37.678	5.478 - j4.090
150.0MHz	25.417 + j40.306	5.358 - j4.124
155.0MHz	31.057 + j42.418	5.228 - j4.154
160.0MHz	37.957 + j43.459	5.098 - j4.181
165.0MHz	45.887 + j42.666	4.966 - j4.207
170.0MHz	54.067 + j39.253	4.835 - j4.232
175.0MHz	61.108 + j33.055	4.703 - j4.254
180.0MHz	65.507 + j24.750	4.570 - j4.275
185.0MHz	66.543 + j16.037	4.438 - j4.295
190.0MHz	64.708 + j8.599	4.305 - j4.313
195.0MHz	61.237 + j3.326	4.172 - j4.329
200.0MHz	57.339 + j0.253	4.040 - j4.343
205.0MHz	54.664 - j1.231	3.907 - j4.336
210.0MHz	52.559 - j1.918	3.894 - j4.327
215.0MHz	51.058 - j2.137	3.821 - j4.321
220.0MHz	50.106 - j2.139	3.748 - j4.315
225.0MHz	49.586 - j2.096	3.677 - j4.311
230.0MHz	49.353 - j2.101	3.605 - j4.306
235.0MHz	49.243 - j2.160	3.534 - j4.305
240.0MHz	49.111 - j2.180	3.464 - j4.304
245.0MHz	48.872 - j1.968	3.395 - j4.303
250.0MHz	48.549 - j1.250	3.326 - j4.303
255.0MHz	48.427 - j0.305	3.236 - j4.269
260.0MHz	48.341 + j1.734	3.147 - j4.234
265.0MHz	48.795 + j5.376	3.057 - j4.199
270.0MHz	50.611 + j11.185	2.968 - j4.163
275.0MHz	55.197 + j19.942	2.878 - j4.126
280.0MHz	65.460 + j32.879	2.789 - j4.089
285.0MHz	89.012 + j51.522	2.699 - j4.050

Figure 12 Simulation result of output matching of PA

The result of the output matching network was shown above. The Smith chart shows the s-parameter across the frequency. In the frequency of interest, 216 to 247MHz, the 50 ohm matching was closely reached. This was shown in the table above. The impedance value was displayed and the impedance was close to 50 ohm. This indicated the output 50 ohm matching has been approximated.

Another parameter of interest is the input/output return loss. This parameter was less than -40 dB, which was small enough to create any reflection to both the input and output of the device.

4.3 Harmonic Filter and Antenna Switch ADS Simulation

Harmonic filter and antenna switch are the two sections of the circuitry in transmitter before the signal being transmitted and radiated out of the radio to the air. The main purpose of harmonic filter is to suppress any of the harmonics produced by the transmitter while the antenna switch ensures good isolation between transmitter and receiver. This is the continuation of work from the industrial training in Motorola. With ADS and the simulation file created during internship, the circuitry was optimized and simulated. The schematics of the harmonic filter and antenna switch were shown in figure 13 below.

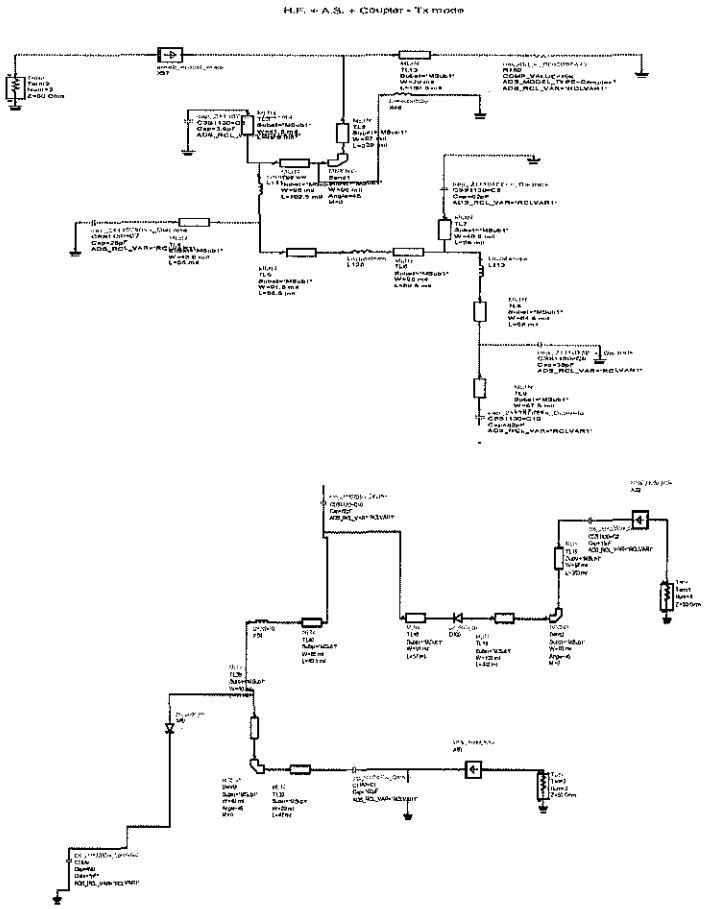


Figure 13 Antenna switch and harmonic filter of transmitter

With ADS, the simulation has been performed by using real time components and transmission lines. The result was obtained and displayed in the figure 14.

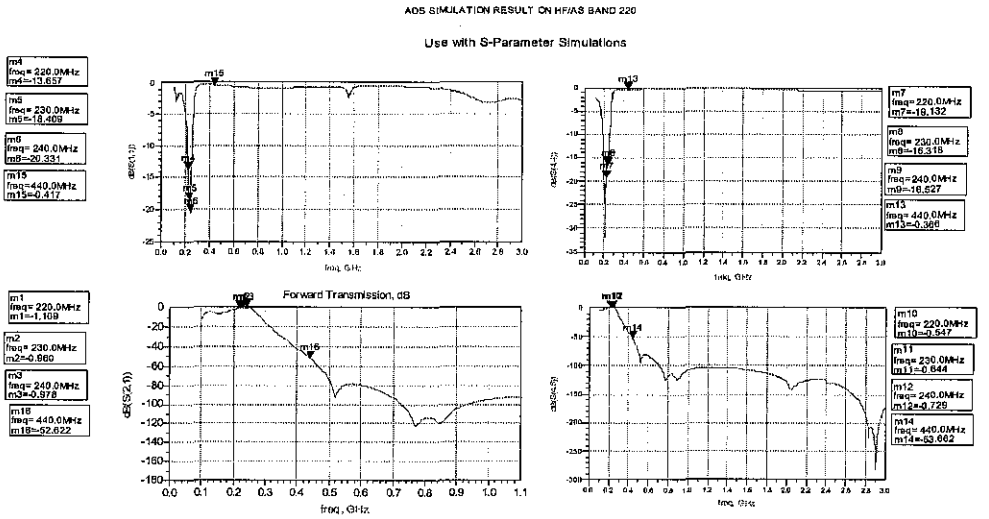


Figure 14 HF/AS Simulation Result

The result shows the simulation of the HF/AS on ADS. The two curves on the left are the input/output return loss and insertion loss of the HF/AS in receive mode while the two curves on the right are the input/output return loss and insertion loss at transmit mode. There are some internal specifications to be met in designing HF/AS.

Parameters	Receive Mode	Transmit Mode
Input/Output Return Loss (pass band)	-15 dB	-12 dB
Insertion Loss (pass band)	-1.5 dB	-1.5dB

Table 5 Specifications to be met for HF/AS Design

Comparing the result obtained from ADS and the specifications, it shows the design is passing the specifications by at least one dB Smaller input/output return loss is desired to suppress the reflected energy at both transmit and receive mode, thus, ensure signal pass in one direction. Insertion loss is high to allow the signal to pass through with minimal losses.

4.4 Coupler Simulation

The figure 15 below shows the location of coupler and the ADS schematic of coupler. The coupler is a micro strip printed circuit, which couples a small amount of the forward power of the RF power from power amplifier. The coupled signal is rectified to an output power which is proportional to the DC voltage rectified by diode and the resulting DC voltage is routed to the power control to ensure that the forward power out of the radio is held to constant value.

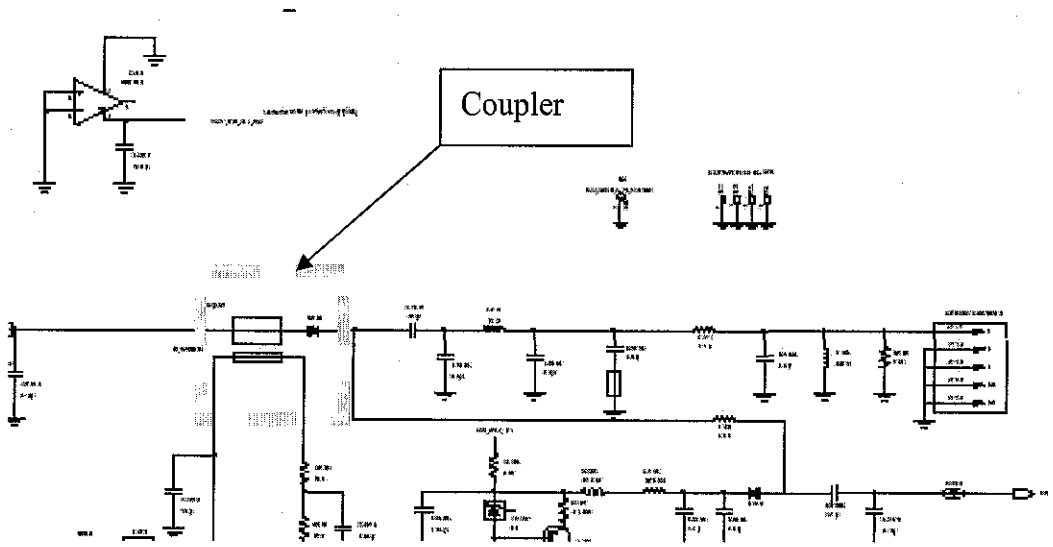
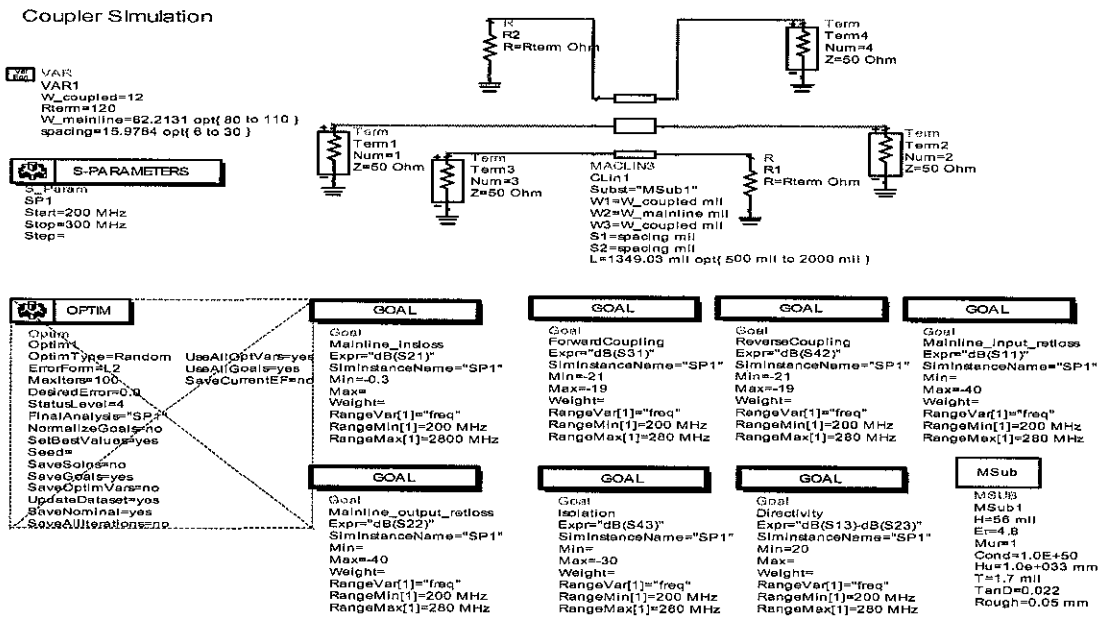


Figure 15 Location of coupler (above) and Coupler schematic (below)



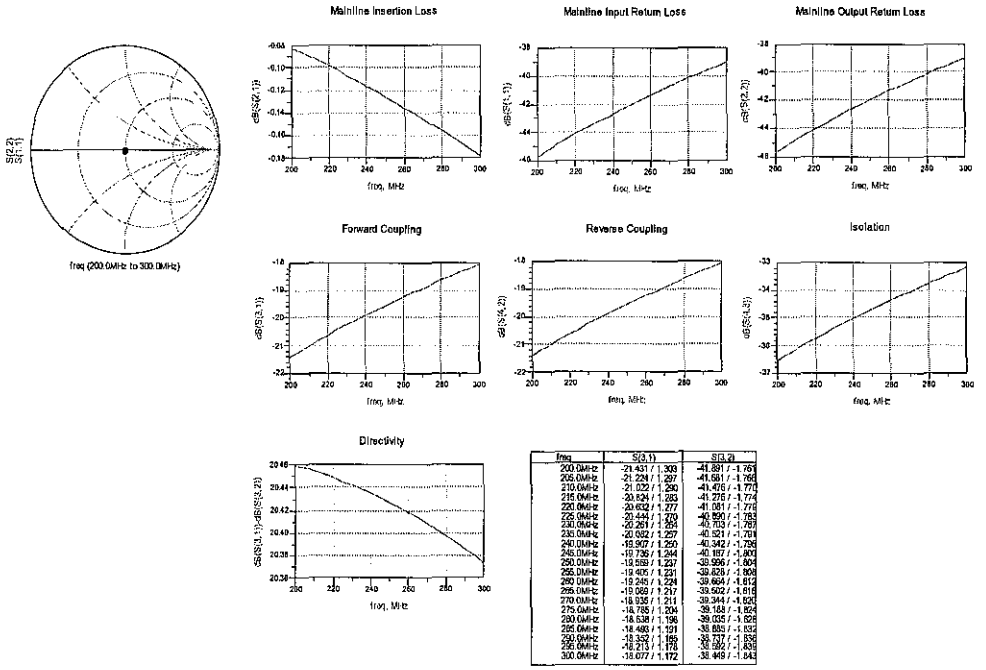
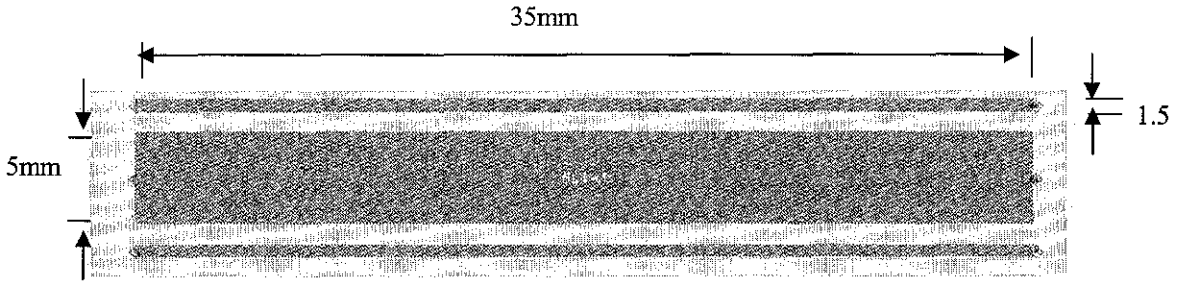


Figure 16 Simulation result of Coupler (above) and the resultant coupler on PCB (below)



The result above shows the 50 ohm matched coupler and the graphs show the insertion loss and return loss of the coupler across the frequency. From the simulation, the on board coupler can be simulated as shown in the diagram above, where the coupler consists of one mainline and two smaller coupling path.

4.5 Power Control ALC Simulation

The purpose of applying power control was stated in the theory section of this report. The schematic below shows the power control of the PA device. This was partial of the whole power control of the radio as the simulation of the power control of whole PA may take much longer time to understand and simulate. The PA model below was basically represented by a non linear voltage control voltage source in order to show the PA non linear voltage characteristic.

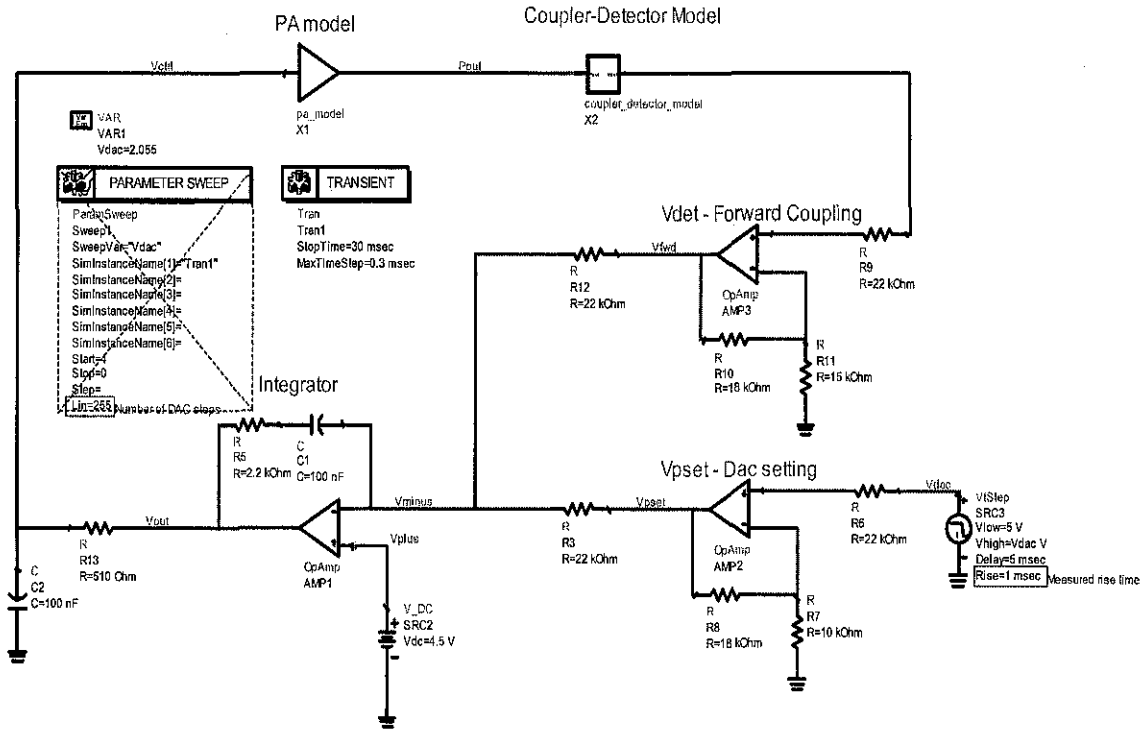


Figure 17 Power control of final PA

The graphs in figure 18 show the PA stage power control. There is output power versus time to show the transient when the PA was powered up. Then, the rest of the graphs show the changes of voltage level at starting up or transient stage. This stage is critical especially in transmission mode. When PA was keyed up, the time it took to reach its rated power will determine its ability in sending out the message at that particular channel. Consider a crowded and busy 2 way radio communication situation, the radio that has the shortest transient period will be capable of transmitting the signal by capturing the particular channel. Slow transient will cause delay in transmission of signal

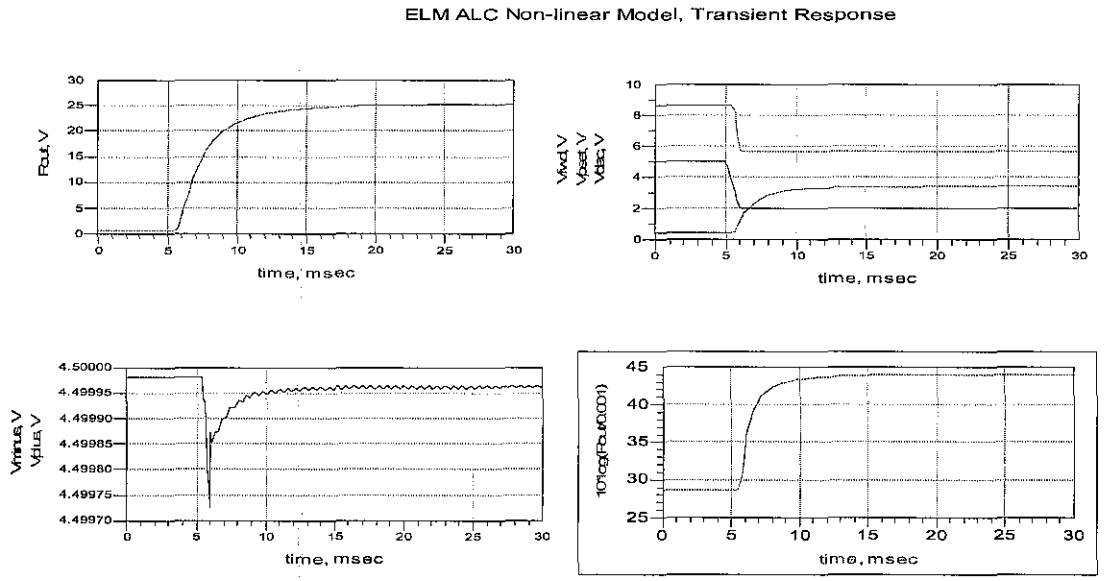


Figure 18 Power Control Simulation Result

4.6 Antenna Switch and Harmonic Filter- On Board Measurement

The simulation result obtained has been implemented on board. In practical, the AS/HF section of the board will go through measurement by using HP network analyzer with high accuracy. Here, the AS/HF section is isolated from the receiver and transmitter path in order to investigate the performance of the AS/HF itself. In this measurement, there will be two sub measurements, transmit path and receive path. The parameters being measured are Return loss and insertion loss. These parameters have significant implication as their values will predict the performance of the radio. Here, a comparison of the ADS simulation result and on board measurement has been shown and discussed below.

4.6.1 ADS Simulation

The figure 19 shows the ADS simulation result of HF/AS in transmit path. The result is similar to figure 13 but in this case, the transmit path result has been taken and zoomed in. By using ADS simulation, a set of capacitors value has been obtained.

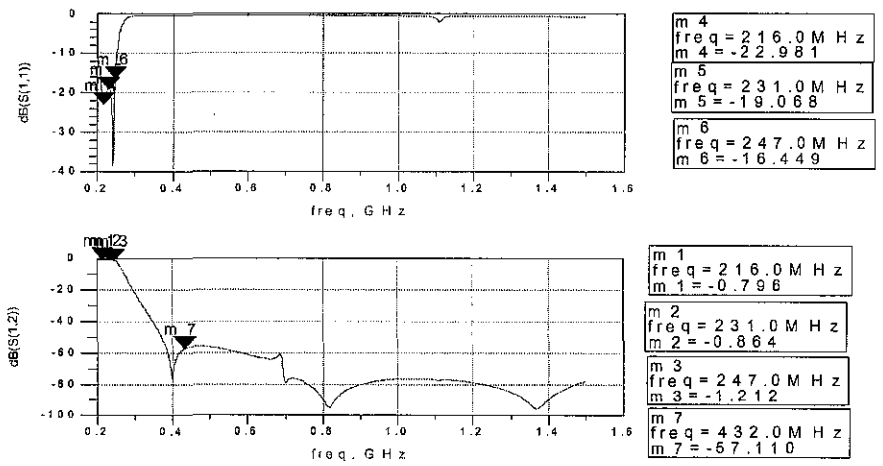


Figure 19 ADS Simulation result on transmit path- Return loss(above) and insertion loss (below)

Figure 19 shows the ADS simulation result of the AS/HF. The parameters are meeting the specification as specified by the design guidelines where insertion loss must not less than -1.5 dB and return loss must be less than -15 dB. From ADS, it gave a good approximation in designing the AS/HF. In order to get accurate result, transmit and receive simulation has been performed and optimized.. The design has

then been implemented on PCB board and the measurement has been done by using network analyzer. The result has been obtained and analyzed. On board optimization has been performed to get better performance.

4.6.2 On Board Measurement of AS/HF

The set of values from ADS have been obtained and applied on board. The practical measurement using network analyzer has been conducted and the result was tabulated as below.

TX	Frequency, MHz	Insertion Loss, dB	I/O RL, dB	GOAL	
				Insertion Loss, dB	I/O RL, dB
	216	-0.7	-18	-1	-15
	231.5	-0.8	-17		
	247	-0.9	-18		
RX	Frequency MHz	Insertion Loss dB	I/O RL dB	Insertion Loss, dB	I/O RL, dB
	216	-0.8	-14	-1.5	-12
	231.5	-0.9	-17		
	247	-0.9	-16		

Table 6 AS/HF On-board Measurement Result

Table 6 show that the Tx and Rx path have parameters passing the goal with good margin. This result is obtained after some optimization has been performed on the AS/HF.

4.7 Power and Current of Transmitter Line Up

With the completion of AS/HF design and optimization, the matching network of the PA output is integrated with the AS/HF that has been designed early on. The matching network topology is based on the UHF 350MHz radio while the set of starting values for the RLC components for PA output matching are obtained from ADS simulation. The configurations for matching network from predriver to driver stage are based on UHF 350MHz radio as the interstate matching is feasible for operation in 216 to 247 MHz range. Here, the result before and after on board measurement are shown.

4.7.1 Pre-optimized Power

With the set of values obtained from the matching network in ADS simulation, the power level is not encouraging. The power is measured at its maximum power tapped out from the antenna. The result has been shown in table 7 below.

Frequency MHz	Pmax W
216	18.5
229	16
247	15.6

Table 7 Maximum Power

The goal for the maximum power is 37.5W while rated current goal is less than 6A. The rated current level at its rated power is not obtainable since the power could not reach the rated power of 25W. (Notes: rated current is the current when the rated power is reached). With that, it indicates that the matching network developed from the ADS is far from the desire result. From here, some optimization on the matching network is definitely needed.

4.7.2 Post-optimized Power and Current

On board optimization is the practice conducted to improve the relevant parameters by tweaking the capacitor or inductor values. Simulation result may give a rough first time approximation as the starting point of the design while tweaking is still much

needed to obtain the desire result.

Here, optimization has been mainly conducted on the output matching network. Tweaking of the capacitors is conducted by replacing the capacitor with a higher or lower cap values. After some optimization, the power and current of the design is measured and the result is shown below.

			GOAL	
Frequency MHz	P MAX W	I RATED A	P MAX W	I RATED A
216	54	5.8	>37.5	<6
221.2	52	4.9	>37.5	<6
226.4	42	5.5	>37.5	<6
231.5	40	4.8	>37.5	<6
236.7	39	4.8	>37.5	<6
241.9	38	4.6	>37.5	<6
247	38	4.4	>37.5	<6

Table 8 Post-optimized power and current level

The result shows great improvement after optimization. The result is passing the specifications as in the design guidelines. With that, the transmitter line up is set up. The full line up and its corresponding components are updated to the schematic and layout. With that, the radio can be prototyped and the performance of the radio as a whole can be tested and evaluated.

4.8 Conducted Spur

During the design process, we faced a conducted spur issue where the radio was failing this parameter by more than 3dB. Thus, this issue was brought in and discussed here.

Conducted Spur is one of the significant parameters in transmitter line up design. When the PA is powered up, the tx line up (from pre-driver to PA) will amplify the signal coming from the function generating unit of the radio (FGU). The signal from FGU is set a particular frequency within the range of 216 to 247 MHz. However, when the signal comes out from the PA, the harmonics of the signal will get amplified as well. In FGU, the signal is generated at one frequency and same time; the harmonics will be produced as well. The harmonics will go through the amplification stages and radiated out from the antenna. Conducted Spur is a measure of the harmonics level generated and radiated out from the antenna. Refer to the design of transmitter line up; there is actually a harmonic filter stage before the antenna. This HF is actually responsible to suppress these harmonics. After the radio is prototyped, this parameter is investigated and the result is shown below.

Conducted Spur can be measured by using high end spectrum analyzer. By having appropriate setup and safety procedures, the conducted spur can be seen in the spectrum. The conducted spur at the transmit frequency was capture and shown below. The same method is repeated at its harmonic frequencies.

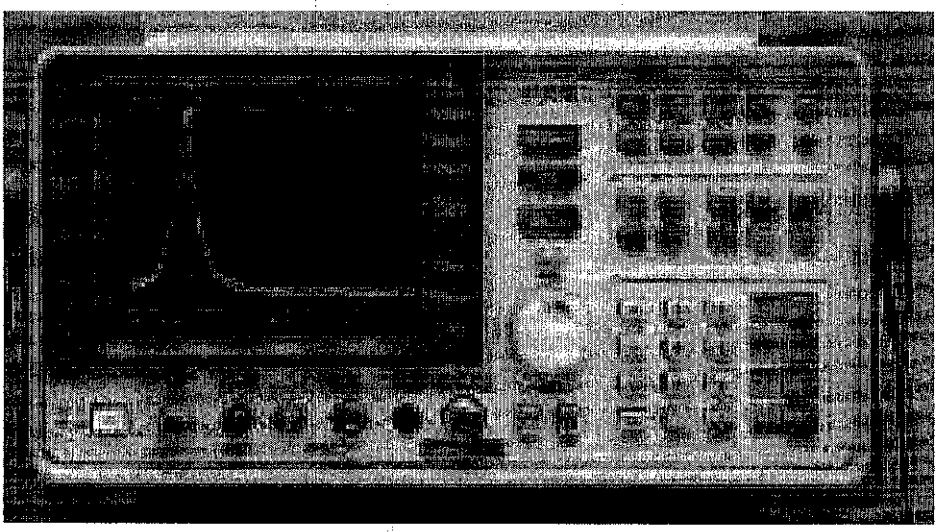


Figure 20 Spectrum analyzer and conducted spur at fc

The figure 20 shows the spur at the transmit frequency, 216MHz. The spectrum clearly shows the spurious level and that frequency. The spur at this frequency is relatively higher than other harmonics level. This is explainable due to the reason that the harmonic filter is tailored for transmission at the frequency range of 216 to 247MHz. The insertion loss of frequency in this range is higher, thus signal can pass through the filter. However, the filter is designed to suppress the harmonics to less than -36dbm. The test has been done and the result is shown in table 9.

Channel 1		Operating Voltage, V		Channel 2		Operating Voltage, V		Channel 3		Operating Voltage, V	
216 MHz	10.88	13.8	16.32	231.5 MHz	10.88	13.8	16.32	247 MHz	10.88	13.8	16.32
Fc in dBm				Fc in dBm				Fc in dBm			
2 fc	-25.42	-23.6	-22.9	2 fc	-30	-29.4	-31.6	2 fc	-50.7	-48	-53
3 fc	-46	-43.1	-41	3 fc	-45	-43.1	-42.3	3 fc	-68.6	-41	-39
4 fc	-44	-43	-42	4 fc	-41	-38	-40	4 fc	-41	-42	-44
5 fc	-44	-42	-44.5	5 fc	-49	-49	-45	5 fc	-54	-56	-54
6 fc	-56	-57	-55	6 fc	-44	-43	-44	6 fc	-53	-53	-54
7 fc	-55	-53	-53.9	7 fc	-53	-49	-53	7 fc	-59	-55	-62
8 fc	-60	-58	-55	8 fc	-53	-52	-52	8 fc	-67	-68	-68
9 fc	-62	-61	-59.8	9 fc	-51	-45	-50.5	9 fc	-58	-56	-53
10 fc	-64	-62	-62	10 fc	-50	-51	-50	10 fc	-68	-58	-70

Table 9 Conducted Spur Measurement (Goal: fc<-36dBm)

The result shows that failure is seen in 2^{nd} fc. This reflected that the harmonics at 2^{nd} fc is relatively high since the HF attenuation is insufficient to suppress this harmonic. As a result, optimization has been conducted to alleviate this conducted spur problem. Changes have been made to the HF and output matching stages. The radio has been reworked and the post-optimized result was shown below. The implementation shows no degradation in power and current measurement. It is shown below.

	R1		R2		GOAL	
Frequency	P MAX	I RATED	P MAX	I RATED	P MAX	I RATED
MHz	W	A	W	A	W	A
216	44.5	5.5	49	5.5	>37.5	<6
221.2	45	4.8	48	4.7	>37.5	<6
226.4	43	4.5	45	4.5	>37.5	<6
231.5	44	4.7	46	4.8	>37.5	<6
236.7	45	5.2	47	5.4	>37.5	<6
241.9	47	5.5	49	5.7	>37.5	<6
247	47	5.6	51	5.8	>37.5	<6

Table 10 Post-optimization Power and Current Measurement

Channel 1		Voltage, V		Channel 2		Voltage, V		Channel 3		Voltage, V	
216 MHz	10.88	13.8	16.32	231.5 MHz	10.88	13.8	16.32	247 MHz	10.88	13.8	16.32
fc				fc				fc			
2	-50	-50	-52	2	-45	-43	-43	2	-44	-42	-43
3	-44	-44	-42	3	-55	-53	-51	3	-47	-49	-46
4	-42	-40	-38	4	-44	-42	-42	4	-42	-47	-42
5	-50	-47	-50	5	-48	-45	-47	5	-42	-43	-42
6	-48	-49	-50	6	-49	-48	-47	6	-44	-45	-47
7	-50	-51	-48	7	-48	-45	-46	7	-44	-45	-48
8	-49	-53	-49	8	-51	-50	-51	8	-42	-48	-47
9	-54	-48	-51	9	-52	-51	-50	9	-48	-44	-43
10	-48	-47	-46	10	-50	-50	-50	10	-44	-45	-47

Table 11 Post-optimization Conducted Spur Measurement

The result after optimization shows great improvement in conducted spur measurement. With that, the conducted spur issue has been solved. The root cause is identified as high harmonics due to mismatch of the output matching of PA to the harmonic filter section.

4.9 EIA/TIA Key Up/Down safety Test

EIA/TIA is the governance that stands for Telecommunication Industry Association, which is responsible in governing the standard and specifications of telecommunication products. Two way radios is one of the products that is being governed by this authority. Key up/down test is one of the safeties tests that need to go through before the radio can be released to the market. This test involves the temperature measurement of the different part of the radio. The temperature, when the radio is transmitting and receiving signal, is recorded by the hi-end devices. Thermal sensor is placed on driver, power amplifier device, crystal and the ambient point. The procedure involves keying up the radio for one minute and followed by 4 minutes of dekeying. The temperature at that various points will be recorded by the sensor and workstation. The test on one of the operating frequency has been completed so far and it is shown below.

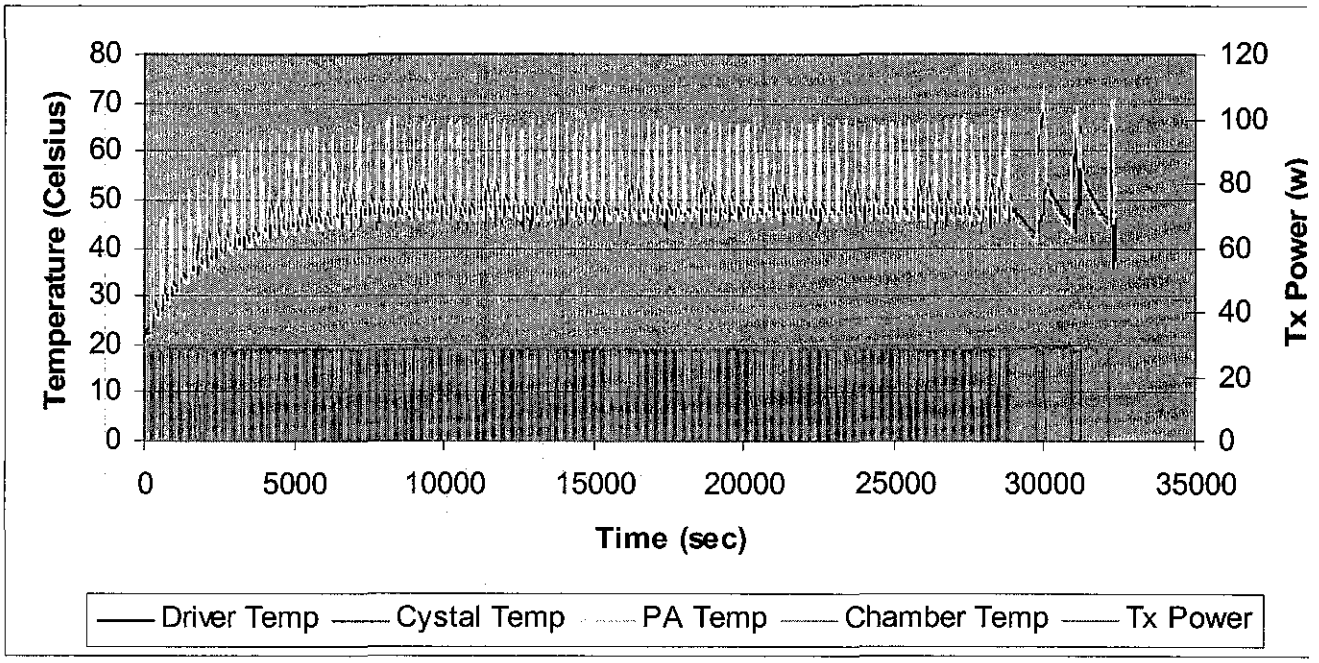


Figure 21 EIA Key Up/Down Test For frequency 231.5MHz

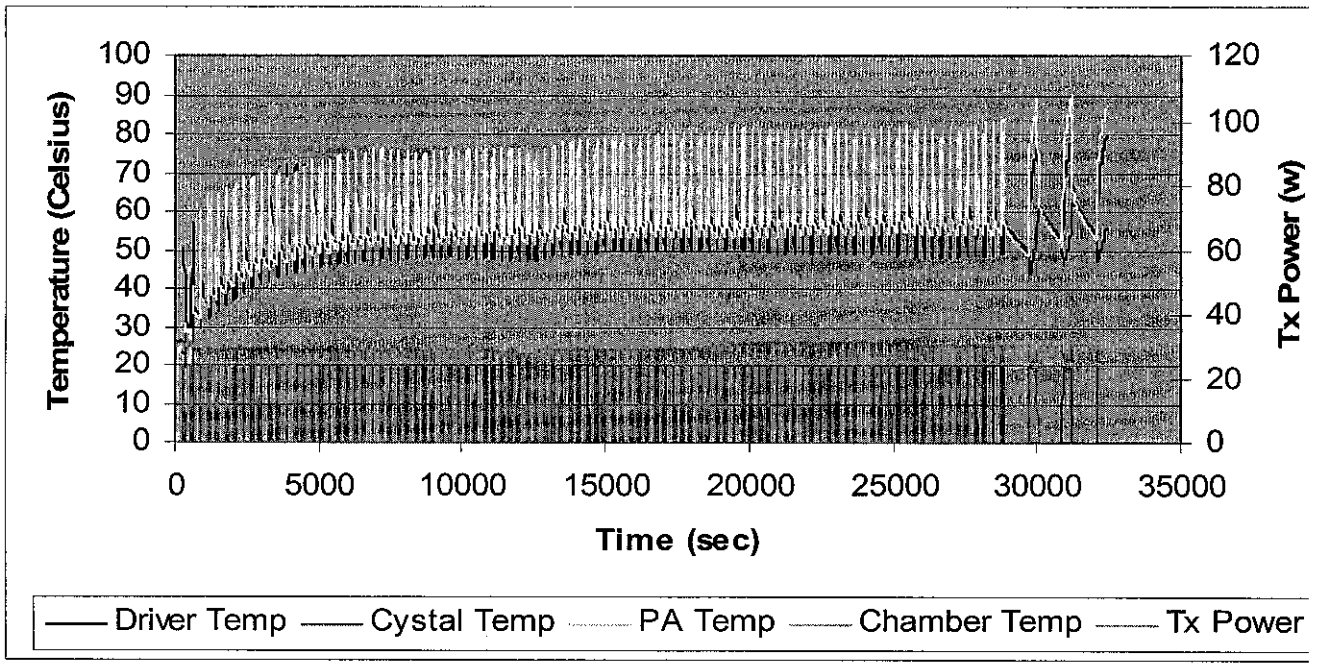


Figure 22 EIA Key Up/down for frequency 247MHz

The result shows that the PA and driver temperature is higher than crystal and it is norm of the operation as most of the temperature will be dissipated at driver and PA. However, there is a strange phenomenon at the end of the cycle as the driver temperature is higher than PA. It maybe caused by the malfunction of the station as it is the first time running after down for a while in host company. More verification will be done in near future.

4.10 TIA Parametric Measurement

According to Federal Communication Commission, all the two way radios need to go through a series of parametric check before the radio can be released and used in the market. Referring to the project objective and proposal from Motorola, the transmitter line up needs to go through and pass all the parametric test before the design is considered completed. The testing and evaluations involve the testing as listed below.

- Transmit Power and Current
- Transmit Frequency Error
- Transmit Harmonic Distortion
- FM Hum and Noise
- Conducted Spur

Each of these parameters has significant effect on the radio performance during transmit mode. For each parameter, there is specification that the radio needs to pass before the design is considered complete. The significance of the parameters has been explained in the literature review section of this report while the measurement methods are explained in the appendices. The radio has been tested and the result is shown in table 12 and 13 below.

Transmitter Test Data	Summary								
Model:									
Channel Spacing					25k				
Frequency		216			232			247	
Voltage:	10.88	13.60	16.32	10.88	13.60	16.32	10.88	13.60	16.32
Test Parameter									
Frequency Error	0.13	0.07	0.06	0.12	0.06	0.08	0.15	0.01	0.01
Tx. Power (W):	15.8	26	25.1	17.1	27	26.6	15	26	26
Tx. Current (A):	4.2	5.2	5.3	3.7	4.5	4.3	4.4	5.3	5.5
Harmonic Distortion (%):	0.5	0.5	0.5	0.4	0.5	0.5	0.5	0.4	0.5
FM Hum & Noise (dB):	-49.1	-50.3	-50.4	-49.1	-49.3	-49.2	-46.8	-47.1	-47.9
Conducted Spurious (dBm):									
2fc	-50	-50	-52	-45	-43	-43	-44	-42	-43
3fc	-44	-44	-42	-55	-53	-51	-47	-49	-46
4fc	-42	-40	-38	-44	-42	-42	-42	-47	-42
5fc	-50	-47	-50	-48	-45	-47	-42	-43	-42
6fc	-48	-49	-50	-49	-48	-47	-44	-45	-47
7fc	-50	-51	-48	-48	-45	-46	-44	-45	-48
8fc	-49	-53	-49	-51	-50	-51	-42	-48	-47
9fc	-54	-48	-51	-52	-51	-50	-48	-44	-43
10fc	-48	-47	-46	-50	-50	-50	-44	-45	-47

Table 12 Transmit parametric result for 25khz channel spacing

Channel Spacing					12.5k				
Frequency		216			232			247	
Voltage:	10.88	13.60	16.32	10.88	13.60	16.32	10.88	13.60	16.32
Test Parameter									
Frequency Error	0.28	0.22	0.24	0.3	0.25	0.27	0.3	0.28	0.3
Tx. Power (W) :	16	25	5.4	17	27	26.7	15	25.2	26
Tx. Current (A) :	4.2	5.3	5.4	3.7	4.4	4.4	4.5	5.4	5.5
Harmonic Distortion (%) :	0.8	0.8	0.8	0.9	0.9	0.9	1.0	0.9	1.0
FM Hum & Noise (dB) :	-45.3	-45	-45.1	-43.8	-43.9	-43.3	-42.5	-42.5	-42.3
Conducted Spurious (dBm) :									
2fc	-49	-50	-52	-46	-44	-43	-44	-43	-43
3fc	-43	-44	-43	-52	-53	-53	-48	-49	-45
4fc	-42	-40	-38	-44	-42	-42	-42	-47	-42
5fc	-50	-47	-50	-48	-45	-47	-42	-43	-42
6fc	-48	-49	-50	-49	-48	-47	-44	-45	-47
7fc	-50	-51	-48	-48	-45	-46	-44	-45	-48
8fc	-49	-53	-49	-51	-50	-51	-42	-48	-47
9fc	-54	-48	-51	-52	-51	-50	-48	-44	-43
10fc	-48	-47	-46	-50	-50	-50	-44	-45	-47

Table 13 Transmit parametric result for 12.5khz channel spacing

4.11 Talk and Listen Test

The radio, upon assembled, has been brought back to UTP. A talk and listen test has been carried out. During the test, two radios and accessories have been used. One radio was setup in the car, which was parked about 2km away from the laboratory while another radio was setup in laboratory where it is powered up by power source HP6033A (high current power source).

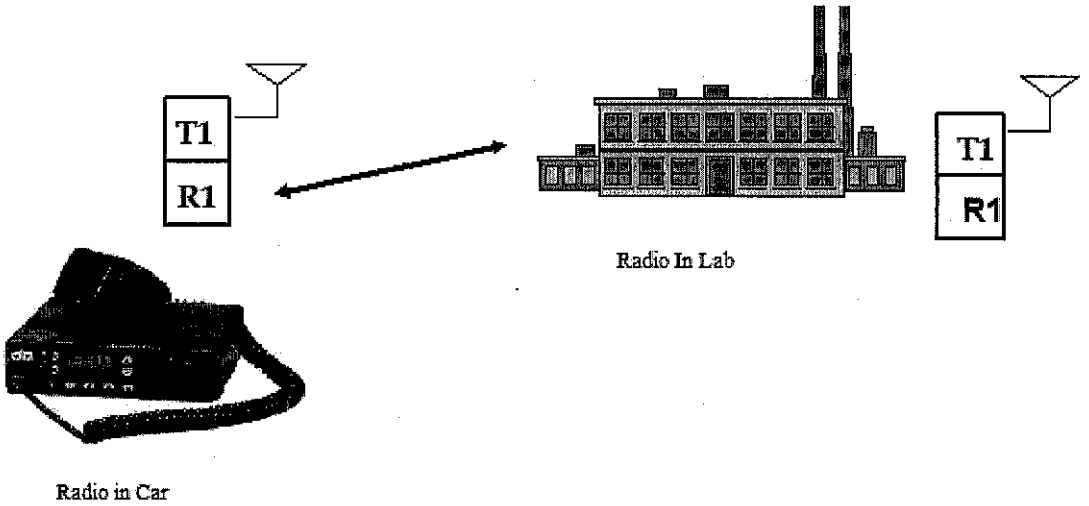


Figure 23 Talk and Listen test

The car was started and the testing was started. The personnel in the lab and car are mutually talking and listening to each other. In the test, the quality of the signal was closely monitored and evaluated. The result was a clear and distinct conversation.
After the talk and listen, the testing was further enhanced and got more interesting by setting out a set of conversation code to both parties of the speakers. Each time, the listening party should be able to figure out the code sent by speaking party. The result was all the parties could figure out the conversation code sent from the other party. It proved the conversation through the two way radio was reliable.

4.12 Load Pull Test

The radio is subjected to VSWR load of 4:1 and key up. The spectrum in the spectrum analyzer is observed at the span of 400MHz and 1GHz to investigate the presence of any spur at frequency other than the operating frequency. The reason of changing the span is to change the resolution of the spectrum and also the wideness of the spectrum. Upon a series of checking, the spectrum is seems clean as there is no spur throughout the spectrum. This means the transmitter line up is stable.

Frequency(MHz)	Existence of Spur	Comment
216	Nil	No Spur is observed except at fc level
231.5	Nil	No Spur is observed except at fc level
247	Nil	No Spur is observed except at fc level

Table 14 Load Pull Result

The load pull test shows that there is no spur seen throughout the test except the spur at harmonics level.

4.13 Linearization Study

Knowing the PA and transmitter in the line up are working in non linear region, linearization techniques can be used to characterize the non linear region as in a linear region. Several methods were identified. Feed forward, Cartesian feedback, pre-distortion and so on. The summary of each methods were done after study on each of them was performed (*see appendix E for summary*).

Out of all the techniques, pre-distortion was identified as the most feasible method with its low cost of implementation and effectiveness in linearization. Using this method, the whole PA and predistorter will be characterized as a whole. Thus, the PA will have to be characterized beforehand.

Thus far, no result was simulated as this technique is in the study and research stage. The planned action for this technique is to use MATLAB or ADS to perform the simulation on the effect of this technique to the system.

4.14 LDMOSFET MODELING STUDY

The second semester has been spent partially on the LDMOSFET Modeling study. This involved the study of the power amplifier characteristics, parameters and its significance, the modeling technique in different simulation software and ADS transistor modeling.

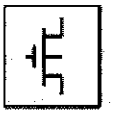
The power amplifier characteristics and relevant parameters can be obtained from the datasheet in the appendix G of this report. The parameters that are specified in it are of significance in simulating the device characteristic in simulation software. However, transferring these parameters in datasheet to a model in simulation software requires a deep understanding of the model that is in use in the software. One of the common simulation software is PSPICE. The model of transistor in PSPICE is captured and shown below.

```
---------------------------------------------------------------------
MODEL OF TRANSISTOR: PHD45N03LT/PLP-X 1 2 3
* 1=drain 2=gate 3=source
L1 1 11 3.5e-9
L2 2 22 7.5e-9
L3 3 33 7.5e-9
Cgs 6 33 1373E-12
Cgd1 6 4 2828E-12
Cgd2 11 4 140E-12
M1 5 6 33 33 MOST1
M2 4 6 5 33 MOST2
D1 33 12 Dbody
Rdiode 12 11 Rtemp 2.8e-3
Rdrain 5 11 Rtemp 7.8e-3
Rgate 22 6 15
.MODEL MOST1 NMOS (LEVEL=3 W=0.1 L=0.3e-6 Vto=1.89 Kp=6.33e-5
+                  RS=0 RD=0 UO=650 VMAX=0 XJ=0.5E-6 KAPPA=10E-2
+                  ETA=5e-5 TPG=1 IS=0 LD=0 WD=0 CGSO=0 CGDO=0
+                  CGBO=0 NFS=0.64e12 DELTA=0.1)
.MODEL MOST2 NMOS (LEVEL=3 W=0.1 L=0.3e-6 Vto=-1.65 Kp=6.33e-5
+                  RS=700 RD=700 UO=650 VMAX=0 XJ=0.5E-6 KAPPA=10E-2
+                  ETA=5e-5 TPG=1 IS=0 LD=0 WD=0 CGSO=0 CGDO=0
+                  CGBO=0 NFS=0 DELTA=0.1)
.MODEL Dbody D(Is=1e-14 N=0.8 Rs=2.7e-3 Ikf=1e3 Cjo=0 M=0.5 Vj=0.4
+                 Bv=25 Ibv=250e-6 Tt=50e-9)
.MODEL Rtemp RES(TC1=4.025e-3 TC2=1.26e-5)
.ENDS
*$
```

From there, a comparison has been made to the model with the device datasheet. However, it was found out that there is not a direct matching between the datasheet parameters with the model parameters. The relationships of them are actually represented in some equations. This does not happen in PSPICE while ADS uses the similar way to perform the modeling. To do this kind of modeling, the relationships of the parameters in datasheet need to be understood deeply in order to derive the other parameters that exist in the model. Here is one of the models that can be used in ADS to represent a transistor device. In comparison with the model that from PSPICE, it was found that the method of modeling has similarities. It can only be concluded that, to model a LDMOSFET (or other transistor), we need to know the relationship of each parameters, understand the equations that can derive the parameters that are needed in the simulation software model.

MM30_Model (Philips MOS Model 30)

Symbol



Parameters

NMOS = NMOS Model Type; YES, NO (default: YES)
PMOS = PMOS Model Type; YES, NO (default: YES)
Ron = Ohmic resistance at zero-bias, Ohm (default: 1.0)
Rsat = space charge resistance at zero-bias in Ohms (default: 1.0)
Vsat = critical drain-source voltage for hot carrier, V (default: 10.0)
Psat = velocity saturation coefficient (default: 1.0)
Vp =pinch off voltage at zero gate and substrate voltages, V (default: -1.0)
Tox = gate oxide thickness, cm (default -1.0)
Dch = doping level channel, cm-3 (default: 1.0e+15)
Dsub = doping level substrate, cm-3 (default: 1.0e+15)
Vsub = substrate diffusion voltage, V (default: 0.6)
Cgate = gate capacitance at zero-bias, F (default: 0.0)
Csub = substrate capacitance at zero-bias, F (default: 0.0)
Tausc = space charge transit time of the channel, F (default: 0.0)
Tref = reference temperature on Celsius (default: 25.0)
Vgap = bandgap voltage channel, V (default: 1.2)
Ach = temperature coefficient resistivity of the channel (default: 0.0)
Kf = flicker noise coefficient (default: 0.0)
Af =flicker noise exponent (default: 1.0)
AllParams = Data Access Component (DAC) based parameters

Figure 24 ADS MM30_MODEL for Philips MOSFET

There are some others model that can be used in ADS like Level 3, BSIM and so on. They are shown in the appendix H.

CHAPTER 5
CONCLUSION AND RECOMMENDATION

Two-way mobile radio is a half duplex device that consists of receiver, transmitter and function generating unit. Input signal is frequency modulated with carrier and travel to transmitter line up where the signal is amplified to 25W before radiated out through antenna. It serves as an important tool for communication purposes in commercial sectors like manufacturing, transportation and so on.

Transmitter line up of current existing bands of radios has been studied and 350MHz transmitter line up has been benchmarked for this project. This is decided based on several testing and research done on existing radios.

Transmitter line up of the radio has been designed with the help of ADS simulation. The transmitter line up uses 3 stage amplifications and the output of power can go up to maximum of 40W.

ADS simulation has been performed for harmonic filter and antenna switch (HF/AS), power control, coupler and transmitter line up. The simulation result has been helpful throughout the design stage as the result is accurate.

The design has been implemented and radio has been prototyped. Slight deviation has been seen compared with simulation. Optimization has been done to improve the performance of the radio.

The prototyped radio has been tested and evaluated. The result shows that the design of the transmitter line up has been a successful one because it is satisfying the specifications set by TIA.

In particular, the transmitter

- provides a 25W power with a 13.8V with a **current goal of < 6.5A** and meet the 0.25uW of radiated and conducted spur emission up to 1GHz and 2.5uW level up to 4GHz
- operates through +80 deg C to -40 deg C at operating supplies of 10.88V to 16.32V with a power leveling specification of -3dB +2dB.
- is unconditionally stable to a load mismatch of VSWR=4:1 over voltage
- does not exceed the die temperature limit and the whole system stays within the safety temperature limits when test through a 7+1 hour EIA Key down test

Recommendations

With the support from UTP lecturers and hardware, software and technical knowledge from Motorola Technology, the project has been completed. The final outcome is a radio that could function well and passing the industrial standard. The ADS simulation on matching has been performed on the output matching of PA only. In future, the whole line up will be simulated and correlated in order to ease the process of transmitter design. Linearization and LDMOSFET modeling studies will be carried on in the future to gain more knowledge about them. The eventual product of this project is a working radio. However, before the radio can be released to the market, more testing and evaluation are needed. The radio will go through radiated test to check the radiated spurious level of the signal during both transmit and receive test. This is part and parcel of the safety test for two way radio. Besides, the radio has to go through range test to check its functionality in real life. Should there be any failure in the test will lead to further optimization of the design in order to meet the stringent requirements of the users and authority.

REFERENCES

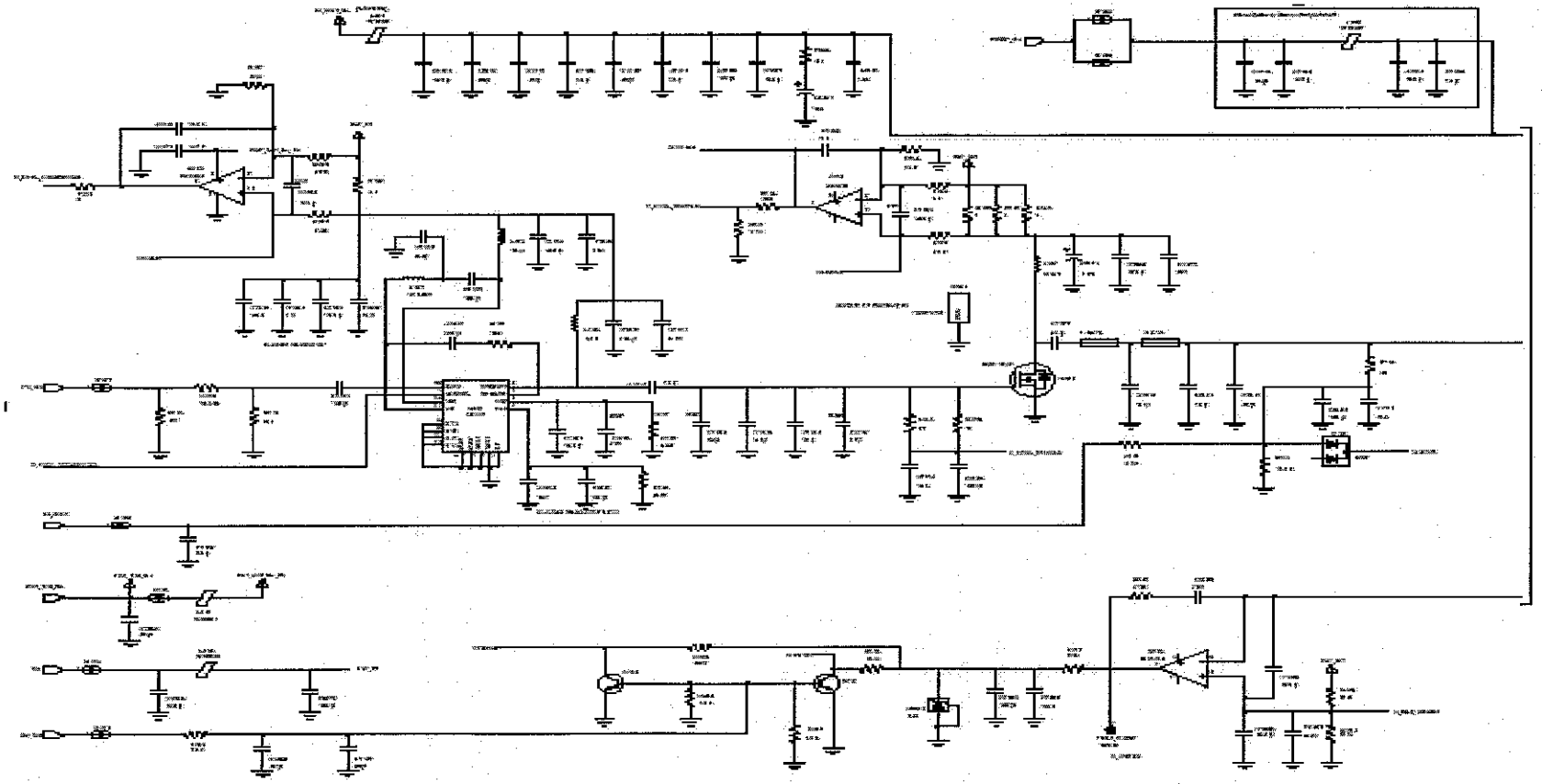
1. Chris Bowick, 'RF Circuit Design', Prentice Hall, 1st Edition, 1995, pp. 256~392
2. Reinhold Ludwig, Pavel Bretchko, 'RF Circuit Design, Theory and Application', Prentice Hall, 1st Edition, 2000, pp. 138~236
3. G.S.Kok, 'Transmitter Line Up Design Proposal', Motorola R&D Penang, August 2004
4. Kenneth R.Demarest, 'Engineering Electromagnetics', Prentice Hall, 1st Edition, 1998, pp. 132~251
5. Peter Vizmuller, 'RF Design Guide', Artech House Inc, 1st Edition, 1995, pp. 403~478
6. Tomasi, 'Electronic Communication Systems', Prentice Hall, Fifth Edition, 2003, pp. 396~512
7. Daniel Foty, 'MOSFET Modeling With SPICE: Principles and Practice', Prentice Hall, 1st Edition, 1997, pp. 34~161
8. Jeonghyeon Char, Jaehyij Yi, Jangheon Kim, and Bumman Kim, 'Optimum Design of a Predistortion RF power amplifer for multicarrier WCDMA applications', Microwave Theory and Techniques, IEEE Transactions on Volume 52, Issue 2, Feb. 2004 Page(s):655 - 663
9. In Seung Park, Edward J. Powers, GuangHan Yu, 'Parallel Adaptive Pre-distortion for RF power amplifier linearization', Global Telecommunications Conference,1997.GLOBECOM'97.,IEEE Volume 1, 3-8 Nov. 1997 Page(s):82 - 86 vol.1
10. Ruslan Ghazali , 'PA Power Control Design Training', Motorola Technology Penang Internal Documents, September 2001
11. Alfonso J.Zozaya and Eduard Bertran , 'Passivity Theory Applied to the Design of Power Amplifier Linearizers', Vehicular Technology, IEEE Transactions on Volume 53, Issue 4, July 2004 Page(s):1126 - 1137
12. D.C.Pawsey, 'A note on the design of broad band Impedance Matching Network', Circuits and Systems ,IEEE Transactions on Volume 30, Issue 1, Jan 1983 Page(s):51 – 54

13. Voyce, K.G.; McCandless, J.H.; 'Power amplifier linearization using IF feedback', Microwave Symposium Digest, 1989., IEEE MTT-S International 13-15 June 1989 Page(s):863 - 866 vol.3
14. Katz, A.; Guida, A.; Dorval, R.; Dragone, J., 'Input adaptive linearizer system', Microwave Symposium Digest., 2000 IEEE MTT-S International Volume 3, 11-16 June 2000 Page(s):1499 - 1502 vol.3
15. TIA/EIA website, http://www.tiaonline.org

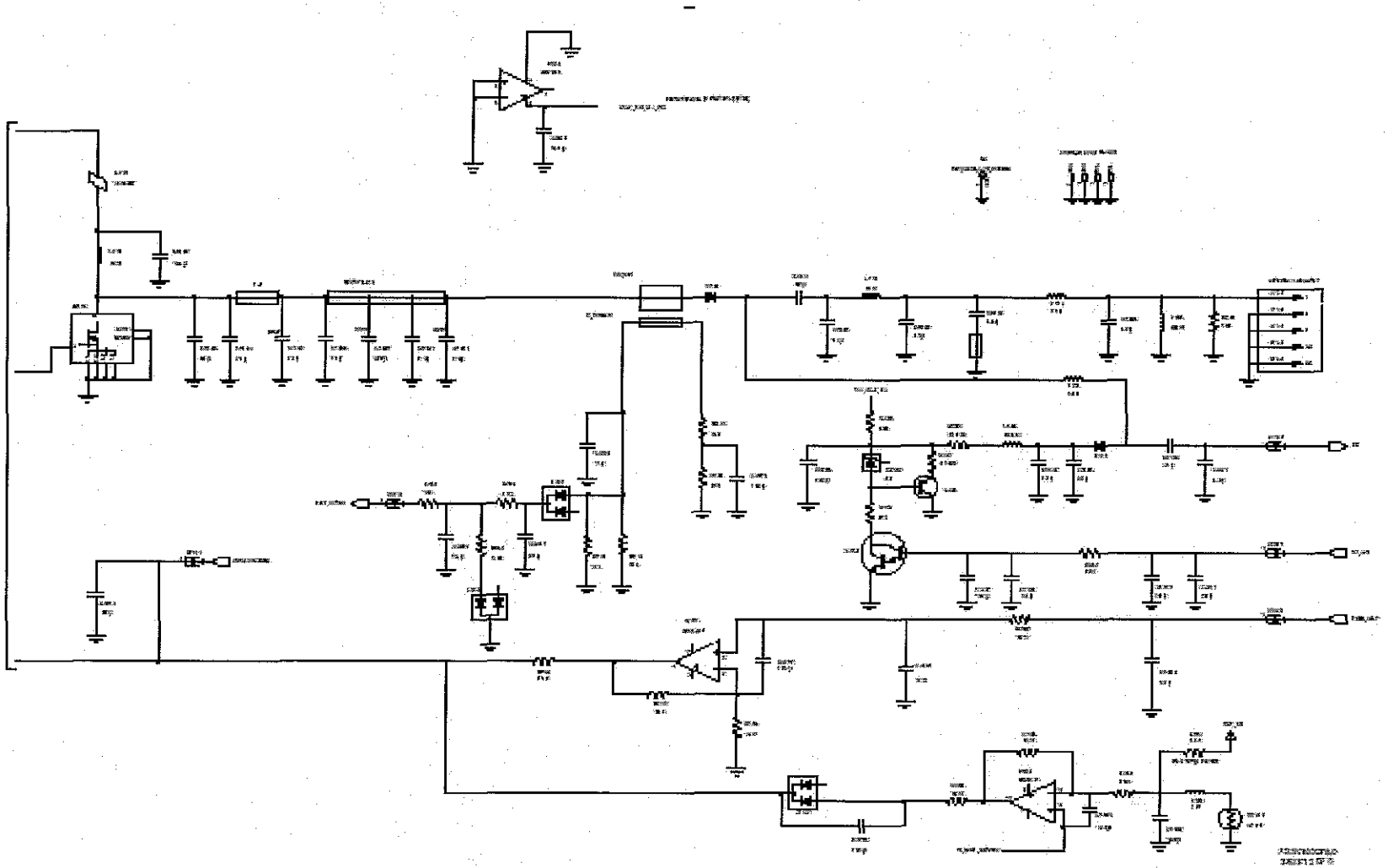
APPENDICES

APPENDIX A

TRANSMITTER SCHEMATICS



UHF1 (403-440MHz) Transmitter (Sht 1 of 2)



UHF1 (403-440MHz) Transmitter (Sht 2 of 2)

APPENDIX B

ADS SIMULATION SCHEMATICS

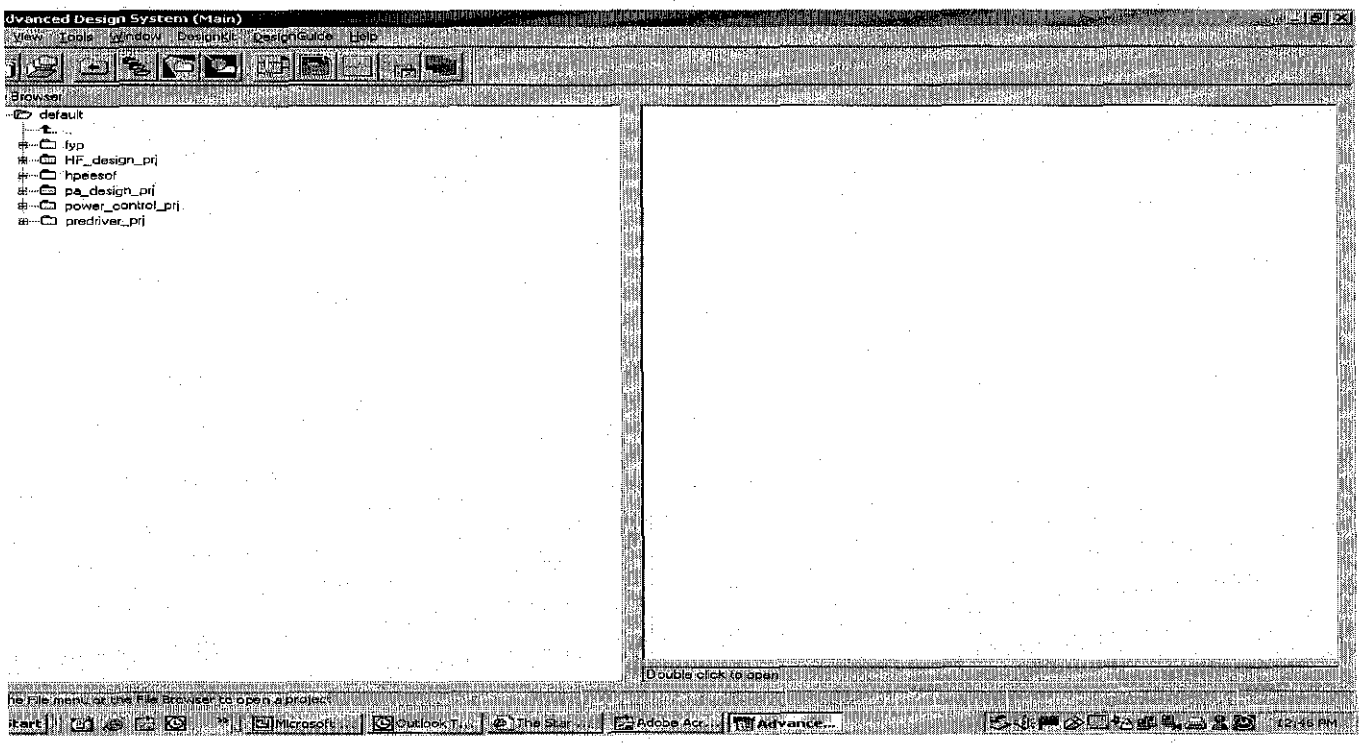


Figure: ADS starting page to choose project and schematics

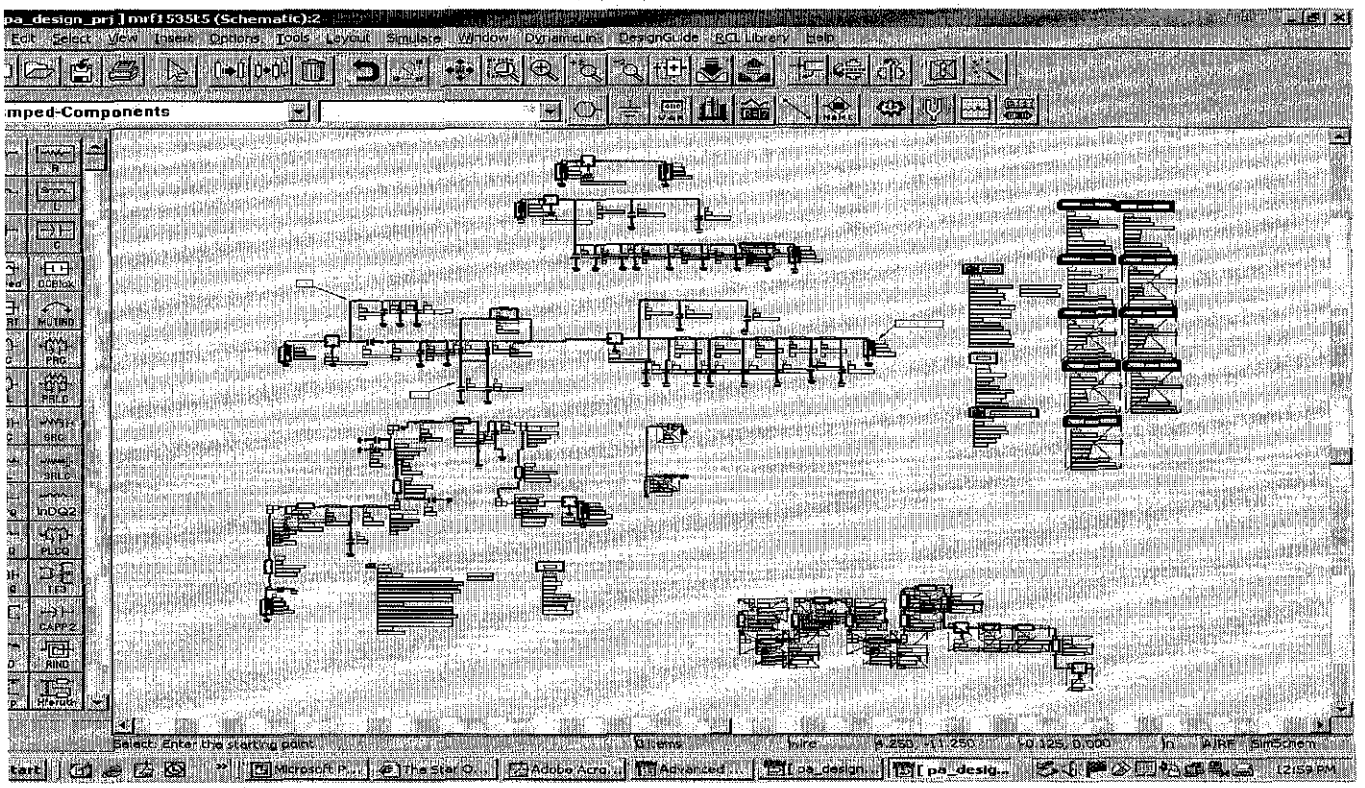
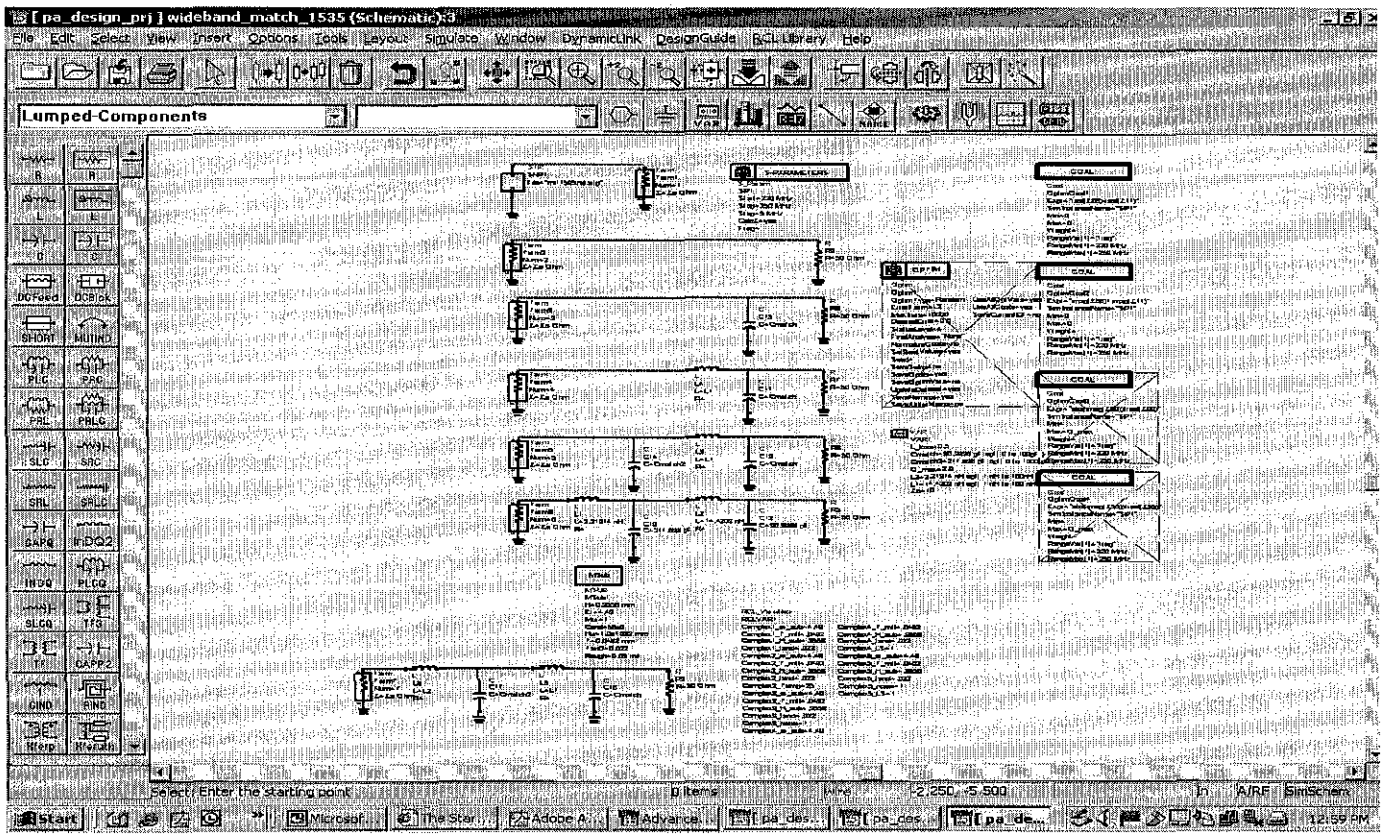
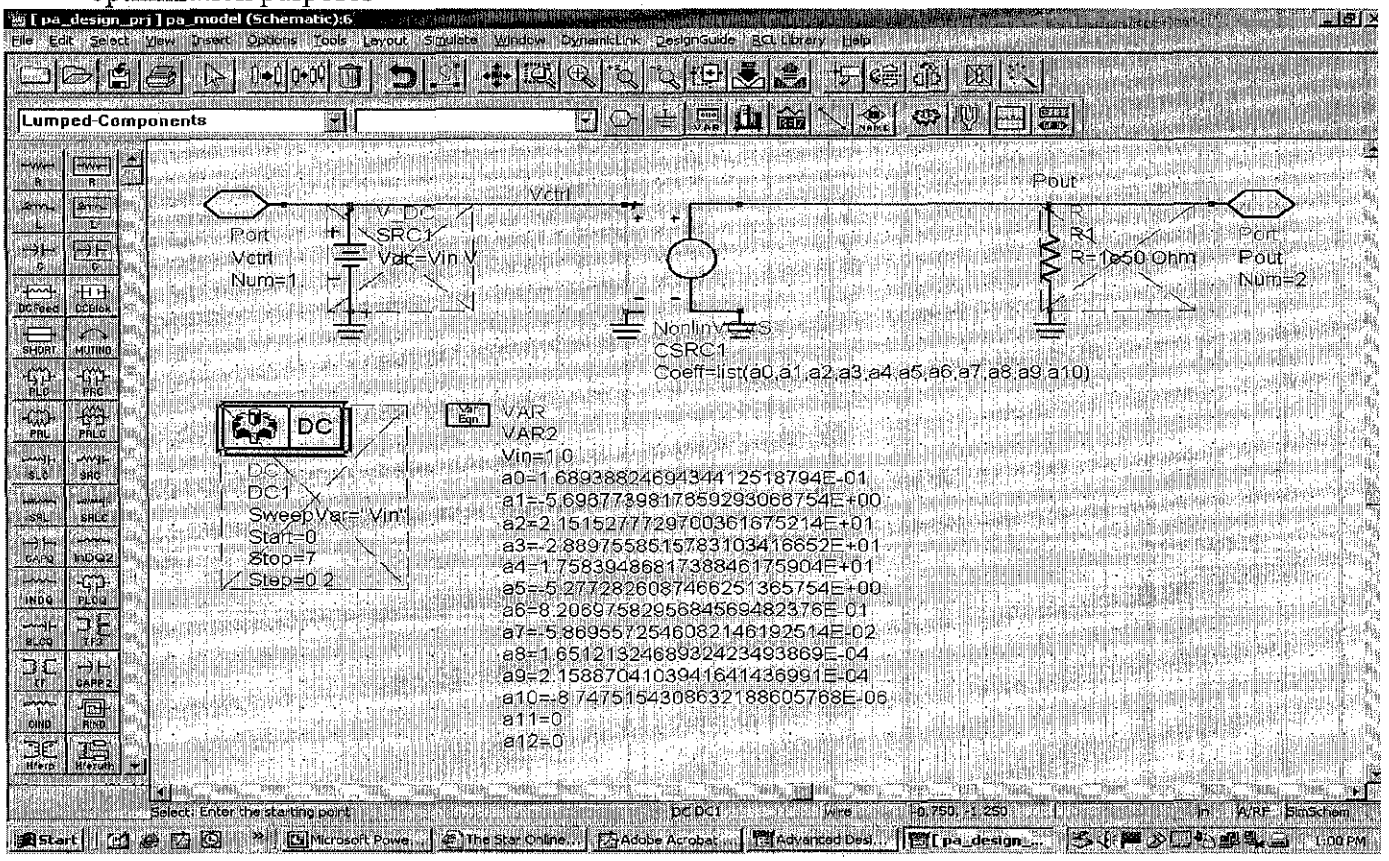


Figure shows the ADS schematic for the transmitter line up, the relevant parameters definition and goal specifications



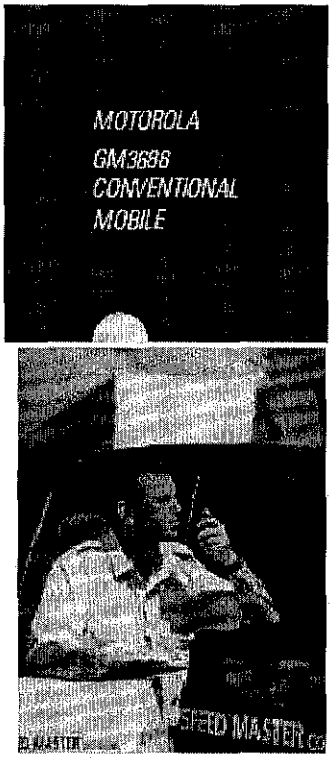
Impedance matching by stages, goals were set on the right for simulation and optimization purposes



Sub-circuit schematic drawing for amplifier for voltage control simulation

APPENDIX C

TWO WAY MOBILE RADIO BROCHURE



MOTOROLA
intelligence everywhere

Cost-Effective and Customisable Productivity Tool

Take the ruggedly-built Motorola GM3688 for a ride into the tough worlds of the Construction, Taxi, Courier and Manufacturing industries and watch it perform. Superb audio quality makes communication a breeze even in high-noise environments.

Now with a alphanumeric display and PTT ID function, callers from any of the 64 supported channels can be identified. Advanced capabilities for enhanced fleet management can be added on quickly and easily via the 16-pin external accessory port or an option board interface. In addition, a comprehensive range of accessories can be customised to suit individual users' needs, even within the same fleet. The GM3688 Conventional Mobile – made to grow with your fleets.

Features

Rugged Construction
The mobiles are built to meet or exceed the stringent Motorola ALT, MIL-STD 810C/D/E and IP54 international standards, which make them suitable for use in rough environments.

Audio Enhancement
The mobiles offer voice compression mode and powerful 4W front-firing speakers for maximal audio clarity. Optional 13w external speakers are available for high-noise environments like the construction and manufacturing industries.

64 Channels
Able to accommodate your growing business needs and communication channels.

8-character Alphanumeric Display
Large display with icons, for quick identification of radio status, and incoming calls.

16-pin External Accessory Port/Option Board Interface
Allows easy expansion of radio's capability, without messy dismantling and rewiring. Devices such as GPS module, data modem and a host of others can be added on as your business needs grow.

User Friendly
- Large ON/OFF Knob and Channel Buttons enable easy and quick operation.
- 4 Programmable Buttons provide convenient access to frequently used functions.
- LED Status Indicators and Alert Tones allow clear indication of radio's operating status and timely notification of incoming calls.

Voice Operated Transmission (VOX)
Radio may be activated by voice control when connected to a Visor microphone, thus allowing users to concentrate on road safety.

Signalling Capabilities

MDC1200

PTT ID Encode/Decode
Identifies the radio during transmission, so callers do not have to verbally identify themselves.

Selective Radio Inhibit Decode
If missing or stolen, the dispatcher or system can remotely disable the radio for greater security.

Radio Check Decode
Allow radios to be checked if it is working or operating within range.

Emergency
Provides instant help by activating the foot switch.

DTMF
- PTT ID Encode
- Selective Call Encode
- Call Alert Encode

Quick Call II
- Selective Call Encode/Decode
- Call Alert Encode/Decode

Additional Features
- Programmable Channel Spacing
- Busy Channel Lockout
- External Alarm
- Public Address Mode
- Repeater / Talkaround
- Dual Priority Scan
- Nuisance Channel Delete
- Tight / Normal Squelch
- Time Out Timer

Industrial Applications

The GM3688 can be used as a Radio Frequency (RF) pipe for integrated solutions such as Automatic Vehicle Locator Systems (AVL) and Telemetry. A host of devices can be connected via the mobile's 16-pin external port, to offer a multitude of solutions.

Automatic Vehicle Locator Systems (AVL)
Allows remote tracking of your vehicle's location using the Global Positioning System (GPS) and integrated software. This ensures a more efficient utilisation of the fleet, dynamic planning of delivery routes and estimation of arrival time, thereby resulting in better customer service and profitability. The AVL system can also be used to track vehicles carrying precious cargo and company personnel in high-risk environments.

Telemetry
Enables remote real-time monitoring of environmental conditions or equipment parameters. Together with integrated hardware and software solutions, the mobiles can be used for remote monitoring of water levels in inaccessible areas, or to track key operations / process parameters to ensure the safety of plant workers.

GM3688 Specifications*

General Specifications	VHF	UHF
Frequency	146-174MHz	403-440MHz (1-25W) 438-470MHz, 465-495MHz (25-40W)
Channel Capacity	64	
Power Output	1-25W, 25-45W(VHF), 25-40W(UHF)	
Power Supply	13.8 Vdc (11 Vdc - 16.8 Vdc) negative vehicle ground	
Channel Spacing	12.5/20/25KHz	
Frequency Stability (-30°C, + 60°C, +25°C Ref)	+/-2.5ppm	
Dimensions (H * W * L)	44mm x 169mm x 118mm	
Weight	1.01 Kg	
Operating temperature	- 30 (to + 60°C	
Sealing	Passes rain and dust testing to IP54	
Shock and Vibration	Meets MIL-STD 810-C,D&E and TIA/EIA 603	

Receiver	VHF	UHF
Sensitivity (12db Sinad)	0.35uV (12.5KHz) 0.3uV (25KHz)	
Intermodulation	65dB (12.5KHz) 75dB (25KHz)	60dB (12.5KHz) 70dB (25KHz)
Adjacent Channel Selectivity	65dB (12.5KHz) 75dB (25KHz)	60dB (12.5KHz) 70dB (25KHz)
Spurious Rejection	75dB	70dB
Rated Audio (extended audio with 4 ohm speaker)	4W internal 13W external	
Audio Distortion @ Rated Audio	3% typical	
Hum and Noise	-40 dB (12.5KHz) -45 dB (25KHz)	-35 dB (12.5KHz) -40 dB (25KHz)
Audio Response (300 to 3000Hz)	+1, -3dB	
Conducted Spurious Emission	-57 dBm < 1GHz -47dBM > 1GHz	

Transmitter	VHF	UHF
Modulation Limiting	+/-2.5KHz (12.5KHz) +/-4KHz (20KHz) +/-5KHz (25KHz)	
FM Hum & Noise	-40 dB (12.5KHz) -45 dB (25KHz)	-35 dB (12.5KHz) -40 dB (25KHz)
Conducted / Radiated Power	-36 dBm < 1GHz -30 dBm > 1GHz	-36 dBm < 1GHz -30 dBm > 1GHz
Adjacent Channel Power	-60 dB (12.5KHz) -70 dB (25KHz)	-60 dB (12.5KHz) -70 dB (25KHz)
Audio Response (300 to 3000Hz)	+1, -3dB	
Audio Distortion @ 1000Hz, 60% Rated Max. Deviation	3% typical	

* Availability subject to country's law and regulations. Specifications subject to change without notice.
All specifications shown are typical. Radios meet applicable regulatory requirements.

™ Stringent Motorola Accelerated Life Testing simulating five years of hard use in real life. EIA RS-316B in Shock, Vibration, Dust, Humidity, IP54 for Sealing.

Stamp of approval from the U.S. Military for use in rough environments.

Compliance with ISO 9001 Standard - an international quality system assurance on design, development, production, installation and servicing of a product.

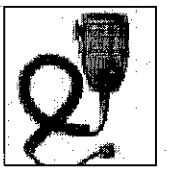
Enhance Your Radio's Capabilities

A comprehensive range of accessories is also available so that the radios can be customised to suit your needs. Adding the proper handset, speakers, microphone & mounting accessories can enhance your productivity. Motorola accessories are built with the highest quality standards and are specially engineered to assure maximum performance of your radio.

Accessories for GM3688

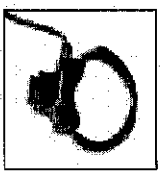
Microphone

HMN2596	Compact Palm Microphone
HMN1035	Heavy Duty Palm Microphone
RMN5029	Enhanced Keypad Microphone
AARE04517	Telephone Style Handset



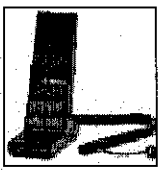
Hands-free Solution

GMMN4065	Visor Mounted Microphone (requires use of the remote PTT configuration below)
RLN4857	Pushbutton with Remote PTT
RLN4836	Remote Footswitch PTT



Desktop Solution

HMN3009	Desktop Microphone
HSN6145	7.5 W External Speaker
RSN4001	13 W External Speaker
HPN4002	Desktop Power Supply



MOTOROLA

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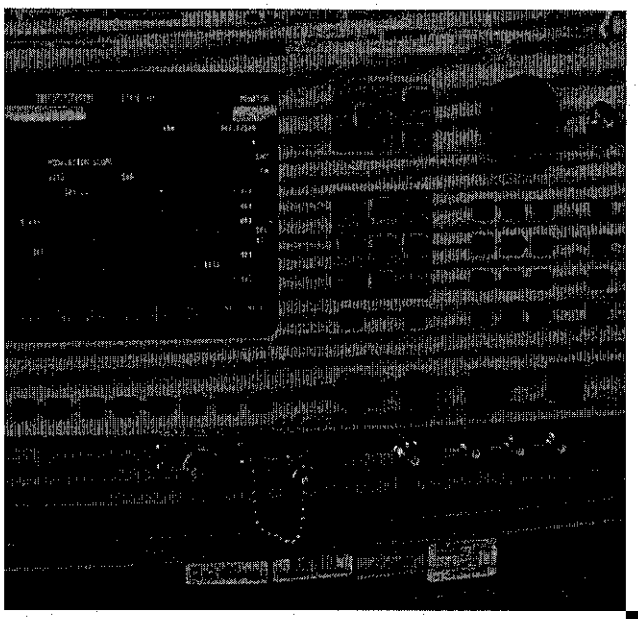
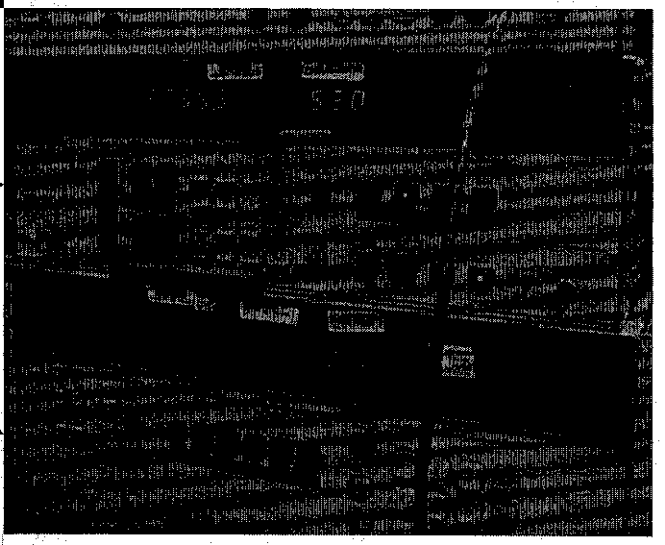
AC3-01-012

APPENDIX D

EQUIPMENT AND MATERIAL

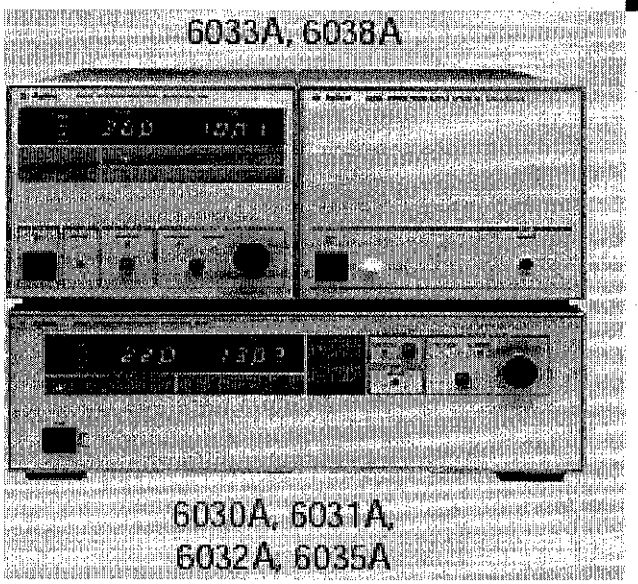


Hi end Communication Analyzer

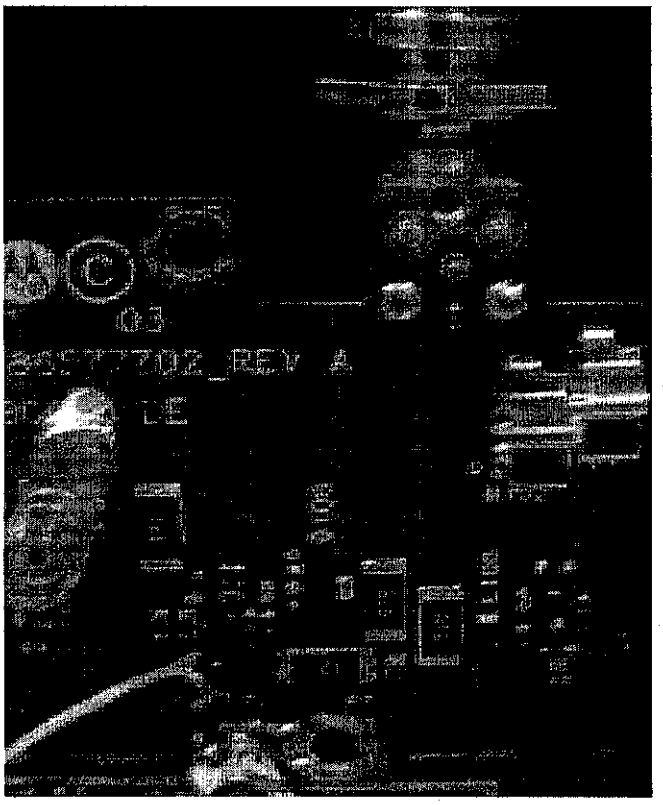


Audio Analyzer

Modulation Analyzer



High Current Power Supply



HF/AS PCB front end

HF/AS PCB back end

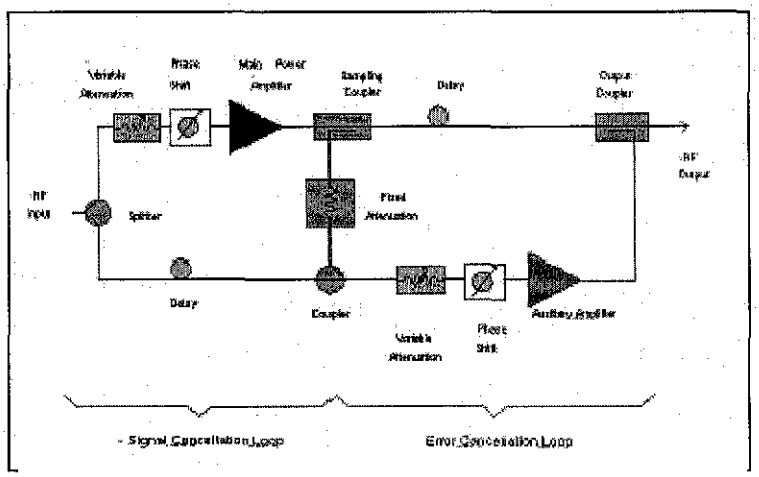
APPENDIX E

LINEARIZATION SUMMARY

Types of linearization techniques

a) Feedfoward linearization

The configuration of this technique was shown in the figure below. This method was frequently used in radio communication, mainly QAM due to the fluctuating AM envelopes. There are two main circuits in this configuration: error cancellation and signal cancellation circuit. Signal cancellation is mainly used to suppress the reference signal from the main power amplifier output signal, leaving only amplifier distortion, both linear and nonlinear in the error signal. Linear distortion is mainly caused by the deviations of the amplifier's frequency response from the flat gain and linear phase. The purpose of the error cancellation circuit is to suppress the distortion component of the PA output signal, leaving only the linearly amplified component in the linearizer output signal. In order to suppress the error signal, the gain of the error amplifier is chosen to match the sum of the values of the sampling coupler, fixed attenuator and output coupler so that the error signal is increased to approximately the same level as the distortion component of the PA output signal



b) LINC- Linear amplification using nonlinear components

This technique is used whereby a linear modulation signal is converted into two constant envelope signals that are independently amplified by power efficient class C amplifiers and then combined using a hybrid coupler. The use of power efficient amplifiers can provide significant improvement in the overall sstem. The envelope conversion operation is a non linear process that generates spectral components outside of the modulation bandwidth. Any imbalance between the

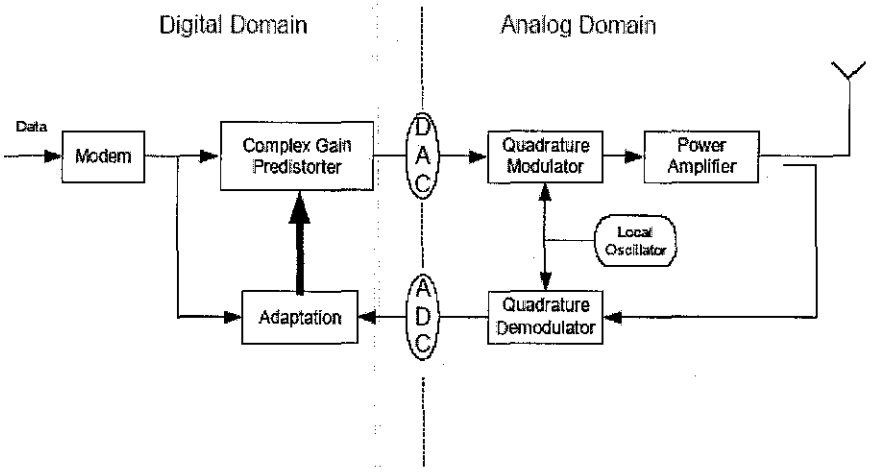
two class C amplifiers needs to be eliminated. A complex gain adjuster can be inserted into one of the branches to adaptively control the balance between the amplifiers. The adaptation process can use either the ACPR minimization approach of Gradient based correlator approach.

c) Cartesian feedback

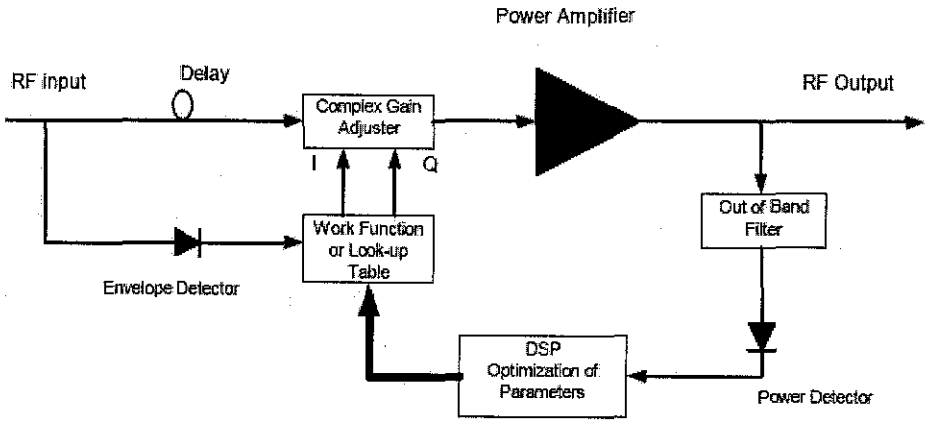
In this method, the error signal is created by subtracting the PA output from that of the input signal. The error signal is the input of the power amplifier. The limitations of the Cartesian feedback linerizer are the achievable bandwidth and system stability.

d) Digital Predistortion

Two common techniques- Vector mapping look up table approach and complex gain look up table approach Vector mapping approach stores compensation vector into a look up table for each input signal vector but it requires large amount of data storage. Complex gain look up approach provides more accurate representation of the inverse nonlinearity. The look up table is indexed by either magnitude or power.



Digital Predistortion for digital communication



Digital Predistortion for RF input

APPENDIX F

IMPEDANCE MATCHING

A Note on the Design of Broad-Band Impedance Matching Networks

D. C. PAWSEY

Abstract —Formulas are given which are intended to assist in the design of simple low-pass networks to match a resistive source to a complex load impedance when the desired type of frequency response does not coincide with one for which explicit formulas for the element values have been published to date. Third-order elliptic is one such response, and its adoption in a matching network allows some compromise to be achieved between matching and filtering performance.

The formulas are applicable to the design of matching networks whose response, when connected to the load, is of second or third-order polynomial form or, alternatively, third-order elliptic (or similar). All the networks are suitable for RC parallel (or GL series) load impedances and, in the case of the polynomial networks, for certain RLC (or GLC) loads also.

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TABLE I
FORMULAS FOR SECOND-ORDER POLYNOMIAL NETWORKS

From Fig. 1(a)	From Fig. 1(b)
$a = C_L + C_1$	$a = L_L + L_2$
$p = R_L + R_S$	$p = G_L + G_S$
$q = L_2 + (R_S R_L C_1)$	$q = C_1 + (G_S G_L L_2)$

then

$$b_1 = \frac{pa}{(1+p)a^2 - (1+q)a + q}$$

$$b_2 = b_1\left(\frac{(1+q)a - a}{a}\right)$$

Existing literature on broad-band impedance matching networks includes a comprehensive set of explicit formulas for the element values of low-pass networks possessing Butterworth or Chebychev response [1]. In addition, tables have been published giving element values for networks possessing nonalternating zeros of reflection coefficient with a variety of polynomial responses including Butterworth, Chebychev, maximally flat delay, linear phase, Gaussian and Legendre [2]. A design procedure for elliptic response networks has been presented also [3], [4], and, more recently, a method of design which is not dependent on the adoption of any analytic form of response [5].

The formulas given here supplement the above material to the extent that they allow resistively terminated LC ladders possessing either second- or third-order polynomial response or, alternatively, third-order elliptic type response, to be adapted to accept a complex load impedance comprised of a resistor R_L and capacitor C_L, in parallel (or a conductance G_L and inductor L_L, in series). As discussed by Chen under Case 1 [1], the polynomial ladder networks are able to accommodate, also, loads comprised of an inductor L_{L1} of limited value, in series with the parallel combination $R_L C_L$ (or the corresponding dual form). This point is illustrated in the first numerical example below.

The insertion characteristic of the prototype is preserved in the resulting network and a flat component of transducer loss appears, this being equal to the sum of the minimum value of the insertion loss and the mismatch loss between the terminating resistors.

In application, the $RC\omega_c$ (or $GL\omega_c$) product at one end of the chosen filter is scaled by a factor a to equal the product $R_L C_L \omega_L$ (or $G_L L_L \omega_L$) of the complex load in question. Here R, C, and ω_c represent, respectively, the values of resistor, capacitor and passband limit of the prototype filter and R_L, C_L, and ω_L, the corresponding values of the desired matching network. The formulas in Tables I, II, or III as appropriate, now give the constants, $b_1 \cdots b_i$ by which the other elements of the prototype, including the source resistance R_s (or conductance G_s), should be multiplied to preserve the insertion characteristic. For convenience, R has here been taken to equal R_L and also ω_c to equal ω_L.

As an example, it will be assumed that matching is required with a linear phase response of 0.5° equiripple phase error over the frequency range 0 to ω_L into the parallel combination $R_L C_L$ such that the product $R_L C_L \omega_L = 3.9625$. Adopting the first entry

TABLE II
FORMULAS FOR THIRD-ORDER POLYNOMIAL NETWORKS

From Fig. 2(a)	From Fig. 2(b)
$a = C_L + C_1$	$a = L_L + L_1$
$p = R_L + R_S$	$p = G_L + G_S$
$r = R_S R_L C_1 + L_2$	$r = G_S G_L L_1 + C_2$
$s = R_S R_L C_3 + L_2$	$s = G_S G_L L_3 + C_2$
$t = R_L^2 C_3 + L_2$	$t = G_L^2 L_3 + C_2$
$u = R_S C_1 + (R_L C_3) + r + t$	$u = G_S L_1 + (G_L L_3) + r + t$

where

$$b_2 = a\left(\frac{(r+s)a - 2r}{(p+1)a^3 - (1+r+s)a^2 + (1+u)a - u}\right)$$

$$b_1 = p^{-1}\left(\frac{a}{(p^{-1}+1)b_2 a^2 - (1+u)a + u}\right)$$

$$b_3 = b_1^{-1}\left(\frac{a}{(1+s)a - a}\right)$$

TABLE III
FORMULAS FOR THIRD-ORDER ELLIPTIC TYPE NETWORKS

From Fig. 3(a)	From Fig. 3(b)
$R_S = R_L = R$	$G_S = G_L = G$
$C_1 = C_3 = C$	$L_1 = L_3 = L$
$a = C_L + C$	$a = L_L + L$
$p = L_2 + (R^2 C)$	$p = C_2 + (G^2 L)$
$s = C_2 + C$.	$s = L_2 + L$

then

$$b_2 = \frac{sa \pm \sqrt{s^2 a^2 - 4vy}}{2v}$$

$$b_1 = \frac{b_2 a^2 - (1 + 0.5p) b_2 a - a + y b_2}{a b_2 a + y a_2^2 - (1 + 0.5p) b_2 + 1}$$

$$b_3 = \frac{(1 - ab_2) + 0.5p}{(a + b_2 - 1) - 0.5p}$$

where

$$v = a\left(2y^{-1}a^2 - a + (1 + 2a)\right)$$

$$w = -4y^{-1}a^2 + (1 - 2a)a - (1 + 2a)$$

$$a = 2(y^{-1}a + a)$$

lastly

$$b_3 = \frac{b_2 a - 1}{1 - b_2 b_1}$$

for third-order filters of this type given by Zverev [2], and, accordingly, taking R_L and ω_L each to be unity, requires the output capacitor, C_1, of the chosen filter to be multiplied by $a = (3.9625 \div 2.4250) = 1.63402$. The formulas of Table II then give $b_2 = 0.49963$, $b_1 = 1.8373$, and $b_3 = 0.50000$. Hence the elements of the matching network, together with load, become

$R_L = 1.0000$ load

$aC_1 = 3.9625 = C_L$ load

$b_2 L_2 = 0.5105$

$b_1 C_1 = 1.0168$

$b_3 R_s = 0.5000$.

(It will be noted that the value of a taken above allows direct comparison of results with a later entry in Zverev's tables. In

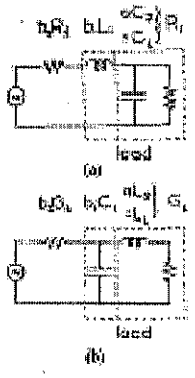


Fig. 1. Second-order polynomial networks for: (a) CR parallel (and certain LCR) loads. (b) LG series (and certain CLG) loads. Passband limit $\cdots \omega_c$ rad/s.

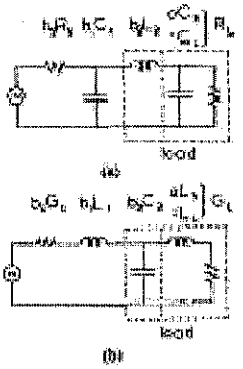


Fig. 2. Third-order polynomial networks for: (a) CR parallel (and certain LCR) loads. (b) LG series (and certain CLG) loads. Passband limit $\cdots \omega_c$ rad/s.

practice, the formulas would be used for interpolation between tabulated values.) The flat component of transducer loss is 0.512 dB.

The polynomial network above could accept, if required, an inductor L_L in series with the parallel combination $R_L C_L$ provided that $L_L \ll b_2 L_2 = 0.5105$ H (normalized value).

By comparison, a second-order network (Fig. 1) fulfilling the same linear phase and $R_L C_L \omega_c$ requirements (developed from Zverev's tables [2] using the formulas of Table I) would introduce a flat loss of 0.742 dB and accommodate, if required, a series inductor $L_L \ll 0.2951$ H.

A third-order elliptic matching network, (Fig. 3), with a passband ripple of 0.5 dB and frequency of infinite loss, ω_∞, equal to 2.27007 ω_c was obtained from Skwirzynski's designs [6] (scaled to give $\omega_c = 1$) by using the formulas of Table III. Element values for both the prototype and the resulting matching network of Fig. 3(a) are given below for a load-bandwidth factor, $R_L C_L \omega_c$, equal to 3.0.

Prototype	Matching Network
$\omega_c = 1.0000$	$\omega_c = 1.0000$
$R_L = 1.0000$	$R_L = 1.0000$
$C_1 = 1.4446$	$aC_1 = 3.0000 = C_L$
$L_2 = 0.9367$	$b_2 L_2 = 0.3010$
$C_2 = 1.4446$	$b_2 C_2 = 2.0388$
$R_1 = 1.0000$	$b_2 R_1 = 0.4517$
$L_2 C_2 = \omega_\infty^{-2} = 0.194034 = b_2 L_2 b_2^{-1} C_2$	

The insertion loss at $\omega = 2\omega_c$ is 31.2 dB and the flat component of transducer loss is 0.668 dB.

For comparison, a Chebyshev network, having the same values of passband ripple and $R_L C_L \omega_c$ product, gives an insertion loss of 19.2 dB at $\omega = 2\omega_c$ with a flat loss of 0.541 dB. (The element values for this network, obtained by applying Table II to a prototype given by Manthan [7] were found to be consistent with those evaluated from explicit formulas published previously [1], [8].)

Since the insertion characteristic remains unchanged in deriving the matching structure, the elliptic type offers a more rapid transition from pass to stopband than the corresponding polynomial network. However, this is achieved at the expense of transducer loss which increases as ω_∞ is reduced from infinity toward ω_c. (Other values of the flat component of this loss are 0.546 dB and 1.152 dB at $\omega_\infty = 11.540\ \omega_c$ and $1.203\ \omega_c$, respectively, when ripple and load are held at their previous values.) Thus for a given value of passband ripple, some "tradeoff" is available between the matching and filtering properties of the elliptic type of network derived by this method.

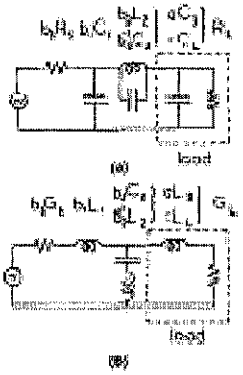


Fig. 3. Third-order elliptic type of network for: (a) CR parallel loads; (b) LG series loads. Passband limit $\cdots \omega_c$ rad/s. Point of loss at $\cdots \omega_\infty = (L_2 C_2)^{-1/2}$ rad/s.

The numerical examples above involve equiripple (phase or magnitude) behavior in the passband but any response appropriate to the configuration in question may be chosen. Thus maximally flat delay, for example, could be adopted for the polynomial networks and an inverse-Chebyshev response substituted for the elliptic type above.

Conclusion

By requiring the coefficients of the insertion ratio function to remain unchanged with variation the RC parallel (or GL series) pendant at one end of a resistively terminated low-pass LC ladder, formulas have been developed allowing the design of simple impedance matching networks incorporating second- or third-order polynomial or third-order elliptic types of frequency response.

Since any existing ladder design within the above categories is

suitable as a prototype (subject to the presence of physical symmetry in the case of the elliptic type), a variety of frequency responses is available for the matched structure.

Acknowledgment

The author is indebted to Dr. D. W. Griffin for valuable discussion and to the reviewers for their suggestions.

References

[1] W. K. Chen, "Explicit formulas for the synthesis of optimum broad-band impedance-matching networks," *IEEE Trans. Circuit Syst.*, vol. CAS-24, pp. 187–189, Apr. 1977.

[2] A. I. Zverev, *Handbook of Filter Synthesis*. New York: Wiley, 1967.

[3] W. K. Chen, "On the design of broad-band elliptic impedance-matching networks," *J. Franklin Inst.*, vol. 301, pp. 431–443, June 1976.

[4] W. K. Chen, *Theory and Design of Broad-Band Matching Networks*. Oxford: Pergamon, 1976.

[5] H. J. Carlin and P. Amstutz, "On optimum broad-band matching," *IEEE Trans. Circuits Syst.*, vol. CAS-28, pp. 401–405, May 1981.

[6] J. K. Skwirzynski, *Design Theory and Data for Electrical Filters*. London, England: Van Nostrand, 1965.

[7] G. L. Matthaei, L. Young and E. M. T. Jones, *Microwave Filters, Impedance Matching Networks and Coupling Structures*. New York: McGraw-Hill, 1964.

[8] L. Weinberg and P. Slepian, "Takahasi's results on Tchebycheff and Butterworth ladder networks," *IRE Trans. Circuit Theory*, vol. CT-7, pp. 88–101, June 1960.

APPENDIX G

DEVICE DATASHEET- MRF1535 AND MRF1518

The RF MOSFET Line

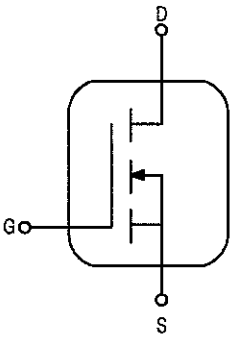
RF Power Field Effect Transistor

N–Channel Enhancement–Mode Lateral MOSFET

MRF1518T1

The MRF1518T1 is designed for broadband commercial and industrial applications with frequencies to 520 MHz. The high gain and broadband performance of this device make it ideal for large–signal, common source amplifier applications in 12.5 volt mobile FM equipment.

- Specified Performance @ 520 MHz, 12.5 Volts
  Output Power — 8 Watts
  Power Gain — 11 dB
  Efficiency — 55%
- Capable of Handling 20:1 VSWR, @ 15.5 Vdc, 520 MHz, 2 dB Overdrive
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- RF Power Plastic Surface Mount Package
- Broadband UHF/VHF Demonstration Amplifier Information Available Upon Request
- Available in Tape and Reel. T1 Suffix = 1,000 Units per 12 mm, 7 Inch Reel.



520 MHz, 8 W, 12.5 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFET

CASE 466–02, STYLE 1
(PLD–1.5)

PLASTIC

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	40	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous	I_D	4	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	62.5 0.50	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	150	°C

THERMAL CHARACTERISTICS

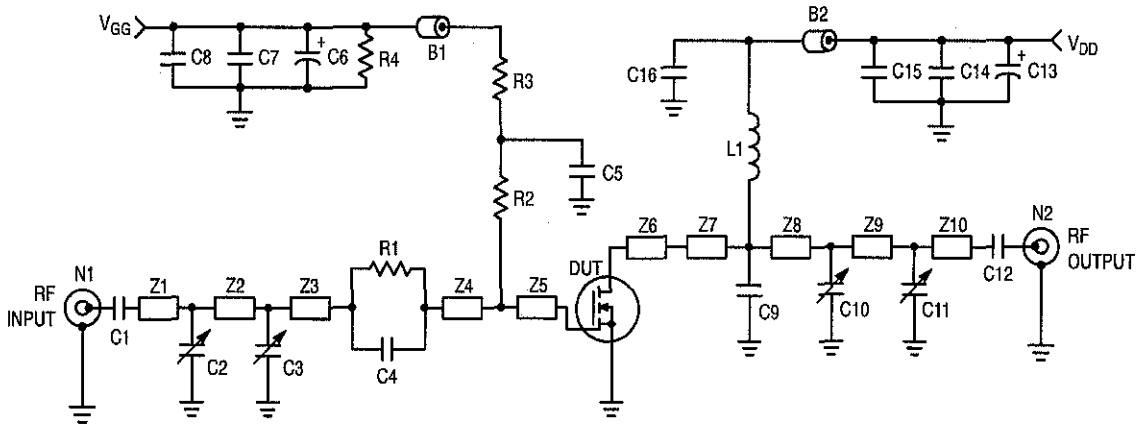
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2	°C/W

(1) Calculated based on the formula $P_D = \frac{T_J - T_C}{R_{\theta JC}}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Zero Gate Voltage Drain Current (V_{DS} = 40 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 10 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 12.5 Vdc, I_D = 100 μA)	$V_{GS(th)}$	1.0	1.6	2.1	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	0.4	—	Vdc
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	66	—	pF
Output Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	33	—	pF
Reverse Transfer Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	4.5	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain (V_{DD} = 12.5 Vdc, P_{out} = 8 Watts, I_{DQ} = 150 mA, f = 520 MHz)	G_{ps}	10	11	—	dB
Drain Efficiency (V_{DD} = 12.5 Vdc, P_{out} = 8 Watts, I_{DQ} = 150 mA, f = 520 MHz)	η	50	55	—	%



B1, B2	Short Ferrite Beads, Fair Rite Products (2743021446)	R4	33 kΩ, 1/8 W Resistor
C1, C12	240 pF, 100 mil Chip Capacitors	Z1	0.451″ x 0.080″ Microstrip
C2, C3, C10, C11	0 to 20 pF Trimmer Capacitors	Z2	1.005″ x 0.080″ Microstrip
C4	82 pF, 100 mil Chip Capacitor	Z3	0.020″ x 0.080″ Microstrip
C5, C16	120 pF, 100 mil Chip Capacitors	Z4	0.155″ x 0.080″ Microstrip
C6, C13	10 µF, 50 V Electrolytic Capacitors	Z5, Z6	0.260″ x 0.223″ Microstrip
C7, C14	1,200 pF, 100 mil Chip Capacitors	Z7	0.065″ x 0.080″ Microstrip
C8, C15	0.1 µF, 100 mil Chip Capacitors	Z8	0.266″ x 0.080″ Microstrip
C9	30 pF, 100 mil Chip Capacitor	Z9	1.113″ x 0.080″ Microstrip
L1	55.5 nH, 5 Turn, Coilcraft	Z10	0.433″ x 0.080″ Microstrip
N1, N2	Type N Flange Mounts	Board	Glass Teflon®, 31 mils, 2 oz. Copper
R1	15 Ω Chip Resistor (0805)		
R2	51 Ω, 1/2 W Resistor		
R3	10 Ω Chip Resistor (0805)		

Figure 1. 450 – 520 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 450 – 520 MHz

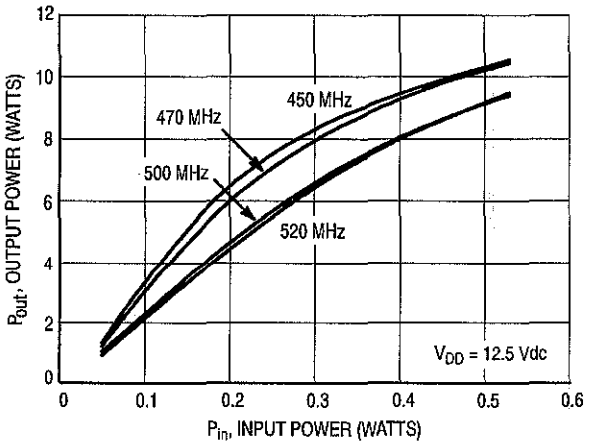


Figure 2. Output Power versus Input Power

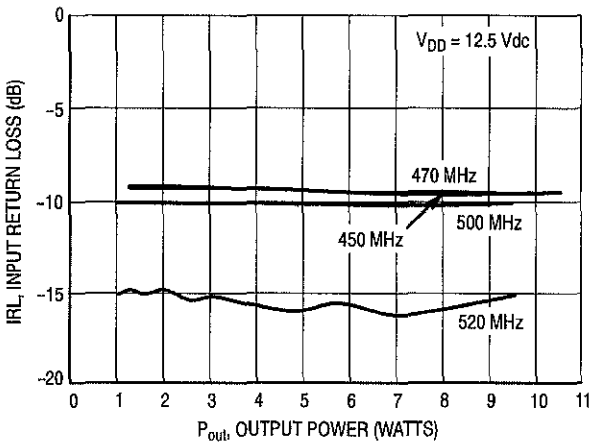


Figure 3. Input Return Loss versus Output Power

TYPICAL CHARACTERISTICS, 450 – 520 MHz

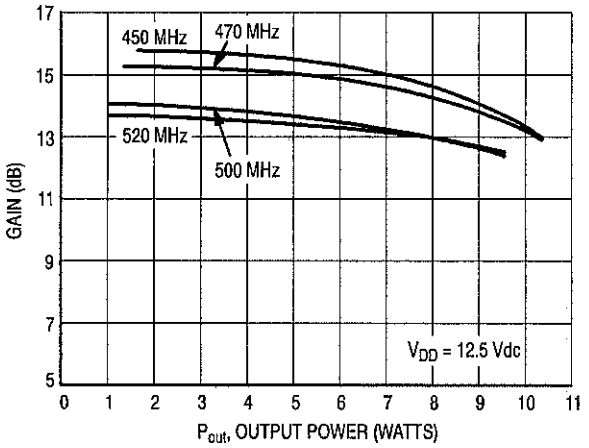


Figure 4. Gain versus Output Power

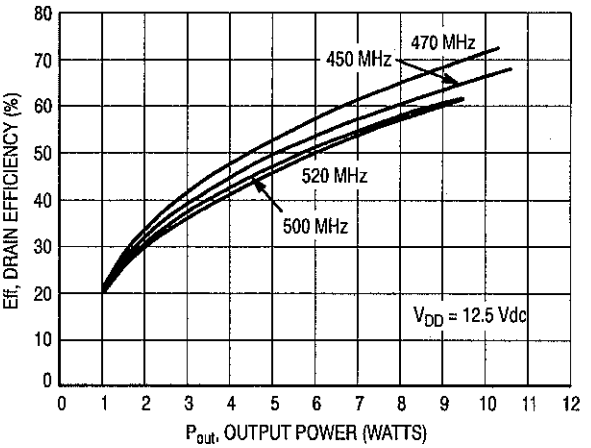


Figure 5. Drain Efficiency versus Output Power

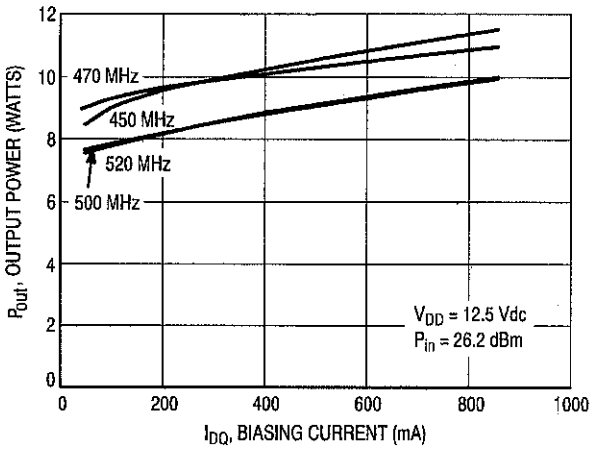


Figure 6. Output Power versus Biasing Current

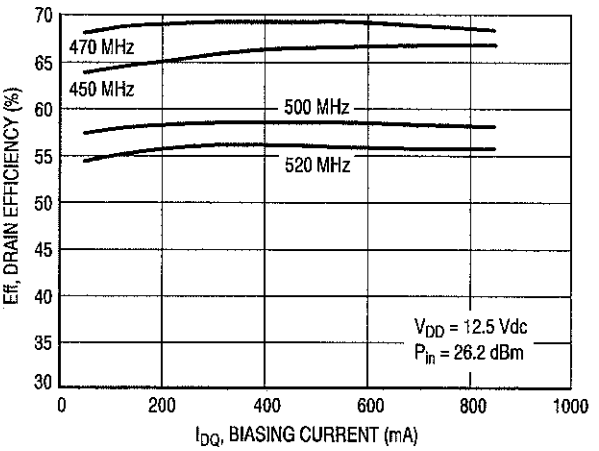


Figure 7. Drain Efficiency versus Biasing Current

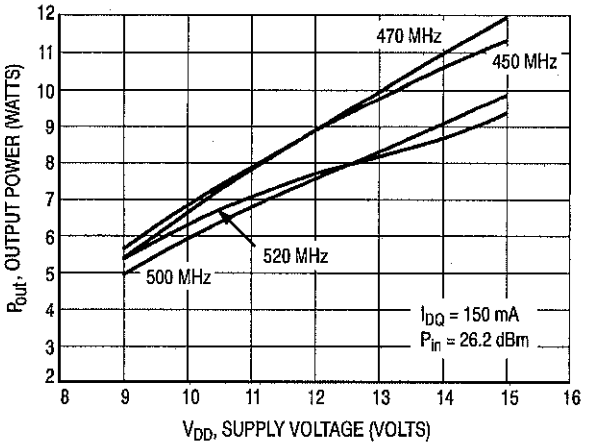


Figure 8. Output Power versus Supply Voltage

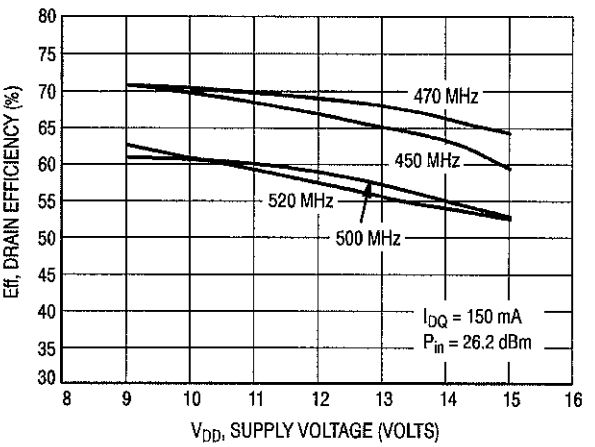
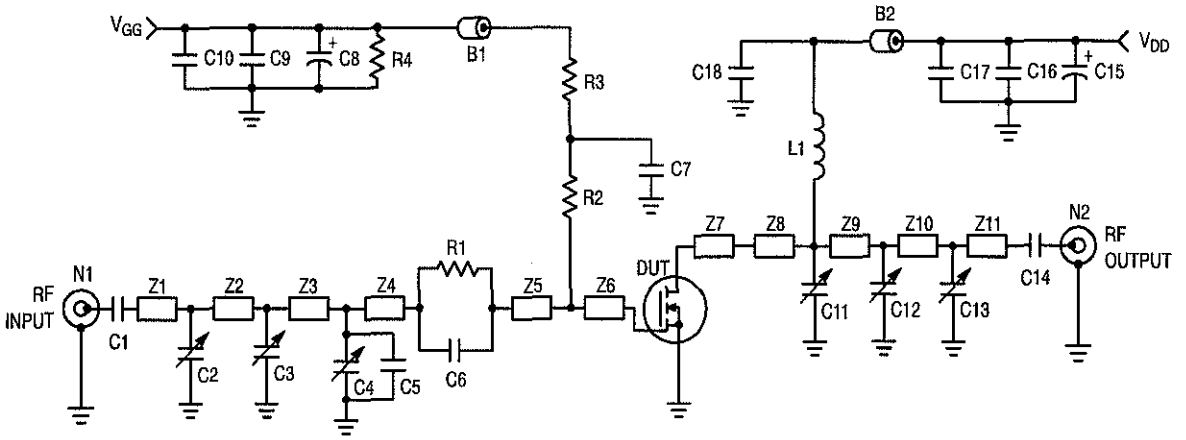


Figure 9. Drain Efficiency versus Supply Voltage



B1, B2	Short Ferrite Beads, Fair Rite Products (2743021446)	R3	10 Ω Chip Resistor (0805)
		R4	33 kΩ, 1/8 W Resistor
C1, C14	240 pF, 100 mil Chip Capacitors	Z1	0.476″ x 0.080″ Microstrip
C2, C3, C4, C11,		Z2	0.724″ x 0.080″ Microstrip
C12, C13	0 to 20 pF Trimmer Capacitors	Z3	0.348″ x 0.080″ Microstrip
C5	30 pF, 100 mil Chip Capacitor	Z4	0.048″ x 0.080″ Microstrip
C6	47 pF, 100 mil Chip Capacitor	Z5	0.175″ x 0.080″ Microstrip
C7, C18	120 pF, 100 mil Chip Capacitors	Z6, Z7	0.260″ x 0.223″ Microstrip
C8, C15	10 µF, 50 V Electrolytic Capacitors	Z8	0.239″ x 0.080″ Microstrip
C9, C16	1,200 pF, 100 mil Chip Capacitors	Z9	0.286″ x 0.080″ Microstrip
C10, C17	0.1 µF, 100 mil Chip Capacitors	Z10	0.806″ x 0.080″ Microstrip
L1	55.5 nH, 5 Turn, Coilcraft	Z11	0.553″ x 0.080″ Microstrip
N1, N2	Type N Flange Mounts	Board	Glass Teflon®, 31 mils, 2 oz. Copper
R1	15 Ω Chip Resistor (0805)		
R2	51 Ω, 1/2 W Resistor		

Figure 10. 400 – 470 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 400 – 470 MHz

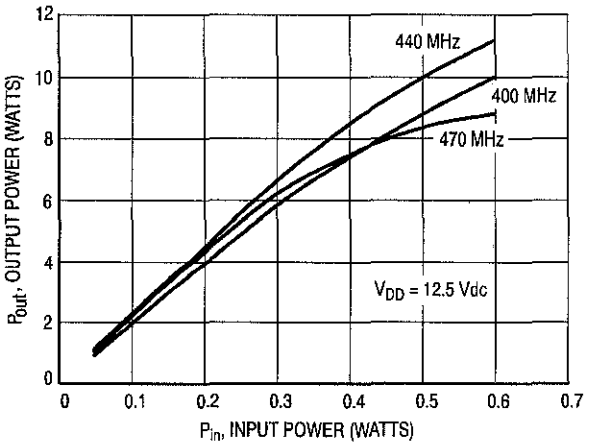


Figure 11. Output Power versus Input Power

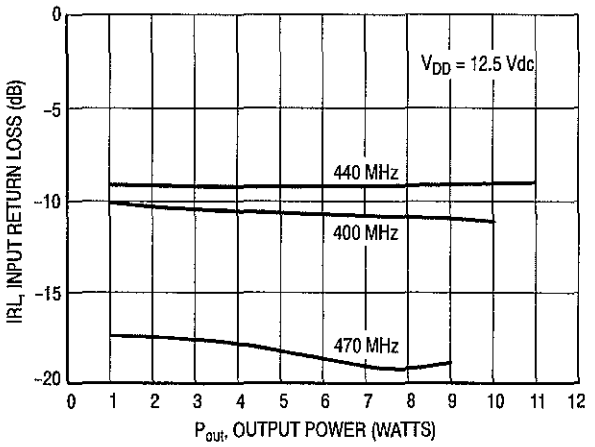


Figure 12. Input Return Loss versus Output Power

TYPICAL CHARACTERISTICS, 400 – 470 MHz

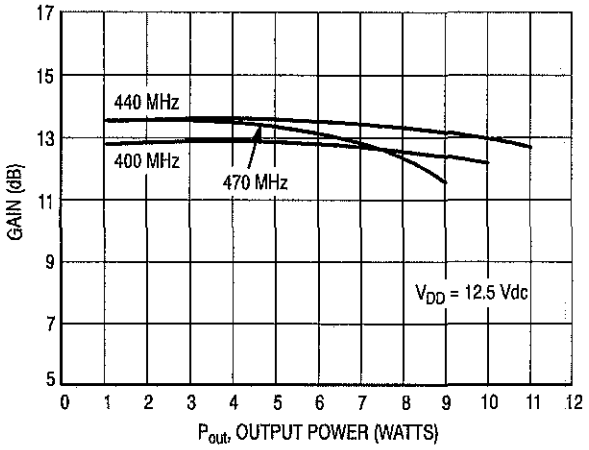


Figure 13. Gain versus Output Power

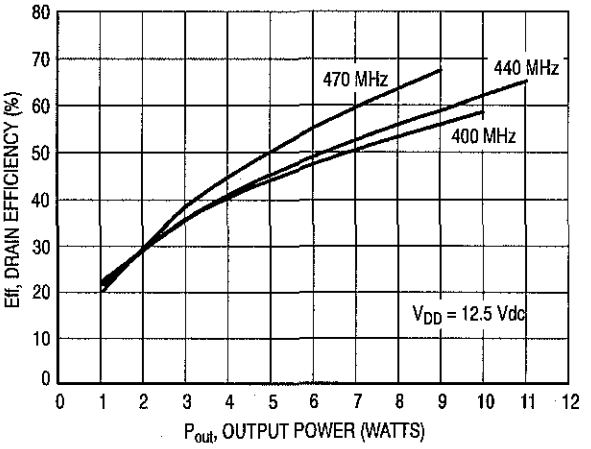


Figure 14. Drain Efficiency versus Output Power

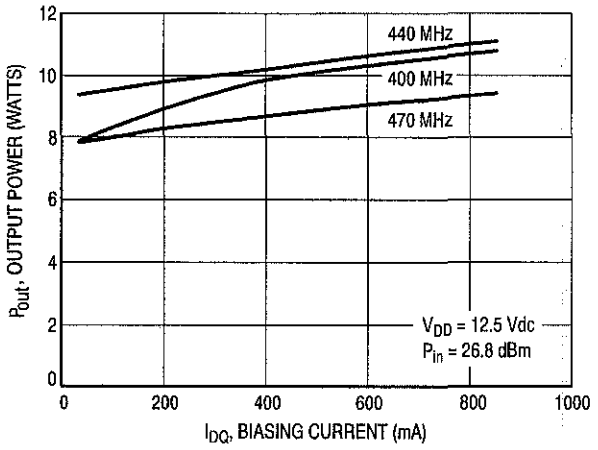


Figure 15. Output Power versus Biasing Current

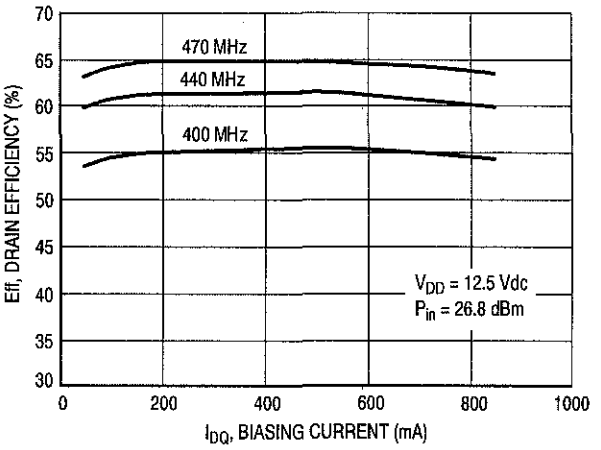


Figure 16. Drain Efficiency versus Biasing Current

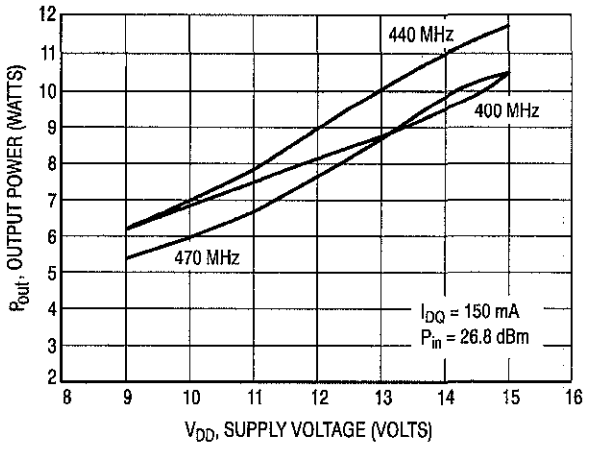


Figure 17. Output Power versus Supply Voltage

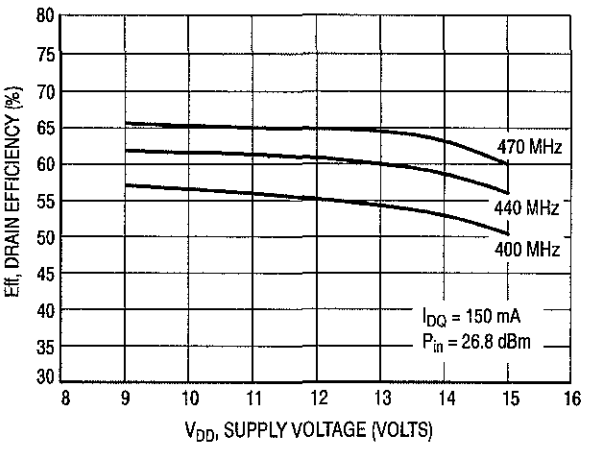
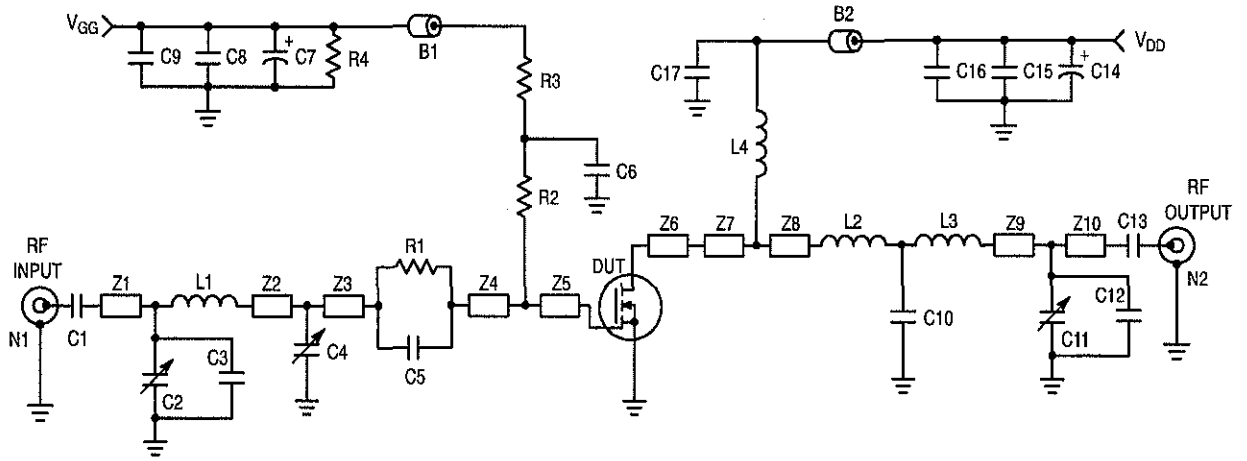


Figure 18. Drain Efficiency versus Supply Voltage



B1, B2	Short Ferrite Beads, Fair Rite Products (2743021446)	L4	55.5 nH, 5 Turn, Coilcraft
C1, C13	330 pF, 100 mil Chip Capacitors	N1, N2	Type N Flange Mounts
C2, C4, C11	0 to 20 pF Trimmer Capacitors	R1	15 Ω Chip Resistor (0805)
C3	12 pF, 100 mil Chip Capacitor	R2	56 Ω, 1/4 W Carbon Resistor
C5	43 pF, 100 mil Chip Capacitor	R3	100 Ω Chip Resistor (0805)
C6, C17	75 pF, 100 mil Chip Capacitors	R4	33 kΩ, 1/8 W Carbon Resistor
C7, C14	10 µF, 50 V Electrolytic Capacitors	Z1	0.115″ x 0.080″ Microstrip
C8, C15	1,200 pF, 100 mil Chip Capacitors	Z2	0.255″ x 0.080″ Microstrip
C9, C16	0.1 µF, 100 mil Chip Capacitors	Z3	1.037″ x 0.080″ Microstrip
C10	75 pF, 100 mil Chip Capacitor	Z4	0.192″ x 0.080″ Microstrip
C12	13 pF, 100 mil Chip Capacitor	Z5, Z6	0.260″ x 0.223″ Microstrip
L1	26 nH, 4 Turn, Coilcraft	Z7	0.125″ x 0.080″ Microstrip
L2	5 nH, 2 Turn, Coilcraft	Z8	0.962″ x 0.080″ Microstrip
L3	33 nH, 5 Turn, Coilcraft	Z9	0.305″ x 0.080″ Microstrip
		Z10	0.155″ x 0.080″ Microstrip
		Board	Glass Teflon®, 31 mils, 2 oz. Copper

Figure 19. 135 – 175 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 135 – 175 MHz

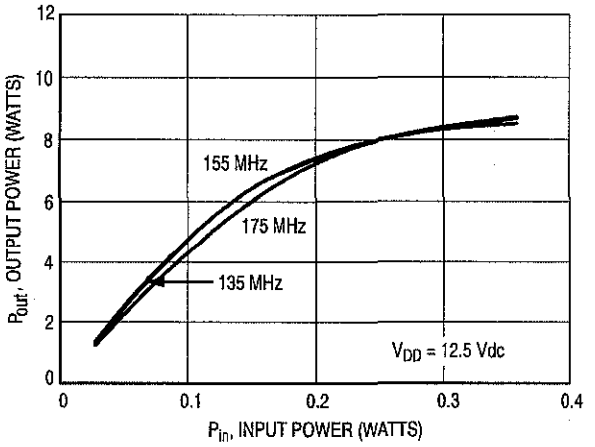


Figure 20. Output Power versus Input Power

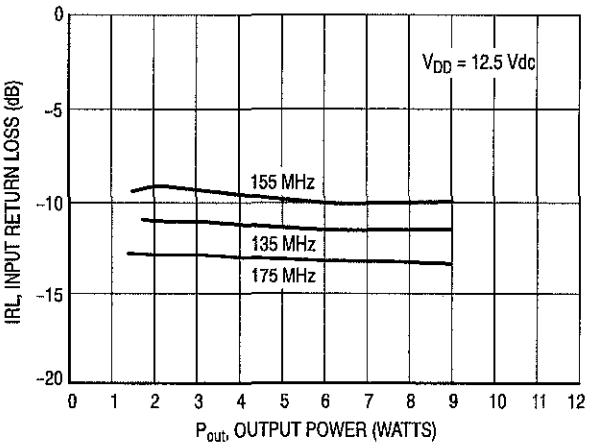


Figure 21. Input Return Loss versus Output Power

TYPICAL CHARACTERISTICS, 135 – 175 MHz

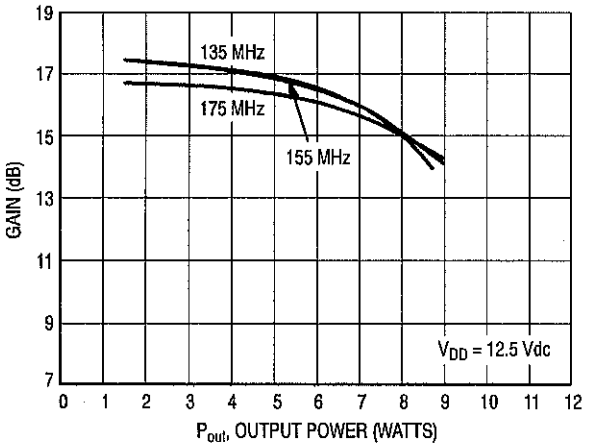


Figure 22. Gain versus Output Power

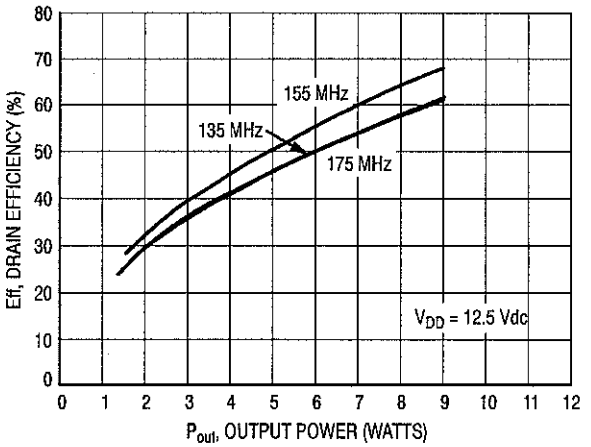


Figure 23. Drain Efficiency versus Output Power

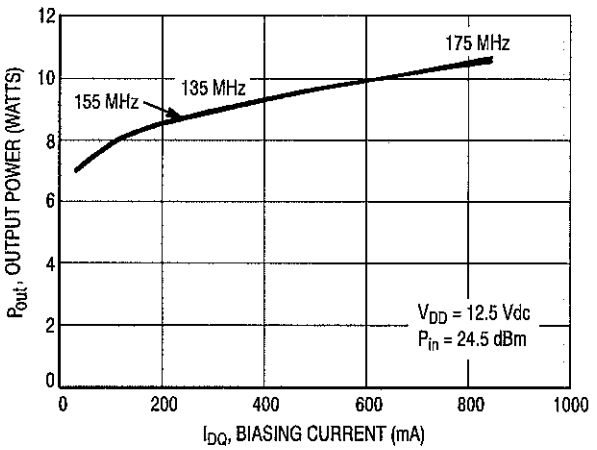


Figure 24. Output Power versus Biasing Current

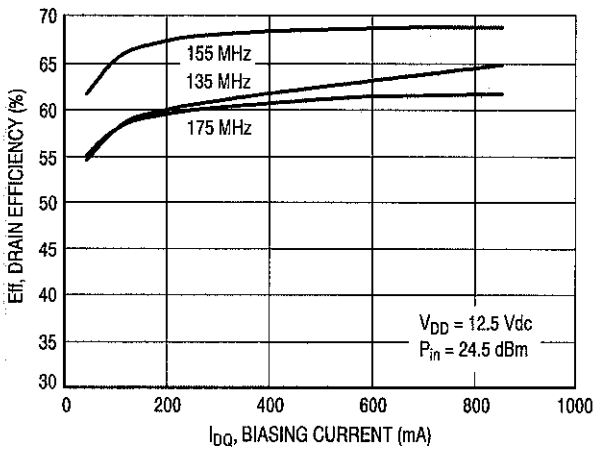


Figure 25. Drain Efficiency versus Biasing Current

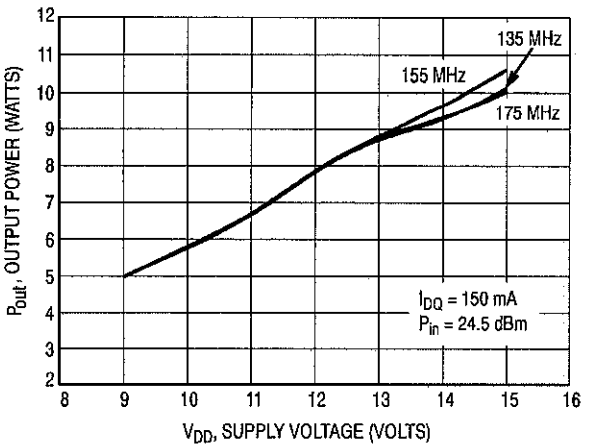


Figure 26. Output Power versus Supply Voltage

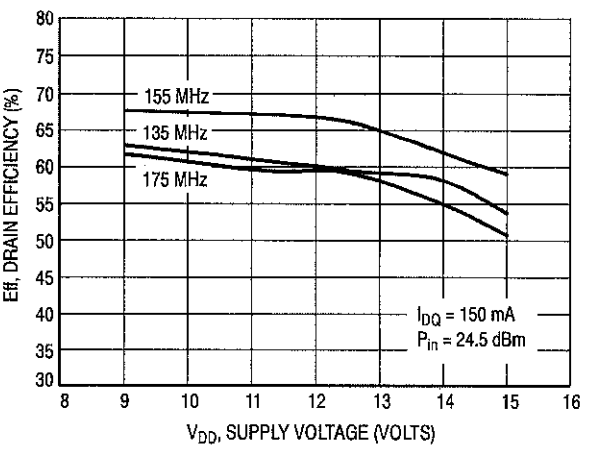
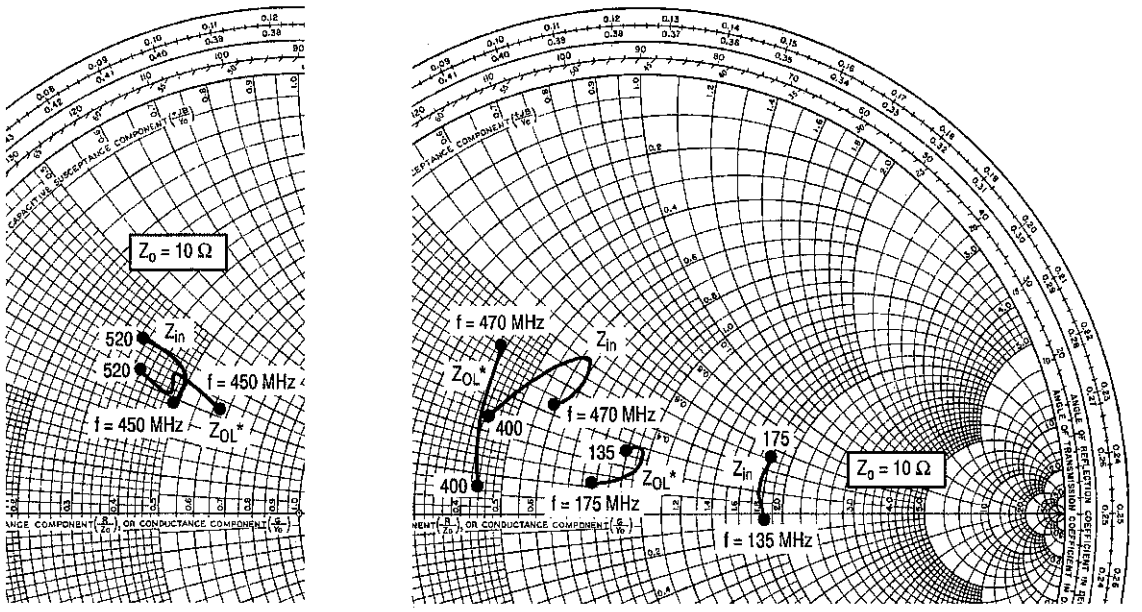


Figure 27. Drain Efficiency versus Supply Voltage



V_{DD} = 12.5 V, I_{DQ} = 150 mA, P_{out} = 8 W

f MHz	Z_{in} Ω	Z_{OL}* Ω
450	4.9 +j2.85	6.42 +j3.23
470	4.85 +j3.71	4.59 +j3.61
500	4.63 +j3.84	4.72 +j3.12
520	3.52 +j3.92	3.81 +j3.27

Z_{in} = Complex conjugate of source impedance with parallel 15 Ω resistor and 82 pF capacitor in series with gate. (See Figure 1).

Z_{OL}* = Complex conjugate of the load impedance at given output power, voltage, frequency, and η_D > 50 %.

V_{DD} = 12.5 V, I_{DQ} = 150 mA, P_{out} = 8 W

f MHz	Z_{in} Ω	Z_{OL}* Ω
400	4.28 +j2.36	4.41 +j0.67
440	6.45 +j5.13	4.14 +j2.53
470	5.91 +j3.34	3.92 +j4.02

Z_{in} = Complex conjugate of source impedance with parallel 15 Ω resistor and 47 pF capacitor in series with gate. (See Figure 10).

Z_{OL}* = Complex conjugate of the load impedance at given output power, voltage, frequency, and η_D > 50 %.

V_{DD} = 12.5 V, I_{DQ} = 150 mA, P_{out} = 8 W

f MHz	Z_{in} Ω	Z_{OL}* Ω
135	18.31 –j0.76	8.97 +j2.62
155	17.72 +j1.85	9.69 +j2.81
175	18.06 +j5.23	7.94 +j1.14

Z_{in} = Complex conjugate of source impedance with parallel 15 Ω resistor and 43 pF capacitor in series with gate. (See Figure 19).

Z_{OL}* = Complex conjugate of the load impedance at given output power, voltage, frequency, and η_D > 50 %.

Note: Z_{OL}* was chosen based on tradeoffs between gain, drain efficiency, and device stability.

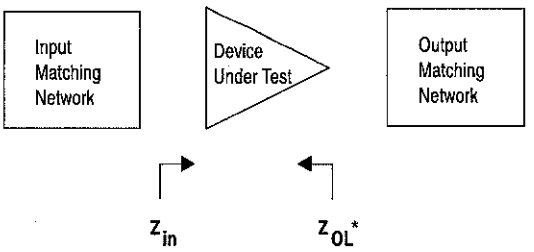


Figure 28. Series Equivalent Input and Output Impedance

Table 1. Common Source Scattering Parameters (V_{DD} = 12.5 Vdc)

I_{DQ} = 150 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
50	0.88	−148	18.91	99	0.033	11	0.67	−144
100	0.85	−163	9.40	86	0.033	−6	0.66	−158
200	0.85	−170	4.47	73	0.026	−17	0.69	−162
300	0.87	−171	2.72	64	0.025	−28	0.74	−163
400	0.88	−172	1.85	56	0.021	−21	0.79	−164
500	0.90	−173	1.35	52	0.019	−30	0.83	−165
600	0.92	−173	1.04	47	0.014	−26	0.85	−167
700	0.93	−174	0.83	44	0.015	−39	0.88	−168
800	0.94	−175	0.68	39	0.014	−31	0.90	−169
900	0.94	−175	0.55	36	0.010	−41	0.91	−170
1000	0.96	−176	0.46	30	0.011	−38	0.95	−170

I_{DQ} = 800 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
50	0.90	−159	20.80	97	0.020	14	0.73	−162
100	0.88	−169	10.35	88	0.018	1	0.74	−169
200	0.88	−174	5.09	79	0.017	−9	0.75	−171
300	0.89	−175	3.23	73	0.015	−18	0.77	−171
400	0.89	−175	2.30	67	0.015	−17	0.80	−171
500	0.90	−176	1.74	63	0.014	−22	0.82	−170
600	0.91	−176	1.39	59	0.014	−19	0.83	−171
700	0.92	−176	1.16	55	0.009	−23	0.85	−171
800	0.93	−176	0.96	50	0.011	−14	0.87	−172
900	0.94	−177	0.80	46	0.007	4	0.88	−173
1000	0.94	−177	0.67	41	0.010	−15	0.89	−173

I_{DQ} = 1.5 A

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
50	0.91	−159	20.18	97	0.015	11	0.73	−165
100	0.89	−169	10.05	89	0.016	−5	0.74	−171
200	0.88	−174	4.93	80	0.015	−3	0.75	−172
300	0.89	−175	3.14	73	0.014	−14	0.78	−172
400	0.89	−176	2.24	67	0.014	−20	0.80	−171
500	0.90	−176	1.70	64	0.014	−22	0.82	−170
600	0.92	−176	1.36	59	0.010	−16	0.84	−171
700	0.92	−176	1.13	55	0.013	−10	0.85	−171
800	0.93	−177	0.94	50	0.008	−13	0.87	−172
900	0.94	−177	0.78	46	0.013	−26	0.87	−173
1000	0.94	−178	0.65	41	0.007	8	0.87	−172

APPLICATIONS INFORMATION

DESIGN CONSIDERATIONS

This device is a common–source, RF power, N–Channel enhancement mode, Lateral Metal–Oxide Semiconductor Field–Effect Transistor (MOSFET). Motorola Application Note AN211A, "FETs in Theory and Practice", is suggested reading for those not familiar with the construction and characteristics of FETs.

This surface mount packaged device was designed primarily for VHF and UHF portable power amplifier applications. Manufacturability is improved by utilizing the tape and reel capability for fully automated pick and placement of parts. However, care should be taken in the design process to insure proper heat sinking of the device.

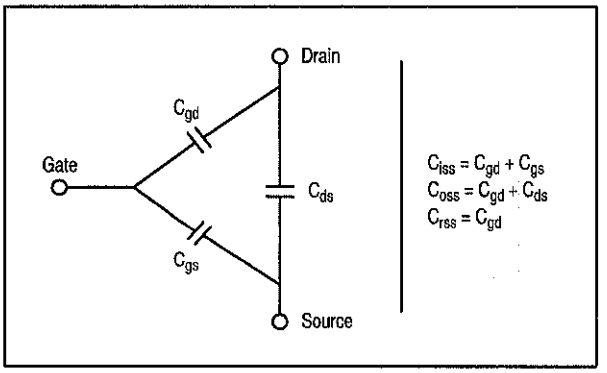
The major advantages of Lateral RF power MOSFETs include high gain, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage.

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain–to–source (C_{ds}). These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case, the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



DRAIN CHARACTERISTICS

One critical figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $R_{DS(on)}$, occurs in the linear region of the output characteristic and is specified at a specific gate–source voltage and drain current. The drain–source voltage under these conditions is termed $V_{DS(on)}$. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

BV_{DSS} values for this device are higher than normally required for typical applications. Measurement of BV_{DSS} is not recommended and may result in possible damage to the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The DC input resistance is very high – on the order of 10^9 Ω — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended. Using a resistor to keep the gate–to–source impedance low also helps dampen transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate–threshold voltage and turn the device on.

DC BIAS

Since this device is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. RF power FETs operate optimally with a quiescent drain current (I_{DQ}), whose value is application dependent. This device was characterized at I_{DQ} = 150 mA, which is the suggested value of bias current for typical applications. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of this device may be controlled to some degree with a low power dc control signal applied to the gate, thus facilitating applications such as manual gain control, ALC/AGC and modulation systems. This characteristic is very dependent on frequency and load line.

MOUNTING

The specified maximum thermal resistance of 2°C/W assumes a majority of the 0.065″ x 0.180″ source contact on the back side of the package is in good contact with an appropriate heat sink. As with all RF power devices, the goal of the thermal design should be to minimize the temperature at the back side of the package. Refer to Motorola Application Note AN4005/D, "Thermal Management and Mounting Method for the PLD–1.5 RF Power Surface Mount Package," and Engineering Bulletin EB209/D, "Mounting Method for RF Power Leadless Surface Mount Transistor" for additional information.

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for this device. For examples see Motorola Application Note AN721, "Impedance Matching Networks Applied to RF Power Transistors." Large–signal impedances are provided, and will yield a good first pass approximation.

Since RF power MOSFETs are triode devices, they are not unilateral. This coupled with the very high gain of this device yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. The RF test fixture implements a parallel resistor and capacitor in series with the gate, and has a load line selected for a higher efficiency, lower gain, and more stable operating region.

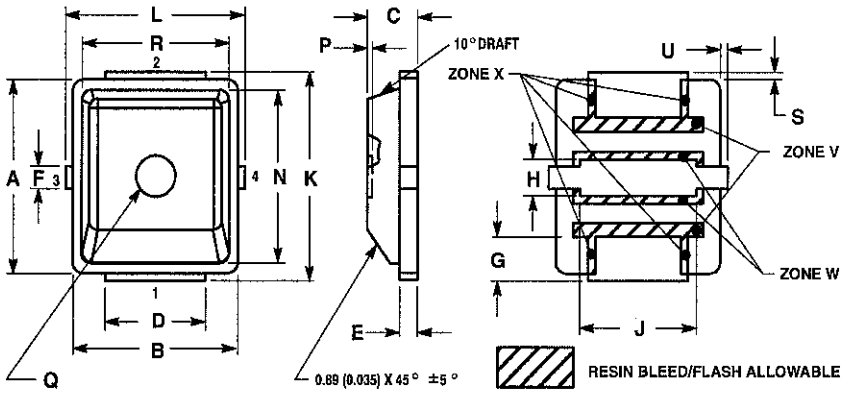
Two–port stability analysis with this device's S–parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A, "RF Small–Signal Design Using Two–Port Parameters" for a discussion of two port network theory and stability.

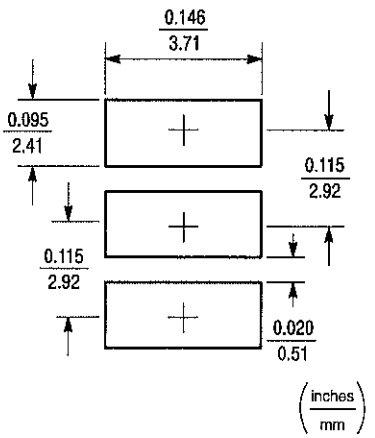
NOTES

NOTES

NOTES

PACKAGE DIMENSIONS





SOLDER FOOTPRINT

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.255	0.265	6.48	6.73
B	0.225	0.235	5.72	5.97
C	0.065	0.072	1.65	1.83
D	0.130	0.150	3.30	3.81
E	0.021	0.026	0.53	0.66
F	0.026	0.044	0.66	1.12
G	0.050	0.070	1.27	1.78
H	0.045	0.063	1.14	1.60
J	0.160	0.180	4.06	4.57
K	0.273	0.285	6.93	7.24
L	0.245	0.255	6.22	6.48
N	0.230	0.240	5.84	6.10
P	0.000	0.008	0.00	0.20
Q	0.055	0.063	1.40	1.60
R	0.200	0.210	5.08	5.33
S	0.006	0.012	0.15	0.31
U	0.006	0.012	0.15	0.31
ZONE V	0.000	0.021	0.00	0.53
ZONE W	0.000	0.010	0.00	0.25
ZONE X	0.000	0.010	0.00	0.25

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. SOURCE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH
3. RESIN BLEED/FLASH ALLOWABLE IN ZONE V, W, AND X.

CASE 466–02
ISSUE B
(PLD–1.5)

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  450–520 MHz
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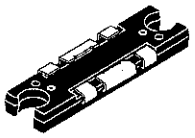
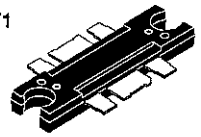


CASE 1264–08, STYLE 1
TO–272
PLASTIC
MRF1535T1



CASE 1264A–02, STYLE 1
TO–272 STRAIGHT LEAD
PLASTIC
MRF1535FT1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	40	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous	I_D	6	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	135 0.50	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	175	°C

THERMAL CHARACTERISTICS

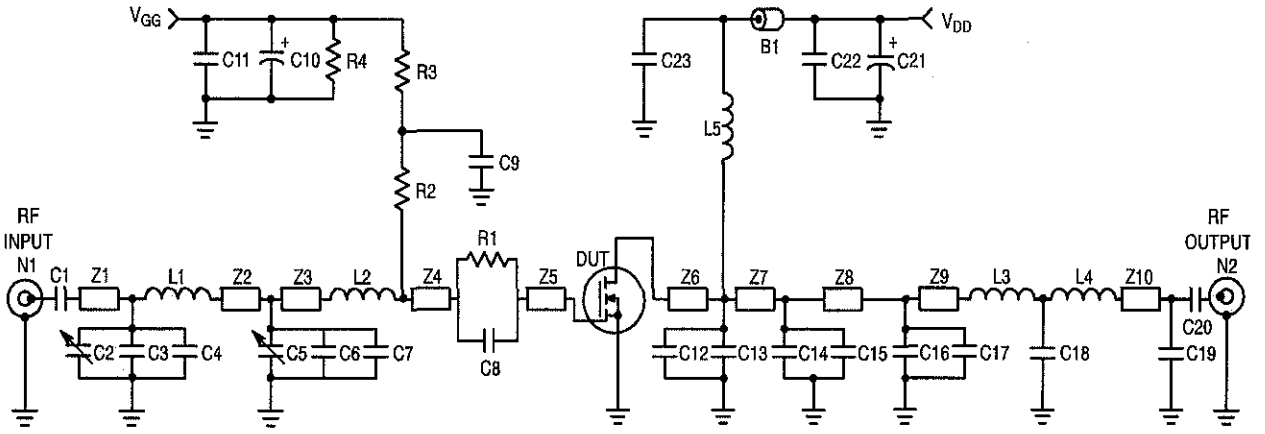
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.90	°C/W

(1) Calculated based on the formula $P_D = \frac{T_J - T_C}{R_{\theta JC}}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 100 μAdc)	$V_{(BR)DSS}$	60	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 10 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	0.3	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 12.5 Vdc, I_D = 400 μA)	$V_{GS(th)}$	1	—	2.6	Vdc
Drain–Source On–Voltage (V_{GS} = 5 Vdc, I_D = 0.6 A)	$R_{DS(on)}$	—	—	0.7	Ω
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 2.0 Adc)	$V_{DS(on)}$	—	—	1	Vdc
DYNAMIC CHARACTERISTICS					
Input Capacitance (Includes Input Matching Capacitance) (V_{DS} = 12.5 Vdc, V_{GS} = 0 V, f = 1 MHz)	C_{iss}	—	—	250	pF
Output Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0 V, f = 1 MHz)	C_{oss}	—	—	150	pF
Reverse Transfer Capacitance (V_{DS} = 12.5 Vdc, V_{GS} = 0 V, f = 1 MHz)	C_{rss}	—	—	20	pF
RF CHARACTERISTICS (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain (V_{DD} = 12.5 Vdc, P_{out} = 35 Watts, I_{DQ} = 500 mA) f = 520 MHz	G_{ps}	10	—	—	dB
Drain Efficiency (V_{DD} = 12.5 Vdc, P_{out} = 35 Watts, I_{DQ} = 500 mA) f = 520 MHz	η	50	—	—	%
Load Mismatch (V_{DD} = 15.6 Vdc, f = 520 MHz, 2 dB Input Overdrive, VSWR 20:1 at All Phase Angles)	Ψ	No Degradation in Output Power Before and After Test			



B1	Ferroxcube #VK200	L4	1 Turn, #26 AWG, 0.240″ ID
C1, C9, C20, C23	330 pF, 100 mil Chip Capacitors	L5	4 Turn, #24 AWG, 0.180″ ID
C2, C5	0 to 20 pF Trimmer Capacitors	N1, N2	Type N Flange Mounts
C3, C15	33 pF, 100 mil Chip Capacitors	R1	6.5 Ω, 1/4 W Chip Resistor
C4, C6, C19	18 pF, 100 mil Chip Capacitors	R2	39 Ω Chip Resistor (0805)
C7	160 pF, 100 mil Chip Capacitor	R3	1.2 kΩ, 1/8 W Chip Resistor
C8	240 pF, 100 mil Chip Capacitor	R4	33 kΩ, 1/4 W Chip Resistor
C10, C21	10 µF, 50 V Electrolytic Capacitors	Z1	0.970″ x 0.080″ Microstrip
C11, C22	470 pF, 100 mil Chip Capacitors	Z2	0.380″ x 0.080″ Microstrip
C12, C13	150 pF, 100 mil Chip Capacitors	Z3	0.190″ x 0.080″ Microstrip
C14	110 pF, 100 mil Chip Capacitor	Z4	0.160″ x 0.080″ Microstrip
C16	68 pF, 100 mil Chip Capacitor	Z5, Z6	0.110″ x 0.200″ Microstrip
C17	120 pF, 100 mil Chip Capacitor	Z7	0.490″ x 0.080″ Microstrip
C18	51 pF, 100 mil Chip Capacitor	Z8	0.250″ x 0.080″ Microstrip
L1	17.5 nH, Coilcraft #A05T	Z9	0.320″ x 0.080″ Microstrip
L2	5 nH, Coilcraft #A02T	Z10	0.240″ x 0.080″ Microstrip
L3	1 Turn, #26 AWG, 0.250″ ID	Board	Glass Teflon®, 31 mils

Figure 1. 135 – 175 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 135 – 175 MHz

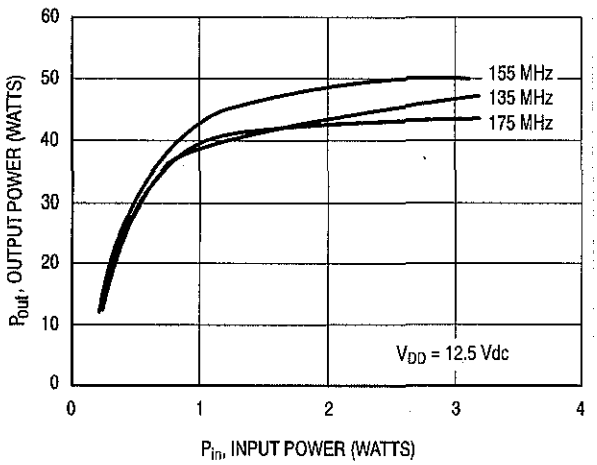


Figure 2. Output Power versus Input Power

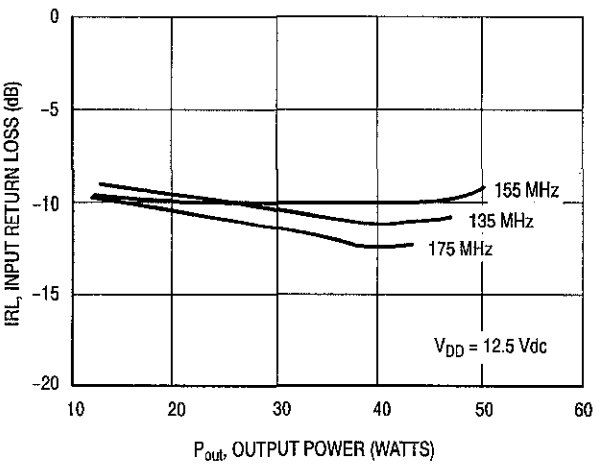


Figure 3. Input Return Loss versus Output Power

TYPICAL CHARACTERISTICS, 135 – 175 MHz

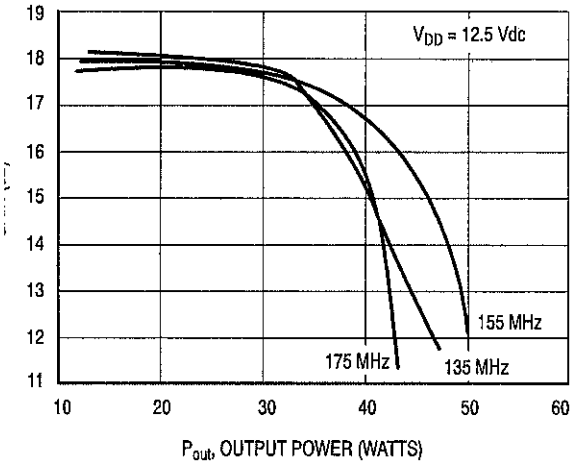


Figure 4. Gain versus Output Power

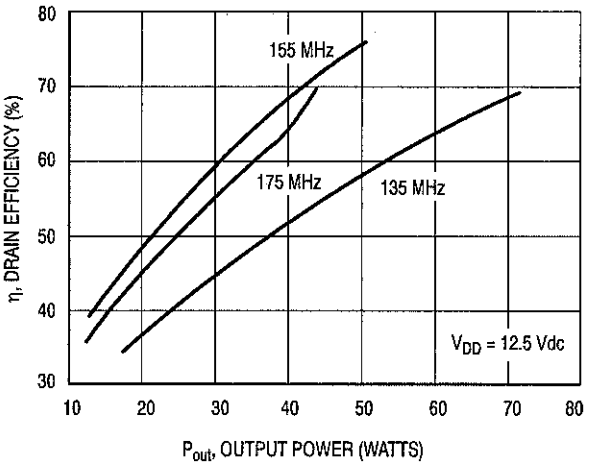


Figure 5. Drain Efficiency versus Output Power

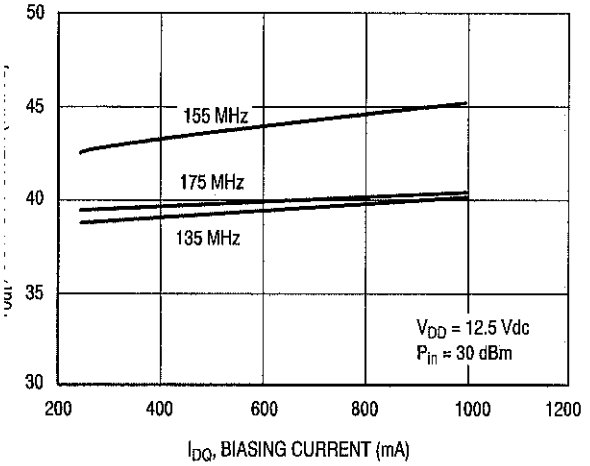


Figure 6. Output Power versus Biasing Current

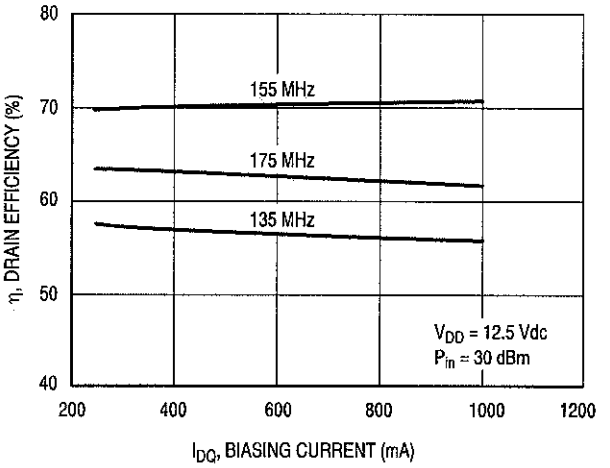


Figure 7. Drain Efficiency versus Biasing Current

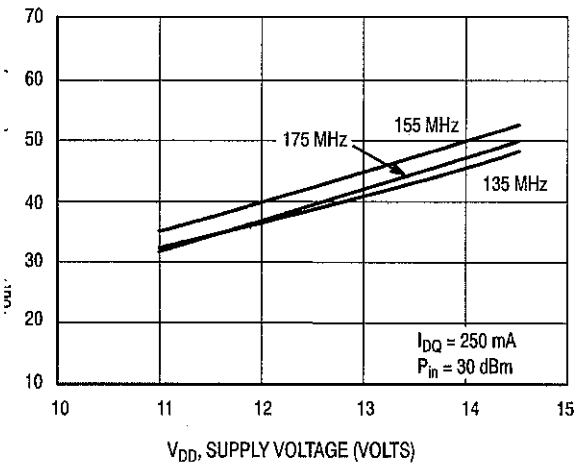


Figure 8. Output Power versus Supply Voltage

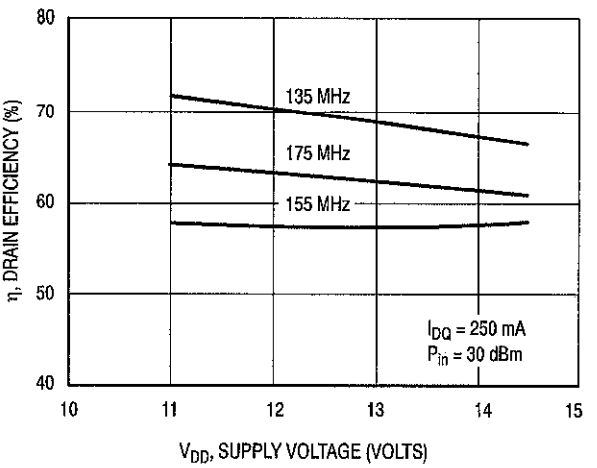
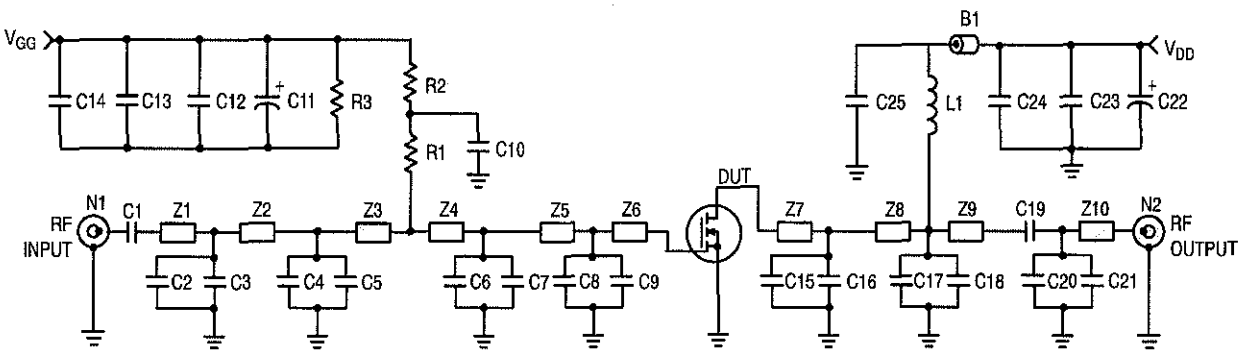


Figure 9. Drain Efficiency versus Supply Voltage



B1	Ferroxcube VK200	C21	1.8 pF, 100 mil Chip Capacitor
C1	160 pF, 100 mil Chip Capacitor	L1	47.5 nH, 5 Turn, Coilcraft
C2	3 pF, 100 mil Chip Capacitor	N1, N2	Type N Flange Mounts
C3	3.6 pF, 100 mil Chip Capacitor	R1	500 Ω Chip Resistor (0805)
C4	2.2 pF, 100 mil Chip Capacitor	R2	1 kΩ Chip Resistor (0805)
C5	10 pF, 100 mil Chip Capacitor	R3	33 kΩ, 1/8 W Chip Resistor
C6, C7	16 pF, 100 mil Chip Capacitors	Z1	0.480″ x 0.080″ Microstrip
C8, C15, C16	27 pF, 100 mil Chip Capacitors	Z2	1.070″ x 0.080″ Microstrip
C9	43 pF, 100 mil Chip Capacitor	Z3	0.290″ x 0.080″ Microstrip
C10, C14, C25	160 pF, 100 mil Chip Capacitors	Z4	0.160″ x 0.080″ Microstrip
C11, C22	10 µF, 50 V Electrolytic Capacitors	Z5, Z8	0.120″ x 0.080″ Microstrip
C12, C24	1,200 pF, 100 mil Chip Capacitors	Z6, Z7	0.120″ x 0.223″ Microstrip
C13, C23	0.1 µF, 100 mil Chip Capacitors	Z9	1.380″ x 0.080″ Microstrip
C17, C18	24 pF, 100 mil Chip Capacitors	Z10	0.625″ x 0.080″ Microstrip
C19	160 pF, 100 mil Chip Capacitor	Board	Glass Teflon®, 31 mils
C20	8.2 pF, 100 mil Chip Capacitor		

Figure 10. 450 – 520 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 450 – 520 MHz

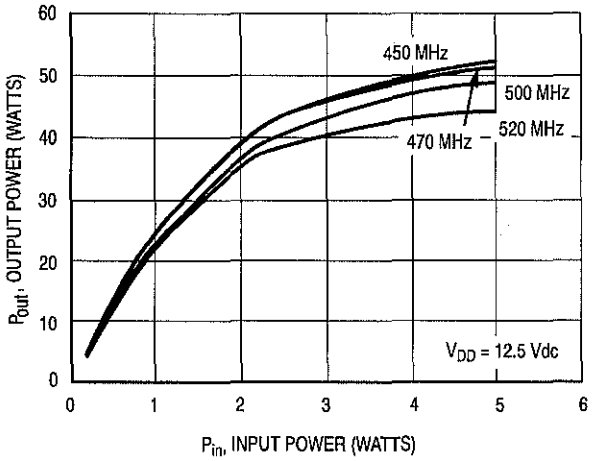


Figure 11. Output Power versus Input Power

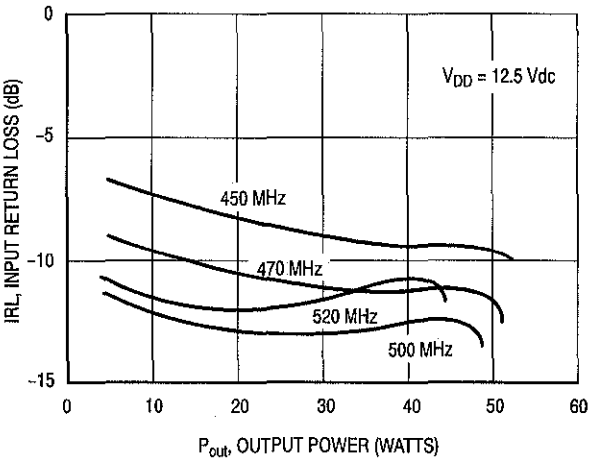


Figure 12. Input Return Loss versus Output Power

TYPICAL CHARACTERISTICS, 450 – 520 MHz

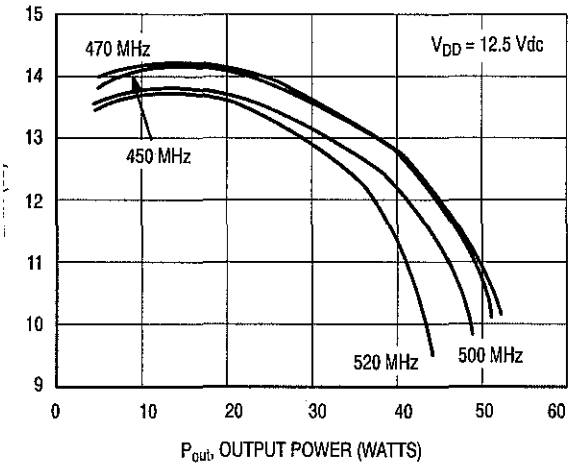


Figure 13. Gain versus Output Power

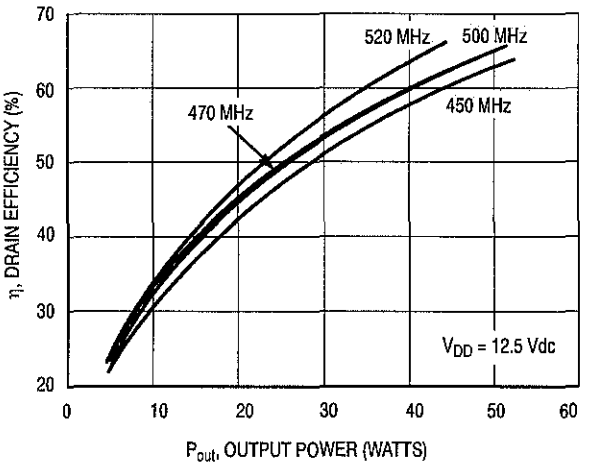


Figure 14. Drain Efficiency versus Output Power

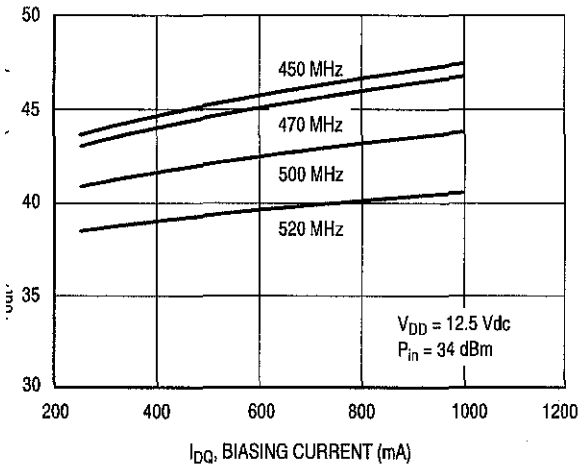


Figure 15. Output Power versus Biasing Current

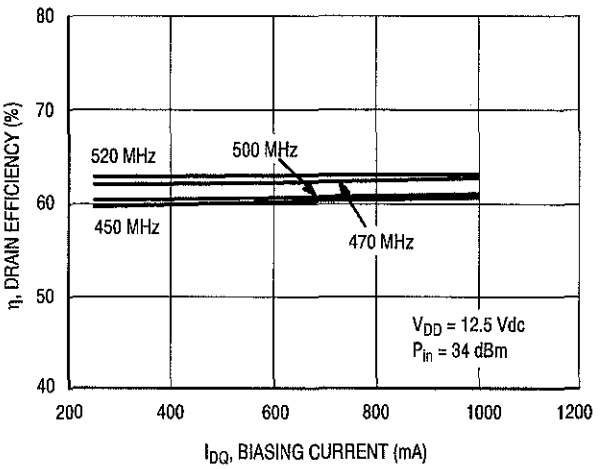


Figure 16. Drain Efficiency versus Biasing Current

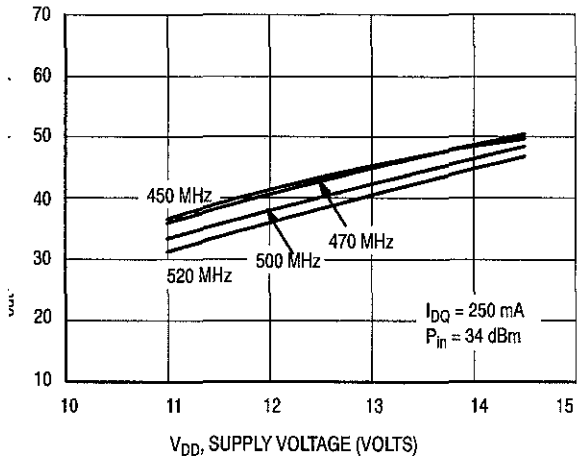


Figure 17. Output Power versus Supply Voltage

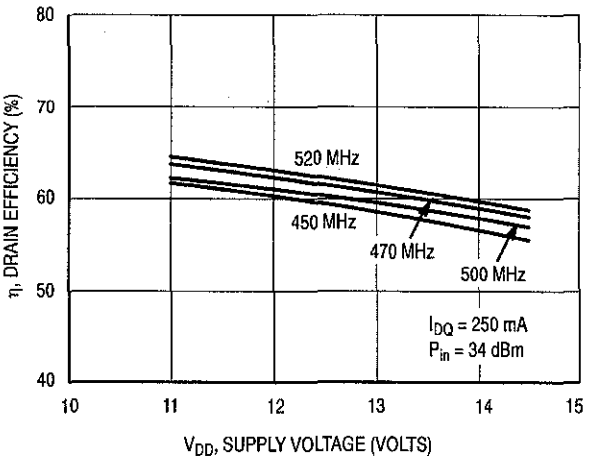
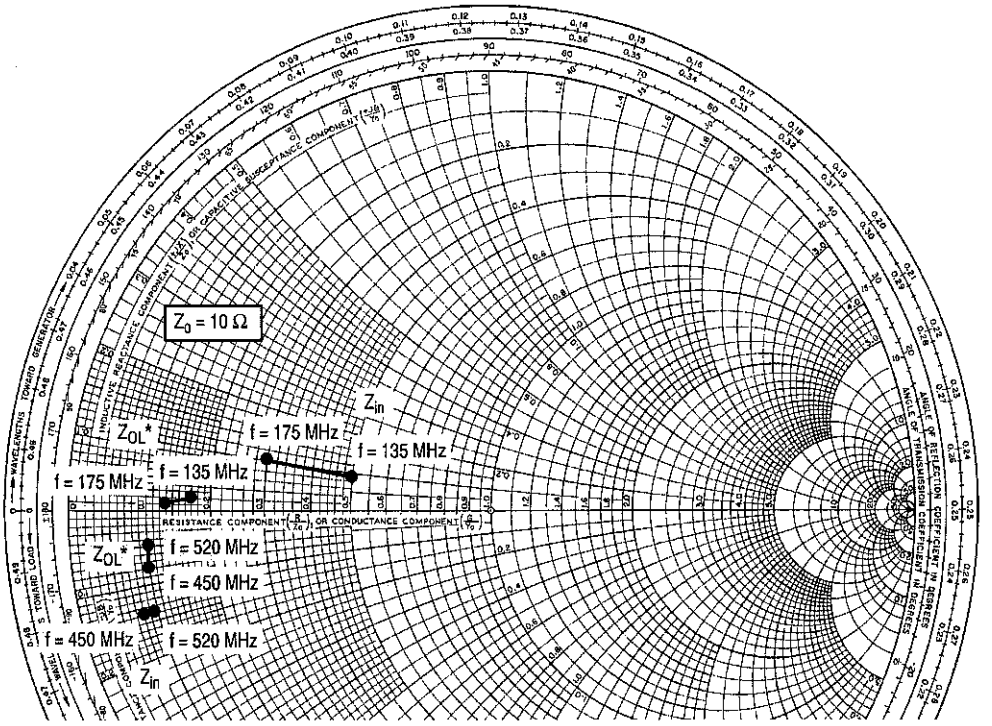


Figure 18. Drain Efficiency versus Supply Voltage



V_{DD} = 12.5 V, I_{DQ} = 250 mA, P_{out} = 35 W

f MHz	Z_{in} Ω	Z_{OL}^* Ω
135	5.0 + j0.9	1.7 + j0.2
155	5.0 + j0.9	1.7 + j0.2
175	3.0 + j1.0	1.3 + j0.1

V_{DD} = 12.5 V, I_{DQ} = 500 mA, P_{out} = 35 W

f MHz	Z_{in} Ω	Z_{OL}^* Ω
450	0.8 – j1.4	1.0 – j0.8
470	0.9 – j1.4	1.1 – j0.6
500	1.0 – j1.4	1.1 – j0.6
520	0.9 – j1.4	1.1 – j0.5

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the load impedance at given output power, voltage, frequency, and η_D > 50 %.

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the load impedance at given output power, voltage, frequency, and η_D > 50 %.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, drain efficiency, and device stability.

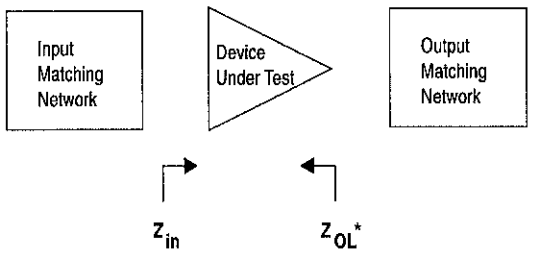


Figure 19. Series Equivalent Input and Output Impedance

Table 1. Common Source Scattering Parameters (V_{DD} = 12.5 Vdc)

I_{DQ} = 250 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
50	0.89	–173	8.496	83	0.014	–26	0.76	–170
100	0.90	–175	3.936	72	0.014	–14	0.79	–170
150	0.91	–175	2.429	63	0.011	–23	0.82	–170
200	0.92	–175	1.627	57	0.010	–44	0.86	–170
250	0.94	–176	1.186	53	0.007	–16	0.88	–170
300	0.95	–176	0.888	49	0.005	–44	0.91	–171
350	0.96	–176	0.686	48	0.005	36	0.92	–170
400	0.96	–176	0.568	44	0.005	–1	0.94	–171
450	0.97	–176	0.457	44	0.004	49	0.94	–172
500	0.97	–176	0.394	44	0.003	–51	0.95	–171
550	0.98	–176	0.332	42	0.001	31	0.95	–173
600	0.98	–177	0.286	41	0.013	99	0.94	–173

I_{DQ} = 1.0 A

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
50	0.90	–173	8.49	83	0.006	–39	0.86	–176
100	0.90	–175	3.92	72	0.009	–5	0.86	–176
150	0.91	–175	2.44	63	0.006	7	0.87	–176
200	0.92	–175	1.62	57	0.008	21	0.88	–175
250	0.94	–176	1.19	53	0.006	8	0.89	–174
300	0.95	–176	0.89	48	0.008	3	0.89	–174
350	0.96	–176	0.69	48	0.007	48	0.91	–174
400	0.96	–176	0.57	44	0.004	41	0.93	–173
450	0.97	–176	0.46	44	0.004	43	0.93	–173
500	0.97	–176	0.39	44	0.003	57	0.94	–173
550	0.98	–176	0.33	41	0.006	62	0.94	–174
600	0.98	–177	0.28	41	0.009	96	0.93	–173

I_{DQ} = 2.0 A

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	∠ϕ	$\|S_{21}\|$	∠ϕ	$\|S_{12}\|$	∠ϕ	$\|S_{22}\|$	∠ϕ
50	0.94	–176	9.42	88	0.005	–72	0.89	–177
100	0.94	–178	4.56	82	0.005	4	0.89	–177
150	0.94	–178	2.99	78	0.003	7	0.89	–177
200	0.94	–178	2.14	74	0.005	17	0.90	–176
250	0.95	–178	1.67	71	0.004	40	0.90	–175
300	0.95	–178	1.32	67	0.007	35	0.91	–175
350	0.95	–178	1.08	67	0.005	57	0.92	–174
400	0.96	–178	0.93	63	0.003	50	0.93	–173
450	0.96	–178	0.78	62	0.007	68	0.93	–173
500	0.96	–177	0.68	61	0.004	99	0.94	–173
550	0.97	–177	0.59	58	0.008	78	0.93	–175
600	0.97	–178	0.51	57	0.009	92	0.92	–174

APPLICATIONS INFORMATION

DESIGN CONSIDERATIONS

This device is a common–source, RF power, N–Channel enhancement mode, Lateral Metal–Oxide Semiconductor Field–Effect Transistor (MOSFET). Motorola Application Note AN211A, "FETs in Theory and Practice", is suggested reading for those not familiar with the construction and characteristics of FETs.

This surface mount packaged device was designed primarily for VHF and UHF mobile power amplifier applications. Manufacturability is improved by utilizing the tape and reel capability for fully automated pick and placement of parts. However, care should be taken in the design process to insure proper heat sinking of the device.

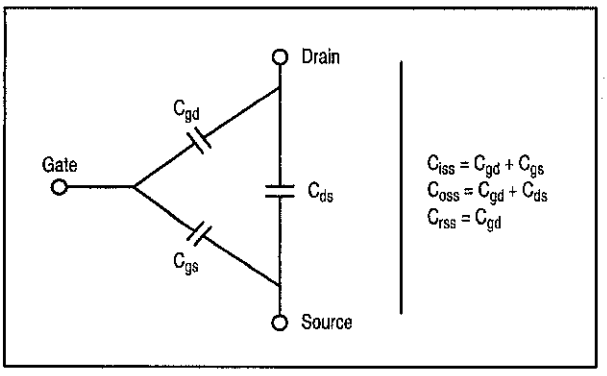
The major advantages of Lateral RF power MOSFETs include high gain, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage.

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain–to–source (C_{ds}). These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case, the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



DRAIN CHARACTERISTICS

One critical figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $R_{DS(on)}$, occurs in the linear region of the output characteristic and is specified at a specific gate–source voltage and drain current. The drain–source voltage under these conditions is termed $V_{DS(on)}$. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

BV_{DSS} values for this device are higher than normally required for typical applications. Measurement of BV_{DSS} is not recommended and may result in possible damage to the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The DC input resistance is very high – on the order of 10^9 Ω — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended. Using a resistor to keep the gate–to–source impedance low also helps dampen transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate–threshold voltage and turn the device on.

DC BIAS

Since this device is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. RF power FETs operate optimally with a quiescent drain current (I_{DQ}), whose value is application dependent. This device was characterized at I_{DQ} = 150 mA, which is the suggested value of bias current for typical applications. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of this device may be controlled to some degree with a low power dc control signal applied to the gate, thus facilitating applications such as manual gain control, ALC/AGC and modulation systems. This characteristic is very dependent on frequency and load line.

IOUNTING

The specified maximum thermal resistance of 0.9°C/W as-ımes a majority of the 0.170″ x 0.608″ source contact on ıe back side of the package is in good contact with an ap-ropriate heat sink. As with all RF power devices, the goal of ıe thermal design should be to minimize the temperature at ıe back side of the package. Refer to Motorola Application ote AN4005/D, "Thermal Management and Mounting Meth-d for the PLD–1.5 RF Power Surface Mount Package," and ngineering Bulletin EB209/D, "Mounting Method for RF ower Leadless Surface Mount Transistor" for additional in-›rmation.

.MPLIFIER DESIGN

Impedance matching networks similar to those used with ipolar transistors are suitable for this device. For examples ee Motorola Application Note AN721, "Impedance Matching letworks Applied to RF Power Transistors." Large–signal impedances are provided, and will yield a good first pass approximation.

Since RF power MOSFETs are triode devices, they are not unilateral. This coupled with the very high gain of this device yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. The RF test fixture implements a parallel resistor and capacitor in series with the gate, and has a load line selected for a higher efficiency, lower gain, and more stable operating region.

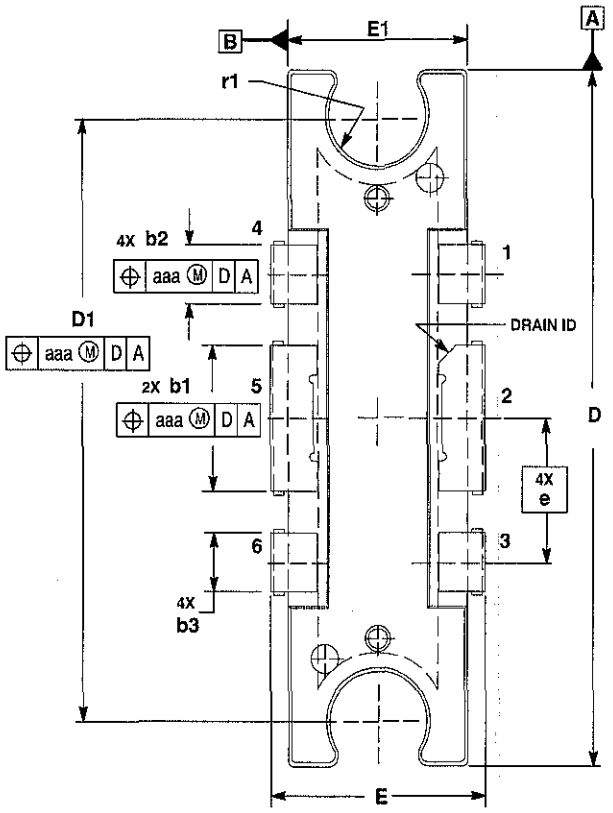
Two–port stability analysis with this device's S–parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A, "RF Small–Signal Design Using Two–Port Parameters" for a discussion of two port network theory and stability.

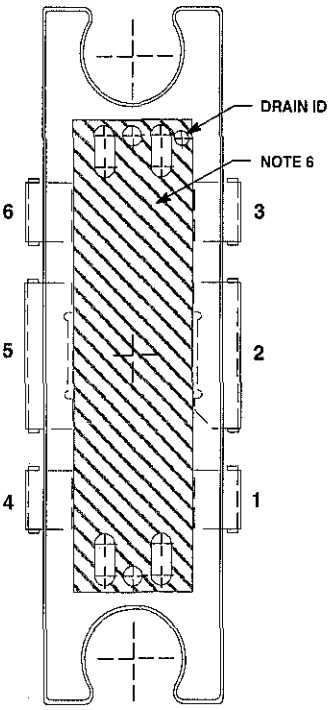
NOTES

NOTES

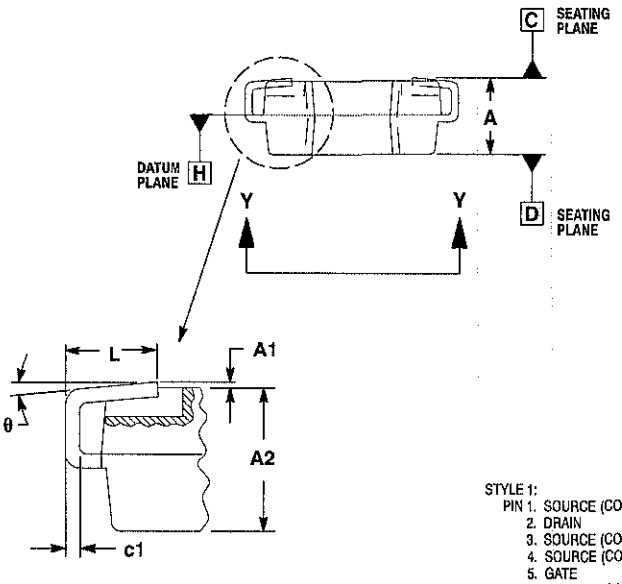
NOTES

PACKAGE DIMENSIONS





VIEW Y–Y

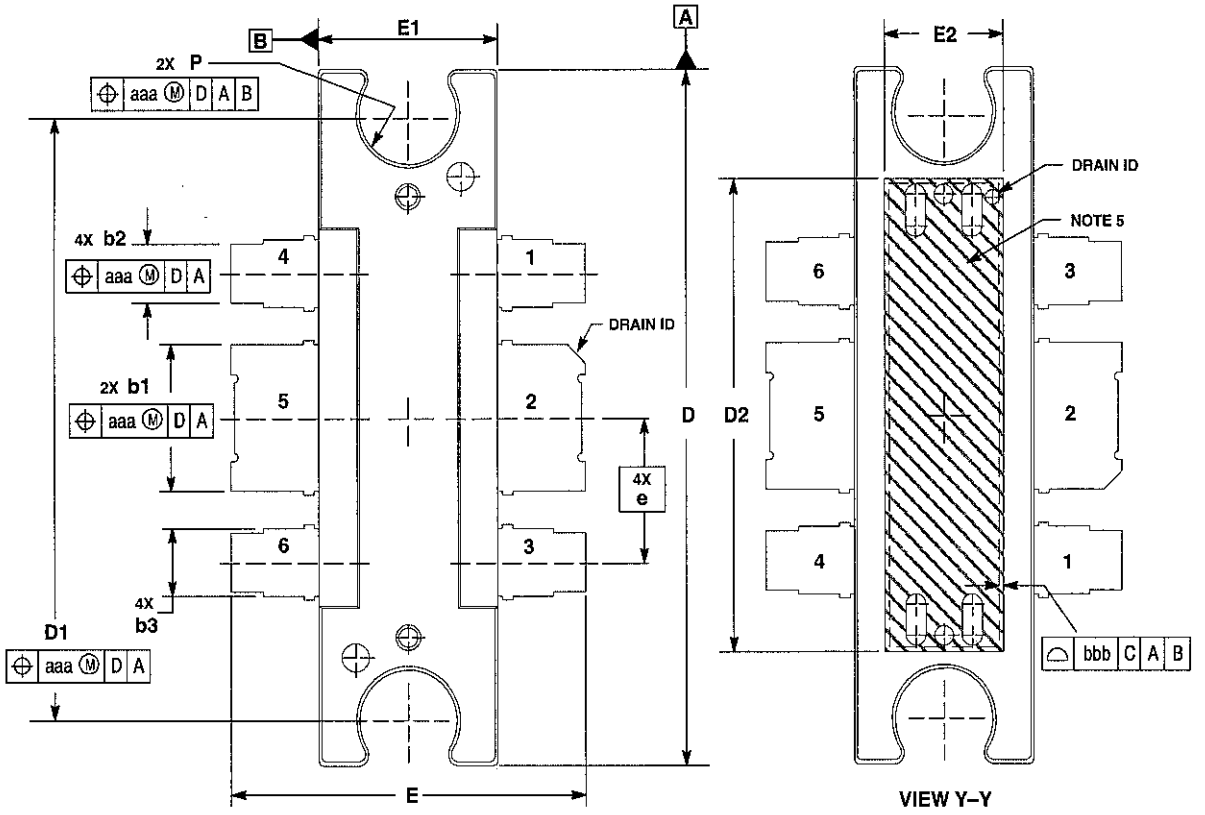


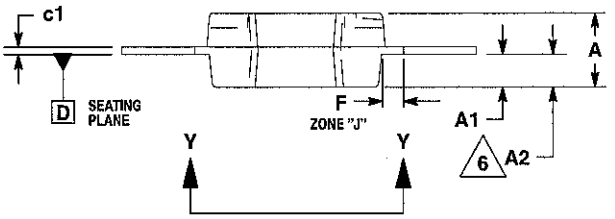
STYLE 1:
PIN 1. SOURCE (COMMON)
2. DRAIN
3. SOURCE (COMMON)
4. SOURCE (COMMON)
5. GATE
6. SOURCE (COMMON)

NOTES:
1. CONTROLLING DIMENSION: INCH .
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE -H- IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.006 PER SIDE. DIMENSION D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS b1 AND b3 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.005 TOTAL IN EXCESS OF THE b1 AND b2 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. CROSSHATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.098	0.110	2.489	2.794
A1	0.000	0.004	0.000	0.102
A2	0.098	0.106	2.489	2.692
D	0.926	0.934	23.520	23.724
D1	0.806	0.814	20.472	20.676
E	0.296	0.304	7.518	7.722
E1	0.246	0.254	6.248	6.452
L	0.060	0.070	1.524	1.778
b1	0.193	0.199	4.902	5.055
b2	0.078	0.084	1.981	2.134
b3	0.088	0.094	2.235	2.388
c1	0.007	0.011	0.178	0.279
e	0.193 BSC		4.902 BSC	
r1	0.053	0.058	1.600	1.727
θ	0°	6°	0°	6°
aaa	0.004		0.102	

CASE 1264–08
ISSUE H
TO–272
PLASTIC
MRF1535T1





NOTES:
1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.006 PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
4. DIMENSIONS b1 AND b3 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.005 TOTAL IN EXCESS OF THE b1 AND b2 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
5. CROSSHATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.
6. DIMENSION A2 APPLIES WITHIN ZONE J ONLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.098	0.106	2.49	2.69
A1	0.038	0.044	0.96	1.12
A2	0.040	0.042	1.02	1.07
D	0.926	0.934	23.52	23.72
D1	0.810 BSC		20.57 BSC	
D2	0.608 BSC		15.44 BSC	
E	0.492	0.500	12.50	12.70
E1	0.246	0.254	6.25	6.45
E2	0.170 BSC		4.32 BSC	
F	0.025 BSC		0.64 BSC	
P	0.126	0.134	3.20	3.40
b1	0.193	0.199	4.90	5.05
b2	0.078	0.084	1.98	2.13
b3	0.089	0.094	2.24	2.39
c1	0.007	0.011	0.178	0.279
e	0.193 BSC		4.90 BSC	
aaa	0.004		0.10	
bbb	0.008		0.20	

STYLE 1:
PIN 1. SOURCE (COMMON)
2. DRAIN
3. SOURCE (COMMON)
4. SOURCE (COMMON)
5. GATE
6. SOURCE (COMMON)

CASE 1264A–02
ISSUE A
TO–272 STRAIGHT LEAD
PLASTIC
MRF1535FT1

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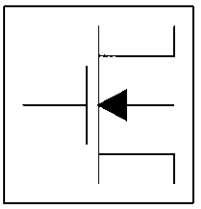
APPENDIX H

ADS MOSFET MODEL STRUCTURE

;IM3_Model (BSIM3 MOSFET Model)

mbol



rameters

)del parameters must be specified in SI units.

Table 5-4. BSIM3_Model Parameters

rameter	Description	Units	Default
/IOS	N-channel type model		yes
/IOS	P-channel type model		no
;mod	Ids model		8
rsion	model version		3.2.2
)bmod	mobility model selector		1
ıpmod	capacitance model selector		1
)imod	noise model selector		1
ramchk	model parameter checking selector		0
ıunit	bin unit selector		1
ı	gate resistance	ohms	0
;h	drain and source diffusion sheet resistance	ohms/sq	0.0
	bulk P-N emission coefficient		1.0
	junction current temp. exponent		3.0
	gate saturation current	A/m^2	10^{-4}
w	sidewall junction reverse saturation current	A/m^2	0.0
ıt	length offset fitting parameter	m	0.0
	coefficient of length dependence for length offset	m^{Lln}	0.0

Calculated parameter

Table 5-4. BSIM3_Model Parameters (continued)

rameter	Description	Units	Default
ı	power of length dependence of length offset		1.0
'	coefficient of width dependence for length offset	m^{Lwn}	0.0
'n	power of width dependence of length offset		1.0
'l	coefficient of length and width cross term for length offset	$m^{(Lwn+Lln)}$	0.0
nt	width offset fitting parameter	m	0.0
	coefficient of length dependence for width offset	m^{Wln}	0.0
n	power of length dependence of width offset		1.0
w	coefficient of width dependence for width offset	m^{Wwn}	0.0
wn	power of width dependence of width offset		1.0
wl	coefficient of length and width cross term for width offset	$m^{(Wwn+Wln)}$	0.0
om	parameter measurement temp.	°C	25
x	oxide thickness	m	1.5×10^{-8}
	zero-bias bulk junction bottom capacitance	F/m^2	5.0×10^{-4}
	bulk junction bottom grading coefficient		0.5
sw	zero-bias bulk junction sidewall capacitance	F/m	5.0×10^{-10}
sw	bulk junction sidewall grading coefficient		0.33
	bulk junction potential	V	1.0
sw	sidewall junction potential	V	1.0

Calculated parameter

Table 5-4. BSIM3_Model Parameters (continued)

rameter	Description	Units	Default
	doping depth	m	1.55×10^{-7}
m	maximum applied body bias	V	–5.0
x	Vth transition body voltage	V	†
	metallurgical junction depth	m	1.5×10^{-7}
/g	coefficient of Weff's gate dependence	m/V	0.0
/b	coefficient of Weff's body dependence	$m/V^{(1/2)}$	0.0
h	channel doping concentration	$1/cm^3$	1.7×10^{17}
ub	substrate doping concentration	$1/cm^3$	6.0×10^{16}
ate	poly-gate doping concentration	$1/cm^3$	†
mma1	body effect coefficient near interface	$V^{(1/2)}$	†
mma2	body effect coefficient in the bulk	$V^{(1/2)}$	†
ha0	1st parameter of impact ionization current	m/V	0.0
ta0	2nd parameter of impact ionization current	V	30.0
0	zero-bias threshold voltage	V	†
	first order body effect coefficient	$V^{(1/2)}$	†
	second order body effect coefficient		†
	narrow width effect coefficient		80.0
b	body effect coefficient of K3	1/V	0.0
)	narrow width effect W offset	m	2.5×10^{-6}
:	lateral non-uniform doping effect	m	1.74×10^{-7}
t0	short channel effect coefficient 0		2.2
t1	short channel effect coefficient 1		0.53
t2	short channel effect coefficient 2	1/V	–0.032
t0w	narrow width effect coefficient 0	1/m	0.0
t1w	narrow width effect coefficient 1	1/m	5.3×10^{6}

alculated parameter

Table 5-4. BSIM3_Model Parameters (continued)

rameter	Description	Units	Default
t2w	narrow width effect coefficient 2	1/V	–0.032
so	gate-source overlap capacitance, per channel width	F/m	†
do	gate-drain overlap capacitance, per channel width	F/m	†
bo	gate-bulk overlap capacitance, per channel length	F/m	0.0
art	flag for channel charge partition		0.0
out	DIBL effect on Rout coefficient		0.56
ub	DIBL effect coefficient in subthreshold region		(fixed by Drout)
	linear Vgs dependence of mobility	m/V	2.25×10^{-9}
1	temperature coefficient of Ua	m/V	4.31×10^{-9}
	quadratic Vgs dependence of mobility	$(m/V)^2$	5.87×10^{-19}
1	temperature coefficient of Ub	$(m/V)^2$	-7.61×10^{-18}
	body-bias dependence of mobility	m/V^2 1/V	-4.65×10^{-11} Mobmod =1,2–0.0465 Mobmod=3
1	temperature coefficient of Uc	m/V^2 1/V	-5.6×10^{-11} Mobmod=1,2 –0.056 Mobmod=3
	low-field mobility at T=Tnom	$cm^{2/Vs}$	670.0 NMOS 250.0 PMOS
e	temperature coefficient of mobility		–1.5
sw	source drain resistance per width	ohms $\times \mu m^{Wr}$	0.0
wg	gate bias effect coefficient of Rdsw	1/V	0.0
wb	body effect coefficient of Rdsw	1/V	0.0
	width dependence of Rds		1.0
	temperature coefficient of Rdsw	ohms $\times$ µm	0.0
at	saturation velocity at T=Tnom	m/s	8.0×10^4

alculated parameter

Table 5-4. BSIM3_Model Parameters (continued)

rameter	Description	Units	Default
	temperature coefficient of Vsat	m/s	3.3×10^4
	bulk charge effect coefficient for channel length		1.0
ta	body-bias coefficient of bulk charge	1/V	–0.047
s	gate bias coefficient of Abulk	1/V	0.0
	first non-saturation factor for PMOS	1/V	0.0
	second non-saturation factor for PMOS		1.0
	bulk charge effect coefficient for channel width	m	0.0
	bulk charge effect width offset	m	0.0
ff	threshold voltage offset	V	-0.08
actor	subthreshold swing factor		1.0
sc	D/S and channel coupling capacitance	F/m^2	2.4×10^{-4}
scb	body-bias dependence of Cdsc	$F/V/m^2$	0.0
scd	drain-bias dependence of Cdsc	$F/V/m^2$	0.0
	interface state capacitance	F/m^2	0.0
a0	subthreshold region DIBL coefficient		0.08
ab	body-bias coefficient for DIBL effect	1/V	–0.07
lm	channel-length modulation coefficient		1.3
iblc1	first Rout DIBL effect coefficient		0.39
iblc2	second Rout DIBL effect coefficient		0.0086
iblcb	body effect coefficient of DIBL correction parameters	1/V	0
cbe1	first substrate current body effect	V/m	4.24×10^8
cbe2	second substrate current body effect	m/V	10^{-5}
ag	Vg dependence of Rout coefficient		0.0
lta	effective Vds parameter	V	0.01
	temperature coefficient of Vth	V	–0.11

alculated parameter

Table 5-4. BSIM3_Model Parameters (continued)

rameter	Description	Units	Default
1l	channel length sensitivity of Kt1	V×m	0.0
2	body bias coefficient of Kt1		0.022
ısl	light doped source-gate region overlap capacitance	F/m	0.0
ıdl	light doped drain-gate region overlap capacitance	F/m	0.0
:appa	coefficient for lightly doped region overlap capacitance	F/m	0.6
	fringing field capacitance	F/m	
;	constant term for short channel model	m	0.1×10^{-6}
ə	exponential term for short channel		0.6
;	length offset fitting parameter from C-V	m	Lint
vc	width offset fitting parameter from C-V	m	Wint
ev	Noise model level		-1
lwnoi	Drain noise parameters for Nlev=3		1
	flicker (1/f) noise coefficient		0.0
	flicker (1/f) noise exponent		1.0
	flicker (1/f) noise frequency exponent		1.0
ı	flicker (1/f) noise parameter	V/m	4.1×10^{7}
ıia	noise parameter A		1.0×10^{20} NMOS 9.9×10^{18} PMOS
ıib	noise parameter B		5.0×10^{4} NMOS 2.4×10^{3} PMOS
ıic	noise parameter C		-1.4×10^{-12} NMOS 1.4×10^{12} PMOS
ax	explosion current	A	10.0
'subfwd	substrate junction forward bias (warning)	V	infinite
ıvsub	substrate junction reverse breakdown voltage (warning)	V	infinite

:alculated parameter

Table 5-4. BSIM3_Model Parameters (continued)

rameter	Description	Units	Default
ivg	gate oxide breakdown voltage (warning)	V	infinite
ivds	drain-source breakdown voltage (warning)	V	infinite
idsmax	maximum drain-source current (warning)	A	infinite
xm	gate oxide thickness tox value at which parameters are extracted	m	
o	DC flat-band voltage	V	†
iff	CV parameter in VgsteffCV for weak-to-strong inversion region		1.0
ffcv	CV parameter in VgsteffCV for weak-to-strong inversion region		1.0
i	diode limiting current	A	†
iha1	substrate current parameter	1/V	0.0
de	exponential coefficient for charge thickness in the accumulation and depletion regions	m/V	1.0
in	coefficient for the gate-bias dependent surface potential	$V^{(1/2)}$	15.0
b	temperature coefficient of pb	V/K	0.0
bsw	temperature coefficient of pbsw	V/K	0.0
bswg	temperature coefficient of pbswg	V/K	0.0
j	temperature coefficient of cj	1/K	0.0
jsw	temperature coefficient of cjsw	1/K	0.0
jswg	temperature coefficient of cjswg	1/K	0.0
;	coefficient of length dependence for CV channel length offset	m^{Lln}	DC Ll
ic	coefficient of width dependence for CV channel length offset	m^{Lwn}	DC Lw
ilc	coefficient of length and width cross-term for CV channel length offset	$m^{Lwn + LLn}$	DC Lwl

Calculated parameter

Table 5-4. BSIM3_Model Parameters (continued)

rameter	Description	Units	Default
c	coefficient of length dependence for CV channel width offset	m^{Wln}	DC Wl
wc	coefficient of width dependence for CV channel width offset	m^{Wwn}	DC Ww
wlc	coefficient of length and width cross-term for CV channel width offset	$m^{Wln + Wwn}$	DC Wwl
'max	maximum power dissipation (warning)	W	infinite
m	area calculation method		10
lcacm	flag to use Acm when Acm=12		0
if	length of heavily doped diffusion (ACM=2,3 only)	m	0
f	length of lightly doped diffusion adjacent to gate (ACM=1,2)	m	0
nlt	width diffusion layer shrink reduction factor		1
'	accounts for masking and etching effects	m	0
	accounts for masking and etching effects	m	0
c	additional drain resistance due to contact resistance	Ohms	0
c	additional source resistance due to contact resistance	Ohms	0
ıcv	flat-band voltage parameter for capmod=0 only	F/m	-1.0
qmod	BSIM3 charge model (0 for Berkeley, 1 for Hspice Capmod = 0)		0
wg	S/D (gate side) sidewall junction capacitance	F/m	Cjsw
swg	S/D (gate side) sidewall junction built in potential	V	Mjsw
alculated parameter			

Table 5-4. BSIM3_Model Parameters (continued)

rameter	Description	Units	Default
swg	S/D (gate side) sidewall junction grading coefficient		Pbsw
	bulk junction saturation current	A	1e-14
ısmod	non-quasi-static model selector		0
n	non-quasi-static Elmore constant parameter		5.0
l	drain resistance	Ohms	0
	source resistance	Ohms	0
;mod	flicker noise model selector		0
ev	temperature equation selector (0/1/2/3)		0
evc	temperature equation selector for capacitance (0/1/2/3)		0
	band gap	eV	1.16
ıp1	energy gap temperature coefficient alpha	V/°C	7.02e-4
ıp2	energy gap temperature coefficient beta	K	1108
a	Cj linear temperature coefficient	1/°C	0
ɔ	Cjsw linear temperature coefficient	1/°C	0
a	Vj linear temperature coefficnet	1/°C	0
ɔ	Vjsw linear temperature coefficient	1/°C	0
l	Rd linear temperature coefficient	1/°C	0
;	Rs linear temperature coefficient	1/°C	0
nin	binning minimum width (not used for binning; use BinModel)	m	0
nax	binning maximum width (not used for binning; use BinModel)	m	1
ıin	binning minimum length (not used for binning; use BinModel)	m	0
Calculated parameter			

Table 5-4. BSIM3_Model Parameters (continued)

rameter	Description	Units	Default
ıax	binning maximum length (not used for binning; use BinModel)	m	1
lParams	DataAccessComponent-based parameters		

Calculated parameter

tes/Equations/References

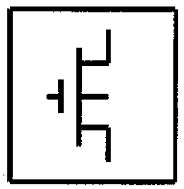
1. Nqsmod is also supported as an instance parameter. For simulation, only the Nqsmod instance parameter is used; the Nqsmod model parameter is not used. This is the way Berkeley defined Nqsmod in BSIM3v3.2. Hspice supports Nqsmod only as a model paramete
2. This model supplies values for a MOSFET device. The default Version is 3.2.2. The previous version can be used by setting the Version parameter to 3.0, 3.1, 3.2, or 3.2.1.
3. BSIM1, BSIM2, and BSIM3 MOSFET models use the same parameters and parameter definitions as the BSIM models in SPICE3 (University of California-Berkeley).
4. The nonquasi-static (NQS) charge model is supported in versions 3.2 and later.
5. Model parameter U0 can be entered in meters or centimeters. U0 is converted to m^2/V sec as follows: if U0 > 1, it is multiplied by 10^{-4}.
6. Use AllParams with a DataAccessComponent to specify file-based parameters (refer to DataAccessComponent). Note that model parameters that are explicitly specified take precedence over those specified via AllParams. Set AllParams to the DataAccessComponent instance name.
7. DC operating point data is generated for this model. If a DC simulation is performed, device operating point data can be viewed for a component. The procedure for doing this is described in the *Circuit Simulation* manual. The device operating point information that is displayed for the BSIM3 model is:

ıb	Small-signal Vbs to Ids transconductance, in Siemens
s	Small-signal drain source conductance, in Siemens

lsat	Saturation voltage, in Volts
ıpbd	Small-signal bulk drain capacitance, in Farads
ıpbs	Small-signal bulk source capacitance, in Farads
ıdM	Small-signal gate drain Meyer capacitance, in Farads
ıbM	Small-signal gate bulk Meyer capacitance, in Farads
ısM	Small-signal gate source Meyer capacitance, in Farads
ıgDvgb	Small-signal transcapacitance dQg/dVg, in Farads
ıgDvdb	Small-signal transcapacitance dQg/dVd, in Farads
ıgDvsb	Small-signal transcapacitance dQg/dVs, in Farads
ıbDvgb	Small-signal transcapacitance dQb/dVg, in Farads
ıbDvdb	Small-signal transcapacitance dQb/dVd, in Farads
ıbDvsb	Small-signal transcapacitance dQb/dVs, in Farads
ıdDvgb	Small-signal transcapacitance dQd/dVg, in Farads
ıdDvdb	Small-signal transcapacitance dQd/dVd, in Farads
ıdDvsb	Small-signal transcapacitance dQd/dVs, in Farads

ıIM3SOI_Model (BSIM3 Silicon On Insulator MOSFET Model)

mbol



rameters

ıdel parameters must be specified in SI units. In some cases, parameters that are ıply geometric variations of a listed parameter, such as L, W, or P, are not listed in s table.

Table 5-5. BSIM3SOI Parameters

rameter	Description	Units	Default
/IOS	N-channel type model		yes
/IOS	P-channel type model		no
ıpmod	short-channel capacitance model selector		2
ıbmod	mobility model selector		1
ıimod	noise model selector		1
mod	self-heating mode selector; 0 = no self-heating, 1 = self-heating		0
lmod	dynamic depletion mode selector		0
nod	gate current model selector		0
ramchk	model parameter checking selector		0
ıunit	Bin unit selector		1
rsion	model version		2.0
‹	gate oxide thickness	m	1.0e-8)
sc	drain, source, and channel coupling capacitance	F/m^2	2.4e-4
sccb	body effect coefficient of Cdsc	F/(V*m^2)	0/0
scd	drain bias dependence of Cdsc	F/(V*m^2	0.0

:alculated parameter

Table 5-5. BSIM3SOI Parameters (continued)

rameter	Description	Units	Default
:	capacitance due to interface change	F/(V*m^2	1.0
actor	subthreshold swing factor		0.0
at	saturation velocity at temp, m/s	m/s	8.0e4
	temperature coefficient for saturation velocity	m/s	3.3e4
)	bulk change effect coefficient		1.0
s	gate bulk coefficient of Abulk	V^-1	0.0
	first saturation factor	V^-1	0.0
	second non-saturation factor		1.0
ta	body-bias coefficient of the bulk charge effect	V^-1	-0.6
ub	substrate doping concentration with polarity	cm	6.0e16
h	Channel doping concentration	cm^-3	17e17
ate	poly-gate doping concentration	cm^-3	0
ımma1	body-effect coefficient near the interface	V^(1/2)	†
ımma2	body-effect coefficient in the bulk	V^(1/2)	†
x	Vth transition body voltage	V	†
m	maximum body voltage	V	-3.0
	doping depth	m	1.55e-7
	body-effect coefficient	V^(1/2)	0.5
l	temperature coefficient for threshold voltage,	V	-0.11
l1	channel length sensitivity of ktl	V+m	0.0
2	body-bias coefficient		0.022
	bulk effect coefficient 2		0.0
	narrow width coefficient		0.0
b	body effect coefficient of K3	V^-1	0.0

:alculated parameter

Table 5-5. BSIM3SOI Parameters (continued)

rameter	Description	Units	Default
ɔ	narrow width		0.0
x	lateral non-uniform doping coefficient	m	1.74e-7
t0	first coefficient of short-channel effect on Vth		2.2
t1	first coefficient of short-channel effect on Vth		0.53
t2	body-bias coefficient of short-channel effect on Vth	V^-1	-0.032
t0w	first coefficient of narrow-width effect on Vth		0.0
t1w	first coefficient of narrow-width effect on Vth	m^1	5.3e6
t2w	second coefficient of narrow-width effect on Vth	m^1	5.3e6
ɔut	L depend		0.56
ub	BL coefficient in sub-threshold region		Drout
ı0	zero-bias threshold voltage		0.7 (NMOS), -0.7 (PMOS)
	first-order mobility degradation coefficient	m/V	2.25e-9
1	temperature coefficient of Ua	m/V	4.31e-9
	second-order mobility degradation coefficient	$(m/V)^2$	5.87e-19
1	temperature coefficient of Ub	$(m/V)^2$	–7.61e-18
	body-bias mobility degradation coefficient	V^-1	–0.0465
1	temperature coefficient of Uc	V^-1	-0.056
	low-field mobility at T=Tnom	m^2/(V*s)	0.067 NMOS 0.025 PMOS
ɜ	temperature coefficient of mobility		–1.5

alculated parameter

Table 5-5. BSIM3SOI Parameters (continued)

rameter	Description	Units	Default
ff	Offset voltage in sub-threshold region	V	0.08
om	measurement temperature	C	25
jdo	G-D overlap capacitance per meter channel width	F/m	†
art	coefficient of channel charge share		0.0
lta	effective Vds	V	0.01
h	drain and source diffusion sheet resistance	Ohm/Sq	0.0
lsw	parasitic resistance per unit width	Ohms*um^Wr	0.0
wg	gate bias effect on parasitic resistance	V^-'	0.0
wb	body effect on parasitic resistance	V^-(1/2)	–0.047
t	temperature coefficient of parasitic resistance	Ohms*um	0.0
a0	sub-threshold region DIBL coefficient		0.08
ab	second non-saturation factor for PMOS	V^-1	-0.07
lm	channel-length modulation effect coefficient		1.3
liblc1	drain induced barrier lowering effect coefficient 1		0.39
liblc2	drain induced barrier lowering effect coefficient 1	V	-0.086
liblc2b	body effect on drain induced barrier lowering	V^-1	0.0
ag	gate voltage dependence of Rout coefficient		0.0
ox	back gate oxide thickness	m	3.0e-7
i	silicon-on-insulator thickness	m	1.0e-7
	metallurgical junction depth	m	Tsi
h0	self-heating thermal resistance	Ohms	0.0

Calculated parameter

Table 5-5. BSIM3SOI Parameters (continued)

rameter	Description	Units	Default
ıo	self-heating thermal capacitance	F	0.0
idi	GIDL first parameter	V	1.2
idi	GIDL second parameter	Ohm^-1	0.0
idi	GIDL third parameter	V/m	0.0
iode	diode non-ideality factor		1.0
jt	temperature coefficient for Isbjt		1.0
if	temperature coefficient for Isdif		1.0
ec	temperature coefficient for Isrec		1.0
ın	temperature coefficient for Istun		0.0
swg	S/D (gate side) sidewall junction built-in potential	V	0.07
swg	S/D (gate side) sidewall junction grading coefficient		0.5
wg	S/D (gate side) sidewall junction capacitance	m	1.0ε–10
ıt	length reduction parameter	m	0.0
	coefficient of length dependence for length offset	m	0.0
ı	power of length dependence of length offset	m	1.0
'	coefficient of width dependence for length offset	m	0.0
'n	power of width dependence for length offset	m	1.0
'l	coefficient of lenth and width cross term length offset	m	0.0
'	width dependence of Rds		1.0
nt	width reduction parameter	m	0.0
/g	coefficient of Weff's gate dependence	m/V	0.0

Calculated parameter

Table 5-5. BSIM3SOI Parameters (continued)

rameter	Description	Units	Default
/b	coefficient of Weff's substrate body bias dependence	m/V^(-1/2)	0.0
l	coefficient of length dependence for width offset	m	0.0
n	power of length dependence for width offset		1.0
w	coefficient of width dependence for width offset	m	0.0
wn	power of width dependence for width offset		1.0
wl	coefficient of length and width cross term width of offset	m	0.0
)	bulk charge coefficient for channel width	m	0.0
	bulk charge effect width offset	m	0.0
sl	light doped source-gate region overlap capacitance	F/m	0.0
appa	coefficient for light doped source-gate region overlap capacitance	F/m	0.0
	fringing field capacitance	F/m	†
:	constant term for the short channel model	m	0.1e-7
:	exponential term for the short channel model		0.0
/c	width offset fitting parameter from C-V	m	Wint
	length offset fitting parameter from C-V	m	Lint
ha0	first parameter of impact ionization current	m/V	0.0
a	noise parameter A		1.0e20 (NMOS), 9.9e18 (PMOS)
b	noise parameter B		5.0e4(NMOS), 2.4e3 (PMOS)

:alculated parameter

Table 5-5. BSIM3SOI Parameters (continued)

rameter	Description	Units	Default
ic	noise parameter C		-1,4e-12 (NMOS), -1,4e-12 (PMOS)
ı	flicker (I/f) noise parameter	V/m	4.1e-7
	flicker (I/f) noise frequency exponent	V	1.0
	flicker (I/f) noise exponent		1.0
	flicker (I/f) noise coefficient		0.0
if	floating body noise ideality factor		1.0
w1	first body effect with dependent parameter	m	0.0
w2	second body effect with dependent parameter	m	0.0
tas	surface potential adjustment for bulk charge effect	V	0.0
/bc	width offset for body contact isolation edge	m	0.0
ta0	first Vds parameter of impact isolation current	V^-1	0.0
ta1	second Vds parameter of impact isolation current		0.0
ta2	third Vds parameter of impact isolation current	V	0.0
satiiO	nominal drain saturation voltage at threshold for impact ionization current	V	0.9
	temperature dependent parameter for impact ionization		0.0
i	channel length dependent parameter threshold for impact ionization		0.0
0	first Vgs dependent parameter for impact ionization current	V^-1	0.5
1	second Vgs dependent parameter for impact ionization current	V^-1	0.1

Calculated parameter

Table 5-5. BSIM3SOI Parameters (continued)

rameter	Description	Units	Default
2	third Vgs dependent parameter for impact ionization current	V^-1	0.1
d	Vgs dependent parameter for impact ionization current	V^-1	0.1
jtii	fraction of bipolar current affecting the impact ionization		0.0
atii	saturation electric field for impact ionization	V /m	1.0e7
ın	reverse tunneling new-ideality factor		10.0
ecf0	recombination non-ideality factor at forward bias		2.0
ecro	recombination non-ideality factor at reversed bias		10.0
t	BJT injection saturation current	A/m^2	1.0e-6
f	Body to source/drain injection saturation current	A/m^2	0.0
ic	recombination in depletion saturation current	A/m^2	1.0e-6
ın	reverse tunneling saturation current	A/m^2	0.0
	electron/hole diffusion length	m	2.0e-6
ec0	voltage dependent parameter for recombination current	V	0.0
ın0	voltage dependent parameter for tunneling current	V	0.0
jt	power coefficient of channel length dependency for bipolar current		1.0
t0	channel length for bipolar current	m	0.2e-6
f0	channel length dependency coefficient of diffusion cap		1.0
ojt	early voltage for bipolar current	V	10.0

alculated parameter

Table 5-5. BSIM3SOI Parameters (continued)

rameter	Description	Units	Default
ly	channel length dependency of early voltage for bipolar current	V/m	10.0
li	high level injection parameter for bipolar current		0.0
ody	intrinsic body sheet resistance	Ohm/m^2	0.0
sh	extrinsic body sheet resistance	Ohm/m^2	0.0
eo	capacitance per unit channel length	F/m	0/0
	diffusion capacitance transit time coefficient	s	1.0e-12
if	power coefficient of channel length dependency for diffusion capacitance		-1.0
dfb	capacitance flatband voltage	V	†
dth	capacitance threshold voltage	V	†
dmin	source/drain bottom diffusion minimum capacitance	F	†
d	source/drain bottom diffusion smoothing parameter		0.3
esw	source/drain sidewall fringing capacitance per unit channel length	F/m	0/0
ecf	temperature coefficient for Ncref		0.0
ecr	temperature coefficient for Ncrer		0.0
cb	length offset fitting parameter for body charge	m	Lint
ody	scaling factor for body charge		1.0
jswg	temperature coefficient of Cjswg	K^-1	0.0
bswg	temperature coefficient of Pbswg	V/K	0.0
de	exponential coefficient for finite charge thickness	m/V	1.0
in	coefficient for gate-bias dependent surface potential	V^(1/2)	15.0

alculated parameter

Table 5-5. BSIM3SOI Parameters (continued)

rameter	Description	Units	Default
lvt	threshold voltage adjust for CV, V		0.0
1	coefficient of Vbs0 dependency on Ves		1.0
)g	length offset fitting parameter for backgate charge	m	0.0
(qm	effective oxide thickness considering quantum effect	m	Tox
h0	minimum width for thermal resistance calculation	m	0.0
ıalo	Body halo sheet resistance	Ohms	1.0e15
ox	power term of gate current		1.0
xref	target oxide thickness	m	2.5e-9
)g	effective bandgap in gate current calculation	V	1.2
evb	valence-band electron non-ideality factor	V	3.0
ohagb1	first Vox dependent parameter for gate current in inversion		0.35
etagb2	second Vox dependent parameter for gate current in inversion		0.03
gb1	third Vox dependent parameter for gate current in inversion		300.0
ecb	condition-band electron non-ideality factor		1.0
phagb2	first Vox dependent parameter for gate current in accumulation		0.43
etagb2	second Vox dependent parameter for gate current in accumulation		0.05
gb2	third Vox dependent parameter for gate current in accumulation		17.0

Calculated parameter

Table 5-5. BSIM3SOI Parameters (continued)

rameter	Description	Units	Default
xh	limit of Vox in gate current calculation	V	5.0
ltavox	Smoothing parameter in the Vox smoothing function	V	0.005
alculated parameter			

tes

1. BSIMSOI is a deep submicron, silicon-on-insulator MOSFET device model for SPICE engines. it is developed by the BSIM Group under the direction of Professor Chenming Hu in the Department of Electrical Engineering and Computer Sciences at the University of California, Berkeley. BSIMSOI is closely related to the industry standard bulk MOSFET model, BSIM.
2. BSIMDP2.2 is the new version of the Partial Depletion SOI MOSFET model, BSIMPD2.2. The gate-body tunneling (substrate current) is added in this release to enhance the model accuracy. BSIMDP2.2 information can be found on the BSIMSOI website (*http://www-device.eecs.berkeley.edu/~bsimsoi*).

;IM3 Silicon On Insulator Transistor, Floating Body (NMOS and PMOS)

IM3SOI_NMOS (BSIM3 SOI Transistor (Floating Body), NMOS
IM3SOI_PMOS (BSIM3 SOI Transistor (Floating Body), PMOS,)

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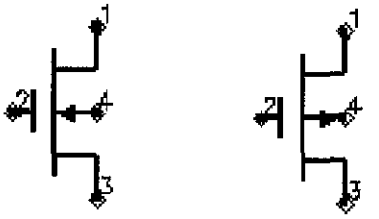

'ameters

del parameters must be specified in SI units

del =model instance name

ıgth =channel length in um, mm, cm, meter, mil, or in (default: 5.0e-6)

ɪth = channel width in um, mm, cm, meter, mil, or in (default: 5.0e-6)

= area of drain diffusion, in m^2 (default: 0.0)

=area of source diffusion, in m^2 (default: 0.0)

= perimeter of the drain junction, in m (default: 0.0)

=perimeter of the drain junction, in m (default: 0.0)

ɪ = number of squares of the drain diffusion (default: 1.0)

; =number of squares of the source diffusion (default: 1.0)

› = number of squares in body (default:1.0)

›ff = BJT on/off flag (yes = 1, no = 0; default: no)

ı0 = instance thermal resistance in Ohms (default: model Rth0)

ı0 =instance thermal resistance in F (default: model Cth0)

: = number of body contact insulation edge (default: 0.0)

:g = number segments for width partitioning (default: 1.0)

›cp =perimter length for bc parasitics at drain side (default: 0.0)

ıcp =perimter length for bc parasitics at source side (default: 0.0)

bcp = gate to body overlap area for bc parasitics, in m^2 (default: 0.0)

bcp =substrate to body overlap area for bc parasitics, in m^2 (default: 0.0)

susr = Vbs specified by the user, in V (default: Vbs)

mp = device operating temperature, Celsius (default: 25.0)

ode = simulation mode for this device (default: nonlinear)

ise =noise generation option (yes = 1, no = 0; default: yes)

l = number of devices in parallel (default: 1)

VEL3_Model (MOSFET Level-3 Model)

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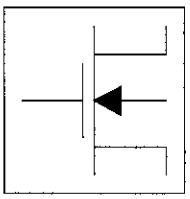


ameters

del parameters must be specified in SI units.

Table 5-9. LEVEL3_Model Parameters

rameter	Description	Unit	Default
MOS	N-channel model		yes
MOS	P-channel model		no
smod	IDS model		3
pmod	capacitance model selector		1
o†	zero-bias threshold voltage	V	0.0
)†	transconductance coefficient	A/V^2	2×10^{-5}
mma	bulk threshold	$\sqrt{V}$	0.0
i†	surface potential	V	0.6
l	drain ohmic resistance	ohms	0.0
	source ohmic resistance	ohms	0.0
d†	zero-bias bulk-drain junction capacitance	F	0.0
s†	zero-bias bulk-source junction capacitance	F	0.0
	bulk junction saturation current	A	10^{-14}
†	bulk junction potential	V	0.8
so	gate-source overlap capacitance per meter of channel width	F/m	0.0

arameter value varies with temperature based on Tnom of model and Temp of vice.

Value of 0.0 is interpreted as infinity.

Table 5-9. LEVEL3_Model Parameters (continued)

rameter	Description	Unit	Default
;do	gate-drain overlap capacitance per meter of channel width	F/m	0.0
;bo	gate-bulk overlap capacitance per meter of channel length	F/m	0.0
h	drain and source diffusion sheet resistance	ohms/sq	0.0
†	zero-bias bulk junction bottom capacitance per square meter of junction area	F/m^2	0.0
j	bulk junction bottom grading coefficient		0.5
sw†	zero-bias bulk junction periphery capacitance per meter of junction perimeter	F/m	0.0
jsw	bulk junction periphery grading coefficient		0.33
†	bulk junction saturation current per square meter of junction area	A/m^2	0.0
x	oxide thickness	m	10^{-7}
;ub	substrate (bulk) doping density	$1/cm^3$	0.0
;s	surface state density	$1/cm^2$	0.0
's	fast surface state density	$1/cm^2$	0.0
)g	gate material type: 0=aluminum; −1=same as substrate; 1=opposite substrate		1
	metallurgical junction depth	m	0.0
l	lateral diffusion length	m	0.0
)†	surface mobility	$cm^2/(V \times s)$	600.0
nax	carriers maximum drift velocity	m/s	0.0
]c	coefficient of channel charge share		1.0
ev	Noise model level		-1

Parameter value varies with temperature based on Tnom of model and Temp of vice.

Value of 0.0 is interpreted as infinity.

Table 5-9. LEVEL3_Model Parameters (continued)

·ameter	Description	Unit	Default
lwnoi	Drain noise parameters for Nlev=3		1
	flicker noise coefficient		0.0
	flicker noise exponent		1.0
	bulk junction forward-bias depletion capacitance coefficient		0.5
lta	width effect on threshold voltage		0.0
eta	mobility modulation	1/V	0.0
a	static feedback		0.0
ıppa	saturation field factor		0.2
	gate ohmic resistance	ohms	0.0
ls	drain-source shunt resistance	ohms	infinity††
ıom	nominal ambient temperature at which these model parameters were derived	°C	25
	bulk P-N emission coefficient		1.0
	bulk P-N transit time	sec	0.0
e	Flicker noise frequency exponent		1.0
ıax	explosion current	A	10.0
/subfwd	substrate junction forward bias (warning)	V	infinite
3vsub	substrate junction reverse breakdown voltage (warning)	V	infinite
3vg	gate oxide breakdown voltage (warning)	V	infinite
3vds	drain-source breakdown voltage (warning)	V	infinite
dsmax	maximum drain-source current (warning)	A	infinite
³max	maximum power dissipation (warning)	W	infinite
lParams	DataAccessComponent-based parameters		

³arameter value varies with temperature based on Tnom of model and Temp of vice.

Value of 0.0 is interpreted as infinity.

es/Equations/References

1. The simulator provides three MOSFET device models that differ in formulation of I-V characteristics. LEVEL3_Model is a semi-empirical model derived from [1].

2. LEVEL3_Model includes second order effects such as threshold voltage shift, mobility reduction, velocity saturation, channel length modulation, and subthreshold conduction.

3. Parameters Vto, Kp, Gamma, Phi, and Lambda determine the dc characteristics of a MOSFET device. Program will compute these parameters (except Lambda) if, instead of specifying them, you specify the process parameters Tox, Uo, Nsub, and Nss.

4. Vto is positive (negative) for enhancement mode and negative (positive) for depletion mode N-channel (P-channel) devices.

5. The p-n junctions between the bulk and the drain and the bulk and the source are modeled by parasitic diodes. Each bottom junction is modeled by a diode and each periphery junction is modeled by a depletion capacitance.

6. The diode parameters for the bottom junctions can be specified as absolute values (Is, Cbd and Cbs) or as per unit junction area values (Js and Cj).

   If Cbd=0.0 and Cbs=0.0, Cbd and Cbs will be computed:

   $Cbd = Cj \times Ad \qquad Cbs = Cj \times As$

   If Js>0.0 and Ad>0.0 and As>0.0, Is for drain and source will be computed:

   $Is(drain) = Js \times Ad \qquad Is(source) = Js \times As$

   Drain and source ohmic resistances can be specified as absolute values (Rd, Rs) or as per unit square value (Rsh).

   If Nrd≠0.0 or Nrs≠0.0, Rd and Rs will be computed:

   $Rd = Rsh \times Nrd \qquad Rs = Rsh \times Nrs$

7. Charge storage in the MOSFET consists of capacitances associated with parasitics and intrinsic device.

   The parasitic capacitances consist of three constant overlap capacitances (Cgdo, Cgso, Cgbo) and the depletion layer capacitances for both substrate junctions (divided into bottom and periphery) that vary as Mj and Mjsw power of junction

voltage, respectively, and are determined by the parameters Cbd, Cbs, Cj, Cjsw, Mj, Mjsw, Pb and Fc.

The intrinsic capacitances consist of the nonlinear thin-oxide capacitance, which is distributed among the gate, drain, source, and bulk regions.

3. Charge storage is modeled by fixed and nonlinear gate and junction capacitances. MOS gate capacitances, as a nonlinear function of terminal voltages, are modeled by Meyer's piece-wise linear model for levels 1, 2, and 3. The Ward charge conservation model is also available for levels 2 and 3, by specifying the XQC parameter to a value smaller than or equal to 0.5. For Level 1, the model parameter TOX must be specified to invoke the Meyer model when Capmod is equal to 1 (default value). If Capmod = 0, no gate capacitances will be computed. If Capmod = 2, a smooth version of the Meyer model is used. If Capmod =3, the charge conserving first-order MOS charge model [2] that was used in Libra is used.

9. Use AllParams with a DataAccessComponent to specify file-based parameters (refer to DataAccessComponent). Note that model parameters that are explicitly specified take precedence over those specified via AllParams. Set AllParams to the DataAccessComponent instance name.

nperature Scaling

model specifies Tnom, the nominal temperature at which the model parameters e calculated or extracted. To simulate the device at temperatures other than m, several model parameters must be scaled with temperature. The temperature hich the device is simulated is specified by the device item Temp parameter. nperatures in the following equations are in Kelvin.)

depletion capacitances Cbd, Cbs, Cj, and Cjsw vary as:

$$Cbd^{NEW} = Cbd\left[\frac{1 + Mj[4\times 10^{-4}(Temp - T_{REF}) - \gamma^{Temp}]}{1 + Mj[4\times 10^{-4}(Tnom - T_{REF}) - \gamma^{Temp}]}\right]$$

$$Cbs^{NEW} = Cbs\left[\frac{1 + Mj[4\times 10^{-4}(Temp - T_{REF}) - \gamma^{Temp}]}{1 + Mj[4\times 10^{-4}(Tnom - T_{REF}) - \gamma^{Temp}]}\right]$$

$$Cj^{NEW} = Cj\left[\frac{1 + Mj[4\times10^{-4}(Temp - T_{REF}) - \gamma^{Temp}]}{1 + Mj[4\times10^{-4}(Tnom - T_{REF}) - \gamma^{Temp}]}\right]$$

$$Cjsw^{NEW} = Cjsw\left[\frac{1 + Mjsw[4\times10^{-4}(Temp - T_{REF}) - \gamma^{Temp}]}{1 + Mjsw[4\times10^{-4}(Tnom - T_{REF}) - \gamma^{Temp}]}\right]$$

vhere γ is a function of the junction potential and the energy gap variation with emperature.

: surface potential Phi and the bulk junction potential Pb vary as:

$$Phi^{NEW} = \frac{Temp}{Tnom}\times Phi + \frac{2k\times Temp}{q}ln\left(\frac{n_i^{Tnom}}{n_i^{Temp}}\right)$$

$$Pb^{NEW} = \frac{Temp}{Tnom}\times Pb + \frac{2k\times Temp}{q}ln\left(\frac{n_i^{Tnom}}{n_i^{Temp}}\right)$$

: transconductance Kp and mobility Uo vary as:

$$Kp^{NEW} = Kp\left(\frac{Temp}{Tnom}\right)^{3/2}$$

$$Uo^{NEW} = Uo\left(\frac{Temp}{Tnom}\right)^{3/2}$$

: source and drain to substrate leakage currents Is and Js vary as:

$$Is^{NEW} = Is\times exp\left(\frac{q\times E_G^{Tnom}}{k\times Tnom} - \frac{q\times E_G^{Temp}}{k\times Temp}\right)$$

$$Js^{NEW} = Js\times exp\left(\frac{q\times E_G^{Tnom}}{k\times Tnom} - \frac{q\times E_G^{Temp}}{k\times Temp}\right)$$

vhere E_G is the silicon bandgap energy as a function of temperature.

: MOSFET threshold voltage variation with temperature is given by:

$$Vto^{NEW} = Vto + \gamma\left(\sqrt{Phi^{NEW}} - \sqrt{Phi}\right) + \frac{Phi^{NEW} - Phi}{2} - \frac{E_G^{Temp} - E_G^{Tnom}}{2}$$

ise Model

ırmal noise generated by resistor Rg, Rs, Rd, and Rds is characterized by the ɔwing spectral density:

$$\frac{< i^2 >}{\Delta f} = \frac{4kT}{R}$$

ınnel noise and flicker noise (Kf, Af, Ffe) generated by dc transconductance g_m and ɾent flow from drain to source is characterized by the spectral density:

$$\frac{< i_{ds}^2 >}{\Delta f} = \frac{8kTg_m}{3} + k_f \frac{I_{DS}^{a_f}}{f^{f_{fe}}}$$

he preceding expressions, *k* is Boltzmann's constant, *T* is the operating ıperature in Kelvin, *q* is the electron charge, *kf*, *af*, and *ffe* are model parameters, *f* ıe simulation frequency, and Δf is the noise bandwidth.

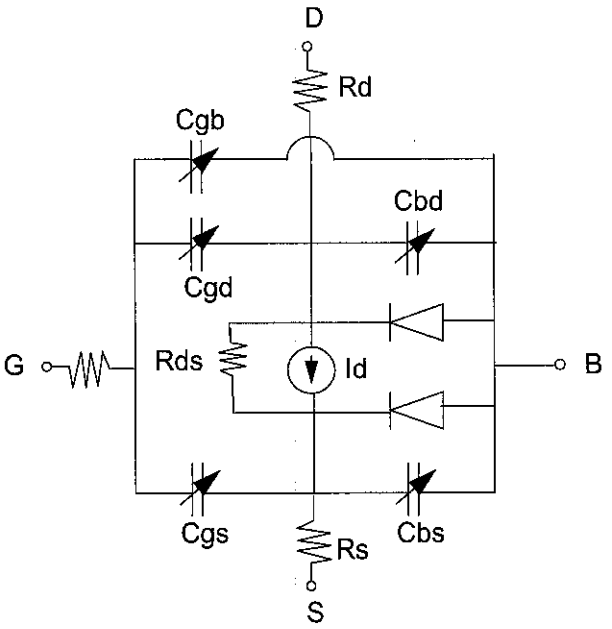
erences

1] Vladimirescu, and S. Liu. The Simulation of MOS Integrated Circuits Using SPICE2, Memorandum No. M80/7, February 1980.

2] Karen A. Sakallah, Yao-tsung Yen, and Steve S. Greenberg. "The Meyer Model Revisited: Explaining and Correcting the Charge Non-Conservation Problem," *ICCAD*, 1987.

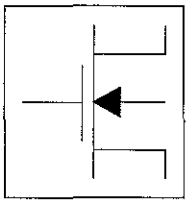
3] P. Antognetti and G. Massobrio. *Semiconductor device modeling with SPICE*, New York: McGraw-Hill, Second Edition 1993.

ıivalent Circuit



VEL3_MOD_Model (LEVEL 3 NMOD MOSFET Model)

nbol



ameters

del parameters must be specified in SI units.

Table 5-10. LEVEL3_MOD_Model Parameters

ımeter	Description	Unit	Default
OS	N-channel model		yes
OS	P-channel model		no
nod	IDS model		6
mod	capacitance model selector		1
†	zero-bias threshold voltage	V	0.0
	transconductance coefficient	A/V^2	0.0
nma	bulk threshold parameter	$\sqrt{V}$	0.0
nma2	bulk threshold parameter deep in substrate	$\sqrt{V}$	0.0
a	mobility modulation with substrate bias parameter		0.0
†	surface potential	V	0.6
	drain ohmic resistance	ohms	0.0
	source ohmic resistance	ohms	0.0
†	zero-bias bulk-drain junction capacitance	F	0.0
†	zero-bias bulk-source junction capacitance	F	0.0
	bulk junction saturation current	A	10^{-14}
	bulk junction potential	V	0.8

rameter value varies with temperature based on Tnom of model and Temp of ice.

alue of 0.0 is interpreted as infinity.

Table 5-10. LEVEL3_MOD_Model Parameters (continued)

ımeter	Description	Unit	Default
o	gate-source overlap cap. per meter of channel width	F/m	0.0
lo	gate-drain overlap cap. per meter of channel width	F/m	0.0
ıo	gate-bulk overlap cap. per meter of channel length	F/m	0.0
ı	drain and source diffusion sheet resistance	ohms/sq.	0.0
	zero-bias bulk junction bottom capacitance per square meter of junction area	F/m^2	0.0
	bulk junction bottom grading coefficient		0.5
w†	zero-bias bulk junction periphery capacitance per meter of junction perimeter	F/m	0.0
w	bulk junction periphery grading coefficient		0.33
	bulk junction saturation current per square meter of junction area	A/m^2	0.0
	oxide thickness	m	10^{-7}
ıb	substrate (bulk) doping density	$1/cm^3$	0.0
	surface state density	$1/cm^2$	0.0
	fast surface state density	$1/cm^2$	0.0
;	gate material type: 0=aluminum; -1=same as substrate; 1=opposite substrate		1
	metallurgical junction depth	m	0.0
	lateral diffusion length	m	0.0
	surface mobility	$cm^2/(V\times S)$	600.0
it	critical field for mobility degradation	V/cm	10^{-4}
;p	field exponent in mobility degradation		0.0
ax	carriers maximum drift velocity	m/s	0.0
	coefficient of channel charge share		1.0

ırameter value varies with temperature based on Tnom of model and Temp of ice.

'alue of 0.0 is interpreted as infinity.

Table 5-10. LEVEL3_MOD_Model Parameters (continued)

ımeter	Description	Unit	Default
	flicker noise coefficient		0.0
	flicker noise exponent		1.0
	bulk junction forward-bias depletion cap. coefficient		0.5
ta	width effect on threshold voltage		0.0
ɛta	mobility modulation	1/V	0.0
ı	static feedback		0.0
ɔpa	saturation field factor		0.2
ɔpag	field correction factor gate drive dependence		0.0
.u	subthreshold fitting model parameter for NMOD		1.0
	gate resistance	ohms	0.0
;	drain-source shunt resistance	ohms	infinity††
ɔm	nominal ambient temperature at which these model parameters were derived	C	25
	bulk P-N emission coefficient		1.0
	bulk P-N transit time	sec	0.0
:	flicker noise frequency exponent		1.0
ax	explosion current	A	10.0
'subfwd	substrate junction forward bias (warning)	V	infinite
;vsub	substrate junction reverse breakdown voltage (warning)	V	infinite
;vg	gate oxide breakdown voltage (warning)	V	infinite
;vds	drain-source breakdown voltage (warning)	V	infinite
idsmax	maximum drain-source current (warning)	A	infinite
'max	maximum power dissipation (warning)	W	infinite
Params	DataAccessComponent-based parameters		

arameter value varies with temperature based on Tnom of model and Temp of vice.

Value of 0.0 is interpreted as infinity.

:s/Equations/References

. LEVEL3_MOD_Model is an enhanced version of the SPICE level 3 model. It exhibits smooth and continuous transitions in the weak to strong inversion region, and in the region between linear and saturation modes of device operation.

. Use AllParams with a DataAccessComponent to specify file-based parameters (refer to DataAccessComponent). Note that model parameters that are explicitly specified take precedence over those specified via AllParams. Set AllParams to the DataAccessComponent instance name.