Synchronization and Delay Techniques for Driving 1MHz Totem-Poled Power MOSFET Configuration

By

Nurazlin binti Zakaria

Project dissertation in partial fulfilment of
the requirements for the
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Universiti Teknologi PETRONAS
Bandar Seri Iskandar
31750 Tronoh
Perak Darul Ridzuan

CERTIFICATION OF APPROVAL

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Approved by:

.....

(Ms. Khairul Nisak Md Hasan)
Project Supervisor

UNIVERSITI TEKNOLOGI PETRONAS
TRONOH, PERAK
JUNE 2010

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

.....

(NURAZLIN BINTI ZAKARIA)

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ABSTRACT

This project discusses about the synchronization and delay techniques that are suitable for totem-poled power MOSFET configuration operating at high speed. Modification has been made to the proposed synchronization circuit for earlier PWM controllers that have an operating frequency ranging from 80 kHz to 120 kHz. Experimentation is carried out to obtain the most suitable means in synchronizing the PWM signals and adding delay function. The synchronization and delay network is able to operate at high switching frequency of 1 MHz. In addition, two different sets of complementary square-wave are achieved at duty cycle of 50 % and 20 %. The result with 20 % duty cycle can be used for previous work in investigation of high frequency effects on soft switch-switched synchronous rectifier buck converter.

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CHAPTER 1

INTRODUCTION

1.1 Background of Study

In the ever advancing technology of power electronics, the use of power MOSFET has been substantial in any electronic switching mechanism [1]. To meet with the current trend of fast and efficient operation of the devices, the electronic circuit must operate at high frequency. In order to operate a totem-poled power MOSFET configuration, it is important to first understand each aspect and characteristic of the synchronization and delay techniques. The synchronization circuit performance is studied to investigate the limitations when the network is conducted at high frequency of 1MHz. The delay method is applied to ensure the switching operation works alternately so that there will only be one switch working at a time. To establish better understanding and to improve the methods available in recent days, more research and experimentation was carried out and to be discussed in this work.

A few examples and applications of the totem-poled power MOSFET configuration is for the resonant gate driver (RGD) [2], power electronics DC-DC buck converter [3], and high-speed pulse amplifier. Therefore, this work is proposed for [2] whereby the paper discusses RGD circuit operating at high frequency.

1.2 Problem Statement

With rapid growth of low power application in chip base circuitry, the synchronization and delay techniques were chosen for experimentation work on board. The idea is to get a better insight on how the synchronization circuit and delay circuit to be conducted on board. Performing experimentation using chip is no doubt a simpler way to obtain expected result with required parameters. However, not all chip's operation available has the exact feature needed for experimentation work. Therefore, by constructing a customized circuit will be useful for future reference as one of the option to operate a totem-poled power MOSFET configuration at high frequency. It is an advantage to construct the network based on the preferred parameters and understand the circuit's operation.

In order to achieve high efficiency in high switching of 1MHz in applications such as a resonant gate driver, all possible limitations should be taken into account. In switching mechanism for a totem-poled MOSFET configuration, the switching loss is inevitable [2]. In order to reduce the switching loss, optimization of the switching operation is important to improve its efficiency.

In this project, two pulse width modulations (PWM) signal is used as a mean of digital signal input for the totem-poled MOSFET. The synchronization technique is expected to synchronize the PWM signals. This is because in a digital switching, the starting time of the digital input is unknown. The target is to ensure both PWM signals starting time is at zero ($t = 0$). In basic operation of a power converter, PWM signal is generated at a 50% duty cycle. Delay function is applied to one of the signals whereby the both of the signals operation will work alternately. The purpose of doing so is to make the switching operation of the totem-poled MOSFET will not overlap [2]. Therefore experimentations are carried out to obtain the best method in synchronizing and delaying the PWM

signals for a totem-poled MOSFET configuration to optimize its switching operation thus improve the power converter circuit operation.

1.3 Objectives

The objective of this study is to explain the related knowledge and theories and put into practice in the experimentation work. The aim is to improve the switching operation of a totem-poled MOSFET configuration in a power converter circuit for example a resonant gate driver. In order to achieve the objective, a synchronization and delay network needs to be designed properly. The purpose is to run experimentation and investigate the best technique for synchronizing and delaying the PWM signals. This can substantially increase the efficiency of the converter circuit when operating at high frequency of 1MHz [2]. The features of the synchronization and delay circuit should maximize power stage efficiency.

1.4 Scope of Studies

The interest of this scope of study is to explore possible methods in synchronizing and adding delay function to PWM signals operating at 1MHz. The scope of study includes the implementation of synchronization circuit and time delay circuit using timer chip. Therefore it is significant to understand and study the operation of synchronization and delay circuit. This is to investigate the most suitable implementation of synchronization and delay method.

Furthermore, limitations and restrictions in performing the project in high frequency operation should be put into considerations otherwise it would affect the network's performance. In general, performing experimentation on board with

the circuit's operating at high frequency will produce an inevitable switching loss in its switching mechanism.

In conceptual and theory, all information related to synchronizing and delaying the PWM signals was gathered and revised. Experimentation is carried out to verify that the network configuration proposed is suitable and could perform efficiently for the totem-poled MOSFET switching configuration. Throughout the experimentation, results are recorded, analyzed and further discussed. Hence, the overall performance assessment can provide verification that the network is suitable.

There are various kinds of power MOSFET gate drive chips available in recent days. Normally the commercial gate drivers have a similar circuit configuration: a "Totem-Pole" structure, whereby the drain terminal of a N-channel MOSFET, Q_1 is connected to the drain of an N-channel MOSFET, Q_2 [4]. An example of the totem-poled MOSFET configuration can be seen below. Figure 1 shows the circuit diagram of a conventional gate driver and the power MOSFET being driven.

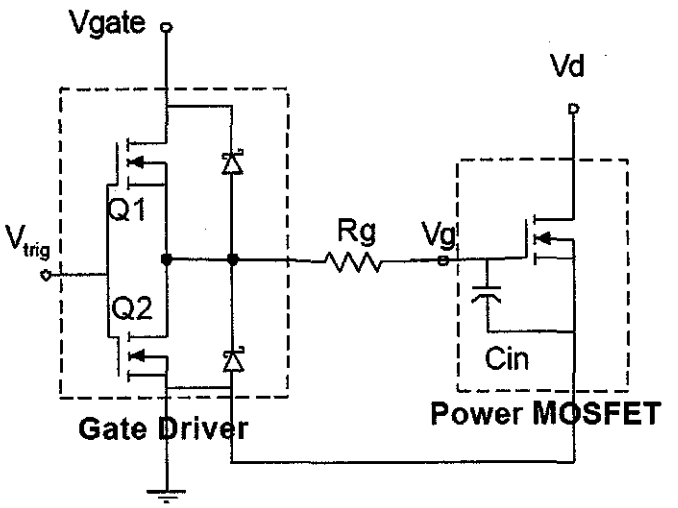

Figure 1: Totem-Poled configuration at the gate driver circuit.

CHAPTER 2

LITERATURE REVIEW

2.1 Signal Characteristics

Pulse Width Modulation (PWM) is a very efficient way of providing intermediate amounts of electrical power between swithcing operation during fully on and fully off. PWM has several advantages in normal switching method [5]. A simple power switch with a typical power source provides full power only, when switched on. PWM is a comparatively-recent technique, made practical by modern electronic power switches.

Pulse width modulation is used to reduce the total power delivered to a load thus provides lesser power loss during switching, which normally occurs when a power source is limited by a resistive element. This results in a faster switching whereby it is suitable for high frequency circuit applications. The underlying principle in the whole process is that the average power delivered is directly proportional to the modulation duty cycle [3]. In addition, the cost of the circuit construction is relatively low as the devices needed is lesser therefore the circuit construction is simpler with the use of semiconductor switches and devices.

To power up the MOSFET switches properly, it is required the PWM signals to be generated at a fixed duty cycle. In order to achieve this, the equal-

pulse (uniform) PWM technique or also known as the single-pulse PWM control is generated [3]. In generating equal pulse widths, the square reference voltage waveform, *Vref* is compared to a triangular control (carrier) voltage waveform as shown in Figure 2 below:

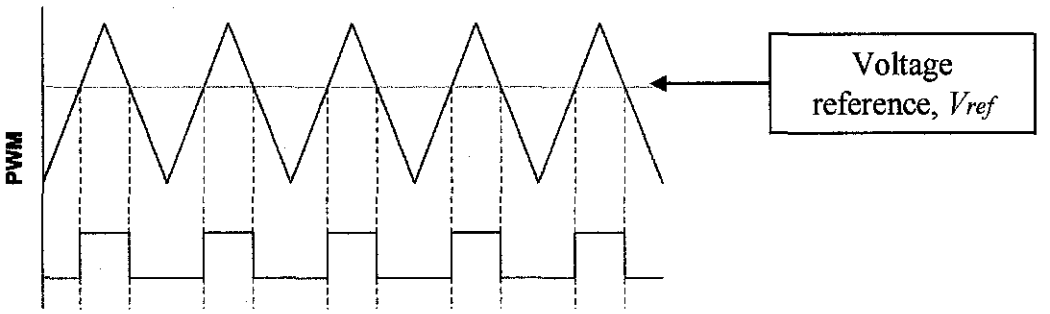

Figure 2: Typical waveform of PWM signal with fixed duty cycle.

Since this work requires PWM with fixed duty cycle, thus a DC level is used as the voltage reference, *Vref*. The PWM signal is required to demonstrate a smooth signal when generated at high frequency of 1 MHz.

The circuit configuration for the PWM signals generated is shown in Figure 3. This PWM generator is capable in producing a 1MHz PWM signal. However it is difficult to precisely tune the circuit configuration to obtain 1MHz precisely. This is because ripple voltages takes place when the circuit operates at high speed operation [6].

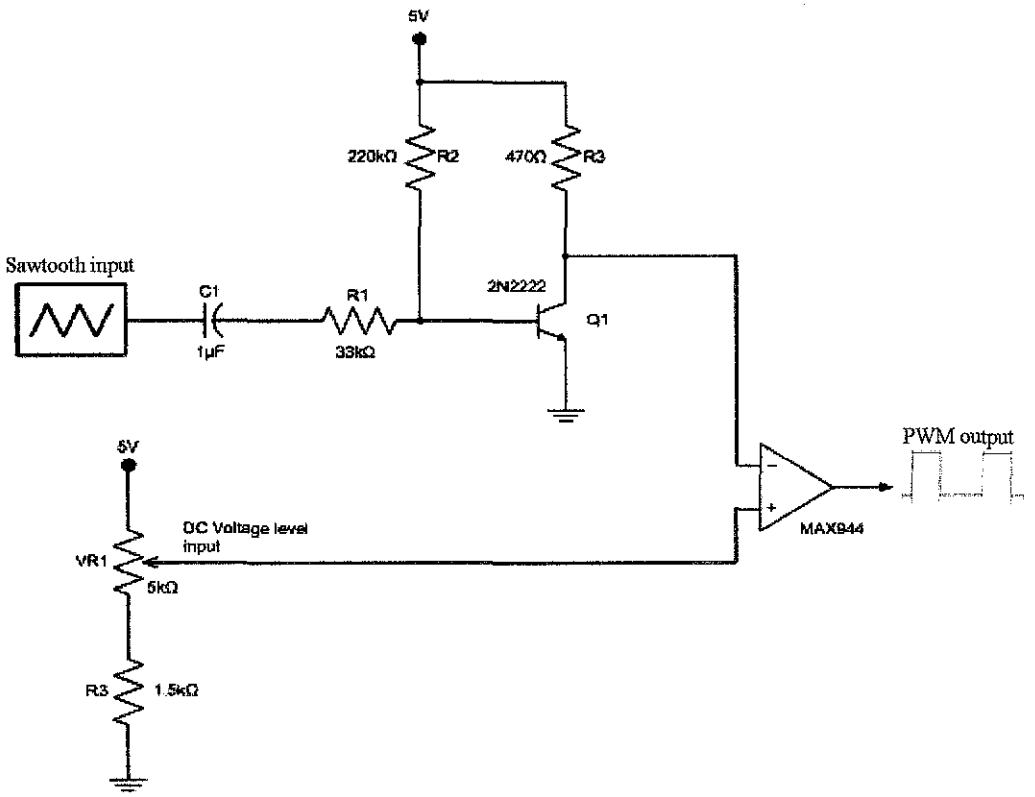

Figure 3: Voltage controlled PWM generator.

2.2 Synchronization of Two PWM Signals

The significant of a synchronization circuit is for synchronizing at least two pulse widths. In other words, the signals occurrence is at the same time or at the same rate or with a regular time relationship. The signals are expected to operate at common timing signals [7].

The two PWM signal needs to be synchronized in order to obtain the correct signal that operates 'ON' and 'OFF' alternately with a zero voltage switching (ZVS) attribute [2]. In able to achieve this target, there are few techniques practiced in recent years. Based on research, conventionally synchronous circuit can be constructed using timer circuit.

There were few synchronous circuits that had been proposed to generate a controlled and synchronized by periodic pulses of the clock used depending on the parameters required for the synchronized output signals.

In synchronous circuits, the inputs are pulses (or levels and pulses) with certain restrictions on pulse width and circuit propagation delay. Therefore synchronous circuits can be divided into ***clocked*** sequential circuits and ***uncklocked*** or ***pulsed*** sequential circuits [8].

The work is mainly based on generating synchronized PWM signals via verification on the experimentation carried out using general purpose timer. Referring to the datasheet [9], the general purpose timers specifically utilize CMOS RC timers providing significantly improved performance over the standard 355 timers. Improved parameters include low supply current, wide operation supply voltage range, low THRESHOLD, TRIGGER and RESET currents, no crowbarring of the supply current during output transitions, higher frequency performance and no requirement to decouple CONTROL VOLTAGE for stable operation [9].

Another way to generate synchronized signals is by applying below configuration. Figure 4 is a block diagram of a pulse generator comprising a D-type flip flop (labeled 31), a latch pulse generator (labeled 32), a gate pulse generator (labeled 33), and an AND gate (labeled 34). The operation of this synchronization circuit is developed by applying a low bit rate frame pulse signal generated by the detector [see Appendix A] is applied to the data input terminal D in the D-type flip-flop (labeled 31). The clock signal CLK1 is applied to the input terminal of the latch pulse generating circuit (labeled 32), which derives a latch pulse signal applied to a clock terminal CLK of the flip-flop (labeled 31) [10].

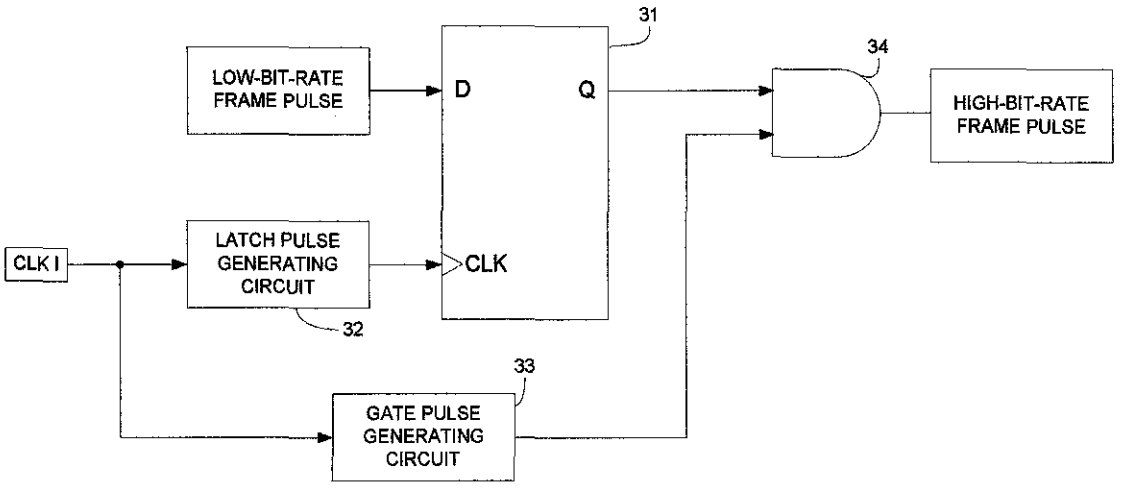

Figure 4: A block diagram of a pulse generator..

Referring to Figure 5, the first clock signal CLK1 is applied to the gate pulse generator which generates a gate pulse signal illustrated in (E). The waveform of each pulses illustrate the gate pulse signal rises in synchronism with the rise of each pulse of second clock signal CLK2 (see Appendix A), and the pulse width equal to the first clock signal CLK1. The gate pulse signal generated by the gate pulse generator (labeled 33) is applied to the AND gate (labeled 34). The output signal of the flip-flop (labeled 31) is shown in (E) whereby it is generated by its output terminal Q is applied to the AND gate (labeled 34). The AND gate executes a logical AND operation on the signals depicted in (E) and (F) IN Figure 4. It also generates the high bit-rate frame pulse signal as shown in (G). As shown in (A), the first clock signal CLK1 is a rectangular wave signal. Each one byte of the input data is illustrated in (C). The input data is synchronized with the first clock signal CLK1 [10].

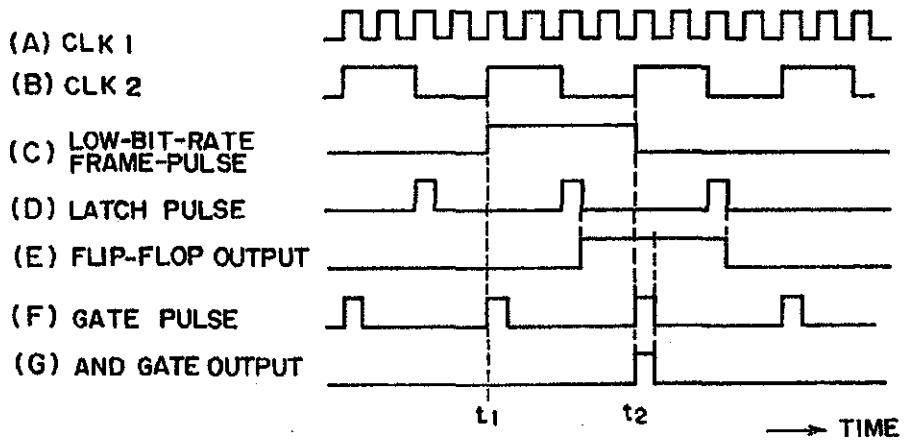

Figure 5: A timing chart showing the operation of the pulse generator in Figure 4 [10].

Above application is applied to establish a frame synchronism using pointers in a digital transmission system. Nonetheless, the general idea on how to achieve synchronism can be further studied to acquire a better understanding and greater vision on how it works.

In an integrated system design, the principle behind a synchronous circuit is that everything is triggered by the same clock [11]. Thus the processing and data management block together with the state machine are all running on the same single clock. However purpose of the project is to apply the synchronization and delay techniques for power converters comprising of a totem-poled MOSFET switching configuration. Therefore, only few synchronization and delay techniques suitable for the experimentation work.

The synchronization of earlier PWM controllers (eg UC3842) has usually been implemented by applying a pulse to the timing capacitor that results in the reset of the timing capacitor voltage. This occurrence is forced to happen earlier in the cycle that would naturally occur. The consequence is a significant decrease in the ramp amplitude and affects the gain of the voltage controlled feedback loop.

Some newer controllers provide a synchronization pin. This is to terminate the ramp waveform and reduce the effective ramp amplitude. The ramp can be reduced up to 50% by this method [12].

Figure 6 shows a synchronization circuit proposed for an UCC28517 [12] which is a power converter controller. Though this circuit was developed for controllers that had internal timing capacitors and no synchronization pin, it can be used for almost any converter. The circuit uses a buffered ramp as an input, however any signal that indicates the frequency of the internal converter can be used.

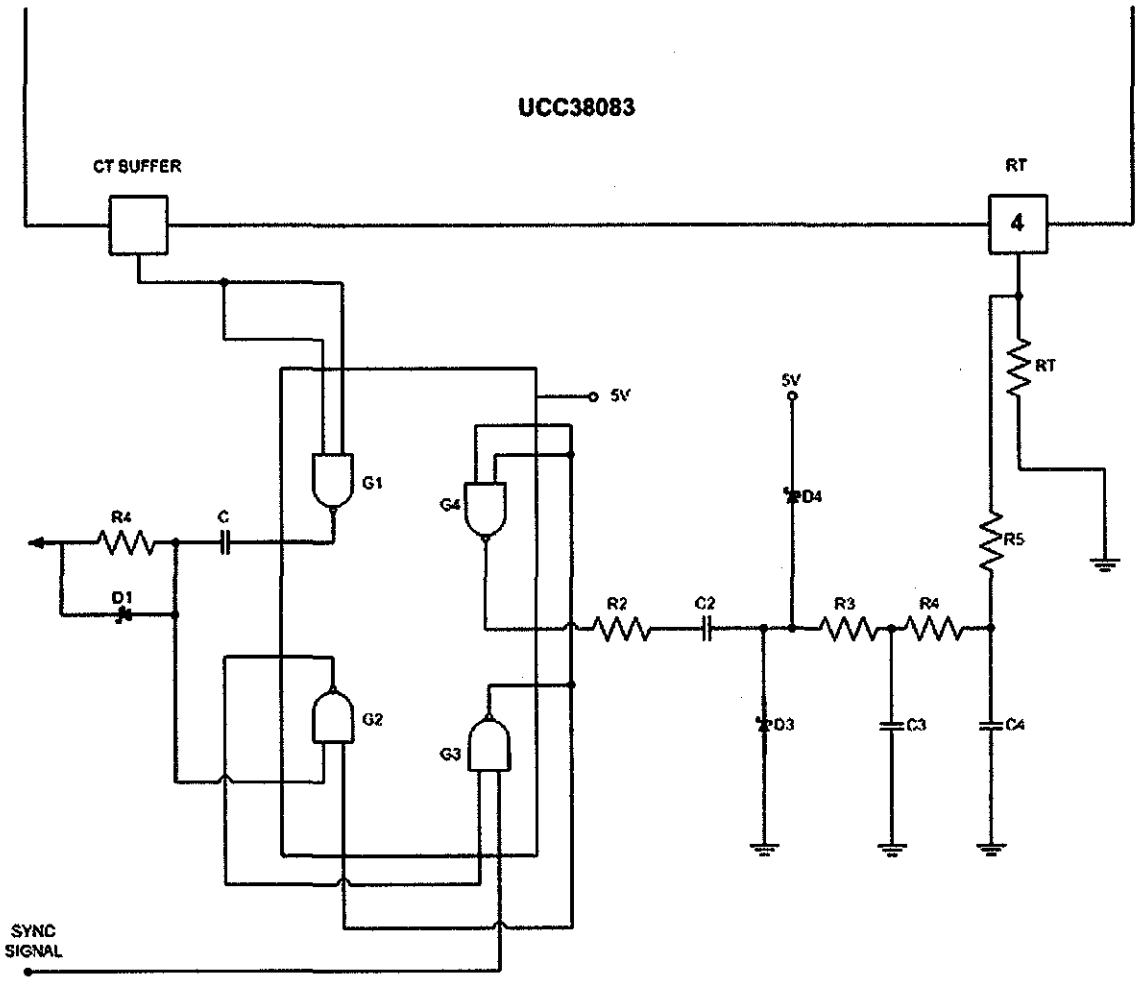

Figure 6: Synchronization Circuit for the UCC 28517.

The circuit operation was found to be able to operate at frequency range of 80 kHz to 120 kHz. Therefore the circuit needs to be modified in order to satisfy the circuit operation in high frequency of 1 MHz. Referring to Figure 7, G4 indicates the output signal from the NAND gate network. The output from G4 is illustrated in Figure 7 where both figures contain the ramp voltage as the top trace. The bottom trace is the incoming synchronization signal.

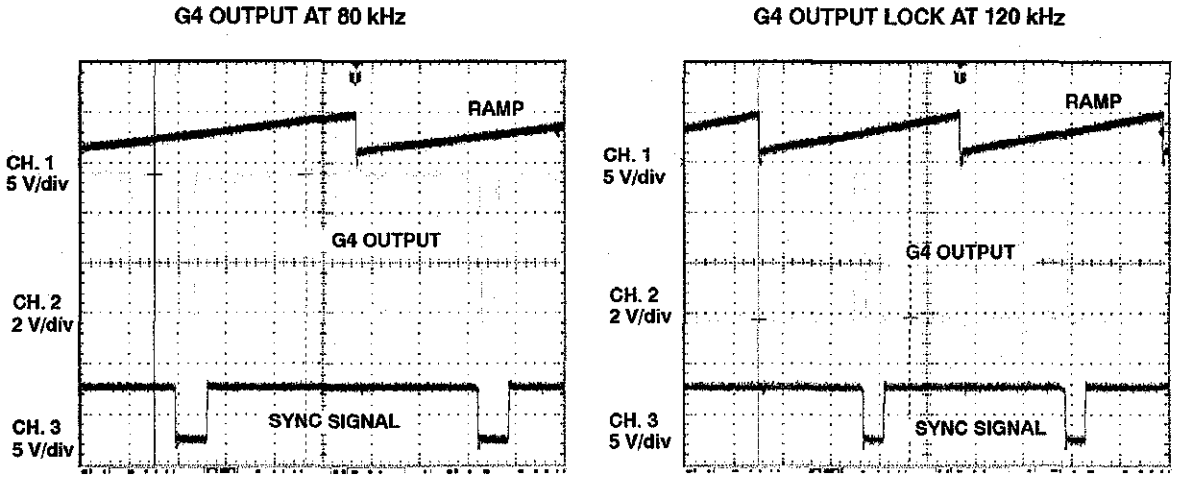

Figure 7: Output waveform for G4 at 80 kHz and 120 kHz [12].

When the sync frequency, f_{sync} is lower than the converter's normal frequency, the average of the G4 output is high whereby the phase can be seen shifted in one direction. As for f_{sync} is higher than the converter's natural frequency, the G4 output average is a low voltage thus the phase is shifted in the other direction.

The original filter configuration for the filter consisting of R3 and C3, it was set up with a 3dB point a factor about 6 below the internal ramp frequency. The second filter is R5 and C5 configuration has to have much higher impedance than the first to limit the influence on the first so resistance and capacitance with a filter of 3dB frequency of 80 kHz was used. The idea with the filters is that the voltage that is presented must be as similar as possible to the DC value and has

the capability to adapt and capture the unit when the two are out of synchronization [12].

At 80 kHz, Figure 7 illustrates the sync signal having the same starting time as the G4 output. When the operating frequency increases to 120 kHz, the starting time for sync signal and G4 output is no longer similar. Because of this, the circuit's configuration needs modification to suite the totem-poled power MOSFET switching operation at 1 MHz and has no output ramp.

Though there might be disturbance in the signals generated, the ideal synchronized PWM signals are expected to achieve as below:

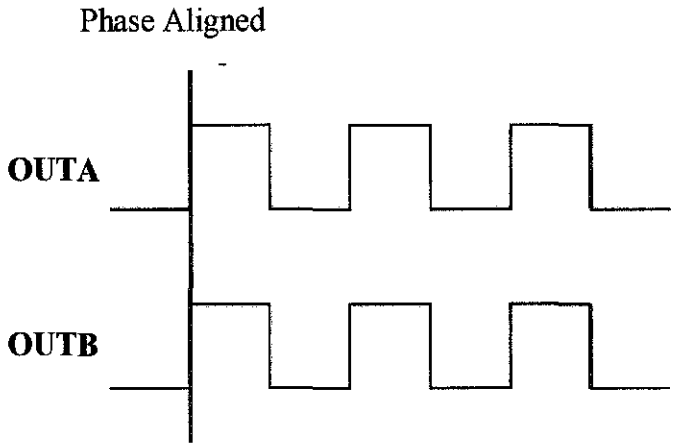

Figure 8: Expected ideal synchronized signals for OUTA and OUTB.

2.3 Signal Delay Element

Delay element introduces a delay of one digit period in a series of signals or pulses [13]. In this project, it is required for the signals to operate alternately in the totem-poled MOSFET switching configuration. Therefore, one of the output signals is required to operate at an alternate cycle whereby will resulting in one switch operating at one time. The rationale to pertain this practice is to ensure the

power supplied to the network will be fully utilized. A method for frequency adjustment of electronic signals in electronic circuit comprises the steps of providing an output signal with a first frequency as input signal for a signal delay element [14].

A delay line is used to produce a number of digital signals, each one delayed in time with respect to each other. Delay lines serve a variety of functions within digital systems. Delay lines provide fixed delays and phase shifts that can perform a variety of signal processing functions. Delay lines are frequently used to adjust timing inconsistencies at complex circuitry mounted to complex printed circuit boards that operate at ever increasing higher frequencies.

Delay lines are used in digital circuits such as board level systems and integrated circuit (IC) devices, including field programmable gate arrays (FPGAs) and microprocessors, to control the timing of various signals in the digital circuits. Digital devices such as mobile phones, personal digital assistants (PDAs), and personal computers are utilized to conveniently handle digital information. When the digital device processes, exchanges, and distributes digital information, the digital device requires triggers generated from a clock signal to process digital data that are sequentially transmitted. A semiconductor integrated circuit accepts an external signal, and outputs an output signal after carrying out processing according to the input signal [15].

To achieve changes in the delay, some delay lines add or subtract delay elements to achieve different delay times, or adjust the corresponding delay elements in a delay line chain to obtain the desired delay time. A delay line generally comprises a circuit device that imparts a fixed or sometimes variable delay to an input waveform. Delay lines generally consist of a set of smaller delay elements stacked one after another to form a longer delay line.

To cater the need of high frequency timer circuit, the use of Intersil ICM 7555 [16] is recommended for this project. Figure 8 shows a basic 555 generally used for delay purposes. This IC can be used for time delay generation and pulse width modulation. This IC can be used with higher impedance timing elements (RC) than regular 555 timers for longer RC time constants. The timing ranges from microseconds to hours. The basic specifications of this IC are as follows:

Operating frequency	:	1 MHz
Supply voltage	:	2V – 18V
Supply current	:	60 μA
Input Currents	:	20 pA

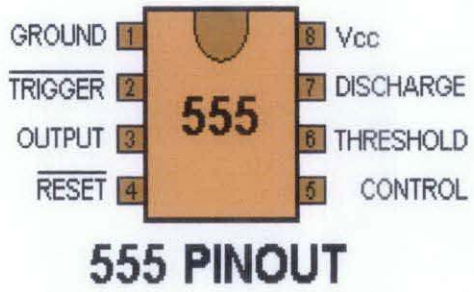

Figure 9: ICM 7555 pin layout [16].

Multiple PWM signals need to be phase synchronized first to ensure the signals start at t_0. The delay is added to one of the signal so that the signal will not conduct more than 1 switch at a time. Figure 10 depicts the signal operation when delay function is added to the PWM signals.

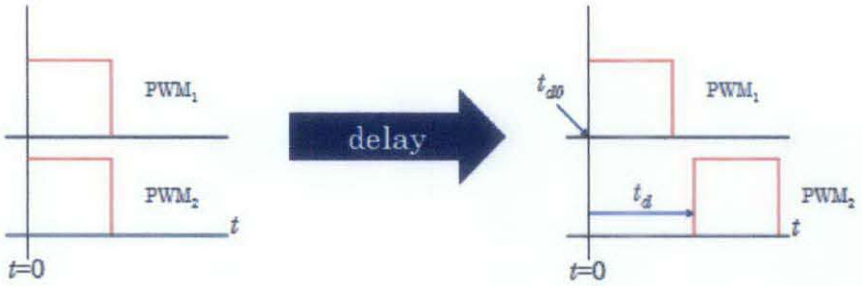

Figure 10: Adding delay function to the signals.

2.4 Power MOSFET

MOSFET requires the continuous application of a gate-source voltage of suitable magnitude in order to operate the switch in the 'on' state. The switching times are very short with a range of $10ns$ to $900ns$ depending on the device type. Switching time dictates the energy loss per transition and determines how high the operating frequency can be. Since the switching time for MOSFET is very short, it shows that it is capable to cater high frequency operation. The on-state resistance $r_{DS\ (on)}$ of the MOSFET between the drain and source increases quickly with the device blocking voltage rating. The 'on' state resistance on a per-unit area basis presented as a function of blocking voltage rating can be expressed in (1).

$$r_{DS(on)} = kBV_{DSS}^{2.5-2.7} \tag{1}$$

where k is a constant that depends on the device geometry. The voltage ratings determine the device power-handling capability [1]. Thus, only devices with small voltage ratings are available that has low 'on' state resistance and hence small conduction losses.

Because their 'on' state resistance has a positive temperature coefficient, MOSFETs are easily paralleled. The device conducting the higher current will heat up and tend to equitably share its current with other MOSFETs in parallel. The temperature coefficient of the device 'on' state resistance determines the ease of connecting them in parallel to handle large currents [1]. Thus, it is an advantage to the totem-poled power MOSFET configuration shown in Figure 11.

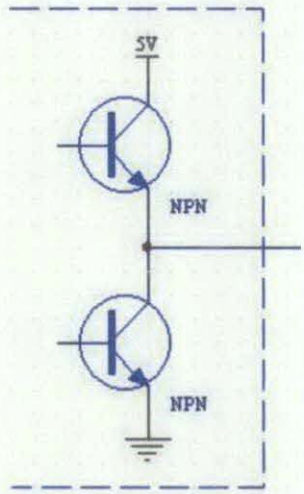

Figure 11: Totem-Poled NMOS configuration.

It is extremely important to consider the available power semiconductor devices and their characteristics. Hence, MOSFET is the most suitable power semiconductor device used for high speed circuit operation.

There are few applications and examples of MOSFET drivers available in Appendix B [20].

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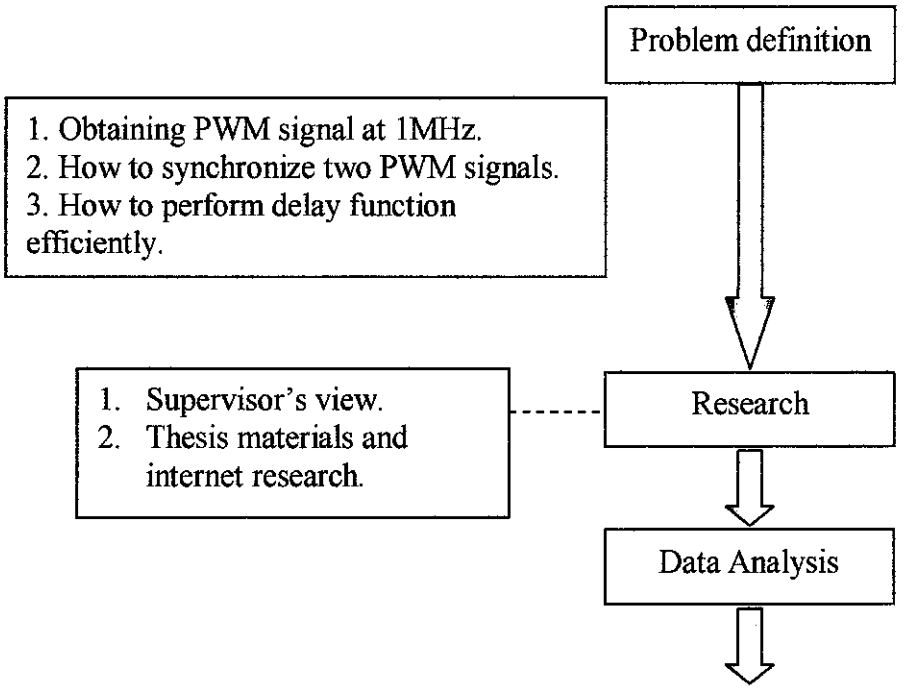
CHAPTER 3

METHODOLOGY

3.1 Planning and Schematic Flow Process

This project is regarding on constructing the network of a multiple PWM signal generation whereby these signals are required to be synchronized. Delay function is then added to the signals as to ensure the switching operating of the new resonant gate driver operates alternately. Thorough research and study are carried out to provide better understanding and ample information to proceed with the experimental work. The workflow of the project is illustrated as in Figure 12:



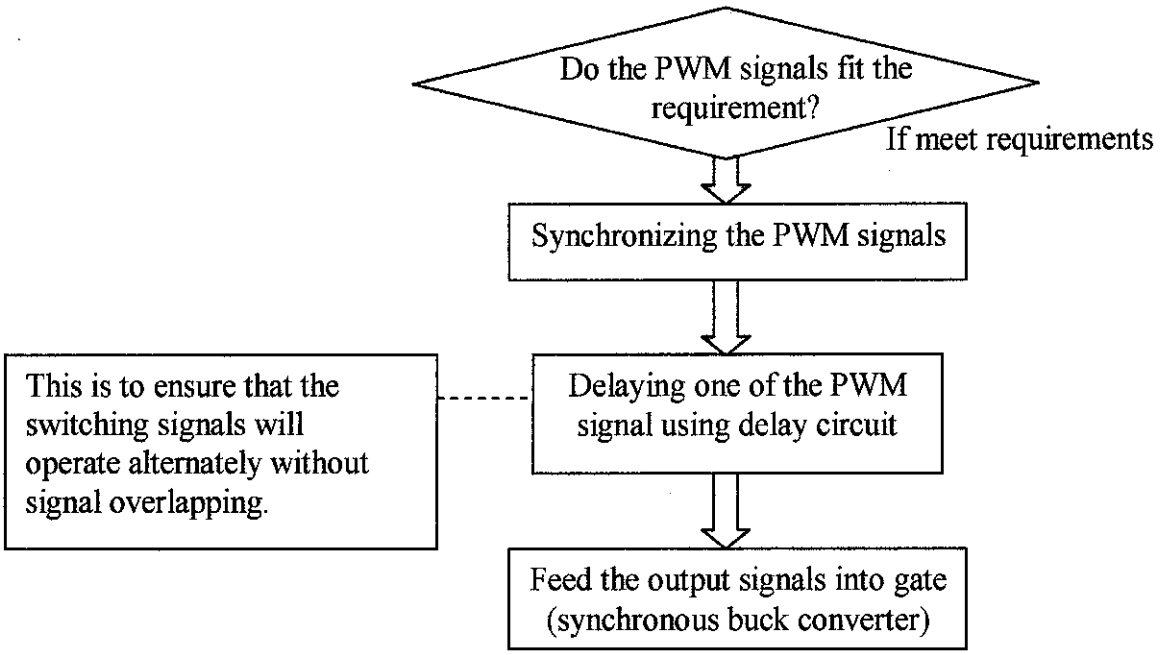


Figure 12: Flowchart of methodology.

3.1.1 Data Gathering

In this project, the study was conducted mainly to verify the experimental work that has being conducted and comparing it with the simulation result obtained in previous paperwork [2]. Furthermore, the switching frequency of the system was varied from 250 kHz to 1.25 MHz. This is to investigate the effect to the system's switching operation when operating at high frequency whether it has the capability to work at frequency greater than 1 MHz. Thus, researches on relevant paperwork were conducted to gather more information.

It is stated earlier that they are two major parts in performing experimental work which are the PWM synchronization and adding delay function to the PWM signals. First step was to recognize possible methods that can be applied to these two major segments. As for PWM generation, it is understood that a voltage comparator is able to generate PWM signals

providing good comprehension on how to control the parameters to obtain the desired signal as in preferred duty cycle. Through comprehensive reading, there are two forms of PWM signal which are Equal-Pulse (Uniform) PWM and sinusoidal PWM. Since this work requires PWM with fixed duty cycle, thus a DC level is used as the voltage reference, *Vref*. The PWM signal is required to demonstrate a smooth signal when generated at high frequency of 1 MHz.

In the synchronization part, a few synchronization circuits were listed for the experimental work. Fundamental understanding is to obtain synchronized PWM signals. When two different signals with the same frequency is fed into the synchronization circuit, the output signals are expected to start at the same time where $t = 0$. In the application report studied, it was stated that the synchronization circuit proposed is only capable to operate at switching frequency of 80 kHz to 120 kHz to work efficiently [12]. In other words, the signals are synchronized operating in this frequency range before the two are out of synchronization. Hence, modification of the original circuit is required, precisely on the filter part. This is to ensure that a wider frequency bandwidth up to 1 MHz is able to pass through the synchronous system.

As for delaying the signals, several methods were practiced to perform delay function. Delay lines, basic timer, programmable timer and delay chips were few of it. The easiest way to cater this requirement is by using an active delay line which will be further discussed in Chapter 4. This delay line has fixed delay time range from 25 ns to 1000 ns. Therefore, the switching time can be adjusted by simply varying the delay time providing the right duty cycle used. The main purpose for adding delay to these signals is to ensure that the switching time for both switches does not overlap. To conclude, both of these techniques synchronizing and

delaying will produce two different sets of complementary square-wave pulses applied at high (Q_1) and low (Q_2) side switches respectively.

3.2 Hardware/ Tools and Software

Hardware and software are one of the essentials in carrying out experimentation to ensure the project is operating accordingly. The hardware and tools that will be employed in carrying out the test are listed below in Table 1.

Table 1: Hardware and software required.

Hardware/Software	Functions / Use
Timer, ICM 7555	General purpose timers, to generate PWM signal.
MAX944	As voltage comparator in PWM generator circuit.
Function generator / PWM generator	Electronic test equipment used to generate electrical waveforms for experimentation.
Oscilloscope	To study and capture the PWM waveform derived from the circuits involved.
CMOS NAND gate	Alternative NAND GATE for TTL NAND gate used in the synchronization circuit.
SN74LS31 timer	Timer proposed for delay function.
8 Pin Leading & Trailing TTL active delay line	Alternative delay line for experimental work.
Digital Multimeter (DMM)	To take important readings (voltage, current, resistance etc.) on the physical circuit.
Electrical components	inductor, capacitor, resistor, transistor and etc.

3.3 Recommended Circuit

3.3.1 PWM Generator

PWM generator circuit proposed for this project can be illustrated as below Figure 13. A DC level voltage level input is needed to derive the PWM signal. In the shaded area, the 5KΩ potentiometer is adjusted to achieve desired duty cycle providing the frequency of the sawtooth signal is also adjusted. These 5KΩ and 1.5KΩ is added to prevent the DC voltage to fall under the lowest range of the sawtooth wave. Thus, this potentiometer works to maintain and keep the duty cycle stable.

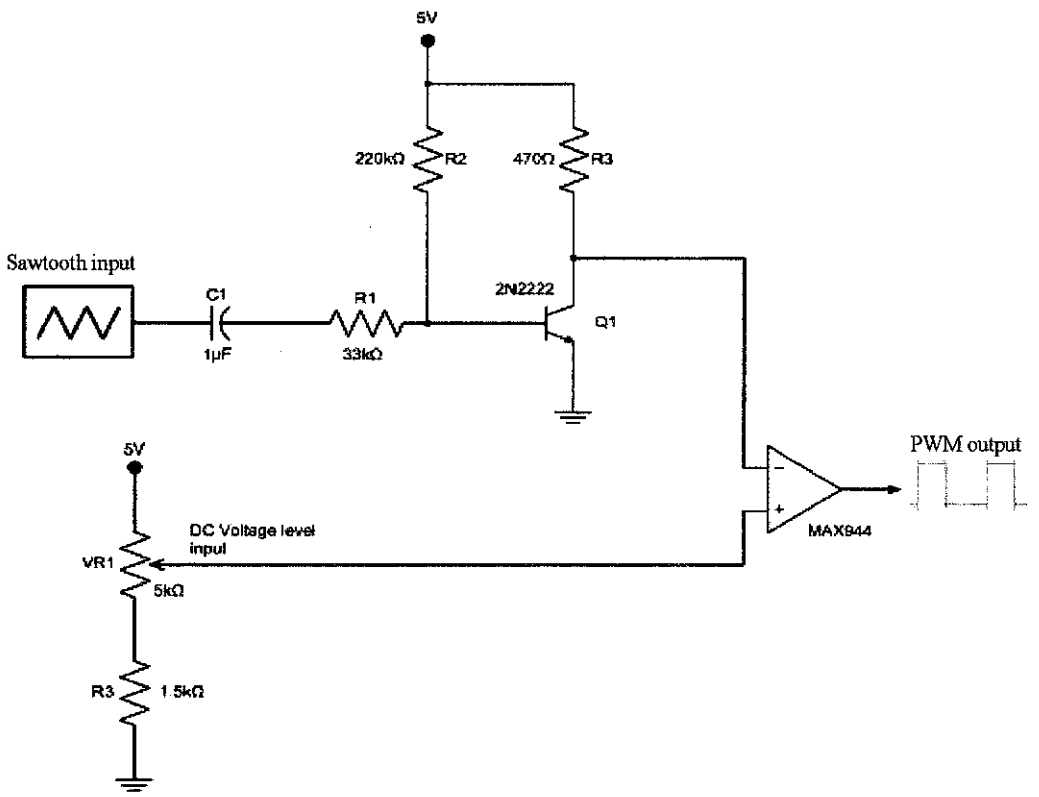


Figure 13: Voltage controlled PWM generator [16].

The comparator chosen to complement this circuit is MAX944. The advantage of using this comparator is that it uses single supply hence

reducing the circuit complexity. The pin layout for this chip is shown in Figure 14.

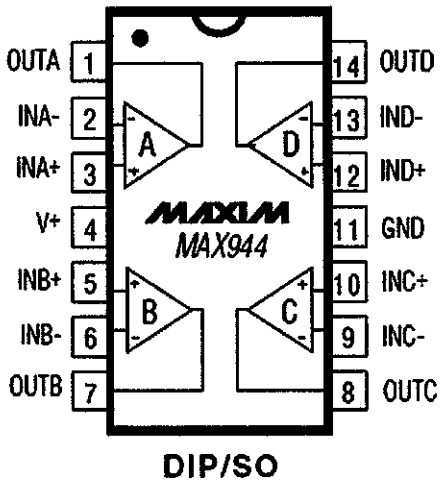


Figure 14: MAX944 pin layout.

3.3.2 Synchronization Circuit

Figure 15 illustrates the synchronization circuit that was set up for the experimentation purpose. The difference of this circuit compared to the synchronization circuit in Figure 6 is that this synchronization circuit suites for converters that have no ramp output. On the other hand, the synchronization circuit in Figure 6 was initially proposed to suite for PWM controllers that have internal timing capacitors and no synchronization pin. The circuits takes both the frequency of the converter and the frequency of the synchronization signal and the frequency of the synchronization signal and mixes the two, resulting in a PWM signal that is changing at the beat frequency of the two signals [12].

The circuit testing was carried out with a nominal frequency of 100 kHz due to the circuit capability to operate form 80 kHz to 120 kHz

without any problems. The selection of sync signal and RT explained as below:

1. Both oscillator and sync signal was set to nominal frequency of 100 kHz.
2. **Sync signal** is the desired synchronized signal that wants to be achieved. For this testing purpose and to verify that the circuit manage to generate synchronized signals, sync signal is generated from the function generator with square-wave attribute.
3. **RT** refering to the UCC38083 datasheet, is the oscillator. Therefore, this input signal is also generated using function generator.

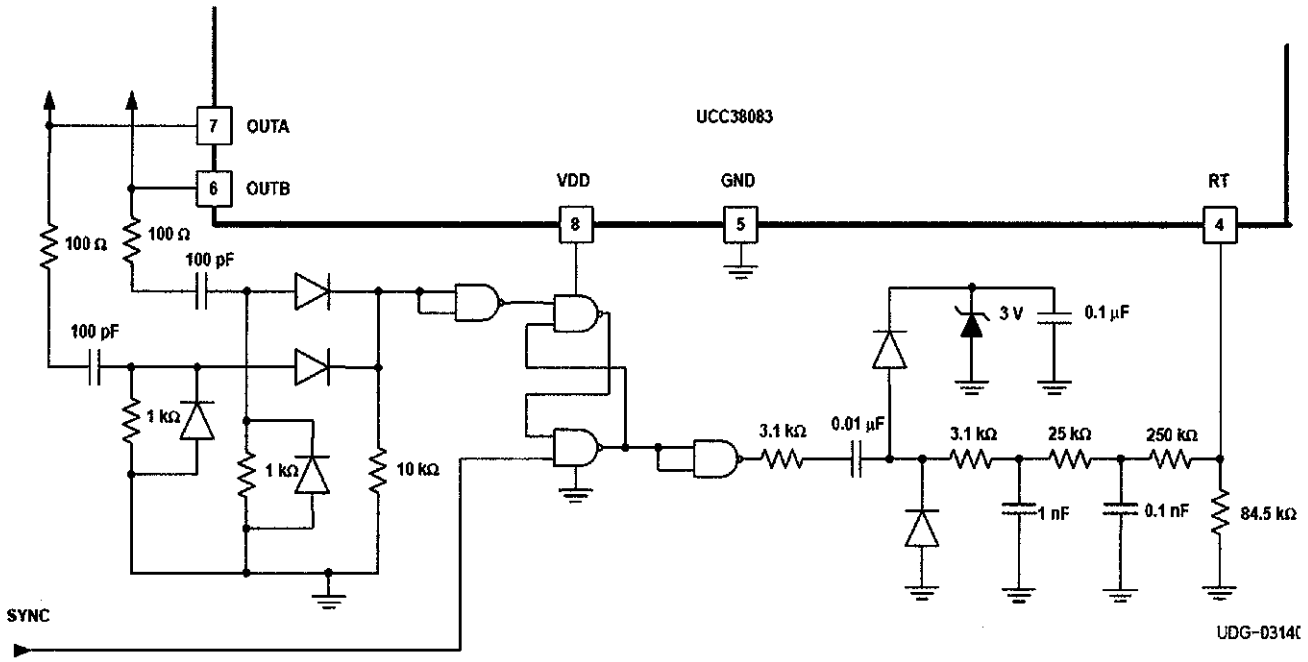


Figure 15: Synchronization circuit used for the experimentation [14].

In Figure 15 illustrates the synchronization circuit used for the experimental work with few alterations that will be further explained in results and discussion chapter.

3.3.3 CMOS NAND Gate

Initially, DM74LS00N was used as the NAND gate in the circuit configuration. DM74LS00N is Transistor-Transistor Logic (TTL) NAND gate. Since TTL devices consume substantially more power compared to CMOS devices at rest therefore it is preferred to use CMOS NAND gate instead [17]. CMOS devices consume power proportionally to their switching frequency. It is recommended to use CD4011B-Quad 2 Input NAND gate as is provides the system with direct implementation of the NAND function and supplement the existing family of CMOS gates. The inputs and outputs are buffered. Below are basic specifications for the CMOS NAND gate chosen:

DC supply-voltage range	:	-0.5V – 20V
DC input current	:	± 10Ma
Noise margin	:	1V at V_{DD} = 5V
		2V at V_{DD} = 10V
		2.5V at V_{DD} = 15V
Lead temperature (during soldering)	:	+265° C

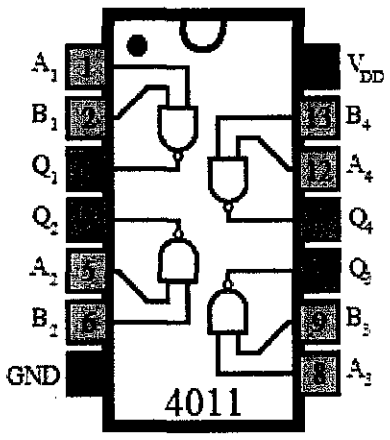


Figure 16: CMOS NAND gate pin layout.

3.3.4 Delay Element – SN74LS31

SN74LS31 is a delay element for generating delay lines. It is a device intended to provide well-defined delays across both temperature and V_{CC} ranges. A limitless range of delay gating is possible when used in cascade. The SN54LS31 is characterized for operation over the full military temperature range of -55 ° C to 125 ° C and operate from 0 ° C to 70 ° C. Below Figure 15 is the proposed delay element proposed to perform delay function:

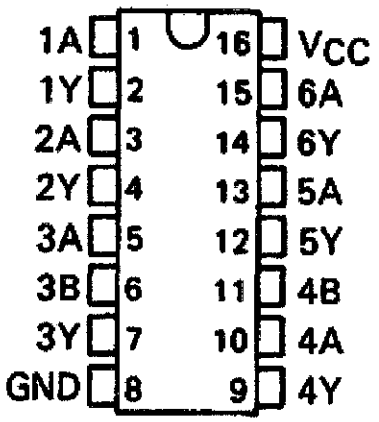


Figure 17: SN74LS31 gate pin layout [17].

This delay element is chosen because of its feature whereby the delay output can be directly obtained by feeding the signals to respective pin assigned. Each pin configuration provides different time delay so it is easier to perform experimentation with various delay parameters. The delay time can be determined as shown in Figure 18.

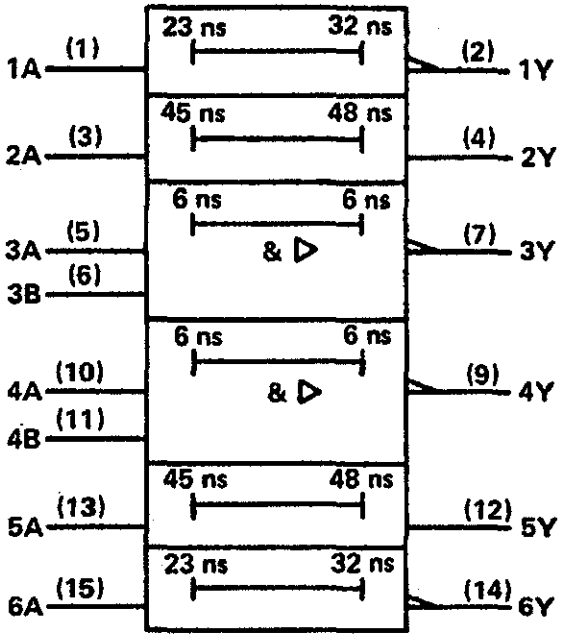


Figure 18: SN74LS31 gate pin layout with respective delay time [17].

3.3.5 Delay Element – 8 Pin Leading & Trailing TTL Active Delay Line

Another delay line proposed is the 8 Pin Leading & Trailing TTL active delay line whereby the TTL is schottky interfaced. This chip is capable to delay PWM signals. The delay lines available are 15A, 14A and 24A. The 15A series is selected to cater the delay function. The input pulse test conditions are as depicted in below:

Pulse voltage	: 3.2V
Duty cycle	: < 50%
Pulse Rise Time	: 2ns (0.75 to 2.4V)
Supply Voltage V_{CC}	: 5.0 ± 0.25 V_{DC}

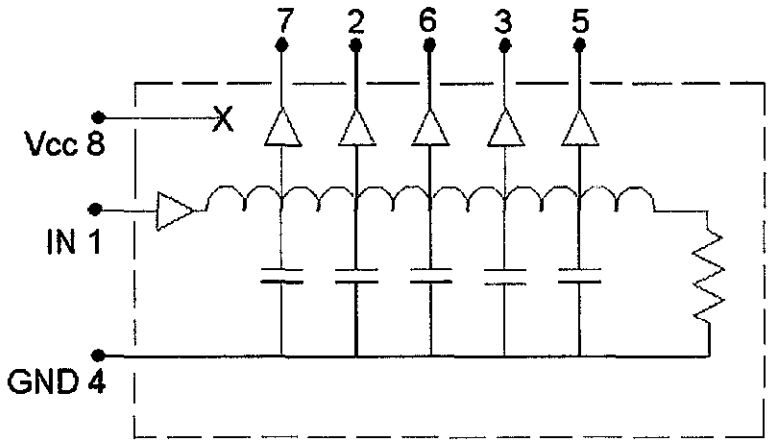


Figure 19: Internal connection of the delay line.

Table 2: Delay line details for respective series.

Part Number	Tap Delay
15A-1000NL	200ns x 5 tap
15A-050NL	10ns x 5 tap
15A-500NL	100ns x 5 tap

The delay line used varies is in the range from 25-1000ns. Each pin indicates increment of 200ns whereas there is delay of 200ns (pin7), 400ns (pin2), 600ns (pin6), 800ns (pin3), and 1000ns (pin5). The layout for the delay line is shown in Figure 19. Table 2 illustrates the delay series available with their respective delay time.

CHAPTER 4

RESULTS AND DISCUSSION

4.1 Synchronization Output Signal Test

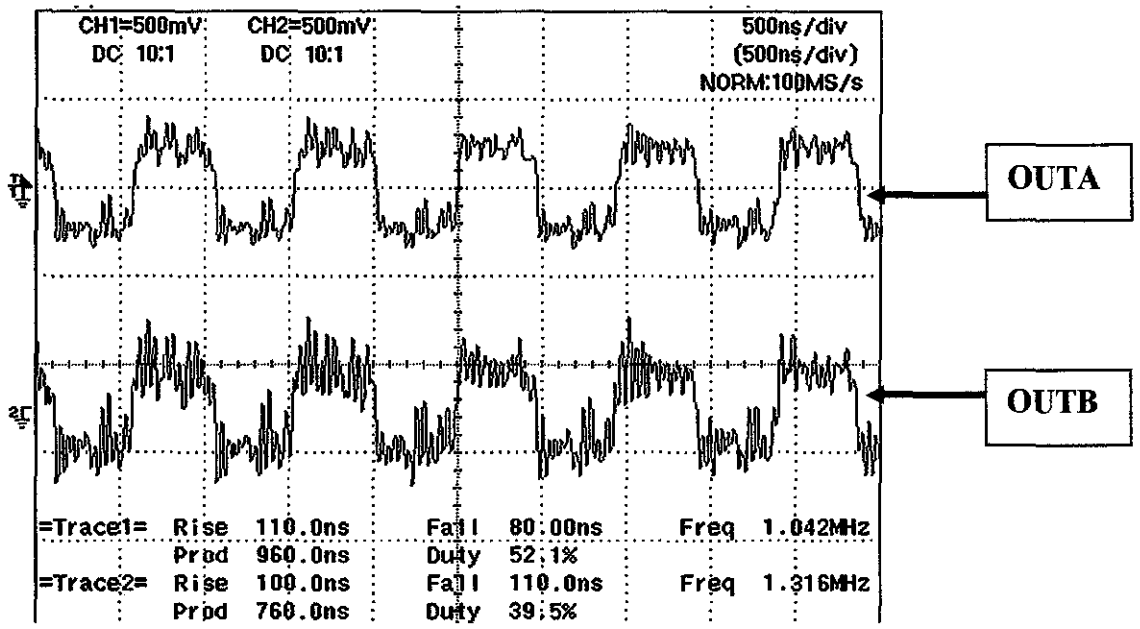


Figure 20: First attempt getting synchronized signals from the synchronization circuit.

Referring to Figure 20, the two output signals are obtained which are OUTA and OUTB. This is the first attempt in getting the result. Unfortunately the results captured is susceptible to noise and disturbance. The output signals obtained are not properly synchronized. The on time for both of the signals are the same, therefore it is synchronized. However, the signals are distorted and

inaccurate. OUTB is more distorted compared to OUTA. Therefore, it is required to modify the synchronization circuit to obtain accurate output signals.

The input signals used in the synchronization circuit are sync signal and oscillator (labeled RT in Figure 15) is at first generated using function generator. Since the synchronization circuit has an operating frequency from range of 80 kHz to 120 kHz, the nominal frequency was set to 100 kHz for experimentation. Both of the input signals were set to 100 kHz in order to obtain the same operating frequency. The synchronized signals desired to achieve might not be precisely synchronized if the operating frequency used to generate the input signals vary.

It is required to modify the synchronization circuit to ensure that the circuit is able to operate at high frequency of 1 MHz. The reason of choosing 1 MHz as the operating frequency is because a higher switching frequency allows for small passive components add up, less area on circuit board, wider control bandwidth and smaller output inductance value of the converter circuit that will be used [2]. However, the drawbacks of conducting the circuit operation at high frequency will result in higher losses in body diode conduction, switching loss and eventually the gate drive loss. For the moment, it is adequate to experiment the circuit operation at high frequency of 1 MHz than testing it at a higher frequency range of 2 MHz or 3 MHz as this will contribute to more losses in the gate drive.

The values of the resistor used vary from 100Ω to 200Ω from the proposed synchronization circuit in Figure 13 and other components such as the capacitors, zener diode, general purpose diode (DN4002, DC) descriptions remain unchanged and similar to the values in the proposed for the circuit. As for NAND gate , DM74LS00N is used. The resistor values vary because it is based on weighted ladder approach since the some of the resistors are not available. The

circuit testing was carried out with a nominal frequency of 100 kHz due to the circuit capability to operate form 80 kHz to 120 kHz without any problems. Another experimentation was carried out with the exact value of resistor configuration as in Figure 15 and below is the result captured:

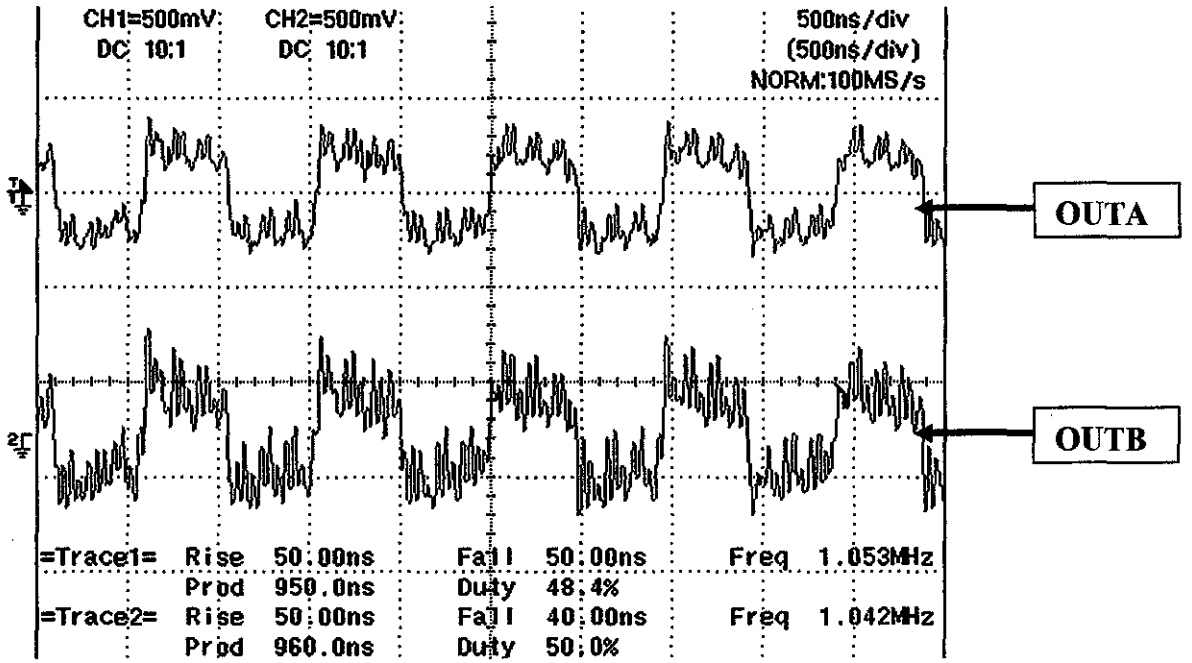


Figure 21: Synchronized signals obtained in second attempt (with modification).

As seen in Figure 21, the results have the below characteristics:

Duty cycle : ± 50%
Switching frequency : ± 1 MHz

Compared to the first result obtained in Figure 20, the distortion in the waveform is improved and the circuit's switching frequency was able to operate at ± 1MHz. However, OUTA and OUTB shows disturbance therefore the result is inaccurate. The reason to this problem is the circuit could not withstand operating in high frequency of 1MHz. The waveform distortion is inevitable. This is proven

where a square-wave signal from an oscillator was fed directly to the oscilloscope and below Figure 22 is the waveform captured:

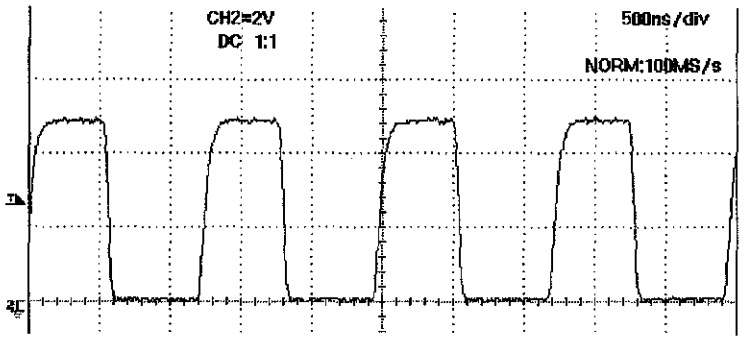


Figure 22: Square-wave of 1 MHz generated by oscillator.

This demonstrates the waveform is not at its ideal form when the frequency was set to 1MHz. The rise and fall time is ± 60ns. Thus there are limitations to produce the desired waveform or most likely the identical waveform. A MOSFET NAND gate is proposed instead of using a TTL NAND gate because MOSFET device promotes better performance operating at high frequency and suitable for the experimentation purpose. The next attempt was carried out using the CMOS NAND gate replacing the DM74LS00N and below are the results:

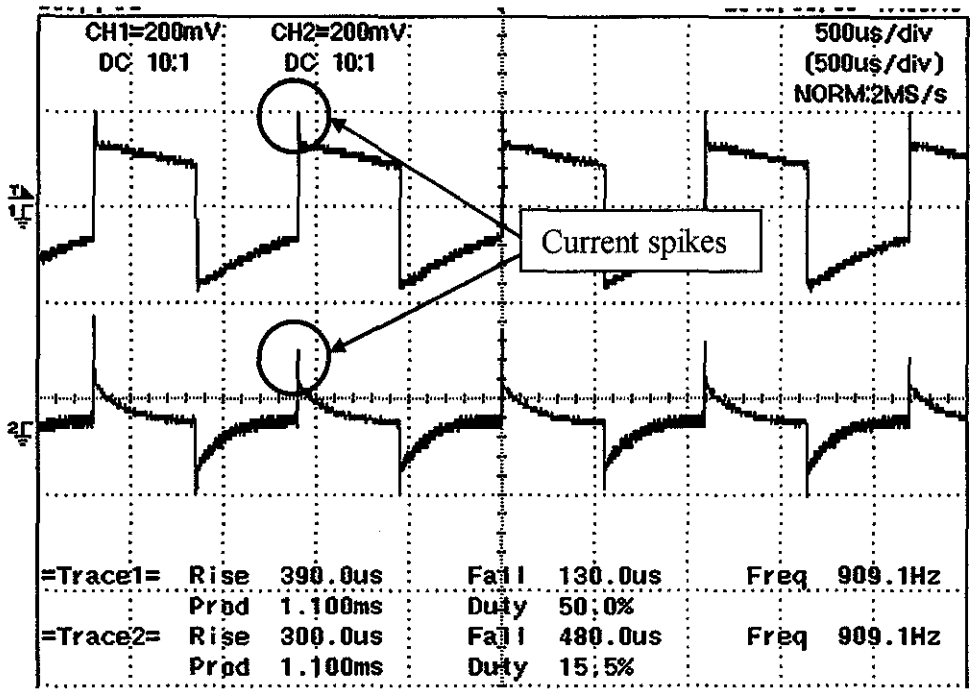


Figure 23: Results using CMOS NAND gate.

As seen above, the result captured seems more stable compared to the ones in Figure 21. The start time and end time for one full cycle of the waveform for both traces are the same, therefore the signals are synchronized. However, the two signals deviate from the expected PWM signals because there are 'spikes' highlighted in RED exist in the system. These spikes pulse exist due to instability of the component configuration and an electrical discharge caused when electric current through an inductive device is suddenly interrupted [17]. Due to these 'spikes', it is impossible for the MOSFET switches to operate with negative and positive signals applied to it at the same time. For this reason, the negative pulse has to be eliminated if PMOS is used as the switch and works vice versa for NMOS.

However, the operating frequency for this system is 0.9 MHz to attain the most minimal 'spikes' in the signal. When the frequency was set to 1 MHz, the waveform obtained has worse pulse spikes. While performing the experiments,

the value of resistance $R_A$and R_B in the synchronization circuit's filter was varied simultaneously and signals begin to show different rate of 'spikes'. Thorough experimentation was carried out in order to achieve the desired synchronized signals with minimal 'spikes'. This can be done by modifying the filter in Figure 13. Filter A is for OUTA and filter B is for OUTB.

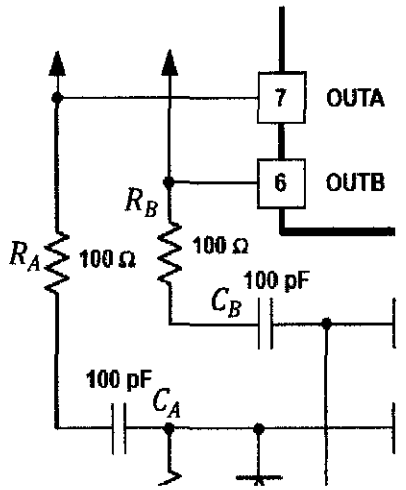


Figure 24: Filter in the synchronization circuit.

Table 3 shows the modification made to the resistors value in the filter in Figure 24 respectively.

Table 3: Resistor value proposed for filter A and B in synchronization circuit.

	Actual Resistor Value	**Proposed Resistor Value**
R_A	100 Ω	± 10 kΩ
R_B	100 Ω	± 10 kΩ

A general relationship for filter configuration can be illustrated in (2).

$$f = \frac{1}{2\pi RC} \tag{2}$$

However it is difficult to obtain a smooth waveform when the frequency calculated for the filter configuration was set to 1 MHz. The capacitor value that should be used for the filters is illustrated as below:

$$1000 = \frac{1}{2\pi(10000)C}$$

$$C = \frac{1}{62831853.07}$$

$$C = 15.9nF$$

To overcome this problem, the filter in the synchronization circuit is modified to reduce or eliminate the spikes thus improving the signal stability. Capacitor works by moving charges into and out of the capacitors when switches are opened and closed therefore capacitor values were varied to remove the sudden electrical discharges. Capacitor value was varied for both filter A and B. However, changing the capacitor value to 16 nF as calculated did not improve the result obtained.

Observation shows that if either one of the filter was modified; the output signal for the other filter was affected too. So in order to choose the right capacitor values for the filters, trial and error method was carried out. The signal waveform shows a greater 'smoothing' effect for bigger capacitor value used. However, one of the signals will be unstable if it exceeded the capacitance threshold limit. Hence, one of the filters which is filter A is configured to have

lower capacitance than filter for B. The proposed capacitor value for the filter is shown in Table 4.

Table 4: Capacitor value proposed for filter A and B in synchronization circuit.

	Actual Capacitor Value	**Proposed Capacitor Value**
C_A	$100\ pF$	$0.1\ nF$
C_B	$100\ pF$	$0.1\ \mu F$

The outcome for the combination of the proposed resistor and capacitor values is shown in Figure 25.

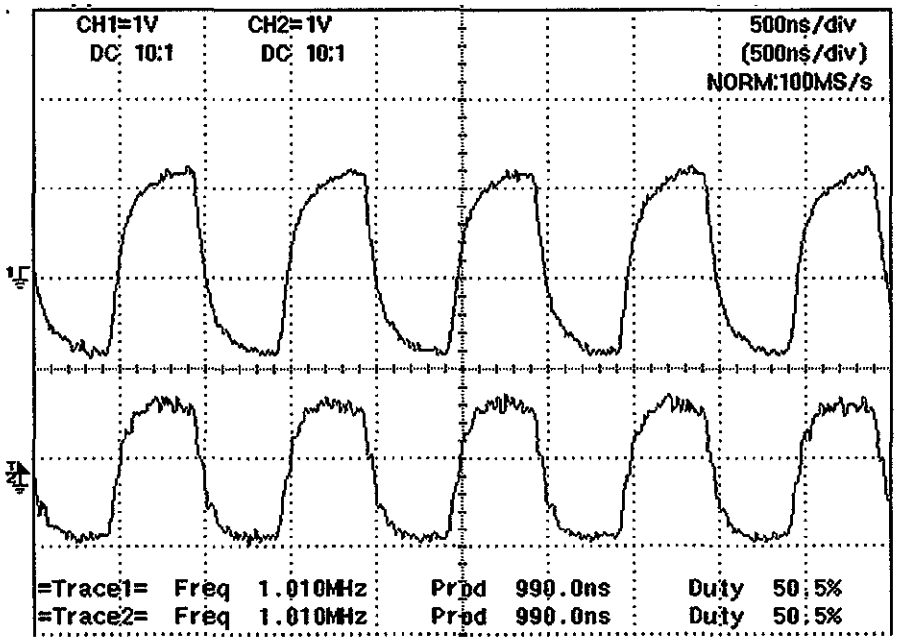


Figure 25: Effect of modifying the filters to eliminate the 'spikes'.

The result obtained in Figure 25 has the below characteristics:

Amplitude	: 5Vp-p
ON time	: 2μs (5μs/div)
OFF time	: 2μs (5μs/div)
Switching frequency	: 1 MHz

Referring to Figure 25, the waveform is improved with smoother curve and acceptable interference. Synchronized signals are achieved by modifying the capacitance value in the filter. However, the problem now is the signal generated is 0.2V which is not able to cater the condition to power up the MOSFET in the driver which needs approximately 7V to guarantee proper operation. The driver operates with a minimum of 5V and maximum 12V of power supply. To counter this problem, the input signal for the synchronization circuit is modified. To obtain a greater signal, the resistance has to be reduced. Therefore, the resistor value in below circuit was reduced to generate greater signal. Figure 26 shows the part where resistance was reduced.

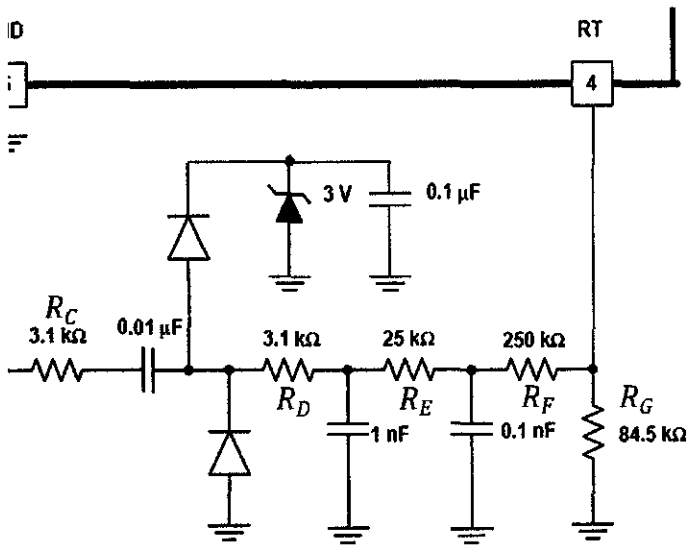


Figure 26: Resistance value was reduced for this part in the synchronization circuit.

The resistors R_C, R_D, R_E, R_F, and R_G was reduced to the ratio of one third (1:3) from the actual value used. If the resistor value is further reduced, the signal will be highly distorted. In Figure 29 and 30 below, it can be seen signal in Trace 2 is slightly more distorted compared to the waveform in Figure 25. However, the signal is only able to operate up to 0.4V only.

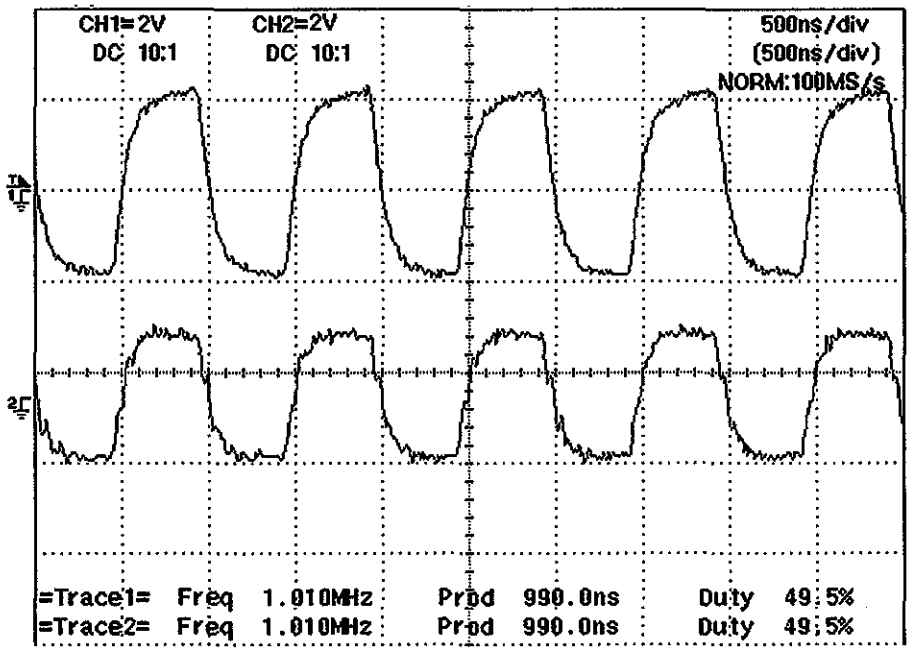


Figure 27: Result of reducing resistance value in Figure 26 of the synchronization circuit.

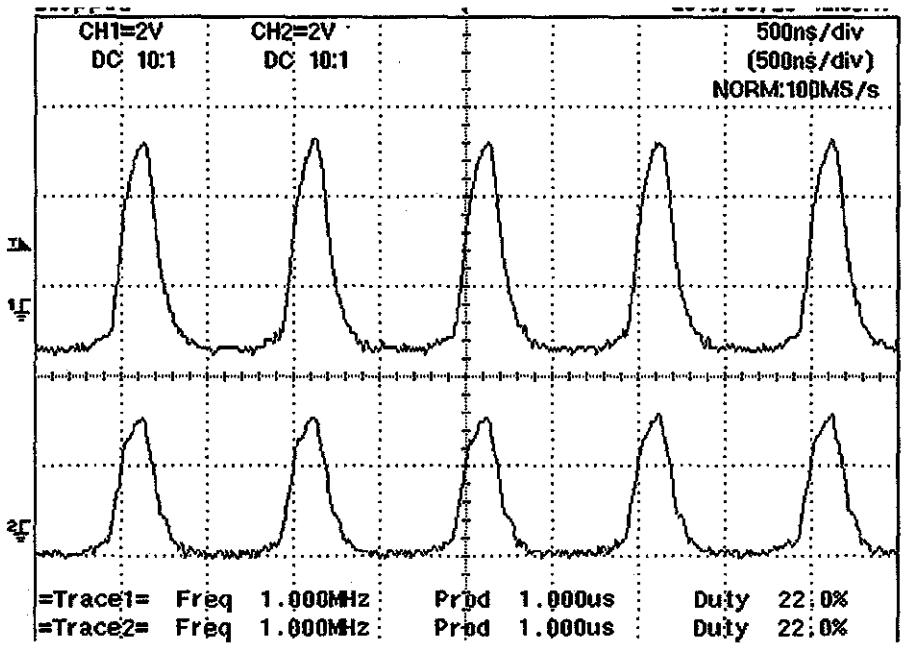


Figure 28: Signals tuned to duty cycle of 20 %.

Signal operating at 0.4V is not compatible to operate the power MOSFET because it is unable to work at the minimum threshold voltage of the MOSFET. Therefore another experiment was carried out using different circuit configuration for the synchronization part. Serving the same purpose to generate synchronized signals, the original circuit configuration proposed for UCC 28517 (in Figure 6) as illustrated in Figure 29 is used but with several modifications.

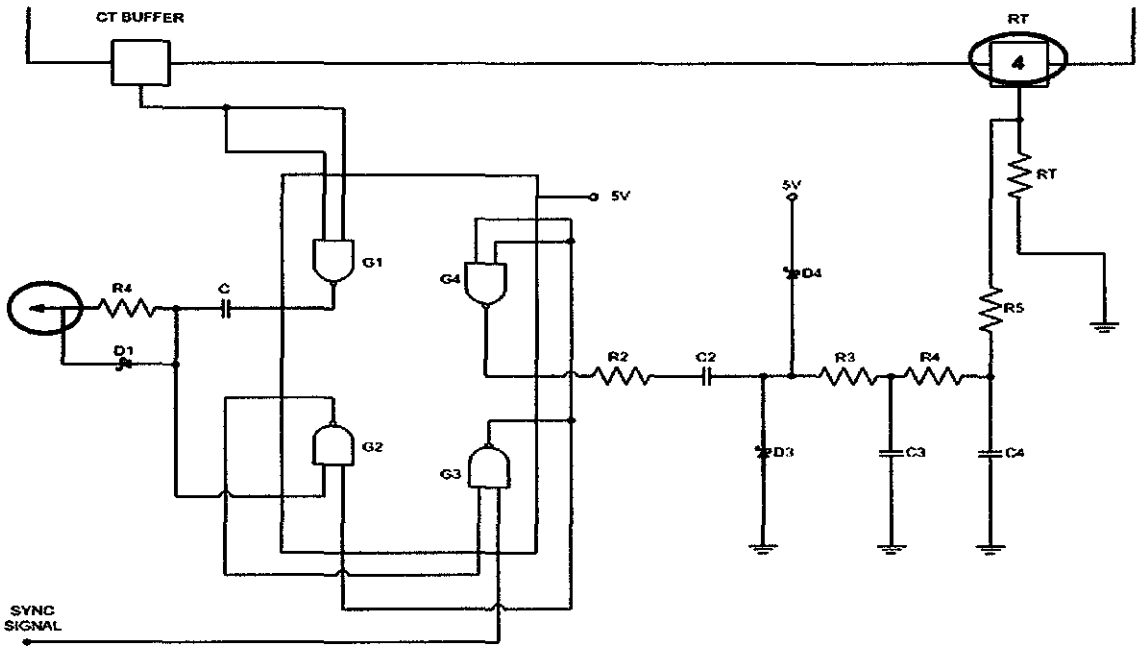


Figure 29: Synchronization Circuit for the UCC 28517.

The resistors values were set in range of 20kΩ to 40kΩ using variable resistor. As for capacitor values, the range are from 100pF to 140pF. The diodes used are zener diode. The combinations of resistors and capacitors were adjusted to obtain a smooth curved signal waveform with no values that vary depending on the desired output signal. The labels CT BUFFER and SYNC SIGNAL were assigned as the input signals. The BLUE mark indicates the output signals required to be synchronized. In Figure 30 and 31, the signal seems more stable and operates at 5V. Below is the result for above circuit configuration:

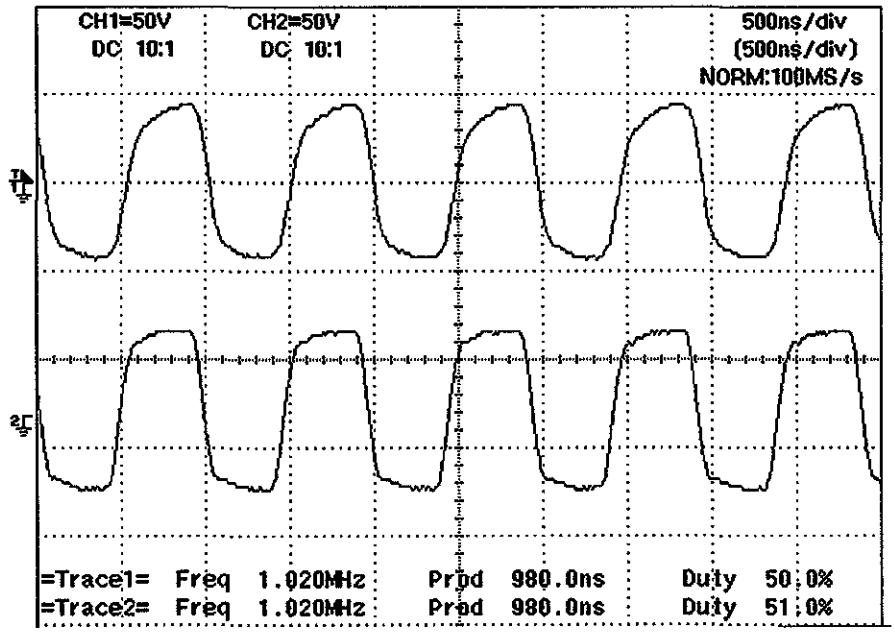


Figure 30: Synchronized signal with 50 % duty cycle.

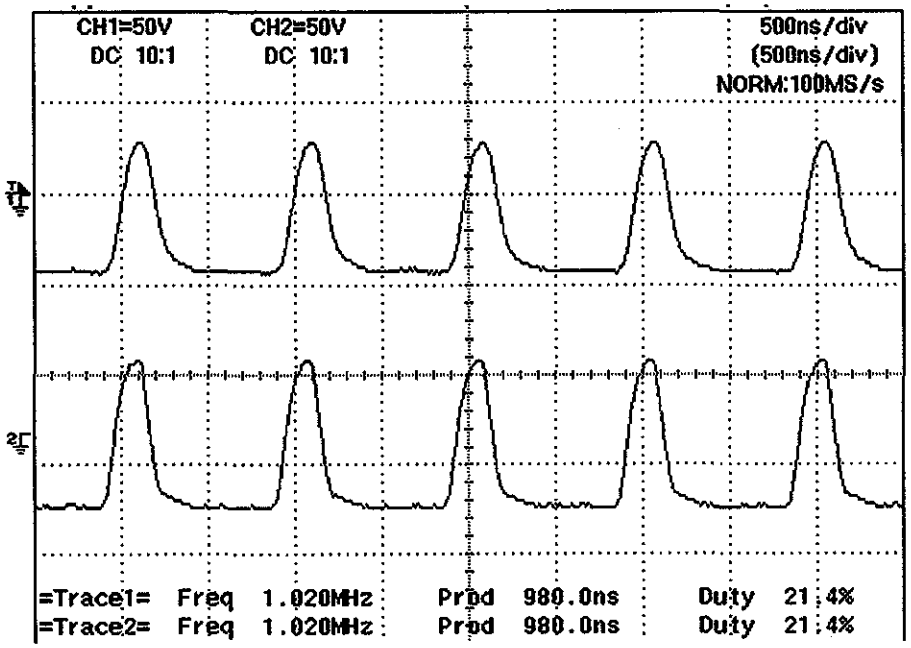


Figure 31: Synchronized signal with 20 % duty cycle.

4.2 Adding Delay Function

Now that the signals are synchronized, delay function is added to the system to generate signals that will not overlap when fed into the totem-poled power MOSFET configuration. The delay line used is 8 pin leading and trailing TTL active delay line. Only one signal is feed into the delay line and is compared to the other signal. The delay time tested was 200ns, 400ns, 600ns, 800ns and 1000ns. The results are presented in accordance to variation of delay time applied to the network. The result is depicted in Figure 32, 33, 34, 35 and 36.

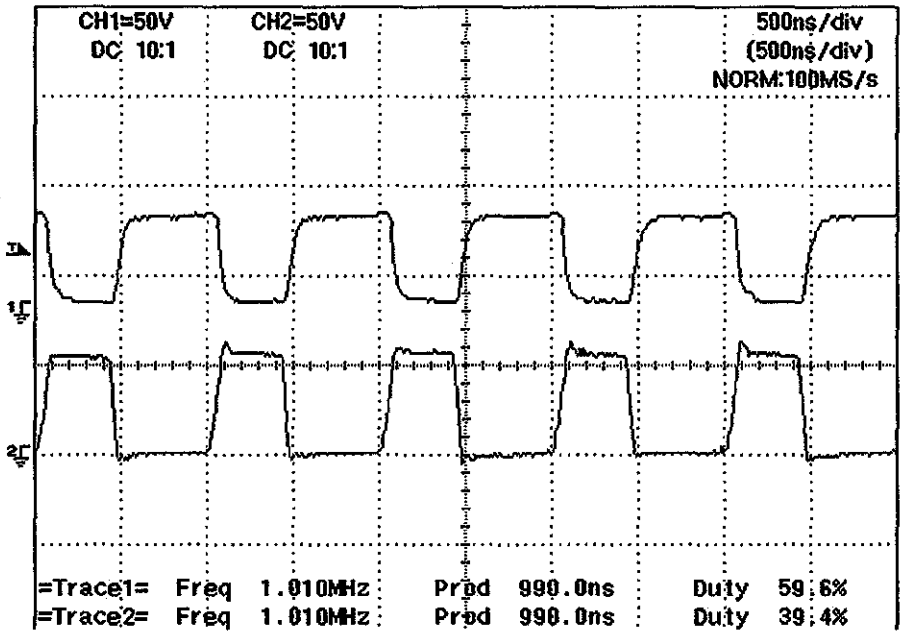


Figure 32: Waveform of the signal added with delay function 200 ns.

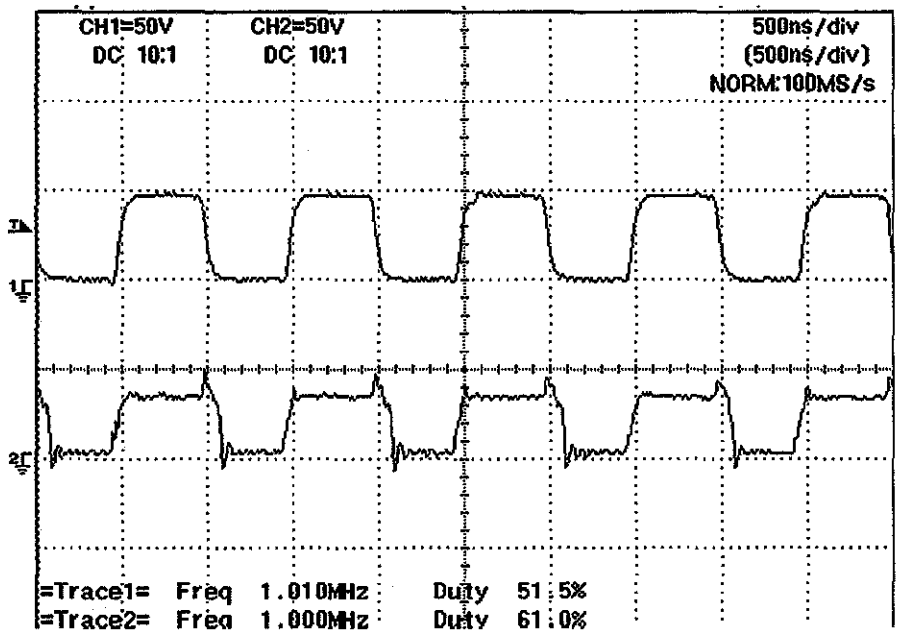


Figure 33: Waveform of the signal added with delay function 400 ns.

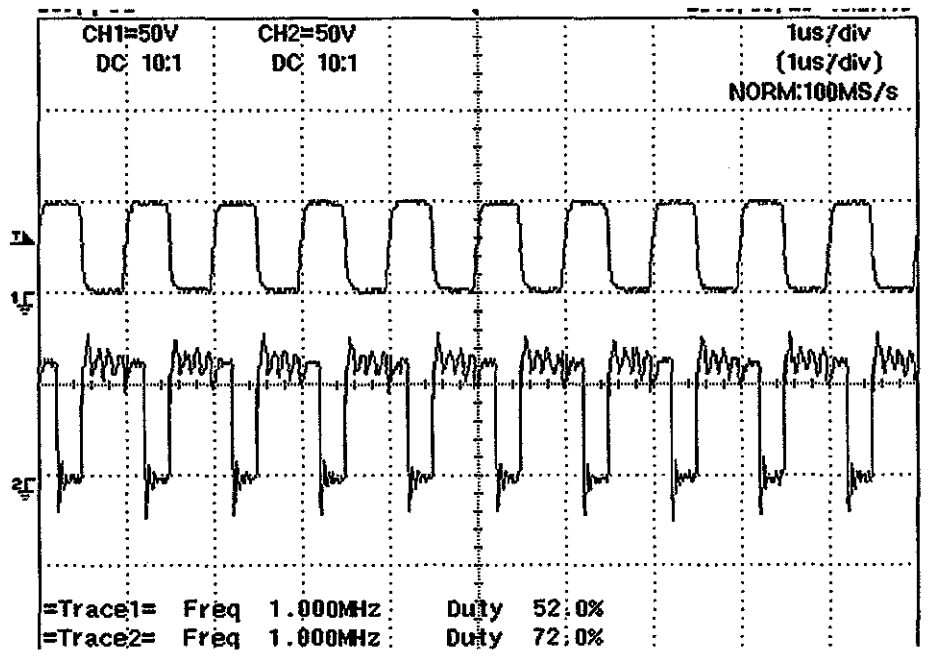


Figure 34: Waveform of the signal added with delay function 600 ns.

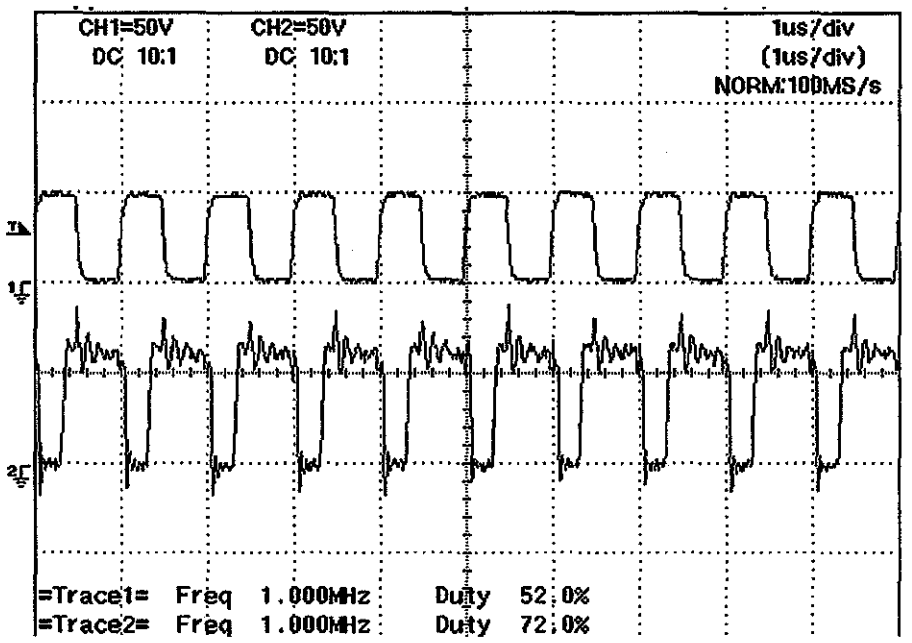


Figure 35: Waveform of the signal added with delay function 800 ns.

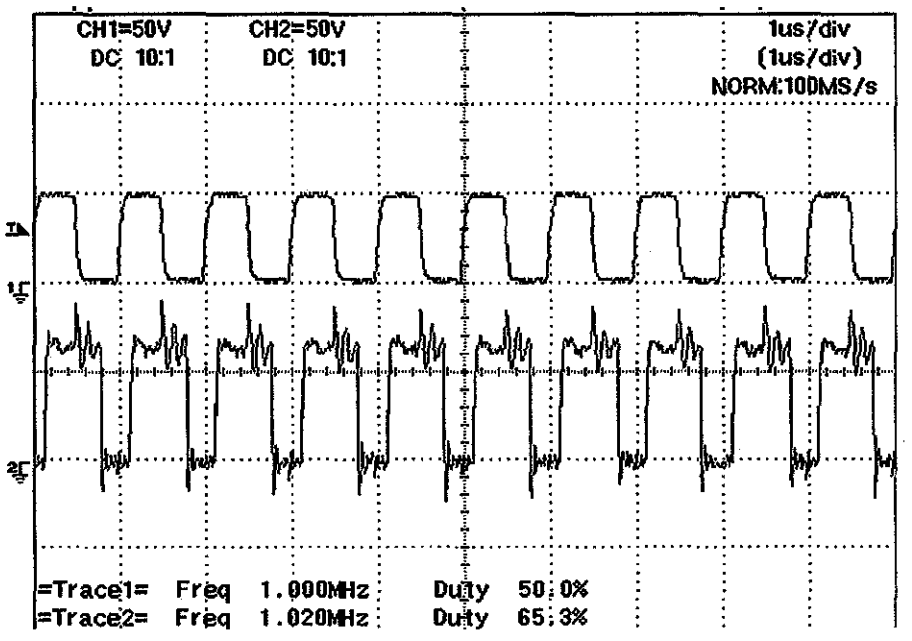


Figure 36: Waveform of the signal added with delay function 1000 ns.

Observation shows that the delay time of 200ns in Figure 32 presents the most suitable signal where both square-waves are complementary. This will best suite the switching operation of the totem-poled power MOSFET configuration. In order to meet the conditions required for the RGD circuit proposed in [2], the duty cycle is set to 20% as shown in Figure 37 below:

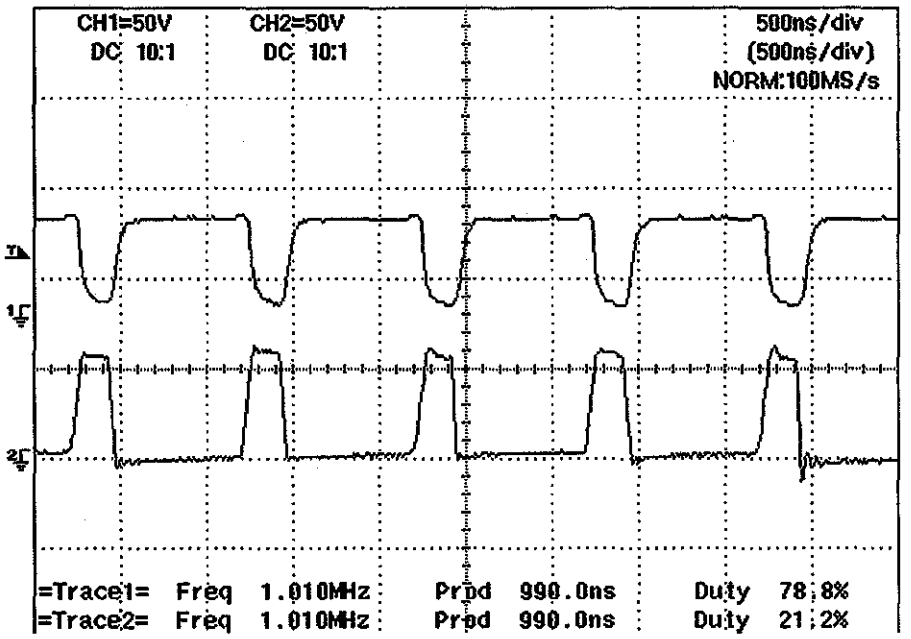


Figure 37: Signal operation with 20 % duty cycle.

4.3 Discussions

The results obtained for the synchronization part is acceptable whereby the PWM signals are synchronized. However, the waveform is susceptible to noise and interference. Inaccuracy of the result might be due to varied values used for the components compared to the proposed configuration. Internal resistance and capacitance may also distribute to the inaccurate result. Synchronization circuit in particular, both sync signal and the oscillator (RT) frequency might be 95 % to 99 % accurate in generating the input signals at 1 MHz. This may lead to

inconsistency of the output signals. To overcome this problem, suitable components should be selected carefully to reduce the result variation.

The duty cycle is fixed at maximum duty cycle of 50%. This is because at duty cycle 60%, the output power will be smaller as the duty cycle of the PWM signal is increased. A turn ON time of 50% and turn OFF time of 50% gives an ideal square wave. Square wave is easier and more feasible to deal with in achieving the synchronized signals which will be added with delay function in the later part. Besides, the interval during the on time will determine the amount of power that is being transferred by the power switch. As a result, more power will be drawn from the power switch and hence reducing the output power. Thus it is more efficient to fix the duty cycle maximum at 50%. The below voltage conversion relationship for V_O illustrates the fact that V_O can be adjusted by adjusting the duty cycle, D. The relationship (3) approaches zero as D approaches zero and increases without bound as D approaches 1. D approaches to 1 when the ratio between τ and T is 0.5:0.5 or in other words, the ON time and the OFF time of the signal has 50% duty cycle.

$$V_O = -V_I \times \frac{D}{1-T} \tag{3}$$

A common simplification is to assume V_{DS}, V_d, and R_L are small enough to ignore. Setting V_{DS}, V_d, and R_L to zero, the equation simplifies considerably to [19]. Therefore this explains why it is preferable to generate the PWM signal at duty cycle of 50%.

In the experimental work, MOSFET is chosen such as for the general purpose CMOS timer and CMOS NAND gate in the synchronization circuit. This is because MOSFET has the capability to operate at high speed operation compared to other semiconductor devices. Since the requirement of this work is to

build a network that operates at 1 MHz, MOSFET is the most suitable mechanism to cater the purpose. With their fast switching capability and low forward voltage drop, power MOSFET is widely used in high frequency, low power applications [1]. For this simple reason, the experimentation has been carried out using power MOSFET to improve the performance of power electronics systems. Figure 38 demonstrates power semiconductor devices in their respective frequency operating range.

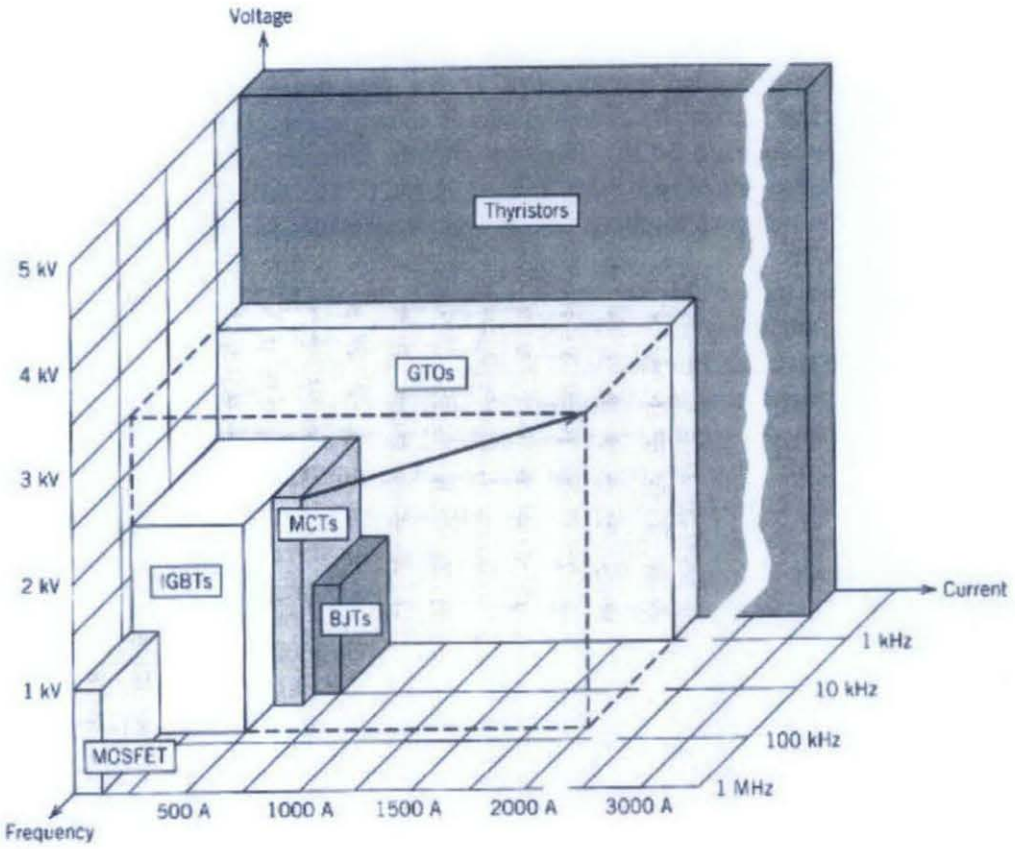


Figure 38: Summary of power semiconductor devices [1].

CHAPTER 5

CONCLUSION AND RECOMMENDATION

5.1 Conclusion

In this work, two synchronized signals are generated. However, modification of the synchronization circuit is required to ensure the signals are accurate and able to operate at 1 MHz with smooth waveform. It is expected the improvement and modification made to the circuit operation can improve the performance of a new resonant gate driver [2] operating at high frequency. In addition, the information gathered in constructing the synchronization circuit for high frequency application can be used to design a chip discrete model.

The delay function has been added to the synchronized signals and the results show that the signals operate alternately which is an achievement. The switching operation of the totem-poled power MOSFET configuration will conduct alternately thus the switching of the gate driver will not overlap.

This work discusses and provides verification on synchronizing and delaying the PWM signals for the totem-poled MOSFET configuration operating at high frequency. Synchronization and delay techniques are recognized where the best way to synchronize the PWM signals is by using the synchronization circuit that is compatible for power converter circuits. As for delaying the signals, the

Delay Element – 8 Pin Leading & Trailing TTL active delay line is the best method for adding delay function to the PWM signals.

Therefore, this study discusses on any improvements and modifications that can be made to the circuit configuration and circuit operation and hence improve the efficiency of the totem-poled MOSFET switching configuration. The result obtained (in Figure 32 and 37) can complement the previous work [2] of improving the performance of a RGD in high frequency converter.

5.2 Recommendations

The followings are recommendations and suggestions for future work:

a) More work has to be done experimentally to validate the findings in this report.
b) Modification on the synchronization circuit to achieve synchronized signals with operating frequency of 1 MHz with lesser disturbance or noise.
c) Obtain the most suitable mean in producing PWM signals that are properly delayed and suitable for the totem-poled MOSFET switching configuration.
d) Use a PWM generator as the PWM signal for the experimental work.
e) Use resistance variables in circuit construction whereby it is easier to control the resistance value rather than using additive method which compromises the accuracy of the circuit operation.
f) The combination of the synchronization and delay techniques studied is most suitable implemented to RGD proposed in [2] with a duty cycle of 20 % in Figure 37.

REFERENCES

[1] Mohan, Undeland, Robbins, " Metal-Oxide-Semiconductor Field Effect Transistors," in *Power Electronics, Converters, Applications, and Design,* Third Edition. University of Minnesota and Norwegian University of Science and Technology, 2003, ch.2, pp. 25-31.

[2] N.Z Yahaya, K.M Begam and M. Awan, "" Investigation of High Frequency effects on Soft-Switched Synchronous Rectifier Buck Converter," in *IEEE Symposium on Industrial Electronics and Applications (ISIEA 2009), pp. 1-5.*

[3] I. Batarseh, "DC-AC Inverters," in *Power Electronic Circuits.* University of Central Florida, 2004, ch. 9, pp. 458-461.

[4] Y. Chen, Fred C. Lee, Dann van Wyk, Dusan Borojevic, "Resonant Gate Drive Techniques for Power MOSFETs," M.S thesis, Faculty of the Virginia Polythechnic Institute and State University, Virginia.

[5] Barr, Michael. (2001, September) "*Pulse Width Modulation,*" Embedded Systems Programming, pp. 103-104 [Online]. Available: http://www.netrino.com/Embedded-Systems/How-To/PWM-Pulse-Width-Modulation

[6] S.Pan and P. K. Jain, "A New Resonant Gate Driver with Two Half Bridge Structures for Both Top Switch and Bottom Switch," *Fellow, IEEE* CHiL Semiconductor Corporation 1 Highwood Drive, Tewksbury, MA 01876.

[7] The Online Dictionary of Computing, (2003, October 10), Definition: Synchronous [Online]. Available: http://dictionary.die.net/synchronous

[8] (-). Synchronous Circuits in *Synchronous and Asynchronous Circuits*. [Online]. Available: http://www.ee.surrey.ac.uk/Projects/CAL/seq-switching/synchronous_and_asynchronous_cir.htm

[9] Intersil Datasheet (2002), *General Purpose Timers, ICM 7555* [Online]. Available: http://www.intersil.com/products/deviceinfo.asp?pn=ICM7555

[10] Synchronization Circuit for Establishing Frame Synchronism Using Pointers in a Digital Transmission System, by Ishihara et al. (1994, January 25). pp 7-16. *Patent 5282206* [Online]. Available: http://www.patents.com/synchronization-circuit-establishing-frame-synchronism-using-pointers-a-digital-transmission-system-5282206.html

[11] *Integrated Systems Design,* Lecture 9: Further FSM and Synchronous System Design, slide 8. [Online]. Available: http://www.scss.tcd.ie/Suhaib.Fahmy/files/lecture9.pdf

[12] J. Bottril, "A New Synchronization Circuit for Power Converters," Texas Instrument, Application Report, SLUA296. October 2003, revised April 2010. pp. 1-5.

[13] The McGraw-Hill Companies, McGraw-Hill Dictionary of Scientific & Technical (2003). *Digit Delay Element.* the Free Dictionary, Encyclopedia [Online]. Available: http://encyclopedia2.thefreedictionary.com/digit+delay+element

[14] Signal Delay Element, Method and Integrated Circuit Device for Frequency Adjustment of Electronic Signals, by Ulrich Weiss, Cedric Lichtenau, Thomas Pflueger, Florian Braun. *Patent AH03B1900FI* [Online]. Available: http://www.faqs.org/patents/app/20090021288#ixzz0nCz85jUP,%20http://www.faqs.org/patents/app/20090021288

[15] Electronics Manufacturers (The premier industry resource for electronic products), "*Delay Lines,*" (2009) Electronics manufacturers' directory. [Online]. Available: http://www.electronics-manufacturers.com/RF_and_microwave_electronics/Delay_lines/

[16] Colin Mitchell, (2010, March 21). "Introduction," in *50, 555 Circuits, A Free E-book,* [Online]. Available: http://talkingelectronics.com/projects/50%20-%20555%20Circuits/50%20-%20555%20Circuits.html

[17] Texas Instrument Datasheet, (1988, March*), SN54LS31, SN74LS31 Delay Elements for Generating Delay Lines* [Online]. Available: http://pdf1.alldatasheet.com/datasheet-pdf/view/27998/TI/SN74LS31.html

[18] Elimination of Current Spikes in Buck Power Converters. (1981, January 13). *Patent 4245288* [Online]. Available: http://www.freepatentsonline.com/4245288.pdf

[19] Paul Horowitz and Winfield Hill, "Keeping CMOS low power," in *The Art of Electronics,* 2nd edition. Cambridge University Press, Cambridge, 1989 ISBN 0521370957, 2001, ch.14, sec 14.16, pp. 970.

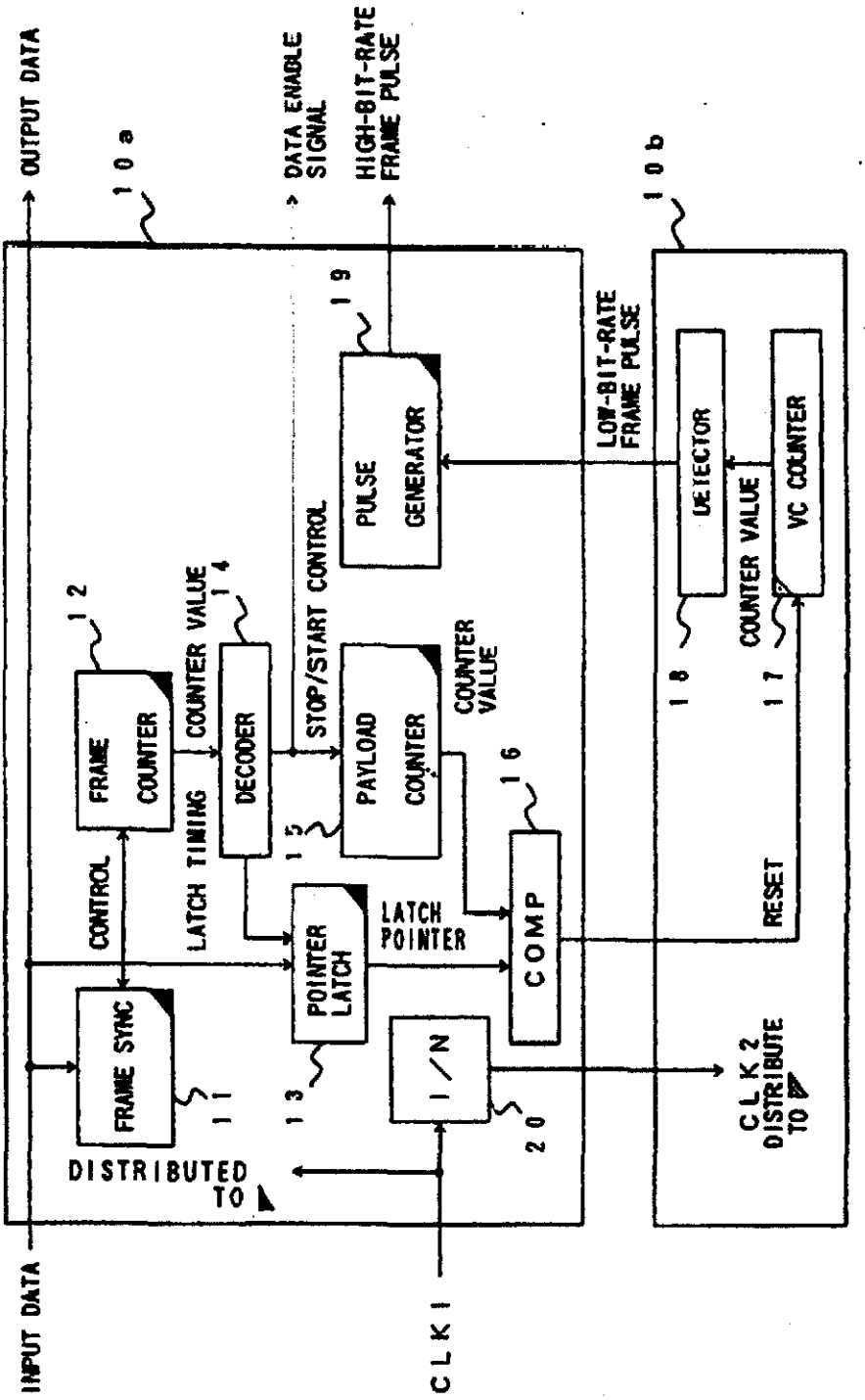
[20] (-). "Schematics and Examples of Totem-Pole and High-Side Drivers," in *Applications and Examples of MOSFET drivers* [Online]. Available: http://hmin.tripod.com/als/fsmyth/pages/mosfet2.html

APPENDICES

APPENDIX A

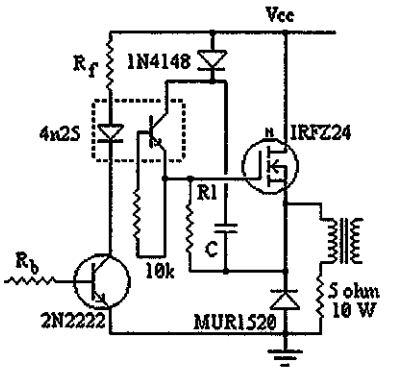
A BLOCK DIAGRAMN OF A FIRST EMBODIMENT OF THE PRESENT INVENTION (COMPLEMENT NETWORK TO FIGURE 4)

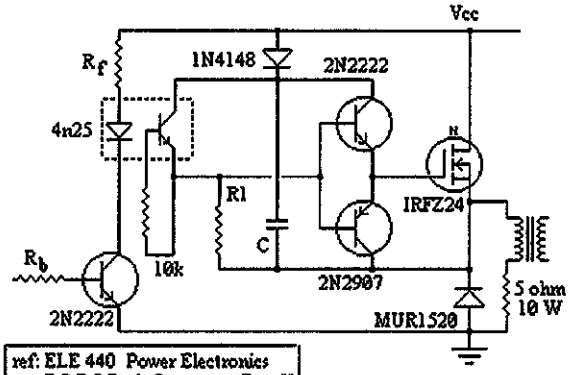
FIG. 5


OUTPUT DATA
10a
DATA ENABLE SIGNAL
HIGH-BIT-RATE FRAME PULSE
10b
19
PULSE GENERATOR
LOW-BIT-RATE FRAME PULSE
DETECTOR
VC COUNTER
18
17
COUNTER VALUE
12
FRAME COUNTER
COUNTER VALUE
14
DECODER
STOP/START CONTROL
PAYLOAD COUNTER
15
COUNTER VALUE
16
COMP
CONTROL
LATCH TIMING
POINTER LATCH
LATCH POINTER
RESET
FRAME SYNC
11
13
1/N
20
DISTRIBUTED TO
CLK2 DISTRIBUTE TO
INPUT DATA
CLK1

APPENDIX B

APPLICATIONS AND EXAMPLES OF MOSFET DRIVERS





ref: ELE 440 Power Electronics
DC-DC Buck Converter Part II
MOSFET Drive Circuit

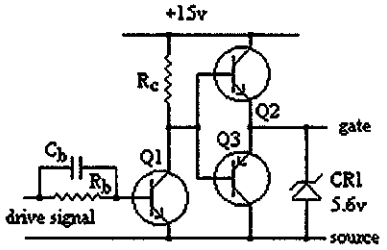
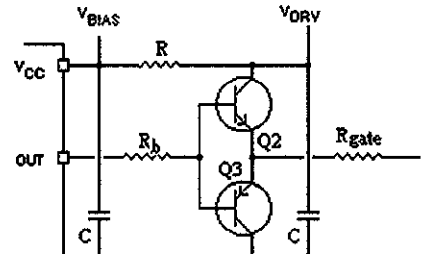


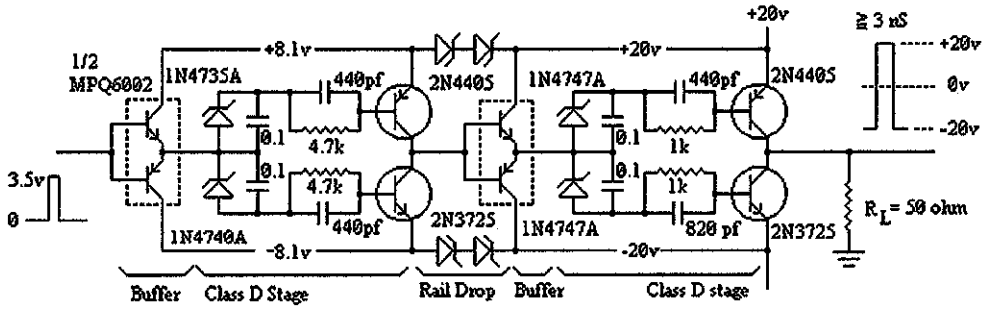
Figure 1: Circuit diagram of a discrete totem pole level shifter/gate driver.

ref: An Isolated MOSFET Gate Driver
Walker/Ledwich

C_b =
R_b = 4.7k
R_c = 8.2k
Q1 = BCS46
Q2 = BCS46
Q3 = BC328
ref: Ben/Doggie



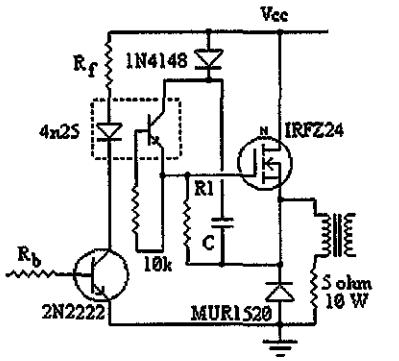
ref: Design and Application Guide for
High Speed MOSFET Gate Drive Circuits
(Abstract; Laszlo Balogh)

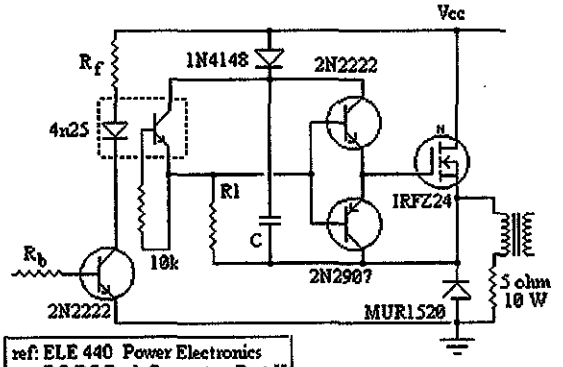


1N4735A 6.2v 1W
1N4740A 10v 1W
1N4747A 20v 1W

High-Speed Pulse Amplifier
ref: www.avtechpulse.com /
papers/thesis/b (appendix B)

MOSFET Gate Drive Circuits
(gatedrv1.bmp)





ref: ELE 440 Power Electronics
DC-DC Buck Converter Part II
MOSFET Drive Circuit

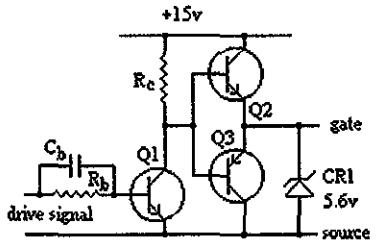


Figure 1: Circuit diagram of a discrete totem pole level shifter/gate driver.

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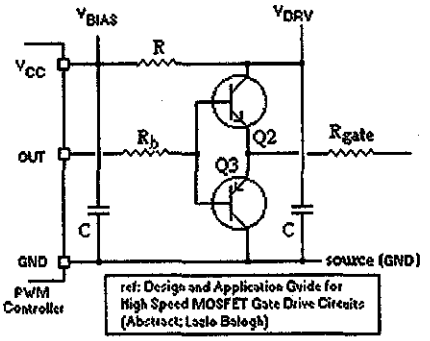
Walker/Ledwich



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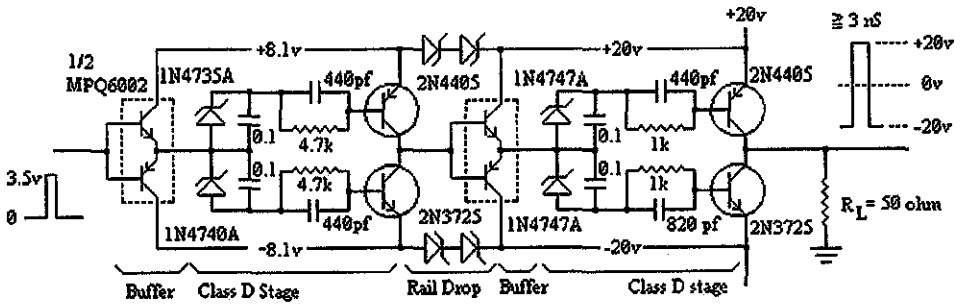
High Speed MOSFET Gate Drive Circuits
(Abstract; Laslo Balogh)



1N4735A 6.2v 1W
1N4740A 10v 1W
1N4747A 20v 1W

High-Speed Pulse Amplifier
ref: www.avtechpulse.com / papers/thesis/b (appendix B)

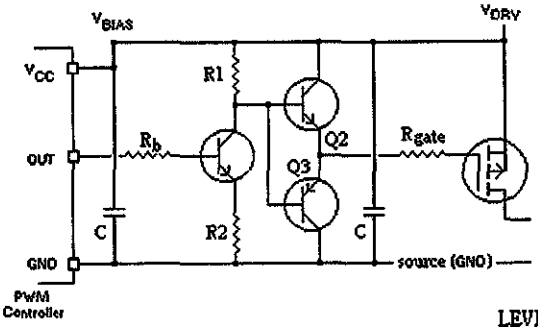


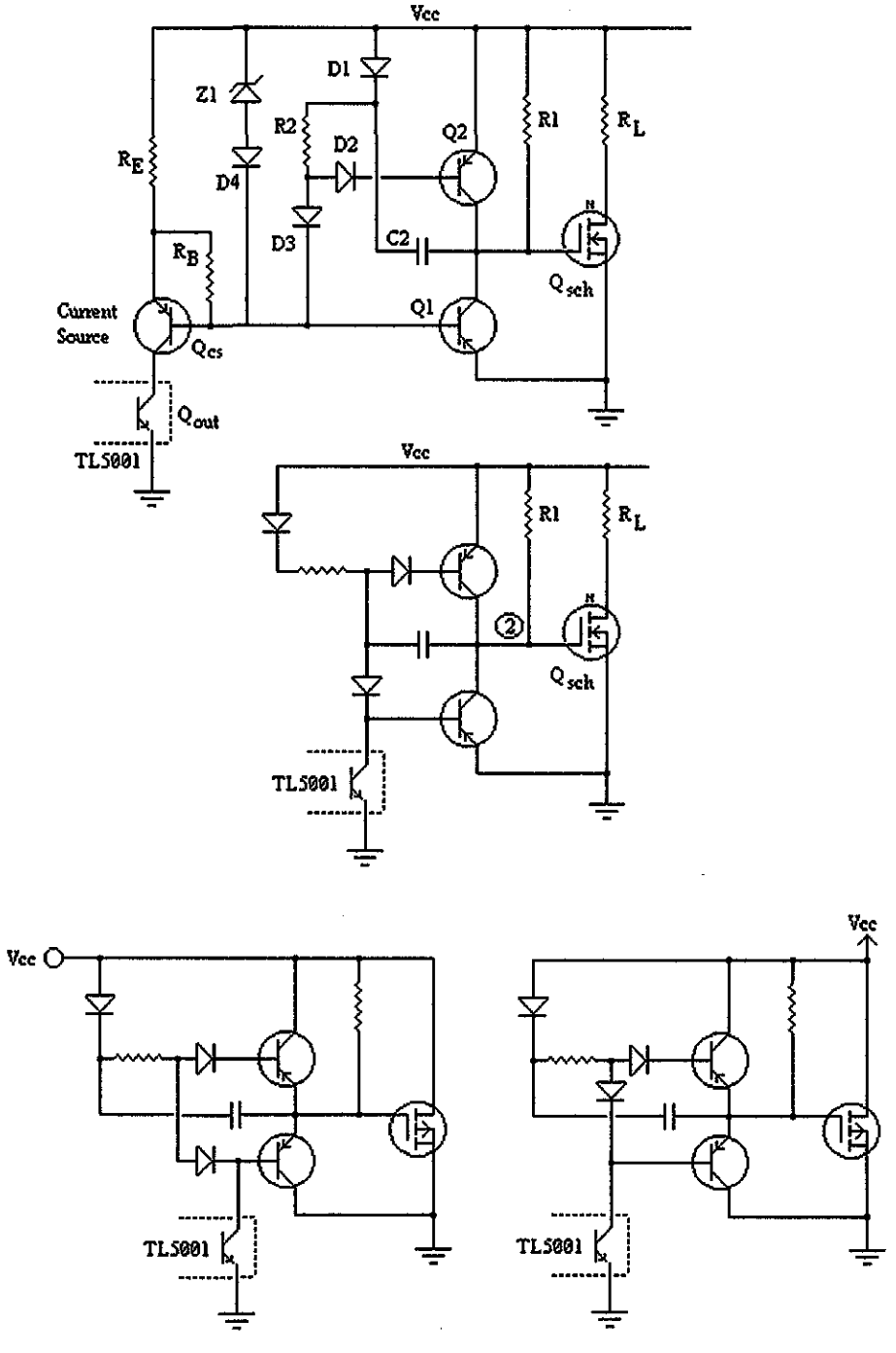
Fig. 20. Level Shifted P-channel MOSFET Driver

$$P_{drive} = Q_G \times V_{drv} \times f_{drv} + \frac{V_{in} \times D_{max}}{R1 + R2}$$

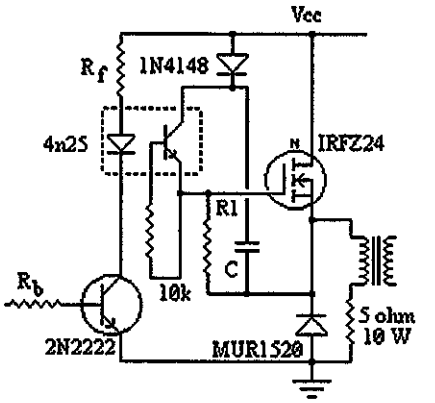
Provides constant gate drive amplitude and fast, symmetrical switching speed during turn-on and turn-off. The dv/dt immunity is primarily set by R1. A lower value resistor will improve immunity, but increase power losses of the level shifter. Built-in self-biasing during startup.

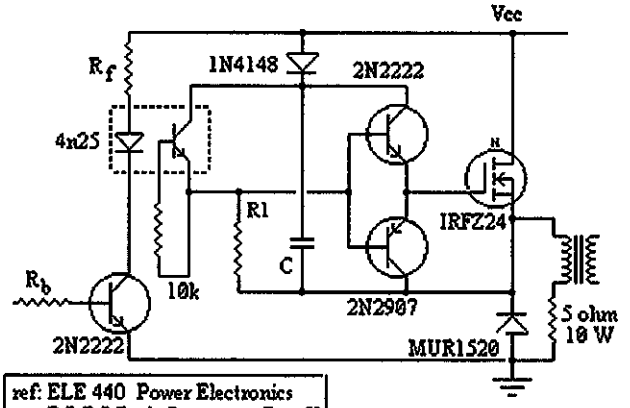
ref: Design and Application Guide for
High Speed MOSFET Gate Drive Circuits
(Abstract; Laslo Balogh)

LEVEL SHIFTERS for MOSFET GATE DRIVE



Totem-Pole Examples
ref: TL5001 data sheet





ref: ELE 440 Power Electronics
DC-DC Buck Converter Part II
MOSFET Drive Circuit

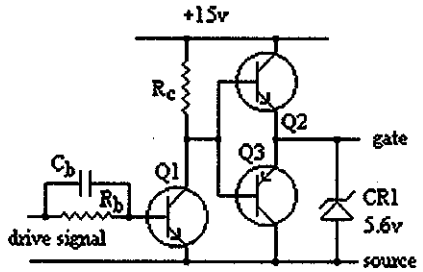
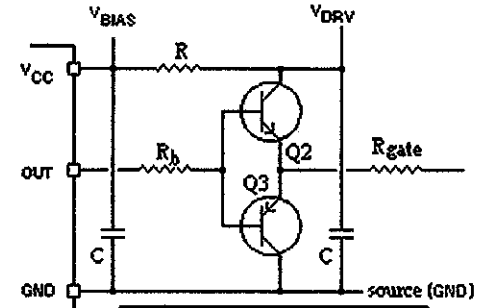


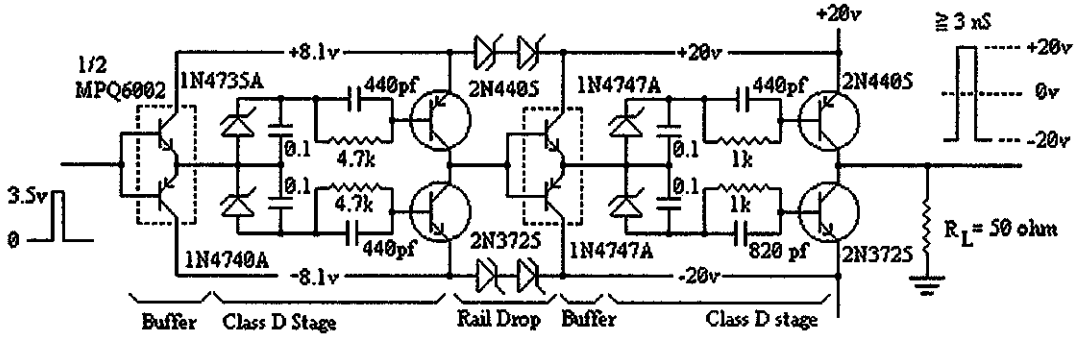
Figure 1: Circuit diagram of a discrete totem pole level shifter/gate driver.

ref: An Isolated MOSFET Gate Driver
Walker/Ledwich

C_b =
R_b = 4.7k
R_c = 8.2k
Q1 = BC546
Q2 = BC546
Q3 = BC328
ref: Ben/Doggie



ref: Design and Application Guide for
High Speed MOSFET Gate Drive Circuits
(Abstract; Laszlo Balogh)



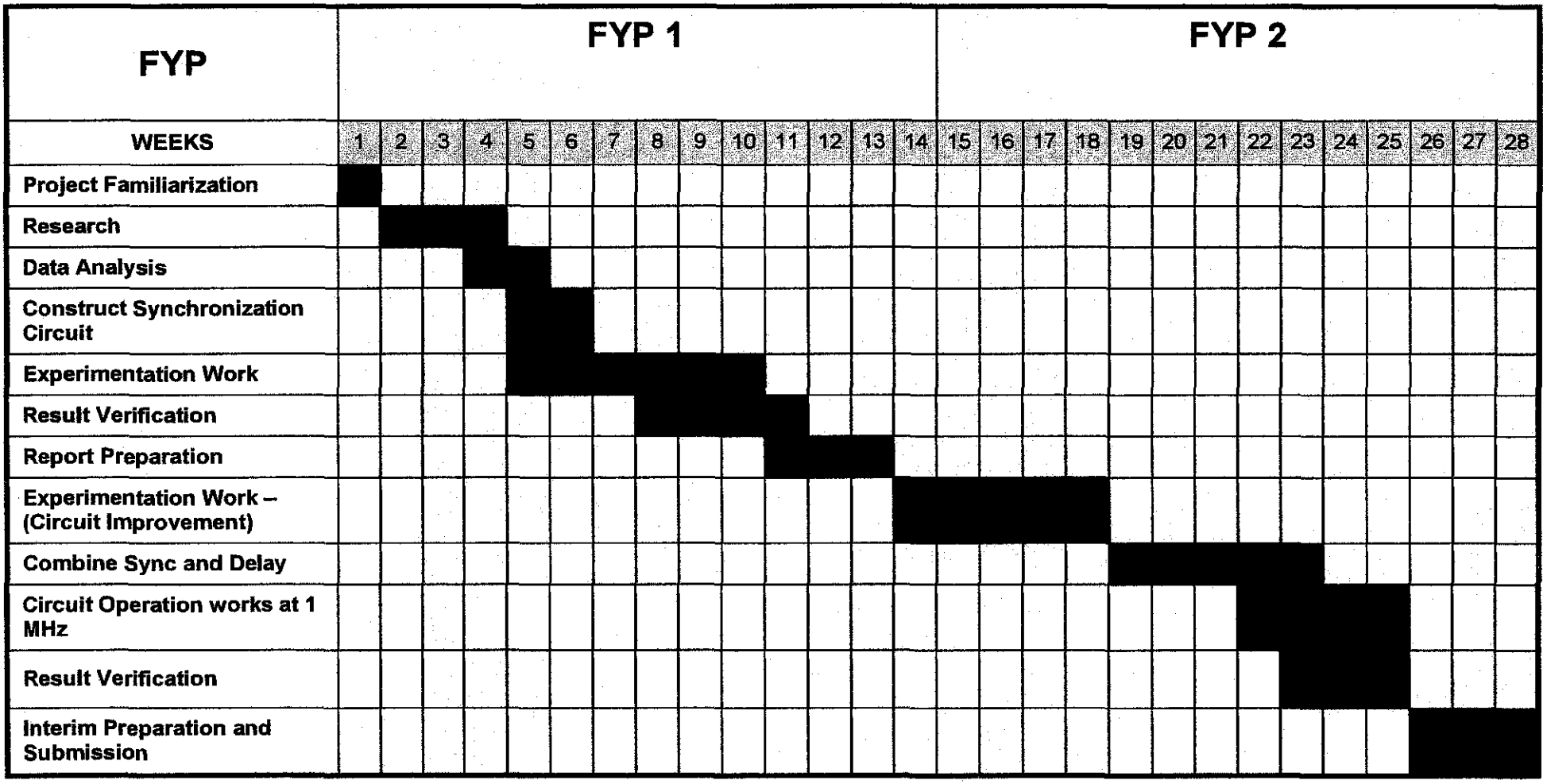
1N4735A 6.2v 1W
1N4740A 10v 1W
1N4747A 20v 1W

High-Speed Pulse Amplifier
ref: www.avtechpulse.com /
papers/thesis/b (appendix B)

Totem-Pole Drivers (3)

APPENDIX C

GANTT CHART AND KEY MILESTONE FOR FYP


FYP
FYP 1
FYP 2
WEEKS
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28
Project Familiarization
Research
Data Analysis
Construct Synchronization Circuit
Experimentation Work
Result Verification
Report Preparation
Experimentation Work – (Circuit Improvement)
Combine Sync and Delay
Circuit Operation works at 1 MHz
Result Verification
Interim Preparation and Submission