DESIGN AND SIMULATE PULSE GENERATOR CIRCUIT

By

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FINAL PROJECT REPORT

Submitted to the Electrical & Electronics Engineering Programme
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CERTIFICATION OF APPROVAL

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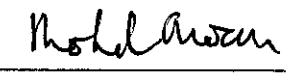

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Project Supervisor

UNIVERSITI TEKNOLOGI PETRONAS
TRONOH, PERAK

December 2007

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

Fazrul Syahrin Shahadan

ABSTRACT

The main purpose of the project is to design and simulate pulse generator impulse based for Ultra Wide Band (UWB) applications. The UWB technology is defined by the Federal Communications Commission's (FCC), the signal must have bandwidth of greater than 500MHz. The structure of the pulse generator is based on Complementary Metal Oxide Semiconductor (CMOS) and the topology of the circuit is adaptation of CR-$(RC)^n$ pulse shaping network. The pulse generator circuit consists of variable length rectangle pulse generator, which mingles up cascaded inverter and N-voltage controlled with a CMOS quasi-Gaussian pulse-shaping filter. In this project, the author successfully designed and simulated the pulse generator. The simulation is done using Virtuoso Analog Design Environment (Cadence) which is able for integrated design circuit and used AMI 0.6um transistor technology. The circuit takes 100MHz pulse as the input. Through the simulation, the author has proved to generate pulse with 660MHz passed frequency. This shows that the topology chosen is able to generate pulse for high frequency purposes.

ACKNWOLEDGEMENTS

I would like to take this opportunity to thank god Almighty for his grace and endless bounty and my supervisor Associate Professor Dr Mohammad Awan for his help and support throughout the course of this project. I appreciate the opportunity he has given to me to work on the project with which I gained new experience in many areas.

I would also like to thank to Mr Said, PHD student who help me a lot and guidance especially for tutoring the Spectre cadence simulation software. Also not forget Mr Asnan Seman who gives support from the beginning of the project and all my friends

Last but not least, my parents who have assist me financially to ensure the completion of the project.

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Fazrul Syahrin Shahadan

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LIST OF ABBREVIATIONS

CMOS : Complementary Metal Oxide Semiconductor

UWB : Ultra Wide Band

NM : Noise Margin

WLAN : Wireless Local Area Network

FCC : Federal Communications Commission's

SRD : Step Recovery Diode

SiGe : Silicon Germanium

RFID : Radio Frequency Identification

WPAN : Wireless Personal Area Network

VTC : Voltage Transfer Characteristic

PRF : Pulse Repetition Frequency

CHAPTER 1

INTRODUCTION

1.1 Background of Study

The advantage of CMOS process in fabricating integrated circuits makes it the popular choice for digital circuit design. This is due to the low power consumption and costless fabrication involve.

Since the CMOS was invented in 1963 by Frank Wanlass at Fairchild Semiconductor, the inventor realized that the CMOS shrank standby power by six times of magnitude over equivalent bipolar or PMOS logic gates [1]. Then more inventions were created in various type of fields or applications such as electronics, computer system, imaging and wireless technology. The invented of wireless transceiver for Bluetooth and IEEE 802.11 WLANs is the example of applications of CMOS [2]. The performance of CMOS circuit at high frequency is comparable to those using bipolar devices due to CMOS aggressive scaling [2]. Ultra Wideband is one of the applications or technologies that can be applied for a wireless system

Ultra Wideband (UWB) communication is different from all other communication techniques due to employing short time pulses and wide bandwidth to communicate between transmitter and receiver. The UWB signal required bandwidth greater than 500MHz, which has been defined by the Federal Communication Commission (FCC).

UWB has a potential for low transmit power design, high performance in multipath channels and ability to work with low signal to noise ratio. The adaptation of CMOS architecture gives simpler transceiver. The transmission of low power pulse

eliminates the need for a power amplifier in UWB transmitter. Besides, the carrier less for UWB transmission, design do not need mixers and local oscillators to translate the carrier frequency to the required frequency band and consequently there is no need for carrier recovery stage at the receiver end. Because of that, CMOS design transmitter is noticeable less complicated and cheaper to design.

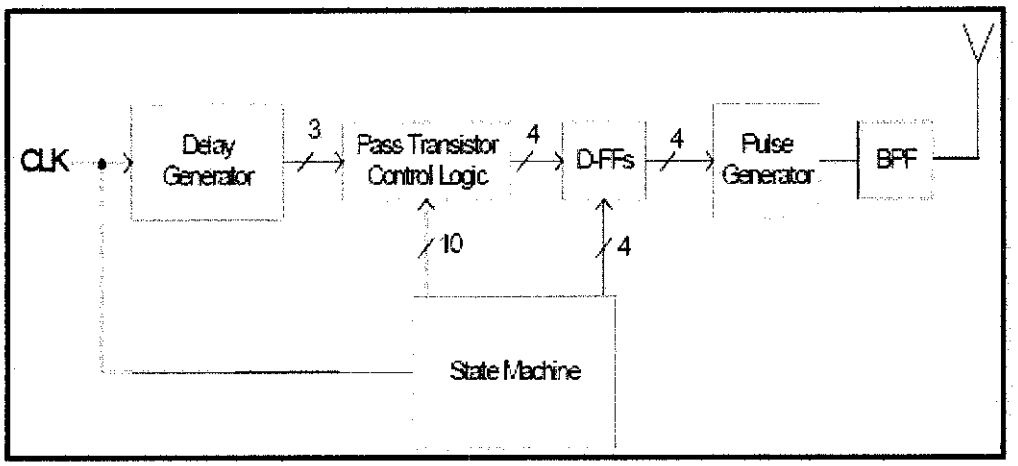

Figure 1: Overall concept of pulse generator design

Figure 1 shows the overall concept of pulse generator that used by [4]. Various CMOS design topology of generating pulse generator presented by [4, 7, 16] and different approaches of design and adopted. Before CMOS pulse generator design was introduced, there are other approaches for generating pulse generator such as step recovery diode (SRD) [17], avalanche transistor [19] and others. The criterion of low power design make CMOS design topology is more popular for VLSI design approach. Among the designs, pulse sources step recovery diode (SRD) is the most popular. Its employ graded doping when the doping level of the semi conductive materials is reduced as the PN junction is approached. This produces an abrupt turn-off by allowing a very fast release of stored charge when switching from forward to reverse bias. Thus it supports high repetition (up to several hundreds of MHz) and has been widely used in applications like high speed sampling circuitry. An input trigger source drives the SRD and generates a step. The step then passes through the short circuited transmission line

and gets reflected with 180 degree phase shift. The design of the broadband baluns was presented in many publications, but the circuits are rather complicated and take a space in the final design and introduced unwanted losses [4, 6, 7].

1.2 Problem Identification

The project title is "Design and Simulate Pulse Generator Circuit". Therefore, the student is requires to design and simulate a pulse generator using CMOS technology. The additional work is to design a pulse generator in high frequency at least 500MHz. The design process includes determining the circuit parameter such as transistor aspect ratio, design approaches etc. to obtain a pulse that can be generated at high frequency.

1.3 Objectives

The objectives of this project are:

1. To design and simulate the pulse generator circuit that can transmit data at high frequency (0-900MHz) with the UWB technology application.
2. To apply knowledge and hands-on experiences that independently working to the project with the guidance of a supervisor.
3. To simulate and design circuit with Spectre software (Virtuoso Analog Design Environment and Virtuoso Analog layout Design).

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

The pulse generator transmitter is combination of processes such as modulating, generating (obtain the pulse signal), transmitting signal. The pulse generator circuit that has to be designed is based correlated to UWB technology. Understanding the basic knowledge of Gaussian pulse and the basic of CMOS is the essential to design the pulse generator. Since the focus of this project is on the development of a pulse generator for an impulse-based system, it is essential to describe the type of pulses. The types of pulses are Gaussian pulses and Gaussian Monocycle pulses [7], [17].

2.1.1 The Gaussian Pulse

Before generating an ultra short pulse, the desired wave shape must be determined for the system. There is various pulse shape design as presented by [15]. The most popular pulse shape for UWB communication systems is the Gaussian pulse since it has the lowest side-lobe compared to a rectangular or sinusoidal pulse because of Gaussian pulse contained most energy in the spectrum.

A Gaussian pulse has the Gaussian shape as shown in Figure 2 and expressed as:

$$V(t, f_c, A) = Ae^{-2(\pi t f_c)^2} \qquad (1)$$

where A is the amplitude of the monocycle pulse, and f_c is the center frequency [5]. The real Gaussian pulse cannot be realized by equation (1), but can be approximated by CR-$(RC)^n$ pulse shaping network in the form of [9].

2.1.2 The Gaussian Monocycle Pulse

Taking the derivative of the equation for the Gaussian pulse (2), we can obtain the equation for a Gaussian monocycle pulse.

$$V(t, f_c, A) = 2\sqrt{e}A\pi t f_c e^{-2(\pi t f_c)^2} \quad (2)$$

The centre frequency of the monocycle pulse is usually defined as $(\pi\tau)^{-1}$ Hz, where τ is defined as the time between the maximum and minimum points of the monocycle pulse [5]. Figure 3 shows the Gaussian monocycle pulse and its frequency spectrum. There are various of pulse based introduced in [5, 7].

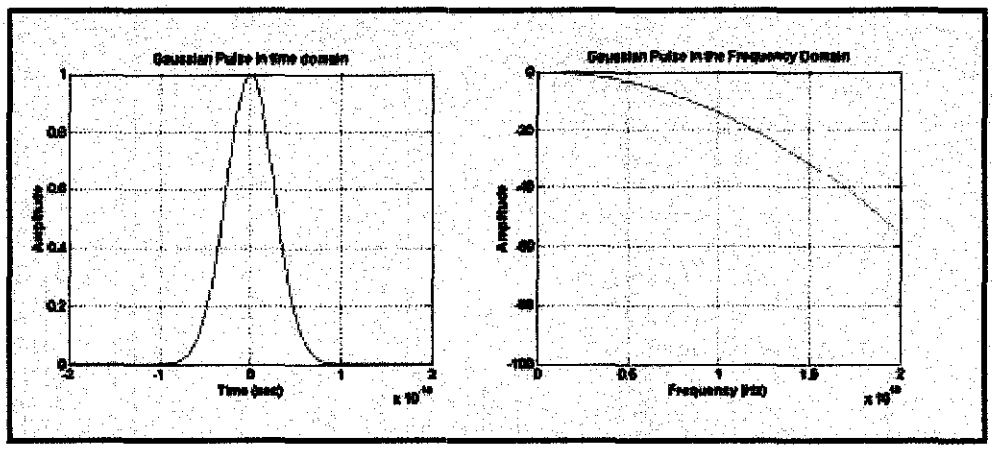

Figure 2: Gaussian Pulse and Frequency Spectrum

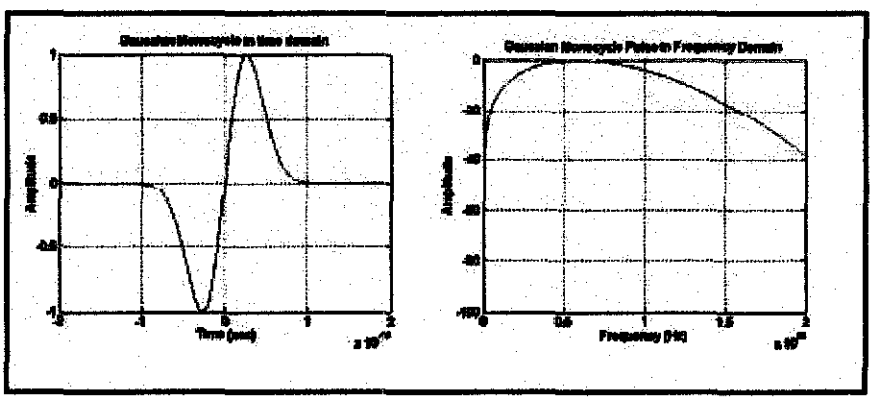

Figure 3: Gaussian Monocycle Pulse and Frequency Spectrum

2.2 Logic Circuit Characterization

To design a pulse generator circuit, there are some parameters that need to be understood especially CMOS basic operation, logic circuit characterization, circuit structure and the other relationship parameter to the design [10]. The most important factor that drives CMOS design development is dissipated the lowest power compare to other digital IC technology and logic circuit families. Some reasons for displacing conventional technology to CMOS technology are summarized below.

- The power dissipation of CMOS is less than the BJT. This factor drives to pack more CMOS circuit on a chip compare to BJT technology.
- High input impedance of MOS allow designer to use charge storage for temporary storage of information in both logic and memory circuit.
- The technology is developing until 0.06um utilize channel as the features size of the CMOS circuit.

For the next sub section will be discussed the parameters that usually used to characterize the performance and operation of logic circuit family.

2.2.1 Noise Margin

Noise margin is the amount by which a signal exceeds the minimum amount for proper operation. The analysis of static operation logic circuit characterize by Voltage Transfer Characteristic (VTC) to evaluate the noise margin. From the VTC we can obtain the V_{OH}, V_{IH}, V_{OL}, and V_{IL} and evaluate the performance. The robustness of a logic circuit family determines by its ability to reject noise and thus the noise margin NM_H and NM_L [9].

$$NM_H = V_{OH} - V_{IH} \qquad (3)$$

$$NM_L = V_{OL} - V_{IL} \qquad (4)$$

2.2.2 Propagation Delay

Propagation delay, symbolized t_p, is the time required for a digital signal to travel from the input(s) of a logic gate to the output. Obviously the shorter propagation delay the higher speed of logic circuit family can operates. The propagation delay defines as;

$$t_p = 0.5\ (t_{pLH} + t_{pHL}) \qquad (5)$$

2.2.3 Power Dissipation

Power dissipation is an important issue in digital circuit design. The reason of reducing the gate power is to maximizing the number of gates on a chip. Thus, a compact and power effectives chip can be produced. There are two types of power dissipation in a logic gate; static and dynamic dissipation. Static dissipation occur when the absence of switching action whereas dynamic dissipation happen the only if gate is switched. An inverter operates from a power supply V_{DD} and driving a load capacitance C_L, dissipates dynamic power P_D, as f, the frequency at which the inverter is being switched [10].

$$P_D = V_{DD}\, C_L\, f \qquad (6)$$

2.2.4 Fan-In and fan-Out

Fan-in of a gate is number of the inputs. In the other hand, the fan-out is the maximum number of similar gates that a gate can drive while remaining within guaranteed specification [10]. The fan-out can reduce V_{OH} and NM_H. This will affect the level of noise in the design.

CHAPTER 3
METHODOLOGY

3.1 Design Flow

In order to design a pulse generator, the author to understand the basic concept of pulse generator it self and make use of all references related. Figure 4 shows the overall design flow for the pulse generator circuit.

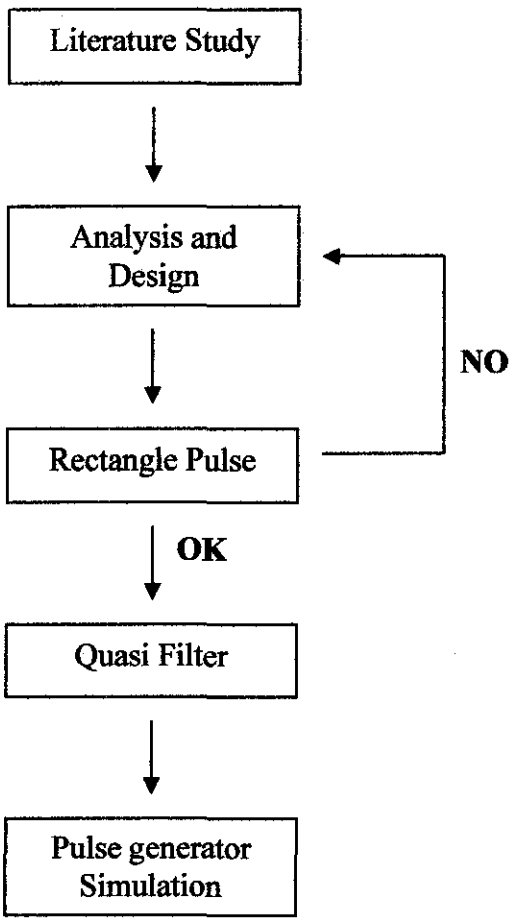

Figure 4: Flow of pulse generator design

3.1.1 Literature Study

Figure 3 shows the design flow for the pulse generator. In the flow chart, the author begins the design phase by doing the literature review. The references such as [5, 9, 10, 14] brief deeply the author the way of designing the pulse generator. Among the focus in activity is to find the suitable logic style and the existing circuit that can implemented for high frequency operation. Among the sources of reference, include:

i. IEEE explore: A lot of references and technical articles that discuss about the pulse generator design generally. These references can be a guild line for designing pulse generator circuit.
ii. UTP library: Most of the technical books are available here.
iii. The Internet: Online resources also provided many references for the circuit design, parameters assumption, fundamental of UWB and others.

3.1.2 Research and Design Consideration

A lot of sources that has been carried out for research on UWB technology and the pulse generator circuit design such as via internet and books that available at library. The pulse generator circuit is based on the CMOS technology. Thus, the author needs to study and understand the fundamental of CMOS circuit design. Reference from [10] refreshed the author a lot to understand the fundamental of designing of CMOS circuit design. Several references describe more details in design of pulse generator circuits with various type of topology and design approach. The most important thing is the design of the pulse generator circuit must fulfill the objective of the project; to design and simulate high frequency pulse generator circuit. Briefly, for this type of design, the modulated signal will be the input of the pulse generator. The designing process developed by using Spectre.

3.1.3 Tools and Equipment Needed

The required software to design pulse generator circuit can be done by using P-spice or Spectre.

CHAPTER 4

GAUSSIAN PULSE GENERATOR

4.1 Introduction

The Federal Communication and Commission (FCC) has classified the three bands range 0-960MHz, 3.1-10.6GHz and 22-29GHz [8]. From the previous designs, the first band will result better low power consumption, lower complexity of design and error and lower complexity. First, the desired wave shape must be determined either impulse based or multiple band pulse will be used for the design. The most popular pulse shape for UWB communication system is the Gaussian pulse due to the accurate location awareness and strong multi-path fading resistance compared to the other pulses. Figure 5 below shows the spectrum mask and occupying a bandwidth of at least 500 MHz or more than 20% of the center frequency, which defined by the FCC. For pulse generator design, it is a requirement of the designers to fulfill the FCC power spectrum mask [18]. The scope of the project is designing the pulse generator circuit which one of the essential part in UWB transmitter showed by Figure 6. As mentioned before, this is one of the designs topology of designing impulse based pulse generator as shown as Figure 7.

CHAPTER 5
SIMULATION RESULTS AND DISCUSSION

5.1 Introduction

As the objectives mentioned earlier, the project required the author to design and simulate pulse generator circuit. It was a successful achievement by the author as the completion of the project. The simulation done by using Virtuoso Analog Design (Spectre) with AMI0.16um CMOS transistor technology. The software is suitable for this project rather than PSPICE or Multisim because the project itself involve micro technology analogue IC design.

5.2 Simulation Setting

In Spectre window, analysis chosen is transient with simulation time 100ns and time step 0.05ns. In this simulation, there is no convergence problem as the time step is sufficiently small to calculate the initial bias point required by Virtuoso analogue Design Environment to complete the job. Figure 15 below shows the essential step which library model setup as its loading the CMOS technology that desired to use. The transient analysis setting setup gives the value of stopping time at 100ns as shows on Figure 16. For the simulation, the supply voltage is 1.8V and bias voltage supplied by the voltage of 1.4V. The value of time constants can be adjusted in three ways. There are varied the transistor sizing, increasing the number of inverters and adding voltage controlled delay element. All three methods have their own advantages and disadvantages. Transistor sizing is simple to design, but it may require huge transistors in the last section. The voltage-controlled delay element can offer flexibility at the cost of an extra control signal but the tuning range is not too high. All three approaches can be applied together in order to get a better result. Figure 17 below shows the delay calculation setting for the rectangle pulse circuit design.

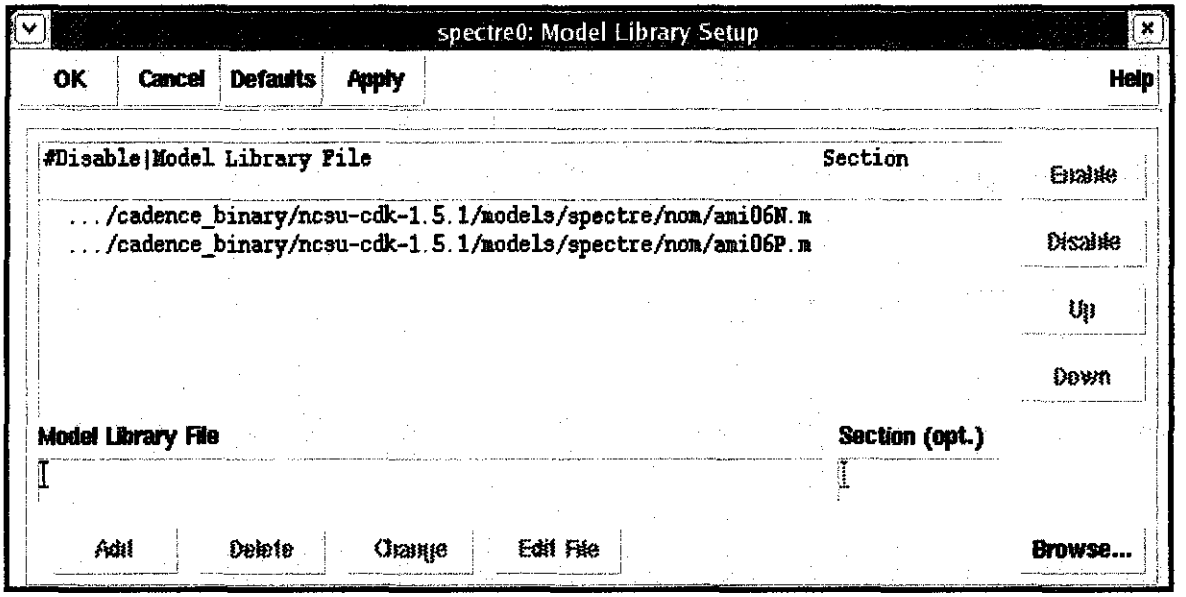

Figure 15: Model library setup for loading the CMOS technology used

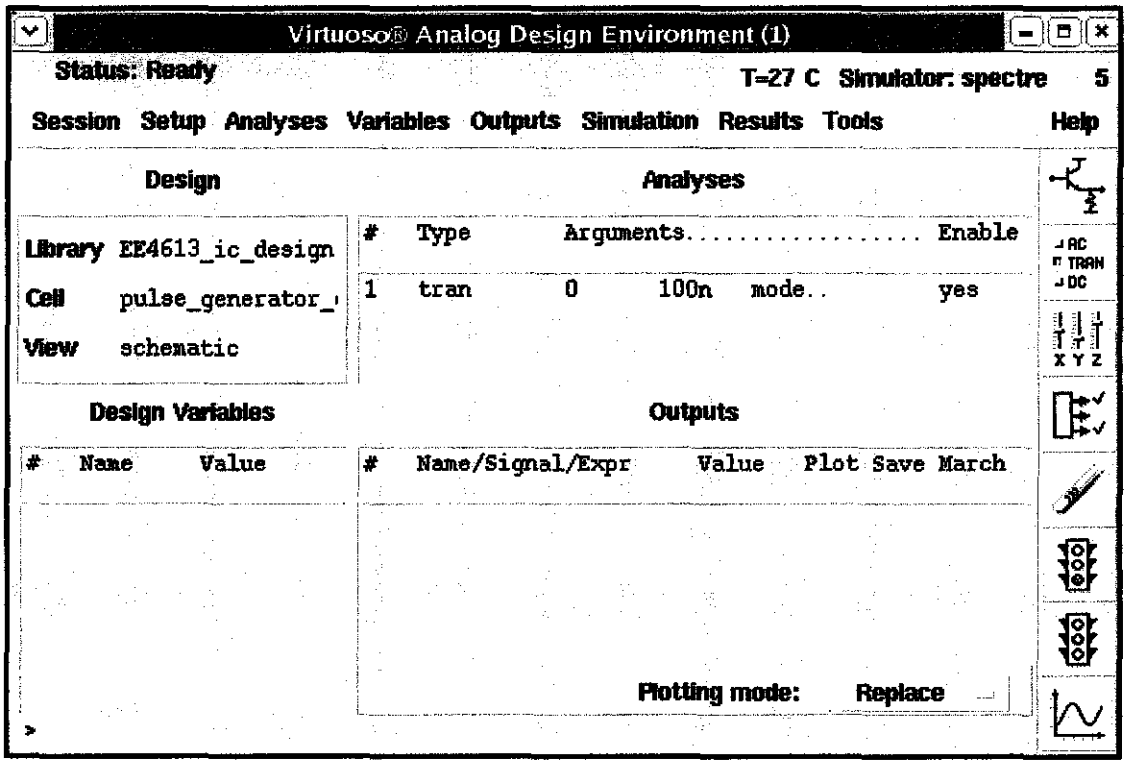

Figure 16: Transient simulation setting

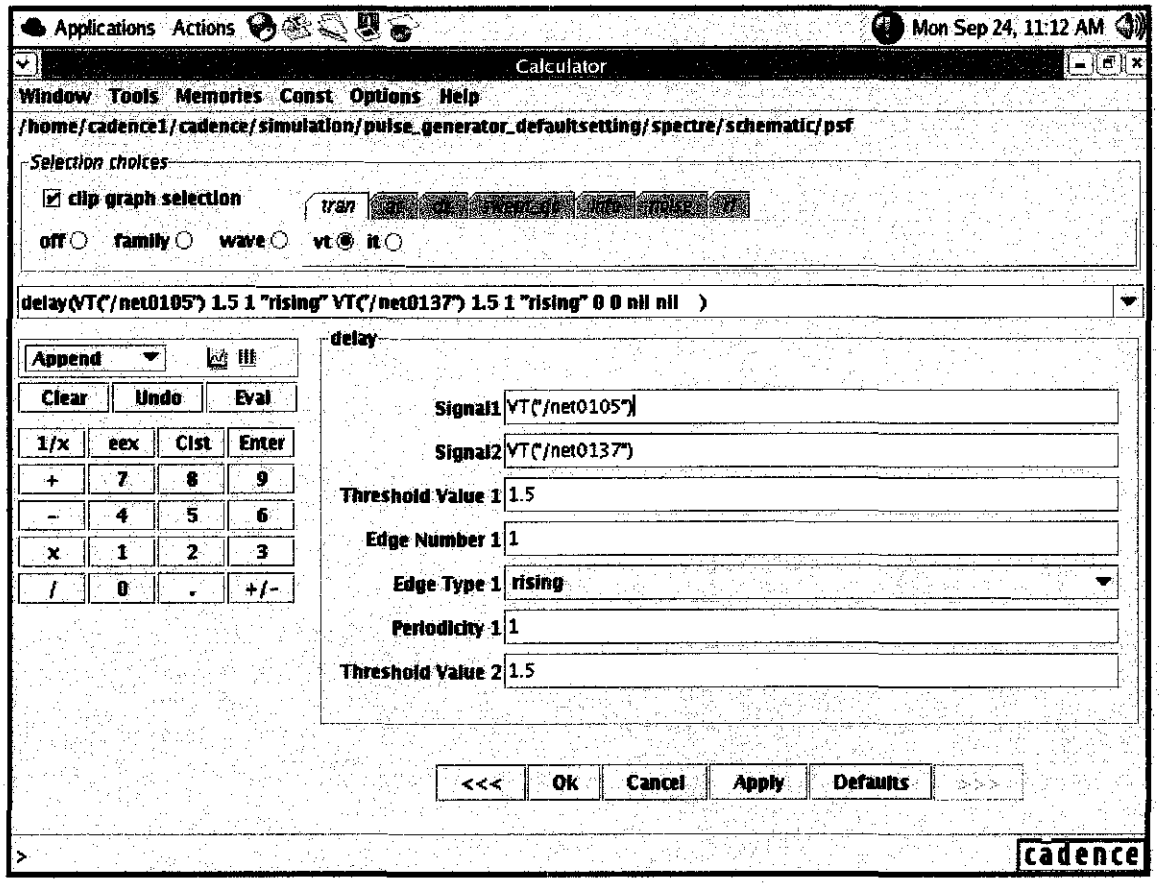

Figure 17: Delay calculation for Rectangle Pulse circuit

5.3 Simulation Result and Discussion

The input of the circuit is set to 100MHz pulse repetition frequency (PRF). The result obtained is approximately same as the theoretical Gaussian pulse. Figure 19 shows the timing diagram and rectangle pulse result. The waveform is obtained from the point represented by the alphabets (Table1), which is showed by Figure 12. To obtain the rectangle pulse, NAND operation is applied to the point C output and point F output as shown in Figure 18. This is the crucial stage where the delay operation time for each inverters and the N-voltage control need to determine first. NAND logic sequence required either one of the inputs to be 0 to obtain positive rectangle pulse. Figure 20 shows the rectangle pulse simulation generated pulse with 500MHz passed frequency.

Table 1: The substitution of waveform labeling

Waveform name	Representation
Input	A
Inverter 1	B
Inverter 2	C
Inverter3	D
Inverter 4	E
NAND Output	F
Rectangle Pulse Output	G
Pulse Output	H

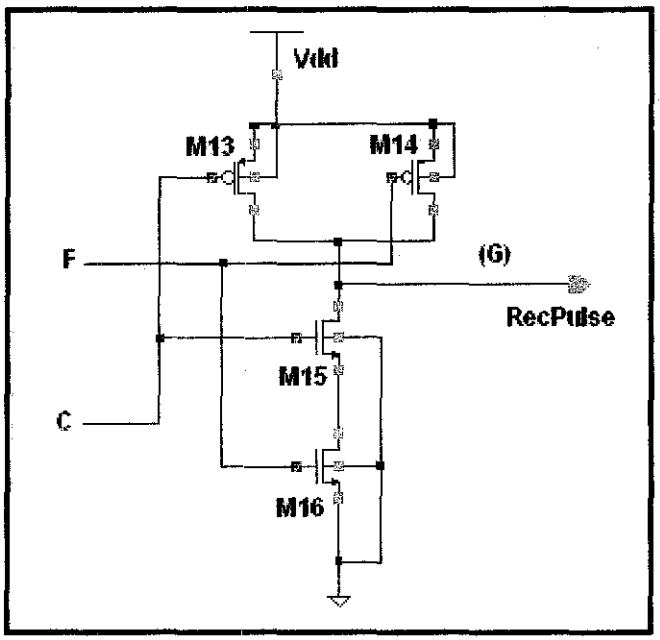

Figure 18: NAND operation applied to obtain the rectangle pulse

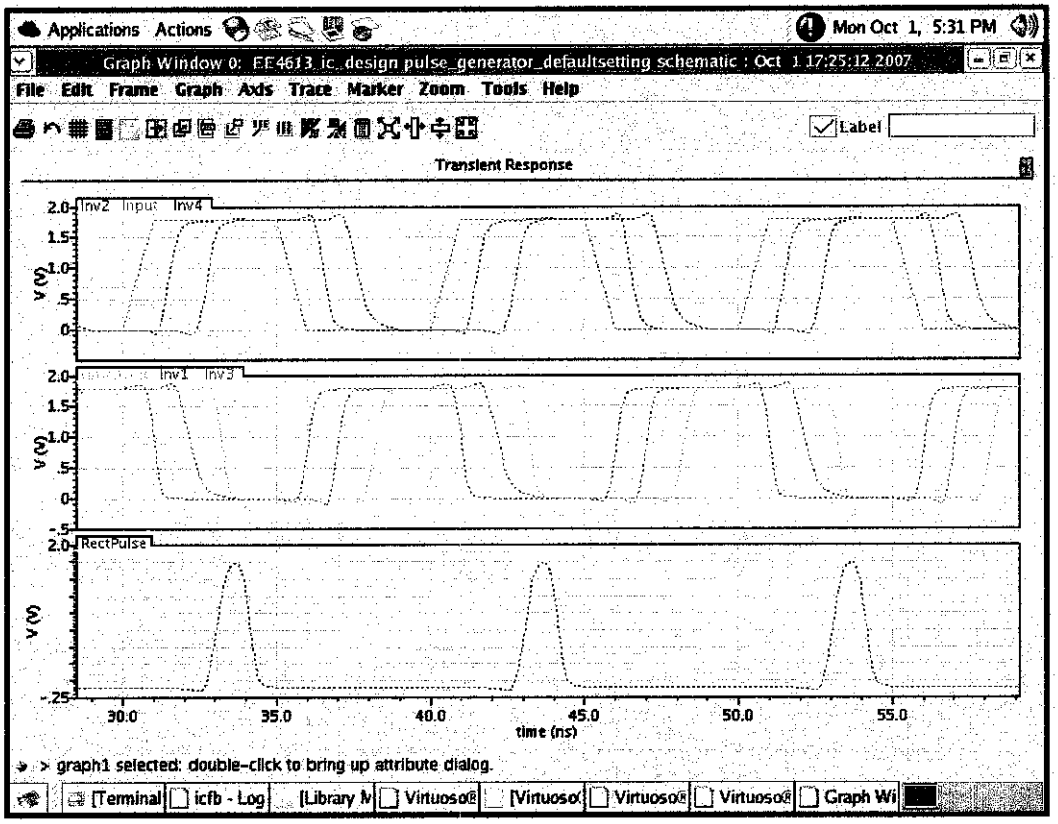

Figure 19: Timing diagram of the pulse generator

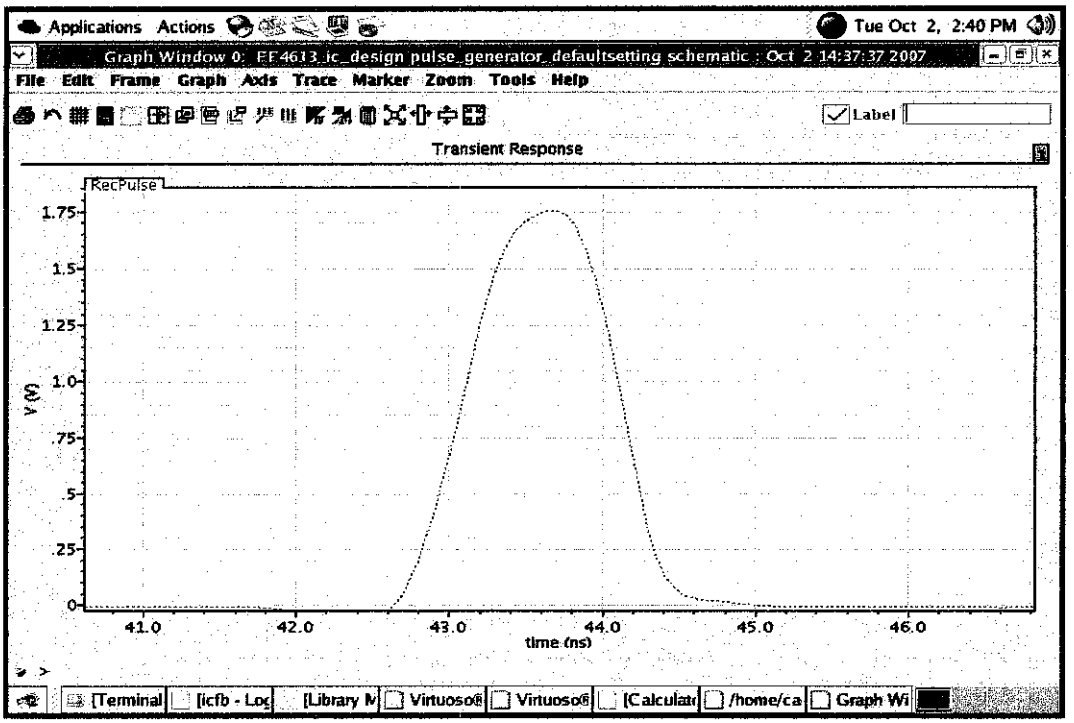

Figure 20: Rectangle pulse output result achieved 500MHz pass frequency

Figure 21 is the evidence for the output result, Gaussian pulse alike. It is better to have different time constants in this $(RC)^n$ filter. The time constants can be increased by decreasing the (W/L) ratios of the transistors. Table 2 shows the aspect ratio transistor value for the design. By decreasing the width of the transistor will be increasing time constant. Furthermore, the gate and diffusion capacitances also decrease resulting in less load capacitances. In the CR-RC circuit described, there is a noticeable undershoot as the pulse attempts to return to the baseline. By using the pole-zero cancellation the peak shape can be improve and eliminates the overshoot. The result is an output pulse exhibiting a simple exponential decay to baseline with the desired differentiator time constant [9]. This circuit uses a zero to cancel a pole in the mathematical representation by complex variables [21]. M7 and M10 act to provide this adjustable resistance through bias control.

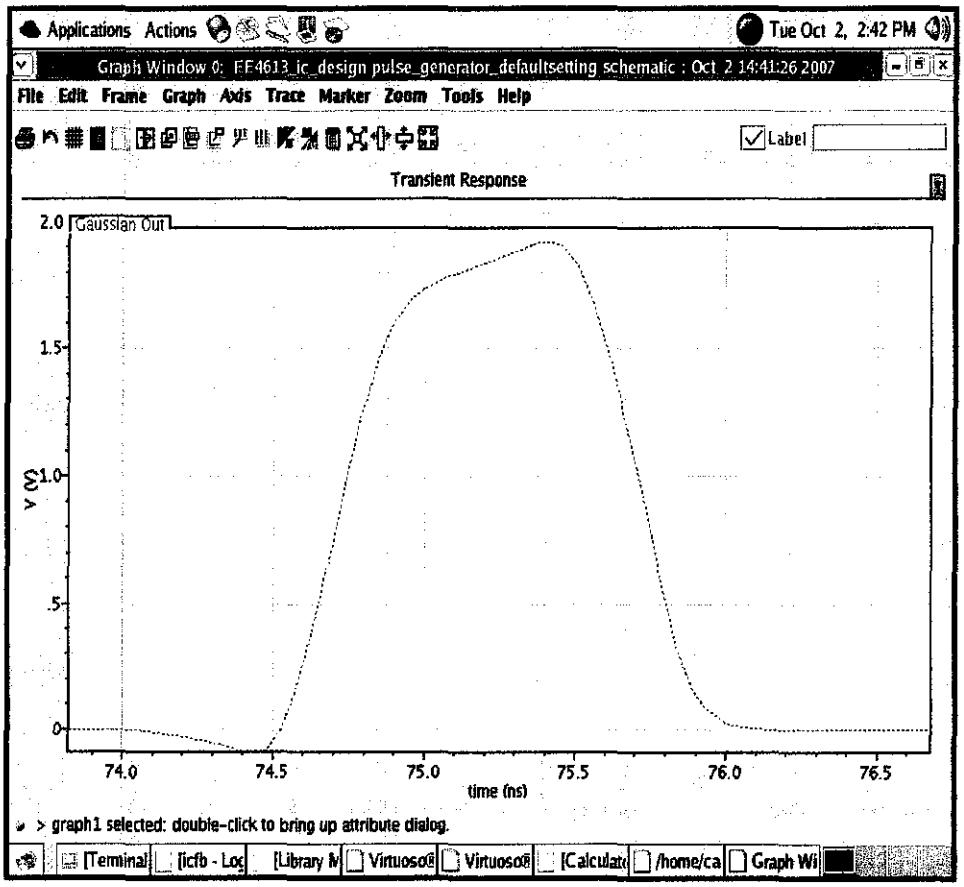

Figure 21: The pulse generator output result achieved 660MHz pass frequency

Table 2: Aspect ratio value of the PMOS and NMOS transistors

AMI 0.6um Aspect Ratio Transistor Technology		
Transistor	Width(um)	Length(nm)
M1	2.4	600
M2	1.5	600
M3	2.4	600
M4	1.5	600
M5	2.4	600
M6	1.5	600
M7	1.5	600
M8	2.4	600
M9	1.5	600
M10	1.5	600
M11	2.4	600
M12	1.5	600
M13	2.4	600
M14	2.4	600
M15	1.5	600
M16	1.5	600
M17	2.0	600
M18	1.2	600
M19	1.9	600
M20	1.5	600
M21	2.4	600
M22	0.9	600
M23	1.8	600
M24	1.5	600

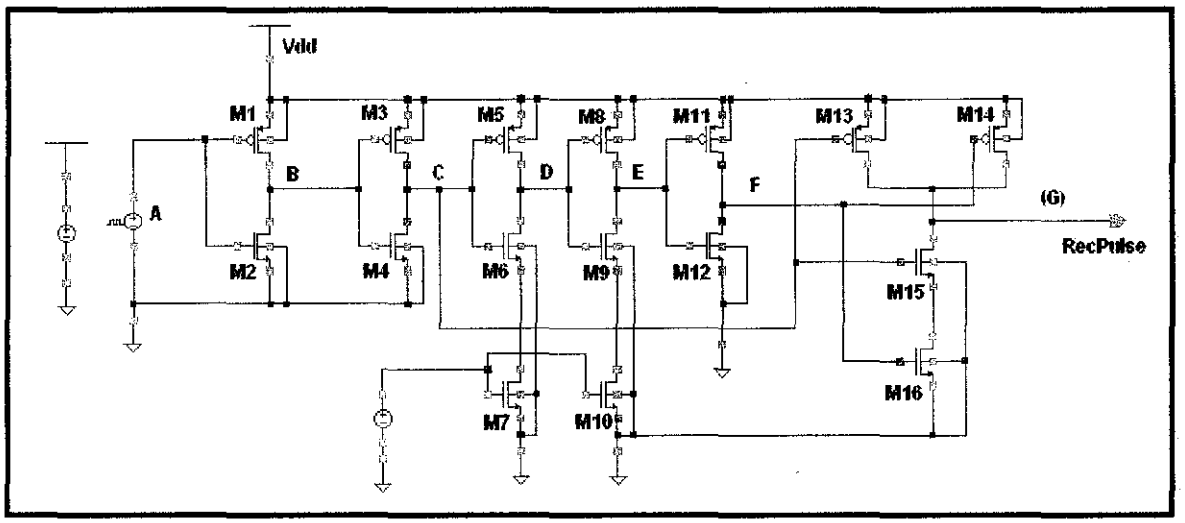

Figure 22: Rectangle pulse generator circuit diagram

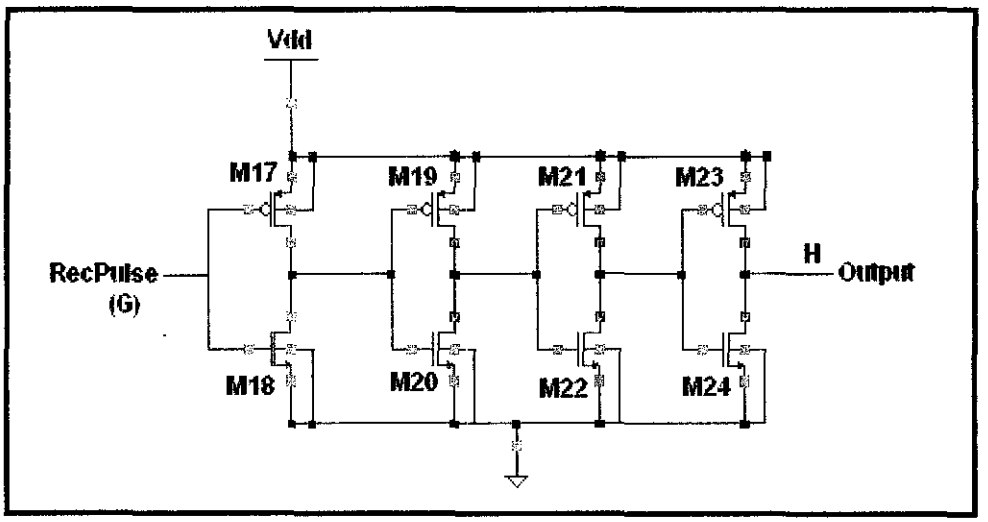

Figure 23: Quasi Gaussian filter circuit diagram

CHAPTER 6
CONCLUSION AND RECOMMENDATIONS

6.1 Conclusion

Throughout the project, the author has become aware of the challenges and complexity in designing integrated circuit for high frequency application. The whole project itself is a new learning process for the author. In particular, the following objectives set in the beginning have been achieved.

i. To design pulse generator at least 500MHz and that can transmit data in high frequency.
ii. To use CMOS logic style in the design. From the simulation, it is verified that the chosen logic style can be used for high frequency application.
iii. To use Spectre cadence software in the circuit simulation. In this project, Spectre has been used extensively, from the modeling until simulation process.

Working on this project has been a constant challenge since the beginning. However, the experience gained and the insight learned is more than what is attained in classroom. Therefore, it is hope that the new found knowledge can be used to design other challenging circuits.

6.2 Recommendations

For two semesters, many things have been learned for completing the project. Even though the project has reached the objectives, there are some improvements to be made for better result. Some of the recommendations are specifically include;

6.2.1 Design with Different Topology

From the references that have been used, there are various pulse generator circuit design with different approach. One interesting approach of designing the pulse generator is using the H-bridge circuit and off chip filter as reported by [20]. The features of H-bridge, which provide balanced positive and negative currents, are suitable for generating the antipodal UWB pulse. The circuit design is also implementing below 1GHz UWB system. Interesting study of various pulse comparisons includes power consumptions and antenna effect consideration in the design.

6.2.2 Design Applications Improvement

In this design, the author makes assumption of high frequency input for generating the pulse. The scope of the project required to generate the pulse generator. Thus, for the next improvement the author suggests to implement the pulse generator in the application design such as reported by [7, 2]. The applications of UWB are very interesting to explore and implementing it to the daily life such as WPAN and RFID technology. The world nowadays urged wireless connection and reduced the wired connection. The assumption is made due to the complexity of the modulation circuit design (creating the high frequency pulse from the low frequency)

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APPENDICES

Appendix A: PMOS transistor process parameter

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* N8BN SPICE BSIM3 VERSION 3.1 (HSPICE Level 49) PARAMETERS
* Level 11 for Cadence Spectre
* DATE: Jan 25/99
* LOT: n8bn                    WAF: 03
* Temperature_parameters=Default
.MODEL ami06P PMOS ( LEVEL=11 &
VERSION=3.1 &
TNOM=27 &
TOX=1.41E-8 &
XJ=1.5E-7 &
NCH=1.7E17 &
VTH0=-0.9179952 &
K1=0.5575604 &
K2=0.010265 &
K3=14.0655075 &
K3B=-2.3032921 &
W0=1.147829E-6 &
NLX=1.114768E-10 &
DVT0W=0 &
DVT1W=5.3E6 &
DVT2W=-0.032 &
DVT0=2.2896412 &
DVT1=0.5213085 &
DVT2=-0.1337987 &
U0=202.4540953 &
UA=2.290194E-9 &
UB=9.779742E-19 &
UC=-3.69771E-11 &
VSAT=1.307891E5 &
A0=0.8356881 &
AGS=0.1568774 &
B0=2.365956E-6 &
--  ami06P.m          (ObjC Abbrev)--L32--Top----------------------
Write file: /tmp/fr-BU81C1/ncsu-cdk-1.5.1/models/spectre/nom/
```

```
B1=5E-6 &
KETA=-5.769328E-3 &
A1=0 &
A2=1 &
RDSW=2.746814E3 &
PRWG=2.34865E-3 &
PRWB=0.0172298 &
WR=1 &
WINT=2.586255E-7 &
LINT=7.205014E-8 &
XL=0 &
XW=0 &
DWG=-2.133054E-8 &
DWB=9.857534E-9 &
VOFF=-0.0837499 &
NFACTOR=1.2415529 &
CIT=0 &
CDSC=4.363744E-4 &
CDSCD=0 &
CDSCB=0 &
ETA0=0.11276 &
ETAB=-2.9484E-3 &
DSUB=0.3389402 &
PCLM=4.9847806 &
PDIBLC1=2.481735E-5 &
PDIBLC2=0.01 &
PDIBLCB=0 &
DROUT=0.9975107 &
PSCBE1=3.497872E9 &
PSCBE2=4.974352E-9 &
--  nmi06P.m          (ObjC Abbrev)--L44--38%------------------
Write file: /tmp/fr-BU81C1/ncsu-cdk-1.5.1/models/spectre/nom/
```

```
PVAG=10.9914549 &
DELTA=0.01 &
MOBMOD=1 &
PRT=0 &
UTE=-1.5 &
KT1=-0.11 &
KT1L=0 &
KT2=0.022 &
UA1=4.31E-9 &
UB1=-7.61E-18 &
UC1=-5.6E-11 &
AT=3.3E4 &
WL=0 &
WLN=1 &
WW=0 &
WWN=1 &
WWL=0 &
LL=0 &
LLN=1 &
LW=0 &
LWN=1 &
LWL=0 &
CAPMOD=2 &
XPART=0.4 &
CGDO=2.4E-10 &
CGSO=2.4E-10 &
CGBO=0 &
CJ=7.273568E-4 &
PB=0.9665597 &
MJ=0.4959837 &
CJSW=3.114708E-10 &
PBSW=0.99 &
--  nmi06P.m          (ObjC Abbrev)--L79--69%------------------
Write file: /tmp/fr-BU81C1/ncsu-cdk-1.5.1/models/spectre/nom/
```

```
WWL=0 &
LL=0 &
LLN=1 &
LW=0 &
LWN=1 &
LWL=0 &
CAPMOD=2 &
XPART=0.4 &
CGDO=2.4E-10 &
CGSO=2.4E-10 &
CGBO=0 &
CJ=7.273568E-4 &
PB=0.9665597 &
MJ=0.4959837 &
CJSW=3.114708E-10 &
PBSW=0.99 &
MJSW=0.2653654 &
PVTH0=9.420541E-3 &
PRDSW=-231.2571566 &
PK2=1.396684E-3 &
WKETA=1.862966E-3 &
LKETA=5.728589E-3     )
```

```
--  ami06P.m          (ObjC Abbrev)--L101--Bot------------------
Write file: /tmp/fr-BU81C1/ncsu-cdk-1.5.1/models/spectre/nom/
```

Appendix B: NMOS transistor process parameter

```
N8BN SPICE BSIM3 VERSION 3.1 (HSPICE Level 49) PARAMETERS
* level 11 for Cadence Spectre
* DATE: Jan 25/99
* LOT: n8bn                    WAF: 03
* Temperature_parameters=Default
.MODEL ami06N NMOS ( LEVEL=11 &
VERSION=3.1 &
TNOM=27 &
TOX=1.41E-8 &
XJ=1.5E-7 &
NCH=1.7E17 &
VTH0=0.7086 &
K1=0.8354582 &
K2=-0.088431 &
K3=41.4403818 &
K3B=-14 &
W0=6.480766E-7 &
NLX=1E-10 &
DVT0W=0 &
DVT1W=5.3E6 &
DVT2W=-0.032 &
DVT0=3.6139113 &
DVT1=0.3795745 &
DVT2=-0.1399976 &
U0=533.6953445 &
UA=7.558023E-10 &
UB=1.181167E-18 &
UC=2.582756E-11 &
VSAT=1.300981E5 &
A0=0.5292985 &
AGS=0.1463715 &
B0=1.283336E-6 &
B1=1.408099E-6 &
KETA=-0.0173166 &
A1=0 &
```

```
KETA=-0.0173166 &
A1=0 &
A2=1 &
RDSW=2.268366E3 &
PRWG=-1E-3 &
PRWB=6.320549E-5 &
WR=1 &
WINT=2.043512E-7 &
LINT=3.034496E-8 &
XL=0 &
XW=0 &
DWG=-1.446149E-8 &
DWB=2.077539E-8 &
VOFF=-0.1137226 &
NFACTOR=1.2880596 &
CIT=0 &
CDSC=1.506004E-4 &
CDSCD=0 &
CDSCB=0 &
ETA0=3.815372E-4 &
ETAB=-1.029178E-3 &
DSUB=2.173055E-4 &
PCLM=0.6171774 &
PDIBLC1=0.185986 &
PDIBLC2=3.473187E-3 &
PDIBLCB=-1E-3 &
DROUT=0.4037723 &
PSCBE1=5.998012E9 &
PSCBE2=3.788068E-8 &
PVAG=0.012927 &
DELTA=0.01 &
MOBMOD=1 &
PRT=0 &
UTE=-1.5 &
KT1=-0.11 &


KT2=0.022 &
UA1=4.31E-9 &
UB1=-7.61E-18 &
UC1=-5.6E-11 &
AT=3.3E4 &
WL=0 &
WLN=1 &
WW=0 &
WWN=1 &
WWL=0 &
LL=0 &
LLN=1 &
LW=0 &
LWN=1 &
LWL=0 &
CAPMOD=2 &
XPART=0.4 &
CGDO=1.99E-10 &
CGSO=1.99E-10 &
CGBO=0 &
CJ=4.233802E-4 &
PB=0.9899238 &
MJ=0.4495859 &
CJSW=3.825632E-10 &
PBSW=0.1082556 &
MJSW=0.1083618 &
PVTH0=0.0212852 &
PRDSW=-16.1546703 &
PK2=0.0253069 &
WKETA=0.0188633 &
LKETA=0.0204965        )
```