DOWNSCALING OF 0.25μM TO 0.13μM NMOS USING SILVACO SOFTWARE WITH DIFFERENT SUBMICRON TECHNOLOGY

By

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FINAL PROJECT REPORT

Submitted to the Electrical & Electronics Engineering Programme
in Partial Fulfillment of the Requirements
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Bachelor of Engineering (Hons)
(Electrical & Electronics Engineering)

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CERTIFICATION OF APPROVAL

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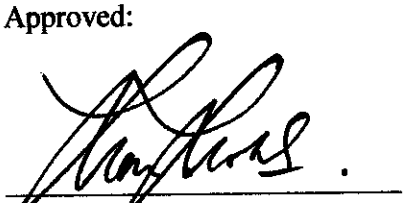
Approved:



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June 2007

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

Norliza binti Mohd Supian

ABSTRACT

For the last three decades, MOS device technologies have been improved due to downscaling. It consumes less power, have shorter delay and occupy less space. The CMOS comprises of p-type and n-type, has become the main growth of miniaturization microelectronics industry. In this project, ATHENA and ATLAS are simulators used with the objective to downscale 0.25μm to 0.13μm NMOS using two different recipes and to obtain its electrical characteristic. A scaling factor, α of 1.923 is utilized. Three factors are investigated; the gate length (L_G), gate oxide thickness (t_{ox}) and threshold voltage (V_{TH}) adjust implant. The parameters evaluated include t_{ox}, V_{TH} and saturation current (I_{Dsat}) as well as I_D-V_D, I_D-V_G and subthreshold current (S_t) curve. After downscaling to 0.13μm, both recipes have t_{ox} values of 3.36nm while the V_{TH} obtain are 0.31V and 0.37V respectively. The I_{Dsat} value is 343μA/μm and 519μA/μm while the S_t is 65mV/dec and 128mV/dec respectively. Each recipe has its own drawback. First recipe has lower I_{Dsat} and lower S_t while second recipe has higher I_{Dsat} and higher S_t. Higher I_{Dsat} means the device can perform at faster speed while lower S_t shows the device has good turn-off characteristics. Overall, the electrical parameters obtained are agreeable with ITRS requirement and other reported works except for the result of I_{Dsat}. This could be due to the direct scaling. Other parameters such as S_t could not be compared as it is confidential to the public.

ACKNOWLEDGEMENTS

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LIST OF ABBREVIATIONS

BF_2	Boron diflouride
CMOS	Complementary metal oxide semiconductor
I_D	Drain current
I_{Dsat}	Saturation current
ITRS	International Technology Roadmap Semiconductor
LDD	Lightly doped drain
Lg	Gate length
LOCOS	Local oxidized silicon
NMOS	n-channel metal oxide semiconductor
PSG	Phosphor silicate glass
RTA	Rapid thermal annealing
SD	Source drain
S_t	Subthreshold current
TI	Texas instrument
t_{ox}	Gate oxide thickness
TSMC	Taiwan semiconductor manufacturing company
V_D / V_{DD}	Drain voltage
V_G	Gate voltage
V_{TH}	Threshold voltage

CHAPTER 1
INTRODUCTION

1.1 Background of Study

For the last few decades, the semiconductor industry has seen rapid pace of improvement in its products. The improvement trends also known as scaling are shown in *Table 1.* [1] These improvements allow fabrication of the devices and circuits in smaller dimensions. Device component dimensions are characterized by the smallest dimension in the design. This is called the feature size and is usually expressed in microns or nanometers. A micron is 1/1,000,000 of a meter or about 1/100 the diameter of a human hair. It also allows device to have greater circuit performance, power control and reliability. [2]

Table 1 Improvement trends for ICs enabled by feature scaling

Trend	**Level**
Cost	Cost per function
Speed	Microprocessor clock rate, GHz
Power	Laptop or cell phone battery life
Compactness	Small and light weight product

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is the basic element of the Integrated Circuits (IC). Therefore it becomes the most important microelectronic device in IC. The complementary metal oxide semiconductor (CMOS) uses both n-type and p-type of MOS transistors. It offers high speed performance and low power

dissipation. The scaling of CMOS has known as a backbone of the growth for semiconductor industry.

1.2 Problem Statement

Downscaling of NMOS transistors will change its operational characteristics. However, it becomes problematic as the scaling enters the deep submicron region. Short channel effect or submicron effects can be observed. The scaling of the gate oxide in deep submicron region will increase the gate direct tunneling current. Off-state leakage also increases with reduction of the gate length. Both of these effects contribute to the increase in power dissipation.

1.3 Objective and Scope of Study

The objective of this project is to design and downscale the 0.25μm NMOS technology to 0.13μm NMOS technology and to characterize its electrical properties with different submicron technologies. The first recipe was obtained from the 0.5μm NMOS laboratory manual while the second recipe was obtained from Noraini Othman.

This needs deep understanding of the NMOS fabrication process as well as its electrical properties. Knowledge of current scaling trend in industry level is a must and its effect in device performance. However, there are difficulties of obtaining this knowledge. This knowledge is only available in semiconductor industry thus it is strictly treated as confidential.

Due to complexity of the device design, simulators play important role in IC industry. With simulation, it allows the author to have better understanding of the fabrication process as it provides internal view processes. In this work, the NMOS fabrication and downscaling process is done with two modules of SILVACO software. ATHENA is utilized to simulate fabrication process while ATLAS is utilized to characterize its electrical properties. Therefore, depth knowledge of using these modules is required.

CHAPTER 2
LITERATURE REVIEW

2.1 Scaling

Scaling of MOS transistors is concerned with systematic reduction of overall dimensions of the devices while preserving the geometric ratios found in the larger device. This is illustrates in *Figure 1.* The proportional scaling of all devices in a circuit would certainly result in a reduction of total silicon area occupied by the circuit, thereby increasing the overall functional density of the chip. [3]

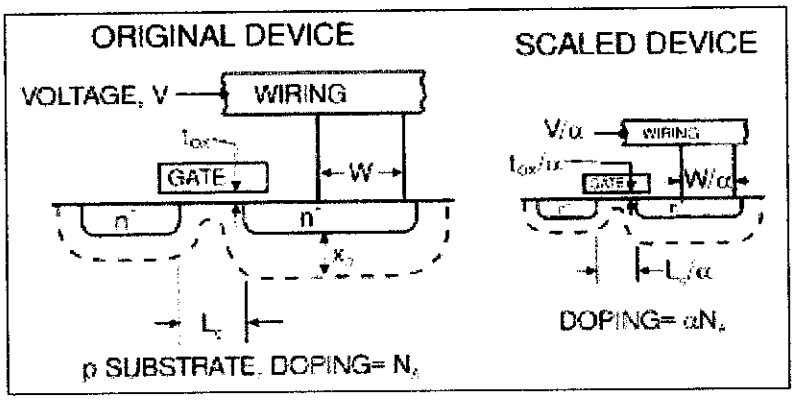

Figure 1 Schematic illustration of scaling by factor α

There are two approaches available in down scaling which is constant field scaling and constant voltage scaling. Consider factor scaling as α. *Table 2* summarizes the scaling steps as a guideline.

Table 2 Scaling properties of silicon MOSFET

Physical Parameters	Before Scaling	After Scaling	
		Constant Field	Constant Voltage
Channel length	L	$L' = L / \alpha$	$L' = L / \alpha$
Gate oxide thickness	t_{ox}	$t_{ox}' = t_{ox} / \alpha$	$t_{ox}' = t_{ox} / \alpha$
Junction depth	x_j	$x_j' = x_j / \alpha$	$x_j' = x_j / \alpha$
Power supply voltage	V_{DD}	$V_{DD}' = V_{DD} / \alpha$	V_{DD}
Threshold voltage	V_{TH}	$V_{TH}' = V_{TH} / \alpha$	V_{TH}
Doping densities	N_A	$N_A' = \alpha . N_A$	$N_A' = \alpha^2 . N_A$
	N_D	$N_D' = \alpha . N_D$	$N_D' = \alpha^2 . N_D$
Drain current	I_D	$I_D' = I_D / \alpha$	$I_D' = \alpha . I_D$
Power dissipation	P	$P' = P / \alpha^2$	$P' = \alpha . P$

2.1.1 Constant field scaling

For constant field scaling, the dimensions are scaled down by factor of α as well as power supply voltage and all terminal voltages. The most attractive features are the significant reduction of power dissipation. This contributes to overall performance improvement. However, the scaling of voltages may not be very practical in many cases especially when goes towards submicron region. [3]

2.1.2 Constant voltage scaling

In constant voltage scaling, all dimensions are reduced by factor of α however power supply voltage and terminal voltages remain unchanged. It is usually preferred than constant field scaling. Certain voltage level may be required in all input and output voltages for some devices. However, it posses other problem as it increases the drain current as well as power dissipation. [3]

2.1.3 General scaling

Hence, the other method is introduced. General scaling method use combination of constant filed and constant voltage scaling. The voltages and dimensions are scaled with different factors. For example dimensions are scaled by factor of κ while voltages are scaled by factor of U. Supply voltage is being scaled but at a slower rate than feature size. *Table 3* summarizes the concept of general scaling. [4]

Table 3 General scaling

Physical Parameters	**Before Scaling**	**After Scaling**
Channel length	L	$L' = L / \kappa$
Gate oxide thickness	t_{ox}	$t_{ox}' = t_{ox} / \kappa$
Power supply voltage	V_{DD}	$V_{DD}' = V_{DD} / U$
Threshold voltage	V_{TH}	$V_{TH}' = V_{TH} / U$
Doping densities	N_A	$N_A' = (\kappa^2 / U).N_A$
	N_D	$N_D' = (\kappa^2 / U).N_D$

2.2 Downscaling Challenges: Short Channel Effects

Reduction of channel length requires some other device parameters to be properly adjusted to avoid possible adverse effects.

2.2.1 Punch through

One of the things that may happen when the channel is shortened is that the drain field may start taking electrons directly from the source. This is illustrated in *Figure 2.* At high drain bias, the drain takes control of current through the device. Excessive heating can occur and cause the device failure. [5]

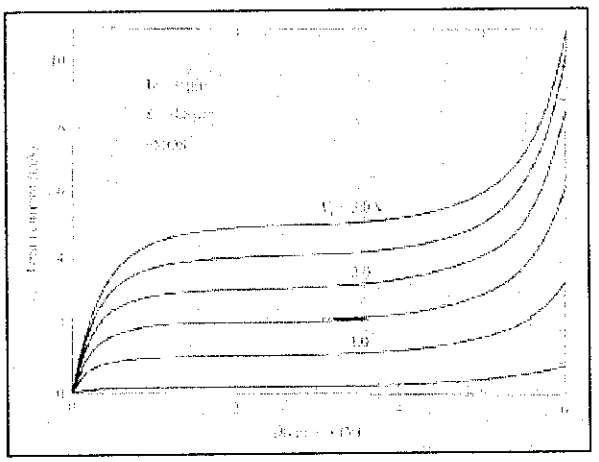

Figure 2 Punch through effect

2.2.2 Threshold voltage roll-off

The smaller the gate length, the more influence drain region has on channel potential. The threshold voltage, V_{TH} with very short channel can be reduced significantly. As a result, the off-state leakage increases and the variation of V_{TH} also become much larger in roll-off region. For small enough gate lengths, the devices will be on at 0 V. This is illustrated in *Figure 3.* [5]

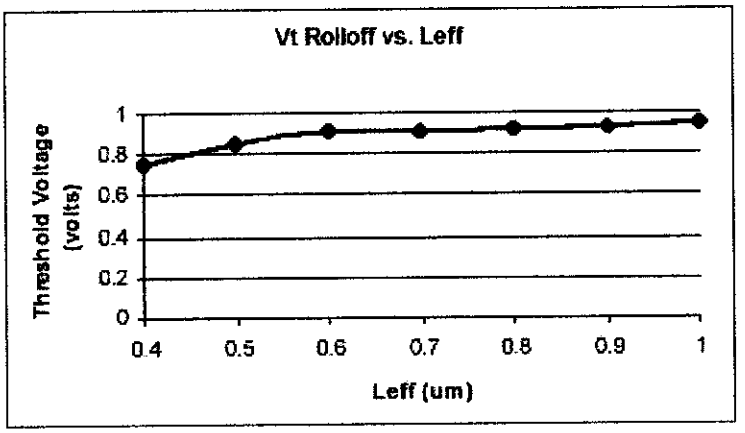

Figure 3 Threshold voltage roll-off

2.2.3 *Drain induced barrier lowering (DIBL)*

When the device is scaled down, the drain region moves closer to the source. Refer to *Figure 4.* In this situation, the drain induced electric field plays a role in attracting carriers to channel without control from the gate terminal. The drain now lowers the potential barrier for source carriers to form the channel. With increasing in drain voltage, the off-state leakage also increases. If gate were in full control, these curves would be one on top of the other. [5]

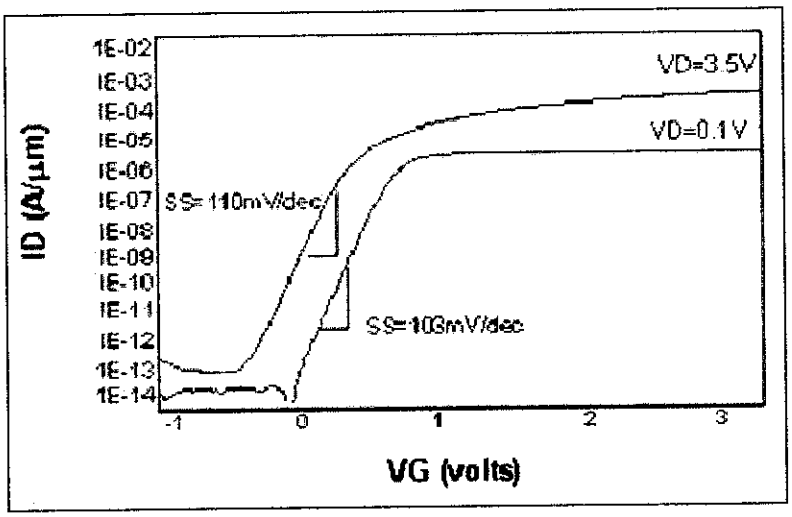

Figure 4 Drain induced barrier lowering

2.2.4 *Subthreshold current*

It is the drain-source current when the gate-source voltage is below the threshold voltage. Smaller transistors require lower operating voltages to restrict the internal electric field. Thus to maintain the device operating speed, lower threshold voltage is required. However this increases transistor leakage since there is substantial amount of current during the off state. [6]

2.2.5 Channel length modulation

Channel length modulation in a MOSFET is caused by the increase of the depletion layer width at the drain as the drain voltage is increased. This leads to a shorter channel length and an increased drain current. An example is shown in *Figure 5*. The channel-length-modulation effect typically increases in small devices with low-doped substrates. An extreme case of channel length modulation is punch through where the channel length reduces to zero. Proper scaling can reduce channel length modulation, namely by increasing the doping density as the gate length is reduces. [7]

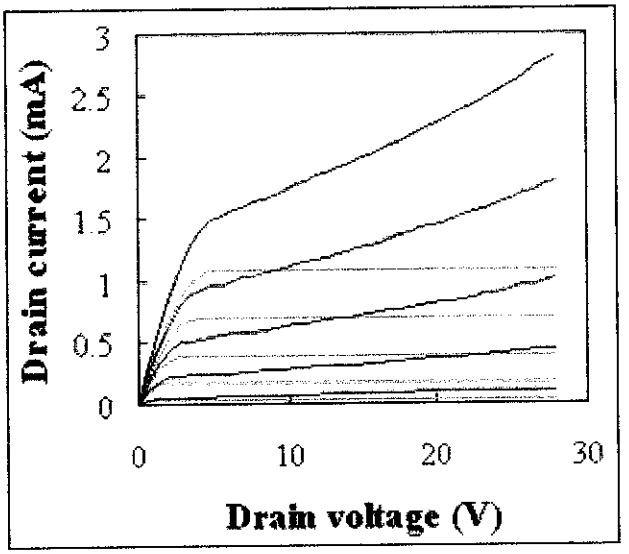

Figure 5 Channel length modulation effect

CHAPTER 3
METHODOLOGY

This chapter provides an overview of device process simulation in designing 0.13μm NMOS. There were two recipes involved, namely known as submicron technology 1 (Sub Tech 1) and submicron technology 2 (Sub Tech 2). The first recipe was obtained from 0.5μm NMOS of the manual laboratory. It served as a design basis for first recipe. The second recipe of 0.25μm NMOS was obtained from Noraini Othman's thesis master. It served as a design basis for second recipe. A comparison was made between these two recipes.

3.1 Procedures

3.1.1 Submicron technology 1

To obtain the 0.13μm NMOS, the basis design of 0.5μm NMOS was scaled down bit by bit to 0.35μm, 0.25μm, 0.18μm and 0.13μm. The structure of NMOS was obtained. Next, electrical characteristics were obtained to evaluate its performances when scaling process took place.

The parameters selected for scaling purposes were the gate length (L_G), gate oxide thickness (t_{ox}), the threshold voltage adjust implant and supply voltage (V_{DD}). The detailed scaling was as listed as below.

1. To decrease the channel length, gate patterning was defined by etched poly at left of x-axis. If the etch was done farther, the gate would be shorter.

POLY DEFINITION
*etch polysilicon left p1.x=**0.13***

2. To reduce the gate oxide thickness as ITRS requirement, the temperature or the time of the gate oxidation should be reduced. For this project, the time was varied while the temperature remained constant.

   # GATE OXIDATION
   *diffus time=**1.5** temp 950 dryo2 press=1.00 hcl.pc=3*

3. To obtain threshold voltage as ITRS required adjustment should be done at boron doping. Increasing the boron doping would increase the threshold voltage.

   # THRESHOLD VOLTAGE ADJUST IMPLANT
   *implant boron dose=**40.5e11** energy=2.6 tilt=7° rotation=0 crystal*

4. Last but not least, the scaled device should have scaled terminal voltages. Therefore the magnitude of all voltages should be reduced as ITRS requirement.

The scaling factor would be differed for each different gate length required. *Table 4* below is the summary of the scaling factor, α utilized in simulation.

Table 4 The scaling factor for Submicron Technology 1

Node Technology	**Scaling Factor**
0.35μm	0.50μm / 0.35μm = 1.428
0.25μm	0.35μm / 0.25μm = 1.400
0.13μm	0.25μm / 0.13μm = 1.923

3.1.2 Submicron technology 2

To obtain the 0.13μm NMOS, the basis design of 0.25μm NMOS was scaled down to 0.13μm. The structure of NMOS was then obtained. Next, electrical characteristics were obtained to evaluate its performances when scaling process took place.

The parameters selected for scaling purposes were the gate length (L_G), gate oxide thickness (t_{ox}), the threshold voltage adjust implant and supply voltage (V_{DD}). The detailed scaling was as listed as below.

1. To decrease the channel length, gate patterning was defined by etched poly at left of x-axis. If the etch was done farther, the gate would be shorter.

   # ETCH POLYSILICON
   etch poly left p1.x=-0.091

2. To reduce the gate oxide thickness as ITRS requirement, the temperature or the time of the gate oxidation should be reduced. For this project, the time was varied while the temperature remained constant.

   # OXIDIZE THE GATE (3.2-3.4nm)
   method grid.oxide=0.004
   diffus time=25 temp=850 dryo2
   diffus time=30 temp=1000 nitro

3. To obtain threshold voltage as ITRS required adjustment should be done at boron doping. Increasing the boron doping would increase the threshold voltage.

   # NVT IMPLANT BORON TO SHIFT THE THRESHOLD
   ***implant bf2 dose=5.6e12** energy=50 tilt=0 rotation=0 pears unit.damage*

4. Last but not least, the scaled device should have scaled terminal voltages. Therefore the magnitude of all voltages should be reduced as ITRS requirement.

Table 5 below is the summary of the scaling factor, α utilized in simulation.

Table 5 The scaling factor utilized for Submicron Technology 2

Node Technology	Scaling Factor
0.13μm	0.25μm / 0.13μm = 1.923

3.2 Tools utilized: SILVACO software

Instead of going through an expensive and time consuming fabrication process, computer simulations could be used to predict electrical characteristics of a device design quickly and cheaply.

Thus, TCAD (Technology Computer Aided Design) was used in this project which was SILVACO software. SILVACO software enabled modeling process to be done such as simulation of the fabrication process. Device modeling and simulation could then be used to predict the electrical characteristics of the given device structure. This gave the author better understanding on various design parameters on device performance. Furthermore, it allowed the investigating of different internal quantities that were not available experimentally.

From all of seven modules available, only two modules were required to conduct this project which was ATHENA and ATLAS. The SILVACO software provided two modules:

3.2.1 The ATHENA module

ATHENA was a simulator that provides general capabilities for numerical, physically-based, two dimensional simulation of semiconductor processing. It provided features such as deposition, diffusion, etch, implantation oxidation, and metallization.

Athena input was a text file. The deckbuild window had two parts; upper window contains commands while lower window displayed comments and results as program ran.

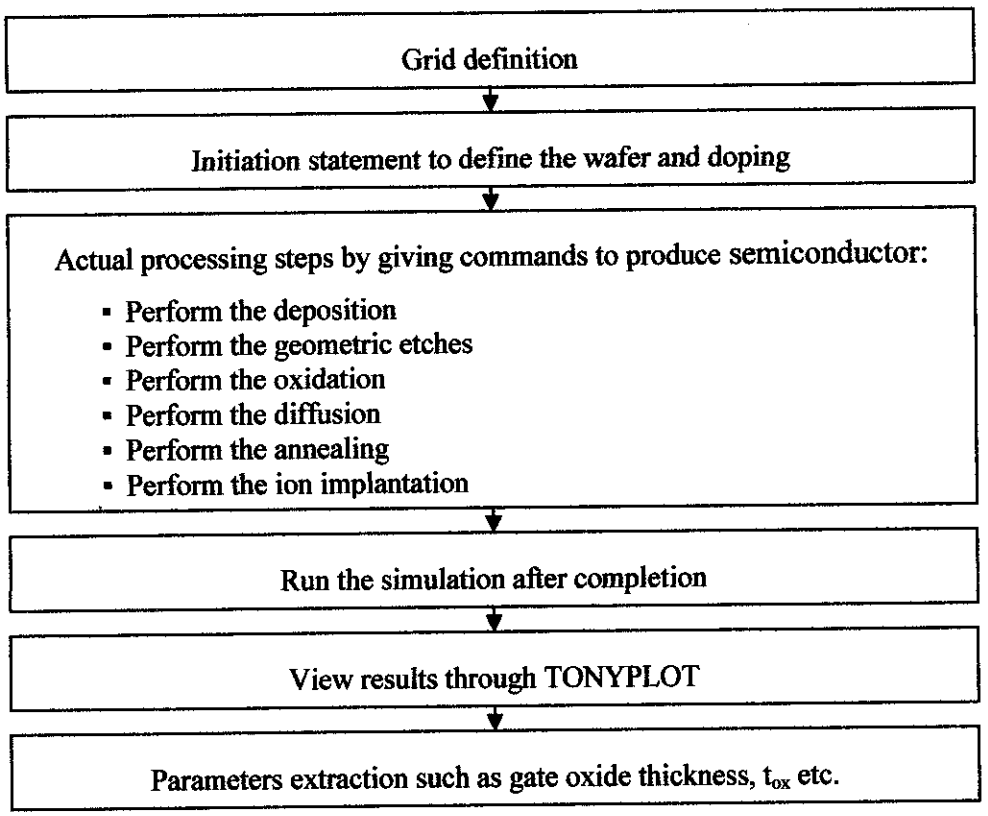

Figure 6 Process of running the ATHENA

3.2.2 The ATLAS module

ATLAS is a physically-based device simulator. It is often used in conjunction with the ATHENA which predicts the physical structures that result from processing steps. The resulting physical structures are used as input by ATLAS, which then predicts the electrical characteristics associated with specified bias conditions. Each input file must contain five groups of statements in correct order.

Table 6 ATLAS command group with primary statement

Group	**Statements**
Structure specification	Mesh, region, electrode, doping
Materials model specification	Material, models, contact, interface
Numerical method selection	Method
Solution specification	Log, solve, load, save
Result analysis.	Extract, tonyplot

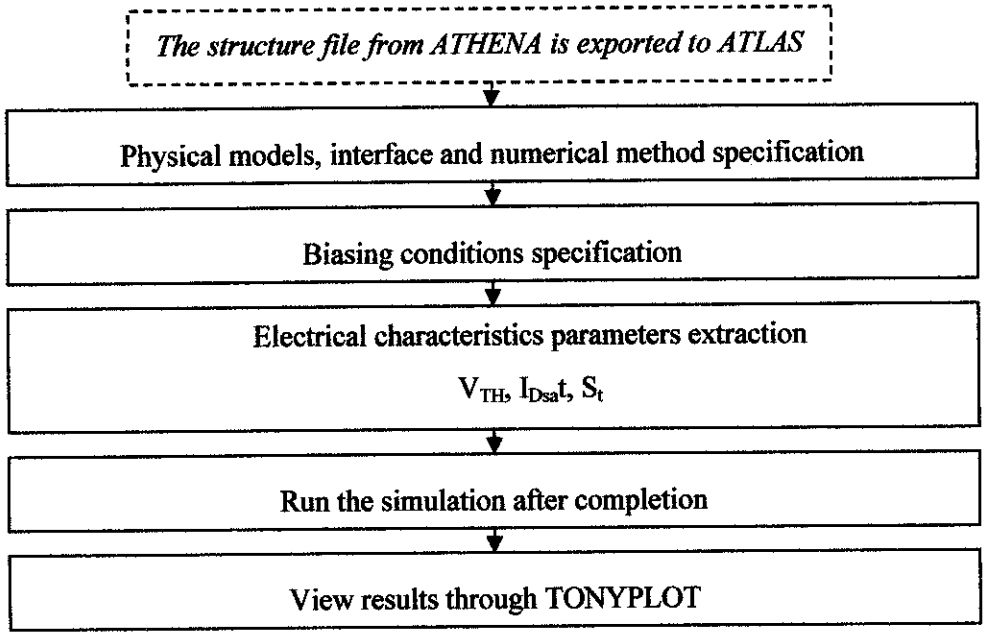

Figure 7 Process of running the ATLAS

The generated structure from the ATHENA simulation was then exported to ATLAS for both recipes. As stated in *Table 6*, physical models, interface properties and numerical method used were specified. The biasing conditions and extract statement should also be specified to acquire the desired parameters value.

In all simulations, the device started with zero bias on all electrodes. Then the voltage was specified on each of the electrodes in the device specified. ATLAS functioned to do calculation on current flow through each electrode. Solutions would be obtained by

stepping the biases on electrodes from initial equilibrium condition and then saved the results using log statement. This log statement had to be inserted in the program before sweeping the bias on gate electrode (to generate I_D-V_G graph) or on the drain electrode (to generate I_D-V_D graph). To extract the device parameters, the extract command provided with the deckbuild environment.

The summary of simulation process design for both recipes was illustrated in *Figure 8* and *Figure 9.*

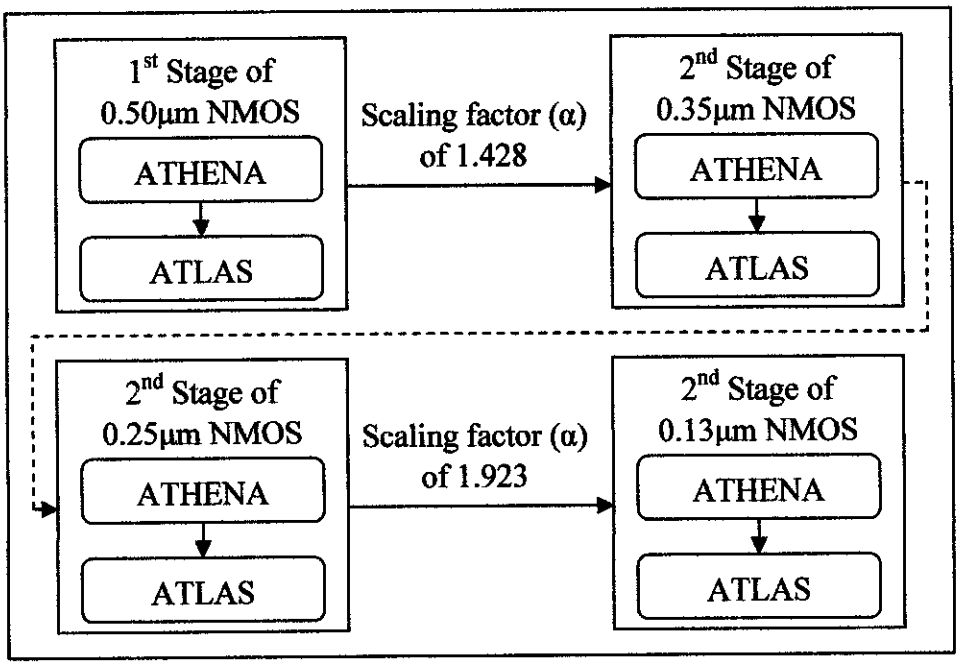

Figure 8 Summary of methodology for submicron technology 1

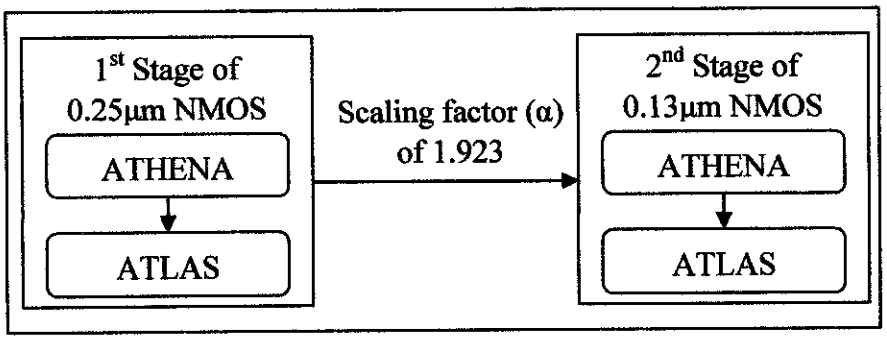

Figure 9 Summary of methodology for submicron technology 2

CHAPTER 4
RESULTS AND DISCUSSIONS

4.1 ATHENA Simulation

4.1.1 Submicron technology 1

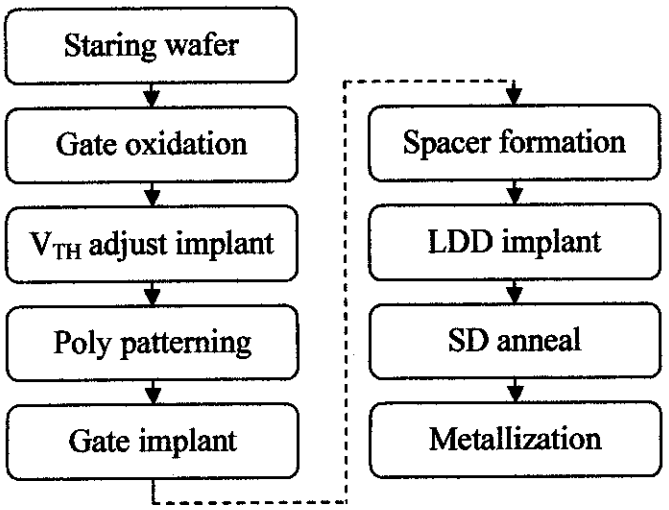

Figure 10 Simulation fabrication process for submicron technology 1

Initially, the silicon was deposited to form a starting wafer. Gate oxide layer is grown on silicon surface by performing dry oxidation. Next, doping impurities was introduced by ion implantation. Here, a V_{TH} adjust implant is utilized using Boron.

The conformal deposition for polysilicon gate was performed and later the geometrical of polysilicon gate was etched. Next, the polysilicon is doped with phosphorous to create an n+ polysilicon gate. Spacer oxide deposition has to be performed because of the

existence of source and drain implants. Next, a dry etch was performed to build the sidewall oxide spacer.

After sidewall spacer formation, an arsenic implantation will be performed to build n++ source/drain. Next, metallization process was performed. The backside electrode could be placed at the bottom of structure without having a metal region. The contact window was formed in source drain region and later the aluminium was deposited and patterned. [8] The summary of process utilized could be referred at *Table 7* and *Table 8.* Refer to APPENDIX A to know detail on internal view simulation process for submicron technology 1.

Table 7 Summary of parameters used in simulation of 0.25μm NMOS Sub Tech 1

Process	**Parameters**	
1. Starting wafer	• Wafer orientation <100> • Boron concentration 1.0×10^{14}	
2. Gate oxidation		*Dry O_2*
	diffuse time (min)	3.5
	temp (°C)	950
3. V_{TH} implant	• Boron • 33.5×10^{11} cm^{-2} • 5keV • Tilt = 7° & -7° • Rotation = 0°	
4. Polysilicon deposition	• Deposit poly thickness = 0.1μm	
5. Polysilicon oxidation		*Wet O_2*
	diffuse time (min)	1.5
	temp (°C)	900
6. Polysilicon implant	• Phosphorous • 3×10^{13} cm^{-2} • 10keV	
7. LDD implant	• Arsenic	

	• 5×10^{15} cm^{-2} • 25keV	
8. Spacer formation	• Deposit oxide thickness = 0.06μm	
9. SD anneal		*Nitrogen*
	diffuse time (minute)	1
	temp (°C)	900
10. Metallization	• Deposit aluminium thickness = 0.0125μm	

Table 8 Summary of parameters used in simulation of 0.13μm NMOS Sub Tech 1

PROCESS	***PARAMETERS***	
1. Starting wafer	• Wafer orientation <100> • Boron concentration 1.0×10^{14}	
2. Gate oxidation		*Dry O_2*
	diffuse time (min)	1.5
	temp (°C)	950
3. V_{TH} implant	• Boron • 40.5×10^{11} cm^{-2} • 5keV • Tilt = 7° & -7° • Rotation = 0°	
4. Polysilicon deposition	• Deposit poly thickness = 0.1μm	
5. Polysilicon oxidation		*Wet O_2*
	diffuse time (min)	1.5
	temp (°C)	900
6. Polysilicon implant	• Phosphorous • 3×10^{13} cm^{-2} • 10keV	
7. LDD implant	• Arsenic • 5×10^{5} cm-2 • 25keV	
8. Spacer formation	• Deposit oxide thickness = 0.06μm	
9. SD anneal		*Nitrogen*

	diffuse time (minute)	1
	temp (°C)	900
10. Metallization	• Deposit aluminium thickness = 0.0125μm	

4.1.2 Submicron technology 2

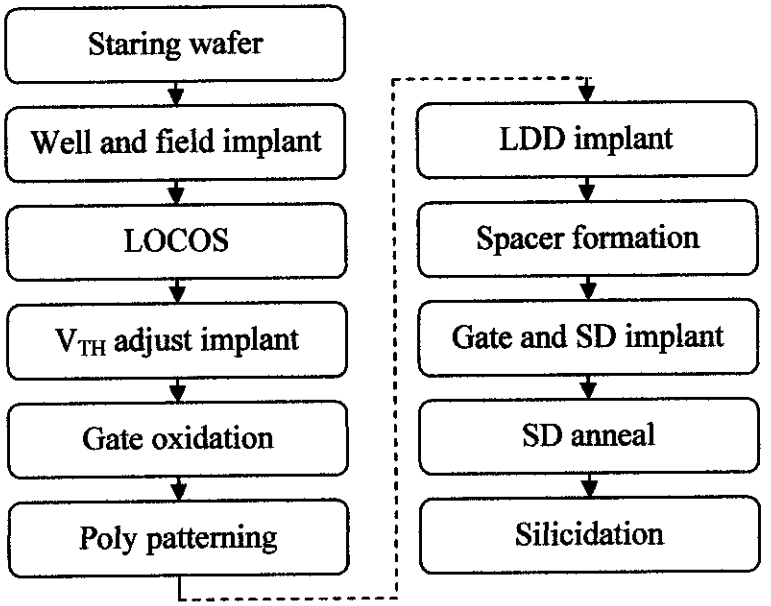

Figure 11 Simulation fabrication process for submicron technology 2

The simulation process began with starting wafer of p type. An n-well was then formed and followed by field implant. Ion implantation was used to form p-type doped isolation region before the field oxide thick growth. Next, LOCOS was formed where it was a technique of growing field oxide in selected regions. The V_{TH} implant adjustment was done with BF_2 to adjust the V_{TH} value. The gate oxidation was performed later and the undoped Polysilicon was deposited.

To form a shallow lightly doped source and drain regions, an arsenic implantation was performed. This process was known as lightly doped drain (LDD). It improved reliability

against hot carrier instability of a transistor by avoiding electric field concentration. The concept was the insertion of grade profiled, n- drain region between n+ part o the drain and channel region. The n- region sustained the drain voltage over a longer region, thus reduced the peak electric field which mainly lateral at the drain. (Tasch et al., 1990)

Prior to LDD implant, the conformal silicon oxide deposition was performed on the silicon surface and followed by anisotropic etching to create sidewall spacer. It etched only in downward vertical direction and not along the silicon surface. Along the Polysilicon sides, the vertical thickness of the oxide layer would be much thicker than on top of Polysilicon. The entire deposited insulator is then removed except for a wedge along the sides of the Polysilicon lines. The sidewall spacers provided diffusion buffer for the dopant in source and drain junction.

Next, by using phosphorous the deep source and drain in regions adjacent to the sidewall was formed. At the same time, the source drain contacts were doped as well as Polysilicon gates by ion implantation. A dual doped poly scheme was utilized meanwhile the poly gate was doped with n+ dopants.

This was later followed by RTA process to repair the damage to the lattice by restoring the single-crystal structure and activating the dopant. RTA was utilized instead of conventional furnace diffusion to minimize dopant diffusion and also produced ultra shallow junctions. The silicidation process was performed later. Silicidation referred as process of forming a surface layer of refractory metal silicide on silicon. Titanium was deposited on silicon and a layer of silicide was formed when the two substances reacted at elevated temperatures. The resistivity of titanium silicide was the lowest among various metal silicides with 12-25 μΩ–cm (Kim et al., 1998). After silicidation, the phosphor silicate glass (PSG) was deposited and subjected to reflow process for smoothness. After that, contact holes were opened by etching. [4] The summary of

process utilized could be referred at *Table 9* and *Table 10.* Please refer to APPENDIX A to know more on internal view simulation process for submicron technology 2 in detail.

Table 9 Summary of parameters used in simulation of 0.25μm NMOS Sub Tech 2

Process	**Parameters**		
1. Starting wafer	• Wafer orientation <100> • Boron concentration = 3.0×10^{14}		
2. Well implant	• Boron • 5×10^{12} cm^{-2} • 60 keV		
3. Field implant	• Boron • 2×10^{13} cm^{-2} • 80 keV		
4. LOCOS		*Wet O_2*	*Nitrogen*
	Diffuse time (min)	120	20
	temp (°C)	1000	1000
5. V_{TH} implant	• BF_2 • 5.6×10^{12} cm^{-2} • 50 keV		
6. Gate oxidation		*Dry O_2*	*Nitrogen*
	diffuse time (min)	25	30
	temp (°C)	850	1000
7. Polysilicon deposition	• Deposit poly thickness = 0.25μm		
8. LDD implant	• Arsenic • 5×10^{13} cm^{-2} • 30 keV • Tilt = 7° & -7° • Rotation = 0°		
9. Spacer formation	• Deposit oxide thickness = 0.3μm		
10. Gate and SD implant	• Phosphorous • 3×10^{15} cm^{-2} • 40 keV		
11. SD anneal		*Nitrogen*	*Nitrogen*
	diffuse time (sec)	10	5
	temp (°C)	900	1050

12. Silicidation	• Deposit titanium thickness = 0.03μm
13. PSG deposition	• Deposit oxide thickness = 0.7μm

Table 10 Summary of parameters used in simulation of 0.13μm NMOS Sub Tech 2

Process	Parameters		
1. Starting wafer	• Wafer orientation <100> • Boron concentration = 3.0×10^{14}		
2. Well implant	• Boron • 5×10^{12} cm^{-2} • 60 keV		
3. Field implant	• Boron • 2×10^{13} cm^{-2} • 80 keV		
4. LOCOS		*Wet O_2*	*Nitrogen*
	diffuse time (min)	120	20
	temp (°C)	1000	1000
5. V_{TH} implant	• BF_2 • 5.4×10^{12} cm^{-2} • 50 keV		
6. Gate oxidation		*Dry O_2*	*Nitrogen*
	diffuse time (min)	23	30
	temp (°C)	800	1000
7. Polysilicon deposition	• Deposit poly thickness = 0.25μm		
8. LDD implant	• Arsenic • 5×10^{13} cm^{-2} • 30 keV • Tilt = 7° & -7° • Rotation = 0°		
9. Spacer formation	• Deposit oxide thickness = 0.3μm		
10. Gate and SD implant	• Phosphorous • 3×10^{15} cm^{-2} • 40 keV		
11. SD anneal		*Nitrogen*	*Nitrogen*
	diffuse time (sec)	10	5
	temp (°C)	900	1050

12. Silicidation	• Deposit titanium thickness = 0.03μm
13. PSG deposition	• Deposit oxide thickness = 0.7μm

4.1.3 The submicron technology involved

4.1.3.1 Local oxidized silicon (LOCOS)

It is an isolator between two transistors. The goal is to oxidize silicon only wherever a field of oxide is needed. This can be done by using silicon nitride (Si_3N_4) to protect the silicon areas that are not to be oxidized. However, selection of Si_3N_4 poses it owns problems. In high tensile stress, it can induce large edge forces on the substrate when pattern. Thus, a thin thermal oxide (pad oxide) is initially grown; follow by deposition of Si_3N_4 and the photoresist. The resist is then patterned and the nitride is etched to protect the active areas. A thick field oxide is then grown on areas which are not covered by the silicon nitride mask. After thermal oxidation, the silicon nitride is then etched off for the next processing steps. [4]

4.1.3.2 Spacer

Spacers are used alongside the poly gates to prevent the higher source/drain implant from penetrating too close to the channel where leakage current punch through could occur. It is formed with multiple control gates by forming side wall control gates adjacent to the gate oxide spacers over heavily-doped regions of the source and drain regions. The side wall control gates can be used to substantially increase the threshold voltage of the transistor. [9]

4.1.3.3 Lightly doped drain (LDD)

Lightly doped drain is implemented. Channel length reduction leads to increases the potential for charges to punch through the transistor source and drain and cause undesirable channel leakage current. This probability can be reduced by reducing the doping concentration of the drain. This will lead to lower number of carrier charge

available at the drain and it will take longer time and bigger potential needed before avalanche take place. [9]

4.1.3.4 Salicide

In the past, polysilicon films doped with phosphorus have often been used as electrodes and interconnections. However, the resistance of gate electrode or the interconnection comprising the polysilicon film doped with phosphorus provides limitation for improvement in a high speed performance of the MOSFET. As feature size is reduced, resistance is increased and that require changes in contact formation.

To solve this problem and permit further improvement in a high speed performance of the MOS field effect transistor, the polysilicon film doped with phosphorus is placed with a polycide structure comprising a polysilicon and a high melting point metal silicide. Particularly, a titanium silicide film has a smaller resistivity in various high melting point metal silicide films. A titanium silicide film serving as the gate electrode is suitable in a self-alignment process for reductions of resistances of source and drain diffusion regions in the MOS field effect transistor. For the above reasons, the titanium silicide film is attractive as an electrode and an interconnection. [4]

4.1.3.5 Rapid thermal annealing (RTA)

It replaced long time furnace annealing especially to minimize the dopant diffusion and produce shallow junctions. [2]

Table 11 Comparison of submicron technology utilized for both recipes

	Submicron technology 1	**Submicron technology 2**
1. LOCOS	-	√
2. Gate oxidation		
• Dry O_2	√	√
• Nitrogen	-	√

3. V_{TH} adjust implant		
• Boron	√	-
• BF_2	-	√
4. Metallization	√	-
5. Silicidation	-	√

4.1.4 Alteration effects for parameters selected

Table 12 showed the standard parameters for different generation from BPTM and ITRS. The simulation value obtained for both submicron technologies recipes would be compared.

Table 12 Summary of MOSFET parameters as standard requirement

Node Technology	**Gate Length, L_G (μm)**	**Oxide Thickness, t_{OX} (nm)**	**V_{TH} (V)**	**V_{DD} (V)**
CMOS model				
0.6μm	0.6	11.0	1.000	5.0
0.35μm	0.35	7.6	0.735	3.3
0.25μm	0.25	4.0	0.596	2.5
0.18μm	0.18	2.5	0.466	1.8
ITRS requirement for NMOS				
0.13μm	0.13±15% (0.12-0.15)	3.3±4% (3.17-3.43)	0.33±12.7% (0.29-0.37)	1.5±10% (1.35-1.65)

Source: California University, 2002

4.1.4.1 Submicron technology 1

4.1.4.1.1 The effect of gate oxide thickness

Changed in time diffusion would result in change of gate oxidation thickness. The time diffusion was altered to obtain the oxide thickness at approximately at range of 3.17nm to 3.43nm.

Table 13 The trial and error for gate oxidation in nanometer

Diffuse time (min)	**Temperature (°C)**	**Gate oxide thickness, t_{ox} (nm)**
11.00	950	10.00
5.50	950	6.50
2.50	950	4.30
2.00	950	3.75
1.50	950	3.40
1.00	950	2.85
0.75	950	2.75

GA*TE OXIDATION*
diffus time=1.5 temp 950 dryo2 press=1.00 hcl.pc=3

4.1.4.1.2 Threshold voltage variation with Boron concentration

Trial and error approach were used to obtain the required V_{TH}, 0.33V±12.7% or 0.29V<V_{TH}<0.37V. Just the doping below the gate has a significant influence on the final device behaviour. The effect of this implantation is to adjust the V_{TH} of the transistor. The V_{TH} is defined as the gate voltage above which the transistor becomes conductive due to an inversion of a thin layer below the gate. The voltage which is necessary to create an inversion layer strongly depends on the original doping concentration, which is adjusted by this implantation. V_{TH} adjust implantations are

always performed with low doses, because just slight modification of the gate concentration are sufficient for the adjustment.

Table 14 The trial and error to obtain the desired threshold voltage

Boron		Threshold voltage, V_{TH}
Dose	**Energy**	
10.5×10^{11}	10	0.06
20.5×10^{11}	10	0.19
30.5×10^{11}	10	0.33
40.5×10^{11}	10	0.37

From observation, the higher the boron dose concentration, the higher the threshold voltage value. Finally the required V_{TH} with the acceptable doping concentration was obtained where

 # THRESHOLD VOLTAGE ADJUST IMPLANT
implant boron dose=40.5e11 energy=5 rotation=30 crystal lat.ratio1=1.0 lat.ratio2=1.0

4.1.4.1.3 Gate length

Channel length can be decreased by *etch poly left p1.x=0.*35 for 0.13μm. If the etch was done farther, the gate became shorter.

4.1.4.2 Submicron technology 2

4.1.4.2.1 The effect of gate oxide thickness

The t_{ox} thickness can be changed by changing the parameter in the diffusion process. At first trial, only the time parameter was changed. By changing the time parameter into longer time, the thickness of the t_{ox} could be increased and vice versa. By increasing the thickness of the t_{ox}, it also increased the minimum V_G to get I_D bigger than zero.

Based on trial and error method, the diffuse time was varied bit by bit and the temperature value was maintained. Here, the compress model was used to model 2D oxidation in non planar structure. The stress effect played a minor role in determining oxide shape. The coding was as stated as below and the result of t_{ox} thickness was observed.

 # OXIDIZE THE GATE (32A~34A)
method grid.oxide=0.004
diffus time=23 temp=800 dryo2
diffus time=30 temp=1000 nitro

Table 15 First attempt

Diffuse time (min)	Temperature (°C)	Gate oxide thickness, t_{ox} (Å)
48	850	88.55
40	850	78.91
30	850	66.19
20	850	52.31
10	850	41.54

The higher the temperature, the thicker the t_{ox} thickness. At 850°C, the t_{ox} reduced from 88.5Å to 52.3Å when varied the temperature from 48°C to 20°C. However, the obtained t_{ox} was far from ITRS requirement, 31.68Å -34.32Å.

Table 16 Second attempt

Diffuse time (min)	Temperature (°C)	Gate oxide thickness, t_{ox} (Å)
48	800	59.34
30	800	37.57
25	800	34.79
23	***800***	***33.66***

The lower the temperature, the size of t_{ox} thickness would be smaller. Thus the second attempt was to reduce the temperature from 850°C to 800°C. When diffuse for 48 minutes, the t_{ox} was lesser immediately at lower temperature than at higher temperature. Observation showed at 800°C, the t_{ox} reduced from 59.3Å to 33.7Å when varied the temperature from 48°C to 20°. Hence, the obtained t_{ox} reached the targeted International Technology Roadmap Semiconductor (ITRS) requirement, 31.68Å -34.32Å.

Thus the gate oxidation was performed by growing the t_{ox} layer on the silicon surface. At first the dry oxidation was performed at 800°C for 23 minutes and latter by nitrogen at 1000°C for 30 minutes.

4.1.4.2.2 Threshold voltage variation with boron diflourine concentration

Another parameter affecting the V_{TH} was the doping concentration of boron (BF_2) in the device.

The theoretical equation (1) for the V_{TH} of an ideal NMOS device is given by

$$V_T = \Phi_M - \chi - \frac{E_O}{2q} + |\Phi_F| + \frac{\left|\sqrt{(2K_S\varepsilon_O qN_B(2|\Phi_F| + V_{BS}))}\right|}{C_O} - \frac{Q\omega}{C_O} \qquad (1)$$

$$\text{Where } |\Phi_F| = \left(\frac{kT}{q}\right)\ln\left(\frac{N_B}{n_i}\right) \qquad (2)$$

The V_{TH} was defined as the gate voltage above which the transistor becomes conductive due to an inversion of a thin layer below the gate. The voltage which was necessary to create an inversion layer strongly depends on the original doping concentration, which was adjusted by this implantation. V_{TH} adjust implantations are always performed with low doses, because just slight modification of the gate concentration were sufficient for the adjustment.

An increased doping concentration in the structure indicated that there were more majority carriers under the oxide silicon interface in the gate region. As such, a higher concentration of minority carriers was needed to generate inversion and depletion layers.

The V_{TH} of operation of the device was determined from the plot of the drain source current voltage versus the gate voltage. The value was determined by extrapolation of the curve from the point of maximum slope to the x-axis intercept.

Based on trial and error method, the dose implantation was varied bit by bit but the energy value was maintained. Simulations were performed, keeping all other quantities constant and changing the threshold voltage. Here ion implantation models used could be either analytical or Monte Carlo.

By default the analytic models were used. It was based on reconstruction of implant profiles from the calculated or measured distribution moments. The Monte Carlo (statistical technique) used the physically based Monte Carlo of ion trajectories in order to calculate the final distribution of stopped particles.

Analytic implant models were made up of *gaussian, pearson* and *dual pearson* models. Gaussian model was performed for 1D profiles and inadequate due to real profiles were asymmetrical in most cases. The pearson model was the simplest and most widely approved method for calculation of asymmetrical ion implantation profiles. Dual pearson was for heavily affected profiles by channeling.

Monte Carlo was used to simulate ion implantation in non standard conditions. This approach allowed calculation of implantation profiles in any random structure with accuracy comparable to the accuracy of analytical models.

4.1.4.2.2.1 Monte Carlo (statistical)

The first attempted coding was as stated as below and the result of V_{TH} was observed for Monte Carlo (bca).

 # NVT IMPLANT BORON TO SHIFT THE THRESHOLD
implant bf2 dose=1.0769e13 energy=50 tilt=0 rotation=0 bca

Table 17 First attempt

BF_2		**Gate oxide thickness, t_{ox} (Å)**	**Threshold voltage, V_{TH} (V)**	**Saturation current, I_{Dsat} (µA/µm)**	**Subthreshold current, St (mA/µm)**
Dose (cm^{-2})	**Energy (keV)**				
1.80×10^{13}	50	33.68	-1.08	897.01	3.01
1.28×10^{13}	50	33.64	-1.48	964.23	3.37
1.18×10^{13}	50	33.64	-1.69	996.66	3.97
1.08×10^{13}	50	56.52	-1.73	1172.72	4.03
1.06×10^{13}	50	33.63	-1.78	1184.50	4.08
1.02×10^{13}	50	33.63	-2.50	1193.33	4.01
8.62×10^{12}	50	33.62	-2.71	1239.11	6.34
8.08×10^{12}	50	33.62	-3.39	1318.70	7.92
5.38×10^{12}	50	33.61	-4.94	1520.01	11.39
2.69×10^{12}	50	33.60	-5.02	1597.46	11.57

The value of V_{TH} obtained was negative. This may due to unsuitable technique since Monte Carlo should be used for non standard conditions. For example, for cases that had not been studied experimentally yet. Thus, this technique was not valid for this case.

4.1.4.2.2.2 Dual pearson (analytical)

The second attempted coding was as stated as below and the result of V_{TH} was observed for dual pearson (pears).

 # NVT IMPLANT BORON TO SHIFT THE THRESHOLD
implant bf2 dose=1.0769e13 energy=50 tilt=0 rotation=0 pears unit.damage dam.factor=0.01

The effect of implant damage enhanced diffusion was important. As damage generated by implantation, it led to diffusion enhancement of the dopants during subsequent heat cycles. First, ATHENA must simulate the implant damage generated by a given implant. Secondly, it must model the effect that these defects had on subsequent impurity diffusion.

The most practical model for coupling the implant damage to subsequent diffusion calculation was the +1 model. In ATHENA, this could be done by using parameter dam.fact on implant statement

Table 18 Second attempt

BF_2		Gate oxide thickness, t_{ox} (Å)	Threshold voltage, V_{TH} (V)	Saturation current, I_{Dsat} (µA/µm)	Subthreshold current, St (mA/µm)
Dose (cm^{-2})	Energy (keV)				
3.80×10^{13}	50	33.990	1.211	12.39	93.41
2.80×10^{13}	50	33.833	1.063	30.39	81.40
1.46×10^{13}	50	33.686	0.809	90.25	66.05
1.15×10^{13}	50	33.661	0.739	117.98	63.17
1.08×10^{13}	50	33.659	0.726	139.10	62.83
1.00×10^{13}	50	33.648	0.648	153.14	61.80
8.62×10^{12}	50	33.637	0.460	267.55	60.96
6.46×10^{12}	50	33.618	0.390	297.23	76.03
5.38×10^{12}	50	33.604	0.318	343.11	78.18

Increasing the substrate doping causes an increase in the V_{TH} of the device. The V_{TH} value obtained was positive. Reduction of implant dose, BF_2 resulted lower in V_{TH}.

4.1.4.2.3 Gate length

To decrease the channel length, gate patterning was defined by etched poly at left of x-axis. If the etch was done farther, the gate would be shorter.

 # ETCH POLYSILICON
etch poly left p1.x=-0.091

4.2 ATLAS Simulation

There were several device parameters being extracted. The results obtained were consists of threshold voltage (V_{TH}), saturation current (I_{Dsat}) and subthreshold swing (St). The measured parameters obtained were then compared with the requirement.

4.2.1 Results for 0.25μm NMOS simulations

4.2.1.1 Submicron technology 1

4.2.1.1.1 Result on saturation current extraction

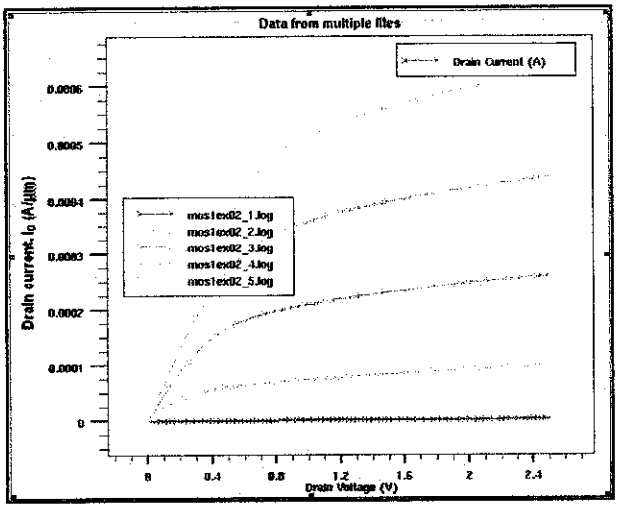

Figure 12 Drain current, I_D versus drain voltage, V_D of 0.25μm NMOS

Saturation current, I_{Dsat} referred to how much current was carried in the ON state. Here, five I_D-V_D curves were required at different gate voltage. The gate voltage chose ranging from 0.5V, 1.0V, 1.5V, 2.0V and 2.5V. The I_{Dsat} obtained was 571.69μA/m. The ideal curve should be almost flat but in submicron device, slope curve was unavoidable. Thus, as much as possible, the slope should be less steep. If not the device would get easily heat up due to the excessive doping. From result and observing at I_D-V_D curve, the slope changes was not drastic and became less steep even though boron doping was increased.

I_D gradually increased when V_D increased. This showed the device experienced channel length modulation. This led to an increase of I_D which occurred in low doping and when critical punch through occurred. The graph itself showed this phenomenon due to I_D rose sharply as V_D further increased and exhibited no true saturation.

4.2.1.1.2 Result on threshold voltage extraction

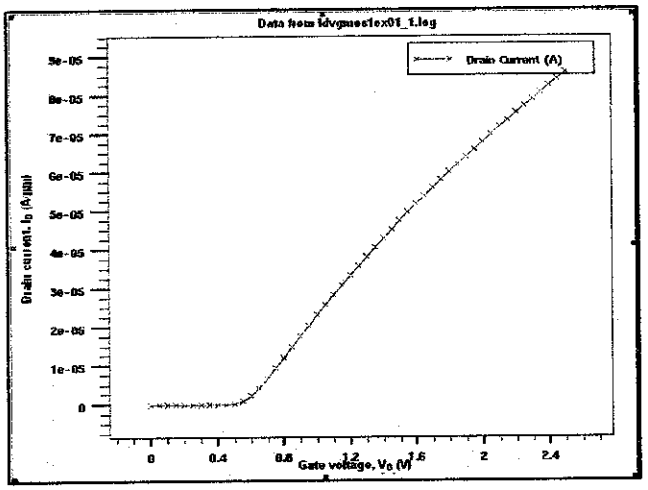

Figure 13 Drain current, I_D versus gate voltage, V_G of 0.25μm NMOS

Linear extrapolation method was used to extract V_{TH} from the simulation. From I_D-V_G curve, the V_{TH} value could then be extracted. The V_{TH} value obtained was 0.51V. Increasing Boron doping will lead to increment of V_{TH}.

4.2.1.1.3 Result on subthreshold swing extraction

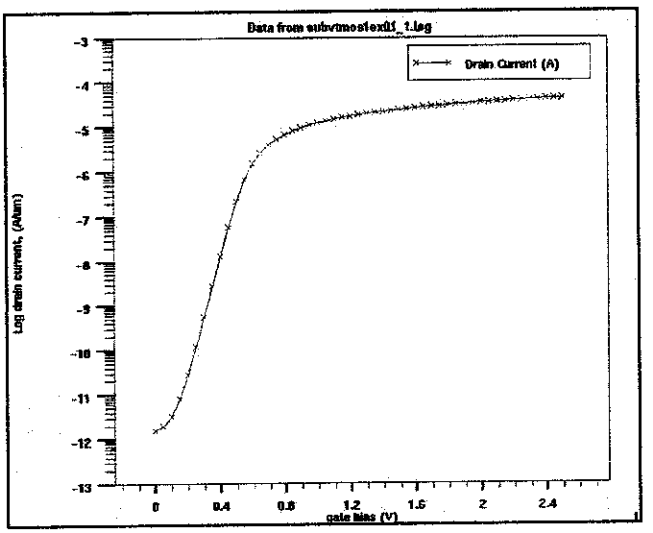

Figure 14 Subthreshold of 0.25μm NMOS

Subthreshold swing, S_t was a measurement of how much of change in V_G was required to change the off-current in the device. It was desirable to have small S_t (the slope below V_{TH} is steep). This was because only small reduction of V_G below V_{TH} could effectively turn-off the device. Large S_t implied significant I_D may still flow in the OFF state where V_G=0V. The S_t obtained was at 74.05mV/dec. *Table 19* below showed summarization of the extracted parameter for 0.25μm NMOS.

Table 19 Summary of extract parameters of 0.25μm NMOS

T_{ox} (Å)	nxj (μm)	V_{TH} (V)	I_{Dsat} (μA/μm)	S_t (mV/dec)
57.84	0.36	0.51	571.69	74.05

4.2.1.2 Submicron technology 2

4.2.1.2.1 Result on saturation current extraction

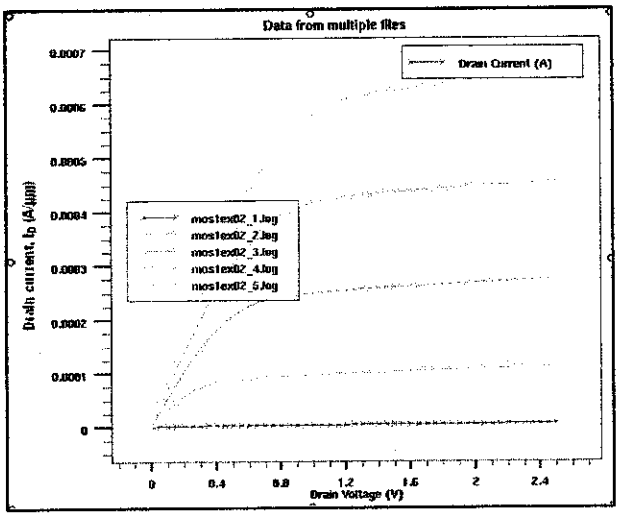

Figure 15 Drain current, I_D versus gate voltage, V_G of 0.25μm NMOS

The gate voltage chose ranging from 0.5V, 1.0V, 1.5V, 2.0V and 2.5V. The I_{Dsat} obtained was 295.72μA/m. The curve showed true saturation which was almost flat. Hence, punch through phenomenon did not occur.

4.2.1.2.2 Result on threshold voltage extraction

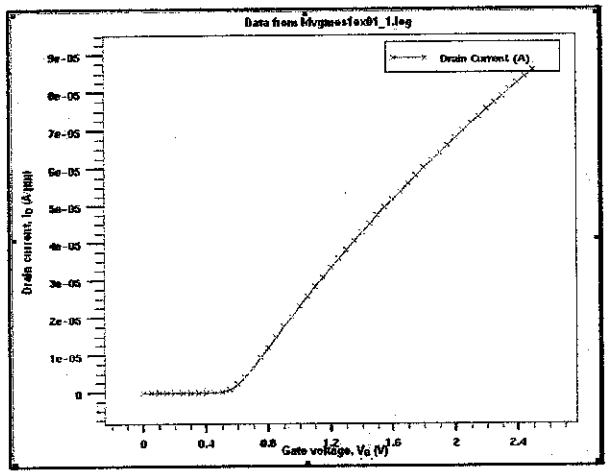

Figure 16 Drain current, I_D versus gate voltage, V_G of 0.25μm NMOS

For extraction of V_{TH}, the I_D-V_G curve was plotted and the sequence of the solve statements were set to ramp the gate bias with drain voltage of 0.05V. The threshold voltage obtained was 0.50V.

4.2.1.2.3 Result on subthreshold swing extraction

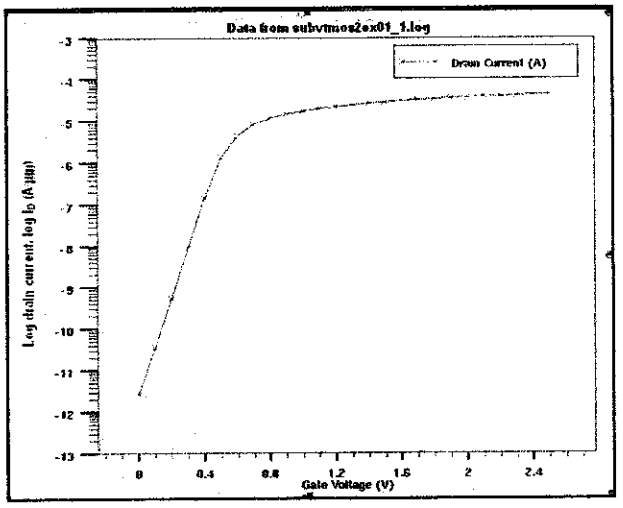

Figure 17 Subthreshold of 0.25µm NMOS

The subthreshold swing value was 81.39mV/dec. The value obtained was larger than the submicron technology 1 by 7.6% which indicated the design had poor turn-off characteristics. *Table 20* was summarization of the extracted parameter for 0.25µm NMOS.

Table 20 Summary of extract parameters of 0.25µm NMOS

T_{ox} (Å)	nxj (µm)	V_{TH} (V)	I_{Dsat} (µA/µm)	S_t (mV/dec)
59.37	0.32	0.50	295.72	81.39

Both extracted parameters for using submicron technology 1 and submicron technology 2 approaches were tabulated for ease in reference.

Table 21 Summary of extracted parameters of 0.25μm NMOS for both approaches

Parameters	T_{ox} (Å)	nxj (μm)	V_{TH} (V)	I_{Dsat} (μA/μm)	S_t (mV/dec)
Submicron technology 1	57.84	0.36	0.51	295.72	74.05
Submicron technology 2	59.37	0.32	0.50	571.69	81.39

The simulation value obtained was then compared with the design reported as tabulated in *Table 22*. Both V_{TH} simulation values obtained were found to be closer with Horvath et al. (2005) with a difference of 2% - 3% only. However, the differences found to higher when compared with Mat Husin et al. (2000). The differences were 23% for submicron technology 1 and 25% for submicron technology 2.

For I_{Dsat}, only 5% and 4% differences were found for submicron technology 1 between Mat Husin et al. (2000) and ITRS (1997) respectively. However, large differences were noted for submicron technology 2 between Mat Husin et al. (2000) and ITRS (1997). The values were 51% and 46% respectively.

For S_t, the value reported was closer when compared submicron technology 1 with Mat Husin et al. (2000) with 7% difference. However, when compared with Horvath et al. (2005) the difference was quite large with 18%. Submicron technology 2 showed much better result. The differences were only 2% and 10% when compared with Horvath et al. (2005) and Mat Husin et al. (2000) respectively.

The recorded parameters displayed that both submicron technology has its own tradeoffs. Each design had both advantages and drawbacks. In this work, introducing one submicron technology such as LOCOS may enhance the I_{Dsat}, however at the same time the S_t value may be increased which was not desired.

Table 22 Comparison of parameters obtained with other design reported

Node Tech.	0.25µm					
Data source	Mat Husin et al., 2000	Horvath et al., 2005	Silvaco Resource Centre	ITRS, 1997	Simulation	
					Sub Tech. 1	Sub Tech. 2
V_{TH} (V)	0.55	0.67	-	-	0.51	0.50
I_{Dsat} (µA/µm)	550	-	-	600	295.72	571.69
S_t (mV/dec)	< 90	80	-	-	74.05	81.39

4.2.2 Results for 0.13µm NMOS simulations

4.2.2.1 Submicron technology 1

4.2.2.1.1 Result on saturation current extraction

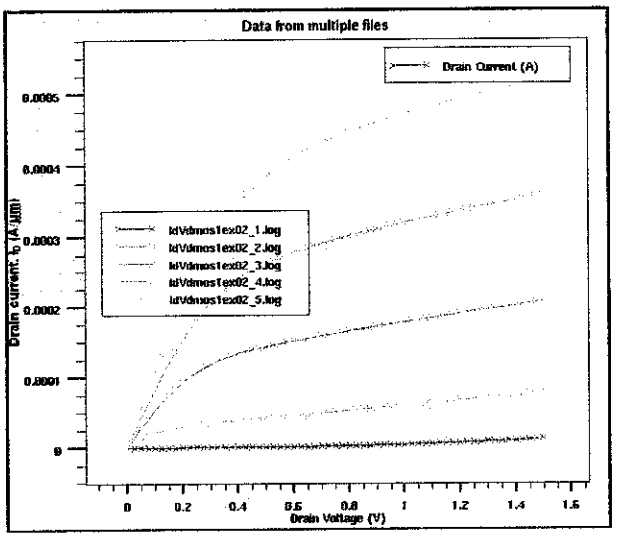

Figure 18 Drain current, I_D versus drain voltage, V_D of 0.13µm NMOS

Saturation current, I_{Dsat} was referred to how much current was carried in the ON state. Here, four I_D-V_D curves were required at different gate voltage. The gate voltage chose ranging from 0.3V, 0.6V, 0.9V, 1.2V and 1.5V. The I_{Dsat} obtained is 519.33μA/m. The ideal curve should be almost flat but in submicron device, slope curve was unavoidable. Thus, as much as possible, the slope should be less steep. If not the device would get easily heat up and this was due to the excessive doping.

From observation, I_D gradually increased when V_D increased. This showed the device experienced channel length modulation. This led to an increase of I_D which occurred in low doping and when critical, punch through occur. The graph itself showed this phenomenon due to I_D rose sharply as V_D further increased and exhibited no true saturation.

4.2.2.1.2 Result on threshold voltage extraction

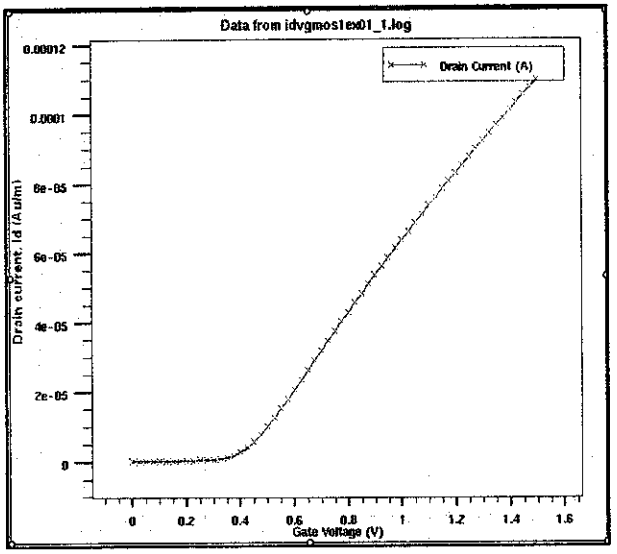

Figure 19 Drain current, I_D versus gate voltage, V_G of 0.13μm NMOS

From I_D-V_G curve, the V_{TH} could then be extracted. The V_{TH} value obtained was 0.37V. Increasing Boron doping will lead to increment of V_{TH}.

4.2.2.1.3 Result on subthreshold swing extraction

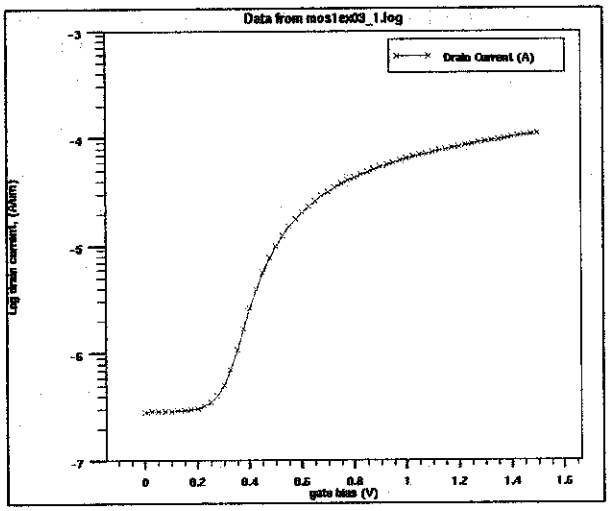

Figure 20 Subthreshold of 0.13μm NMOS

Subthreshold swing, S_t was a measurement of how much of change in V_G was required to change the off-current in the device. It was desirable to have small S_t (the slope below V_{TH} is steep). This was because only small reduction of V_G below V_{TH} could effectively turn-off the device. Large S_t implied significant I_D may still flow in the OFF state where V_G =0V. The S_t obtained was at 127.59mV/dec. *Table 22* below was summarization of the extracted parameter for 0.13μm NMOS.

Table 23 Summary of extract parameters of 0.13μm NMOS

t_{ox} (Å)	nxj (μm)	V_{TH} (V)	I_{Dsat} (μA/μm)	S_t (mV/dec)
33.61	-	0.37	519.33	127.59

4.2.2.2 Submicron technology 2

4.2.2.2.1 Result on saturation current extraction

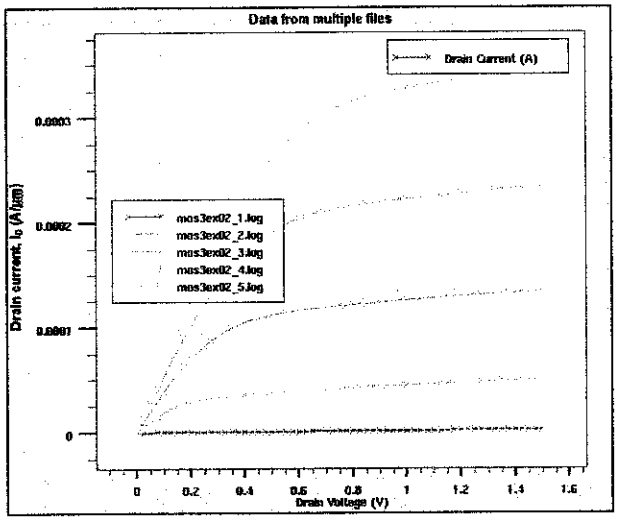

Figure 21 Drain current, I_D versus drain voltage, V_D of 0.13µm NMOS

The gate voltage chose ranging from 0.3V, 0.6V, 0.9V, 1.2V and 1.5V. The I_{Dsat} obtained was 343.11µA/m. The curve showed true saturation which was almost flat. Hence, punch through phenomenon did not occur.

4.2.2.2.2 Result on threshold voltage extraction

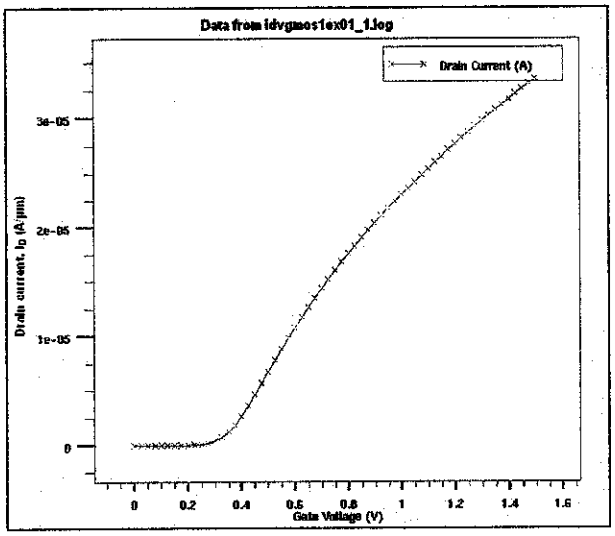

Figure 22 Drain current, I_D versus gate voltage, V_G of 0.13µm NMOS

For extraction of V_{TH}, the I_D-V_G curve was obtained plotted and the sequence of the solve statements are then set to ramp the gate bias with the drain voltage of 0.05V. The threshold voltage obtained was 0.31V.

4.2.2.2.3 Result on subthreshold swing extraction

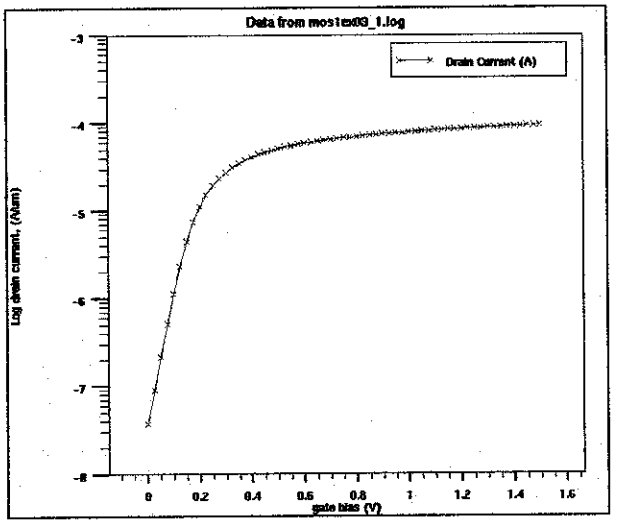

Figure 23 Subthreshold of 0.13μm NMOS

The subthreshold swing value was 64.785mV/dec. The value obtained was larger than the conventional approach by 7.6% which indicated the design had poor turn-off characteristics. *Table 23* below is summarization of the extracted parameter for 0.13μm NMOS.

Table 24 Summary of extract parameters of 0.13μm NMOS

t_{ox} (Å)	nxj (μm)	V_{TH} (V)	I_{Dsat} (μA/μm)	S_t (mV/dec)
33.60	0.41	0.31	343.11	64.79

Both extracted parameters submicron technology approaches were tabulated in *Table 24* for ease in reference.

Table 25 Summary of extracted parameters of 0.13μm NMOS for both approaches

Parameters	t_{ox} (Å)	nxj (μm)	V_{TH} (V)	I_{Dsat} (μA/μm)	S_t (mV/dec)
Submicron technology 1	33.61	-	0.37	519.33	127.59
Submicron technology 2	33.60	0.41	0.31	343.11	64.79

Table 26 Comparison of parameters obtained with other design reported

Node Tech.	**0.13μm**					
					Simulation	
Data source	**TI**	**Intel**	**TSMC**	**ITRS**	**Sub Tech. 1**	**Sub Tech. 2**
V_{DD} (V)	1.20	1.40	1.20	1.35-1.65	1.50	1.50
t_{ox} (nm)	2.40	2.15	2.35	3.17-3.43	3.36	3.36
V_{TH} (V)	0.30	0.33	0.26	0.29-0.37	0.37	0.31
I_{Dsat} (μA/μm)	1000	1125	935	-	343	519
S_t (mV/dec)	-	-	-	-	65	127

The simulation value obtained was then compared with the design reported as tabulated in *Table 26*. Both V_{DD} simulation values obtained were found to be closer with ITRS and Intel with a difference of 7% - 11% only. However, the differences found to higher when compared with TSMC and TI. The differences were 25% for both submicron technologies.

t_{ox} simulation values were found to be closer with ITRS for both submicron technologies with differences range of 2% - 6%. However, the differences found to higher when compared with TI, Intel and TSMC. The differences were 40%, 56% and 43% for both submicron technologies respectively.

Both simulation V_{TH} values were found to be in range with ITRS requirement. However, the differences found to higher when submicron technology 1 was compared with TI, Intel and TSMC. The differences were 23%, 12% and 42% respectively. For submicron technology 2, the V_{TH} values were much more comparable with differences of 3%, 6% and 19% when compared with TI, Intel and TSMC.

For I_{Dsat}, both simulation values were not comparable with the cited work. The differences for submicron technology 1 with TI, Intel and TSMC were 66%, 67% and 63% respectively while for submicron technology 2 the differences were 48%, 54% and 55% respectively.

St value however could not be compared. This information was classified by the industry and treated as confidential.

The recorded parameters displayed that both submicron technology had its own tradeoffs. Each design had both advantages and drawbacks. For submicron technology 1, parameters for t_{ox} thickness and V_{TH} were acceptable and within the range of ITRS requirement. It had lower S_t which was desirable since lower S_t implied that the design has good turn-off characteristics. However, the I_{Dsat} obtained was too small compared with other cited work and even with the second simulated recipe. Too small saturation current mean the device operated at lower speed. Other than that, the drastic increase observed at I_D-V_D curve showed that the device experienced the punch through phenomenon.

For submicron technology 2, parameters for t_{ox} thickness and V_{TH} were also acceptable and within the range of ITRS requirement. However, this time subthreshold current, S_t was much higher than the first recipe. This is undesirable since higher S_t implied that the design has poor turn-off characteristics. Yet, the I_{Dsat} obtained this time was higher than the first simulated recipe but lower than other cited work. Higher I_{Dsat} was desirable since it was illustrated that the device operated at faster speed.

CHAPTER 5
CONCLUSION

5.1 Conclusion

For 0.25μm NMOS, both results displayed the threshold voltage (V_{TH}) value obtained were 0.54V and 0.50V respectively. The saturation current (I_{Dsat}) value obtained was 572μA/μm for the first submicron technology while 296μA/μm for the second submicron technology. For subthreshold current (S_t), the recorded values were 74mV/dec and 81mV/dec respectively.

For 0.13μm NMOS, both results displayed gate oxide thickness (t_{ox}) of 3.36nm while the threshold voltage (V_{TH}) value obtained were 0.31V and 0.37V respectively. These parameters were within the with International Technology Roadmap Semiconductor (ITRS) requirement. The saturation current (I_{Dsat}) value obtained was 343μA/μm for the first submicron technology while 519μA/μm for the second submicron technology. In this case, the second recipes had better performance since higher I_{Dsat} implied the device operated at higher speed. However if compared with other cited work, the I_{Dsat} second submicron technology was almost half than the reported value. For subthreshold current (S_t), the recorded values were 65mV/dec and 128mV/dec respectively. For this condition, the first recipe was far better than the second recipe since lower S_t displayed the device has good turn-off characteristics. This is due the LOCOS is introduce which provide electrical isolation.

Overall, the electrical parameters obtained for both recipes were agreeable with ITRS requirement and other reported works except for the result of saturation current. This

could be due to the direct scaling. Other parameters such as subthreshold current could not be compared due to not all detailed parameters could be displayed to the public.

In conclusion, both recipes had its own tradeoff. Implementation of other submicron technology may have benefit at one area but at the same time other area experienced detrimental effect.

5.2 Recommendation

In order to obtain the optimum design, the LOCOS could be replaced with the advanced technology such as Silicon on Insulator (SOI) as LOCOS suffered from bird beaks effect. As channel length is scaled down, the gate dielectric thickness must also need to be scaled. Silicon dioxide thickness limit will be reached approximately when the gate to channel tunneling current becomes equal to off state source to drain subthreshold leakage. Thus, another alternative is to use high dielectric constant material.

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APPENDICES

APPENDIX A

SIMULATION PROCESS FOR SUBMICRON TECHNOLOGY 1

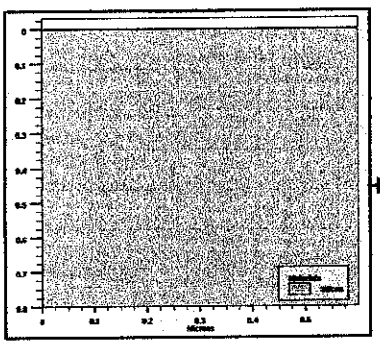

Figure 24 Initial wafer

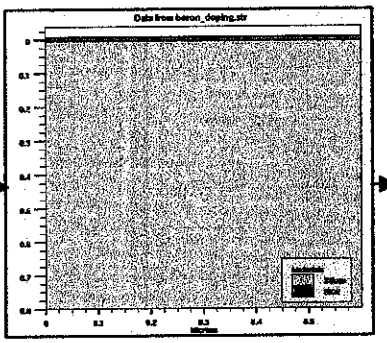

Figure 25 Grow oxide

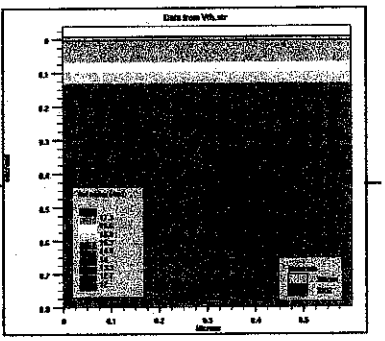

Figure 26 V_{TH} implant

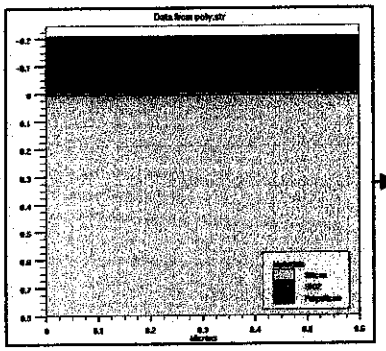

Figure 27 Deposit polysilicon

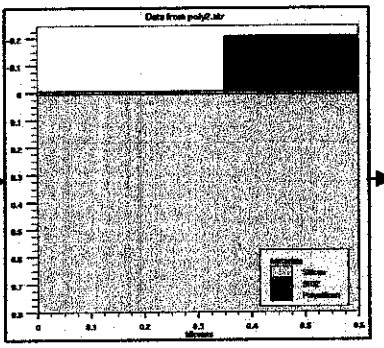

Figure 28 Etch polysilicon

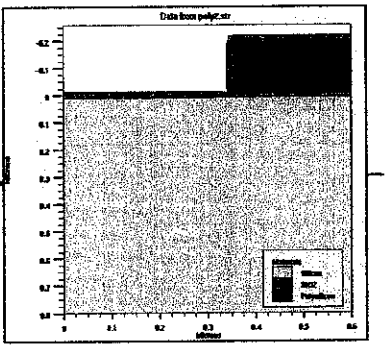

Figure 29 Polysilicon oxidation

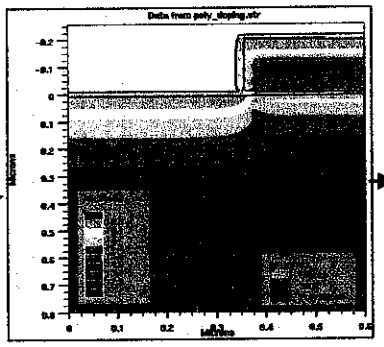

Figure 30 Phosphorous implantation

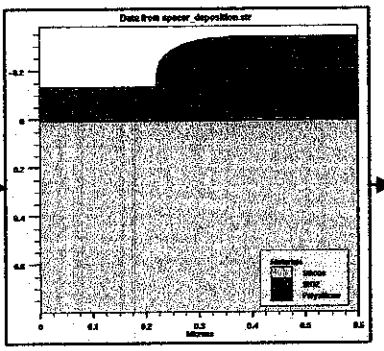

Figure 31 Deposit oxide spacer

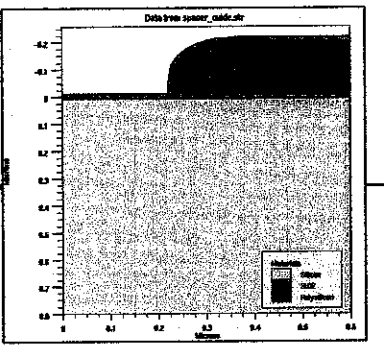

Figure 32 Etch spacer

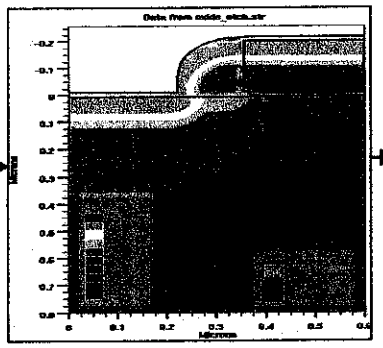

Figure 33 Arsenic implantation

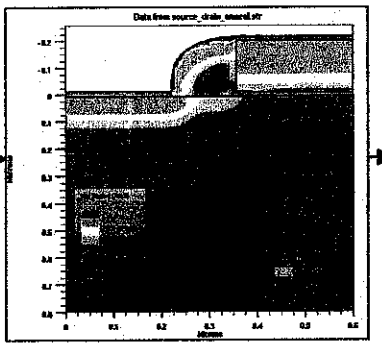

Figure 34 SD anneal

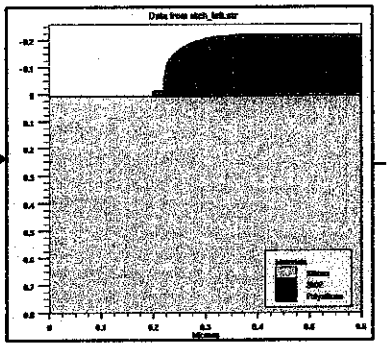

Figure 35 Deposit aluminum

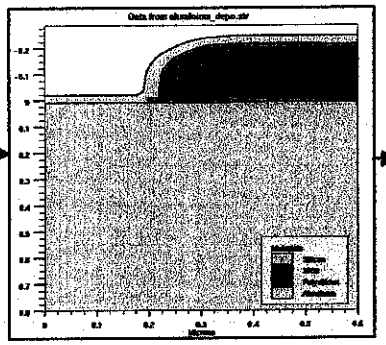

Figure 36 Deposit aluminum

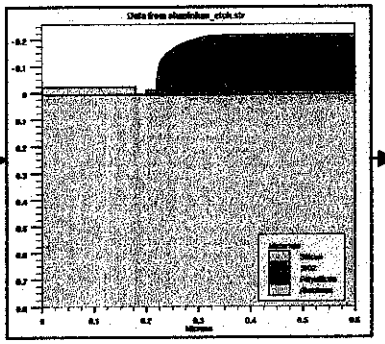

Figure 37 Etch aluminum

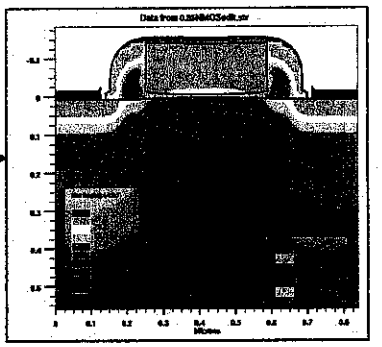

Figure 38 Final structure

APPENDIX B

SIMULATION PROCESS FOR SUBMICRON TECHNOLOGY 2

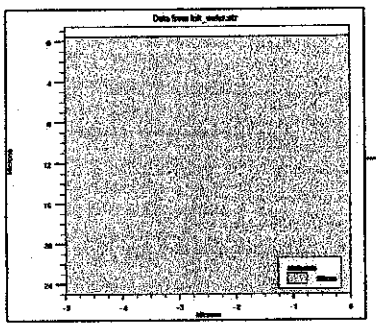

Figure 39 Initial wafer

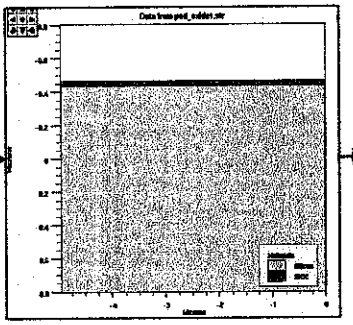

Figure 40 Pad oxide 1

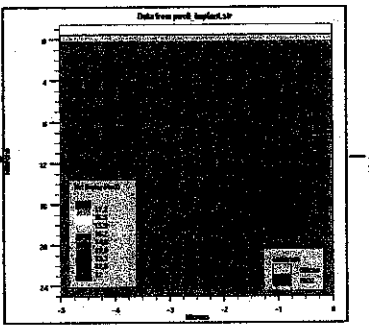

Figure 41Well implant

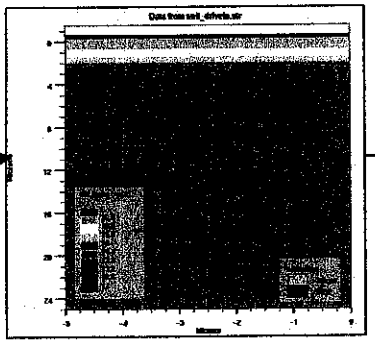

Figure 42 Well drive-in

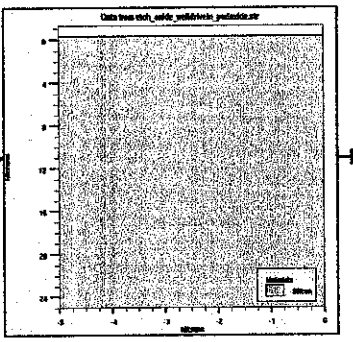

Figure 43 Etch pad oxide 1

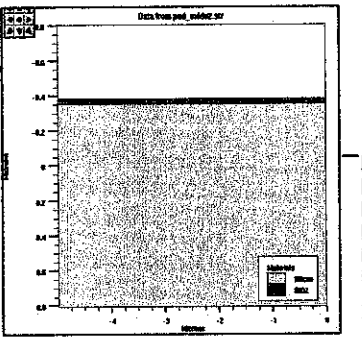

Figure 44 Pad oxide 2

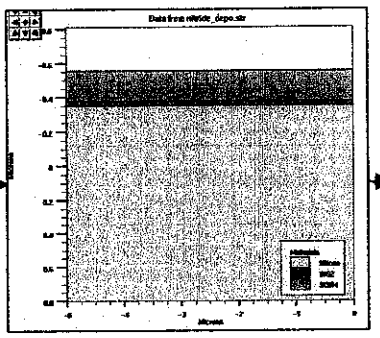

Figure 45 Nitride deposition

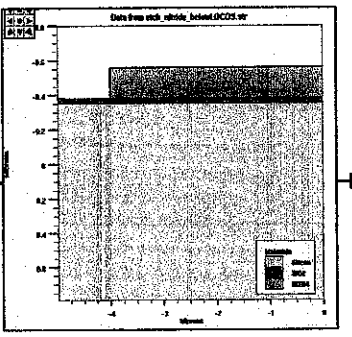

Figure 46 Etch nitride

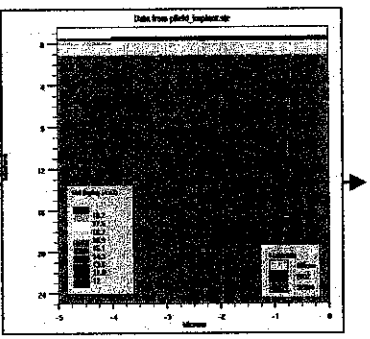

Figure 47 Field implant

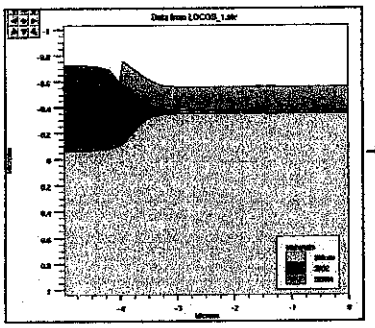

Figure 48 LOCOS

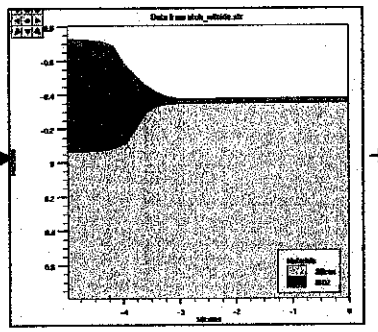

Figure 49 Etch nitride

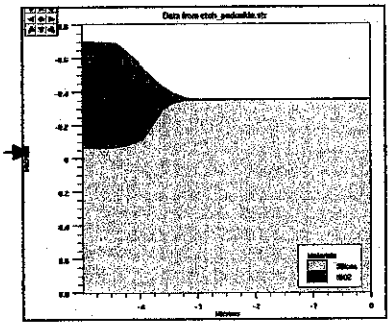

Figure 50 Etch pad oxide

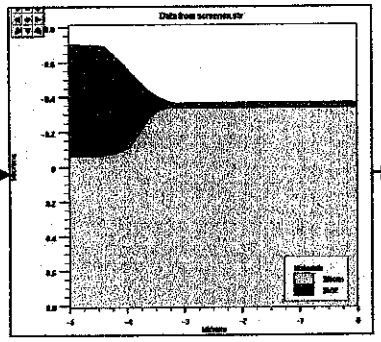

Figure 51 Screen oxidation

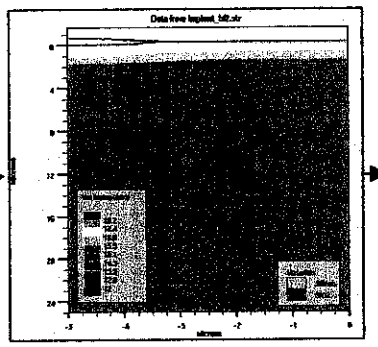

Figure 52 V_{TH} implant

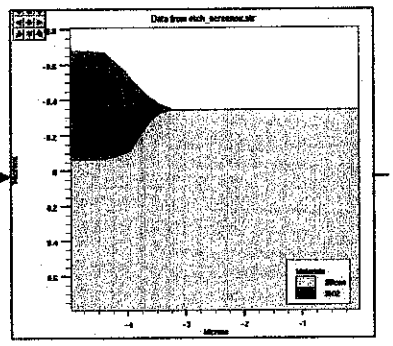

Figure 53 Etch screen oxidation

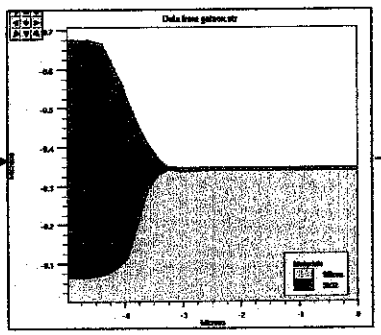

Figure 54 Gate oxidation

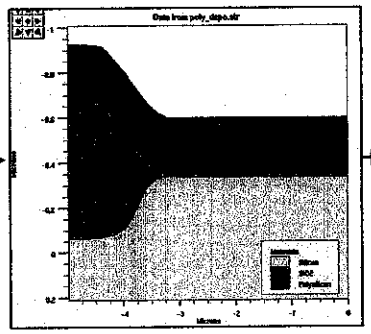

Figure 55 Polysilicon deposition

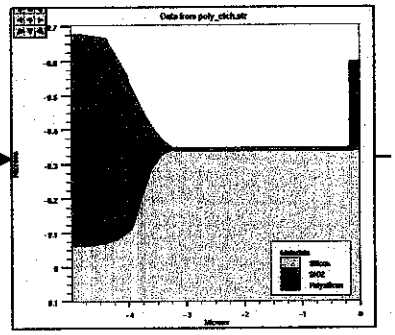

Figure 56 Polysilicon etch

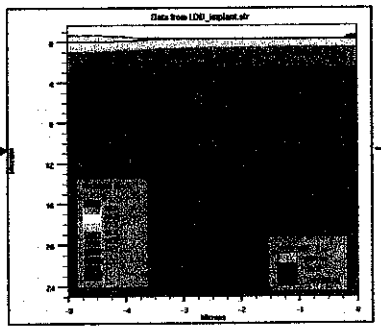

Figure 57 LDD implant

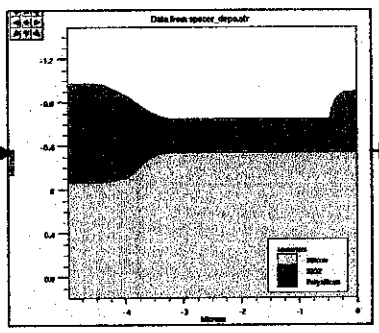

Figure 58 Spacer deposition

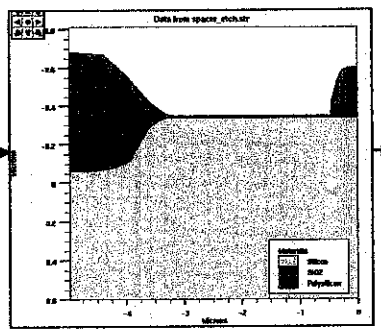

Figure 59 Spacer etch

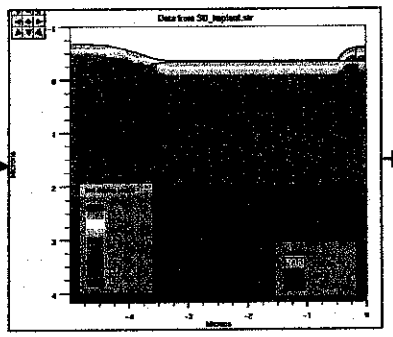

Figure 60 SD Implant oxidation after SD

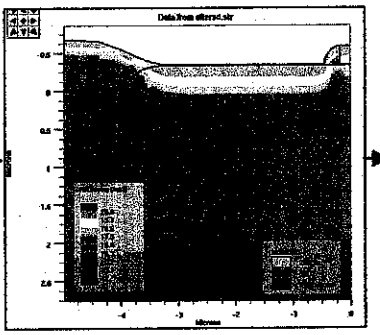

Figure 61RTA

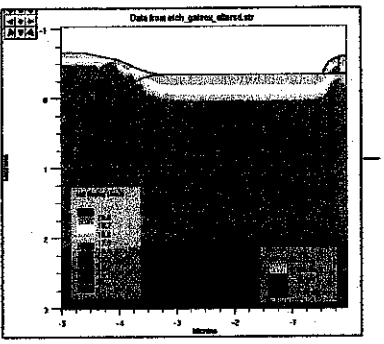

Figure 62 Etch gate

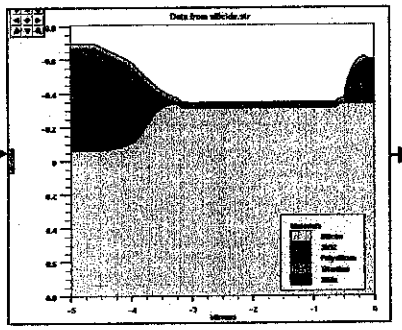

Figure 63 Silicidation

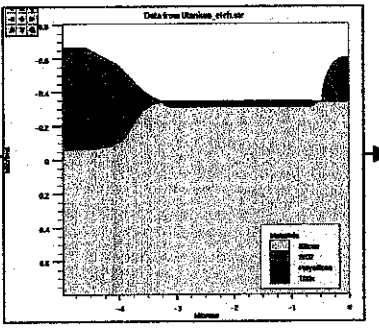

Figure 64 Titanium etch

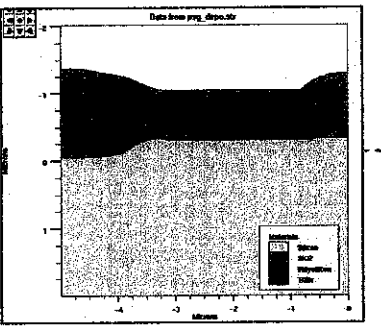

Figure 65 PSG deposition

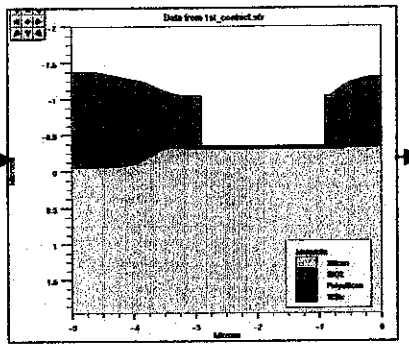

Figure 66 Etch contact hole

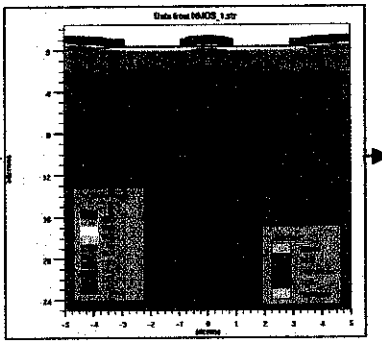

Figure 67 Full structure

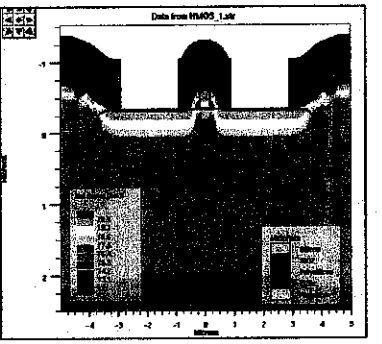

Figure 68 Enlarge full structure

APPENDIX C

RECIPE 0.13μM NMOS FOR SUBMICRON TECHNOLOGY 1

ATHENA

```
go athena

# Non-Uniform Grid(0.6umx0.8um)
line x loc=0.000 spac=0.0260
line x loc=0.052 spac=0.0026
line x loc=0.156 spac=0.0026
#
line y loc=0.000 spac=0.00208
line y loc=0.052 spac=0.026
line y loc=0.130 spac=0.013
line y loc=0.208 spac=0.039

struct outfile=grid.str

# Initial Silicon Structure with <100> Orientation
init silicon c.boron=1.0e14 orientation=100 two.d
struct outfile=initial.str

# Gate Oxidation
diffus time=1.5 temp=926.966 dryo2 press=0.984283 hcl.pc=3
struct outfile=gate_oxidatn.str

#
extract name="Gateoxide" thickness material="SiO~2" mat.occno=1
x.val=0.3
struct outfile=gateoxidethick.str

# Threshold Voltage Adjust implant
implant boron dose=30.5e11 energy=2.6 rotation=31 crystal
lat.ratio1=1.0 \
        lat.ratio2=1.0
structure outfile=boron_doping.str

# Conformal Polysilicon Deposition
deposit poly thick=0.052 divisions=10
structure outfile=poly.str

# Poly Definition
etch poly left p1.x=0.091
structure outfile=poly2.str

# Polysilicon Oxidation
method compress init.time=0.10 fermi
diffus time=0.75 temp=900 weto2 press=1.00 hcl.pc=0
structure outfile=poly_oxidation.str

# Polysilicon Doping
```

```
implant phosphor dose=3.0e13 energy=5.2 rotation=31 crystal
lat.ratio1=1.0 \
        lat.ratio2=1.0
structure outfile=poly_doping.str

# Spacer Oxide Deposition
deposit oxide thick=0.0312 divisions=10
structure outfile=spacer_deposition.str

# Spacer Oxide Etch
etch oxide dry thick=0.0312
structure outfile=spacer.str

# Source/Drain Implant
implant arsenic dose=5.0e15 energy=13 rotation=31 crystal
lat.ratio1=1.0 \
        lat.ratio2=1.0
structure outfile=oxide_etch.str

# Source/Drain Annealing
method vertical init.time=0.06 fermi
diffus time=1 temp=900 nitro press=1.00
structure outfile=source_drain_anneal.str

# Open Contact Window
etch oxide left p1.x=0.052
structure outfile=etch_left.str

# Aluminium Deposition
deposit alumin thick=0.0078 divisions=2
structure outfile=aluminium_depo.str

# Etch Aluminium
etch aluminum right p1.x=0.0468
structure outfile=aluminium_etch.str

#
extract name="nxj" xj material="Silicon" mat.occno=1 x.val=0.052
junc.occno=1
structure outfile=junc_depth.str

#
extract name="n++ sheet res" sheet.res material="Silicon" mat.occno=1 \
        x.val=0.013 region.occno=1
structure outfile=n++_sheet_res.str

#
extract name="ldd sheet resistance" sheet.res material="Silicon"
mat.occno=1 \
        x.val=0.078 region.occno=1
structure outfile=ldd_sheet_res.str

#
extract name="ldvt" ldvt ntype qss=1e10 x.val=0.13
structure outfile=extract_long_chan_Vth.str

#
```

```
struct mirror right

#
electrode name=source x=0.026

#
electrode name=drain x=0.286

#
electrode name=gate x=0.156

#
electrode name=backside backside

#
struct outfile=130nm.str
```

ATLAS

```
###### IdVg ######

go atlas

# set material models
models cvt srh print

contact name=gate n.poly
interface qf=3e10

method newton
solve init

# Bias the drain
solve vdrain=0.1

# Ramp the gate
log outf=idvgmos2ex01_1.log master
solve vgate=0 vstep=0.025 vfinal=1.5 name=gate
save outf=idvgmos1ex01_1.str

# plot results
tonyplot  idvgmos1ex01_1.log -set idvgmos1ex01_1_log.set

# extract device parameters
extract name="nvt"
(xintercept(maxslope(curve(abs(v."gate"),abs(i."drain")))) \
      - abs(ave(v."drain"))/2.0)

extract name="nbeta"
slope(maxslope(curve(abs(v."gate"),abs(i."drain")))) \
            * (1.0/abs(ave(v."drain")))

extract name="ntheta" ((max(abs(v."drain")) *
$"nbeta")/max(abs(i."drain"))) \
      - (1.0 / (max(abs(v."gate")) - ($"nvt")))
```

```
############## Idsat with Vdd=1.5V ################

go atlas


# Define the Gate Qss
interface qf=1e10

# Use the cvt mobility model for MOS
models cvt srh print numcarr=2

#
method gummel newton

# set gate biases with Vds=0.0
solve init
solve vgate=0.3 outf=solve_tmp1
solve vgate=0.6 outf=solve_tmp2
solve vgate=0.9 outf=solve_tmp3
solve vgate=1.2 outf=solve_tmp4
solve vgate=1.5 outf=solve_tmp5


#load in temporary files and ramp Vds
load infile=solve_tmp1
log outf=mos1ex02_1.log
solve name=drain vdrain=0 vfinal=1.5 vstep=0.025


load infile=solve_tmp2
log outf=mos1ex02_2.log
solve name=drain vdrain=0 vfinal=1.5 vstep=0.025


load infile=solve_tmp3
log outf=mos1ex02_3.log
solve name=drain vdrain=0 vfinal=1.5 vstep=0.025

load infile=solve_tmp4
log outf=mos1ex02_4.log
solve name=drain vdrain=0 vfinal=1.5 vstep=0.025

load infile=solve_tmp5
log outf=mos1ex02_5.log
solve name=drain vdrain=0 vfinal=1.5 vstep=0.025

# extract max current and saturation slope
extract name="nidsmax" max(abs(i."drain"))

#
tonyplot -overlay -st mos1ex02_1.log  mos1ex02_2.log mos1ex02_3.log
mos1ex02_4.log mos1ex02_5.log -set mos1ex02_1.set
```

```
############# Subvt ################
go atlas


# set material models
models cvt srh print
interface qf=1e10

# get initial solution

solve init

method gummel newton
solve prev


# Bias the drain a bit...
solve vdrain=0 vstep=0.01 vfinal=0.05 name=drain

# Ramp the gate to a volt...
log outf=mos1ex03_1.log master
solve vgate=0 vstep=0.025 vfinal=1.5 name=gate
save outf=mos1ex03_1.str

# extract the device parameter SubVt...
extract init inf="mos1ex03_1.log"
extract name="nsubvt"
1.0/slope(maxslope(curve(abs(v."gate"),log10(abs(i."drain")))))

tonyplot mos1ex03_1.log -set mos1ex03_1_log.set

quit
```

APPENDIX D

RECIPE 0.13μM NMOS FOR SUBMICRON TECHNOLOGY 2

ATHENA

```
go athena

#
line x loc=-5.0 spac=0.1
line x loc=-2.0 spac=0.1
line x loc=-0.65 spac=0.05
line x loc=0 spac=0.05

#
line y loc=-0.45 spac=0.05
line y loc=0 spac=0.05
line y loc=0.01 spac=0.05
line y loc=0.2 spac=0.05
line y loc=0.4 spac=0.05
line y loc=0.6 spac=0.1
line y loc=1.2 spac=0.1
line y loc=6 spac=0.1
line y loc=10 spac=0.3
line y loc=12 spac=0.4
line y loc=15 spac=0.4
line y loc=20 spac=0.4
line y loc=25 spac=0.4



#
init orientation=100 c.boron=3e14 space.mul=2 two.d
structure outfile=3init_wafer.str

#
method full.cpl

# PAD OXIDATION 250A
method grid.oxide=0.005
diffus time=21 temp=1000 dryo2
diffus time=15 temp=1000 nitro
structure outfile=3pad_oxide1.str

#
extract name="Pad oxide_1" thickness material="SiO~2" mat.occno=1
x.val=-2.0


# P-WELL IMPLANT
implant boron dose=5e12 energy=60 tilt=0 rotation=0 pears unit.damage
dam.factor=0.01
```

```
structure outfile=3pwell_implant.str

# WELL DRIVE-IN
diffus time=60 temp=750 t.final=1100 nitro
diffus time=150 temp=1100 dryo2
diffus time=15 temp=1100 nitro
structure outfile=3well_drivein.str

# ETCH OXIDE THAT RESULTS FROM WELL DRIVE-IN AND THE PREVIOUS PAD OXIDE
etch oxide all
structure outfile=3etch_oxide_welldrivein_padoxide.str

# PAD OXIDATION 250A
diffus time=21 temp=1000 dryo2
diffus time=15 temp=1000 nitro
structure outfile=3pad_oxide2.str

#
extract name="Pad oxide_2" thickness material="SiO~2" mat.occno=1
x.val=-2.0

# NITRIDE DEPOSITION
deposit nitride thick=0.18 divisions=10
structure outfile=3nitride_depo.str

# ETCH NITRIDE OUTSIDE OF THE ACTIVE REGION (means below LOCOS area)
etch nitride left p1.x=-4.0
structure outfile=3etch_nitride_belowLOCOS.str

# P-FIELD IMPLANT (underneath LOCOS area, active area are covered)
implant boron dose=2e13 energy=80 tilt=0 rotation=0 pears unit.damage
dam.factor=0.01
structure outfile=3pfield_implant.str

# LOCOS OXIDATION 5500A
method grid.oxide=0.055
diffus time=120 temp=1000 weto2
diffus time=20 temp=1000 nitro

#
extract name="LOCOS" thickness material="SiO~2" mat.occno=1 x.val=-4.5

structure outfile=3LOCOS_1.str

# ETCH ALL NITRIDE
etch nitride all
structure outfile=3etch_nitride.str

# ETCH PAD OXIDE (cannot etch all, otherwise etch LOCOS also)
etch oxide dry thick=0.025
structure outfile=3etch_padoxide.str

# SCREEN OXIDATION 250A (if not enough, depo to compensate)
method grid.oxide=0.005
diffus time=21 temp=1000 dryo2
diffus time=15 temp=1000 nitro
```

```
#
extract name="Screen oxide" thickness material="SiO~2" mat.occno=1
x.val=-2.0

structure outf=3screenox.str

# NVT IMPLANT BORON TO SHIFT THE THRESHOLD (throughout active region)
implant bf2 dose=1.0769e13 energy=50 tilt=0 rotation=0 pears
unit.damage dam.factor=0.01
structure outfile=3implant_bf2.str

# ETCH SCREEN OXIDE
etch oxide dry thick=0.025
structure outfile=3etch_screenox.str

# OXIDIZE THE GATE 80A (if not enough,depo to compensate)
method grid.oxide=0.004
diffus time=23 temp=800 dryo2
diffus time=30 temp=1000 nitro

#
extract name="Gate oxide" thickness material="SiO~2" mat.occno=1
x.val=-2.0

structure outf=3gateox.str

# DEPOSIT UNDOPED POLY GATE 2500A
deposit poly thick=0.25 divisions=10
structure outfile=3poly_depo.str

# ETCH POLYSILICON
etch poly left p1.x=-0.065
structure outfile=3poly_etch.str

# N-TYPE LDD IMPLANT
implant arsenic dose=5e13 energy=30 tilt=7 rotation=0 pears unit.damage
dam.factor=0.01
implant arsenic dose=5e13 energy=30 tilt=-7 rotation=0 pears
unit.damage dam.factor=0.01
structure outfile=3LDD_implant.str

# LDD SPACER DEPOSITION (SPACER WIDTH TARGET=3000A)
deposit oxide thick=0.3 divisions=10
structure outfile=3spacer_depo.str

# LDD SPACER FORMATION
etch oxide dry thick=0.3
structure outfile=3spacer_etch.str

# N+ GATE AND S/D IMPLANT
implant phosphor dose=3e15 energy=40 tilt=0 rotation=0 pears
unit.damage dam.factor=0.01
structure outfile=3SD_implant.str

# GATE AND S/D ANNEAL (RTA)
diffus time=0.167 temp=900 nitro
diffus time=0.083 temp=1050 nitro
```

```
structure outf=3aftersd.str

# ETCH GATE OXIDE THICKNESS
etch oxide dry thick=0.008
structure outfile=3etch_gateox_aftersd.str

# SILICIDATION
deposit titanium thick=0.03

#
diffus time=0.25 temp=650 nitro

structure outfile=3silicide.str

# ETCH TITANIUM
etch titanium all
structure outfile=3titanium_etch.str

# PSG DEPOSITION 700nm
deposit oxide thick=0.7 divisions=10
structure outfile=3psg_depo.str

# PSG DENSIFICATION
diffus time=0.167 temp=900 nitro

structure outfile=3PSG.str


# ETCH CONTACT HOLES
etch oxide start x=-2.9 y=-1.5
etch cont x=-2.9 y=0
etch cont x=-0.9 y=0
etch done x=-0.9 y=-1.5

structure outfile=3_1st_contact.str


# EXTRACT DESIGN PARAMETERS

# extract the long chan Vt
extract name="1dvt" 1dvt ntype vb=0.0 qss=1e10 x.val=-0.001

# Extract final S/D Xj
extract name="nxj" xj silicon mat.occno=1 x.val=-2.0 junc.occno=1

# Extract the surface conc under the channel
extract name="chan surf conc" surf.conc impurity="Net Doping"\
material="Silicon" mat.occno=1 x.val=-0.1

structure mirror right

electrode name=gate x=0 y=-0.59
electrode name=source x=-2.5
electrode name=drain x=2.5
electrode name=substrate backside
```

```
structure outfile=NMOS_3.str

#PLOT THE STRUCTURE
tonyplot NMOS_3.str -set NMOS_3.set

go devedit
work.area x1=-5 y1=-1.3680302 x2=5 y2=5
# devedit 2.6.0.R (Thu Dec 12 12:40:19 PST 2002)
# libSvcFile 1.8.3 (Sat Dec  7 17:56:58 PST 2002)
# libsflm 4.14.3 (Sat Dec  7 18:02:49 PST 2002)
# libSDB 1.4.3 (Tue Dec 10 19:51:05 PST 2002)
# libDW_Version 2.0.0.R (Thu Nov 28 05:44:29 PST 2002)
region reg=1 mat=Silicon \
      polygon="-5,-0.063 -4.589,-0.063 -4.387,-0.071 -4.182,-0.084 -
3.952,-0.116 -3.603,-0.292 -3.425,-0.331 -3.257,-0.343 -3.243,-0.334 -
3.207,-0.324 "\
      "-3.057,-0.315 -3.0322,-0.315 -2.997,-0.314 -0.557,-0.314 -
0.462,-0.323 -0.419,-0.34 0.419,-0.34 0.462,-0.323 0.557,-0.314 3.033,-
0.314 "\
      "3.058,-0.315 3.207,-0.324 3.243,-0.334 3.257,-0.343 3.425,-0.331
3.603,-0.292 3.952,-0.116 4.182,-0.084 4.387,-0.071 4.592,-0.071 "\
      "4.794,-0.063 5,-0.063 5,5 -5,5"
#
constr.mesh region=1 default

region reg=2 mat="Silicon Oxide" \
      polygon="-5,-1.368 -4.657,-1.368 -4.581,-1.365 -3.989,-1.271 -
3.903,-1.251 -3.787,-1.218 -3.728,-1.199 -3.631,-1.161 -3.445,-1.097 -
3.394,-1.082 "\
      "-3.312,-1.061 -3.276,-1.053 -3.23,-1.045 -3.057,-1.045 -3.0322,-
1.044 -2.9,-1.044 -2.9,-0.344 -2.997,-0.344 -3.022,-0.345 -3.057,-0.345
"\
      "-3.204,-0.355 -3.205,-0.345 -3.23,-0.346 -3.241,-0.346 -3.257,-
0.343 -3.425,-0.331 -3.603,-0.292 -3.952,-0.116 -4.182,-0.084 -4.387,-
0.071 "\
      "-4.589,-0.063 -5,-0.063"
#
constr.mesh region=2 default

region reg=3 mat="Silicon Oxide" \
      polygon="-0.419,-0.34 -0.514,-0.344 -0.9,-0.344 -0.9,-1.044 -
0.763,-1.044 -0.729,-1.073 -0.623,-1.144 -0.584,-1.167 -0.509,-1.204 -
0.419,-1.238 "\
      "-0.244,-1.28 0,-1.299 0.244,-1.28 0.419,-1.238 0.509,-1.204
0.584,-1.167 0.623,-1.144 0.729,-1.073 0.763,-1.044 0.9,-1.044 "\
      "0.9,-0.344 0.557,-0.344 0.507,-0.342 0.464,-0.342 0.419,-0.34" \
      polygon="0.125,-0.346 0.125,-0.583 0.126,-0.591 0.1,-0.596 0,-
0.601 -0.1,-0.596 -0.126,-0.591 -0.125,-0.583 -0.125,-0.346"
#
constr.mesh region=3 default

region reg=4 mat=PolySilicon \
      polygon="-0.125,-0.346 -0.125,-0.583 -0.069,-0.568 -0.044,-0.58
0,-0.57 0.044,-0.58 0.069,-0.568 0.125,-0.583 0.125,-0.346"
#
constr.mesh region=4 default
```

```
region reg=5 name=source mat="Titanium Silicide" elec.id=2 work.func=0
\
      polygon="-2.997,-0.314 -3.0322,-0.315 -3.057,-0.315 -3.207,-0.324
-3.243,-0.334 -3.257,-0.343 -3.241,-0.346 -3.23,-0.346 -3.205,-0.345 -
3.204,-0.355 "\
      "-3.057,-0.345 -3.022,-0.345 -2.997,-0.344 -2.9,-0.344 -0.9,-
0.344 -0.514,-0.344 -0.419,-0.34 -0.462,-0.323 -0.557,-0.314"
#constr.mesh region=5 default

region reg=6 name=gate mat="Titanium Silicide" elec.id=1 work.func=0 \
      polygon="-0.044,-0.58 -0.069,-0.568 -0.125,-0.583 -0.126,-0.591 -
0.1,-0.596 0,-0.601 0.1,-0.596 0.126,-0.591 0.125,-0.583 0.069,-0.568
"\
      "0.044,-0.58 0,-0.57"
#
constr.mesh region=6 default

region reg=7 mat="Silicon Oxide" \
      polygon="5,-0.063 4.794,-0.063 4.592,-0.071 4.387,-0.071 4.182,-
0.084 3.952,-0.116 3.603,-0.292 3.425,-0.331 3.257,-0.343 3.243,-0.346
"\
      "3.216,-0.345 3.205,-0.345 3.204,-0.355 3.058,-0.345 3.033,-0.344
2.9,-0.344 2.9,-1.044 3.204,-1.044 3.222,-1.045 3.276,-1.053 "\
      "3.312,-1.061 3.394,-1.082 3.445,-1.097 3.631,-1.161 3.728,-1.199
3.787,-1.218 3.903,-1.251 3.989,-1.271 4.581,-1.365 4.924,-1.365 "\
      "5,-1.368"
#
constr.mesh region=7 default

region reg=8 name=drain mat="Titanium Silicide" elec.id=3 work.func=0 \
      polygon="0.557,-0.314 0.462,-0.323 0.419,-0.34 0.464,-0.342
0.507,-0.342 0.557,-0.344 0.9,-0.344 2.9,-0.344 3.033,-0.344 3.058,-
0.345 "\
      "3.204,-0.355 3.205,-0.345 3.216,-0.345 3.243,-0.346 3.257,-0.343
3.243,-0.334 3.207,-0.324 3.058,-0.315 3.033,-0.314"
#
constr.mesh region=8 default

substrate name="substrate" electrode=4 workfunction=0


# Set Meshing Parameters
#
base.mesh height=10 width=10
#
bound.cond !apply max.slope=28 max.ratio=300 rnd.unit=0.001
line.straightening=1 align.points when=automatic
#
imp.refine imp="Net Doping" scale=log
imp.refine min.spacing=0.02
#
constr.mesh max.angle=90 max.ratio=300 max.height=10000 \
      max.width=10000 min.height=0.0001 min.width=0.0001
#
constr.mesh type=Semiconductor default
#
constr.mesh type=Insulator default
```

```
#
constr.mesh type=Metal default
#
constr.mesh type=Other default
#
constr.mesh region=1 default
#
constr.mesh region=2 default
#
constr.mesh region=3 default
#
constr.mesh region=4 default
#
constr.mesh region=5 default
#
constr.mesh region=6 default
#
constr.mesh region=7 default
#
constr.mesh region=8 default
Mesh Mode=MeshBuild
refine mode=both x1=-2.94 y1=-0.34 x2=2.92 y2=0.47

structure outf=AB.str
```

ATLAS

```
###### IdVg ######

go atlas


# set material models
models cvt srh print

contact name=gate n.poly
interface qf=3e10

method newton
solve init

# Bias the drain
solve vdrain=0.1

# Ramp the gate
log outf=idvgmos2ex01_1.log master
solve vgate=0 vstep=0.025 vfinal=1.5 name=gate
save outf=idvgmos2ex01_1.str

# plot results
tonyplot  idvgmos2ex01_1.log -set idvgmos2ex01_1_log.set

# extract device parameters
extract name="nvt"
(xintercept(maxslope(curve(abs(v."gate"),abs(i."drain")))) \
      - abs(ave(v."drain"))/2.0)
```

```
extract name="nbeta"
slope(maxslope(curve(abs(v."gate"),abs(i."drain")))) \
            * (1.0/abs(ave(v."drain")))

extract name="ntheta" ((max(abs(v."drain")) *
$"nbeta")/max(abs(i."drain"))) \
      - (1.0 / (max(abs(v."gate")) - ($"nvt")))


############## Idsat with Vdd=1.5V ################


go atlas


# Define the Gate Qss
interface qf=1e10

# Use the cvt mobility model for MOS
models cvt srh print numcarr=2

#
method gummel newton

# set gate biases with Vds=0.0
solve init
solve vgate=0.3 outf=solve_tmp1
solve vgate=0.6 outf=solve_tmp2
solve vgate=0.9 outf=solve_tmp3
solve vgate=1.2 outf=solve_tmp4
solve vgate=1.5 outf=solve_tmp5


#load in temporary files and ramp Vds
load infile=solve_tmp1
log outf=mos2ex02_1.log
solve name=drain vdrain=0 vfinal=1.5 vstep=0.025


load infile=solve_tmp2
log outf=mos2ex02_2.log
solve name=drain vdrain=0 vfinal=1.5 vstep=0.025


load infile=solve_tmp3
log outf=mos2ex02_3.log
solve name=drain vdrain=0 vfinal=1.5 vstep=0.025

load infile=solve_tmp4
log outf=mos2ex02_4.log
solve name=drain vdrain=0 vfinal=1.5 vstep=0.025

load infile=solve_tmp5
log outf=mos2ex02_5.log
solve name=drain vdrain=0 vfinal=1.5 vstep=0.025
```

```
# extract max current and saturation slope
extract name="nidsmax" max(abs(i."drain"))

#
tonyplot -overlay -st mos2ex02_1.log  mos2ex02_2.log mos2ex02_3.log
mos2ex02_4.log mos2ex02_5.log -set mos2ex02_1.set

############# Subvt ################
go atlas


# set material models
models cvt srh print
interface qf=1e10

# get initial solution

solve init

method gummel newton
solve prev


# Bias the drain a bit...
solve vdrain=0 vstep=0.01 vfinal=0.05 name=drain

# Ramp the gate to a volt...
log outf=mos2ex03_1.log master
solve vgate=0 vstep=0.025 vfinal=1.5 name=gate
save outf=mos2ex03_1.str

# extract the device parameter SubVt...
extract init inf="mos3ex03_1.log"
extract name="nsubvt"
1.0/slope(maxslope(curve(abs(v."gate"),log10(abs(i."drain")))))

tonyplot mos2ex03_1.log -set mos2ex03_1_log.set

quit
```