

**OPTICAL TRANSCEIVER INTERFACE FOR DATA TRANSMISSION  
OVER OPTICAL LINK**

By

**VIMELESHWARY A/P SUKUMARAN**

**FINAL PROJECT REPORT**

**Submitted to the Electrical & Electronics Engineering Programme  
in Partial Fulfillment of the Requirements  
for the Degree  
Bachelor of Engineering (Hons)  
(Electrical & Electronics Engineering)**

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# **CERTIFICATION OF APPROVAL**


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Approved:



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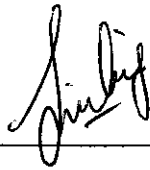
Dr. Lee Sheng Chyan  
Project Supervisor

**UNIVERSITI TEKNOLOGI PETRONAS  
TRONOH, PERAK**

June 2007

## **CERTIFICATION OF ORIGINALITY**

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.



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**Vimeleshwary A/P Sukumaran**

## **ABSTRACT**

This final year Project Part 2 is designed for all final year students and it is compulsory to be taken. It is designed such so that all the final year students will be trained to produce practical solutions besides having a hands on feel before leaving to the industry. This report presents the intention of creating an optical transceiver interface for data transmission over an optical link. The project is targeted to be completed by the end of the course that is by developing the modulator / demodulator which converts the electrical data from PC to optical data as well as retrieve the optical data back to electrical data before it can be read by the other client PC at the receiving end. These days, the utilization of data via the optical transceiver is very limited and in the recent years, news about communication networks technology always seems to involve some pronouncement on the urgent need for more bandwidth. Thus this is part of creating a device to overcome all these problems. This project covers two parts that is research and design. Fourteen weeks have been allocated to complete the design of this project. The project has been researched about and certain components have been purchased to complete it. Besides that, this project also allows us to design on our own and implement as we want it to be.

## **ACKNOWLEDGEMENTS**

Firstly, I would like to thank God for giving me the chance to be able to engage in this project. With Him, all things are possible.

Secondly, I would like to thank my supervisor, Dr. Lee Sheng Chyan. Dr. Lee Sheng Chyan has been a great help in providing guidance and direction to where this project should lead while giving valuable comments on work done.

Last but not least. I express my gratitude towards friends and family members who have indirectly contributed towards the successful execution of this project.

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## **LIST OF ABBREVIATIONS**

**LED – LIGHT EMMITING DIODE**

**RF – RADIO FREQUENCY**

**VCO – VOLTAGE CONTROLLED OSCILLATOR**

**DC – DIRECT CURRENT**

**FM – FREQUENCY MODULATION**

**MSM – METAL SEMICONDUCTOR METAL**

**TIA – TRANSIMPEDANCE AMPLIFIER**

**AGC – AUTOMATIC GAIN CONTROL**

**IB – BASE CURRENT**

**PAL – PHASE ALTERNATING LINE**

# CHAPTER 1

## INTRODUCTION

### 1.1 Background of Study

#### 1.1.1 *Optical Transceiver Interface for Data Transmission over Optical Link*

Our current "age of technology" is the result of many brilliant inventions and discoveries, but it is our ability to transmit information, and the media we use to do it, that is perhaps most responsible for its evolution. Progressing from the copper wire of a century ago to today's fiber optic cable, our increasing ability to transmit more information, more quickly and over longer distances has expanded the boundaries of our technological development in all areas.

Optical communication is any form of telecommunication that uses light as the transmission medium.

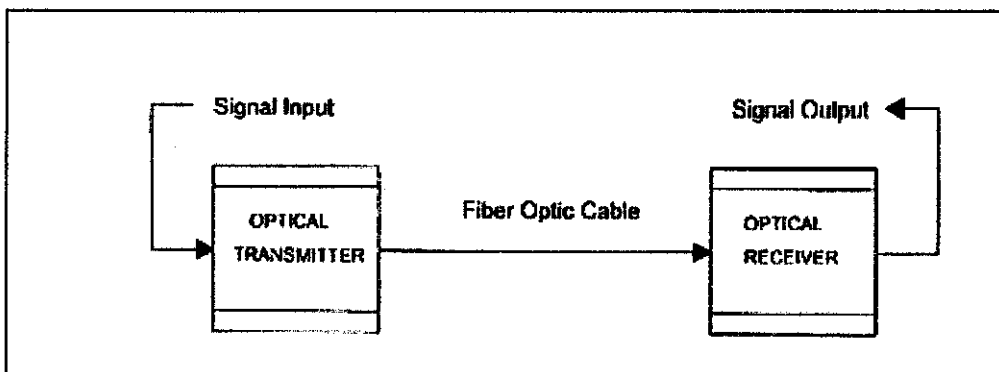


Figure 1 Block diagram of an optical system

An optical communication system (figure 1) consists of a transmitter, which encodes a message into an optical signal, a channel, which carries the signal to its destination, and a receiver, which reproduces the message from the received optical signal.

Fiber-optic communication is a method of transmitting information from one place to another by sending light through an optical fiber. The light forms an electromagnetic carrier wave that is modulated to carry information. First developed in the 1970s, fiber-optic communication systems have revolutionized the telecommunications industry and played a major role in the advent of the Information Age. Because of its advantages over electrical transmission, the use of optical fiber has largely replaced copper wire communications.

The process of communicating using fiber-optics involves the following basic steps:

- i. Creating the optical signal using a transmitter.
- ii. Relaying the signal along the fiber, ensuring that the signal does not become too distorted or weak.
- iii. Receiving the optical signal and converting it into an electrical signal.

The transmitter converts an electrical analog or digital signal into a corresponding optical signal. The source of the optical signal can be either a light emitting diode, or a solid state laser diode. The most popular wavelengths of operation for optical transmitters are 850, 1310, or 1550 nanometers.

### ***1.1.2 Difference of usage between an electrical transmission and optical transmission***

The choice between optical fiber and electrical (or "copper") transmission for a particular system is made based on a number of trade-offs. Optical fiber is generally chosen for systems with higher bandwidths or spanning longer distances than electrical cabling can provide. The main benefits of fiber are its exceptionally low loss, allowing long distances between amplifiers or repeaters; and its inherently high data-carrying capacity, such that thousands of electrical links would be required to replace a single high bandwidth fiber. Another benefit of fiber is that even when run alongside each other for long distances, fiber cables experience effectively no crosstalk, in contrast to some types of electrical transmission lines.

In short distance and relatively low bandwidth applications, electrical transmission is often preferred because of its

- Lower material cost, where large quantities are not required.
- Lower cost of transmitters and receivers.
- Ease of splicing.
- Capability to carry electrical power as well as signals.

Because of these benefits of electrical transmission, optical communication is not common in short box-to-box, backplane, or chip-to-chip applications; however, optical systems on those scales have been demonstrated in the laboratory.

In certain situations fiber may be used even for short distance or low bandwidth applications, due to other important features:

- Immunity to electromagnetic interference, including nuclear electromagnetic pulses (although fiber can be damaged by alpha and beta radiation).

- High electrical resistance, making it safe to use near high-voltage equipment or between areas with different earth potentials.
- Lighter weight, important, for example, in aircraft.
- No sparks, important in flammable or explosive gas environments.
- Not electromagnetically radiating, and difficult to tap without disrupting the signal, important in high-security environments.
- Much smaller cable size - important where pathway is limited.

## **1.2 Background of the project**

This project kicks off by investigating the problems faced by using a normal coaxial transmission method in transmitting data. Next, a practical solution is derived to meet the needs of the users at this process that is not satisfying. This project aims to fill in the gaps in the current system by developing newer, more effective features that will result in better performance, efficiency and most importantly, user satisfaction.

## **1.3 Problem Statement**

Fiber optics is a very important technology. Mankind's future depends upon the effectiveness of his communications. That is expanded today mainly by the Internet, and that is being carried forward not the least by installation of optical networks, and advances in the technology.

Important advances have been in the purity of the fibers themselves, so the light signal can travel as far as possible without being amplified. This has been advanced to about 80 kilometers today, something which is quite amazing considering the thinness of the fiber.

Still, the big problem was that the light signal had to be amplified electronically, meaning it had to be translated into an electronic signal, amplified, and then translated back into an optical signal and sent on its way. This slowed things down

and made it more expensive. So it was a real breakthrough in the early nineties when researchers invented ways of amplifying the pure light signal by doping a part of the fiber with special compound, which when stimulated boosted the ongoing signal. It might have been impossible to keep up with bandwidth demand for the internet today without that invention.

There are still delays on the Internet all the time, even with high-speed connections, and even when accessing perfectly normal web pages. Secondly, there are not video on demand over the net yet. And thirdly there are all kinds of future applications, like telepresence, holographic transmission, and true Virtual Reality, none of which are even remotely approachable by the fastest technologies around today.

Large-scale video transmission systems have been going through a revolution for the past ten years. New technology has been developed that has given these systems a new approach to the overall application and design. Just as coaxial-based systems have given way to optical fiber applications, video transmission over optical fiber has been improved from simple analog modulation schemes to more complex digital compression techniques.

Copper cabling creates resistance and interference problems. Voice, video and data signals are weakened the further they are transmitted. The resistance in copper media slows down the signal or flow of current, limiting the speed of transmission on copper lines. Signals sent over copper wire are direct current electrical signals. Any other signals nearby, like magnetic signals or radio station transmissions, introduce interference and noise into transmission. This leads to people hearing radio station programming on telephone calls, and hearing another person's conversation due to "leaking" electrical transmissions (called crosstalk).

First, it is important to understand the methods of carrying multiple video signals on a fiber optic transmission system.

Analog modulation techniques have been around since video transmissions were first introduced in the late 1930's. Amplitude modulation (AM) and frequency modulation (FM) each have their benefits and limitations. They are, however, considered to be old technology. The devices needed for these methods no longer hold the price advantage they once did. The equipment is becoming obsolete or not cost effective for large-scale video transmission applications.

It is clearly known that FM and AM methods of transmitting signals in a fiber optic system is obsolete. But in this particular project design, the FM system is used to transmit video over an optical system. This is due to the low cost of design as the budget limits are RM 500 only. Besides that it would be a base of setting up a fiber optic project in Universiti Teknologi Petronas.

Hence this project is designed to cater the needs of transferring a video over an optical link just to cater to the demand of bandwidth, faster transmission and lossless video.

## **CHAPTER 2**

### **LITERATURE REVIEW AND THEORY**

#### **2.1 Components of a transmitter**

The most commonly used optical transmitters are semiconductor devices such as light-emitting diodes (LEDs) and laser diodes. The difference between LEDs and laser diodes is that LEDs produce incoherent light, while laser diodes produce coherent light. For use in optical communications, semiconductor optical transmitters must be designed to be compact, efficient, and reliable, while operating in an optimal wavelength range, and directly modulated at high frequencies.

In its simplest form, an LED is a forward-biased p-n junction, emitting light through spontaneous emission, a phenomenon referred to as electroluminescence. The emitted light is incoherent with a relatively wide spectral width of 30-60 nm. LED light transmission is also inefficient, with only about 1% of input power, or about 100 microwatts, eventually converted into “launched power” which has been coupled into the optical fiber. However, due to their relatively simple design, LEDs are very useful for low-cost applications.

Communications LEDs are most commonly made from gallium arsenide phosphide (GaAsP) or gallium arsenide (GaAs). Because GaAsP LEDs operate at a longer wavelength than GaAs LEDs (1.3 micrometers vs. 0.81-0.87 micrometers), their output spectrum is wider by a factor of about 1.7. The large spectrum width of LEDs causes higher fiber dispersion, considerably limiting their bit rate-distance product (a common measure of usefulness). LEDs are suitable primarily for local-area-network applications with bit rates of 10-100 Mb/s and transmission distances of a few kilometers. LEDs have also been developed that use several quantum wells to emit light at different wavelengths over a broad spectrum, and are currently in use for local-area WDM networks.



A semiconductor laser emits light through stimulated emission rather than spontaneous emission, which results in high output power (~100 mW) as well as other benefits related to the nature of coherent light. The output of a laser is relatively directional, allowing high coupling efficiency (~50%) into single-mode fiber. The narrow spectral width also allows for high bit rates since it reduces the effect of chromatic dispersion. Furthermore, semiconductor lasers can be modulated directly at high frequencies because of short recombination time.

Laser diodes are often directly modulated, that is the light output is controlled by a current applied directly to the device. For very high data rates or very long distance links, a laser source may be operated continuous wave, and the light modulated by an external device such as an electroabsorption modulator or Mach-Zehnder interferometer. External modulation increases the achievable link distance by eliminating laser chirp, which broadens the linewidth of directly-modulated lasers, increasing the chromatic dispersion in the fiber.

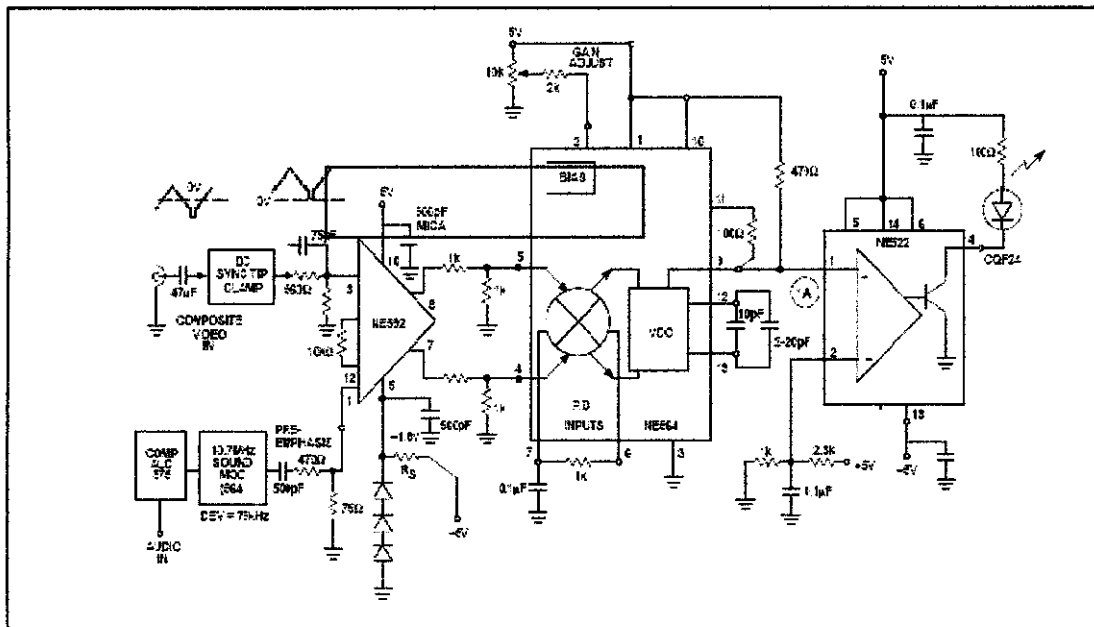


Figure 2 Components of the transmitter

In this circuit, the transmitter circuit consists of a wideband differential amplifier (NE592), a VCO (NE564) and an LED driver, the NE522 high speed comparator (see Figure 2). The video signal is AC coupled into the modulator preamplifier and followed by a sync tip clamp to provide DC restoration of the composite video signal and to prevent variation of modulation deviation with varying picture content. (A complete video clamp and sync processor may be designed using the TDA9045 and TDA2595 combination). A video signal level of 250 to 300mV peak is required to maintain optimum picture modulation. Since there is no AGC circuit in this particular design, this is a critical parameter and must be controlled to prevent over-modulation and picture degradation. Addition of an AGC using the above-mentioned parts would be a definite improvement for varying input level video. Using the present limited design, however, -10dB of attenuation was used with a 1V peak PAL signal source at 75W. This is the common level available from most standard video signal systems. Frequency compensation (pre-emphasis) is inserted in the form of a passive RC lead network at the Pin 14 input to the NE592 differential amplifier. This compensates for degenerative frequency distortion and provides better color balance in transmission. The main FM modulator consists of an NE564 used only as a linear wideband VCO. The other sections of the device are not used. Differential DC coupling to the VCO terminals is attained via the loop filter terminals, Pins 4 and 5. The NE564 VCO is designed as a differential current controlled balanced multivibrator. It possesses an extremely linear transfer function. The VCO center frequency is determined by value of the capacitance across Pins 12 and 13. In this particular circuit, the transmitter operates at 14.3MHz with the VCO set to 26.6MHz.

The slope of the VCO transfer function is termed K<sub>O</sub> and is measured in radians per second per volt or simply Herz per volt. Thus, to obtain the magnitude of the differential voltage for a given frequency deviation the relationship below is used:

$$VD = \frac{\Delta f}{K_0} \quad \text{Mhz}$$

$$K_0 \quad \text{MHz/V}$$

$$IB^2 = \text{Constant}$$

KO is dependent upon the control bias generator current at Pin 2. Higher current into Pin 2 results in a higher conversion gain, KO. For a center frequency of 1MHz and an 800mA bias current into Pin 2, KO is 1.7MHz/V across Pins 4 and 5 (VO). The value of KO also increases linearly with center frequency so that at 30MHz KO becomes 30X 1.7 or 51MHz/V. Note that in this design the bias current is set at 320mA; that is the device is sinking current into Pin 2. This lowers KO below the given value for 800mA requires a higher number of V/MHz to modulate the VCO. The signal to the VCO is DC coupled from the differential output of the NE592 in order to preserve bandwidth and to maintain proper biasing relative to the NE564.

### ***2.1.1 Setting FM deviation***

In order to calculate the approximate frequency deviation, a linear relationship between DKO and DIB2 is assumed. The value of KO for a Pin 2 bias of 320mA is determined by the following relationship:

$$\begin{aligned}
 KO &= \left[ \frac{(1.7-0.95) \times 320}{2 \times 800} + 0.95 \right] \text{ MHz/Volt} \\
 &= 1.1 \text{ MHz / V @ 1 MHz} \\
 &= 33 \text{ MHz / V @ 30 MHz}
 \end{aligned}$$

The measured differential voltage between Pins 4 and 5 for normal operating signal levels and standard PAL color bars transmitted is 80mVP-P. The estimated total deviation is then 1.3MHz. This results in a Video channel bandwidth for the 3.58MHz color signal of approximately:

$$\begin{aligned}
 &= 2(1.3 + 3.58)\text{MHz} \\
 &= 9.8\text{MHz}
 \end{aligned}$$

This is rather a small deviation for wideband video transmission and the decision was made to use the 2nd harmonic of the fundamental VCO frequency to obtain twice the deviation. The VCO modulator is then set at an IB of 320mA which provides sufficient 2nd harmonic content for this to operate successfully.

### **2.1.2 FM signal bandwidth**

For a total video bandwidth of 4.2MHz the transmission bandwidth is:

$$BW = 2 \times (1.3 + 4.2) = 22\text{MHz}$$

Note that a bandpass filter could be installed in the signal path between the NE592 preamp/buffer to reduce noise bandwidth, but this improvement was not tried. Adequate signal space for the baseband video and the 10.7MHz subcarrier would be 11MHz. (Filter characteristics must provide good differential gain and phase response.)

A second bandpass filter could be added in the path between the modulator and the LED driver stage (22MHz bandwidth). This would improve the overall video signal-to-noise ratio. The NE592 is biased with +5V and -1.8V to achieve the critical dynamic swing to properly slew the VCO over the required range without sacrificing faithful waveform reproduction in the transformation to linear FM modulation. Video signals contain both very low and high frequencies which are transient and phase sensitive. The unused input pins to the phase detector, Pins 6 and 7 bypassed to ground. Pin 3 is grounded. The 28.6MHz FM signal from the NE564 is taken from the Pin 9 open collector VCO output port which requires a 470Ω pull-up resistor to 5V. A 100Ω resistor is added to Pin 11 to improve the fall time of the output waveform. The signal is then fed into the NE522 (74F3040) high speed comparator where a threshold level is set up on the inverting terminal to provide duty cycle adjustment and noise threshold. The NE522 has an open collector output which lends itself easily to driving the LED transmitter diode (CQF24); the 74F3040 has a source-sink output stage which requires that the LED be connected. The CQF24 generates 100mW of 850nm optical energy with a typical rise and fall time of 10ns. It is rated at 250mW dissipation and 100mA continuous current.

## 2.2 Components of a receiver

The main component of an optical receiver is a photodetector that converts light into electricity through the photoelectric effect. The photodetector is typically a semiconductor-based photodiode, such as a p-n photodiode, a p-i-n photodiode, or an avalanche photodiode. Metal-semiconductor-metal (MSM) photodetectors are also used due to their suitability for circuit integration in regenerators and wavelength-division multiplexers.

The optical-electrical converter is typically coupled with a transimpedance amplifier and limiting amplifier to produce a digital signal in the electrical domain from the incoming optical signal, which may be attenuated and distorted by passing through the channel. Further signal processing such as clock recovery from data (CDR) by a phase-locked loop may also be applied before the data is passed on.

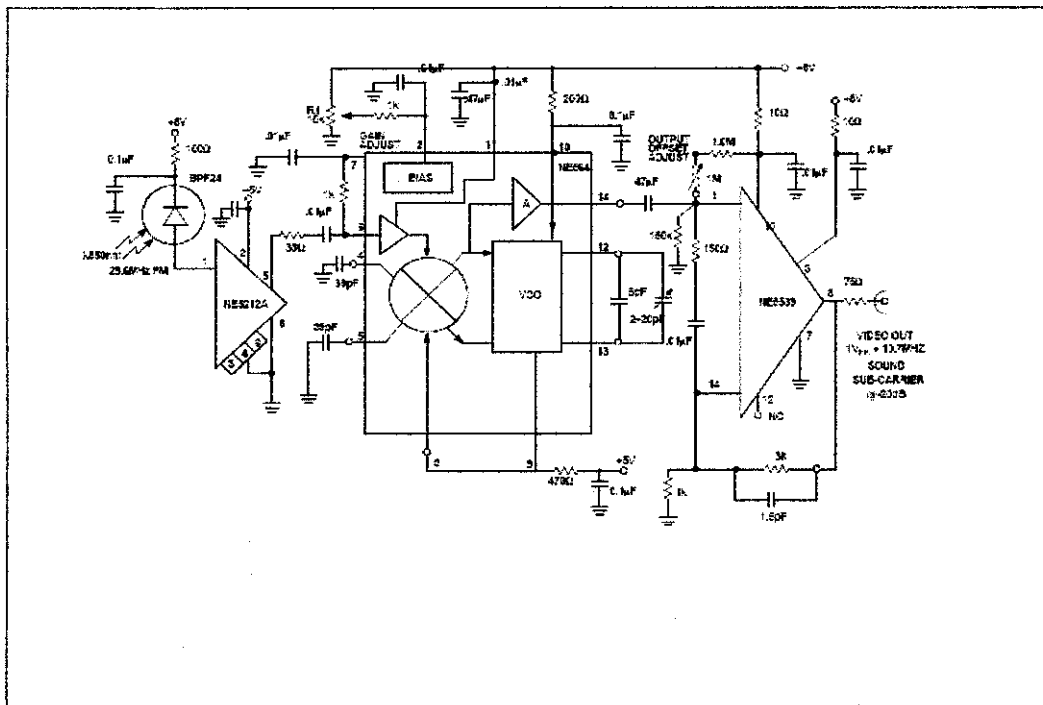


Figure 3 Components of the receiver

Here in this particular circuit, light energy from the fiber optic cable is fed to the BPF24 PIN diode and transformed to a small current typically in the 1 to 5mA range. This photodiode current carries all of the FM carrier information in the signal

bandwidth of approximately 22MHz centered at 28.6MHz. The photo-current is now amplified and transformed into a differential signal voltage by the NE5212 transimpedance amplifier (Pin 1 input). In this particular design, however, the output is not used differentially, but a single-ended signal is taken from Pin 5 of the NE5212 and AC coupled to Pin 6 of the NE564. The NE5212 has a differential transresistance of 14k. This translates to 14mV/mA of input current, yielding 35mV of differential output voltage for 2.5mA input current. Since the device is used single ended, only half, or 17.5mV, output is available to drive the phase detector of the NE564. The low signal level input to the PLL makes it necessary to run the gain setting bias at a higher level than usual; this, in addition to the wide bandwidth, requires a bias current of 2.2mA sinking into Pin 2 of the NE564. Another modification to the nominal NE564 operating conditions is the choice of a higher supply voltage on the phase detector portion of the device (+8V on Pin 1) to increase the linearity and dynamic range for fast video signals. The VCO section is supplied from +8V through a 200W dropping resistor and operates on 4.5V at Pin 10. (Note that the absolute maximum voltages for the phase detector and VCO are 14 and 6V, respectively).

### ***2.2.1 VCO Frequency Adjustments***

The NE564 receiver PLL is operated at the same frequency as the 2nd harmonic of the transmitter fundamental 28.6MHz. Prior to making any adjustments, the bias current to Pin 2 is set to 2.2mA.. When making the initial center frequency adjustment to the VCO trimmer cap (NE564 Pin 12, 13, 2-20pF) the fiber cable is disconnected. (a thermal stabilization time of 1 hour is recommended prior to any transmitter or receiver calibration adjustments.) With the link connected and a proper signal present at the input to the NE554 Pin 5, the PLL will lock onto and track the incoming wideband FM signal. The unwanted harmonic signals number one and three have not been filtered out in this design. The demodulated baseband video plus 10.7MHz signal then appears on the analog output port, Pin14. A wideband amplifier with low differential gain and phase error (NE5539) is used to boost the combined signal with the composite video level raised to 1V peak into 7W. The actual measured value of the video using a PAL color bar signal is 1VP-P on the output port. The NE554 output to the NE564 from Pin14 is 250mVP-P.

### 2.3 Components of the medium

An optical fiber (or fibre) is a glass or plastic fiber designed to guide light along its length by total internal reflection. Fiber optics is the branch of applied science and engineering concerned with such optical fibers. Optical fibers are widely used in fiber-optic communication, which permits digital data transmission over longer distances and at higher data rates than other forms of wired and wireless communications. They are also used to form sensors, and in a variety of other applications.

The operating principle of optical fibers applies to a number of variants including multi-mode optical fibers, single-mode optical fibers, graded-index optical fibers, and step-index optical fibers. Because of the physics of the optical fiber, special methods of splicing fibers and of connecting them to other equipment are needed. A variety of methods are used to manufacture optical fibers, and the fibers are also built into different kinds of cables depending on how they will be used. Thus below is showed the block diagram of the whole system after the transmitter and receiver is combined by an optical link.

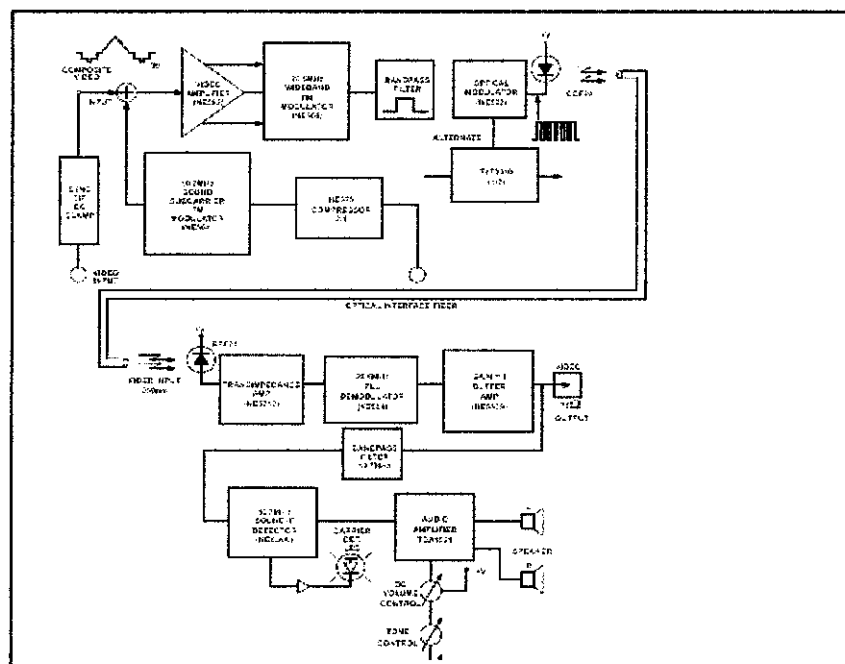


Figure 4 Block diagram of the optical transceiver

## CHAPTER 3

### METHODOLOGY

#### 3.1 Procedure Identification

The methodology that will be used in this project is the waterfall development-based where the operations moves forward from phase to phase.

The advantages of using this methodology are:

- Identify system requirements before start the development of each implementation phase begins.
- Minimize requirement changes as the project proceeds.

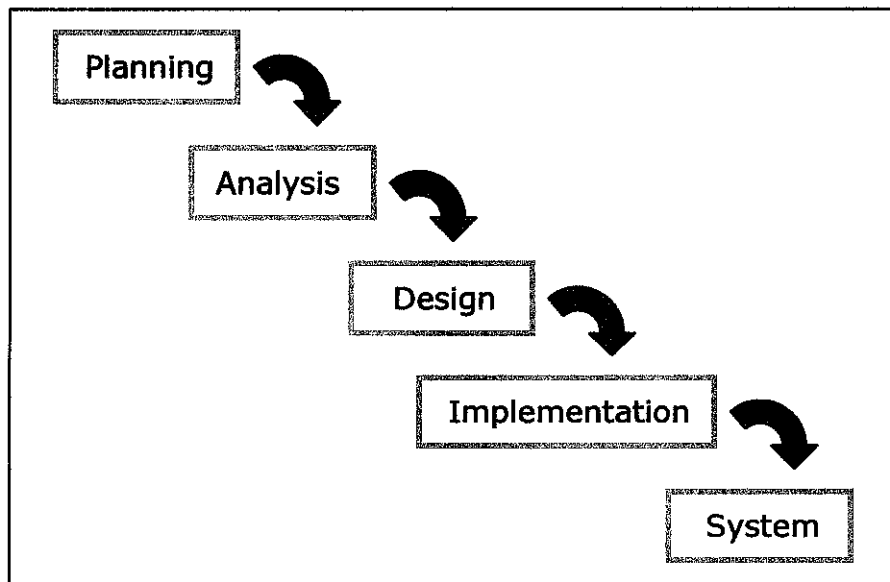


Figure 5 Project Development



### ***3.1.1 Planning Phase***

In the planning phase, several factors are chosen to set the application goals. These goals include anticipating and deciding on the target audience, purpose and objectives for the information. Research on the different kinds of systems eg; WDM, FDM, components and availability are done. Besides, all the stages involved in the completion of this project and possibility error that might be occurred has been pre planned.

### ***3.1.2 Analysis Phase***

In order to improve the application's quality, gathering and comparing about the application and its functionality was done. It is done to help in decision making to go through the process of planning, design and implementing. A study & thorough analysis on the different types of systems; pros and cons of each have been conducted.

### ***3.1.3 Design Phase***

For the design phase, the application's purposes, audience and objective is very important in implementing this project. No software is needed to complete this design. It is totally hardware based. A digital camera will be needed and a monitor as the input and output devices. It totally concentrates on the hardware completion of the transceiver. A few possible circuits to be carried out has been designed and tested and the finalized design was FDM.

### ***3.1.4 Implementation Phase***

The design has been implemented on a project board and PCB.

## **3.2 Testing**

The main testing devices that are used in this project are the spectrum analyzer and

oscilloscope. A monitor and a digital camera is needed as well.

## **CHAPTER 4**

### **RESULTS AND DISCUSSION**

#### **4.1 Results based on testing**

The design makes use of a very wideband VCO to generate an FM modulated carrier at 28.6MHz followed by a fast TTL LED driver to emit saturated 850nm light signals for entry in to the glass fiber. A PIN diode receiver is coupled to a 140MHz bandwidth transimpedance preamplifier for increasing the detected signal amplitude and then fed to a phase-locked loop demodulator for recovering the original modulation signals. The wideband FM sound subcarrier (150kHz deviation) is summed with baseband video at 10.7MHz and transmitted at a reduced level relative to the 3.58MHz color reference signal. Cross modulation between sound and picture information is minimized in this way. FM demodulation of the sound subcarrier is accomplished after passing through an IF gain block by a quadrature-type phase discriminator. The present sound circuit does not automatically frequency-lock to the transmitted subcarrier, but is fixed-tuned to 10.7MHz. A tracking PLL sound demodulator could be used to eliminate drift problems between transmitted sound subcarrier and the receiver in future designs.

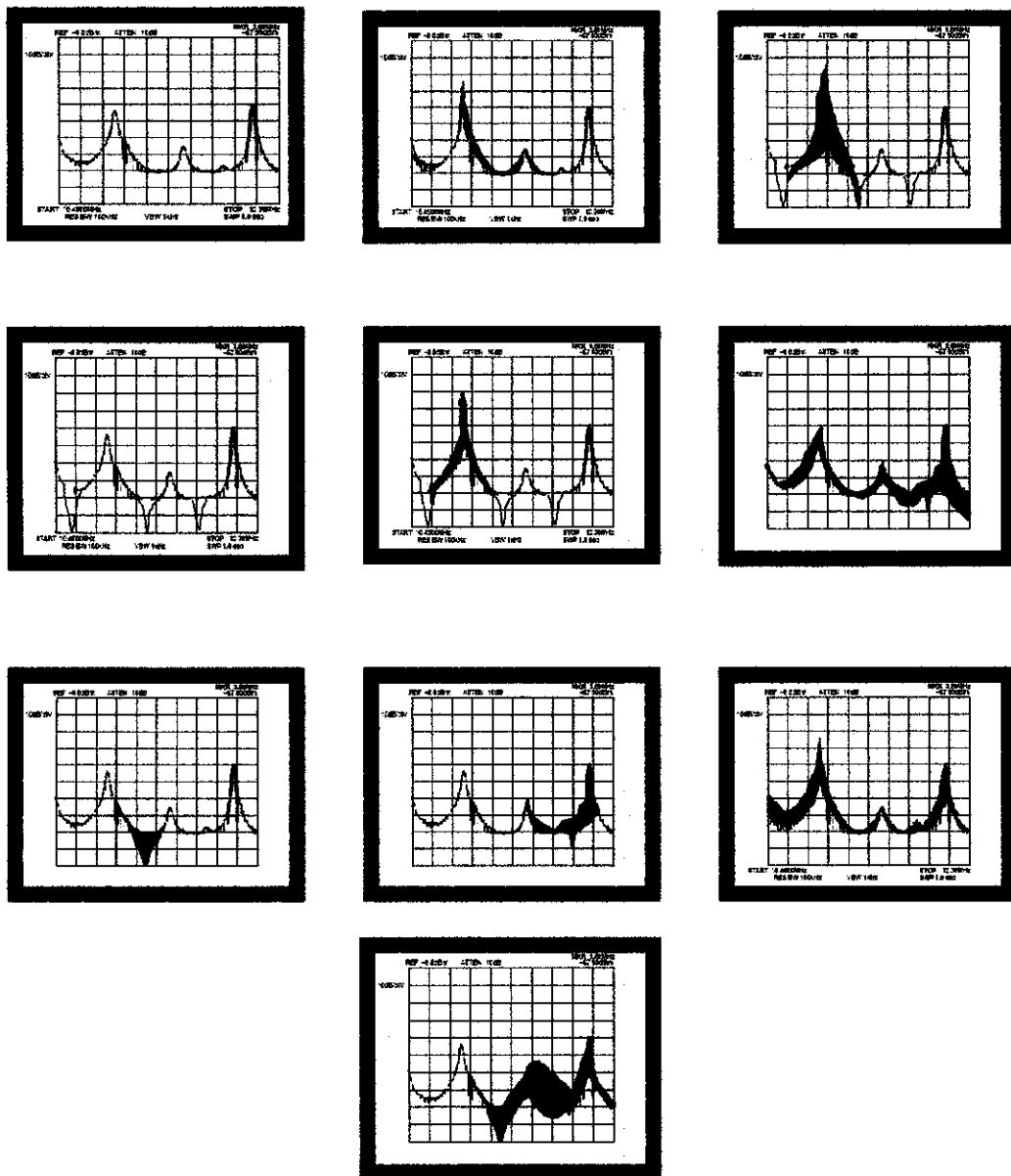


Figure 6 The types of NE952 Output Signal Video Plus 10.7Mhz Subcarrier

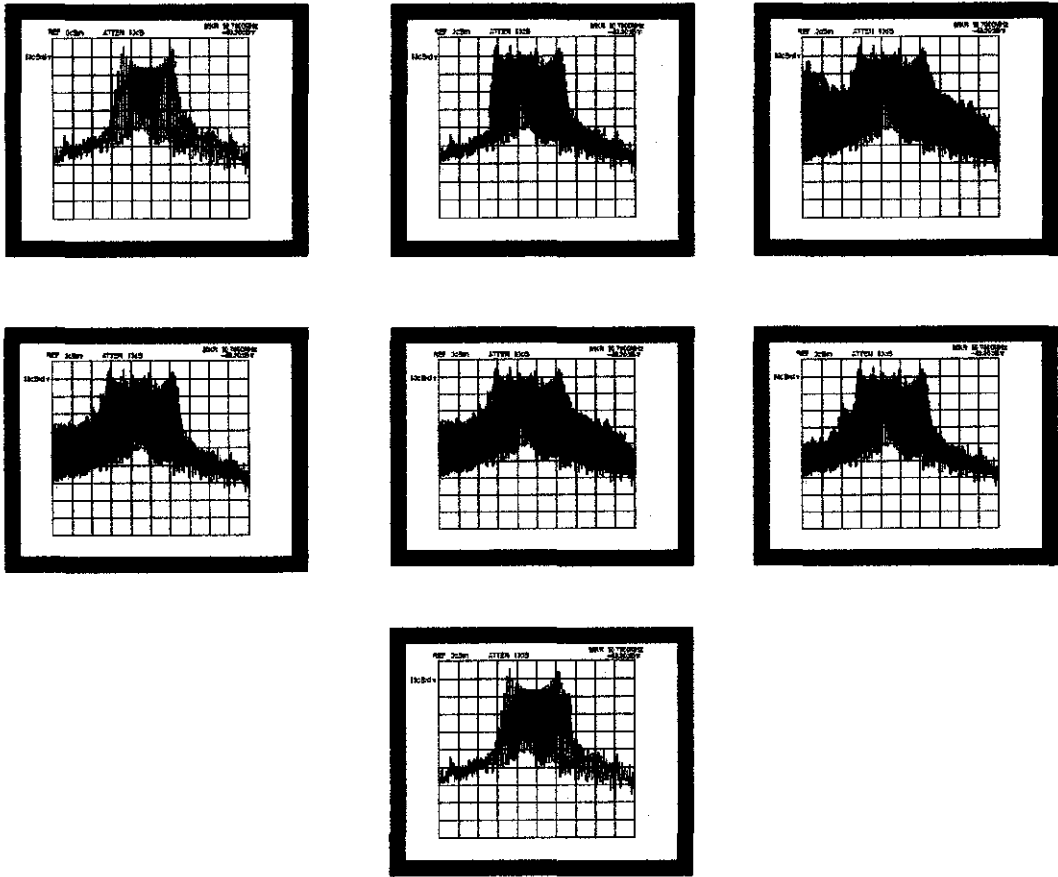


Figure 7 The types of 10.7MHz Subcarrier PLL Output with 1kHz Input

## **CHAPTER 5**

### **CONCLUSION AND RECOMMENDATION**

#### **5.1 Conclusion**

The system described is capable of transmitting single channel color video and sound transmission at 850nm with glass or plastic fiber optic cable of >2.5km. Signal transmission is of adequate quality for Industrial inspection, security and other applications of this limited nature. The most notable feature is its minimal cost. It is not meant to be used in broadcast quality environments. The next stage is to make improve and alter the system to attain greater stability and higher quality.

The choice between optical fiber and electrical (or "copper") transmission for a particular system is made based on a number of trade-offs. Optical fiber is generally chosen for systems with higher bandwidths or spanning longer distances than electrical cabling can provide.

The main benefits of fiber are its exceptionally low loss, allowing long distances between amplifiers or repeaters; and its inherently high data-carrying capacity, such that thousands of electrical links would be required to replace a single high bandwidth fiber. Another benefit of fiber is that even when run alongside each other for long distances, fiber cables experience effectively no crosstalk, in contrast to some types of electrical transmission lines.

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Because of these benefits of electrical transmission, optical communication is not common in short box-to-box, backplane, or chip-to-chip applications; however, optical systems on those scales have been demonstrated in the laboratory.

In certain situations fiber may be used even for short distance or low bandwidth applications, due to other important features:

- Immunity to electromagnetic interference, including nuclear electromagnetic pulses (although fiber can be damaged by alpha and beta radiation).
- High electrical resistance, making it safe to use near high-voltage equipment or between areas with different earth potentials.
- Lighter weight, important, for example, in aircraft.
- No sparks, important in flammable or explosive gas environments.
- Not electromagnetically radiating, and difficult to tap without disrupting the signal, important in high-security environments.
- Much smaller cable size - important where pathway is limited.

## **5.2 Improvement**

Suggested areas of improvement are:

1. The addition of bandpass filters to improve transmitter and receiver signal-to-noise;
2. Video sync tip or black level clamp with AGC at transmitter modulation input;
3. Addition of an AGC stage after the receiver transimpedance amplifier to improve optical path dynamic range.

## REFERENCES

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## **APPENDICES**

**APPENDIX A**  
**NE564 DATASHEET**

# Phase-locked loop

# NE/SE564

### DESCRIPTION

The NE/SE564 is a versatile, high guaranteed frequency phase-locked loop designed for operation up to 50MHz. As shown in the Block Diagram, the NE/SE564 consists of a VCO, limiter, phase comparator, and post detection processor.

### FEATURES

- Operation with single 5V supply
- TTL-compatible inputs and outputs
- Guaranteed operation to 50MHz
- External loop gain control
- Reduced carrier feedthrough
- No elaborate filtering needed in FSK applications
- Can be used as a modulator
- Variable loop gain (externally controlled)

### APPLICATIONS

- High speed modems
- FSK receivers and transmitters
- Frequency Synthesizers

### PIN CONFIGURATIONS

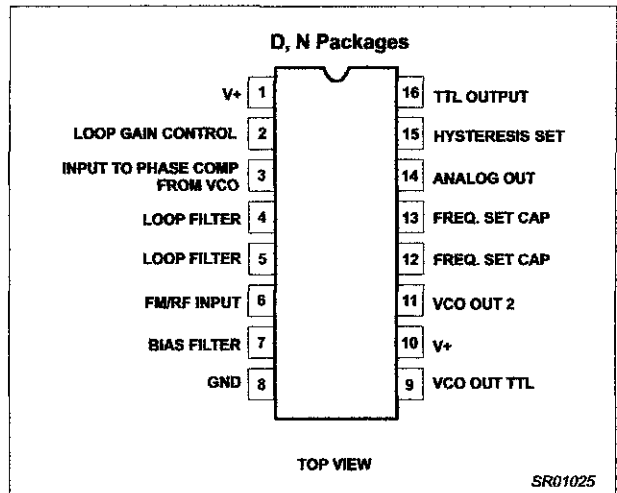


Figure 1. Pin Configuration

- Signal generators
- Various satcom/TV systems
- pin configuration

### ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline (SO) Package	0 to +70°C	NE564D	SOT109-1
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE564N	SOT38-4
16-Pin Plastic Dual In-Line Package (DIP)	-55 to +125°C	SE564N	SOT38-4

### BLOCK DIAGRAM

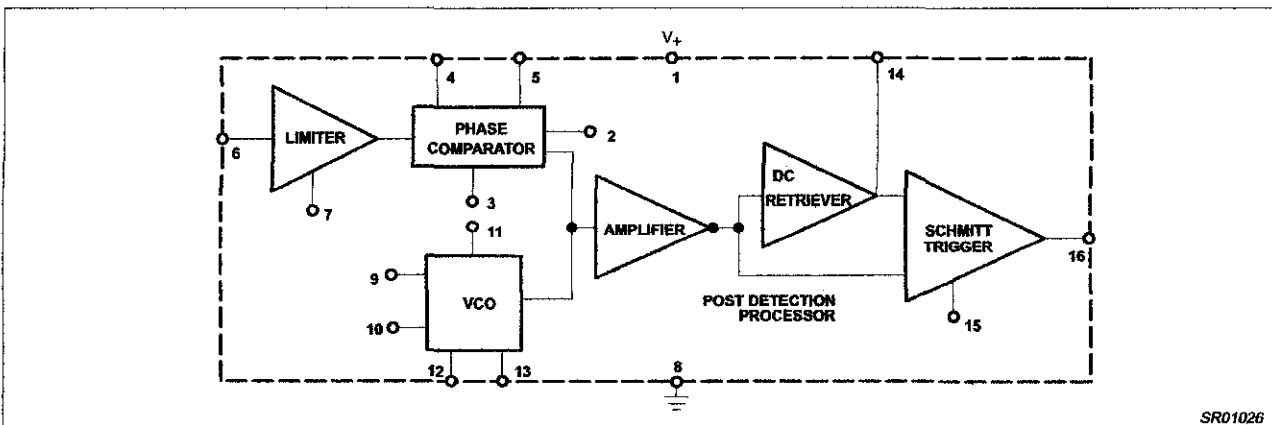


Figure 2. Block Diagram

## Phase-locked loop

NE/SE564

## ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V+	Supply voltage Pin 1 Pin 10	14 6	V V
I <sub>OUT</sub>	Sink Max (Pin 9) and sourcing (Pin 11)	11	mA
I <sub>BIAS</sub>	Bias current adjust pin (sinking)	1	mA
P <sub>D</sub>	Power dissipation	600	mW
T <sub>A</sub>	Operating ambient temperature NE SE	0 to +70 -55 to +125	°C °C
T <sub>STG</sub>	Storage temperature range	-65 to +150	°C

## NOTE:

Operation above 5V will require heatsinking of the case.

## DC AND AC ELECTRICAL CHARACTERISTICS

V<sub>CC</sub> = 5V; T<sub>A</sub> = 0 to 25°C; f<sub>O</sub> = 5MHz, I<sub>2</sub> = 400µA; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			LIMITS			UNITS
			SE564			NE564			
			MIN	TYP	MAX	MIN	TYP	MAX	
	Maximum VCO frequency	C <sub>1</sub> = 0 (stray)	50	65		45	60		MHz
	Lock range	Input ≥ 200mV <sub>RMS</sub> T <sub>A</sub> = 25°C T <sub>A</sub> = 125°C T <sub>A</sub> = -55°C T <sub>A</sub> = 0°C T <sub>A</sub> = 70°C	40 20 50	70 30 80		40	70 70 40		% of f <sub>O</sub>
	Capture range	Input ≥ 200mV <sub>RMS</sub> , R <sub>2</sub> = 27Ω	20	30		20	30		% of f <sub>O</sub>
	VCO frequency drift with temperature	f <sub>O</sub> = 5MHz, T <sub>A</sub> = -55°C to +125°C T <sub>A</sub> = 0 to +70°C = 0 to +70°C f <sub>O</sub> = 5MHz, T <sub>A</sub> = -55°C to +125°C T <sub>A</sub> = 0 to +70°C		500 300	1500 800		600 500		PPM/°C
	VCO free-running frequency	C <sub>1</sub> = 91pF R <sub>C</sub> = 100Ω "Internal"	4	5	6	3.5	5	6.5	MHz
	VCO frequency change with supply voltage	V <sub>CC</sub> = 4.5V to 5.5V		3	8		3	8	% of f <sub>O</sub>
	Demodulated output voltage	Modulation frequency: 1kHz f <sub>O</sub> = 5MHz, input deviation: 2%T = 25°C 1%T = 25°C 1%T = 0°C 1%T = -55°C 1%T = 70°C 1%T = 125°C	16 8 6 12	28 14 10 16		16 8	28 14 13 15		mV <sub>RMS</sub> mV <sub>RMS</sub> mV <sub>RMS</sub> mV <sub>RMS</sub> mV <sub>RMS</sub>
	Distortion	Deviation: 1% to 8%		1			1		%
S/N	Signal-to-noise ratio	Std. condition, 1% to 10% dev.		40			40		dB
	AM rejection	Std. condition, 30% AM		35			35		dB
	Demodulated output at operating voltage	Modulation frequency: 1kHz f <sub>O</sub> = 5MHz, input deviation: 1% V <sub>CC</sub> = 4.5V V <sub>CC</sub> = 5.5V	7 8	12 14		7 8	12 14		mV <sub>RMS</sub> mV <sub>RMS</sub>
I <sub>CC</sub>	Supply current	V <sub>CC</sub> = 5V I <sub>1</sub> , I <sub>10</sub>		45	60		45	60	mA
	Output "1" output leakage current "0" output voltage	V <sub>OUT</sub> = 5V, Pins 16, 9 I <sub>OUT</sub> = 2mA, Pins 16, 9 I <sub>OUT</sub> = 6mA, Pins 16, 9		1 0.3 0.4	20 0.6 0.8		1 0.3 0.4	20 0.6 0.8	µA V V

Phase-locked loop

NE/SE564

TYPICAL PERFORMANCE CHARACTERISTICS

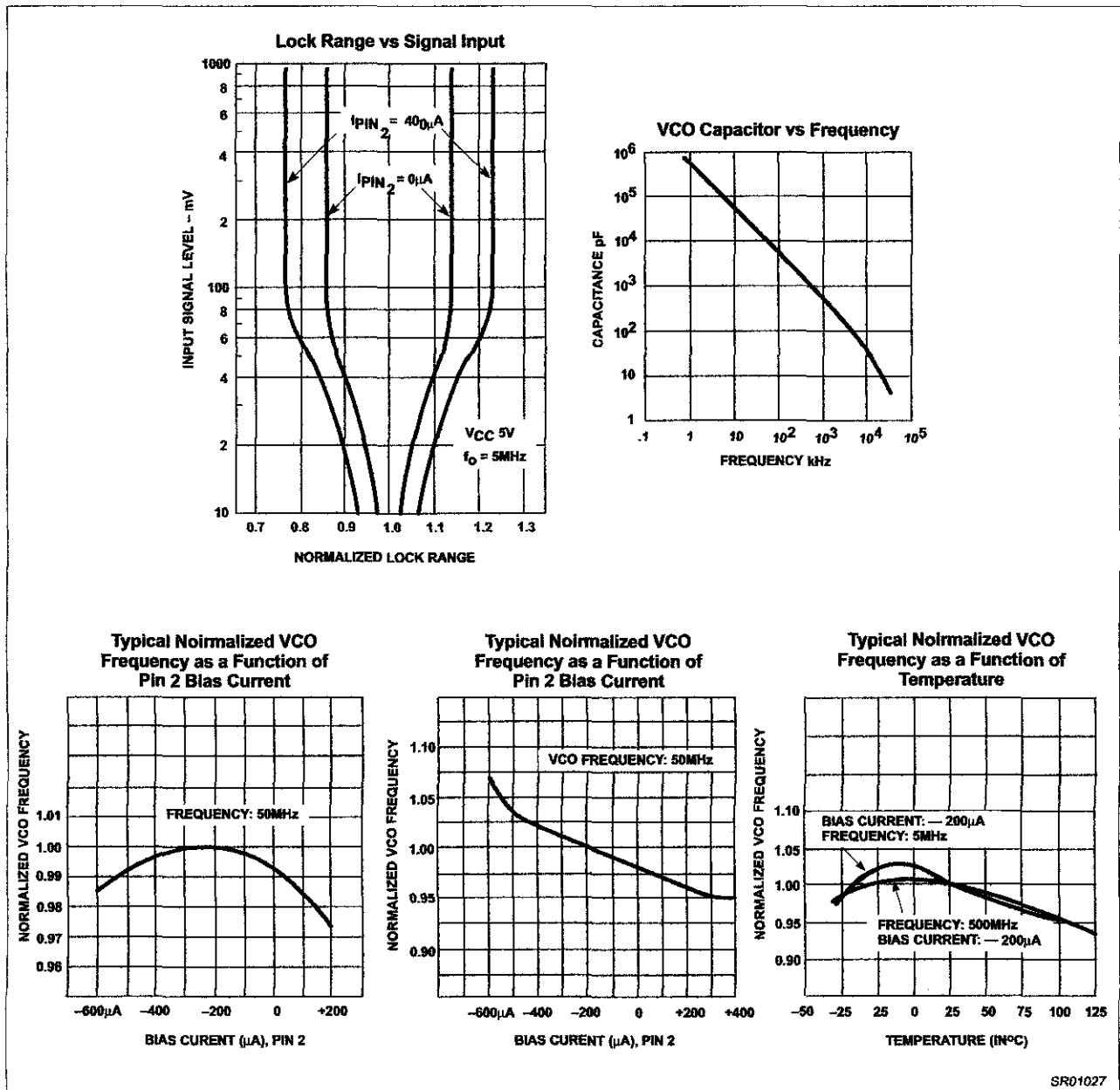


Figure 3. Typical Performance Characteristics

Phase-locked loop

NE/SE564

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

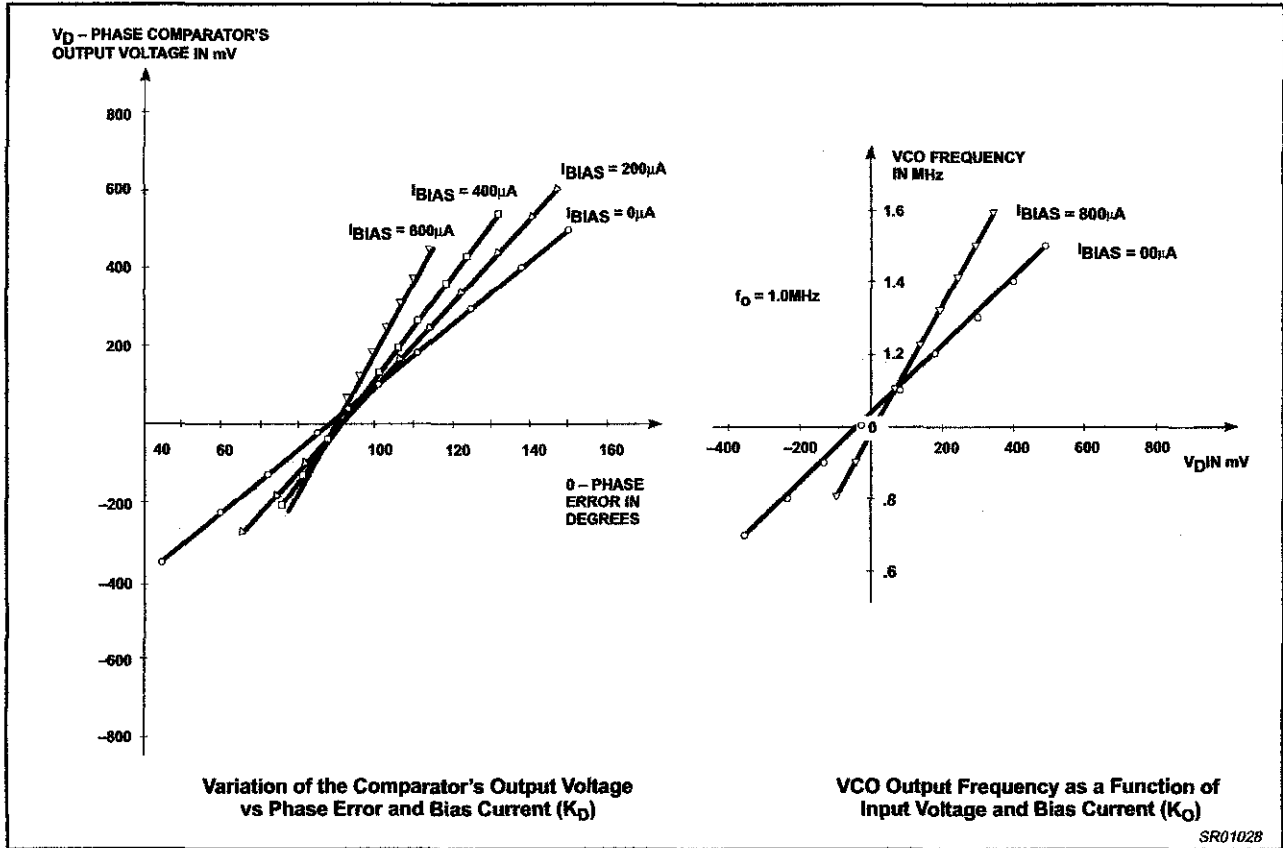


Figure 4. Typical Performance Characteristics (cont.)

TEST CIRCUIT

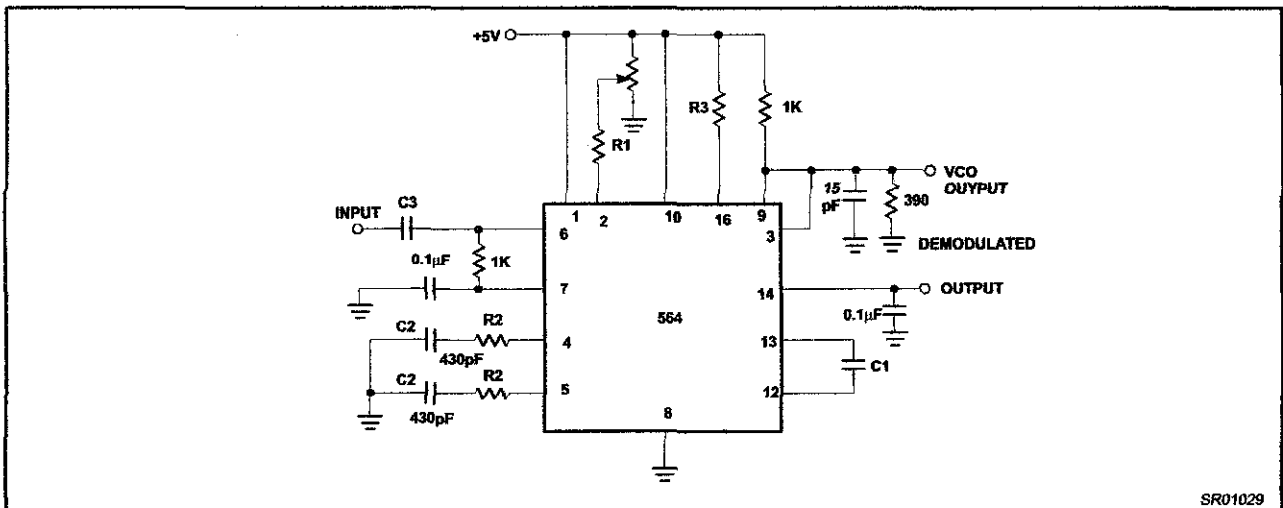


Figure 5. Test Circuit

## Phase-locked loop

NE/SE564

## FUNCTIONAL DESCRIPTION

**(Figure 6)**

The NE564 is a monolithic phase-locked loop with a post detection processor. The use of Schottky clamped transistors and optimized device geometries extends the frequency of operation to greater than 50MHz.

In addition to the classical PLL applications, the NE564 can be used as a modulator with a controllable frequency deviation.

The output of the PLL can be written as shown in the following equation:

$$V_O = \frac{(f_{IN} - f_O)}{K_{VCO}} \quad (1)$$

$K_{VCO}$  = conversion gain of the VCO

$f_{IN}$  = frequency of the input signal

$f_O$  = free-running frequency of the VCO

The process of recovering FSK signals involves the conversion of the PLL output into logic compatible signals. For high data rates, a considerable amount of carrier will be present at the output of the PLL due to the wideband nature of the loop filter. To avoid the use of complicated filters, a comparator with hysteresis or Schmitt trigger is required. With the conversion gain of the VCO fixed, the output voltage as given by Equation 1 varies according to the frequency deviation of  $f_{IN}$  from  $f_O$ . Since this differs from system to system, it is necessary that the hysteresis of the Schmitt trigger be capable of being changed, so that it can be optimized for a particular system. This is accomplished in the 564 by varying the voltage at Pin 15 which results in a change of the hysteresis of the Schmitt trigger.

For FSK signals, an important factor to be considered is the drift in the free-running frequency of the VCO itself. If this changes due to temperature, according to Equation 1 it will lead to a change in the DC levels of the PLL output, and consequently to errors in the digital output signal. This is especially true for narrowband signals where the deviation in  $f_{IN}$  itself may be less than the change in  $f_O$  due to temperature. This effect can be eliminated if the DC or average value of the signal is retrieved and used as the reference to the comparator. In this manner, variations in the DC levels of the PLL output do not affect the FSK output.

**VCO Section**

Due to its inherent high-frequency performance, an emitter-coupled oscillator is used in the VCO. In the circuit, shown in the equivalent schematic, transistors Q21 and Q23 with current sources Q25 - Q26 form the basic oscillator. The approximate free-running frequency of the oscillator is shown in the following equation:

$$f_O \cong \frac{1}{22 R_C (C_1 + C_S)} \quad (2)$$

$R_C = R_{19} = R_{20} = 100\Omega$  (INTERNAL)

$C_1$  = external frequency setting capacitor

$C_S$  = stray capacitance

Variation of  $V_D$  (phase detector output voltage) changes the frequency of the oscillator. As indicated by Equation 2, the frequency of the oscillator has a negative temperature coefficient due to the monolithic resistor. To compensate for this, a current  $I_R$  with negative temperature coefficient is introduced to achieve a low frequency drift with temperature.

**Phase Comparator Section**

The phase detection processor consists of a doubled-balanced modulator with a limiter amplifier to improve AM rejection. Schottky-clamped vertical PNPs are used to obtain TTL level inputs. The loop gain can be varied by changing the current in  $Q_4$  and  $Q_{15}$  which effectively changes the gain of the differential amplifiers. This can be accomplished by introducing a current at Pin 2.

**Post Detection Processor Section**

The post detection processor consists of a unity gain transconductance amplifier and comparator. The amplifier can be used as a DC retriever for demodulation of FSK signals, and as a post detection filter for linear FM demodulation. The comparator has adjustable hysteresis so that phase jitter in the output signal can be eliminated.

As shown in the equivalent schematic, the DC retriever is formed by the transconductance amplifier  $Q_{42} - Q_{43}$  together with an external capacitor which is connected at the amplifier output (Pin 14). This forms an integrator whose output voltage is shown in the following equation:

$$V_O = \frac{g_M}{C_2} \int V_{IN} dt \quad (3)$$

$g_M$  = transconductance of the amplifier

$C_2$  = capacitor at the output (Pin 14)

$V_{IN}$  = signal voltage at amplifier input

With proper selection of  $C_2$ , the integrator time constant can be varied so that the output voltage is the DC or average value of the input signal for use in FSK, or as a post detection filter in linear demodulation.

The comparator with hysteresis is made up of  $Q_{49} - Q_{50}$  with positive feedback being provided by  $Q_{47} - Q_{48}$ . The hysteresis is varied by changing the current in  $Q_{52}$  with a resulting variation in the loop gain of the comparator. This method of hysteresis control, which is a DC control, provides symmetric variation around the nominal value.

**Design Formula**

The free-running frequency of the VCO is shown by the following equation:

$$f_O \cong \frac{1}{22 R_C (C_1 + C_S)} \quad (4)$$

$R_C = 100\Omega$

$C_1$  = external cap in farads

$C_S$  = stray capacitance

The loop filter diagram shown is explained by the following equation:

$$f_S = \frac{1}{1 + sRC_3} \text{ (First Order)} \quad (5)$$

$R = R_{12} = R_{13} = 1.3k\Omega$  (Internal)\*

By adding capacitors to Pins 4 and 5, a pole is added to the loop transfer at

$$\omega = \frac{1}{RC_3}$$

**NOTE:**  
\*Refer to Figure 6.

Phase-locked loop

NE/SE564

EQUIVALENT SCHEMATIC

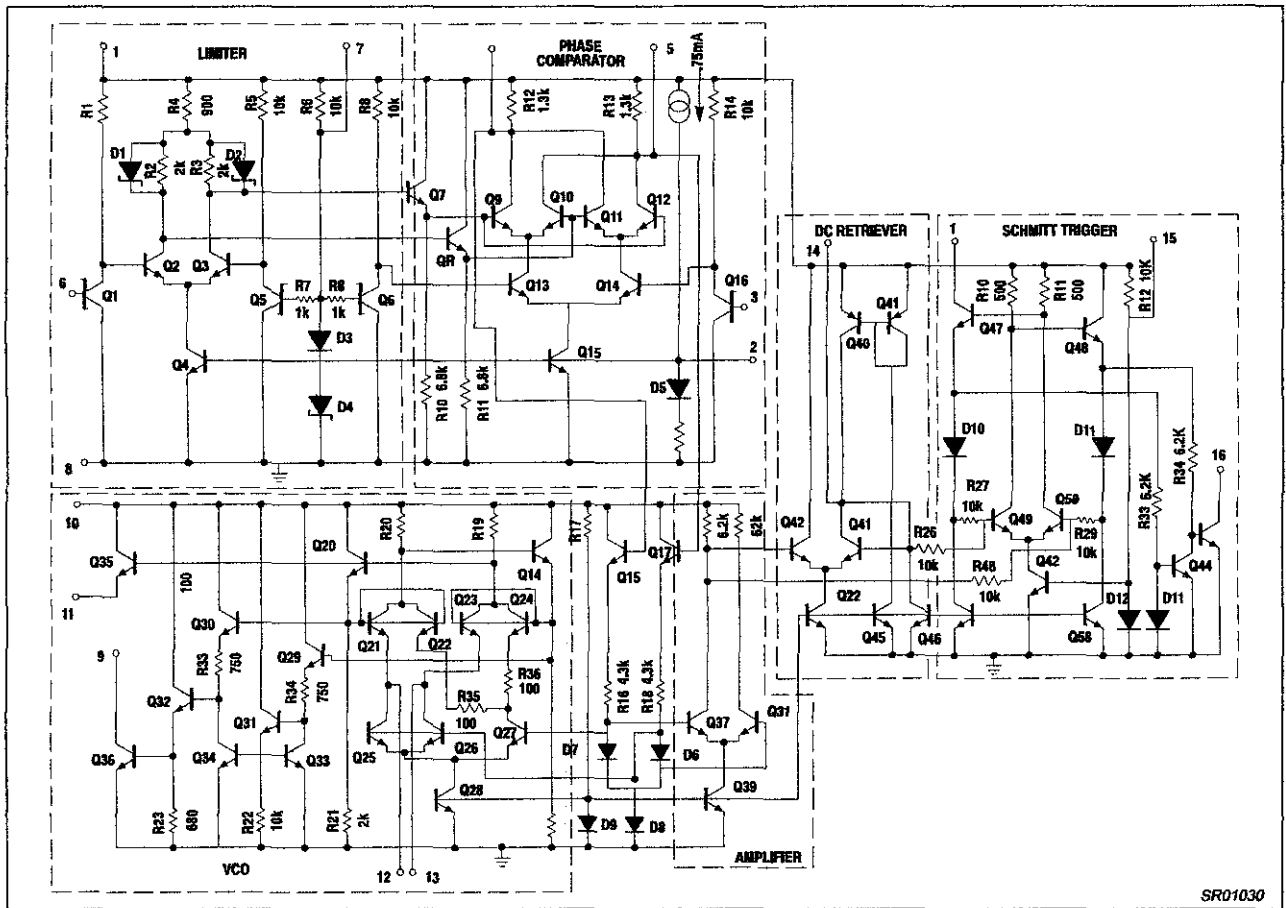


Figure 6. Equivalent Schematic

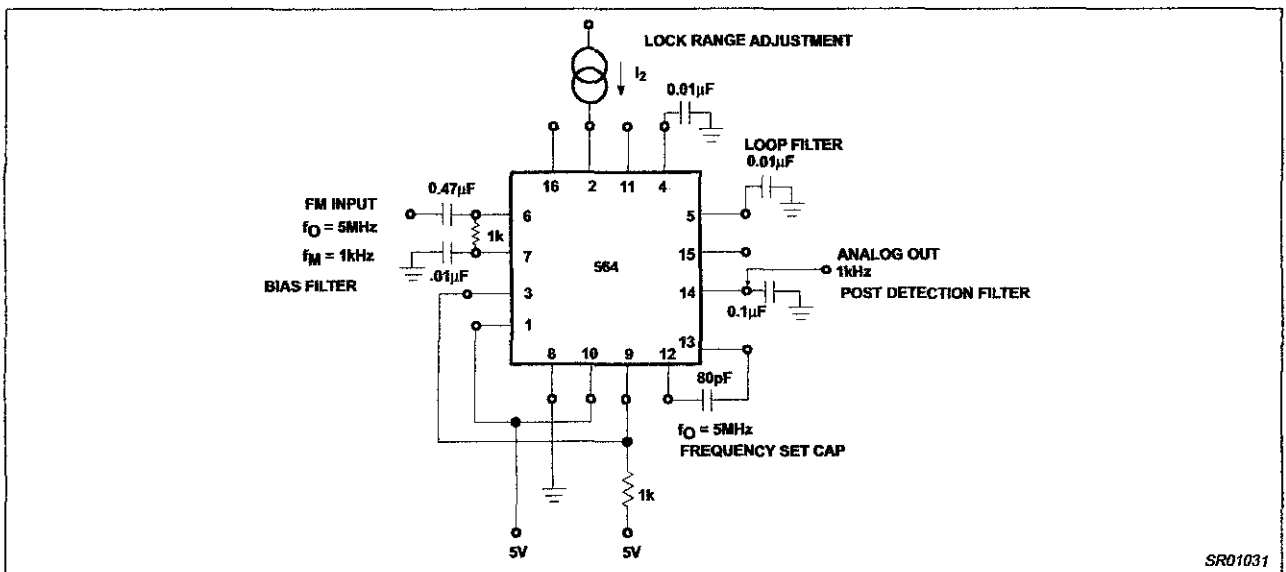


Figure 7. FM Demodulator at 5V



# Phase-locked loop

# NE/SE564

## APPLICATIONS

### FM Demodulator

The NE564 can be used as an FM demodulator. The connections for operation at 5V and 12V are shown in Figures 7 and 8, respectively. The input signal is AC coupled with the output signal being extracted at Pin 14. Loop filtering is provided by the capacitors at Pins 4 and 5 with additional filtering being provided by the capacitor at Pin 14. Since the conversion gain of the VCO is not very high, to obtain sufficient demodulated output signal the frequency deviation in the input signal should be 1% or higher.

### Modulation Techniques

The NE564 phase-locked loop can be modulated at either the loop filter ports (Pins 4 and 5) or the input port (Pin 6) as shown in Figure 9. The approximate modulation frequency can be determined from the frequency conversion gain curve shown in Figure 10. This curve will be appropriate for signals injected into Pins 4 and 5 as shown in Figure 9.

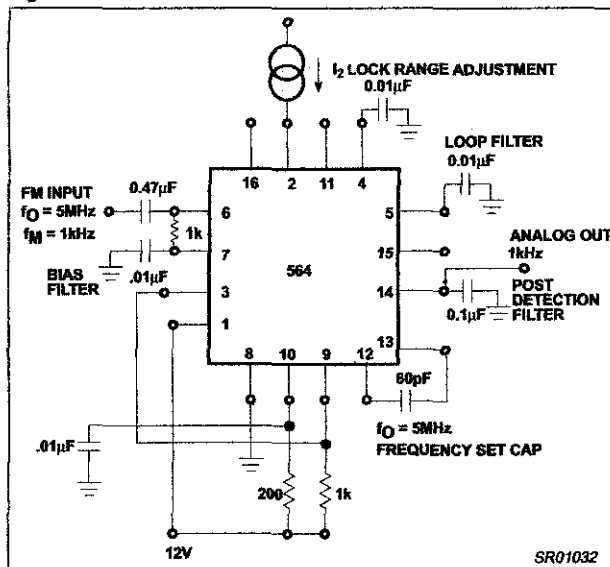


Figure 8. FM Demodulator at 12V

### FSK Demodulation

The 564 PLL is particularly attractive for FSK demodulation since it contains an internal voltage comparator and VCO which have TTL compatible inputs and outputs, and it can operate from a single 5V power supply. Demodulated DC voltages associated with the mark and space frequencies are recovered with a single external capacitor in a DC retriever without utilizing extensive filtering networks. An internal comparator, acting as a Schmitt trigger with an adjustable hysteresis, shapes the demodulated voltages into compatible TTL output levels. The high-frequency design of the 564 enables it to demodulate FSK at high data rates in excess of 1.0M baud.

Figure 10 shows a high-frequency FSK decoder designed for input frequency deviations of  $\pm 1.0\text{MHz}$  centered around a free-running frequency of 10.8MHz. the value of the timing capacitance required was estimated from Figure 8 to be approximately 40pF. A trimmer capacitor was added to fine tune  $f_0$  10.8MHz.

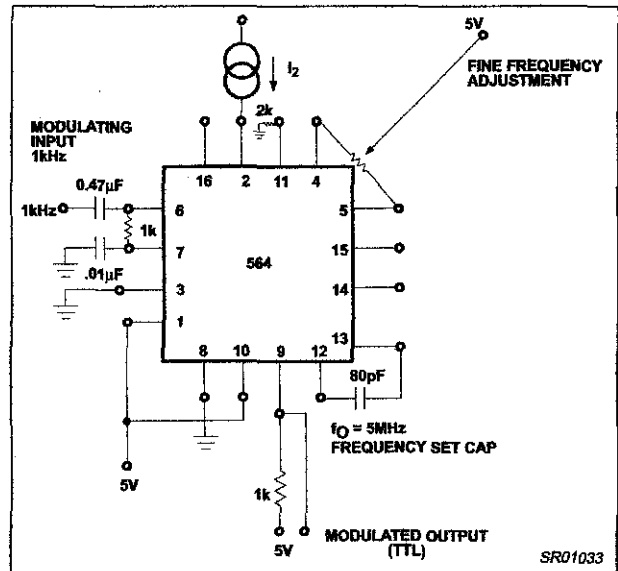


Figure 9. Modulator

The lock range graph indicates that the  $\pm 1.0\text{MHz}$  frequency deviations will be within the lock range for input signal levels greater than approximately 50mV with zero Pin 2 bias current. (While strictly this figure is appropriate only for 50MHz, it can be used as a guide for lock range estimates at other  $f_0$  frequencies).

The hysteresis was adjusted experimentally via the 10kΩ potentiometer and 2kΩ bias arrangement to give the waveshape shown in Figure 12 for 20k, 500k, 2M baud rates with square wave FSK modulation. Note the magnitude and phase relationships of the phase comparators' output voltages with respect to each other and to the FSK output. The high-frequency sum components of the input and VCO frequency also are viable as noise on the phase comparator's outputs.

## OUTLINE OF SETUP PROCEDURE

1. Determine operating frequency of the VCO:  $f_0 = N$  in feedback loop, then  $f_0 = N \times f_{IN}$ .

2. Calculate value of the VCO frequency set capacitor:

$$C_0 \cong \frac{1}{2200 f_0}$$

3. Set  $I_2$  (current sinking into Pin 2) for  $\cong 100\mu\text{A}$ . After operation is obtained, this value may be adjusted for best dynamic behavior, and replace with fixed resistor value of  $R_2 = \frac{V_{CC} - 1.3V}{I_{B2}}$ .

4. Check VCO output frequency with digital counter at Pin 9 of device (loop open, VCO to  $\phi$  det.). Adjust  $C_0$  trim or frequency adj. Pins 4 - 5 for exact center frequency, if needed.

5. Close loop and inject input signal to Pin 6. Monitor Pins 3 and 6 with two-channel scope. Lock should occur with  $\Delta\phi_{3-6}$  equal to  $90^\circ$  (phase error).

# Phase-locked loop

# NE/SE564

- 6. If pulsed burst or ramp frequency is used for input signal, special loop filter design may be required in place of simple single capacitor filter on Pins 4 and 5. (See PLL application section)
- 7. The input signal to Pin 6 and the VCO feedback signal to Pin 3 must have a duty cycle of 50% for proper operation of the phase detector. Due to the nature of a balanced mixer if signals are not

50% in duty cycle, DC offsets will occur in the loop which tend to create an artificial or biased VCO.

- 8. For multiplier circuits where phase jitter is a problem, loop filter capacitors may be increased to a value of 10 - 50 $\mu$ F on Pins 4, 5. Also, careful supply decoupling may be necessary. This includes the counter chain  $V_{CC}$  lines.

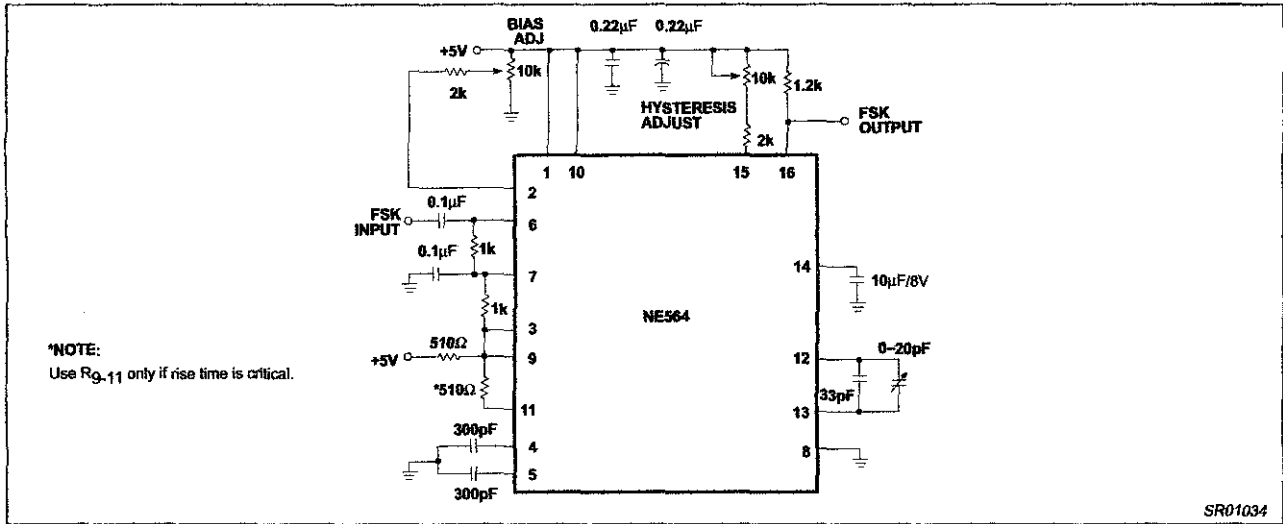


Figure 10. 10.8MHz FSK Decoder Using the 564

Phase-locked loop

NE/SE564

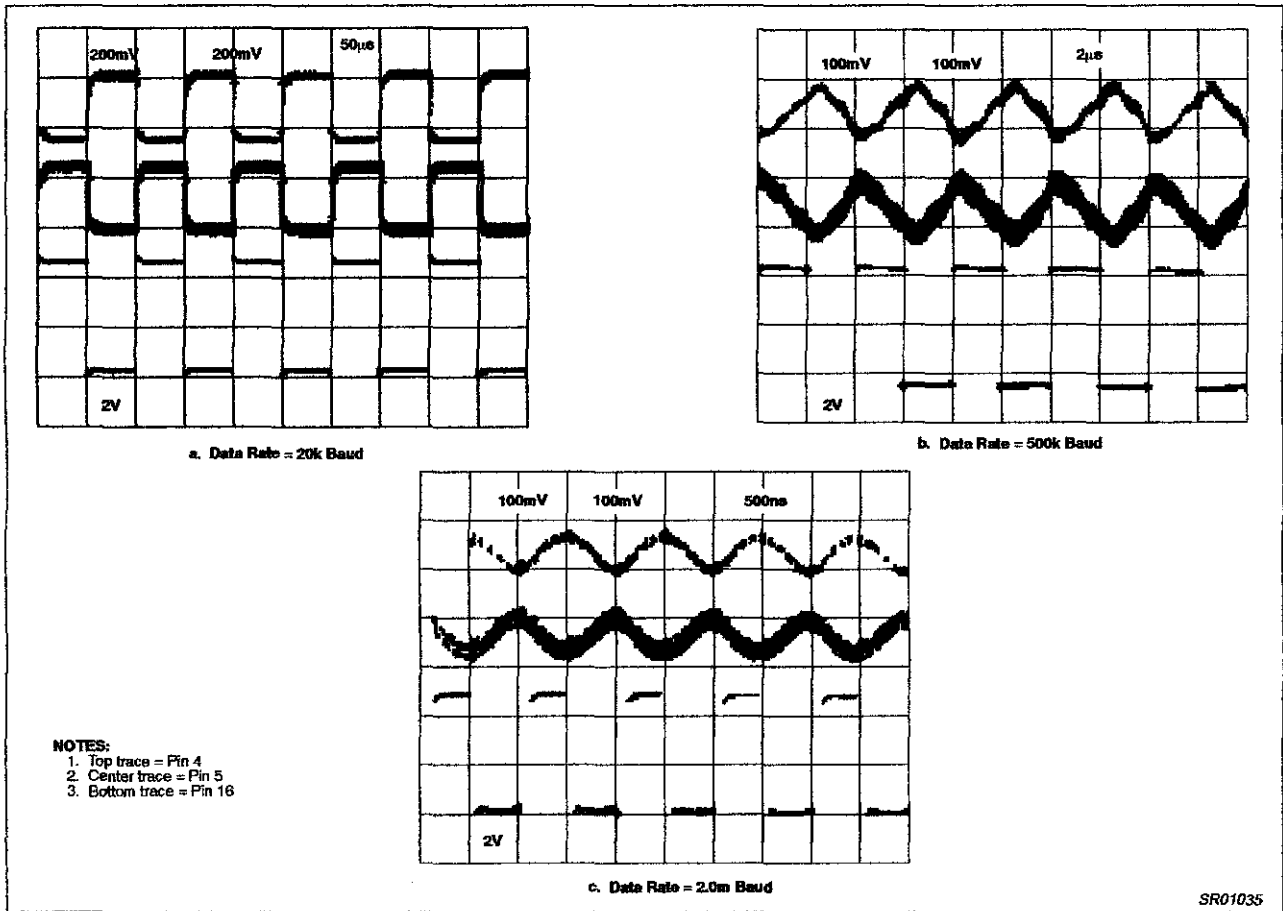


Figure 11. Phase Comparator (Pins 4 and 5) and FSK (Pin 16) Outputs

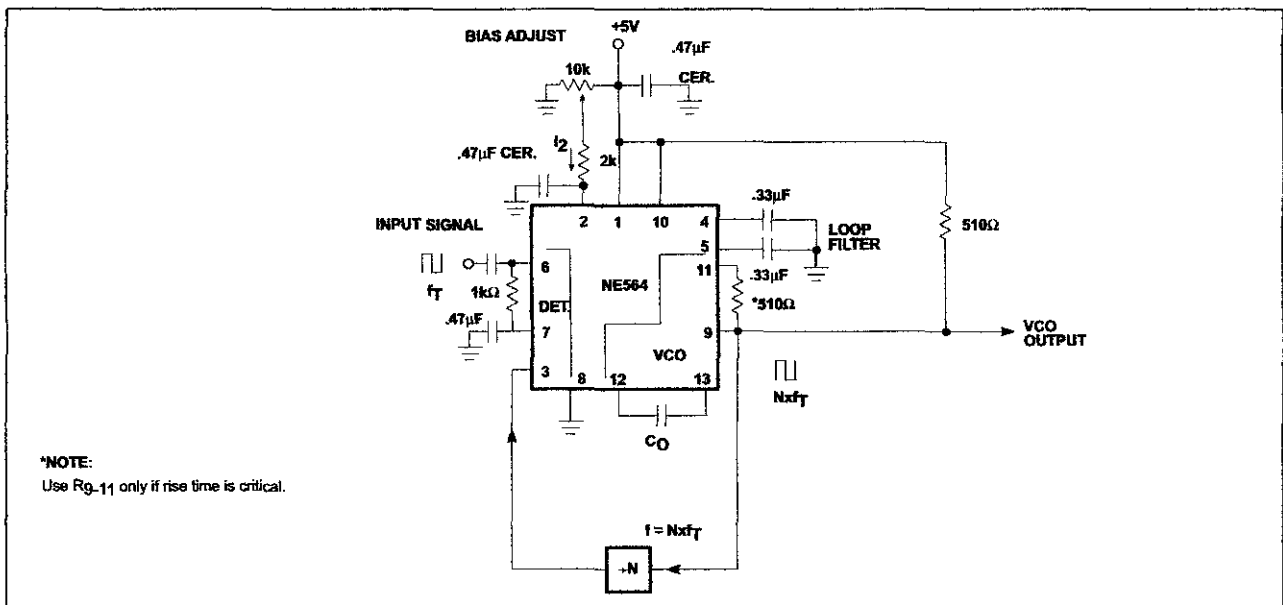


Figure 12. NE564 Phase-Locked Frequency Multiplier

**This datasheet has been download from:**

[www.datasheetcatalog.com](http://www.datasheetcatalog.com)

**Datasheets for electronics components.**

**APPENDIX B**  
**NE5539 DATASHEET**

### FEATURES

Improved Replacement for Signetics SE/NE5539

### AC PERFORMANCE

Gain Bandwidth Product: 1.4 GHz typ

Unity Gain Bandwidth: 220 MHz typ

High Slew Rate: 600 V/ $\mu$ s typ

Full Power Response: 82 MHz typ

Open-Loop Gain: 47 dB min, 52 dB typ

### DC PERFORMANCE

All Guaranteed DC Specifications Are 100% Tested  
For Each Device Over Its Full Temperature  
Range - For All Grades and Packages

$V_{OS}$ : 5 mV max Over Full Temperature Range  
(AD5539S)

$I_B$ : 20  $\mu$ A max (AD5539J)

CMRR: 70 dB min, 85 dB typ

PSRR: 100  $\mu$ V/V typ

MIL-STD-883B Parts Available

### PRODUCT DESCRIPTION

The AD5539 is an ultrahigh frequency operational amplifier designed specifically for use in video circuits and RF amplifiers. Requiring no external compensation for gains greater than 5, it may be operated at lower gains with the addition of external compensation.

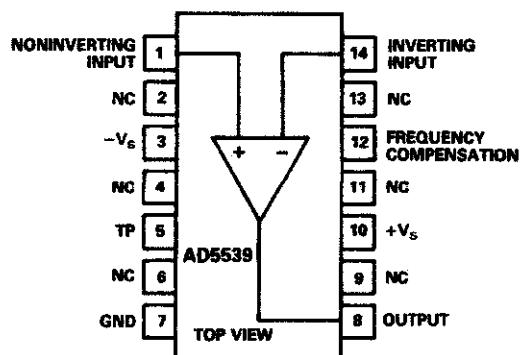
As a superior replacement for the Signetics NE/SE5539, each AD5539 is 100% dc tested to meet all of its guaranteed dc specifications over the full temperature range of the device.

The high slew rate and wide bandwidth of the AD5539 provide low cost solutions to many otherwise complex and expensive high frequency circuit design problems.

The AD5539 is available specified to operate over either the commercial (AD5539JN/JQ) or military (AD5539SQ) temperature range. The commercial grade is available either in 14-pin plastic or cerdip packages. The military version is supplied in the cerdip package. Chip versions are also available.

### CONNECTION DIAGRAM

Plastic DIP (N) Package  
or Cerdip (Q) Package



### PRODUCT HIGHLIGHTS

1. All guaranteed dc specifications are 100% tested.
2. The AD5539 drives 50  $\Omega$  and 75  $\Omega$  loads directly.
3. Input voltage noise is less than 4  $nV\sqrt{Hz}$ .
4. Low cost RF and video speed performance.
5.  $\pm 2$  volt output range into a 150  $\Omega$  load.
6. Low cost.
7. Chips available.

### REV. B

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

Parameter	AD5539J			AD5539S			Units
	Min	Typ	Max	Min	Typ	Max	
<b>OUTPUT CHARACTERISTICS</b>							
Positive Output Swing							
$R_L = 150 \Omega^3$	+2.3	+2.8		+2.3	+2.8		V
$R_L = 2 \text{ k}\Omega$	+2.3	+3.3		+2.5	+3.3		V
$T_{\text{MIN}}$ to $T_{\text{MAX}}$ with $R_L = 2 \text{ k}\Omega$	+2.3			+2.3			V
Negative Output Swing							
$R_L = 150 \Omega^3$		-2.2	-1.7		-2.2	-1.7	V
$R_L = 2 \text{ k}\Omega$		-2.9	-1.7		-2.9	-2.0	V
$T_{\text{MIN}}$ to $T_{\text{MAX}}$ with $R_L = 2 \text{ k}\Omega$			-1.5			-1.5	V
<b>POWER SUPPLY (No Load, No Resistor to <math>-V_S</math>)</b>							
Rated Performance		$\pm 8$			$\pm 8$		V
Operating Range	$\pm 4.5$		$\pm 10$	$\pm 4.5$		$\pm 10$	V
Quiescent Current							
Initial $I_{\text{CC}+}$		14	<b>18</b>		14	<b>17</b>	mA
$T_{\text{MIN}}$ to $T_{\text{MAX}}$			<b>20</b>			<b>18</b>	mA
Initial $I_{\text{CC}-}$		11	<b>15</b>		11	<b>14</b>	mA
$T_{\text{MIN}}$ to $T_{\text{MAX}}$			<b>17</b>			<b>15</b>	mA
<b>PSRR</b>							
Initial		100	<b>1000</b>		100	<b>1000</b>	$\mu\text{V/V}$
$T_{\text{MIN}}$ to $T_{\text{MAX}}$			<b>2000</b>			<b>2000</b>	$\mu\text{V/V}$
<b>TEMPERATURE RANGE</b>							
Operating, Rated Performance							
Commercial (0°C to +70°C)		AD5539JN, AD5539JQ			AD5539SQ		
Military (-55°C to +125°C)							
<b>PACKAGE OPTIONS</b>							
Plastic (N-14)		AD5539JN			AD5539SQ, AD5539SQ/883B		
Cerdip (Q-14)		AD5539JQ					
J and S Grade Chips Available							

## NOTES

<sup>1</sup>Input Offset Voltage specifications are guaranteed after 5 minutes of operation at  $T_A = +25^\circ\text{C}$ .

<sup>2</sup>Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at  $T_A = +25^\circ\text{C}$ .

<sup>3</sup> $R_X = 470 \Omega$  to  $-V_S$ .

<sup>4</sup>Externally compensated.

<sup>5</sup>Defined as voltage between inputs, such that neither exceeds +2.5 V, -5.0 V from ground.

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

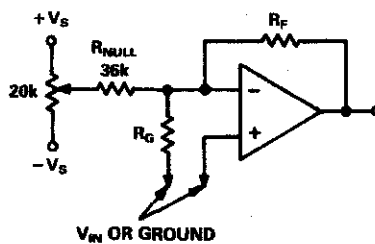
# D5539

## ABSOLUTE MAXIMUM RATINGS\*

Supply Voltage	±10 V
Internal Power Dissipation	550 mW
Input Voltage	+2.5 V, -5.0 V
Differential Input Voltage	0.25 V
Storage Temperature Range (Q)	-65°C to +150°C
Storage Temperature Range (N)	-65°C to +125°C
Operating Temperature Range	
AD5539JN	0°C to +70°C
AD5539JQ	0°C to +70°C
AD5539SQ	-55°C to +125°C
Lead Temperature Range (Soldering 60 Seconds)	+300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## OFFSET NULL CONFIGURATION



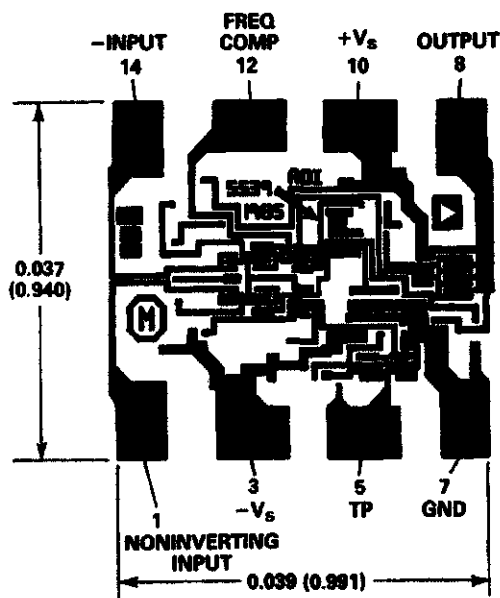
$$\text{OUTPUT NULL RANGE} \cong +V_s \left( \frac{R_F}{R_{NULL}} \right) \text{ TO } -V_s \left( \frac{R_F}{R_{NULL}} \right)$$

OFFSET NULL CONFIGURATION

## METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).

Contact factory for latest dimensions.



## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5539 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.





# Typical Characteristics—AD5539

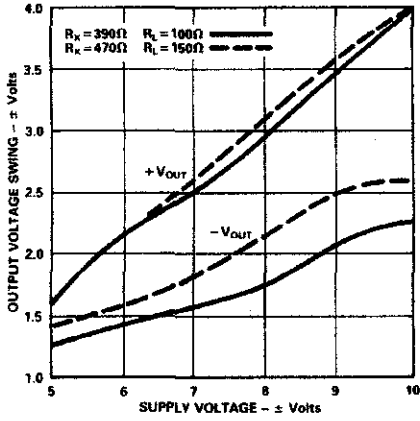


Figure 1. Output Voltage Swing vs. Supply Voltage

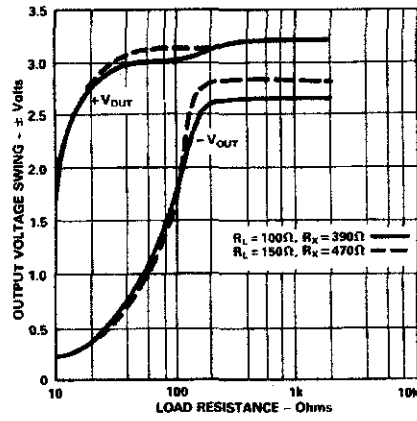


Figure 2. Output Voltage Swing vs. Load Resistance

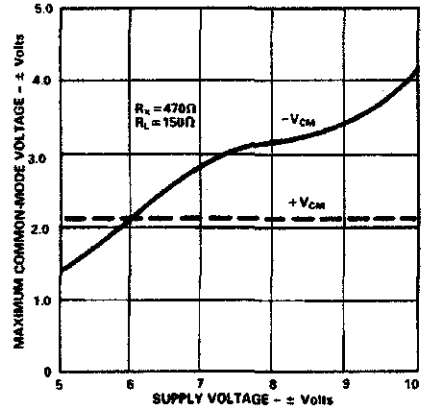


Figure 3. Maximum Common-Mode Voltage vs. Supply Voltage

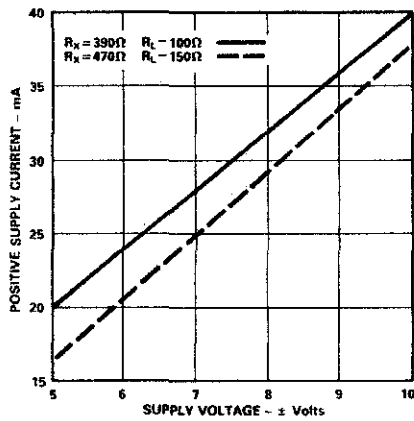


Figure 4. Positive Supply Current vs. Supply Voltage

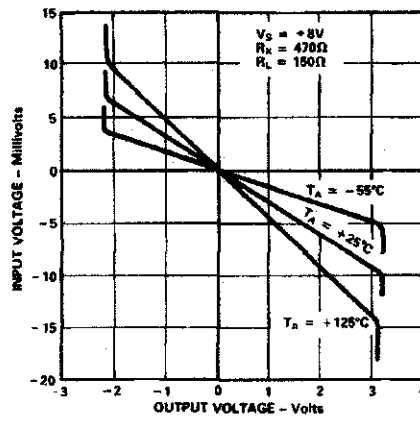


Figure 5. Input Voltage vs. Output Voltage for Various Temperatures

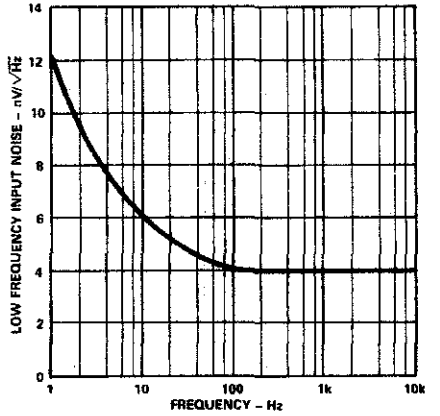


Figure 6. Low Frequency Input Noise vs. Frequency

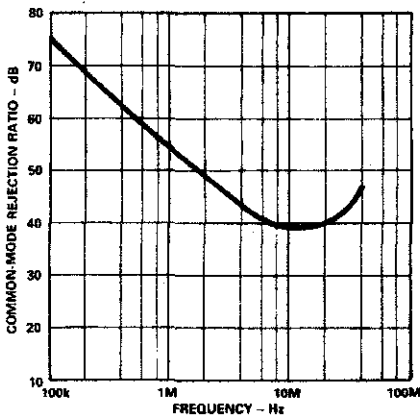


Figure 7. Common-Mode Rejection Ratio vs. Frequency

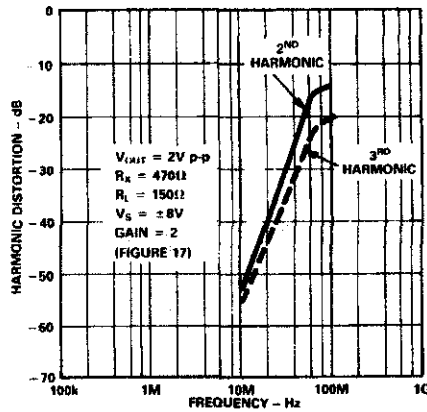


Figure 8. Harmonic Distortion vs. Frequency - Low Gain

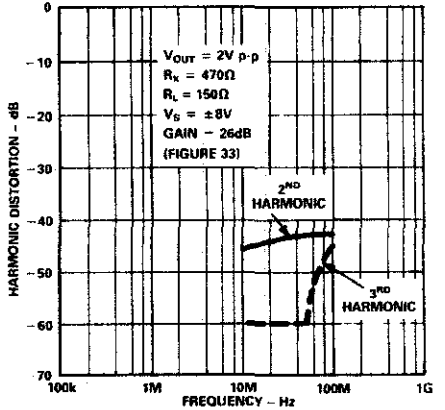


Figure 9. Harmonic Distortion vs. Frequency - High Gain

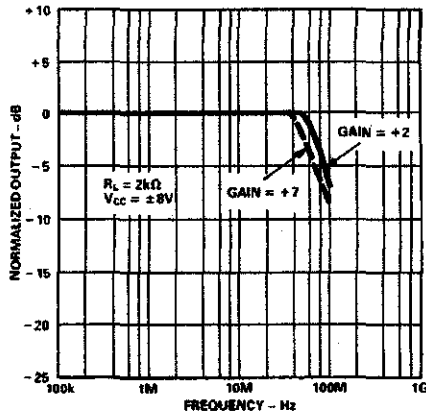


Figure 10. Full Power Response

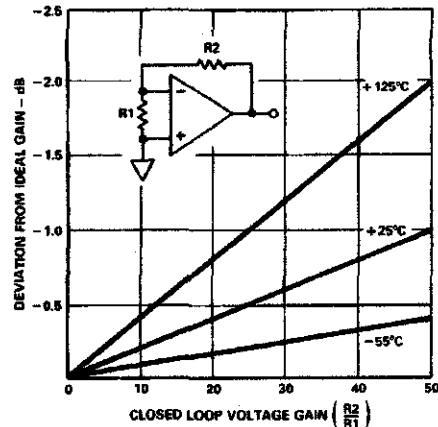


Figure 11. Deviation from Ideal Gain vs. Closed-Loop Voltage Gain

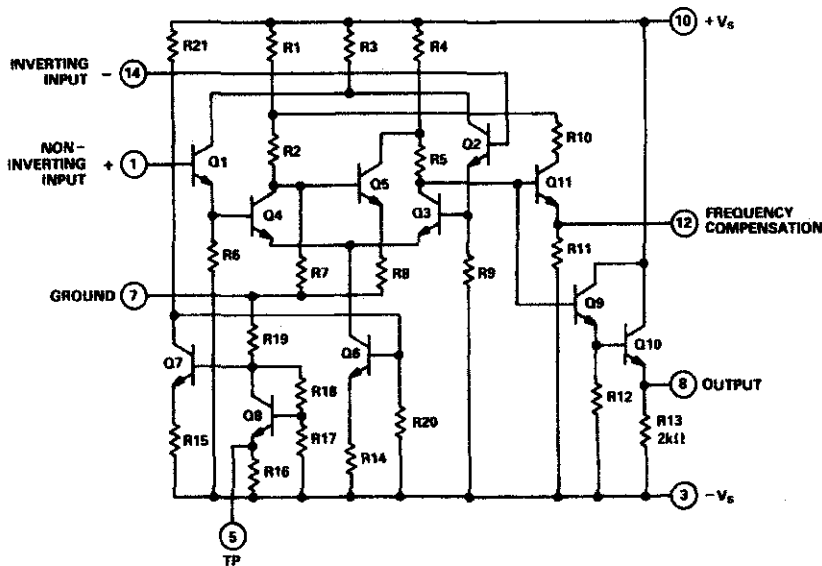


Figure 12. AD5539 Circuit

**FUNCTIONAL DESCRIPTION**

The AD5539 is a two-stage, very high frequency amplifier. The first stage consists of a differential gain amplifier with input transistors Q1, Q4-Q2, Q3 form the first stage—a differential gain amplifier with a voltage gain of approximately 50. The second stage, Q5, is a single-ended amplifier whose input is derived from one phase of the differential amplifier output; the other phase of the differential output is summed with the output of Q5. The all NPN design of the AD5539 is configured such that the emitter of Q5 is returned to ground through a small resistor to ground; this eliminates the need for separate level shifting circuitry.

The output stage, consisting of transistors Q9 and Q10, is a common-emitter voltage follower with a resistive pull-down. The biasing network, consisting of transistors Q6, Q7 and Q8, provides a stable emitter current for the input section, compensating for temperature and power supply variations.

**SOME GENERAL PRINCIPLES OF HIGH FREQUENCY CIRCUIT DESIGN**

When designing practical circuits with the AD5539, the user must remember that whenever very high frequencies are involved,

some special precautions are in order. All real-world applications circuits must be built using proper RF techniques: the use of short interconnect leads, adequate shielding, groundplanes, and very low profile IC sockets. In addition, very careful bypassing of power supply leads is a must.

Low-impedance transmission line is frequently used to carry signals at RF frequencies: 50 Ω line for telecommunications purposes and 75 Ω for video applications. The AD5539 offers a relatively low output impedance; therefore, some consideration must be given to impedance matching. A common matching technique involves simply placing a resistor in series with the amplifier output that is equal to the characteristic impedance of the transmission line. This provides a good match (although at a loss of 6 dB), adequate for many applications.

All of the circuits here were built and tested in a 50 Ω system. Care should be taken in adapting these circuits for each particular use. Any system which has been properly matched and terminated in its characteristic impedance should have the same small signal frequency response as those shown in this data sheet.

**APPLYING THE AD5539**

The AD5539 is stable for closed-loop gains of 4 or more as an inverter and at (noise) gains of 5 or greater as a voltage follower. This means that whenever the AD5539 is operated at noise gains below 5, external frequency compensation must be used to insure stable operation.

The following sections outline specific compensation circuits which permit stable operation of the AD5539 down to follower (noise) gains of 3 (inverting gains of 2) with corresponding -3 dB bandwidths up to 390 MHz. External compensation is achieved by modifying the frequency response to the AD5539's external feedback network (i.e., by adding lead-lag compensation) so that the amplifier operates at a noise gain of 5 (or more) at frequencies over 44 MHz, independent of signal gain.

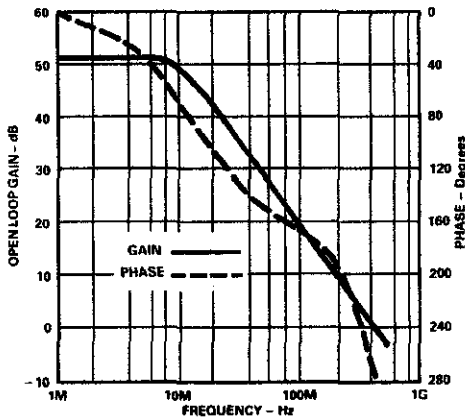


Figure 13. Small Signal Open-Loop Gain and Phase vs. Frequency

**GENERAL PRINCIPLES OF LEAD AND LAG COMPENSATION**

The AD5539 has its first pole or breakpoint in its open-loop frequency response at about 10 MHz (see Figure 13). At frequencies beyond 100 MHz, phase shift increases such that the output lags the input by 180°—well before the unity gain crossover frequency. Therefore, severe peaking (and possible oscillation) will result if the AD5539 is operated at noise gains below 5, unless external compensation is employed. Figure 14 shows the uncompensated closed-loop frequency response of the AD5539

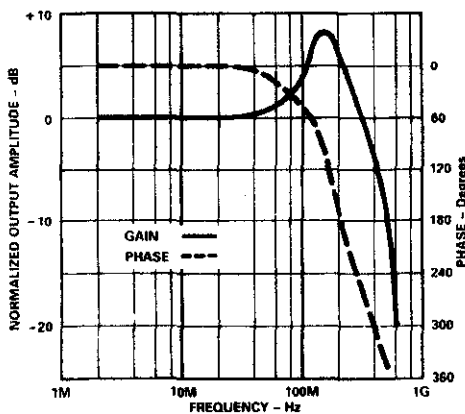


Figure 14. AD5539 Uncompensated Response, Closed-Loop Gain = 7

when operating at a noise gain of 7. Under these conditions, excess phase shift causes nearly 10 dB of peaking at 150 MHz.

Figure 15 illustrates the use of both lead and lag compensation to permit stable low-gain operation. The AD5539 is shown connected as an inverting amplifier with the required external components added to provide stability and improve high frequency response. The stray capacitance between the amplifier summing junction and ground,  $C_X$ , represents whatever capacitance is associated with the particular type of op amp package used plus the stray wiring capacitance at the summing junction.

Evaluating the lead capacitance first (ignoring  $R_{LAG}$  and  $C_{LAG}$  for now): the feedback network, consisting of  $R_2$  and  $C_{LEAD}$ , has a pole frequency equal to:

$$F_A = \frac{1}{2\pi(C_{LEAD} + C_X)(R_1 \parallel R_2)} \quad (1)$$

and a zero frequency equal to:

$$F_B = \frac{1}{2\pi(R_1 \times C_{LEAD})} \quad (2)$$

Usually, frequency  $F_A$  is made equal to  $F_B$ ; that is,  $(R_1 C_X) = (R_2 C_{LEAD})$ , in a manner similar to the compensation used for an attenuator or scope probe. However, if the pole frequency,  $F_A$ , will lie above the unity gain crossover frequency (440 MHz), then the optimum location of  $F_B$  will be near the crossover

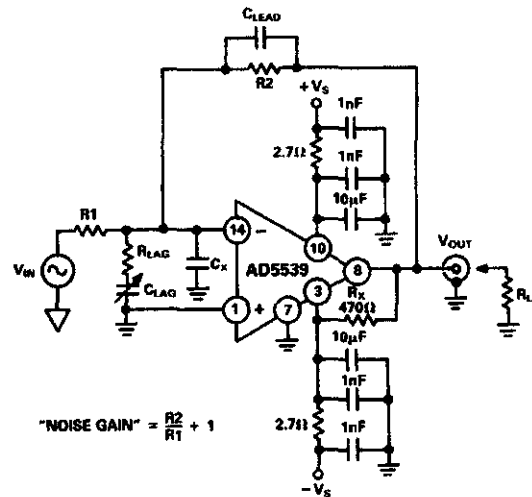


Figure 15. Inverting Amplifier Model Showing Both Lead and Lag Compensation

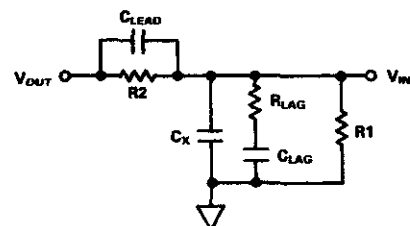


Figure 16. A Model of the Feedback Network of the Inverting Amplifier

frequency. Both of these circuit techniques add a large amount of leading phase shift at the crossover frequency, greatly aiding stability.

The lag network ( $R_{LAG}$ ,  $C_{LAG}$ ) increases the feedback attenuation, i.e., the amplifier operates at a higher noise gain, above the crossover frequency, typically one-tenth of the crossover frequency. For example, to achieve a noise gain of 5 at frequencies above 10 MHz, for the circuit of Figure 15, would require a network

$$R_{LAG} = \frac{R1}{(4R1/R2) - 1} \quad (3)$$

and ...

$$C_{LAG} = \frac{1}{2\pi R_{LAG} (44 \times 10^6)} \quad (4)$$

It is worth noting that an  $R_{LAG}$  resistor may be used alone, to increase the noise gain above 5 at all frequencies. However, this approach has the disadvantage of also increasing the dc offset and low frequency noise errors by an amount equal to the increase in gain, in this case, by a factor of 5.

**SOME PRACTICAL CIRCUITS**

The preceding general principles may now be applied to some practical circuits.

**General Purpose Inverter Circuit**

Figure 17 is a general purpose inverter circuit operating at a gain of -2.

For this circuit, the total capacitance at the inverting input is approximately 3 pF; therefore,  $C_{LEAD}$  from Equations 1 and 2 needs to be approximately 1.5 pF. As shown in Figure 17, a trimmer is used to optimize the frequency response of this circuit. Without a lag compensation network, the noise gain of the circuit is 3.0 and, as shown in Figure 18, the output amplitude remains within  $\pm 0.5$  dB to 170 MHz and the -3 dB bandwidth is 200 MHz.

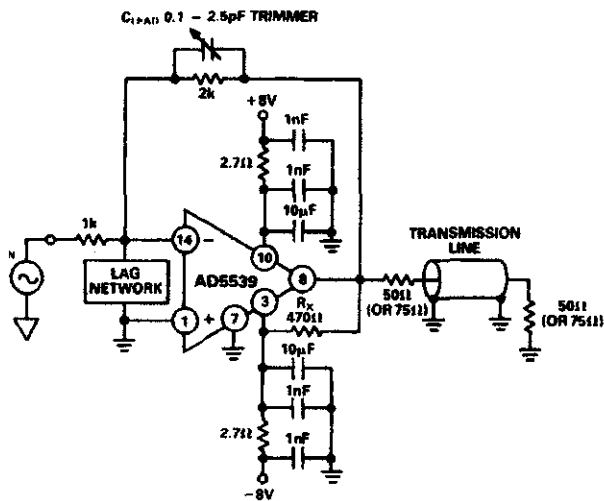


Figure 17. A General Purpose Inverter Circuit

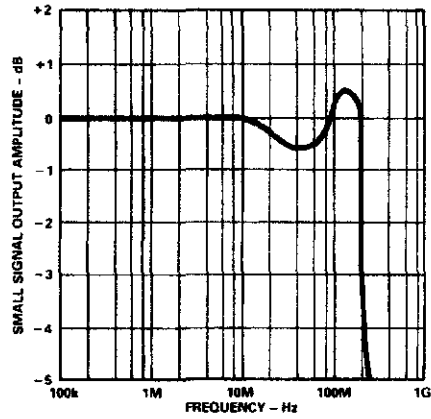


Figure 18. Response of the (Figure 17) Inverter Circuit without a Lag Compensation Network

A lag network (Figure 15) can be added to improve the response of this circuit even further as shown in Figures 19 and 20. In almost all cases, it is imperative to make capacitor  $C_{LEAD}$  adjustable; in some cases,  $C_{LAG}$  must also be variable. Otherwise, component and circuit capacitance variations will dominate circuit performance.

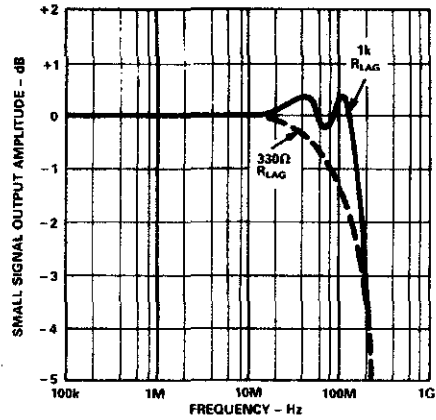


Figure 19. Response of the (Figure 17) Inverter Circuit with an  $R_{LAG}$  Compensation Network Employed

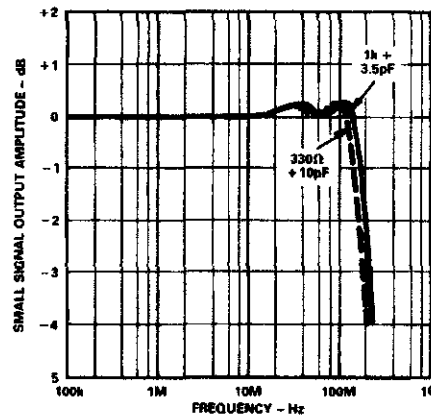


Figure 20. Response of the (Figure 17) Inverter Circuit with an  $R_{LAG}$  and a  $C_{LAG}$  Compensation Network Employed

Figures 21 and 22 show the small and large signal pulse responses of the general purpose inverter circuit of Figure 17, with  $C_{LEAD} = 1.5 \text{ pF}$ ,  $R_{LAG} = 330 \text{ } \Omega$  and  $C_{LAG} = 3.5 \text{ pF}$ .

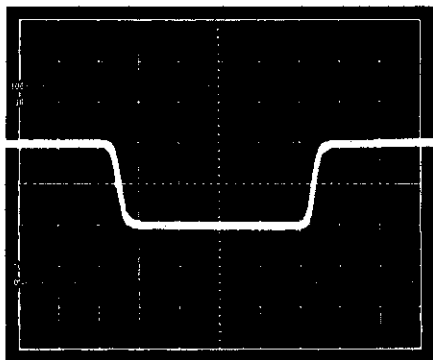


Figure 21. Small Signal Pulse Response of the (Figure 17) Inverter Circuit; Vertical Scale: 50 mV/div; Horizontal Scale: 5 ns/div

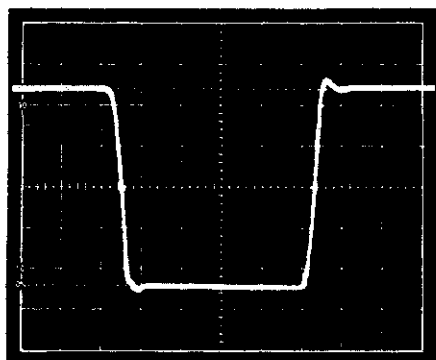


Figure 22. Large Signal Response of the (Figure 17) Inverter Circuit; Vertical Scale: 200 mV/div; Horizontal Scale: 5 ns/div

A  $C_{LEAD}$  capacitor may be used to limit the circuit bandwidth and to achieve a single pole response free of overshoot

$$\left( -3 \text{ dB frequency} = \frac{1}{2 \pi R_2 C_{LEAD}} \right)$$

If this option is selected, it is recommended that a  $C_{LEAD}$  be connected between Pin 12 and the summing junction, as shown in Figure 23. Pin 12 provides a separately buffered version of the output signal. Connecting the lead capacitor here avoids the excess output-stage phase shift and subsequent oscillation problems (at approx. 350 MHz) which would otherwise occur when using the circuit of Figure 17 with a  $C_{LEAD}$  of more than about 2 pF.

Figure 24 shows the response of the circuit of Figure 23 for each connection of  $C_{LEAD}$ . Lag components may also be added to this circuit to further tailor its response, but, in this case, the results will be slightly less satisfactory than connecting  $C_{LEAD}$  directly to the output, as was done in Figure 17.

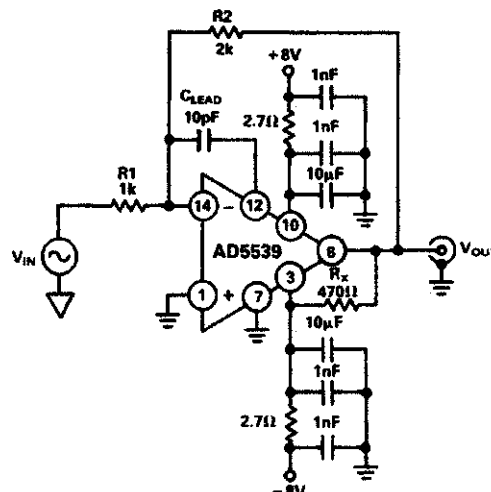


Figure 23. A Gain of 2 Inverter Circuit with the  $C_{LEAD}$  Capacitor Connected to Pin 12

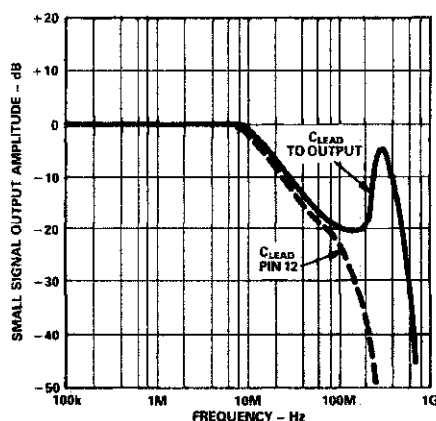


Figure 24. Response of the Circuit of Figure 23 with  $C_{LEAD} = 10 \text{ pF}$

#### A General Purpose Voltage Follower Circuit

Noninverting (voltage follower) circuits pose an additional complication, in that when a lag network is used, the source impedance will affect the noise gain. In addition, the slightly greater bandwidth of the noninverting configuration makes any excess phase shift due to the output stage more of a problem.

For example, a gain of 3 noninverting circuit with  $C_{LEAD}$  connected normally (across the feedback resistor – Figure 25) will require a source resistance of 200  $\Omega$  or greater to prevent UHF oscillation; the extra source resistance provides some damping as well as increasing the noise gain. The frequency response plot of Figure 26 shows that the highest  $-3 \text{ dB}$  frequency of all the applications circuits can be achieved using this connection, unfortunately, at the expense of a noise gain of 14.2.

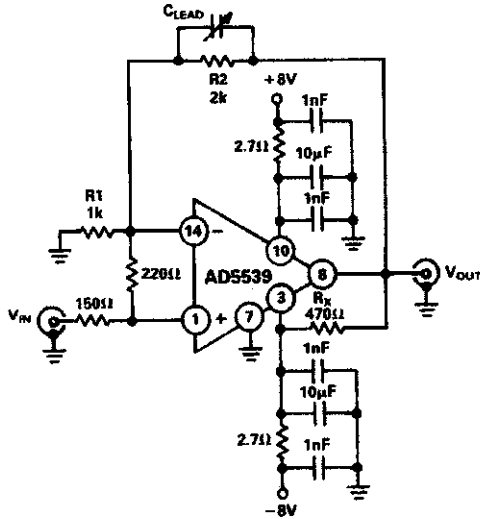


Figure 25. A Gain of 3 Follower with Both Lead and Lag compensation

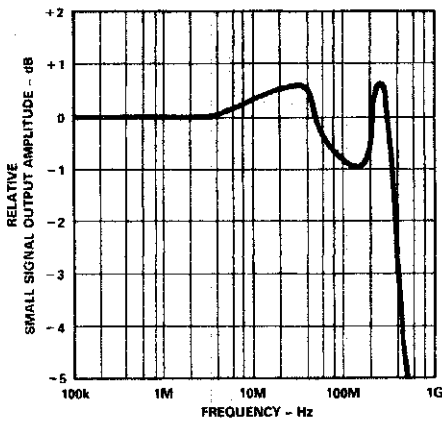


Figure 26. Response of the Gain of 3 Follower Circuit

Adding a lag capacitor (Figure 27) will greatly reduce the midband and low frequency noise gain of the circuit while sacrificing only a small amount of bandwidth as shown in Figure 28.

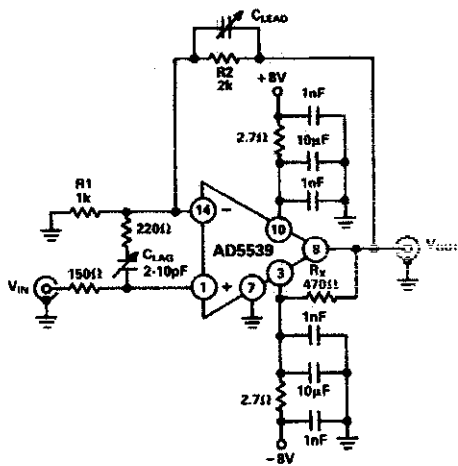


Figure 27. A Gain of 3 Follower Circuit with Both CLEAD and RLag Compensation

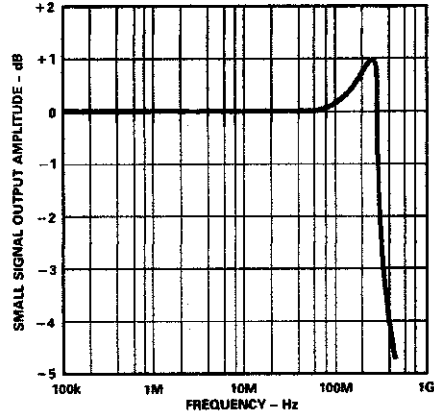


Figure 28. Response of the Gain of 3 Follower with CLEAD, CLAG and RLag

These same principles may be applied when capacitor CLEAD is connected to Pin 12 (Figure 29). Figure 30 shows the bandwidth of the gain of 3 amplifier for various values of RLag. It can be seen from these response plots that a high noise gain is still needed to achieve a reasonably flat response (the smaller the

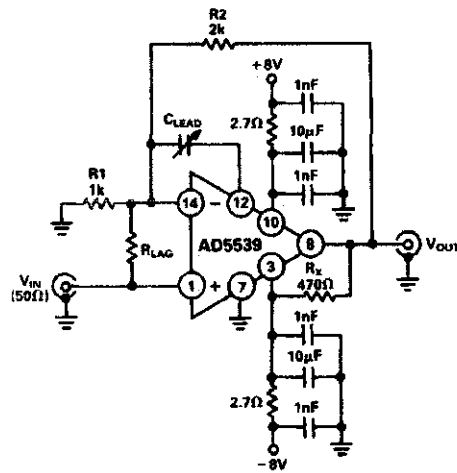


Figure 29. A Gain of 3 Follower Circuit with CLEAD Compensation Connected to Pin 12

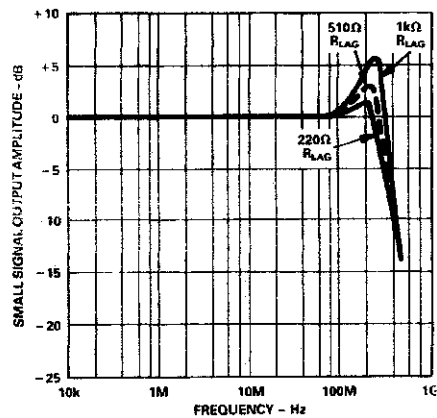


Figure 30. Response of the Gain of 3 Follower Circuit with CLEAD Connected to Pin 12

value of  $R_{LAG}$ , the higher the noise gain). For example, with a  $220\ \Omega$   $R_{LAG}$  and a  $50\ \Omega$  source resistance, the noise gain will be 12.8, because the source resistance affects the noise gain.

Figures 31 and 32 show the small and large signal responses of the circuit of Figure 29.

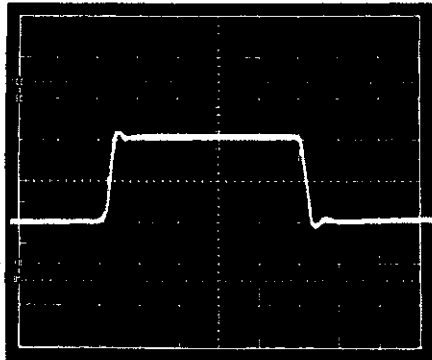


Figure 31. The Small-Signal Pulse Response of the Gain of 3 Follower Circuit with  $R_{LAG}$  and  $C_{LEAD}$  Compensation to Pin 12; Vertical Scale: 50 mV/div; Horizontal Scale: 5 ns/div

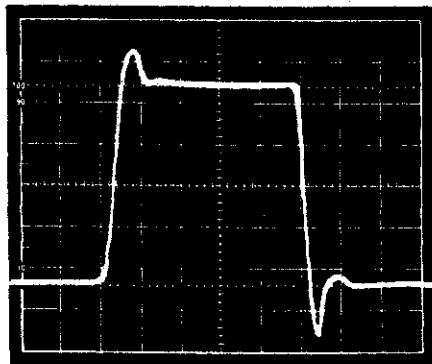


Figure 32. The Large-Signal Pulse Response of the Gain of 3 Follower Circuit with  $R_{LAG}$  and  $C_{LEAD}$  Compensation to Pin 12; Vertical Scale: 200 mV/div; Horizontal Scale: 5 ns/div

**A Video Amplifier Circuit with 20 dB Gain (Terminated)**

High gain applications (14 dB and up) require only a small lead capacitance to obtain flat response. The 26 dB (20 dB terminated) video amplifier circuit of Figure 33 has the response shown in Figure 34 using only approximately 0.5-1 pF lead capacitance. Again, a small  $C_{LEAD}$  can be connected, either to the output or to Pin 12 with very little difference in response.

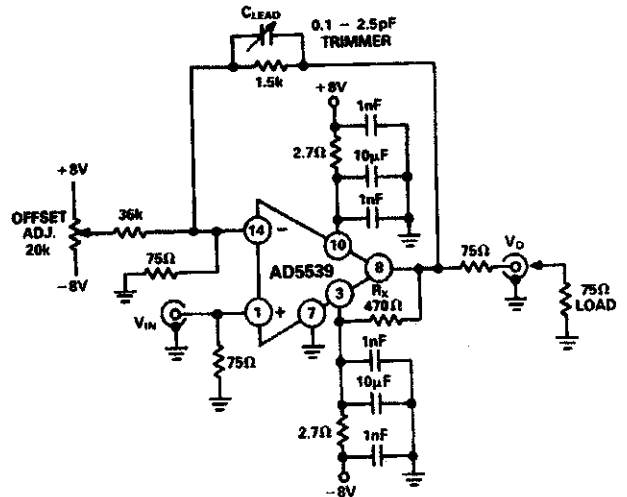


Figure 33. A 20 dB Gain Video Amplifier for 75  $\Omega$  Systems

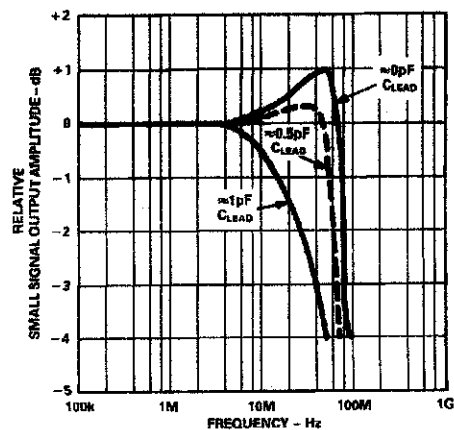


Figure 34. Response of the 20 dB Video Amplifier

In color video applications, the quality of differential gain and differential phase response is very important. Figures 35 and 36 show a circuit and test setup to measure the AD5539's response to a modulated ramp signal (0-90 IRE p-p ramp, 40 IRE p-p modulation, 4.4 MHz).

Figures 37 and 38 show the differential gain and phase response.

**APPENDIX D**  
**TDA 9045 DATASHEET**



**APPENDIX D**  
**TDA 9045 DATASHEET**

## DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

TDA9045

## VIDEO PROCESSOR AND INPUT SELECTOR

### GENERAL DESCRIPTION

The TDA9045 is a monolithic integrated circuit for video signal processing and input selection.

### FEATURES

- Selection stage for three different inputs
- 4 dB amplifier
- Constant output signal amplifier controlled by synchronizing level and peak white level
- Clamping stage for a constant black level
- Circuit for stopping clamping pulses during the sync pulses
- Emitter follower output stage

### QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V <sub>p</sub>	—	12	—	V
Supply current		I <sub>p</sub>	—	60	—	mA
<b>Pre-amplifier</b>						
Composite colour video input signals (peak-to-peak value)		V <sub>2, 3, 4-11(p-p)</sub>	—	—	2	V
<b>AGC amplifier</b>						
Composite video signal (peak-to-peak value)	±6 dB	V <sub>12-11(p-p)</sub>	—	0,4	—	V
<b>Sync level detector</b>						
Threshold voltage for sync level control		V <sub>9-11</sub>	—	1,8	—	V
<b>Selection</b>						
active input pin 2		V <sub>1-11</sub> V <sub>15-11</sub>	— —	5 5	— —	V V
active input pin 3		V <sub>1-11</sub> V <sub>15-11</sub>	0 —	— 5	— —	V V
active input pin 4		V <sub>1-11</sub> V <sub>15-11</sub>	0 0	— —	— —	V V
Not allowed condition		V <sub>1-11</sub> V <sub>15-11</sub>	— —	5 0	— —	V V

### PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

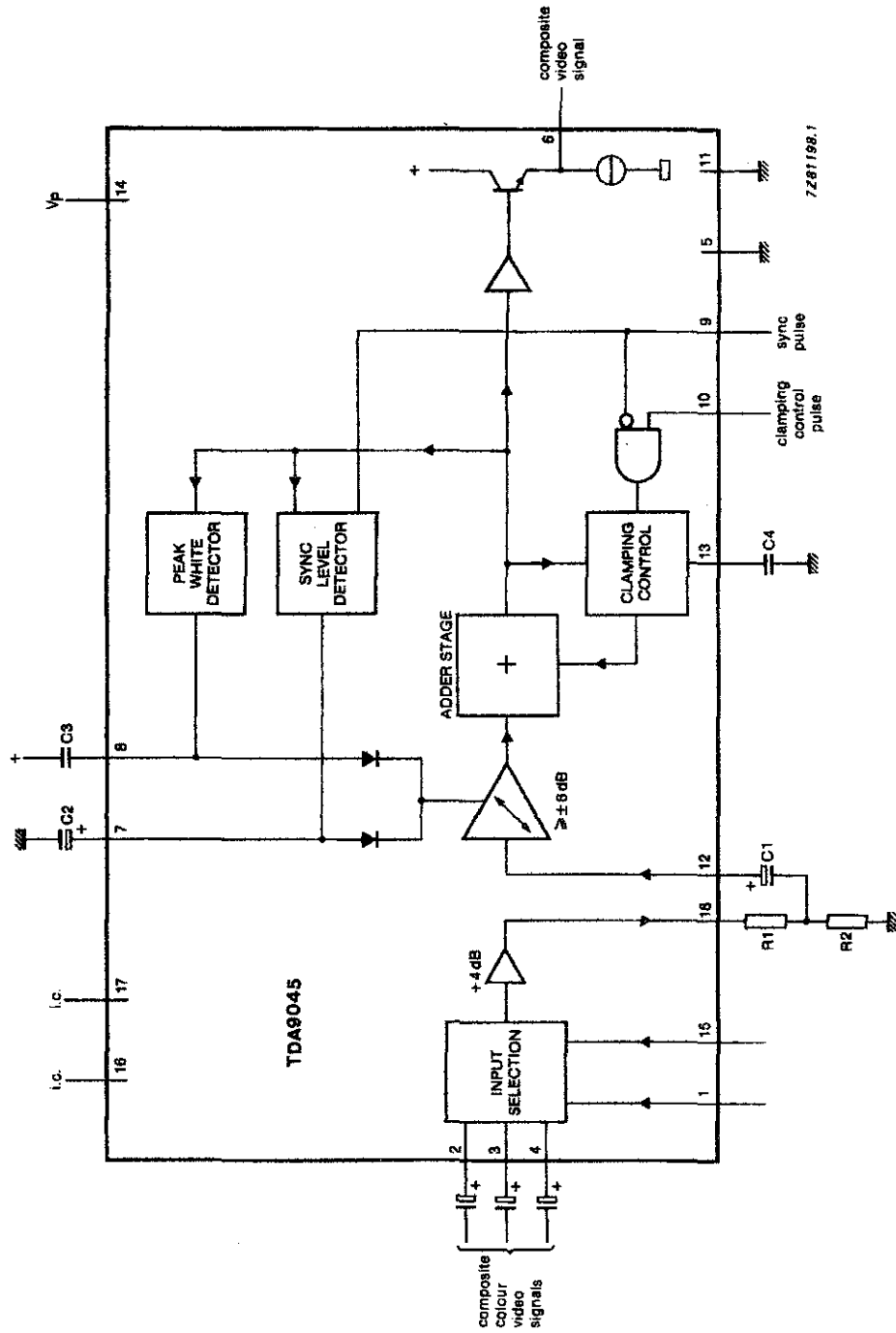


Fig. 1 Block diagram.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V <sub>p</sub>	0	13,2	V
Voltage on pins 9, 10, 12 to pin 11 (GND)		V <sub>n-11</sub>	0	V <sub>p</sub>	V
Voltage readings		V <sub>2, 3, 4-11</sub>	0	0,8 V <sub>p</sub>	V
		V <sub>7, 8-11</sub>	0,7 V <sub>p</sub>	V <sub>p</sub>	V
		V <sub>13-11</sub>	0,25 V <sub>p</sub>	V <sub>p</sub>	V
		V <sub>1, 15-11</sub>	0	5,5	V
Current readings		I <sub>6</sub>	—	10	mA
		I <sub>18</sub>	—	20	mA
Total power dissipation		P <sub>tot</sub>	—	1	W
Storage temperature range		T <sub>stg</sub>	-25	+150	°C
Operating ambient temperature range		T <sub>amb</sub>	0	+70	°C

**CHARACTERISTICS**V<sub>p</sub> = V<sub>14-11</sub> = 12 V; trigger pulse width pin 10 = 4 μs; T<sub>amb</sub> = 25 °C; measured in test circuit Fig. 2 unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V <sub>p</sub>	9,6	—	13,2	V
Supply current		I <sub>p</sub>	—	60	—	mA
<b>Input channel selector</b>						
Input resistance		R <sub>1-11</sub>	—	7,5	—	kΩ
Selector switching voltage select input pin 4		V <sub>1-11</sub>	0	—	1	V
		V <sub>15-11</sub>	0	—	1	V
select input pin 3		V <sub>1-11</sub>	0	—	1	V
		V <sub>15-11</sub>	2,5	5	5,5	V
select input pin 2		V <sub>1-11</sub>	2,5	5	5,5	V
		V <sub>15-11</sub>	2,5	5	5,5	V

DEVELOPMENT DATA

## CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
<b>Pre-amplifier</b>						
Composite colour video input signals (peak-to-peak value)		$V_{2,3,4-11(p-p)}$	—	1	2,0	V
Input resistance		$R_{2,3,4-11}$	—	10	—	k $\Omega$
Input capacity		$C_{2,3,4-11}$	—	10	—	pF
Amplification		$A_{18-2,3,4}$	—	4	—	dB
DC output voltage		$V_{18-11}$	—	5,8	6,4	V
Frequency response	0 to 7 MHz		—	—	$\pm 2$	dB
Signal suppression at output	pin 18 with no input		50	—	—	dB
<b>AGC amplifier</b>						
Input voltage composite video signal (peak-to-peak value)	$\pm 6$ dB	$V_{2,3,4-11(p-p)}$	—	0,4	—	V
Input resistance		$R_{12-11}$	—	10	—	k $\Omega$
Input capacity		$C_{12-11}$	—	10	—	pF
Frequency response	0 to 7 MHz		—	—	$\pm 2$	dB
<b>Peak white and sync pulse level detectors</b>						
capacitor current charging current		$-I_8$	—	15	—	mA
discharging current		$I_8$	—	0,8	—	$\mu$ A
charging current		$-I_7$	—	0,3	—	mA
discharging current		$I_7$	—	0,3	—	mA
Threshold voltage for sync level controls		$V_{9-11}$	1	1,8	2,4	V
Input current		$-I_{9-11}$	—	—	50	$\mu$ A
<b>Clamping control triggering and sync pulse regeneration</b>						
Threshold voltage for clamping control ON	$V_{9-11} = 0$ V	$V_{10-11}$	1	1,8	2,4	V
Input current		$-I_{10-11}$	—	—	50	$\mu$ A
Charging current		$-I_{13}$	—	0,3	—	mA
Discharging current		$I_{13}$	—	0,3	—	mA
Black level voltage		$V_{6-11}$	5,2	5,6	6	V
Controlled output signal (peak-to-peak value)		$V_{6-11(p-p)}$	3,7	3,9	4,1	V

DEVELOPMENT DATA

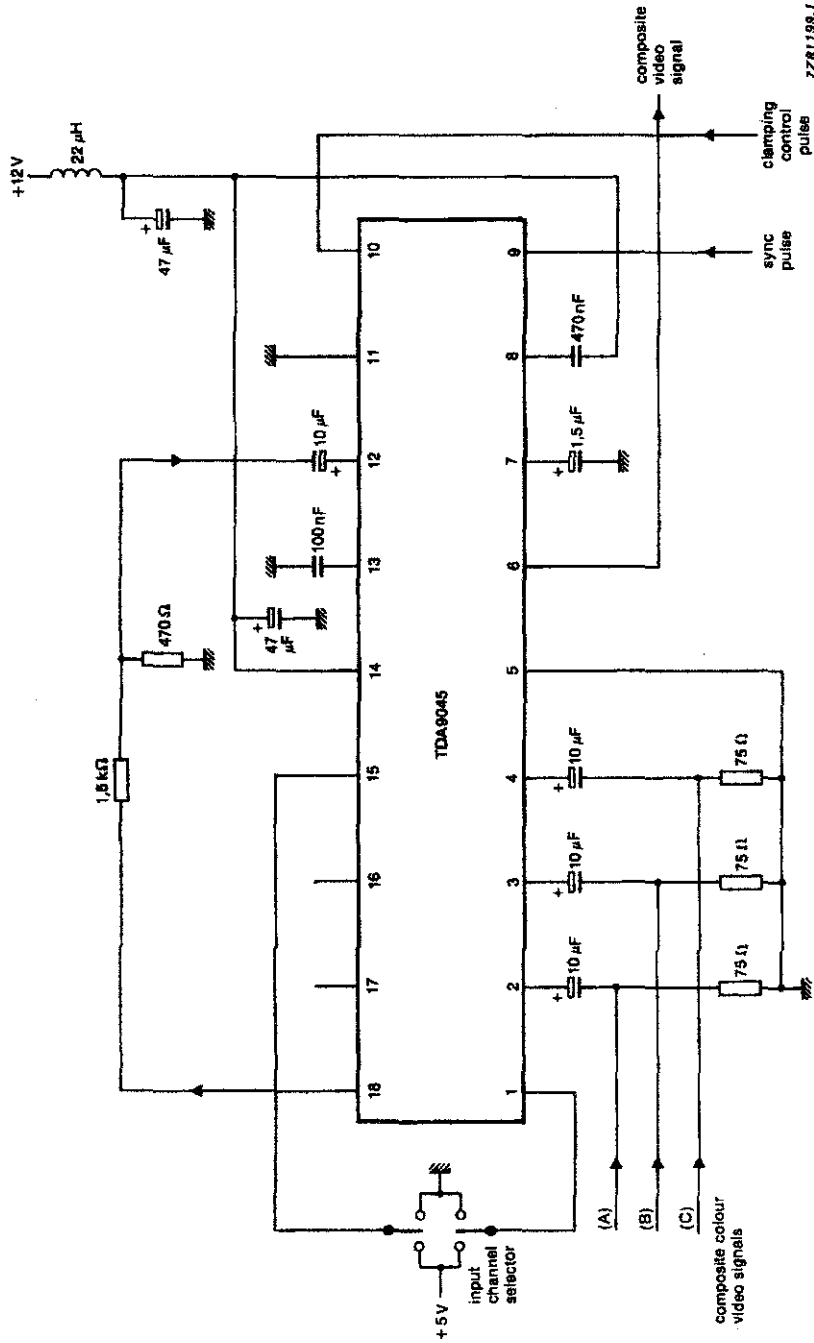


Fig. 2 Application diagram; also used as test circuit.