Simulation and Study of an Insulated Gate Bipolar Transistor (IGBT) for Medium Power Application

by

Mohd Khairun Affandy bin Mohamad@Hamid

Dissertation submitted in partial fulfillment of
the requirements for the
Bachelor of Engineering (Hons)
(Electrical & Electronics Engineering)

JUNE 2007

Universiti Teknologi PETRONAS
Bandar Seri Iskandar
31750 Tronoh
Perak Darul Ridzuan

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CERTIFICATION OF APPROVAL

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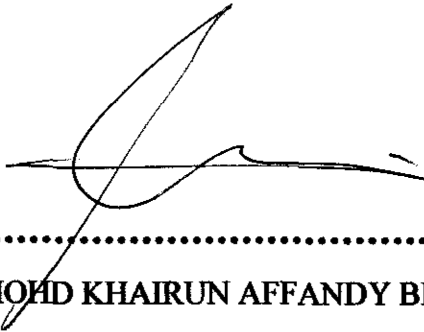
Approved by,

....
(ASSOCIATE PROFESSOR DR. NORANI MUTI MOHAMED)

Universiti Teknologi PETRONAS
Bandar Seri Iskandar
31750 Tronoh
Perak Darul Ridzuan

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.



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(MOHD KHAIRUN AFFANDY BIN MOHAMAD)

ABSTRACT

Insulated Gate Bipolar Transistor (IGBT) is one of the switching devices which is widely use in medium power application. IGBT provide the characteristic of almost ideal switch for very high voltage and current level. The advantage of IGBT is that is uses the high current density bipolar application which will result in low conduction loss. The main objective of this project is to investigate and study on the devices structuring process involves in creating IGBT. The focus of this project is to improve the performance of the existing design which is commercially available. This project was done by familiarizing with the semiconductor fabrication software. During this period, simulation of the NMOS fabrication structure was done using the ATHENA and ATLAS software. Then, the available example of the IGBT will be loaded, the structure of the IGBT will be reviewed and electrical performance of the IGBT will be evaluated. The IGBT structure will be modified in order to investigate whether the modified IGBT performance will improve or become worst. The expected result should be the new structure of the modified IGBT with improves performance and comparison data between the conventional IGBT and modified IGBT. Due to some technical problem occur during handling this project, student are not able to produce the expected result. Due to this problem, student are required to do study on the IGBT design for reducing EMI effect in order to backup the result of this project due to technical problem occur.

ACKNOWLEDGEMENT

First and foremost, I would like to thank Allah the most Gracious and Merciful for all His blessing that made all things possible while doing this project. This project would not have been possible without productive contributions, supports, guidance and efforts from Universiti Teknologi PETRONAS. I would like to thank my supervisor, Associate Professor Dr Norani Muti Mohamed for all guidance through the period of this study. Without the advice and supervisions, this study may not be able to be accomplished. I would like to extend my gratitude to technician Mr. Megat and Mdm Siti Hawa in guiding me in completing this project. My credit also goes to my colleagues and friends, who also have given a great deal of contribution and moral support in term of references and useful data. Finally, thank to others who had also helped me directly and indirectly throughout this course completion.

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CHAPTER 1

INTRODUCTION

1.1 BACKGROUND OF STUDY

IGBT is widely use in industrial application today. IGBT displaced the power bipolar transistor for the high current and high voltage application. The industry trend today of IGBT is to replace the MOSFET application except for very low current application. IGBT is actually the switching device which is use in power conversion process [1]. Since the power conversion relies more on switched application, devices which approach ideal switch should be designed. Ideal switch should have following characteristic:

- Zero resistance or forward voltage drop in on-state
- Infinite resistance in off-state
- Switch with infinite speed
- Do not require any input power to make it switch

In solid state technologies, ideal switch must be deviate and a device which suits the application with minimal loss of efficiency must be choose [1]. Choices of the device involve the following consideration [1]:

- Voltage
- Current
- Switching speed
- Drive circuitry

- Load
- Temperature effects

Combination of easily driven MOS gate and low conduction loss of BJT, make the IGBT are much preferable to displace bipolar transistor for high current and high voltage application. The operation of the IGBT is controlled by the gate voltage drive requirement. Its gate drive requirements are inherited from the MOSFET, and are much more modest than those of the GTO. The IGBT gate appears to its driver as capacitor, which simply has to be charged around +15V to turn the device on, and discharged to turn it off. Also inherited from the MOSFET is an active region where the gate can control the device current (this has important implications for its behavior as a switch). From its bipolar features, IGBT gain lower conduction losses than those of a similarly rated MOSFET. There are two types of IGBT available in the markets which are as follow:

- Punch Through (PT) IGBT
- Non Punch Through (NPT) IGBT

This project will be focusing on the simulation and comparative study about the conventional IGBT and modified IGBT base on basic operation of the IGBT.

1.2 PROBLEM STATEMENT

In this project, student needs to design the IGBT for a medium power application. Actually, IGBT is one of the switching devices which is widely use in medium power application. This is because the IGBT provide the characteristic of almost ideal switch for very high voltage and current levels.

Actually in this project, no new structure will be creating. Some modification will be done to the existing design in the Sun Microsystem workstation in order to improve the performance of the device. Student only needs to focus on some portion of the device performance. Modification will be done by modifying the structure characteristic of the device which will result in the changes of the devices performance. The improvement of the devices performance can be identified by evaluating the structure and electrical characteristic of the devices after modification was done.

At the same time, student also required to locate standard IGBT characteristic that are available industry. Then, student need to identify whether the modified device performance become better or worst compared to standard IGBT. The end result of this project will be the comparison between the conventional IGBT and modified IGBT. The performance of the modified IGBT will be analyzed in order to identify whether it is improved or become worst.

1.3 OBJECTIVE OF THE PROJECT

The objectives of this project are as follow:

- To familiarize with the semiconductor fabrication software (Silvaco ATHENA and Silvaco ATLAS) using Sun Microsystem workstation.
- To load the standard or existing IGBT example that available in Sun Microsystem workstation and modifying that IGBT structure using Silvaco ATHENA software.
- To interpret and analyzed the electrical performance of the standard IGBT and modified IGBT through the simulation by using Silvaco ATLAS software.
- To identify whether the performance of the modified IGBT is improve or not compared to standard IGBT.
- To come out with the comparison data between conventional IGBT and modified IGBT.

The existing device sample that available in Sun Microsystem workstation will be modified in order to get the new device structure. Hopefully, this new IGBT structure will come out with the improve performance. Lot of literature review was done before and after student starts this project. Continuous study and literature review are very important in order to complete this project.

1.4 SCOPE OF STUDY

Refer to figure 1 below for the scope of study that need to be follow by the student in order to complete this project.

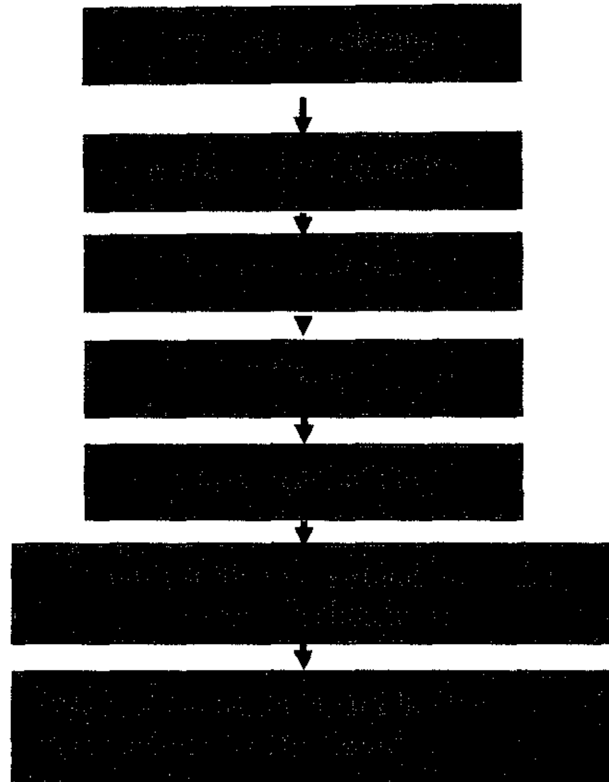


Figure 1: Scope of Study

From figure 1, first of all, student must identify the problem statement of the project. From this problem statement, student will be able to identify and setting up the objective of the project need to be achieved. Student must identify and understand the problem statement of the project before start the project. Once we know and understand the objective of the project, we will automatically identify the scope of study in implementing this project. Lot of literature research and review should be done in order to fully grab the information and understanding about the theory of the devices. In this part, all the information about the project must be grabbing through the research in internet and through the reading of the journals, conference paper and also the text book. After this step was done, continue with the methodology of the project. In this

methodology step, all the work in completing the project will be done. For the last semester, the methodology of the project that was done is familiarization with the software to be used in implementing this project. For this semester, methodology part will cover about the modification and result evaluations in order to achieve a new improve IGBT performance. Lastly, the result, analyze data, and devices performance characteristic will be collect in order to make a comparison with the existing devices for the presentation purpose.

1.4.1 Project Requirement

I. To conduct a study on IGBT structure for medium power applications.

II. Identifying the process involve in creating the IGBT structure and verifying the effect of the device characteristics when its parameters are changed by using ATHENA and ATLAS simulations.

III. To collect the comparison and analyzed data of modified structure with the existing device.

IV. To investigate how the parameter changes effects the device electrical characteristics.

V. Find out the ways of how to improve the device performance so that a better device can be created.

1.4.2 Feasibility of the Project within the Scope and Time Frame

The allocated time for this project is two semesters (28 weeks). Base on the Gantt chart (**Appendix A**) and project planning, the study on IGBT structure was implemented on the first semester. For this semester, student will be focusing on the modification and study on the existing device because of the limited time frame. That's why in this second semester, student will focusing in modifying the existing devices that's available in order to get the comparison between the modified devices and existing devices.

CHAPTER 2

LITERATURE REVIEW AND THEORY

2.1) BASIC IGBT STRUCTURE

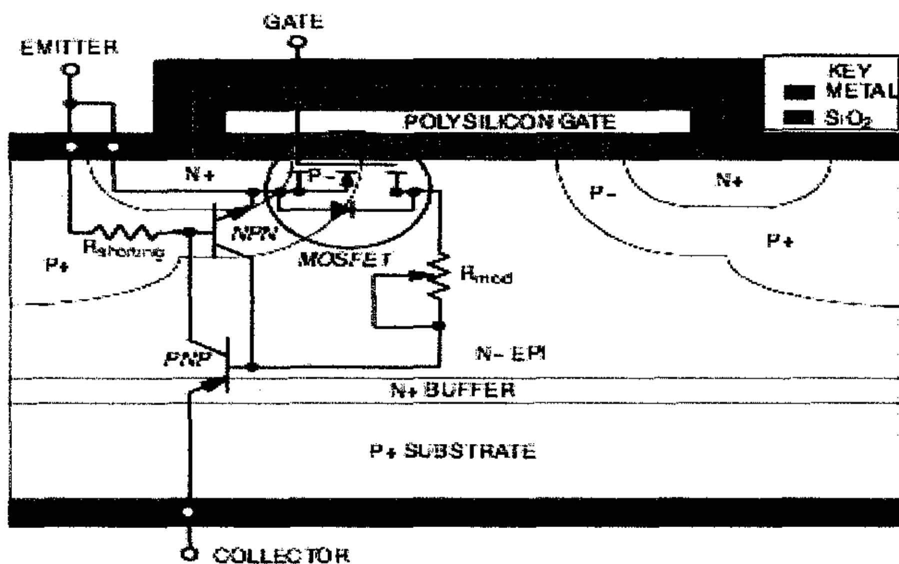


Figure 2.1 : Cross Section and Equivalent Schematic of the IGBT cell.

Figure 2.1a shows the cross section and equivalent schematic of the IGBT cell taken from [1]. As we can see, IGBT structure basically consists of:

- P+ substrate
- P- and P+
- N+ buffer
- N- EPI
- N+

N- EPI region was placed on P+ substrate forming a p-n junction where conductivity modulation takes place. P+ substrate, N-EPI layer and P+ "emitter" form a BJT transistor and the N-EPI acts as a wide base region. Current flowing from collector to emitter must pass through a p-n junction formed by the P+ substrate and N- EPI layer. For fast devices, the N+ buffer layer is highly doped for recombination and speedy turn off. The additional doping keeps the gains of the PNP low and allow two third of the current to flow through the base of PNP (electron current) while one third pass through the collector (hole current). Rshorting is the parasitic resistance of the P+ emitter region. Current flowing through Rshorting will result in a voltage across the base-emitter junction of the NPN. If the base emitter voltage is above a certain threshold level, the NPN will begin to conduct causing the NPN and PNP to enhance each other's current flow and both devices can become saturated.

The structure of the devices is similar to that of vertical double diffuse MOSFET with the exception that a highly doped p- type substrate is used is lieu of a highly doped n-type drain contact in a vertical double diffused MOSFET. Figure 2.2 shows the cross section and equivalent schematic of a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) cell taken from [1]. Compare figure 2.1 and 2.2 to catch the differences and similarity between IGBT and MOSFET.

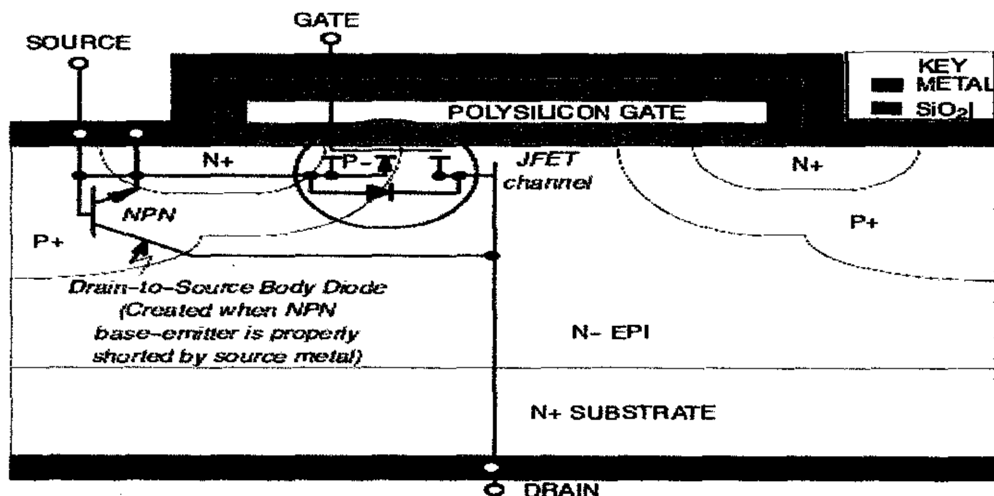


Figure 2.2: Cross section and equivalent schematic of a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) cell

Figure 2.3 shows the cross section schematic of IGBT half cell taken from [2].

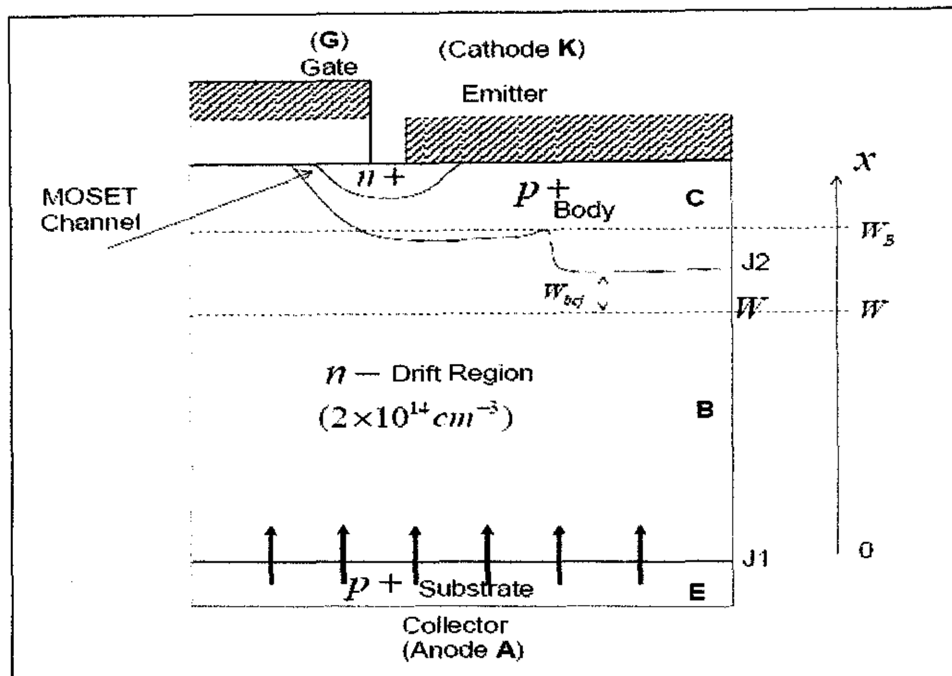


Figure 2.3: Cross section schematic of IGBT half cell

A lightly doped thick n-type epitaxial layer ($N_B = 10^{14}$ cm^{-3}) is grown on top of the p-type substrate. The function of this layer is to support the high blocking voltage in the reverse bias mode state. A highly doped p-type region ($N_A = 10^{19}$ cm^{-3}) is used to prevent the activation of the PNPN thyristor during device operation [1]. A highly doped n+ buffer layer could also be added on top of the highly doped p+ substrate. According to [2], this layer help in reducing the Turn-Off time of the IGBT during the transient operation. Refer to figure 2.1a for the configuration of this layer. This buffer layer can be chosen whether to be included or not in IGBT structure. IGBT that consist this type of layer is known as PT IGBT. IGBT without this buffer layer is known as NPT IGBT.

For PT IGBT, the epilayer is not as thick (less thick) as NPT IGBT because a n+ layer is placed over the p+ layer. This n+ layer can handle some of the punch through and act as a shield to the J1 junction [2]. This layer occupies some spaces in the base of IGBT, which leaves less space for the total charges in the base region during the IGBT on state (turn-on) operation. Meaning that, these charges are removed more quickly

when switching occurs. Holes will be recombining with electron in n+ layer before reaching the base region. Fewer holes will be injected into the base region (lower efficiency). This will result in carrier lifetime reduce and increased in switching frequency. Since less carriers injected into the base region if compared to NPT IGBT, conductivity is reduced and the on-state voltage is increased. The trade OFF between the reduced turn-OFF time and the increased on-state voltage should be accounted during IGBT designing [1].

For NPT IGBT, the epilayer thickness is thick enough because no n+ layer exists on top of the highly doped p+ layer substrate. Meaning that, n- layer (drift region) for NPT IGBT is greater than PT IGBT. This will result in high resistance in this region and higher reversed voltage can be sustained when J2 is reversed biased.
For better understanding of the equivalent circuit of the IGBT, refer to the figure 2.4 below which were taken from [2].

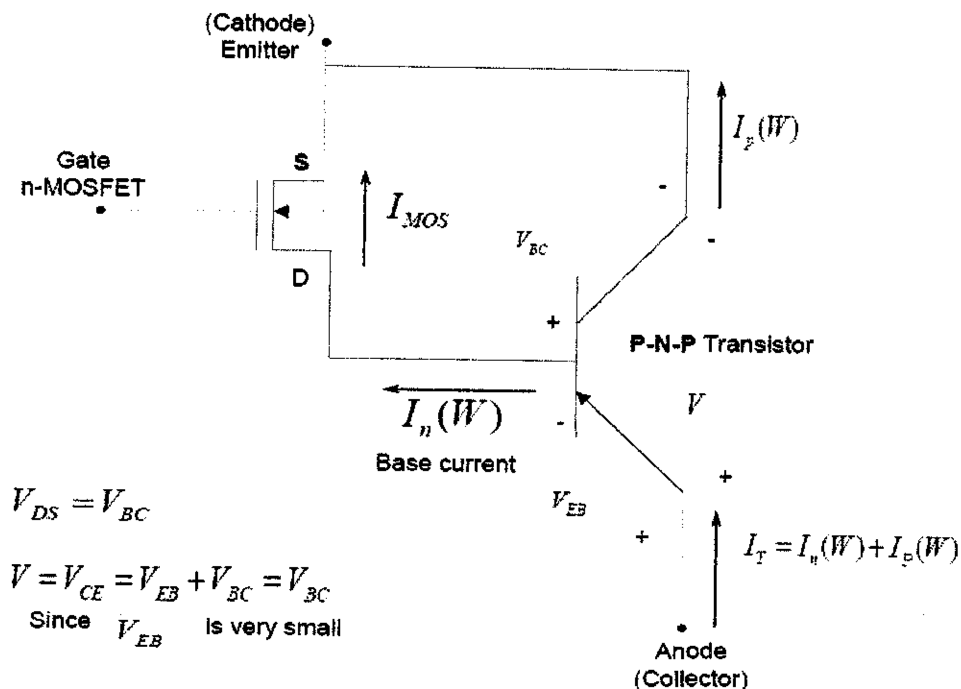


Figure 2.4: Equivalent Circuit Model of IGBT

As we can see from figure 3, we will understand that the equivalent circuit model of the IGBT consist of a wide base P-N-P bipolar junction transistor (BJT) in cascade with MOSFET. Since the IGBT is the combination of the BJT and MOSFET, the basic material use in creating the IGBT structure is as follow:

- Polysilicon
- Silicon
- Silicon Dioxide
- Aluminum

The silicon is defined as an initial structure of the device. From the silicon structure, the silicon dioxide, SiO_2 layer is produced through the oxidation process. This process is used to form the gate oxide layer. The polysilicon is defined as a multilayer deposit structure and the aluminum is used in the metallization process. From [3], the basic semiconductor device fabrications are oxidation process, photolithography and etching, diffusion and ion implantation, and metallization. All this fabrication process will be done through the ATHENA software that available in Sun Microsystem workstation. Actually, the fabrication process is done to produce the physical characteristic of the device. According to [3], all the fabrication processes will be briefly describe in section 2.2.

2.2 SEMICONDUCTOR FABRICATION PROCESS

2.2.1 Oxidation

- There are two type of oxidation, wet and dry, depending on whether dry oxygen or wet vapour is used.
- Dry oxidation is usually used to form thin oxides in a devices structure because of it's good Si – SiO_2 interface characteristic.
- Wet oxidation is used for thicker layer because of its higher growth rate
- Semiconductors can be oxidized by various methods such as follow:
  - Thermal oxidation
  - Electrochemical anodization
  - Plasma enhanced chemical vapour deposition (PECVD)
- Among these methods, thermal oxidation is most important for silicon devices.
- For gallium arsenide, thermal oxidation will result in generally non stoichiometric films.
- The oxides provide poor electrical insulation and semiconductor surface protection: hence, these oxides are rarely used in gallium arsenide technology.
- During oxidation process, silicon wafer is heated around 900°C to 1200°C in atmosphere containing oxygen or water vapor.
- Chemical process involve in oxidation step is as follow:
  - O2 or H2O (oxidant) diffuse to silicon surface
  - Oxidation reaction occurs:

$$Si + O_2 \longrightarrow SiO_2$$

$$Si + 2H_2O \longrightarrow SiO_2 + 2H_2$$

- Refer to figure 2.5 for the furnace layout and figure 2.6 for the process gas options layout of the of the oxidation process.

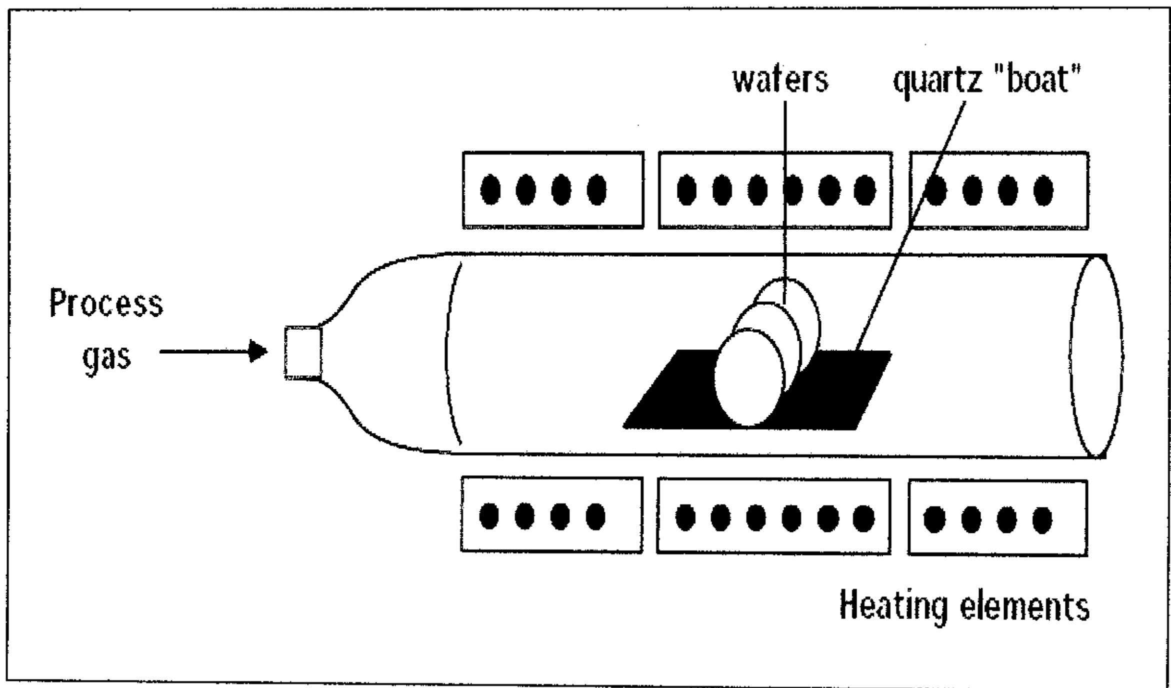


Figure 2.5: Furnace layout of the oxidation process

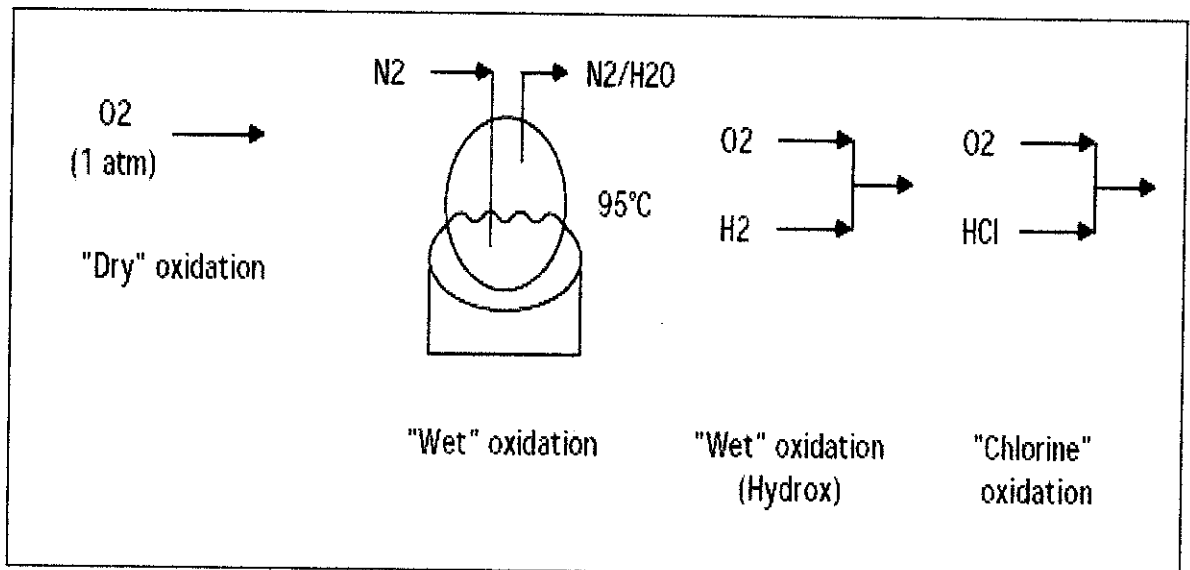


Figure 2.6: Process gas option

2.2.2 Photolithography and Etching

- Photolithography is used to define the geometry of the p-n junction.
- After the formation of SiO_2, the wafer is coated with an ultraviolet (UV) light sensitive material called a photoresist, which is spun on the wafer surface by a high speed spinner.
- Then, the wafer is baked at about 80°C to 100°C to drive the solvent out of the resist and to harden the resist for improved adhesion. Then, the wafer will be exposed through a patterned mask using a UV light source.
- The exposed region of the photoresist – coated wafer undergoes a chemical reaction depending on the type of resist. The area exposed to light become polymerized and difficult to remove in an etchant.
- Wafer is baked again to 120°C to 180°C for 20 minutes to enhance the adhesion and improve the resistance to the subsequent etching process.
- Then, etching process is performing by using the buffered hydrochloric acid (HF) to removes the unprotected SiO_2 surfaces.
- There are two type of etching available in semiconductor fabrication process which are wet and dry etching. Refer to table 1 for the comparison between the wet and dry etching.
- In table 1, there are isotropic and anisotropic term to be consider where:
  - Isotropic etching means the etching rate is the same in both horizontal and vertical direction.
  - Anisotropic etching means the etching rate is different in horizontal and vertical direction.
- Actually etching is the continuous from lithography process. Meaning that, after oxidation process, devices will go through lithography process. After lithography process, etching process will take place.
- Lastly, after lithography process, device will go through strip mask (resist) process. Refer to figure 2.7 for the flow of etching process.

Type of Etching	Wet	Dry
Method	Chemical Solution	Ion Bombardment or Chemical Reactive
Environment and Equipment	Atmosphere, Bath	Vacuum Chamber
Advantage	1) Low cost, easy to implement 2) High etching rate 3) Good selectivity for most materials	1) Capable of defining small feature size (< 100nm)
Disadvantage	1) Inadequate for defining feature size <1um 2) Potential of chemical handling hazards 3) Wafer contamination issues	1) High cost, hard to implement 2) Low throughput 3) Poor selectivity 4) Potential radiation damage
Directionality	Isotropic (Except for etching Crystalline Materials)	Anisotropic

Table 1: Comparison between wet and dry etching

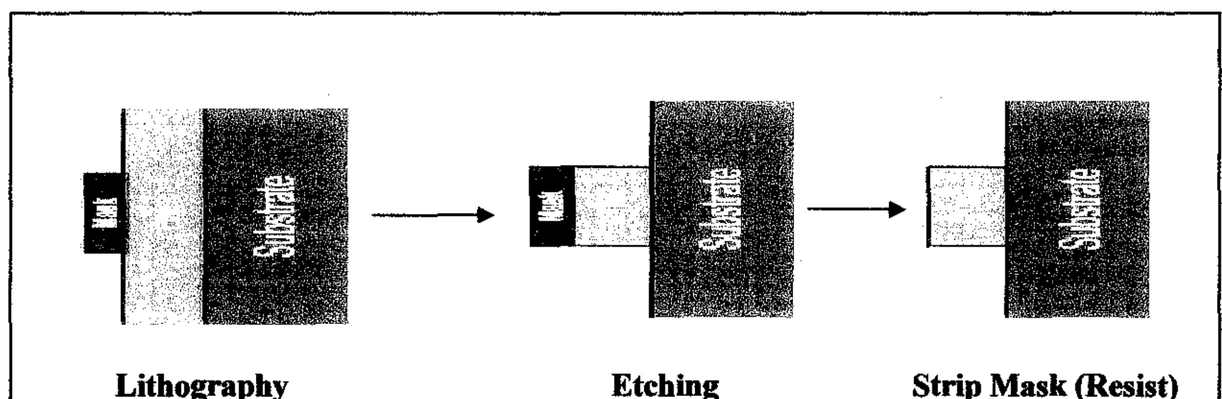


Figure 2.7: Flow of the etching process

2.2.3 Diffusion and Ion Implantation

- In diffusion step, semiconductor surface which is not protected by the oxide is exposed to a source light concentration of opposite-type impurity.
- By a solid state diffusion, the impurity moves into the semiconductor crystal.
- In ion implantation, the intended impurity is introduced into the semiconductor by accelerating the impurity ions to a high energy level and then implanting the ions in the semiconductor.
- SiO2 layer serve as a barrier to impurity diffusion or ion implantation.
- p-n junction will be formed after diffusion or ion implantation process.

2.2.4 Metallization

- Metallization is used to form ohmic contacts and interconnections.
- Metal film can be formed by physical layer deposition or chemical vapour deposition.
- The photolithography process is again used to define the front contact.
- A similar metallization step is performed on the back contact without using a lithography process.
- Normally, a low temperature (< / = 500 °C) anneal would also be performed to promoted low-resistance contact between the metal layer and the semiconductor.
- Procedure for metallization process are as follow:

  - ➢ Wet chemical roughen the dielectric layer. Refer to figure 2.8.
  - ➢ Electrodes plate using Cu seed layer. Refer to figure 2.9.
  - ➢ Apply photoresist, dry bake. Refer to figure 2.10.
  - ➢ Photo-expose, develops, and post cure. Refer to figure 2.11.
  - ➢ Pattern-plate the Cu. Refer to figure 2.12
  - ➢ Strip the photoresist. Refer to figure 2.13
  - ➢ Etch the seed Cu layer. Refer to figure 2.14

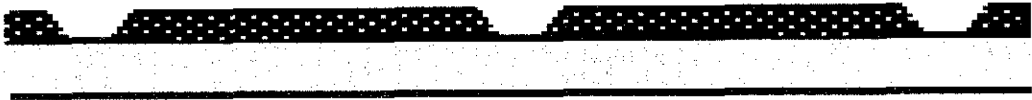


Figure 2.8: Wet chemical roughen dielectric layer

Figure 2.9: Electrodes plate using Cu seed layer

Figure 2.10: Photoresist (dry bake)

Figure 2.11: Photo expose, develops, and post cure

Figure 2.12: Pattern plate (Cu)

Figure 2.13: Strip the photoresist

Figure 2.14: Etch the seed Cu layer

-Refer to table 2 for the type of chemicals use in metallization process.

Process	Chemicals
Swell	Propylene Carbonate
Etch	Permanganate – based
Neutralizer	H_2O_2
Pre- Catalyst	$SnCl_2$
Catalyst	Palladium
Electrodes Plating	Copper Salt + Formaldehyde

Table 2: Chemicals used in metallization

Modification to all this fabrication process will result in modified new structure of the IGBT. Not the whole process will be modified. Only the parameter involves in all of this process will be modified in order to evaluate whether the performance of the devices will improve or not. Student must investigate first the effect consequences of the devices performance before and after changing any parameter of the devices.

2.3 IGBT OPERATION

2.3.1 IGBT Blocking Operation

Refer to figure 2.8 for the references of the discussion in this part. The on/off state of the device is controlled by the gate voltage (V_G). If the voltage applied to the gate contact, with respect to the emitter, is less than the threshold voltage (Vth), then no inversion layer is created and the devices is turned off. In this case, any applied forward voltage will fall across the reversed biased junction J2. The only current to flow will be a small leakage current. The forward breakdown voltage is therefore determined by the breakdown voltage of this junction. This is an important factor for power devices where large voltages and currents are being dealt with. The breakdown voltage of the one sided junction is dependent on the doping of the lower-doped side of the junction. Refer to figure 2.8, the lower doped side of the junction is the n^- side. This is because the lower doping results in a wider depletion region and thus a lower maximum electric field in the depletion region. For this reason, the n- drift region is doped much lighter than the p-type body region. The n+ buffer layer is often present to prevent the depletion region of junction J2 from extending right to the p bipolar collector. The inclusion of this layer drastically reduces the reverse blocking capability of the device. This is dependent on the breakdown voltage of junction J3 which is reversed biased under reverse voltage condition. The benefit of this buffer layer is that it allows the thickness of the drift region to be reduced, thus reducing on state losses.

2.3.2 IGBT On-state Operation

The turning on of the devices is achieved by increasing the gate voltage (V_G) to make it greater than the threshold voltage (Vth). This will result in an inversion layer forming under the gate which provides a channel linking the sources to the drift region of the device. Electrons are then injected from the source into the drift region. At the same time, junction J3 which is forward biased will injects the holes into the n^- doped drift region. Refer to figure 2.9 for the flow of electrons and holes during on state operation.

This injection causes conductivity modulation of the drift region where both the electron and hole densities are several orders of magnitude higher than original n^- doping. This conductivity modulation gives the IGBT its low on state voltage because of the reduced resistance of the drift region. Some of the injected holes will recombine in the drift region. Others will cross the region via drift and diffusion and will reach the junction with the p-type region where they will be collected. Therefore, we can consider the operation of the IGBT like a wide-base pnp transistor whose base drive current is supplied by the MOSFET current through the channel.

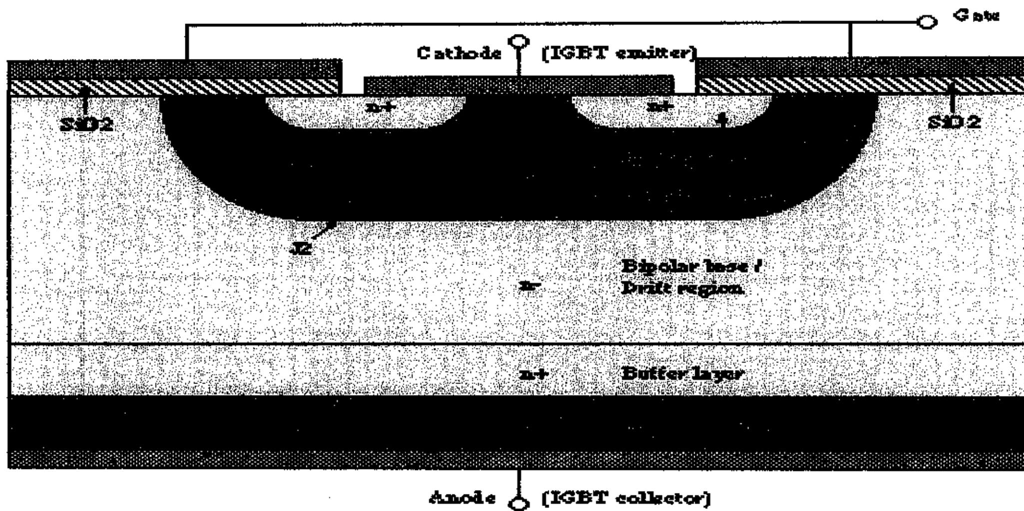


Figure 2.8: Full cell of the IGBT structure

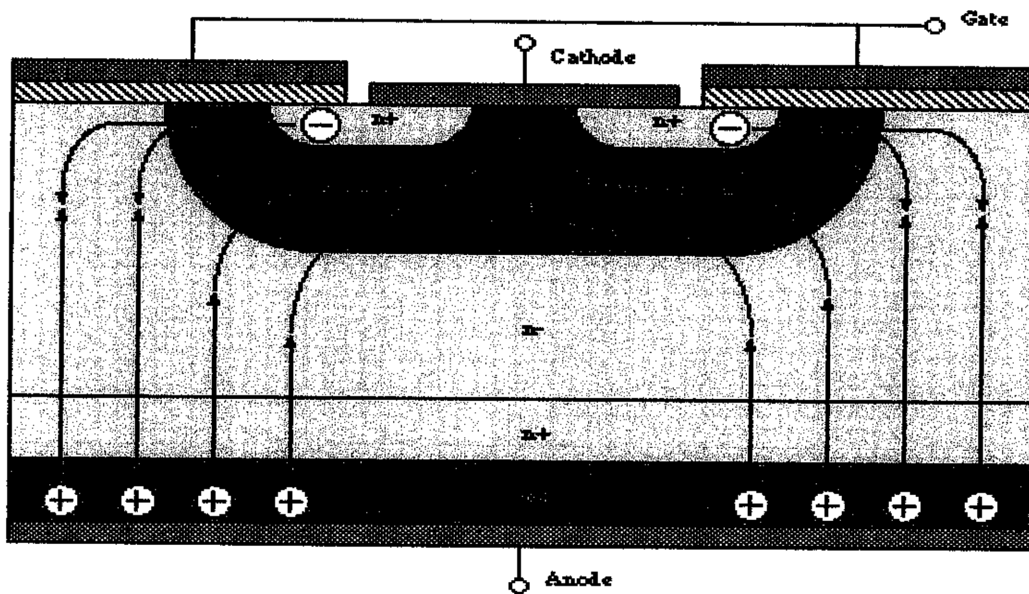


Figure 2.9: Flow of electrons and holes during on state operation

CHAPTER 3

METHODOLOGY AND PROJECT WORK

3.1 PROCEDURE

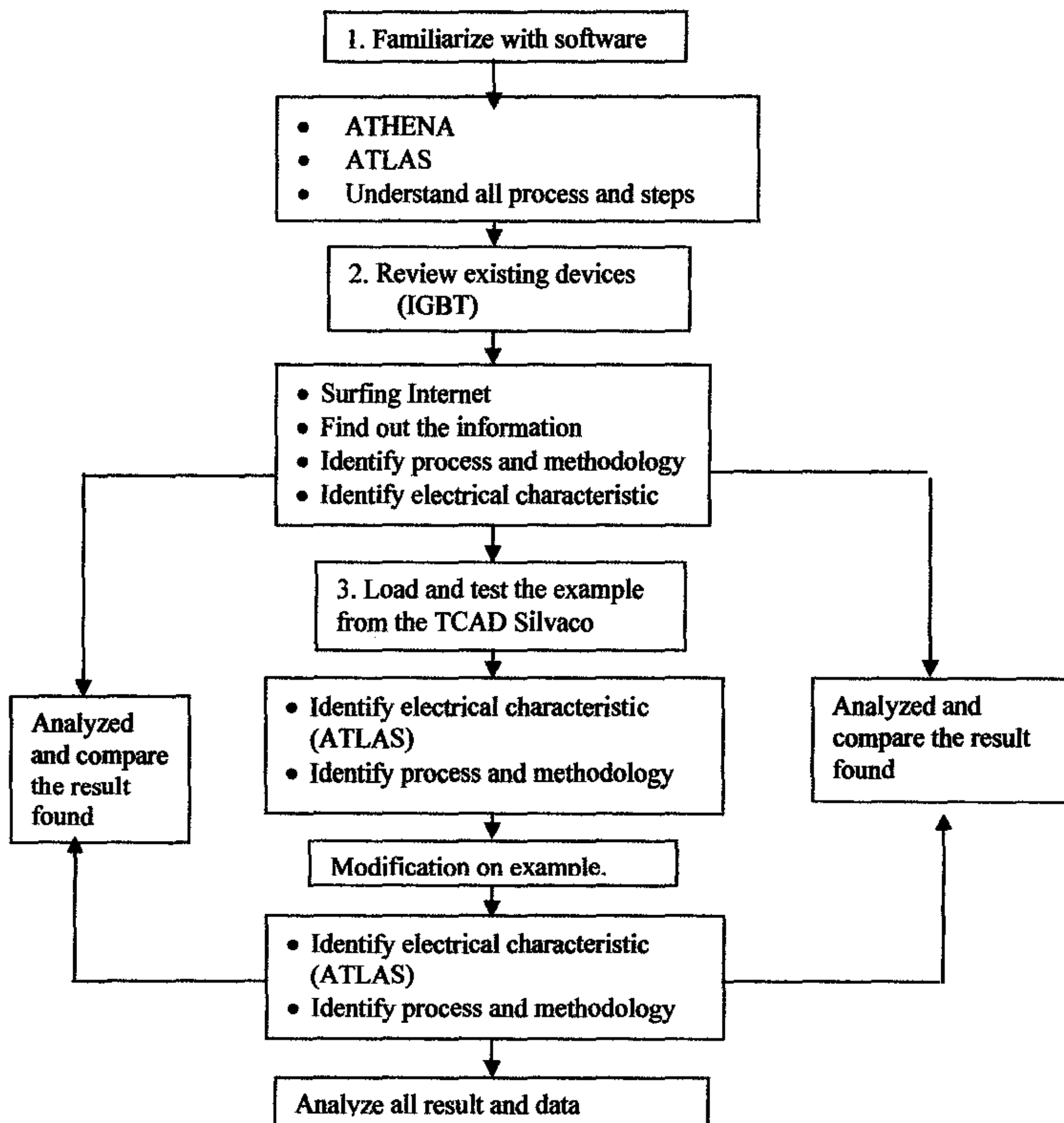


Figure 3.1: Project Flow Diagram

Figure 3.1 shows the project flow diagram which represents the complete process flow of the project. The current stage of this project is identifying electrical characteristic and devices process methodology for the modified IGBT and standard IGBT used in industry. This stage will be repeating until student gets the improve performance of the modified IGBT compared to standard IGBT used in industry.

3.1.1 Familiarize with the Software

Silvaco TCAD workshop tools consist of the ATHENA and ATLAS simulator. . ATHENA and ATLAS simulator are used for different purpose where the ATHENA is used in creating the device structure where the materials, width and concentration are defined. On the other hand, ATLAS simulator is used in testing the device structure created in ATHENA. Device electrical characteristics can be analyzed in ATLAS simulation both in term of data measurement and graphical approach.

The exercise and practice have been done in the SILVACO TCAD workstation by getting started with the software through the creating a basic NMOS device structure using ATHENA. The example available in the workstation also reviewed in order to get an idea how the semiconductor device structure looks like. After the structure is created in ATHENA, its electrical performance is tested in ATLAS simulation and the characteristics curve is displayed. Four weeks are allocated in familiarize the software.
Basic operations required for creating a typical NMOS input file from [5]:

i. Developing a good simulation grid
ii. Performing conformal deposition
iii. Performing geometric etches
iv. Performing oxidation, diffusion, annealing and ion implantation
v. Structure manipulation
vi. Saving and loading structure information.

3.1.2. Review on the Existing Device Structure

All the information about the IGBT was discovered through the literature review about the current issue and current data on existing devices that available in market. All of this information can be used as a reference in completing this project. Journals and articles are mostly found by searching in the internet through IEEE websites. All the data and finding was recorded for comparison purpose between the results of the project.

Some example on IGBT in SILVACO TCAD workstation will be reviewed and studied. Electrical characteristic of the reviewed example will be identified through the ATLAS simulation and structuring process of the devices can be identified through the ATHENA simulation. Every structure and process will be covered so that the modification can be done to the available structure in the workstation.

The next step of the project is to play around with the example available in the workstation by study the effect of the performance when the structure parameters are changed i.e.:

i. Drift length
ii. Trench depth
iii. Trench width
iv. Gate length
v. Channel length.
vi. Material Concentration

The device electrical characteristics will be tested again after the modification and the results obtained will be compared with both the standard existing commercial device performance and the initial device from the example in the workstation. The characteristics performance will be triggered in term of data measurement and graphical representation. [4]

3.1.3 Load and Test Available Example in the Sun Microsystem Workstation.

In this step, the available example which exists in the Sun Microsystem workstation was load and run to get the structure and electrical characteristic of the IGBT. The example that was loads and run through the system is about the IGBT transient latch up with lattice heating. This load example shows the following result:

- Definition of IGBT structure using ATLAS.
- IGBT collector steady state solution at 300V.
- Transient gate voltage ramp to produce latch up.

From this example, student can analyze the structure, electrical characteristic and the process fabrication step of the IGBT. All the result of this example can be reviewed in chapter 4 (Result and Discussion section)

3.2. Tool Required

i. **Silvaco TCAD workstations.**
ii. **Silvaco ATHENA simulation software** – To predict the physical structure of the device that result from processing.
iii. **ATLAS simulation software** – To predict the electrical characteristics associated with specified bias conditions

CHAPTER 4

RESULT AND DISCUSSION

4.1. Creating an NMOS Device Structure Using ATHENA

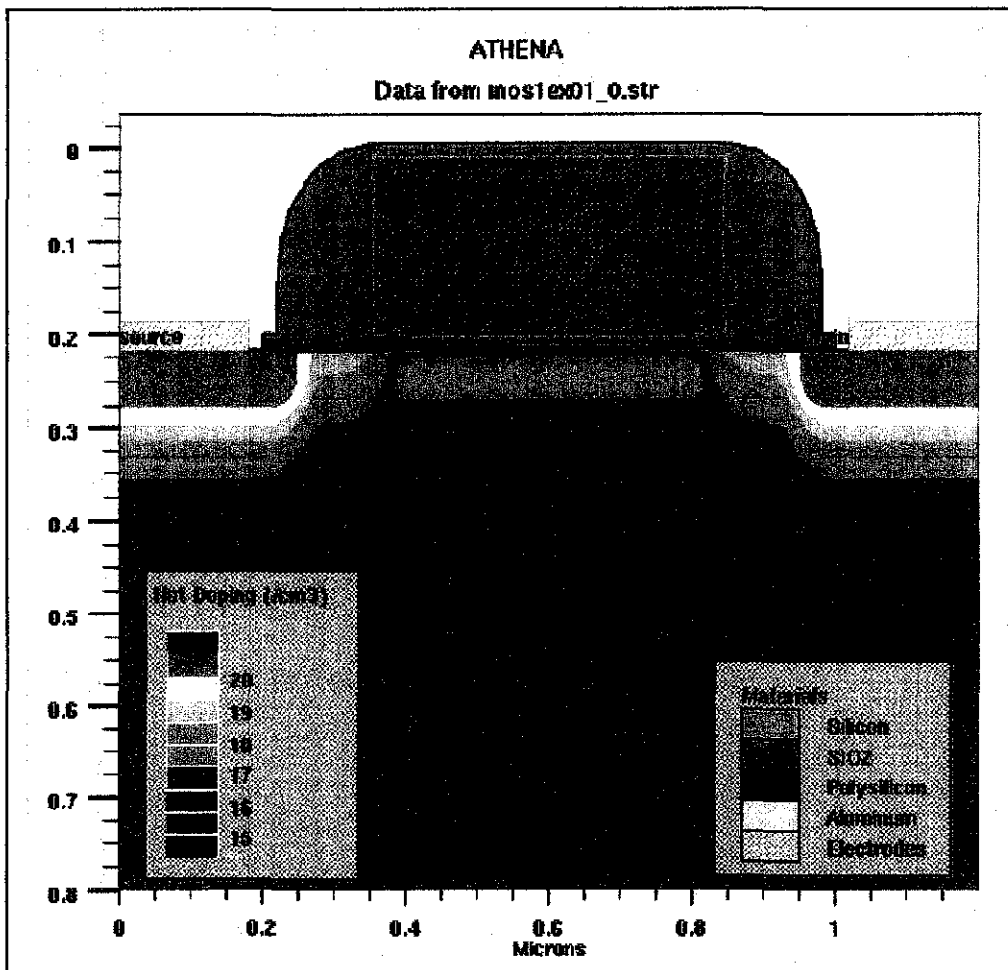


Figure 4.1: Full NMOS Structure

Figure 4.1 show the result of the workstation practice during familiarization period with the software. During familiarization, we were exposed to design process of the NMOS structure. During structuring process, only half of the NMOS structure was created. Since the right side and left side of the structure are the same, we just mirroring the image of the half structure of NMOS. The, the result of mirroring the image of the half structure of NMOS is the full NMOS structure shown in figure 4.1. This device structuring process was done by using the ATHENA simulator. Silvaco ATHENA analysis allows for the calculation of resultant impurity concentrations, layer thickness, and much ore for processes such as oxidation, diffusion, implantation and deposition for temperatures above 800 C. Refer to **Appendix B** in appendices section for the ATHENA program that is used in creating the NMOS devices structure during software familiarization practice.

4.2. Electrical Characteristic Prediction Using ATLAS

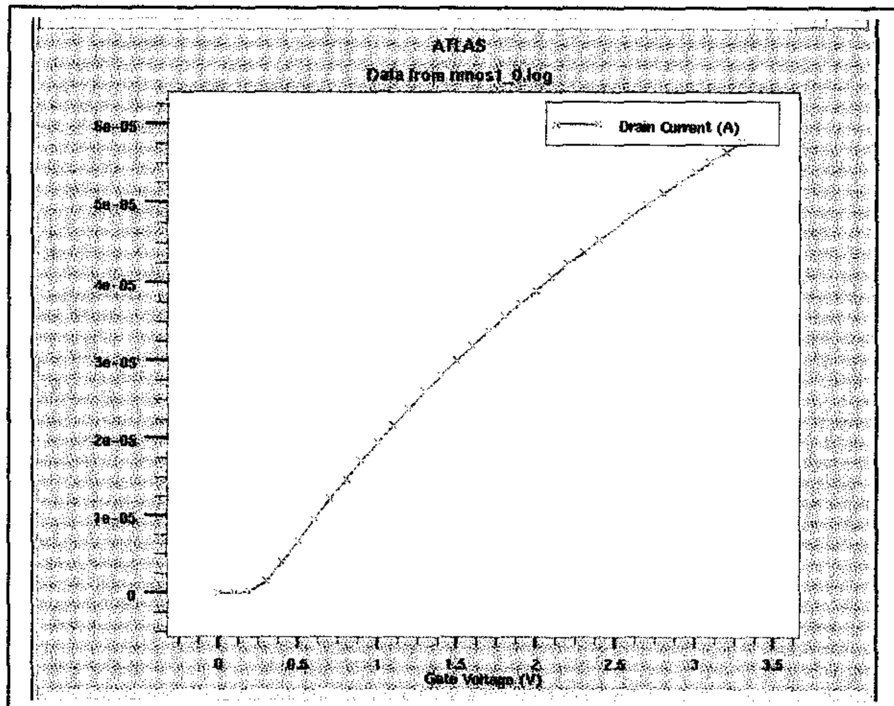


Figure 4.2: Plot of Id versus Vgs for NMOS devices

Figure 4.2 shows the characteristics curve of Id versus Vgs for the NMOS device structure created in the workstation practice. The curve was plotted by using the following command:

Solve name=gate vgate=0 vfinal=3.3 vstep=0.1

According to the command, the simulator will ramp the gate voltage from 0V to 3V with the bias size of 0.1V. The curve represents the relationship between drain current, Id and gate-source voltage, Vgs.

By using some command in the ATLAS simulator, we can create family of curve of one result. Meaning that, if we want to compare the performance of the same devices but with different value, we can easily compare the result by looking at the family of curve. Below are the special commands that can be used to produce the family of curve in ATLAS simulator.

```
Log off
Solve vgate=1.1 outfile=solve1
Solve vgate=2.2 outfile=solve2
Solve vgate=3.3 outfile=solve3
#
Load infile=solve1
Log outf=nmos2_0.log
Solve name-drain vdrain=0 vfinal=3.3 vstep=0.3
Solve init
Log outf=nmos3+0.log
Solve name=drain vdrain=0 vfinal=3.3 vstep=0.3
Tonyplot –overlay nmos2_0.log nmos3_0.log nmos3_0.log –set nmos.set
Quit
```

Figure 4.3 shows the family of curve of Id versus Vgs that was generated by using the above command for NMOS device. This kind of graph representation gives a very useful method for us in interpreting the same kind of performance of the devices

but with difference values. This command is very useful to student in order to predict the same performance of the device (IGBT), but with different value. From this kind of graph, student are able to predict whether increasing or decreasing the value that are being investigated will result in an improve performance or not.

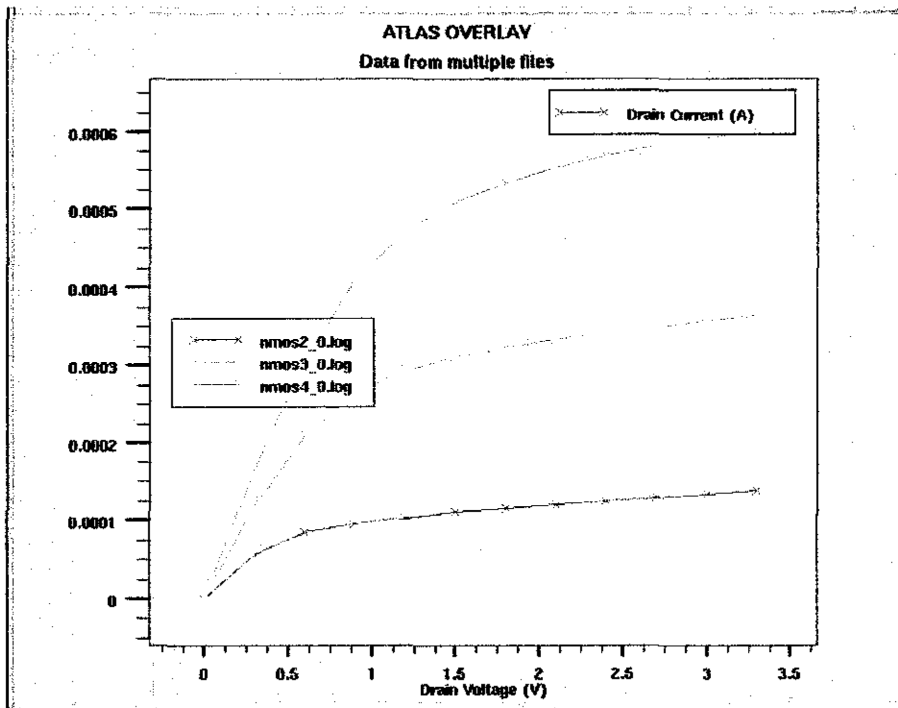


Figure 4.3: Family of curve of Id versus Vgs that was generated for NMOS.

* Refer to **Appendix C** in appendices section to see the program for ATLAS simulation in interpreting the electrical performance of the NMOS.

4.3 CREATING IGBT STRUCTURE

The standard IGBT structure is already available in the Sun Microsystem. Standard IGBT structure can be create by loading the available example in the workstation. IGBT example falls under power devices group. Student has already loaded the available example in order to extract the standard IGBT structure for this project purpose. Refer to figure 4.4 for structure of the standard IGBT. From figure 4.4, only half cell of the IGBT structure is shown. From literature review, student found that the structure of the IGBT is similar for the right hand side and left hand side. Since the structure of the IGBT is same for right and left side, Sun Microsystem workstation only generate half cell of the IGBT structure. Full cell of the IGBT can be obtained by key in the mirroring command that was use during NMOS fabrication practice. The full structure of the standard IGBT can be reviewed in figure 2.8.

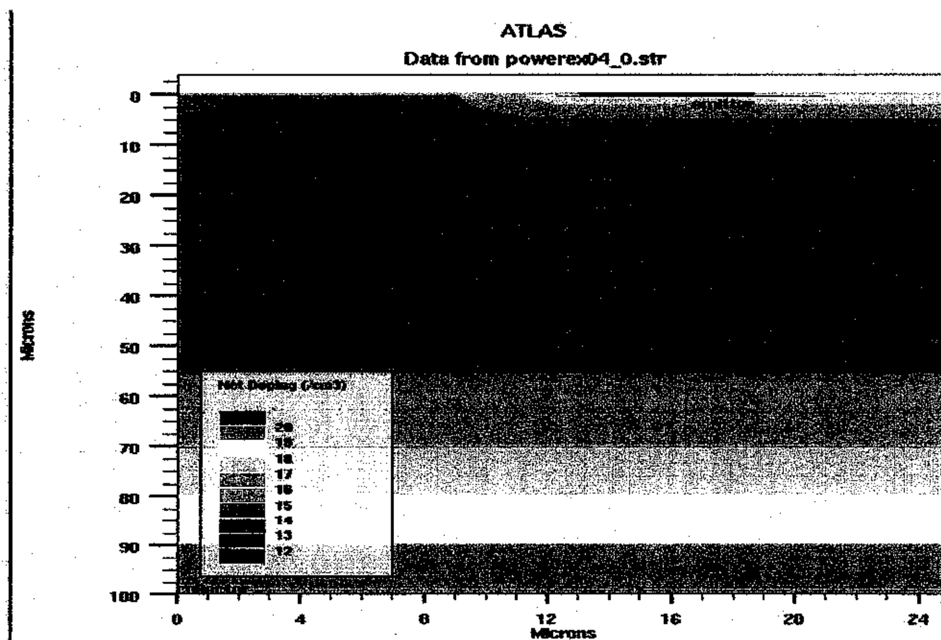


Figure 4.4: Half cell structure of the standard IGBT

Student was compared the differences between figure 4.4 and figure 4.1. The structures between these two devices are totally difference. Figure 4.1 is NMOS structure and figure 4.4 is IGBT structure. They supposed to be different. From this comparison,

student has identified that NMOS structure was implemented using ATHENA software and IGBT structure was implemented using ATLAS software. From literature review and software familiarization period, student found that, the structure of the devices should be implemented using the ATHENA software. After loading the IGBT example, student found that the programmer was implemented the structure of the IGBT using ATLAS software. This phenomenon gives a big problem to the student in order to modified the structure of the IGBT. Since the IGBT example was loaded using ATLAS software, the structure file of the IGBT did not presented. Devices structure file will be available if the device is implemented using ATHENA software.

In chapter 3, student was declared that modification step will be proceed after loading the available example in the Sun Microsystem workstation. From literature review and software familiarization process, student found the modification to the device can only be implemented by changing certain device parameter in the structure file. During NMOS fabrication process, student has performed try and error process in order to see the result of changing certain parameters of the NMOS structure. Changing the parameters will affect the performance of the device. This is the main objective of this project. Student is required to modify the structure of the standard IGBT and analyses the electrical performance of the devices. Constructing a new structure of the devices step by step are time consuming and very complicated process. Since student did not have any basic background about the semiconductor fabrication process and software, student only required to modify the structure of the devices that already available in the workstation. Since the structure file of the IGBT did not available in ATHENA mode, no modification can be made to the existing IGBT structure. Student has tried to change the parameter in the program to see the result of modification. Changing the parameter in the program and loading it again only result in the error of the simulation. This is the main problem that student was faced up during conducting this project.

4.4 ELECTRICAL PERFORMANCE EVALUATION OF THE LOADED EXAMPLE

The result of the loaded example is about the transient behavior of the device. This is the direct result of the loaded example that was run under ATLAS mode. In electrical and electronic engineering, transient is declared as a sudden change of steady state voltage, current, or load. These sudden changes are mostly found as the result of the operation of switching devices. Turn ON time of the IGBT is quite fast, but the turn OFF time can be slow because of the open base of the PNP transistor during the turn OFF period. Refer to figure 4.5 for the transient behavior of the standard IGBT (result from loaded example).

From part 2.3.2, student understands that the electrons are injected from the n-region into the p-region and holes are injected from p-region into n-region during forward bias. During this operation, the minority carrier distributions lead to current flow and to store the charge in the p-n junction. The stored charged effect the junction capacitance and the transient behavior of the p-n junction due to sudden changes of bias. For switching application, the forward-to-reverse bias transition must be nearly abrupt and the transient time short. Student must understand that the transient behaviors represent the switching characteristic of the device. Reducing the transient time will increase the switching speed of the devices and vice versa [3]

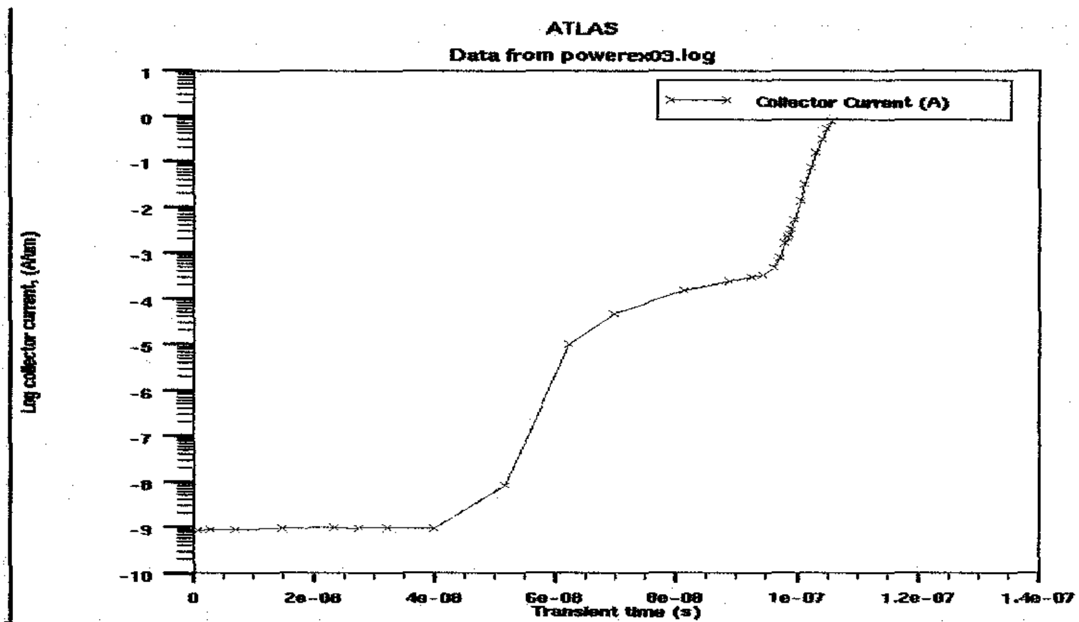


Figure 4.5: Transient behavior of the standard IGBT

The transient time may be estimated as follows. Under the forward bias condition, the stored minority carriers in the n-region for a p^+-n junction is given as follow:

$$Q_p = \tau_p J_p = \tau_p \frac{I_F}{A}$$

Where:

I_F = total forward current

A = device area

If the average current flowing during the turn-off period is $I_{R,\ ave}$, the turn off time is the length of time required to remove the total stored charge Q_p:

$$t_{off} \cong \frac{Q_p A}{I_{R,ave}} = \tau_p \left(\frac{I_F}{I_{R,ave}} \right)$$

The turn of time depend on both the ratio of forward to reverse currents and the lifetime of the minority carriers. For fast switching devices, we must reduce the lifetime of the minority carriers [3].

4.5 MODIFYING IGBT STRUCTURE

Since the structure file of the IGBT did not available because the loaded example was run using the ATLAS software, student has struggle to find the solution. Fabricating devices structure step by step is very complicated and time consuming. This matter has been discussed with the supervisor, Dr. Norani Muti Mohamed in order to precede this project. Modifying the structure means changing the devices parameter in the structure file and the result will be changes in the electrical performance of the devices. Supervisor has suggested to do study on other issues on IGBT that available in the internet as a backup for this project. At the same time, supervisor is looking for the solution from the industrial people about this matter. At the end of this project period, supervisor has got the file which enables us to do some modification to the devices structure. Since the time is very limited due to limited lab access and lot of project to be done through the semester, student cannot concentrate more on modifying the devices. This is because, before this, student is more concentrating with the study on other issues on IGBT. Student was complete some modification to the devices structure in order to see the resulting changes. This modification is concentrating on modification of the doping concentration of the structure and resulting transient behavior was investigated. Refer to figure 4.6 for the modified structure of the IGBT and figure 4.7 for the resulting transient behavior of the IGBT after modification.

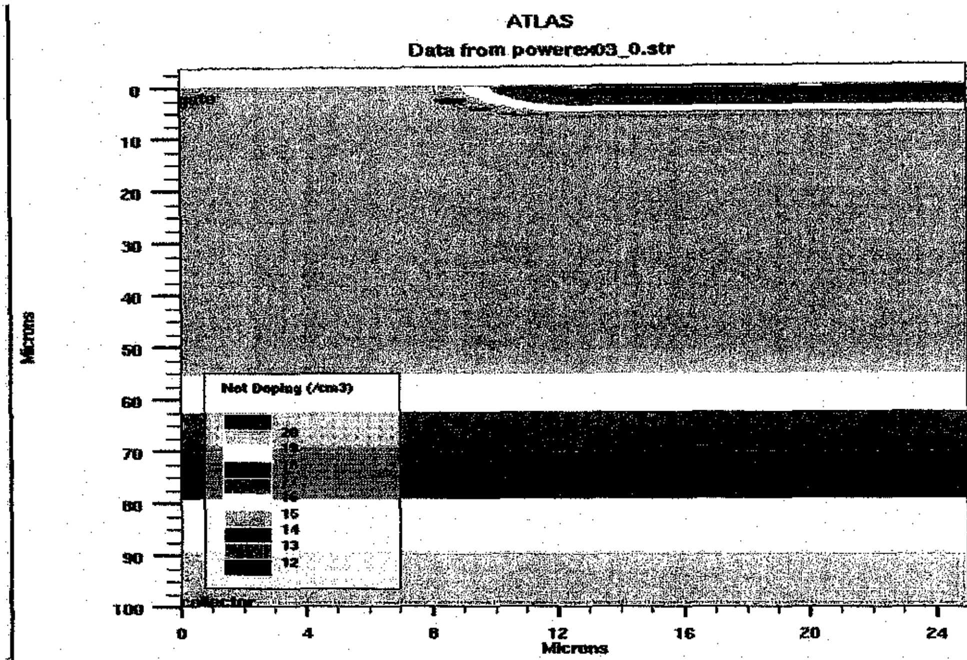


Figure 4.6: IGBT structure after modification

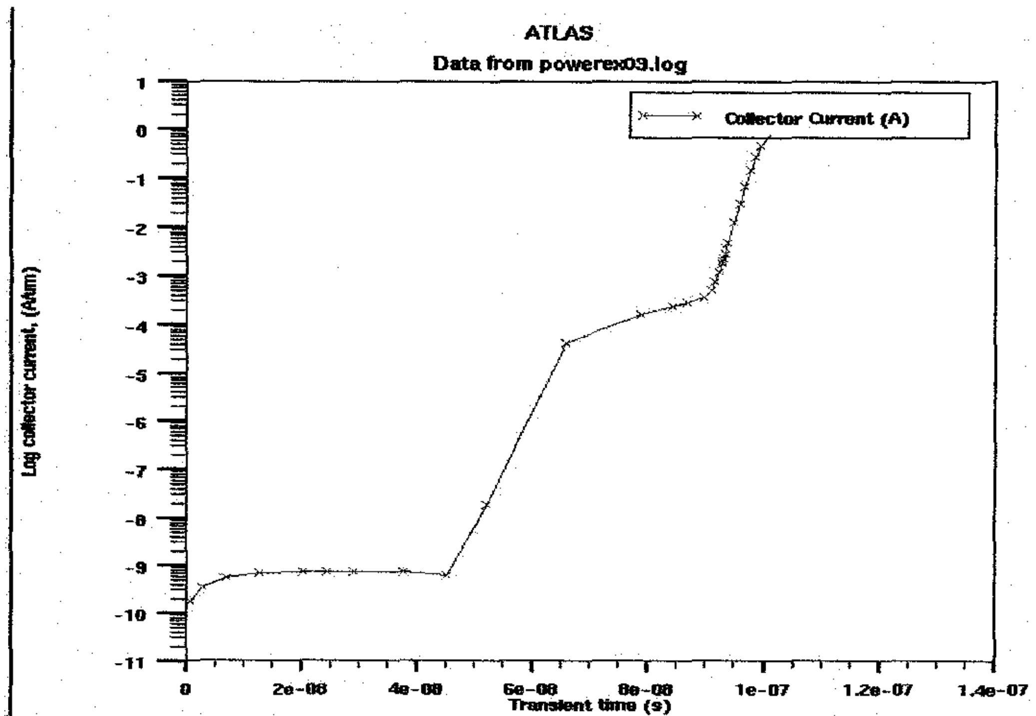


Figure 4.7: IGBT transient behavior after modification

Modification that was done to the IGBT structure is modification to the doping concentration of the buffer layer. This IGBT structure is a Punch Through IGBT structure because the buffer layer is presence on top of the p+ layer. Modification was done by increasing and reducing the doping concentration of the buffer layer. The result that was captured during modification and simulation are the same for increasing and reducing the doping concentration. Comparing figure 4.4 and 4.6, we can see a little changes in the buffer layer thickness for modified structure compared to standard structure. For the resulting transient behavior, not so much changes happen. The resulting transient time after modification is not so much changes compared to standard IGBT. Since the time is very limited, supervisor suggests the student to continue on the study of another issue about the IGBT. In this case, student was concentrating on the study on the way to reduce the EMI effect of the IGT. Section 4.6 will describe briefly about the study that was done by the student.

Please refer to **Appendix D** in apendices section for the standard IGBT datasheet and performance that available in industry. Refer to **Appendix E** in appendices section for the guideline in choosing the right IGBT for future references.

4.6 STUDIES ON REDUCING EMI EFFECT OF THE IGBT

Since modification to the IGBT structure cannot be done as expected, student was suggested by the supervisor to do a case study on the improvement of the IGBT. in this studies, student is concentrating on studying the way to reduce the EMI effect of the IGBT. In this study, student was considering a Quick Punch Through (QPT) IGBT design concept to reduce EMI. The concept of Punch Through (PT) IGBT has been covered in chapter 2. From the literature review [6], the PT IGBT generates more EMI compared to MOSFET. IGBT is a two carrier device and its switching characteristics being controlled by the gain of the p-n-p bipolar. This nature of the IGBT has results the PT IGBT to generate more EMI than MOSFET. Actually, EMI is the result of the abrupt turn off di/dt. QPT IGBT can be achieved by designing the Punch Through (PT) IGBT with a thinner lower concentration drift region [6]. Reducing drift region concentration will allow the depletion layer to punch through to the buffer at lower voltage. Capacitance of the QPT IGBT also needs to be optimized. This is to make sure that the channel remains open until the collector voltage reaches the bus voltage. This will provide the control ability and thereby minimize the turn-off di/dt [6].

Actually, reducing the di/dt comes with a penalty. The penalty in reducing the di/dt is the increased in turn off losses (E_{off}). If we compare between the PT IGBT with the MOSFET, PT IGBT have lower conduction losses and higher switching losses than MOSFET. IGBT EMI is higher due to abrupt di/dt during turn off [6]. Figure 4.8 below show the turn off waveform for the typical PT IGBT. IGBT can be designed to provide low di/dt and collector over-voltage during turn-off [6]. Refer to figure 4.9 for the typical Non-Punch Through IGBT simulated turn off waveform.

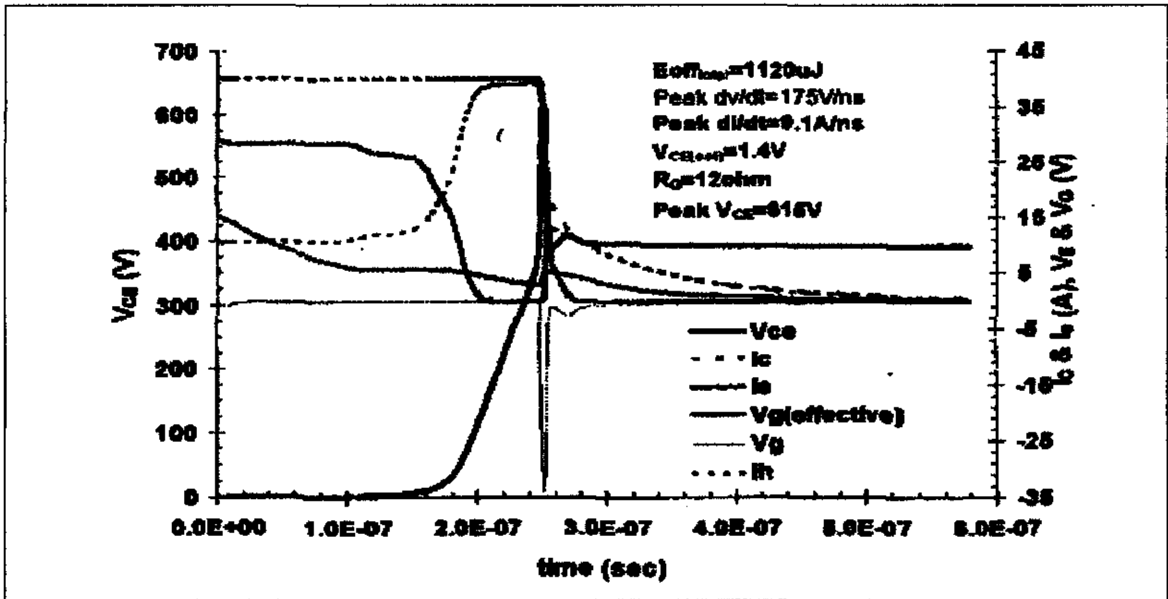


Figure 4.8: Turn Off waveform for the typical PT IGBT

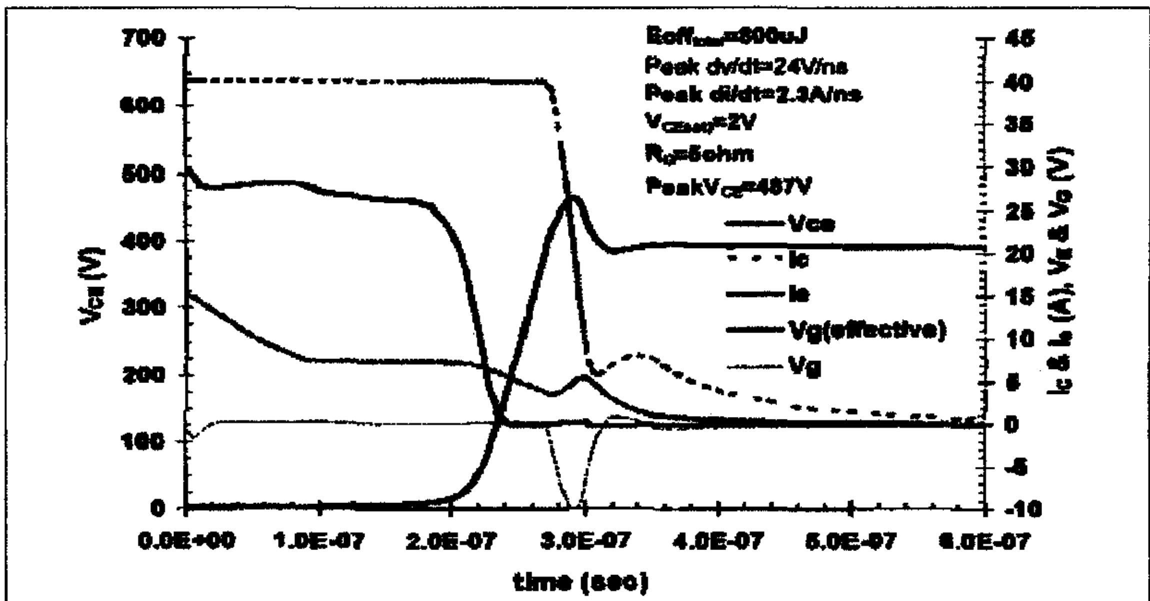


Figure 4.9: Turn Off waveform for typical NPT IGBT

4.6.1 Study on QPT Inductive Turn – Off

The measured turn-off waveform for the QPT IGBT can be viewed in figure 4.10 below.

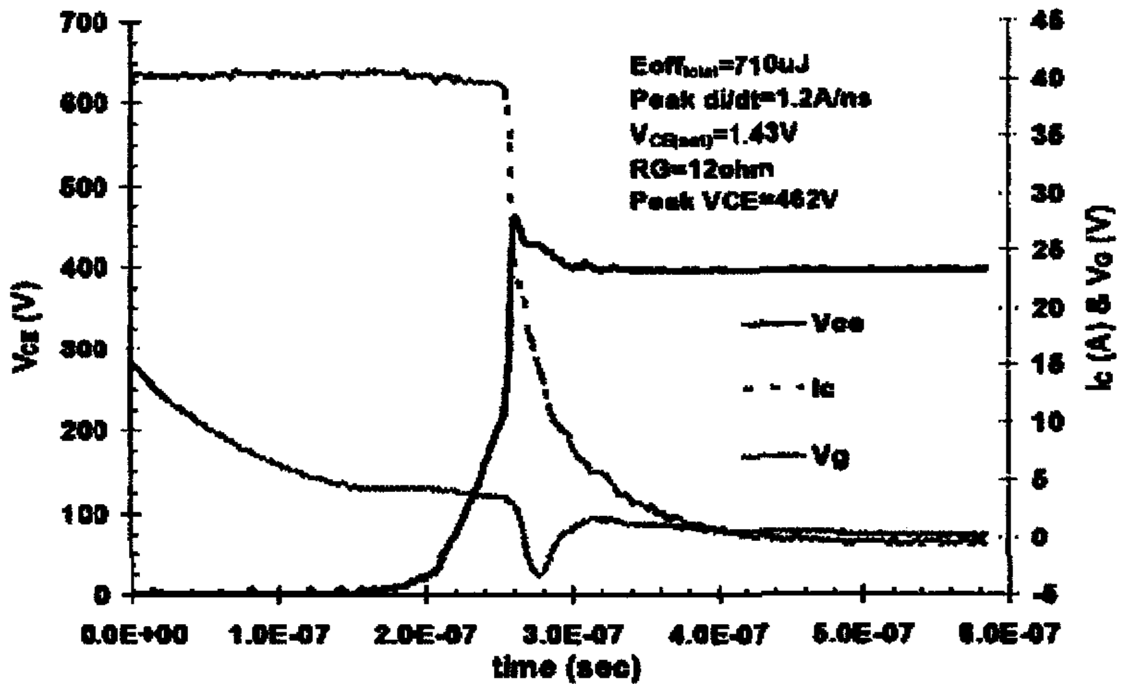


Figure 4.10: Turn off waveform for the QPT IGBT

This QPT did not fully optimized yet, but we can see from the graph the smooth current fall and minimization of the Vce overshoot. The fully optimized QPT IGBT turn off waveform can be viewed in figure 4.11.

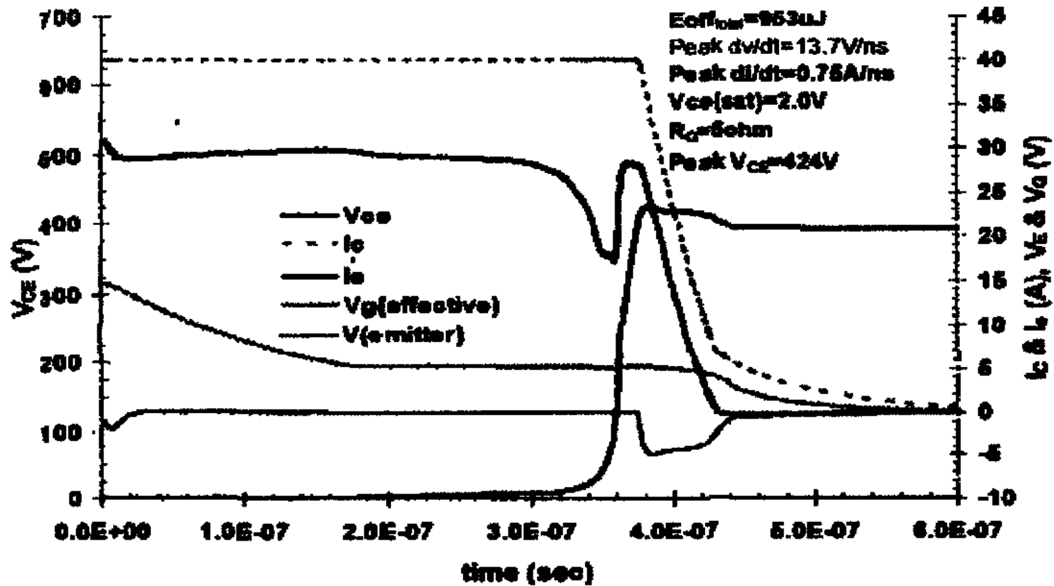


Figure 4.11: Fully Optimized QPT IGBT Turn Off waveform

The threshold voltage V_{TH} of the QPT IGBT is 3.5 V. The QPT IGBT dv/dt during turn off is similar to that of MOSFET. This dv/dt generates a displacement current that aids in sustaining the $V_{G\ (effective)}$. In order to make sure the QPT $V_{G\ (effective)}$ is maintained at a voltage above the V_{TH} during the rise in V_{CE}, the capacitances have been optimized. From figure 4.11, we can observe that the QPT gate is ON and Ie continues to flow during the current fall. This is similar to the MOSFET characteristic. The initial di/dt during the current fall also same as MOSFET. See figure 4.12 below for the MOSFET characteristic to be compared with the QPT IGBT in figure 4.11.

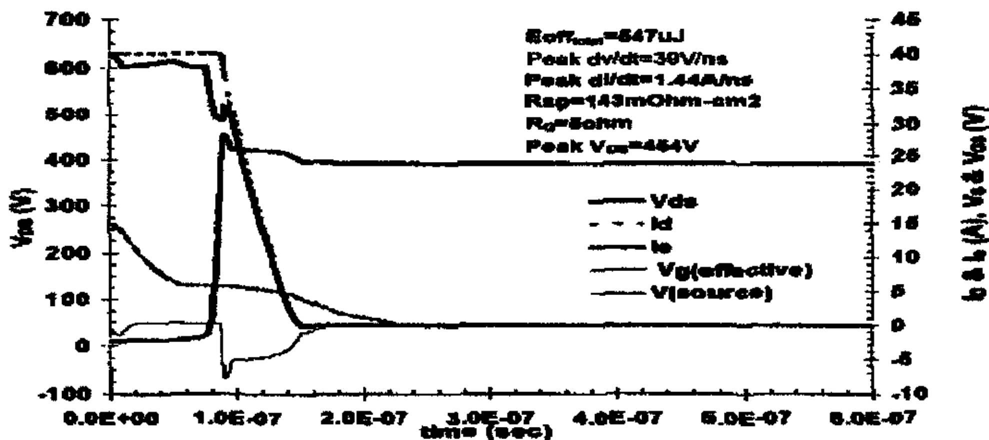


Figure 4.12: MOSFET turn off waveform characteristic

The difference between the QPT and MOSFET turn off occurs at the end of the current fall. See figure 4.11 and 4.12 to locate the differences. The QPT tail current is generated by the recombination of holes in the N buffer and increases E_{off}. Further optimization of the buffer will result in lowering the QPT E_{off}. As a result, QPT will have a lower maximum operating frequency than a MOSFET. However, the QPT has a lower 125oC conduction drop ranging from 1.4 to 2.0 making it more suitable for frequencies less than 100 kHz. The advantage of maintaining the flow of Ic until after Vce reaches the bus voltage is dynamic avalanche suppression and preventing failure due to non uniform turn off. [7].

Lastly, from this study, student understands that QPT design can be achieved by making changes in the conventional PT IGBT vertical structure and design. QPT has been shown to obtained gate controllable turn – off di/dt similar to MOSFET. This QPT design can be achieved without adding any additional process or complexity to the IGBT wafer fabrication process. The QPT low turn off di/dt provides for lower EMI while maintaining a good $V_{ce(sat)}$ versus E_{off} trade-off. An additional advantage of reducing the turn off stress on the QPT is obtained by maintaining the channel open until after V_{ce} reaches the bus voltage.

CHAPTER 5

CONCLUSION

After completing this project, student has gain lot of knowledge about the semiconductor fabrication process. The most important knowledge that was gain through this project is about the designing and simulation of the IGBT fabrication process. Throughout this project, student can conclude that most of the project objective was achieved but some of the project objective cannot be done due to technical problem. After two semesters conducting this project, student was familiarizing with the semiconductor fabrication software which is ATHENA and ATLAS. Student also has successfully loaded the available example in the workstation and interprets the electrical performance of the standard IGBT. Due to technical problem, modification to the device cannot be done throughout the project since. Until the end of project period, student is unable to come out with the new (modified) IGBT structure with an improve performance. The last objective of this project which is come out with the comparison data between the conventional IGBT and modified IGBT also cannot be achieve due to that technical problem. Although some of the project objective cannot be achieved throughout the project period, student has performed a study about the design of the Quick Punch Through IGBT in order to reduce the EMI effect. Hopefully, this study will be useful for the student for future references.

RECOMMENDATION

Since some of the objective cannot be achieved due to the technical problem, student recommends that this project can be continuing in the future. Before starting this project, any student who are going to further this project must at least have a basic background about the semiconductor fabrication. That student also must be able to construct the structure of the IGBT step by step using the ATHENA software although this process is very complicated and time consuming. This file structure is the core thing in order to achieve the last two objectives of this project which is not achievable in this project. Hopefully, those who are continuing this project in the future will be able to come out with the new modified IGBT structure with an improve performance. This project is very useful to those who are planning to join the semiconductor fabrication company in the future. Hopefully, the committee of the Final Year Project will continue this project in the next semester for another student who is going to do their final year project.

REFERENCES

[1] Jack Takesuye and Scott Deuty, Motorola Inc, September 2000 (**Introduction to Insulated Gate Bipolar Transistors**)

[2] Mohsen A.Hajji , B.S in EE., University of Pittsburgh, 1988, M.S in EE, University of Pittsburgh, 1996 (**A Transient Model For Insulated Gate Bipolar Transistor IGBT**)

[3] S.M.Sze : " **Semiconductor Devices Physics and Technology**" 2nd edition (pp 169 172)

[4] Gary S. May, Simon M. Sze.; "Basic Fabrication Step," in *Fundamental of Semiconductor Fabrication,* Wiley International Edition. USA: John Wiley & Sons, pp. 11-14, 2004.

[5] *TCAD workshop using SILVACO TCAD TOOLS,* Volume I and II, SILVACO International

[6] J.Yedinak, J. Gladish, B.Brockway, S.Shekhawat, P. Shenoy, D. Lange, G.Dolny, M.Rinehimer: "A **600V Quick Punch Through (QPT) IGBT Design Concept for Reducing EMI**", Discrete Power Product Development, Fairchild Semiconductor Corporation, USA.

[7] Petra Rose, "Investigation on the Stability of Dynamic Avalanche in IGBTs", ISPSD'02, pp 165 - 166

APPENDICES

Appendix A

PROJECT GANTT CHART FOR FYP1

No.	Detail/ Week	1	2	3	4	5	6	7	8	9	10	11	12	13	14	SW	EW
1	Project proposal preparation																
	- Research work																
2	Preliminary Research Work																
	- SILVACO TCAD Tools Workshop																
3	Submission of Preliminary Report																
4	Project Work																
	- Perform structure specification																
	- Perform material model specification																
5	Submission of Progress Report																
6	Project work continue																
	- Identify the existing Device																
	- Modification on the device available																
	- Complete results analysis																
7	Submission of Interim Report																
8	Oral Presentation																

Legend: **SW**: Study week **EW**: Exam week

PROJECT GANTT CHART FOR FYP 2

No.	Detail/ Week	1	2	3	4	5	6	7	8	9	10	11	12	13	14	SW	EW	JUN
1	Continue on project research - Research work																	
2	Continue working with the software - SILVACO TCAD Tools Workshop																	
3	Submission of Progress Report 1																	
4	Project Work - Locating standard IGBT parameter																	
5	Submission of Progress Report 2																	
6	Project work continue																	
	- Identify the existing Device																	
	- Modification on the device available																	
	- Study on QPT IGBT																	
7	Submission of Draft Report																	
8	Submission of Final Report Softcover																	
9	Submission of Technical Report																	
9	Oral presentation																	
10	Submission of Final Report Hardcover																	

Legend: **SW:** Study Week **EW :** Exam Week

Appendix B

Program of the ATHENA used in creating the NMOS device structure during the practice:

```
go athena
# Non-Uniform Grid (0.6um x 0.8um)
line x loc=0.00 spac=0.10
line x loc=0.2 spac=0.01
line x loc=0.6 spac=0.01
#
line y loc=0.0 spac=0.008
line y loc=0.2 spac=0.01
line y loc=0.5 spac=0.05
line y loc=0.8 spac=0.15
# Initial Silicon Strucutre with <100> Orientation
Init silicon c.boron=1.0e14 orientation=100 two.d
#Gate Oxidation
Diffuse time=11 temp=925.727 dryo2 press=0.982979 hcl.pc=3
#
Extract name="Gateoxide" thickness material="SiO~2" mat.occno=1 x.val=0.3
# Threshold Voltage Adjust Implant
Implant boron dose=9.5e11 energy=10 crystal
# Conformal Polysilicon Deposition
Deposit polysilicon thick=0.2 divisions=10
# Poly Definition
Etch polysilicon left p1.x=0.35
# Polysilicon Oxidation
Method Fermi compress
Diffus time=3 temp=900 weto2 press=1.00
# Polysilicon Doping
```

```
Implant phosphor dose=3e13 energy=20 crystal
# Spacer Oxide Deposition
Deposit oxide thick=0.12 divisions=10
# Spacer Oxide Etch
Etch oxide dry thick=0.12
# Source/Drain Implant
Implant arsenic dose=5e15 energy=50 crystal
# Source/Drain Annealing
Method Fermi
Diffuse time=1 temp=900 nitro press=1.00
# Open Contact Window
Etch oxide left p1.x=0.2
# Aluminum Deposition thick=0.03 divisions=2
# Etch Aluminum
Etch aluminum right p1.x=0.18
Electrode name=source x=0.1
Electrode name=drain x=1.1
Electrode name=gate x=0.6
Electrode name=backside backside
Struct outfile=nmos.str
```

Appendixes C

Program for ATLAS simulation in interpreting electrical performance of the NMOS

```
go atlas
#
Mesh infile=nmos.str
#
Models srh cvt boltzman print temperature=300
#
mobility bn.cvt=4.75e=007 bp.cvt=9.925e+06 cn.cvt=174000 cp.cvt=884200\
taun.cvt=0.125 taup.cvt=0.317 gamn.cvt=2.5 gamp.cvt=2.2 \
mu0n.cvt=52.2 mu0n.cvt=44.9 mu1n.cvt=43.4 muip.cvt=29 mumaxn.cvt=1417 \
mumaxp.cvt=470.5 crn.cvt=9.68e+16 crp.cvt=2.23e+17 csn.cvt=3.43e+20 \
csp.cvt=6.1e+20 alphn.cvt=0.68 alphn.cvt=0.71 betan.cvt=2 betap.cvt=2 \
pcn.cvt=0 pcp.cvt=2.3e+15 deln.cvt=5.82e+14 delp.cvt=2.0546e+14
#
contact name=gate n.poly
#
Interface s.n=0.0 s.p=0.0 qf=3e10
#
method Newton gummel itlimit=25 trap atrap=0.5 maxtrap=4 autonr \
nrcriterion=0.1 tol.time=0.005 dt.min=1e-25 daamped delta=0.5 \
damploop=10 dfactor=10 iccg 1u1cri=0.003 1u2cri=0.03 maxinner=25
solve init
solve vdrain=0.1
log outf=nmos1_0.log
solve name=gate vgate=0 vfinal=3.3 vstep=0.1
```

```
extract name="vt" (xintercept (maxslope(curve(abs(v."gate"), abs(i."drain")))) –
abs(ave(v."drain")) / 2.0)
extract name="beta" slope (maxslope(curve(abs(v."gate"), abs(i."drain")))) *
(1.0/abs(ave(v."drain")))
extract name="theta" ((max(abs(v."drain")),*$"beta") / max(abs(i."drain"))) – (1.0 /
max( abs(v."gate")) – ($"vt")))
Tonyplot nmos1_0.log
Log off
Solve vgate=1.1 outfile=solve1
Solve vgate=2.2 outfile=solve2
Solve vgate=3.3 outfile=solve3
#
Load infile=solve1
Log outf=nmos2_0.log
Solve name-drain vdrain=0 vfinal=3.3 vstep=0.3
Solve init
Log outf=nmos3+0.log
Solve name=drain vdrain=0 vfinal=3.3 vstep=0.3
Tonyplot –overlay nmos2_0.log nmos3_0.log nmos3_0.log –set nmos.set
quit
```

Appendix d (Standard IGBT Datasheet)

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CES}	1200	Vdc
Collector-Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	1200	Vdc
Gate-Emitter Voltage — Continuous	V_{GE}	±20	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	28 20 56	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	174 1.39	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150	°C
Short Circuit Withstand Time (V_{CC} = 720 Vdc, V_{GE} = 15 Vdc, T_J = 125°C, R_G = 20 Ω)	t_{sc}	10	μs
Thermal Resistance — Junction to Case - IGBT — Junction to Ambient	$R_{θJC}$ $R_{θJA}$	0.7 35	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	260	°C
Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-to-Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 25 μAdc) Temperature Coefficient (Positive)	$V_{(BR)CES}$	 1200 —	 — 870	 — —	Vdc mV/°C
Emitter-to-Collector Breakdown Voltage (V_{GE} = 0 Vdc, I_{EC} = 100 mAdc)	$V_{(BR)ECS}$	25	—	—	Vdc
Zero Gate Voltage Collector Current (V_{CE} = 1200 Vdc, V_{GE} = 0 Vdc) (V_{CE} = 1200 Vdc, V_{GE} = 0 Vdc, T_J = 125°C)	I_{CES}	 — —	 — —	 100 2500	μAdc
Gate-Body Leakage Current (V_{GE} = ± 20 Vdc, V_{CE} = 0 Vdc)	I_{GES}	—	—	250	nAdc
ON CHARACTERISTICS (1)					
Collector-to-Emitter On-State Voltage (V_{GE} = 15 Vdc, I_C = 10 Adc) (V_{GE} = 15 Vdc, I_C = 10 Adc, T_J = 125°C) (V_{GE} = 15 Vdc, I_C = 20 Adc)	$V_{CE(on)}$	 — — —	 2.42 2.36 2.90	 3.54 — 4.99	Vdc
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mAdc) Threshold Temperature Coefficient (Negative)	$V_{GE(th)}$	 4.0 —	 6.0 10	 8.0 —	Vdc mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 20 Adc)	g_{fe}	—	12	—	Mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	1860	—	pF
Output Capacitance	C_{oes}	—	122	—	
Transfer Capacitance	C_{res}	—	29	—	

SWITCHING CHARACTERISTICS (1)

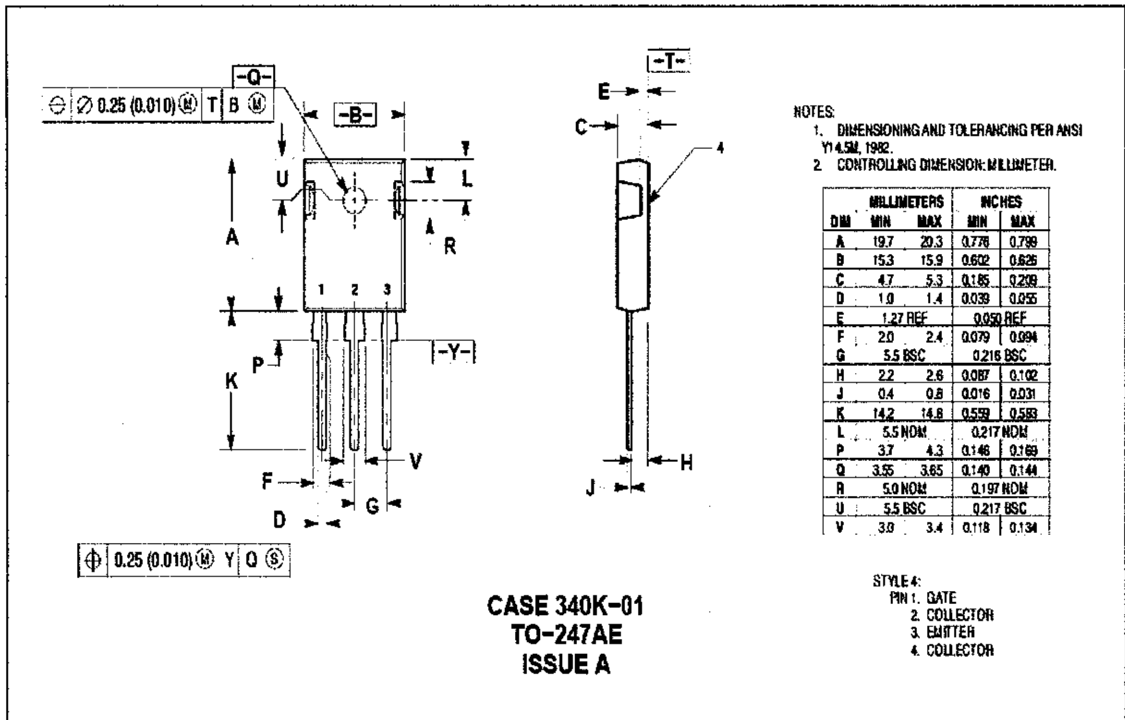
Turn–On Delay Time	(V_{CC} = 720 Vdc, I_C = 20 Adc, V_{GE} = 15 Vdc, L = 300 μH R_G = 20 Ω) Energy losses include "tail"	$t_{d(on)}$	—	88	—	ns
Rise Time		t_r	—	103	—	
Turn–Off Delay Time		$t_{d(off)}$	—	190	—	
Fall Time		t_f	—	284	—	
Turn–Off Switching Loss		E_{off}	—	1.65	2.75	mJ
Turn–On Delay Time	(V_{CC} = 720 Vdc, I_C = 20 Adc, V_{GE} = 15 Vdc, L = 300 μH R_G = 20 Ω, T_J = 125°C) Energy losses include "tail"	$t_{d(on)}$	—	83	—	ns
Rise Time		t_r	—	107	—	
Turn–Off Delay Time		$t_{d(off)}$	—	216	—	
Fall Time		t_f	—	494	—	
Turn–Off Switching Loss		E_{off}	—	3.19	—	mJ
Gate Charge	(V_{CC} = 720 Vdc, I_C = 20 Adc, V_{GE} = 15 Vdc)	Q_T	—	62	—	nC
		Q_1	—	21	—	
		Q_2	—	25	—	

INTERNAL PACKAGE INDUCTANCE

Internal Emitter Inductance (Measured from the emitter lead 0.25″ from package to emitter bond pad)	L_E	—	13	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

PACKAGE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.7	20.3	0.776	0.799
B	15.3	15.9	0.602	0.626
C	4.7	5.3	0.185	0.209
D	1.0	1.4	0.039	0.055
E	1.27 REF		0.050 REF	
F	2.0	2.4	0.079	0.094
G	5.5 BSC		0.216 BSC	
H	2.2	2.6	0.087	0.102
J	0.4	0.8	0.016	0.031
K	14.2	14.8	0.559	0.583
L	5.5 NOM		0.217 NOM	
P	3.7	4.3	0.146	0.169
Q	3.55	3.65	0.140	0.144
R	5.0 NOM		0.197 NOM	
U	5.5 BSC		0.217 BSC	
V	3.0	3.4	0.118	0.134

CASE 340K–01
TO–247AE
ISSUE A

TYPICAL ELECTRICAL CHARACTERISTICS

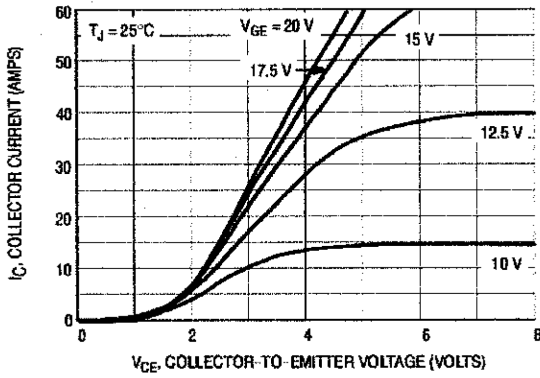


Figure 1. Output Characteristics

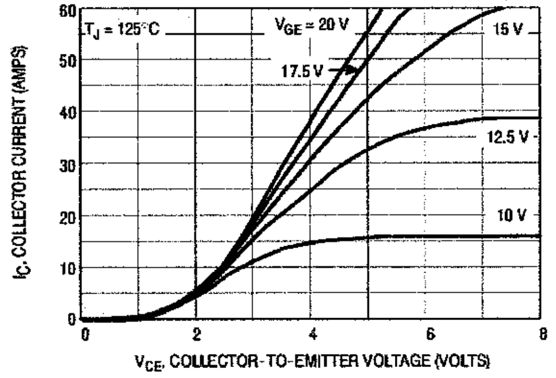


Figure 2. Output Characteristics

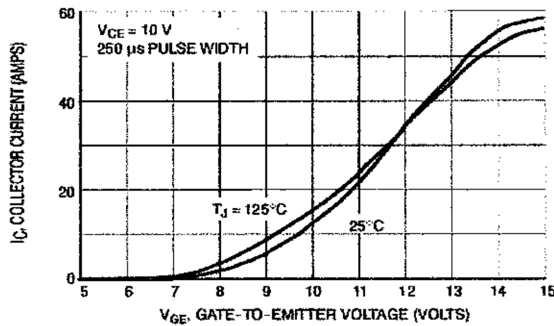


Figure 3. Transfer Characteristics

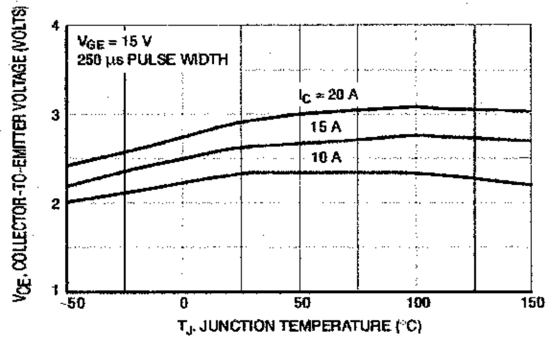


Figure 4. Collector–to–Emitter Saturation Voltage versus Junction Temperature

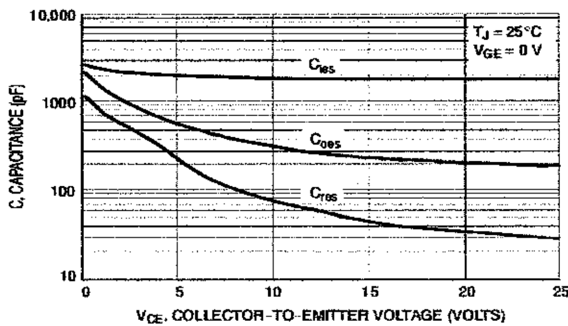


Figure 5. Capacitance Variation

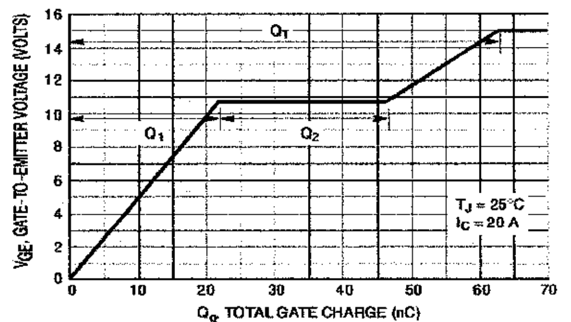


Figure 6. Gate–to–Emitter Voltage versus Total Charge

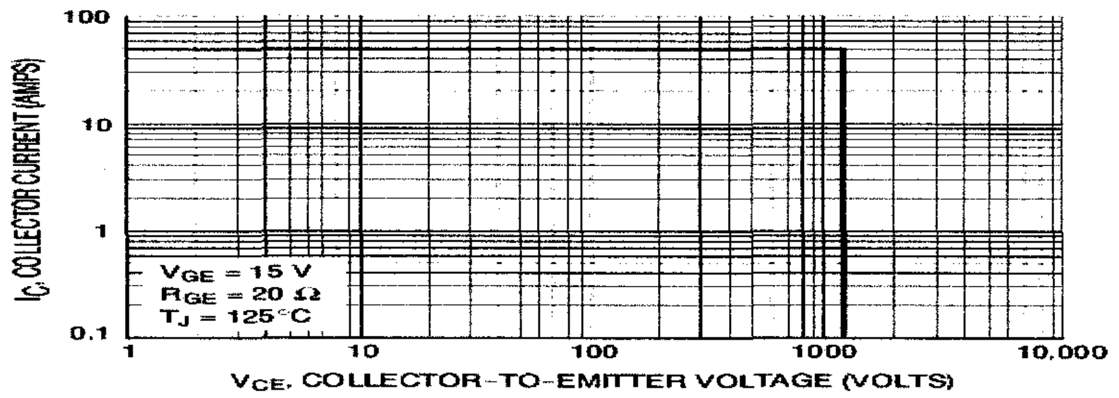


Figure 7. Reverse Biased Safe Operating Area

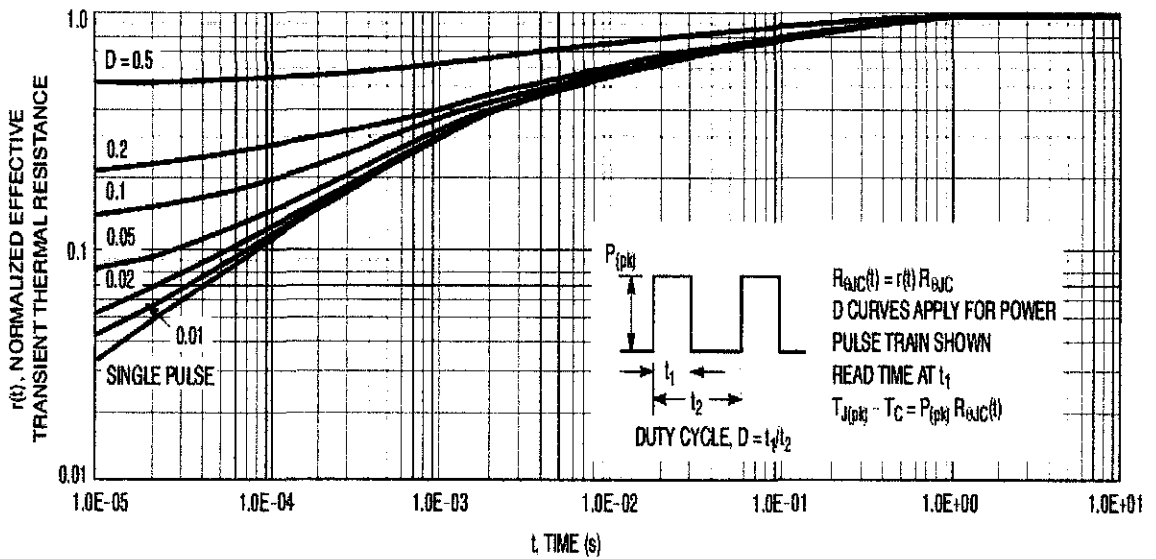


Figure 8. Thermal Response

Appendix E

IGBT PART NUMBERING