STUDY OF GATE TURN OFF THYRISTOR STRUCTURE FOR POWER CONTROL APPLICATION USING SIMULATION

By

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Final Project Report

Submitted to the Electrical & Electronics Engineering Programme

In partial fulfillment of

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(Electrical & Electronics Engineering)

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CERTIFICATION OF APPROVAL

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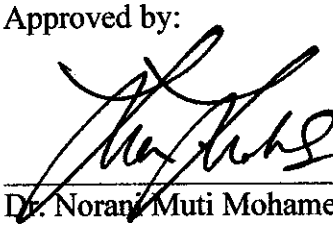
Approved by:



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TRONOH, PERAK

June 2007

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

MOHD NAZRI BIN MOHAMAD ZAKI

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First of all, the deepest gratitude to Allah S.W.T. for his blessing and mercy, I managed to complete this Final Year Project.

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Mohd Nazri Bin Mohamad Zaki

ABSTRACT

The turn-on and turn-off losses in a GTO thyristor must be properly accounted for because they can comprise upwards of 60% of the total losses. If a research can be done to remove the defect and reduce the losses and improved the performance of the GTO thyristor, it will be a great breakthrough to the semiconductor field. This report represents the study on the Gate Turn- Off (GTO) Thyristor using simulation software. This project which was done in 2 semesters (July 2006 semester and January 2007 semester) is the study on the method to improve the performance of the GTO thyristor by reducing it losses. During the first part of the project, familiarization with the TCAD SILVACO ATHENA and ATLAS is done in order to continue doing a critical evaluation to the device; furthermore this step is very important during the extraction process of the electrical performance for the conventional device. For the second semester, the review process of the researches done by other people began to take place. Each of the reference and research found will be carefully compared. The best design or steps is then being chosen to be adopted in the project.

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CHAPTER 1
INTRODUCTION

1.1 Background of Study

The gate turn off thyristor (GTO) is a very high power semiconductor switch, destined for use in industrial applications demanding the ultimate in voltage blocking and current carrying capabilities [1]. This device is widely used in power- control applications like variable- speed electric motors, uninterruptible power supply, high voltage converters, DC/DC converters, etc. The GTO are available up to 4500V and 2500A. It is a four- layer devices with three terminals that can be turned on or off by applying a pulse to the cathode gate. GTO thyristors differ from conventional thyristors, in that they are designed to turn-off when a negative voltage is applied to the gate electrode, thereby causing a reversal of gate current.

This project is only concern on expending the constructing of proper GTO thyristors models using the proper simulation and analysis. Exploration and studies to the GTO thyristors structure will provide information and data necessary in crafting more convenient design and product.

1.2 Problem Statement

Generally, GTO thyristors consist of thousands of individual switching elements fabricated on a silicon wafer. GTO thyristors not only require complex peripheral circuitry to ensure reliable operation but also switch at low frequency. Losses occur in all four conditions of operation (on, off, switching on, switching off).

The powers losses in the thyristor are mainly those of turn-on and conduction losses, the turn off losses are dissipated in the commutation circuitry. For GTO systems however the majority of the switching loss is dissipated by the GTO itself. The generating of these losses will contribute to the generating heat of the thyristor.

The economic and efficient removal of the heat generated by these losses is consequently a major design consideration for the overall system, and because considerable cost, space and weight is taken up by the thermal management equipment there are significant savings to be had from a reduction in these losses.

Detail researches will be conducted to the GTO Thyristors to in creating an improvement to its structure of device or enhancing electrical and electronic performance in power control application. Modification to the GTO thyristors structure is also made in finding ways to simplify its fabrication processing steps. By using the software and application provided, more discovery and prediction can be made to its electrical behavior structures and provides insight into the internal physical mechanisms associated with the device operation.

1.3 Objective of Project

The objective of this project consists of four (4) attributes and listed such as below:

i. To generate a GTO thyristor structure.
ii. To perform electrical characteristic and functionality analysis to GTO thyristor structure.
iii. To do a comparative study on the performance of the GTO thyristor; between the conventional and advance device.
iv. To compare the efficiency, reliability and capability of both GTO thyristors structure and come up with the best solution that has the most consistency and better performance.

These attributes has been carefully evaluate and manage in order to meet the intended outcome. The first two of the objective are already achieved during last semester (July 2006), whereas the final two objectives are schedule to be successfully done in the in this semester (January 2007).

1.4 Scope of Work

The scope of work for this project is:

i. To study all the finding and information regarding the semiconductor fabrication.
ii. To modified the structure of the existing GTO thyristors.
iii. To design a new GTO thyristor structure with respect to design standards and parameters.
iv. To develop processing steps in order to predict the physical structure of the GTO thyristors.
v. To conduct a process simulation and device simulation to the GTO thyristor.

The flow process of this project is briefly shown in the diagram below:

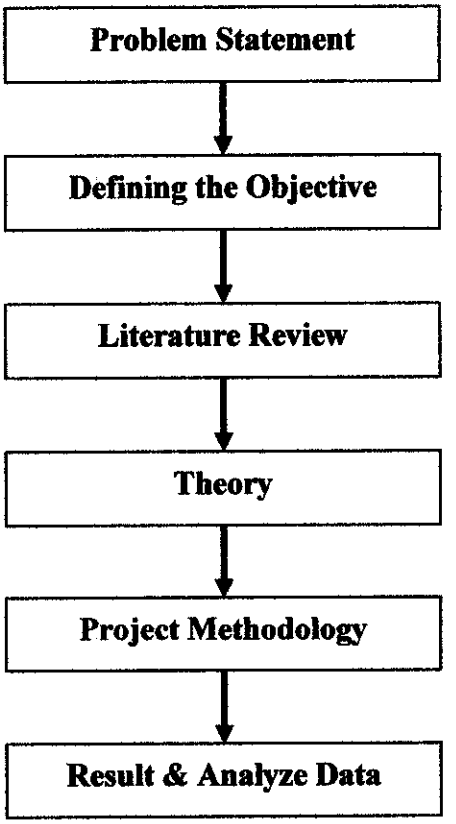

Figure 1: Brief project flow

During this project, the task to be done in order to complete the all of the objectives is:

i. To conduct a study on GTO thyristor structure for used for power control applications.
ii. Identifying the processing steps involve in creating the GTO structure and observe the effect of the device characteristics when its parameters are changed by using ATHENA and ATLAS simulations.
iii. To collect the comparison and analyzed data of modified structure with the existing device.
iv. To investigate how the parameter changes effects the device electrical characteristics.
v. Find out ways of how to improve the device performance so that a better device can be created.
vi. To search of the industrial design and the most updated technique in fabrication of the device.
vii. To do a comparison studies between the designs found in order to select the best method in producing an efficient and reliable GTO thyristor.

The work for this project is carefully planned by using the Gantt chart to make sure that all or the goals and objectives can be achieved the given period of time. The Gantt chart is shown in the appendix section.

CHAPTER 2
LITERATURE REVIEW

2.1 Power Semiconductor Devices

As technology advances, an increasing portion of the electricity in the world needs to be regulated before its utilization. Power electronics involves the technologies used in various kinds of electrical energy regulators [5]. They regulate the raw electrical energy into high quality electrical energy in various forms for various applications. In the process of energy regulation, it is necessary to use devices that can control the electrical energy flow. This role is fulfilled by power semiconductor devices which utilize direction dependant electrical energy flow characteristics of semiconductors.

Dependant on their controllability, power semiconductor devices can be classified into the following three categories [5]:

i. Passive devices (uncontrollable), including the Schottky diode and the PiN diode
ii. Semi-active devices (semi- controllable), including the Thyristor
iii. Active devices (controllable), including the BJT, MOSFET, JFET, IGBT, GTO, SITH, IGCT, MCT, BRT, EST, etc.

2.2 GTO Thyristor Structure

A cross section through a single GTO segment is given below:

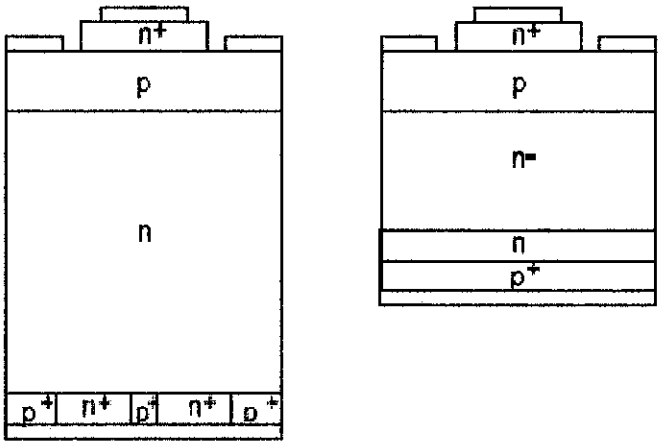

Figure 2: Cross section through a classic anode shorted GTO

The figure 2 above is taken from [1]. Typically, a cathode segment has a length of about 2 to 3 mm, and a width of 100 to 300 microns. Based from [1], GTO is a four layer n+pnp+ regenerative switching device. Each parameters and composition play an important role in determining the devices characteristics. How the parameters and composition affect the device performance is stated below:

i. To obtain high emitter efficiency at the cathode end, desirable for good turn on characteristics, the n+ emitter layer must be highly doped, giving a reverse breakdown voltage to the adjacent p-base.

ii. The design of the p-base greatly influences the trade-off between turn-on and turn-off properties. The doping profile and p-base thickness play dominant roles in the voltage blocking capability of a GTO. The p base itself has conflicting requirements because of its doping concentration is directly related to gate-cathode resistivity. The resistivity should be as low as possible to optimize the turn-off process so the doping concentration should be as high as possible.

However, to obtain high emitter efficiency, the doping concentration should be low.

iii. In order to sustain forward voltages of several kV, the p-base must have a thickness in the range of a few tens of microns, and to guarantee long-term voltage-stability of the "main blocking junction" formed with the n-base "next door", it is terminated with a negative bevel. This requires a highly graded p-base profile.

iv. The maximum forward blocking voltage of the device is always lower than the breakdown voltage of this junction, being dependent on the thickness and resistivity of the aforementioned n-region.

The junction between the n-base and the p+ anode emitter is called the "anode junction", and anode emitter efficiency is very critical to GTO design. An efficient emitter would result in a very low on-state voltage, and low gate trigger-current. However, turn-off capability of such a GTO would be poor, with very low maximum turn-off current and high losses.

2.3 GTO Thyristor Operation Principles

The four different phases in the switching cycle of a GTO which will be briefly described below:

i. Turn- On.
ii. On-State.
iii. Turn-Off
iv. Blocking.

2.3.1 Turn- On

The first phase in the switching cycle of a GTO is the turn- on phase. The figure 3 which is taken from [1] below shows the switching process and in the GTO.

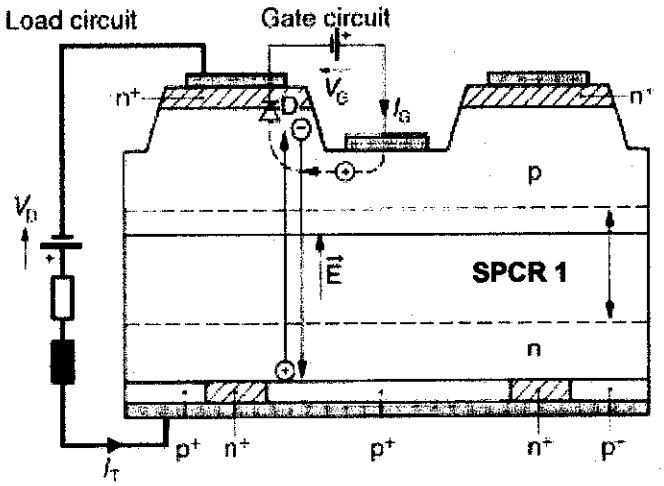

Figure 3: Turn- On switching process of a GTO

According to [1], Gate current is injected across the diode junction D to the n+ layer of the cathode. Because the p n+ junction is forward biased, the n+ layer emits electrons into the p base, some of which reach the space charge region SPCR1 of the p n junction which is blocking anode voltage V_D. These electrons are collected by the electric field E and accelerated towards the anode, where they enter the p+ emitter layer.

This polarizes the n p+ junction in the forward direction and leads to the emission of holes from the p+ emitter layer into the n bases, some of which also reach the space charge region and are accelerated towards the cathode by the same electric field. When these holes enter the n+ emitter layer, they provoke the same effect as the original gate current, i.e. electrons are again emitted from the n+ layer into the p base, and the process is reinforced.

A level of latching current is rapidly reached, at which point the process becomes self-sustaining, with the device remaining in conduction, even if the gate current is interrupted - provided the anode current remains above the holding level. For a GTO, a much larger gate current is required, because many individual thyristors must, in effect, be gated in parallel. If this is done correctly, i.e. with a sufficiently large gate current pulse, all the individual thyristors will ignite simultaneously (there is no spreading effect), and anode current may rise at rates of up to a few thousand amps per microsecond. Depending on wafer diameter and desired anode di/ dt, turn-on gate pulses may vary from a few tens to several hundred amps.

2.3.2 On- State

The regenerative turn-on process just described, injects a great number of electrons and holes from the emitters into the p and n base layers, which become saturated with charge carriers. The resulting carrier concentrations greatly exceed the doping concentrations of the p and n bases, such that GTO replicate the low on-state voltage and high surge current capabilities of conventional thyristors. In figure 4 which is taken from [1], shows in detail the switching state.

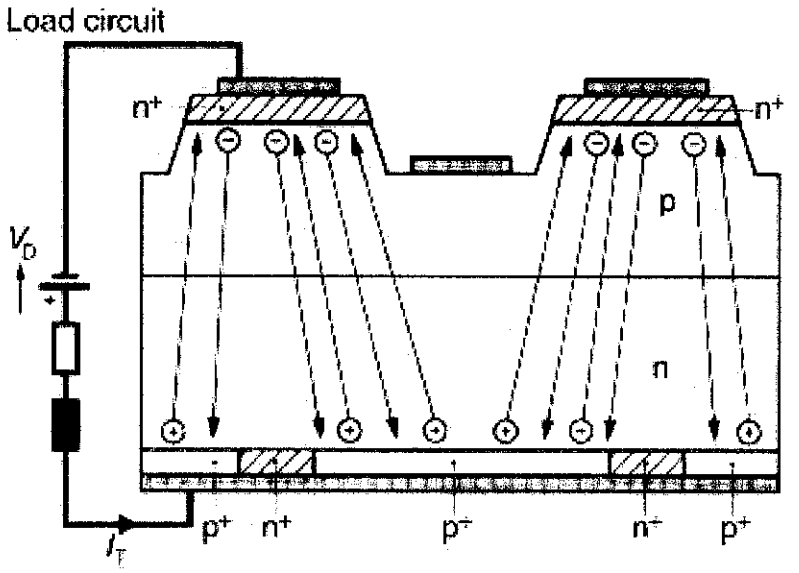

Figure 4: On- state switching state of a GTO

2.3.3 Turn- Off

According to [1], the turn-off process in the GTO is initiated by a negative gate current. Due to the high conductivity of the p-base, holes arriving from the anode partially flow to the negatively polarized gate contact which is shown in figure 5 below:

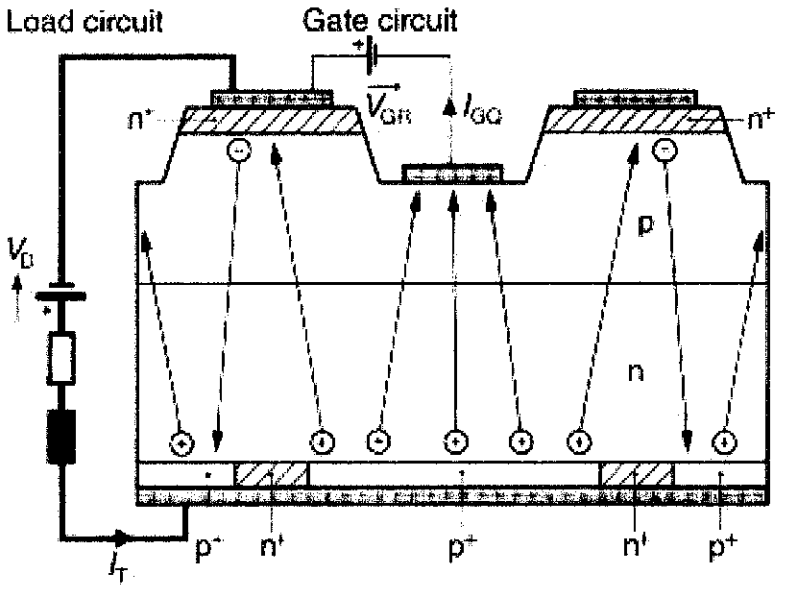

Figure 5: Turn- Off switching process of a GTO

During the storage time, the current progressively filaments towards the middle of the cathode segments, until the filaments are finally "pinched off". At this instant, the anode current falls rapidly, and both the p n+ and p n junctions are again able to sustain voltage. The filamentation of current, towards the cathode centers, reduces the active silicon area during the critical turn-off phase.

2.3.4 Blocking

Figure 6 below, taken from [1], shows the switching process of a GTO during blocking state:

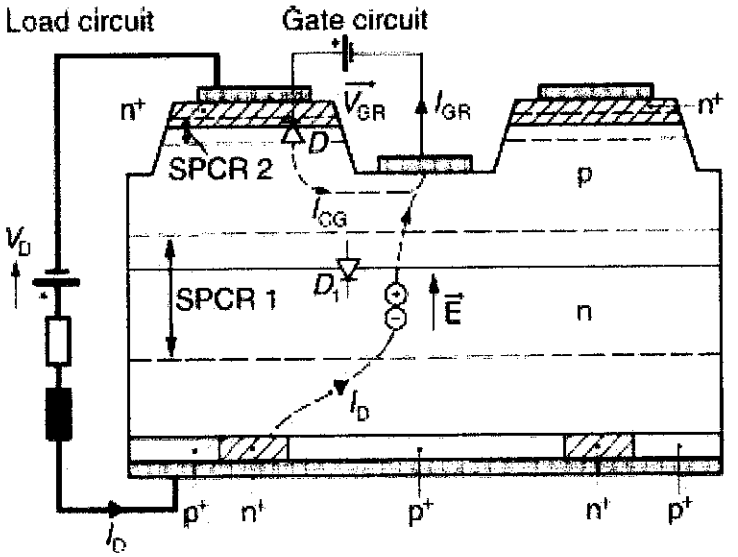

Figure 6: Blocking switching process of a GTO

During the blocking state, the GTO is almost free of mobile charge carriers. The blocking voltage V_D, applied by the external electrical circuit, creates a space charge region SPCR1, while the negative gate voltage, V_{GR}, polarizes diode D in the reverse direction, leading to space charge region SPCR2. The reverse blocking capability of this p n+ diode is limited to about 20 V. Under these conditions, the GTO behaves totally as a p n p transistor, since the reverse biased gate-cathode region prohibits n p n transistor action. Provided the biasing supply is of negligible impedance, the GTO has a virtually unlimited dv/ dt capability.

2.4 Fabrication Process

Basic knowledge of device fabrication processes is important in understanding the structure of power semiconductor devices. The way devices are made affects device parameters hence affects the simplifications and assumptions used in device analysis. Furthermore, without fabrication processing knowledge, it is difficult to optimize the device structure [6]. Because of their high power nature, the fabrication of power devices is different from and more challenging than the fabrication of lower power ICs.

The main fabrication processes include epitaxial growth, oxidation, lithography (masking), diffusion, implantation and deposition. Silicon dioxide (SiO) is an excellent insulator and a barrier to most diffusion.

i. Epitaxial growth

Epitaxial growth is closely related to the crystal growth concept. It involves the growth of a single- crystal semiconductor layers on a single- crystal semiconductor substrate. The epitaxial layer and the substrate materials may be the same, giving rise to homoepitaxy. In an epitaxial process, the substrate wafer acts as the seed crystal. Epitaxial layer can be grown at a temperature substantially below the melting point, typically 30% to 50% lower. The common techniques are chemical vapor deposition (CVD) and molecular beam epitaxy (MBE).

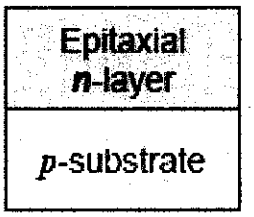

Figure 7: Epitaxial Growth

ii. **Oxidation**

Oxidation is a process that creates an oxide layer by reacting heated silicon with oxygen or water. The oxide width and quality can be controlled by controlling the reacting temperature, time and material. Reacting silicon with oxygen or water are called dry and wet oxidation, respectively. Dry oxidation creates high quality oxide with a superior interface between the oxide and the silicon. Dry oxidation is slow hence is only used in forming a thin layer of high quality oxide. These methods of obtaining superior insulator and diffusion barriers (SiO) are why silicon, rather than Ge and GaAs, is the current dominant semiconductor material. During device fabrication it is necessary to have a reliable insulator device which could act as a barrier to diffusion. Silicon dioxide (SiO_2) is can act as a good insulator device. A high-quality SiO_2 is developed by using the oxidation process.

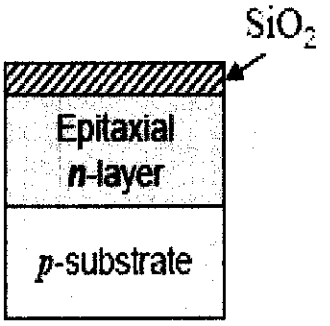

Figure 8: Oxidation process

iii. Photolithography and Etching

Lithography is used to remove a predefined pattern in the oxide layer. The silicon wafer with an oxide layer is covered with a photoresist layer which is then exposed to ultraviolet light through a mask. The mask defines the selective parts of the oxide which is to be removed. After exposure, the part of the positive (negative) photoresist which has reacted (unreacted) with the UV light is dissolved and washed away, and the underlying oxide is exposed. Acid is then used to etch the exposed oxide away. The remaining photoresist is removed after etching is complete.

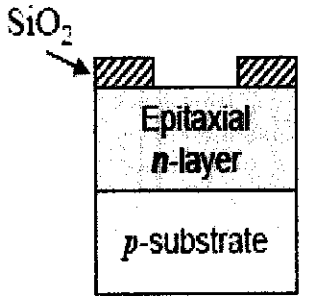

Figure 9: Photolithography and Etching Process

iv. Diffusion and Ion Implantation

After the lithography process, impurities can be introduced through these etched portions of the silicon. Diffusion is commonly used to introduce impurities into silicon. Gas, liquid or solid containing the desired impurities contacts the silicon at a high temperature. Impurity atoms diffuse into the silicon because of the impurity concentration difference. Resultant silicon impurity profiles can be controlled by the source impurity concentration, diffusion time and temperature. An alternative way of doping silicon is implantation where impurity atoms are accelerated to very high speed by a high potential accelerator before penetrating the silicon. With this method, impurity atoms only penetrate to a very shallow depth. This layer of bombed and destroyed silicon is subsequently annealed back to its regular crystalline structure by high temperature treatment. By controlling the annealing time and temperature, deep junctions can be formed since the impurity atom activity is similar to that of the diffusion process. Junctions deeper than 5μm are required in many power devices to block high voltage. Implantation has the advantage over diffusion of controlling precisely the amount of impurity, which makes it the main process for introducing impurities.

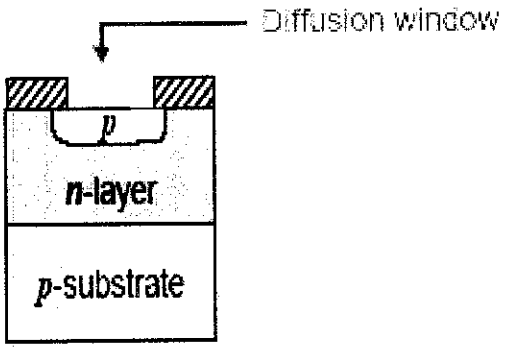

Figure 10: Diffusion and Ion Implantation Process

v. **Metallization**

It is used to form the ohmic contacts and interconnections. A thin film of metal is needed on the device to connect multiple areas to electrodes so that the device can be used in a circuit. Evaporation, sputtering and Chemical Vapor Deposition (CVD) are three options available to form a thin metal film, of which sputtering is the main method used. In sputtering, source metal and the wafer are put on paralleled plates connected to a high-voltage power supply. Ionized by the high voltage, sputtering gas atoms between the plates hit the source and ejects the metal atoms to the wafer plate where they deposit and form a thin metal layer.

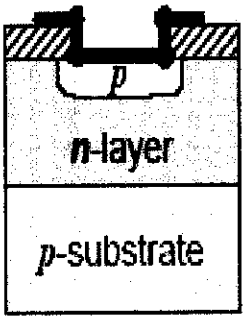

Figure 11: Metallization Process

CHAPTER 3

METHODOLOGY

3.1 Procedure

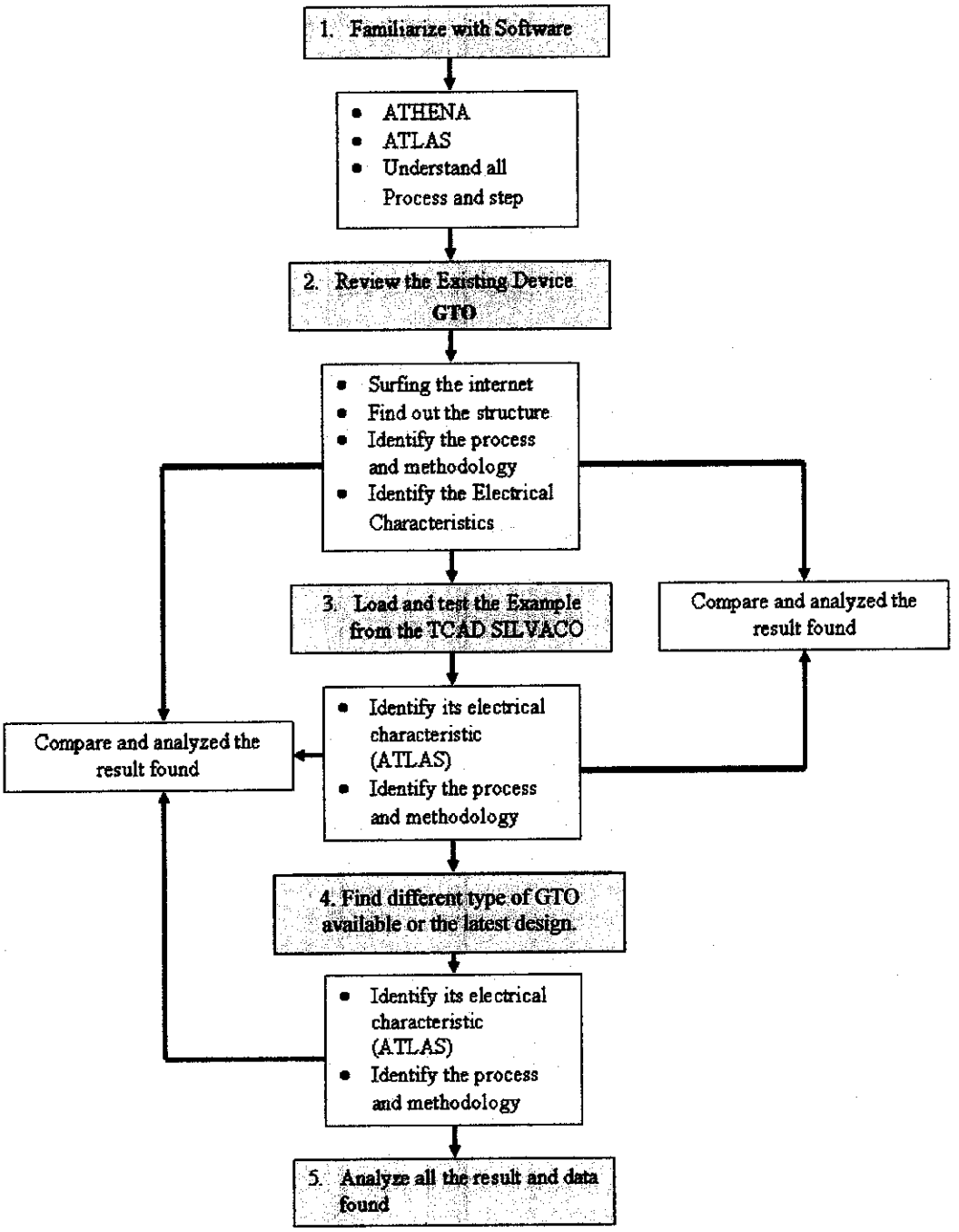

Figure 12: Project flow diagram

From figure 12 which shows the flows of the project, the first thing that the author needs to do is to familiarize with the ATLAS and ATHENA software. In getting familiarize with the software, the author had to learn step by step on how to use the software and the important syntax of the software. This objective is achieved by doing an experiment with the two software tool by generating a NMOS structure based on the workstation manuals.

All the processing step should be understand before going to the next step which is the reviewing the existing device of the GTO thyristor. The reference and guidance can be found in journals, books and internet.

A lot of review for reference regarding the existing device, certain criteria have been observed and take noted such as the structure criteria, the process and methodology involved and the electrical and electronic characteristics of the device. The searching for the reference regarding the processing steps and any other methodology in fabricating this semiconductor is an on going process. Any finding should be carefully recorded and studied.

In Final Year Project 1, the author had reached the third (3) step of the project flow where an example from the TCAD SILVACO software have been loaded and studied. The ATHENA and ATLAS software is used to carry on with the simulation process. The structure of the GTO thyristor have been develop its electrical characteristic is observed and studied.

From this example, the characteristic and parameters of the GTO will be observed and carefully explore. Throughout this project, any parameter of the GTO will be incessantly improved. The modification will only be made on the next level of the project flow where the different between the each observation and the finding stated in the existing research done by other researchers is compared. Finally, all the result and observation should be recorded and analyze.

Optimum structure design is important to achieve good performance from power semiconductor devices. Power semiconductor device design must base on existing fabrication processes to be feasible. Further more, process complexity is associated closely with manufacturing cost. In the semiconductor industry, market requirements and manufacturing cost are of high priority.

In Final year Project 2, the author starts with step four (4) which is to find different type of GTO and found out the most suitable technology and fabrication design of the device. There are many different types of technology which have been implanted to the GTO and had its own advantages and disadvantages. The author needs to find out the processing steps and methodology being used to fabricate the GTO thyristor. The electrical performances of the device need to observe after implementing the technique.

Later on, the author needs to analyze all the result and data found. A comparison study needs to be done between the technologies and the author will configure which are the best techniques in fabricating the most efficient, reliable and economic Gate Turn-Off Thyristor (GTO).

3.2 TCAD Software

SILVACO TCAD workstation can be categorized to 2 main components which is:

- ATHENA simulator

  ATHENA predicts the physical structures that result from processing steps. The resulting physical structures are used as input by ATLAS, which then predicts the electrical characteristics associated with specified bias conditions. It treats process simulation as a serial flow of events.

- ATLAS simulator

  ATLAS simulation is a device simulation tool that can predict the electrical behavior of specified semiconductor structures and provides insight into the internal physical mechanisms associated with the device operation. ATLAS provides general capabilities for physically-based two, and three-dimensional simulation of semiconductor devices.

The combination of ATHENA and ATLAS makes it possible to determine the impact of process parameters on device characteristics. Figure 8 is taken from [4] shows the event that will lead to successfully fabricate GTO device.

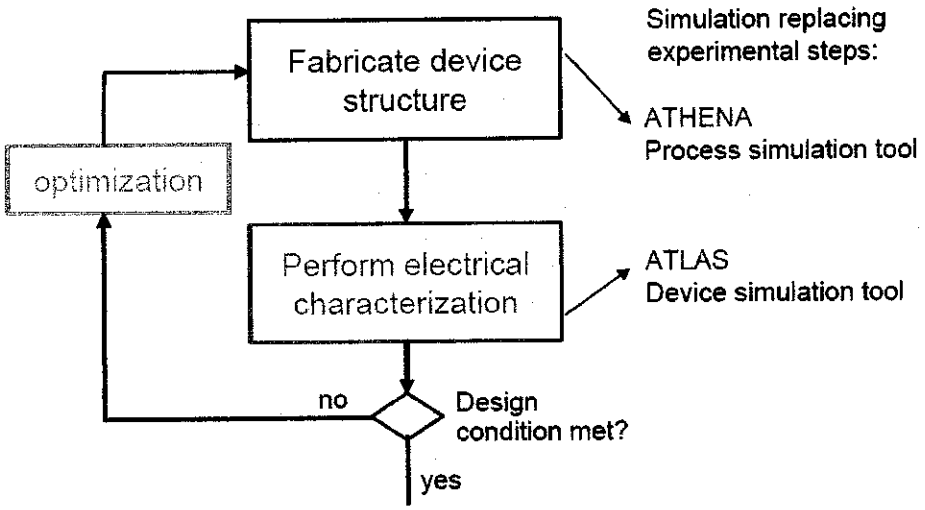

Figure 13: Fabrication processing step

Four weeks have been allocated in getting familiarize with the software, an example has been loaded which is the design of a basic NMOS device structure. The structure of the device is created by using the ATHENA simulator. Then, by using the ATLAS simulator, its electrical performance and characteristic can be observed and tested.

In creating an NMOS device structure using ATHENA [3], the overview of the procedure is:

i. Developing a good simulation grid
ii. Performing conformal deposition
iii. Performing geometric etches
iv. Performing oxidation, diffusion, annealing and ion implantation
v. Structure manipulation
vi. Saving and loading structure information.

3.3 Review on the Existing Device Structure

The existing model design of the GTO thyristor in the SILVACO TCAD workstation is analyze and its characteristic is compared based on the reference already found.

The simulation illustrates the simulation of a Gate Turn- Off Thyristor. The device is embedded in a realistic power device circuit. The interaction between the circuit elements and the active device is important in an accurately simulating the GTO behavior. The steady state behavior is a simulated first. This is used as the initial condition for the transient analysis. The example shows:

i. GTO structure definition with ATLAS.
ii. The SPICE- like command syntax for MIXEDMODE circuit simulation.
iii. GTO steady state solution.
iv. GTO transient turn- off process.

ATLAS is used to define the GTO structure including mesh, materials, electrodes and doping. In the programming part, the mesh rect statement defines a rectangular mesh with grid lines at the locations specified by the x,m and y,m statements. Using the region statement the mesh is divided into three regions: two silicon and one insulator. The electrodes statement defines the cathode, anode and gate electrodes. The doping statement defines doping profiles. The definition of implant type, junction position and characteristic length is also taken note. The net profile is n+ p n p+ from cathode on top to anode on the bottom. The gate is contacted to the p region. After creating the structure is saved and will be used as a device by MIXEDMODE.

In this simulation, the MIXEDMODE circuit simulator uses ATLAS to calculate the transient characteristic of a GTO under specified circuit conditions. First a steady-state simulation of the GTO circuit is performed. The begin and end statement indicates the beginning and end of the MIXEDMODE syntax. The MIXEDMODE commands are

similar to those used in SmartSpice. Circuit component, topology, and analysis are defined in it. In general, the circuit component definition consists are three parts: the type of component, the lead or terminal node assignments, and the component value or model name.

For example, the first component as current source number one, 0 and 1 are the two circuit nodes for this component and 400 indicates that the current source value is 400 amps. This circuit can be divided in tow parts: input and output. The input circuit connects to the cathode and anode of the GTO. It includes current source i1, voltage source v1, resistor r1, r2, r3, diodes d1, d2, d3, inductors I1, I2, I3, and capacitor c1. The output or switching circuits connects to the GTO gate and anode and includes voltage sources v1, v2, v3, diode d4, resistor r2, r4 and inductor I4. The GTO component itself is specified by the agto statement. This statement specifies a device to analyze by ATLAS. The a part of the agto command specifies that this is a device statement. The gto portion simply defines the device name. The option infile= indicates which device structure to be used. The .nodeset statement defines the initial values for node voltages and the .save outfile= statement saves the result to the indicated file. Since this is te steady state solution, no output log file is needed. Since standard diode parts are used in this circuit, the .model dd statement is used to specify additional characteristics. The dd was the model name given in the diode component definition statement. Additionally the .options command sets the solution method to a modified two- level Newton using the m2ln parameter.

To complete the specify simulation, the physical models used by ATLAS must be specify. The model statement is used to turn on the appropriate transport models. This set includes analytic: the analytical concentration dependent mobility model, fldmob: the lateral electric field- dependent mobility model, consrh: Shockley- Read- Hall recombination using concentration dependent lifetimes, auger: recombination accounting for high level injection effects, and bgn: band gap narrowing. The material statement is used to override default material parameter. In this case, the carrier recombination ficed lifetimes are set and for region three, the permittivity is set to that of air. Finally an

impact ionization model is enabled using the impact statement with the selb option. This specifies that the Selberherr impact ionization model is to be used.

The final part of the example is the transient simulation of the gate- turn off. The description of the circuit is similar to the steady state part. The gate turn- off is simulated by pulsing the GTO gate output resistance r4 from 1 megaohm to 1 micro-ohm over 100 ns. This defined by the additional command line option on r4 command line.

All references, data and information of the GTO thyristor are recorded and studied to make a better comparison between the existing device and the new created structure. Any advantages and disadvantages are carefully monitored and further alteration is made if necessary to come up with the best solution in producing the best and reliable device.

CHAPTER 4

RESULTS AND DISCUSSION

4.1 Creating an NMOS Device Structure Using ATHENA

ATHENA simulation in the Silvaco TCAD workstations is the tools required in creating a full NMOS structure which shown in figure 9 below. To shorten up the processing steps and times, the structure of the device, initially was created only in one half. Since the structure is symmetrically to the Y – plane, it is reflected to the Y – plane to obtain the full structure. Silvaco ATHENA analysis shows all the composition of the structure and the characteristic of the device (net doping)[3].

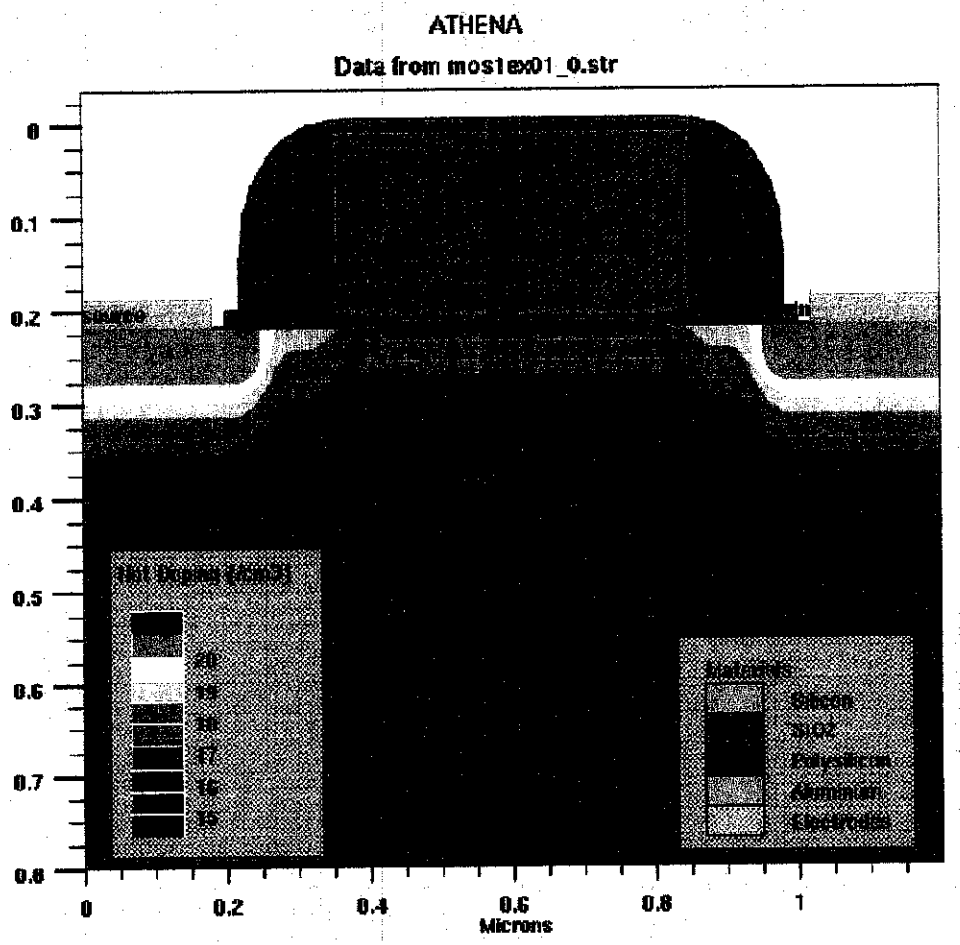

Figure 14: Full NMOS structure

4.2 Electrical Characteristic Prediction Using ATLAS

Using the ATLAS simulator, the electrical characteristic of the NMOS device can be observed. Data measurement and graphical representation of the electrical characteristic of the device is such as **Id versus Vgs curves** and **families of Id versus Vds curves** are plotted. [3]

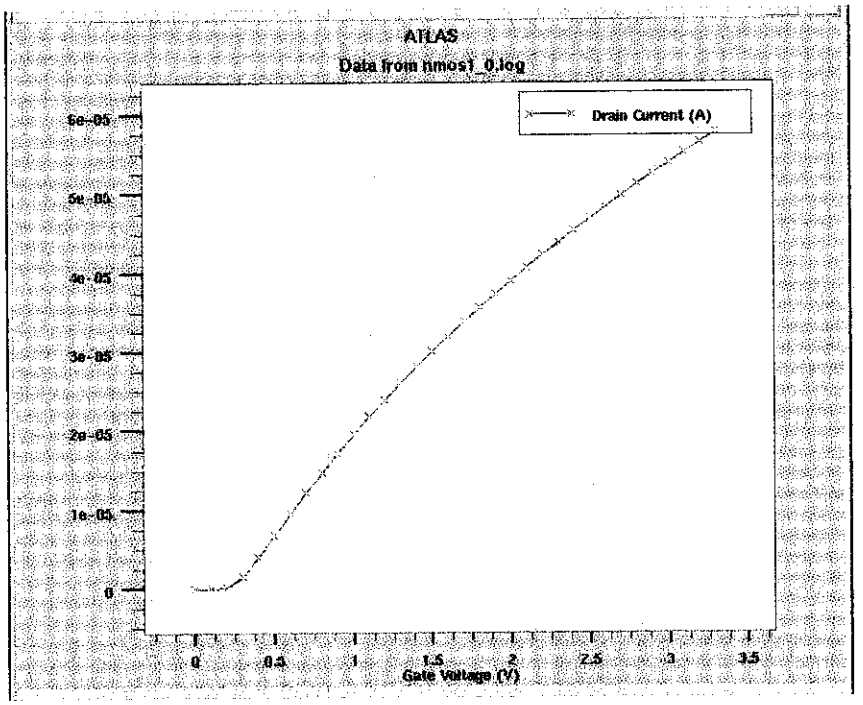

Figure 15: Plot of Id versus Vgs for NMOS device

The curve in figure above is plotted according to the command below:

Solve name=gate vgate=0 vfinal=3.3 vstep=0.1

Then, the simulator will ramp the gate voltage from 0V to 3V with the bias size of 0.1V. The curve represents the relationship between drain current, Id and gate-source voltage, Vgs.

The command used to obtain the Families curve of Id versus Vds for NMOS is:

```
Log off
Solve vgate=1.1 outfile=solve1
Solve vgate=2.2 outfile=solve2
Solve vgate=3.3 outfile=solve3
#
Load infile=solve1
Log outf=nmos2_0.log
Solve name-drain vdrain=0 vfinal=3.3 vstep=0.3
Solve init
Log outf=nmos3+0.log
Solve name=drain vdrain=0 vfinal=3.3 vstep=0.3
Tonyplot –overlay nmos2_0.log nmos3_0.log nmos3_0.log –set nmos.set
quit
```

The ATLAS simulation will plotted the families of Id versus Vds for Vgs = 1.1V, 2.2V and 3.3V as shown in Figure 11. In order to get the curve, the drain voltage, Vd is ramped from 0V to 3.3V with the step of 0.3V[3].

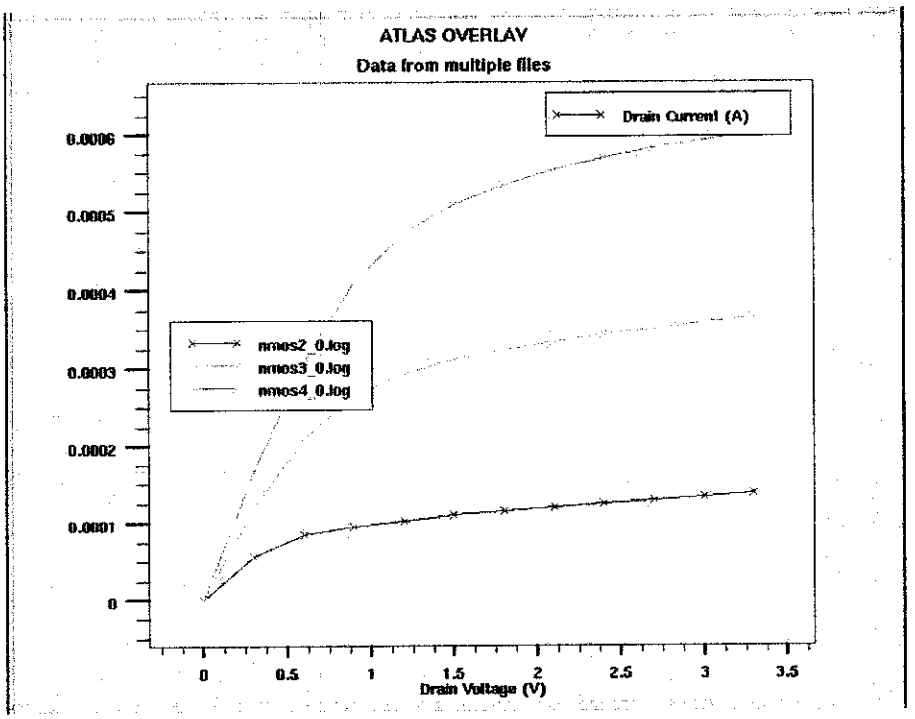

Figure 16: Families curve of Id versus Vds for NMOS

4.3 Method of Producing a GTO Thyristor

A method of producing a GTO thyristor [7]; includes producing a first n type impurity region, a second p type impurity region, a third n type impurity region and a fourth p type impurity region produced in a semiconductor substrate providing a cathode electrode in contact with the first n type impurity region, providing a gate electrode in contact with the second p type impurity region and an anode electrode which short-circuit the third and the fourth regions at the second main surface of the semiconductor substrate. Figure 17 below is taken from [7].

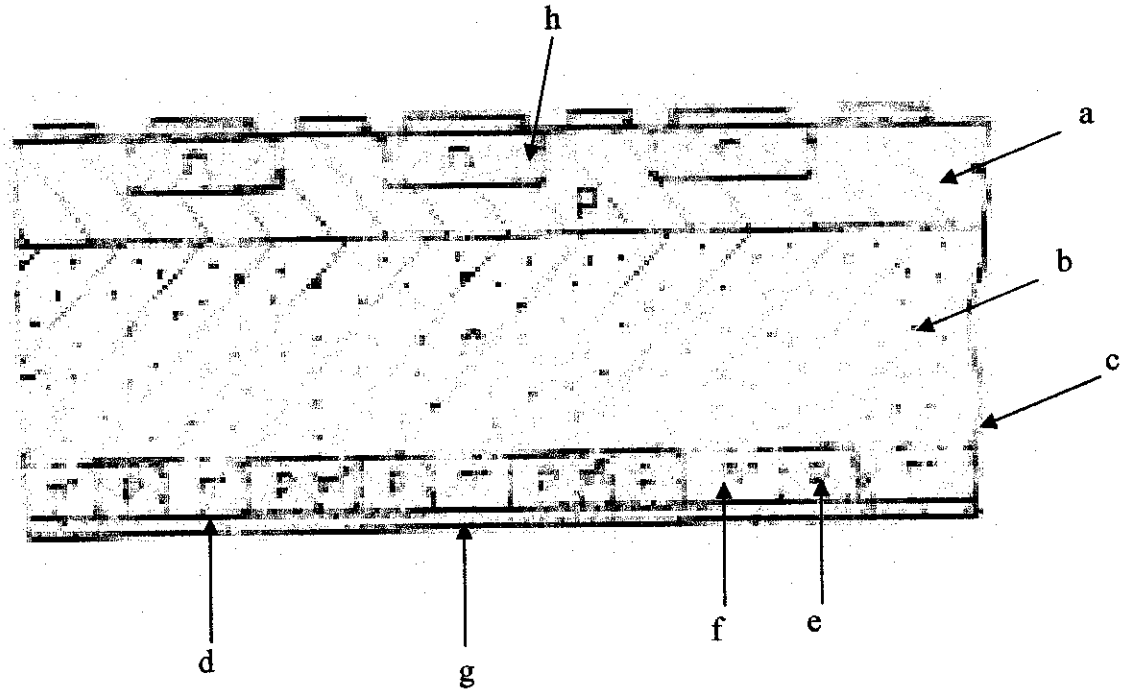

Figure 17: GTO thyristor structure

Detailed description:

i. p type regions (a) are produced at the both surface of the n type silicon substrate (b) by diffusing p type impurities such as gallium or aluminum.
ii. p type region at the opposite side of the p region (a) is removed by producing a silicon wafer (c) comprising of n type silicon substrate (b) and p type region (a) and a predetermine pattern is produced at the surface (d) to which the lapping is conducted.
iii. p type impurities such as boron are diffused to produced p type emitter regions (e).
iv. n+ regions (f) at the anode short- circuited portion are selective produced. p type impurities such as gallium is then diffused to the whole surface therefore producing the p type emitter regions (e). It is necessary the that the density of the n type impurities in the n+ regions (f) are sufficiently higher than p type impurities in the p type emitter regions (e).
v. An anode electrode (g) is produced at the anode surface (d) of the silicon wafer (c).
vi. n type emitter region (h) are produced at the predetermined positions of the counter side surface (cathode surface (i)) of the lapped surface (anode surface (d)) by diffusion of n type impurities.

4.4 Defining the GTO Structure Using ATLAS

To define the GTO structure including mesh, materials, electrodes and doping, the input file statements must be carefully inserted into the DeckBuild and the programme is then being run.

The form of the input file statements is:
<STATEMENT> <PARAMETER> = <VALUE>

The parameter can be (real, integer, character and logical). The order in which the ATLAS commands occur is the following:

i. ***Structure specification:*** MESH, REGION, ELECTRODE, DOPING
ii. ***Material models specification:*** MATERIAL, MODELS, CONTACT, INTERFACE
iii. ***Numerical method selection:*** METHOD
iv. ***Solution specification:*** LOG, SOLVE, LOAD, SAVE
v. ***Results analysis:*** EXTRACT, TONYPLOT

In this example, the first part of the input file statement is structure specifications of the GTO thyristor.

i. **X.MESH, Y.MESH** statements

Specify the location of grid lines along the x and y-axes

- **NODE** - specifies mesh line index
- **LOCATION** - specifies the location of the grid line
- **RATIO** - ratio to be used when interpolating grid lines between given locations
- **SPACING** - specifies mesh spacing at a given location

x.mesh loc=0.0 spac=12.0

x.mesh loc=100 spac=2.0

x.mesh loc=125 spac=5.0

x.mesh loc=150 spac=2.0

x.mesh loc=280 spac=13.0

y.mesh loc=0.0 spac=5.0

y.mesh loc=13.0 spac=0.4

y.mesh loc=17.0 spac=2.0

y.mesh loc=70.0 spac=10.0

y.mesh loc=200.0 spac=50.0

y.mesh loc=410.0 spac=10.0

ii. **REGION** statement

Specifies regions and materials

- **NUMBER** - denotes region number
- **MATERIAL** - can be **SILICON, OXIDE**
- **POSITION** - define location of the region in terms of actual position grid nodes

region num=1 silicon x.min=0 x.max=100 y.min=0 y.max=13

region num=2 silicon x.min=0 x.max=280 y.min=13 y.max=410

region num=3 insulator x.min=100 x.max=280 y.min=0 y.max=13

iii. **ELECTRODE** statement

Must specify at least one electrode within the simulation domain

- **NAME** - defines the name of the electrode: **SOURCE, DRAIN, GATE**
- **POSITION PARAMETER** - **BOTTOM, LEFT, RIGHT, TOP, SUBSTRATE, IX.LOW, IX.HIGH, X.MIN, X.MAX, LENGTH**

elec num=1 top left length=100 name=cathode

elec num=2 bottom name=anode

elec num=3 x.min=150 x.max=280 y.min=0. y.max=13. name=gate

iv. **DOPING** statement

It can be used to set the doping profile analytically. Analytical doping profiles can be defined with the following parameters:

- DISTRIBUTION TYPE - UNIFORM, GAUSSIAN

- DOPING TYPE - N.TYPE, P.TYPE

- CONCENTRATION - peak concentration specification for Gaussian profiles

- CHARACTERISTIC - principal characteristic length of the implant (standard deviation). One can specify junction depth instead.

- PEAK - specifies the location of a peak of a Gaussian profile

- POSITION - X.LEFT, X.RIGHT, REGION

doping reg=2 uniform conc=1.e13 n.type

doping reg=2 gauss conc=1.e17 p.type junc=47

doping reg=1 gauss conc=1.e19 n.type junc=16 x.l=0 x.r=100 rat=0.8

doping reg=2 gauss conc=1.e20 p.type peak=410 junc=393 x.l=0 x.r=170 rat=0.1

doping reg=2 gauss conc=1.e17 n.type peak=410 char=10 x.l=170 x.r=280

Figure 18 in the next page is generated using the TonyPlot as the output file of the input statement.

Part 2 of the input file is where transient and steady-state analysis of the GTO structure (concentration and field-dependent mobilities, impact ionization and radiation induced carrier generation) is key in. The output of the analysis is also generated by using TonyPlot and is shown in figure 19.

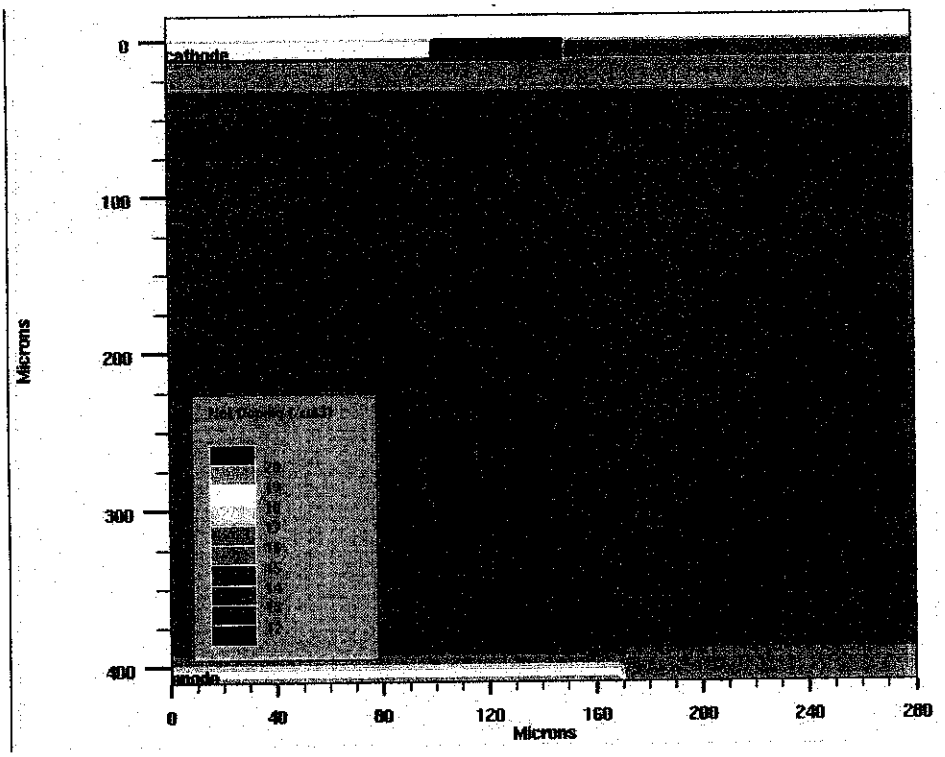

Figure 18: The output of the generating input statement in part 1

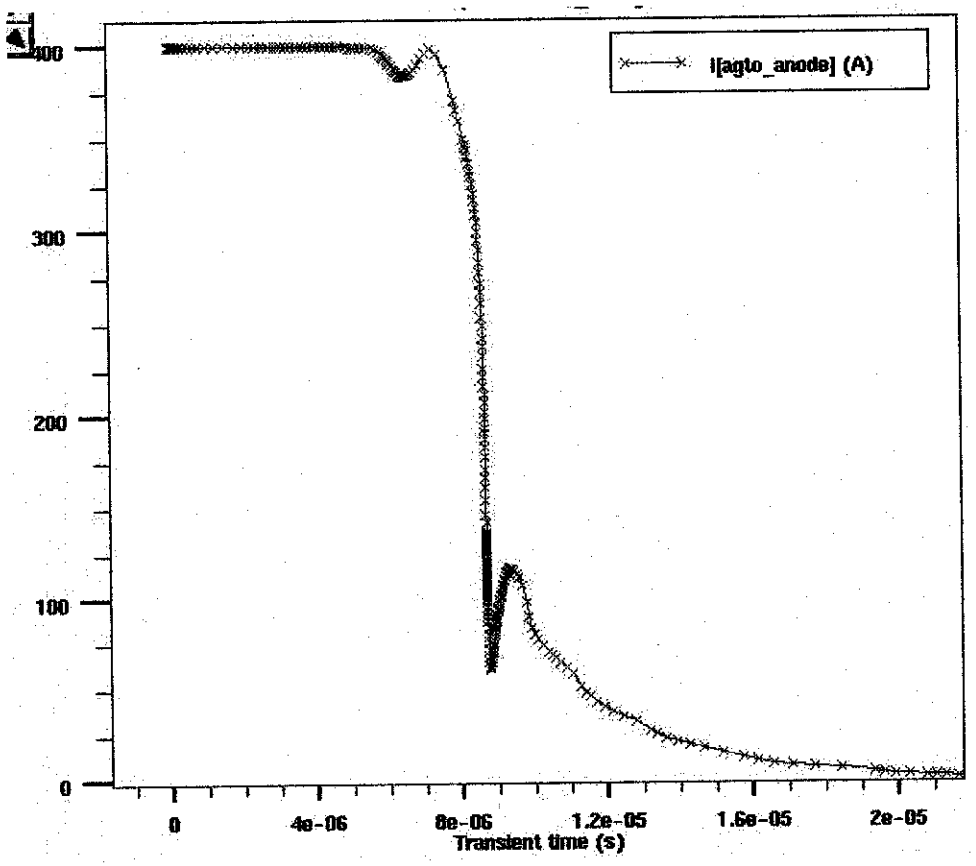

Figure 19: The output of the generating input statement in part 2

4.5 Power Losses in Gate Turn- Off Thyristor

A reduction in the total energy lost in a GTO thyristor due to switching and conduction losses is a most important requirement. For GTO systems, the majority of the switching loss is dissipated by the GTO itself, although the losses in the GTO snubber circuit can also contribute significantly and the switch losses are an important portion of the total overall power losses.

In improvement in a GTO thyristor switch can be achieved by reducing one or all of the following:

i. **Turn-on switching loss**

During the turn-on period the energy loss per pulse (E_{on}) is a strong function of the peak gate current. Increasing the gate current can reduces the turn on time. A large reduction in energy loss can be seen resulting from the correct choice of peak forward gate current. From the device physics viewpoint Eon is strongly dependent on the p-base resistance of the GTO, in a similar manner as for conventional inverter grade thyristor; thus a high resistance gives low energy per pulse. In a conventional thyristor the p-base resistance cannot be increased beyond a certain limit determined by the dv/dt rating. For a GTO however this limit is further reduced because a high p-base resistance seriously limits the current interrupt capability.

ii. **Turn-off switching loss**

At turn-off the switching energy (E_{off}) results mainly from the tail current during the reapplied dv/dt state. The tail current can be controlled by either anode shorts or electron irradiation and the irradiation can be used to optimize the relationship between the on-state and turn-off losses. At the moment of a turn off of the GTO, a numbers of carriers remain in the semiconductor substrate. If the lifetime of the carrier is long then the substantial turn off time of GTO becomes long. However by using the irradiation, the GTO has a number of radiation defect which serves as a

lifetime killer to the carriers hence the turn off time of the GTO will become decrease because a tail current, therefore a tail time is decrease.

iii. Conduction loss

During the conduction period the on-state voltage drop determines the conduction losses. The effect of electron irradiation on the tail current and forward voltage drop (V_{TM}) for a GTO is that the on-state voltage is increased while the tail current is reduced by increasing the radiation dose. This independence of V_{TM} and tail current is typical for GTO thyristor, so although it is possible to use electron irradiation to reduce the tail current, and therefore the switch off loss, the V_{TM} is unfortunately increased. As with conventional thyristor V_{TM} becomes increasingly high for higher blocking voltage devices, and so control of tail current becomes increasingly more difficult. To solve this problem would be to locate the defects in a part of the GTO which gives minimum influence on the on-state resistance but maximum effect on tail current decay.

4.6 GTO Thyristor Improvement Design

Nowadays, there are many techniques that were used by the semiconductor manufacturer in order to develop a better and consistence GTO thyristor. The author had studied 3 techniques that can deliver an optimum performance of the GTO thyristor which are [8] irradiation technique, using anode emitter short technique and gold diffusion method [7].

i. Irradiation technique.

In GTO thyristor, irradiation technique can be applied to the substance of the GTO to limit the life time of the carrier in the GTO substrate. The electron radiation gives a uniform distribution of defects in the silicon, whereas proton damage can be accurately implanted to a selected location inside the GTO thyristor. It is found that when applied to high power GTO thyristor this proton radiation gives a substantial performance improvement over electrons. An important advantage of the proton irradiation is the possibility of controlling separately the gate current (I_{GT}), and turn off switching energy (E_{off}).

ii. Using anode emitter short.

This technique gives a charge extraction path between the GTO n-base and the anode contact. This technique is well known and can achieve a reduction in the turn off tail current and also a low turn off energy. By increasing the size of the anode short it is possible to achieve the same effects as increasing electron radiation dose. However, it is not possible to increase continually the size of the anode short because not only will the V_{TM} become too high, but also the triggering sensitivity of the GTO begins to degrade. As the triggering sensitivity degrades, the GTO turns on more slowly, giving an increase in turn on switching energy. So the anode short must be designed to have maximum effect on tail current extraction but minimal effect on turn on triggering sensitivity.

iii. Gold diffusion technique.

Gold can be diffused into the third region of the GTO thyristor at a predetermine diffusion temperature thereby shortening the lifetime of carriers in the substrate. By referring to figure 17, gold impurities are doped to the element by diffusion method thereby shortening the carrier life time of the n type base region (third region). This gold doping is conducted in such a manner that after the insulating film at the anode surface (d) of the silicon wafer (c) to which the diffusion of the n type impurities is conducted is completely removed by hydrochloric acid or the like, gold is attached to the anode surface (d) by deposition. The quantity of gold doping is determined by the diffusion time and the diffusion temperature and it can be controlled by changing the diffusion during intervals of 25 to 30 minutes. The turn- off loss decrease with the rising of the gold diffusion temperature. It is possible to improve the correlation between the turn- off loss and the on- state voltage by diffusing gold at the diffusion temperature of 820^0C to 825^0C thereby resulting in a reduced turn-off loss without increasing the on-state voltage. GTO having the anode short- circuit structure produced by the gold diffusion has the advantage of being suitable for high frequency operation.

Another interesting technique develop by the semiconductor manufacturer in fabricating the GTO thyristor device is by combining the first and second technique which is the irradiation and anode emitter shorts are carried out to the GTO thyristor.

Based on [8], by combining an optimized proton radiation dose with a new anode short designed to give the optimal relationship between turn on sensitivity and turn off tail current decay, a reduction in total energy losses can be achieved. This improved performance of this new GTO design is compared to that of the previous design (proton radiated technology only), and it can be seen that even compared to the proton radiated it has a much lower energy loss, particularly for low V_{TM} levels.

An indication of the superior characteristic of this new design is given in the following table [8], which compares two GTO designs applied to devices with the same cathode area.

	Combined technology	Proton radiated technology
Maximum repetitive peak-off state voltage /VDRM (V)	4500	4500
Maximum surge on-state current /ITCM (A)	3000	3000
Energy loss per pulse/ E_{ON} (mJ) 1500V/2000A	800	1800
On state voltage / V_{TM} (V) 2000A	2.8	3.5
Turn off switching energy/ E_{OFF} (mJ) 1500V/2000A	2300	2300
Power for 300Hz 30% duty square wave 1500V/2000A	2050	3020

Table 1: Comparison table of combined technology and proton radiated technology

By combining both technologies, the GTO now have lower energy per pulse at turn on and turn off, but also a considerably lower on-state voltage for the same cathode area.

Figure 20 below is taken from [7].

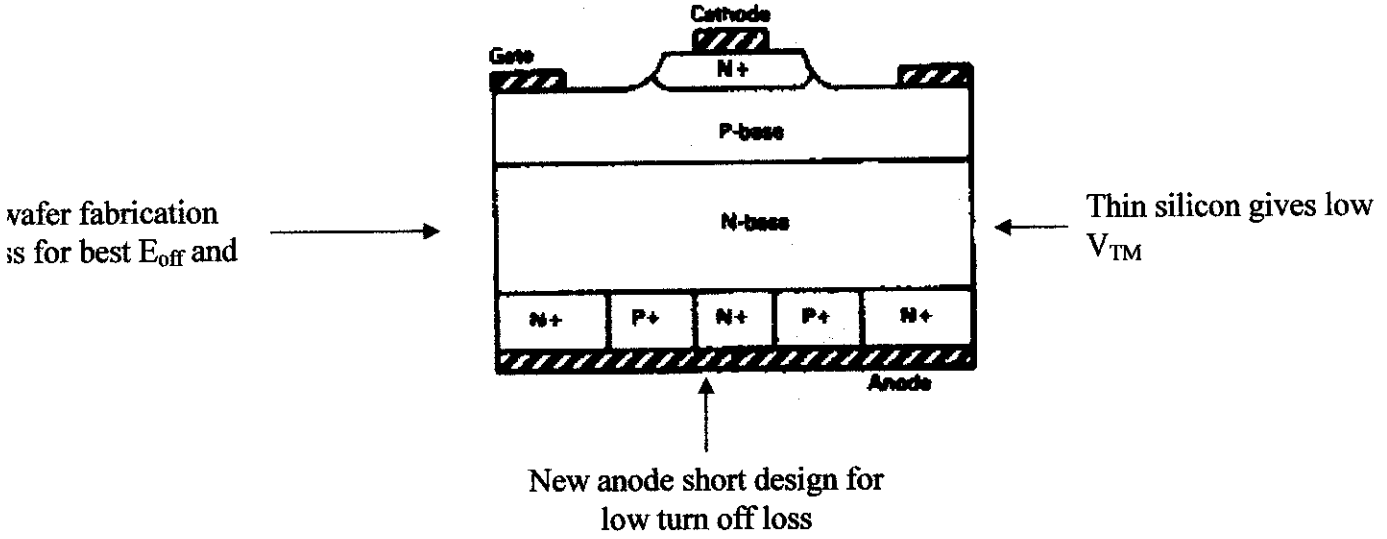

Figure 20: Combination of proton irradiation and anode emitter short technique to GTO

The new design contains a much thinner n-base than used previously to achieve a low V_{TM} and much improved surge current and turn on transient characteristics. The anode short design has been optimized to give charge extraction without affecting the turn on triggering characteristics.

CHAPTER 5
CONCLUSION

During the last 2 semesters, a lot of information and references have been discovered and found in finishing this project. The author also had achieved and accomplished all of the objectives of project which have been mentioned earlier in this report.

Since the author cannot get hold of the recipe of the Gate Turn- Off (GTO) thyristor, the author unable to implement all the technologies in SILVACO TCAD software. However, the most important part to be highlight here is that the author had succeed in understanding how the GTO thyristor is working and steps that need to be taken and considered in improving its performance. A detailed studies, evaluation, comparison and observation have been made in order find the most suitable technology that can actually enhance the performance the GTO thyristor. It is hoped that if the recipe of the GTO thyristor can be acquire, the author will able to implant all of the technique discussed and monitor it real performance.

The comparison studies of the GTO thyristor had provided the author a better picture in considering which processing step can be altered and modified in reducing the losses in GTO thyristor especially during its switching process.

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