THE MODELING & SIMULATION OF SHORT CHANNEL EFFECTS IN MOSFETS

By

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FINAL PROJECT REPORT

Submitted to the Electrical & Electronics Engineering Programme
in Partial Fulfillment of the Requirements
for the Degree
Bachelor of Engineering (Hons)
(Electrical & Electronics Engineering)

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CERTIFICATION OF APPROVAL

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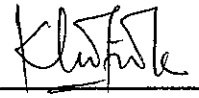
Approved by,



(Mrs Khairul Nisak Md Hasan)

UNIVERSITI TEKNOLOGI PETRONAS

TRONOH , PERAK

JUNE 2007

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

Asmah binti Abdul Halim

ACKNOWLEDGEMENT

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ABSTRACT

This is the Final Year Project Final Report of Universiti Teknologi PETRONAS Final Year Student, Asmah binti Abdul Halim (4092) on The Modeling and Simulation of Short Channel Effect in the MOSFET. This report is organized as follow: Chapter 1 (Introduction) explains on the background study of project, problem statement, as well as the objective and scope of study. Due to expanding technology, the scale of device is getting smaller. This has caused the channel length between source and drain of MOSFETs to be reduced as well, in order to better achieve flow of electron for faster speed in its application. However, this has resulted in short channel that has it effects. Thus, the objective of this project is observing the short channel effect and yet discovers ways to reduce the effects. Chapter 2 is the literature review of the project which describes on the MOSFET physical structure, MOSFET fabrication, MOSFET scaling phenomenon as well as the short channel effects been encountered. It is realized that this topic will be emphasizing more on the threshold voltage aspect as this voltage distinguishes the conduction from the non-conduction states of MOS transistor. ATHENA and ATLAS module of SILVACO software are the tools used in simulating the fabrication and also the electrical performance of the transistors. This is fully described in Chapter 3. Chapter 4 presents the result obtained from the process simulation (ATHENA), followed by the device simulation (ATLAS). Short channel symptoms been observed on the short channel device by considering few related parameters, followed by few adjustments been done to reduce this problem. The conclusion and recommendation parts wrapped up this report which can be found in the Chapter 5. This project of using SILVACO software is really useful in order to observe the short channel effect, realizing that the MOS technology has been growing at an incredible rate since the development of the first MOSFET. Identifying yet overcoming the effect is the ultimate goal of this project.

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CHAPTER 1

INTRODUCTION

1.1 Background Of Study

Over the past decades, the MOSFET has continually been scaled down in size; typical MOSFET channel lengths were once several micrometres, but modern integrated circuits are incorporating MOSFETs with channel lengths of less than a tenth of a micrometre. Great improvements in integrated circuit(IC) speed and functionality have been accomplished in large part by reducing the size, that is by "scaling", individual IC devices. Difficulties with decreasing the size of the MOSFET have been associated with the semiconductor device fabrication process . Reasons for MOSFETs scaling are [1]:

1) Smaller device consumes less power (reducing energy for switching)
2) Intrinsic switching time decreases thus increasing speed of the device
3) Smaller ICs allow more chips per wafer, reducing the price per chip.

1.2 Problem Statement

Producing MOSFETs with channel lengths smaller than a micrometre is a challenge, and the difficulties of semiconductor device fabrication are always a limiting factor in advancing integrated circuit technology. Recently, small size of the MOSFET has created few operational problems. The most discussed problem in this report will be on the power dissipation in the transistors.

There are many types of power dissipations that occur in the transistors. One of them that relates to the device scaling is called leakage power dissipation which occurs due to leakage currents. The different kind of leakage currents present are as follows:

1.2.1 Subthreshold Conduction

This happens due to flow of current in the transistors when they are supposed to be turned off. Due to the voltage scaling, the transistors do not get sufficient voltage to be completely turned off, so they go into saturation region. The operation of the transistor in saturation region causes this type power dissipation. As the threshold voltage decreases, leakage current increases exponentially.

1.2.2 Tunneling Leakage

As the technologies are scaled down, the thickness of the oxide layer also decreases. Due to the decreased thickness, the oxide layer fails to act as a perfect insulator and the current flows through it. This phenomenon is called 'Tunneling' [2] .

1.3 Objectives and Scope of Study

Short Channel Effects on a MOSFET arises due to the technology changes from Deep Submicron over to Nanoscale. The short channel effects will be observed by performing simulation using SILVACO software. The main objectives of this project are:

1) To perform process simulation (fabrication) for the long and short channel NMOS.
2) To perform device simulation of the short channel NMOS.
3) Finding ways to reduce the Short Channel Effects.

The scope of study is as follow:-

1) Study and understand the physical structure of a MOSFET.
2) Understand the problems on the scaling down from Deep Submicron over to Nanoscale , particularly on the Short Channel Effects.
3) Study and learn the software – SILVACO.
4) Perform process simulation of a long channel NMOS (gate length 500nm) and short channel NMOS (gate length of 250 and 180nm) using ATHENA.
5) Observe and analyze the short channel effects on the fabricated device using ATLAS (device simulation) yet suggest ways to reduce the effects.

CHAPTER 2

LITERATURE REVIEW

2.1 MOSFET Physical Structure

The operating process of a MOSFET (Metal Oxide Semiconductor Field Effect Transistor) was first introduced by Lilienfield in 1926, and a working MOSFET was only built in 1960 [3]. MOSFET is three-terminal device, consist of gate, source and drain which can be seen in Figure 2.1. Gate is the control terminal and the source provides electron or hole carriers that are collected by drain. Gate is electrically isolated from drain, source and channel by gate oxide insulator. The region between drain and source is called channel, which is where the conduction takes place. MOSFETs have managed to replace BJTs in many applications due to their simpler gate drive requirements and higher temperature coefficient. Two types of MOSFET are N Channel (Initially ON) and P Channel (Initially Off).

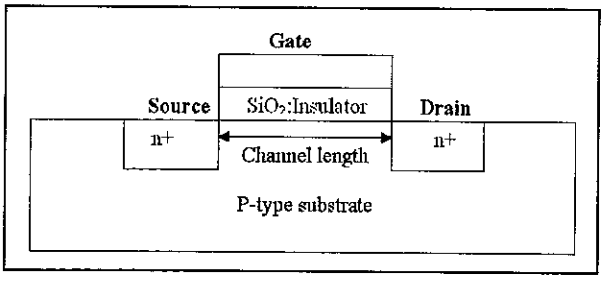


Figure 2.1 : The layout of an N-MOS [1]

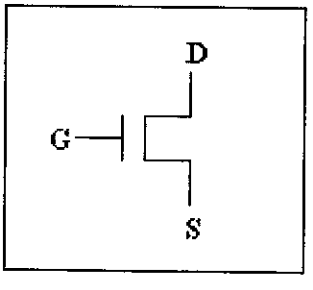


Figure 2.2 : Basic diagram of an N-MOS

2.2 MOSFET Fabrication

2.2.1 Wafer Growth Creation

Semiconductor devices and circuits are formed in thin slices of a material (called a *wafer*) that serves as substrate. For proper operation of the device/circuit, the material must be formed from a single material with the crystals formed by the atoms all aligned in a specific direction. The proper alignment of the crystal lattice has a large effect on the material properties of the substrate including its electrical properties and how it reacts to other materials and chemical processing. Some wafer are uniformly doped with specific impurities (e.g. Boron for p-type wafer with $N_A = 10^{14}$ cm^{-3})[4]

2.2.2 Photolithography

Many steps in the semiconductor fabrication process should only affect specific areas of the wafer. The process of photolithography involves the use of a material called photoresist (PR) to generate a specific pattern on the surface of the wafer. Once the PR has been patterned, the wafer will be covered by PR only in specific areas while the remainder of the wafer is uncovered, Subsequent process steps (e.g. oxidation, diffusion, deposition, etching) will affect only the areas where there is no PR and be blocked where the PR remains. After all necessary processing through pattern, all PR been removed in chemical process.

2.2.3 Doping

The operation of semiconductor devices requires that specific regions of the substrate be doped n-type of p-type with specific dopant concentrations. The concentration of impurities in a semiconductor determines a property called resistivity, ρ which is given by [4] :

$$\rho = 1/(q\mu_n N_D) \quad \text{n-type region} \qquad \text{(Equation 1)}$$

$$\rho = 1/(q\mu_p N_A) \quad \text{p-type region} \qquad \text{(Equation 2)}$$

where q is amount of charge, μ_n is impurities for n-type region , μ_p is impurities for p-type region, N_D is n-type wafer concentration and N_A is p-type wafer concentration.

The electrical resistance of a region which has been doped by impurities is given by [4] :

$$R = (\rho L)/(Wt) \qquad \text{(Equation 3)}$$

where t is the thickness of the doped region, W is the thickness, and L is the length.

To add impurities, 2 methods can be used: diffusion, and implantation.

a) Diffusion

The wafer is placed in a high-temperature furnace where the atmosphere contains the desired impurity in gaseous form. Through the process of diffusion, impurity atoms, which are in high concentration in the atmosphere, will diffuse into the substrate, where they have a low concentration (initially zero). After some time , the impurity atoms are uniformly distributed into the exposed wafer surface at a shallow depth , at a concentration that can be reliably controlled [4] .

b) Implantation

Functionally, implantation is similar to diffusion, but here the atoms are "shot" into the wafer at high velocity (across a very strong electric field) and they embed themselves into the wafer surface. Implantation is more uniform across the wafer than diffusion and allows for very precise control of where the impurities will be. In addition, its peak concentration can be beneath the wafer surface, and it does not require a long period of time at high temperature (which can be harmful) [4].

2.2.4 Oxidation

Insulating dielectric layers provides isolation between conductive layers on the surface of the wafer. In fact, Silicon has become such a successful medium for integrated microelectronics as it has a good native oxide, which means that Silicon oxidizes (combines with elemental Oxygen) to form a dielectric oxide called silicon dioxide, SiO_2. SiO_2 is a good insulating layer and can be created by exposing Si to an O_2 environment. At elevated temperatures (~1000degree C) the oxide grows quickly, which is another characteristic that makes it useful in semiconductor fabrication. Because material (O_2) is being added to the wafer, the wafer grows in thickness, and ~ 50% of the oxide grows beneath the surface and the other half on top of the (original) surface [4].

2.2.5 Deposition

The addition of material to the top of the wafer , require process step generally referred to as deposition. A variety of material can be deposited including conductors, insulators, and semiconductor materials. Several different techniques are employed for deposition, but the process can generally be thought of as a uniform sprinkling of material on the surface of the wafer [4].

a) Dielectric Deposition

Native oxides are only available when native material is still on the surface. Thus, once a wafer has been covered with other materials (e.g. metal), a native oxide can no longer be grown. In addition, after some materials (e.g. metal) have been deposited on the wafer, the wafer can no longer be subjected to high temperatures, which are required to grow native oxides but can melt other materials used in semiconductor fabrication. Thermal oxides are also limited to thin layers . For these three reasons, it is necessary to use deposited dielectrics to cover the wafer and form insulation layers. Deposited dielectrics offer a wide variety of insulating materials including SiO_2 and SiN, they can be deposited on top of any material including metal [4].

b) Polysilicon

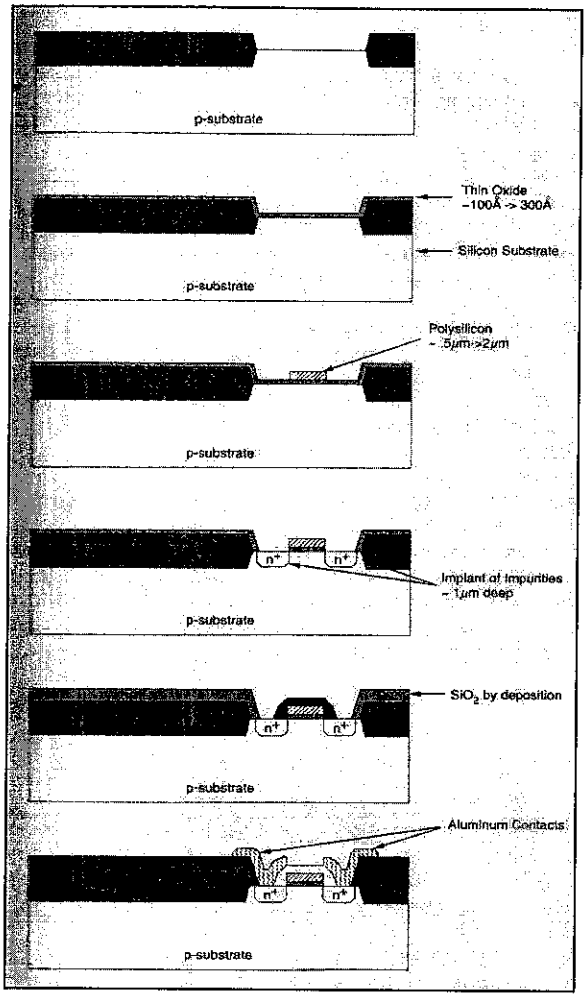
Polysilicon is a Silicon material generally doped to act as a conductor and is used as an interconnect layer and as the gate terminal of an MOS transistor. Primary advantages of polysilicon over other conductors are that it can withstand subsequent high temperature steps, a native oxide can be grown on top of polysilicon, and it has similar material properties to Si and SiO_2 [4].

c) Metals

Various types of elemental metal (e.g. aluminum, gold, copper, nickel, titanium), metal alloys, and other metal compounds are generally deposited and patterned so that contact can be made to the NMOS terminals. Most metals have a low melting temperature, thus therefore must be deposited after all high temperature steps (e.g. diffusion, oxidation. Depositing metal interconnect layers are typically the last steps performed in the semiconductor fabrication process [4].

2.2.6 Etching

Etching refers to the removal of material from the surface of a wafer using a chemical or mechanical process, or a combination of both. Etching processes are needed to pattern deposited layers (e.g. etch metals leaving behind only the desired traces). Chemical etching processes will attack (etch) some materials more quickly than others while mechanical etching will etch all material equally. Both processes require a masking layer (generally either PR or oxide) to block regions where etching is not desired [4].



a) Patterning SiO2 layer

b) Gate Oxidation

c) Patterning Polysilicon

d) Implant or diffusion

e) Contact Cuts

f) Patterning of Aluminium Layer

Figure 2.3: Fabrication steps for silicon gate NMOS transistor [5]

2.3 MOSFET Scaling

MOSFET technology continues to be core of digital integrated circuit(IC). The ultimate aim is to make smaller devices so that more devices can be fabricated on a single chip. Devices with dimensions more than 0.5um are usually called long channel devices whereas term deep submicron technology refers to ICs whose transistor channel lengths are below 0.5um [3]. Whilst, smaller device (approximately below 180nm) is normally categorized as nanometer IC .Technology scaling follows Moore's Law in which number of transistors per die doubles about every two years[3].

2.3.1 Principle of scaling

Constant field MOS scaling theory indicates that the characteristics of an MOS device can be maintained and the basic operational characteristics are preserved if the critical parameters of a device are scaled in accordance to a given criterion in Table 2.1. Electric field across gate oxide, E_{ox} is given by equations below [6]. (The primed parameters refer to the new scaled-down device).

$$E_{ox} = V_{gs} / t_{ox} \qquad \text{(Equation 4)}$$

$$E_{ox}' = \frac{V_{gs} / t_{ox}}{t_{ox} / \alpha} \qquad \text{(Equation 5)}$$

Divide equation

$$\frac{E_{ox}'}{E_{ox}} = \frac{V_{gs} / \alpha}{t_{ox} / \alpha} * \frac{t_{ox}}{V_{gs}} \qquad \text{(Equation 6)}$$

$$\frac{E_{ox}'}{E_{ox}} = 1 \qquad \text{(Equation 7)}$$

$$E_{ox}' = E_{ox} \qquad \text{(Equation 8)}$$

Note: Electric field had been maintained constant, before and after scaling process

V_{gs} = Gate-source voltage
α = Scaling factor
t_{ox} = Gate oxide thickness
E_{ox} = Electric field across gate oxide
E_{ox}' = Electric field across gate oxide(after scaling)

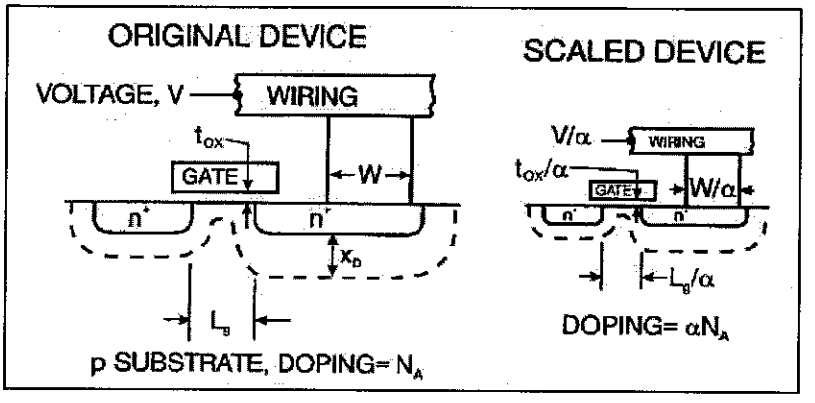


Figure 2.4: Schematic illustration of the scaling of silicon technology by a factor α [7]

To observe the short channel effect, comparison between long and short channel device need to be done. Thus, shorter gate length of the MOSFETs (n-type) is fabricated by modifying the related parameters by factor α , based on the conditions listed in Table 2.1.

Table 2.1: The scaling of MOSFET based on a given α factor [7]

Physical parameters	**Constant electric field scaling factor**
Channel length	1/ α
Channel width	1/ α
Electric field	1
Voltage	1/ α
Doping concentration	A
Area	1/ α
Capacitance	1/ α
Gate delay	1/ α
Power dissipation	$1/\alpha^2$
Power density	1

However, in performing the scaling, there is a limit on which the parameters above can be reduced. As the scaling goes beyond the limits, that is when the short channel effect is realized .

2.3.2 *Short Channel Effects*

2.3.2.1 Threshold voltage difference between long and short channel devices

The mode of operation of MOSFET depends on the threshold voltage, V_{th} . If V_{gs} is less than V_{th}, the transistor in cutoff state. If V_{gs} is greater than V_{th}, an inversion layer is formed and drain current can be induced. The short channel can be affected very much by different threshold voltage.

Difference between the long and short channel device in terms of V_{th} is the amount of depletion charge controlled by the gate. In long channel approximation, it is assumed that all depletion charge is controlled by the gate while for short channel device, some of the depletion charge is controlled by source and drain biases [8]. Thus, difference in threshold voltage of short and long channel device, ΔV_{th} is due to difference in amount of charge controlled by the gate. ΔV_{th} can be obtained by [8]:

$$\Delta V_{th} = (1 - \frac{L + L'}{2L})(\frac{-qN_aW}{C_i}) \qquad \text{(Equation 9)}$$

where q is amount of charge, N_a is dopant concentration ,W is depletion region width, C_i is oxide capacitance, L is long channel length while L' is the short channel length. Since the result of ΔV_{th} is negative, it proves that the threshold voltage for short channel device had been lower compared to the long channel device, as seen in Figure 2.5 .

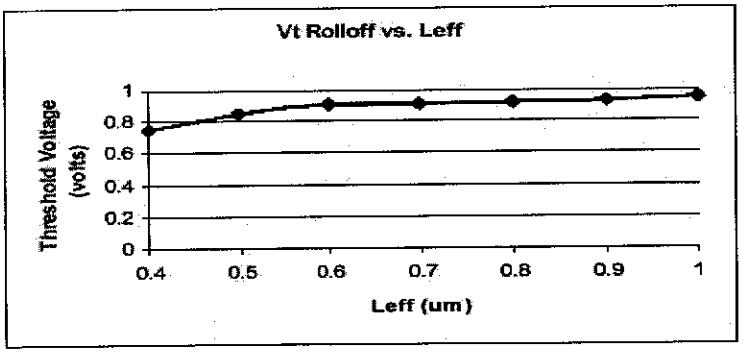


Figure 2.5: V_{th} Rolloff Effect [9]

The threshold voltage reduction increases the transistor leakage since appreciable subthreshold current occurs during the off-state. This current is insignificant for a single device but in 100 million transistor circuit, the impact on the overall power consumption can be significant.

2.3.2.2 Off-state Leakage Current

The short channel effect cause a serious leakage current. When the distance between source and drain is small, the charge space area is created when V_{DD} is applied to the drain (NMOS) and will become too close to the source area as can be seen in Figure 2.6. This will cause the majority carrier charge will be easily flow through the channel even though the gate voltage is zero. This will cause the lost control of transistor over the gate. The leakage current will become more serious when V_{DS} value become bigger. Lost control by gate will cause the lost functioning of transistor and drain voltage, which determined the current at the channel. This will also cause the device become too hot and finally broke down.

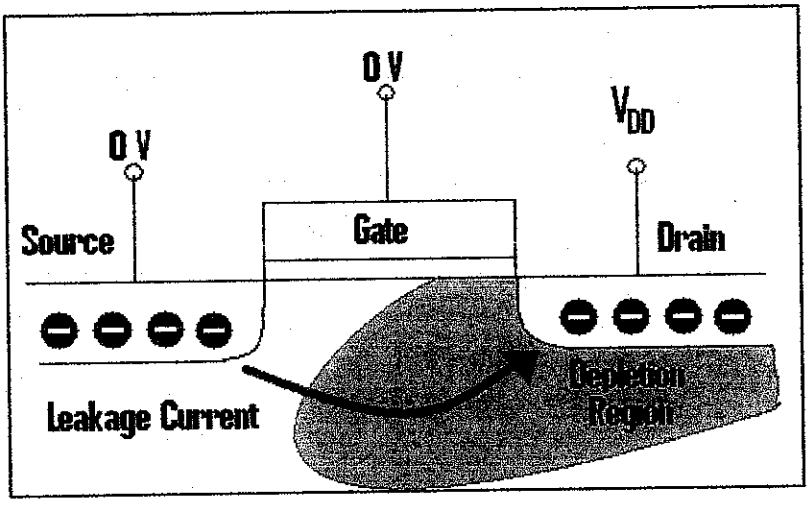


Figure 2.6 : Phenomenon that caused leakage current [10]

2.3.2.3 Failure of current saturation

In large devices , the relative changes of effective channel length ΔL with respect to the total channel length with V_{ds} is negligible, but for shorter devices, ΔL/L becomes important. The effective length of device varies with V_{ds} once the device in saturation and as a result, the curves are no longer flat in this region compared to long channel devices which can be seen in the Figure 2.7 . The small drain current dependence on the V_{ds} in saturation region can be modeled by multiplying saturation current by slope factor that depends on this voltage. The resulting equation is $I_d=I_{dsat}(1+\lambda V_{ds})$.

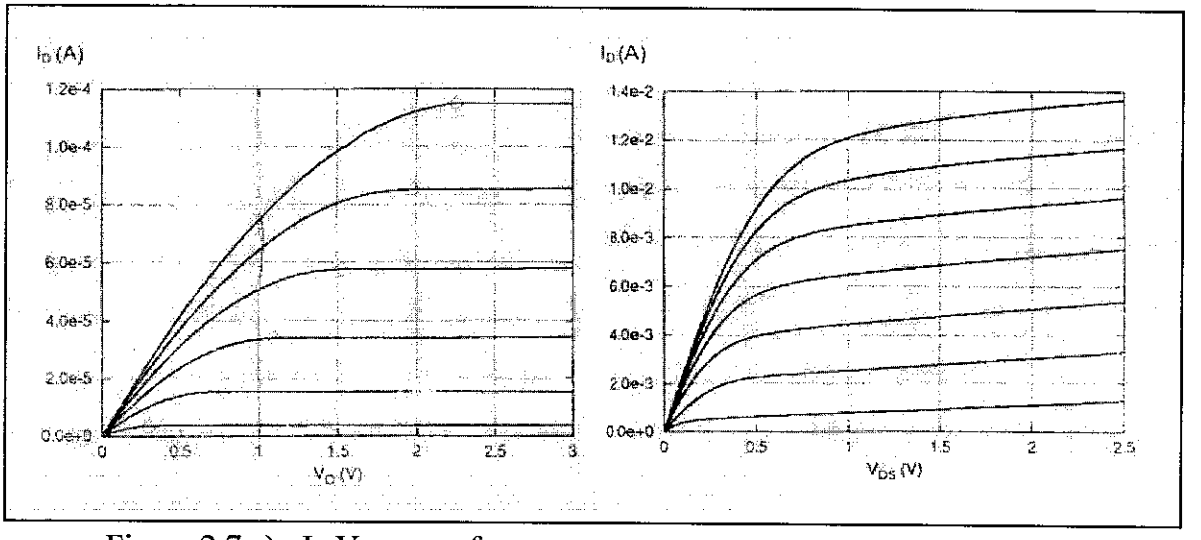


Figure 2.7 a) : I_d-V_{ds} curve for long channel devices[3]

Figure 2.7 b) : I_d-V_{ds} curve for short channel devices[3]

CHAPTER 3

METHODOLOGY

3.1 Project Procedure

3.1.1 Literature Review

The project commenced with the literature review on the physical structure as well as the operation of MOSFET (N-MOS) . It is realized that MOSFET consists of 3 main terminal consist of gate, source and drain. All these terminals play their own important roles to ensure the MOSFET operates accordingly. Then, the literature review been conducted to identify problems been caused by the short channel phenomenon such as threshold voltage reduction and off-state leakage. Major steps of MOSFETs fabrication also been studied so that the simulation would then work properly. These literature review had successfully been carried out by referring to few sources such as books, thesis and websites which been indicated in the references part of this report.

3.1.2 Simulation Design Methodology

As the literature review completed, the researcher proceed to the next step which is the simulation stage, in which involves 2 main modules - ATHENA and ATLAS. The downscaling process of the NMOS had been done first by fabricating the long channel device (500nm) as reference and further reducing the size to the shorter gate length devices, (in this case to 250nm and 180nm) . For different gate lengths, different scaling factor α had been applied. α is derived from direct division of the original gate length to the new gate length. Thus, for 250nm NMOS, the α would be equal to 2 while α equal to 2.778 for 180nm device.

Main parameters been selected for scaling purposes are of the gate length (L_g), supply voltage (V_{dd}) and gate oxide thickness (t_{ox}). References were done to International Technology Roadmap for Semiconductor (ITRS) values during the scaling procedure in order to obtain the optimum results. For instance, according to ITRS, V_{dd} for 250nm needs to be reduced from original value of 4.4V of 500nm device to 2.5V. The same goes to 180nm device that been applied the 1.8V voltage supply. This voltage reduction is important as it is to ensure the constant electrical field across source and drain besides avoiding the oxide break down. As L_g been scaled down, t_{ox} must also be decreased in order to boost the gate control in creating or stopping the inversion channel by the gate electrode. The t_{ox} of 40-50 angstrom is required for 250nm technology, that been further reduced to 36 angstrom for 180nm size . In addition to the reduction of t_{ox}, an increase in channel doping was necessary to reduce the short channel effect. Figure 3.1 summarizes design methodology in downscaling process while Figure 3.2 shows the flow of the whole simulation procedure from the beginning till the end.

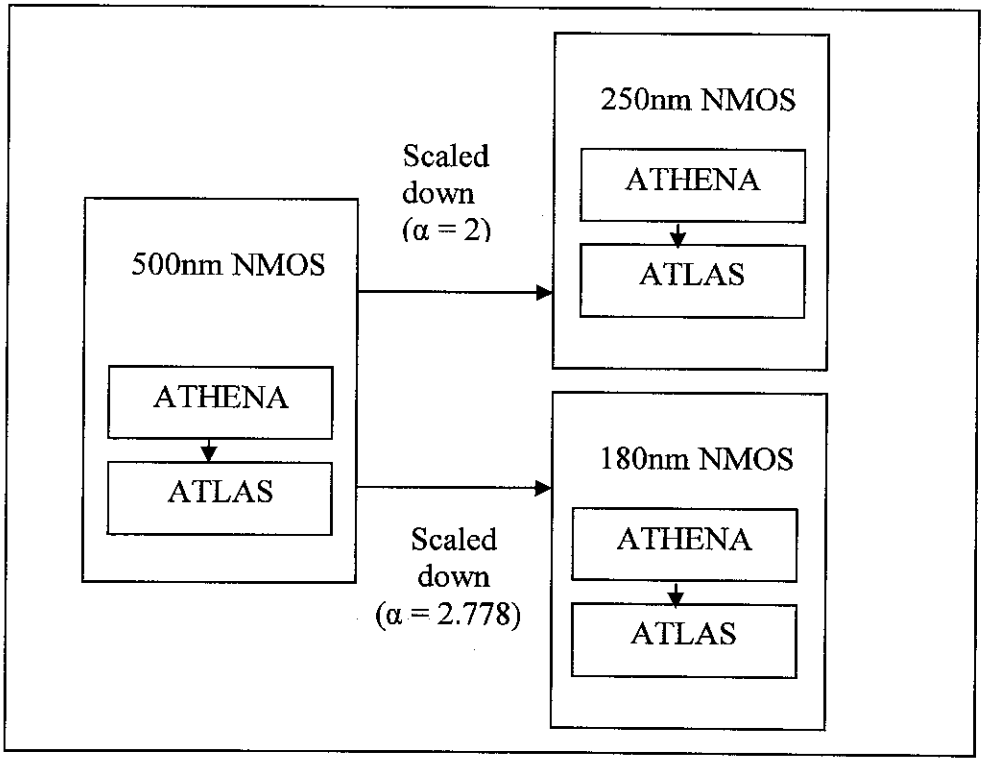


Figure 3.1 : Design methodology in downscaling device

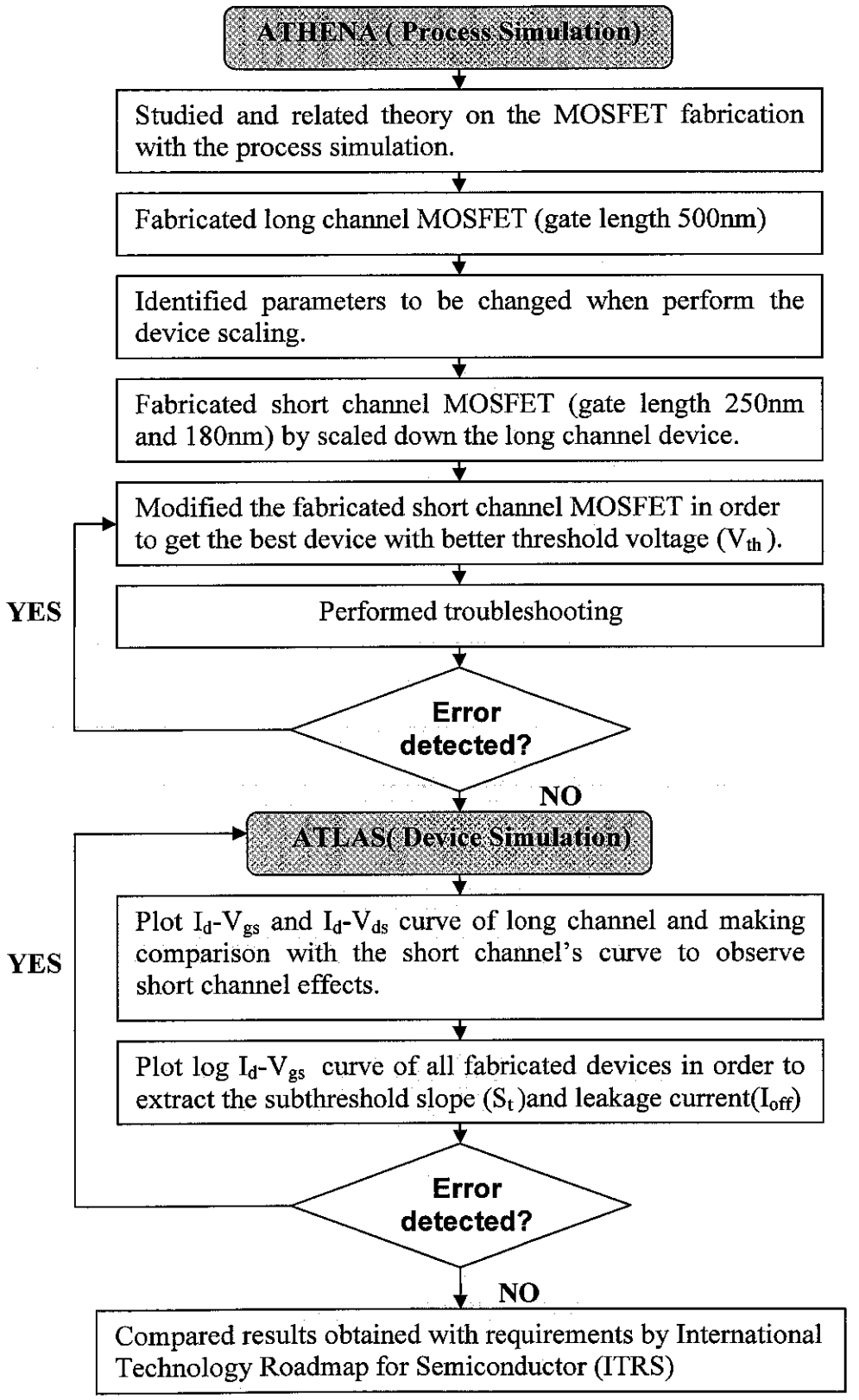


Figure 3.2 : Flow chart of the whole simulation procedure

3.2 Tool (Software)

Virtual Wafer Fab (VWF)

VWF is collection of several software modules, each responsible for part of a device simulation. There are 4 important components - *DeckBuild*, *Athena*, *Atlas*, and *TonyPlot* [11].

1) *DeckBuild* provides a "home base" for the researcher to define code used to fabricate and simulate devices.
2) *Athena* carries out simulation of the device fabrication. It understands processing techniques such as oxidation, materials deposition, diffusion, and etching.
3) *Atlas* responsible for electrical characterization. For instance, researcher specifies terminal voltages, and *Atlas* generates current-voltage curves, yet displays equi-potential lines, electric field lines, and charge carrier concentrations (among other possibilities).
4) *TonyPlot* is responsible for plotting the results of the simulations.

CHAPTER 4

RESULTS & DISCUSSIONS

4.1 ATHENA Simulation

4.1.1 Long Channel MOSFET (500nm) Fabrication

NMOS with gate length of 500nm had been successfully fabricated using ATHENA , with threshold voltage equal to 0.989V. This simulation had been done by fabricating only half of the device as the structure had been mirrored and the complete NMOS had been produced as in Figure 4.1a) and 4.1b) . Full coding of ATHENA process simulation as well as the result.final file can be found in the Appendix .

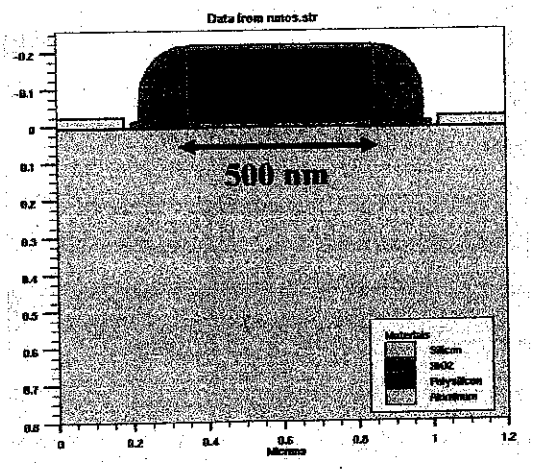


Figure 4.1a) Physical of 500nm fabricated NMOS

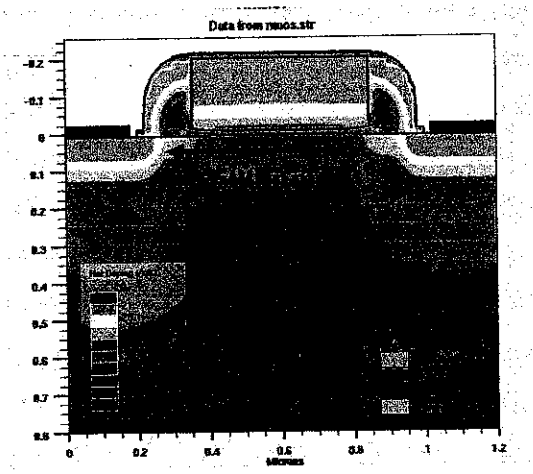


Figure 4.1 b) 500nm fabricated NMOS (indicating doping layer concentration)

4.1.2 Short Channel MOSFET (250nm and 180nm) Fabrication

For different gate lengths , different scaling factor, α had been used. (α =2 for 250nm device while α =2.778 for 180 nm device).Downscaling procedures had been done by [12]:

1) Reducing oxide thickness, T_{ox} by factor α
2) Decreasing gate length by α
3) Reducing V_{dd} by a factor of α
4) Increasing doping concentration by α.

By following the scaling principle, it had yield the result as seen in the Table 4.1.

Table 4.1: Scaled parameters for 3 different gate lengths

Parameters / Gate Length	**500nm**	**250nm**	**180nm**
Oxide Thickness(Angstrom)	101.656	50.127	35.339
Gate Length(μm)	0.5	0.25	0.18
Gate Thickness(μm)	0.2	0.1	0.05
Voltage supply, V_{dd}(V)	4.4	2.5	1.8

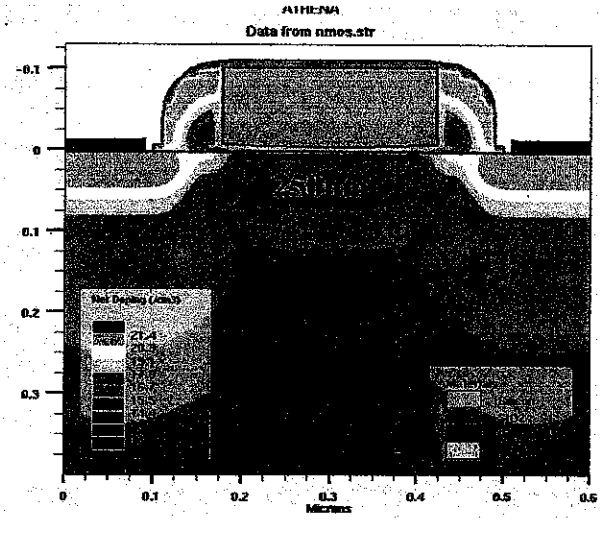


Figure 4.2 a) Fabricated 250nm short channel device.

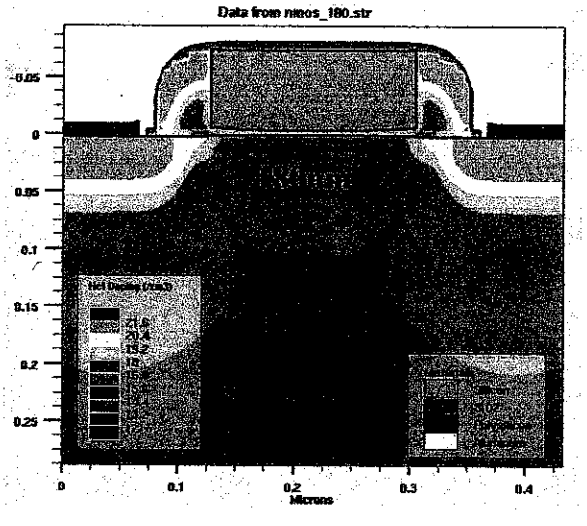


Figure 4.2 b) Fabricated 180nm short channel device

The scaling process is explained as below:

1) Increasing doping concentration by α.

Increasing concentration in implanted regions is quite hard. In this case however, no adjustment of implant dose is necessary since it had been cancelled out by the implant depths which need to be reduced by a factor of α.

2) Decreasing gate length by α

To decrease the gate length, it involves the process of *etch poly left p1.x=0.35*. Thus, by etching farther, the gate will be shorter.

```
# Poly Definition (250nm)
etch poly left p1.x=0.175
structure outfile=poly2.str
```

```
# Poly Definition (180nm)
etch poly left p1.x=0.126
structure outfile=poly3.str
```

3) Reducing source and drain junction depths by a factor of α

Time or temperature been reduced at which drive-in diffusion is done. Energy of the implants also been reduced to bring the dopants closer to the surface of the device.

```
# Source/Drain Implant(250nm)
implant arsenic dose=5.0e15 energy= 25
rotation=31 crystal lat.ratio1=1.0 \
     lat.ratio2=1.0
structure outfile=oxide_etch1.str
```

```
# Source/Drain Implant(180nm)
implant arsenic dose=5.0e15 energy= 17.99
rotation=31 crystal lat.ratio1=1.0 \
     lat.ratio2=1.0
structure outfile=oxide_etch2.str
```

4) Reducing oxide thickness by factor α

The temperature or the time of the gate oxidation reduced.

```
# Gate Oxidation(250nm)
diffus time=3.5 temp=926.966 dryo2
press=0.984283 hcl.pc=3
```

```
# Gate Oxidation(180nm)
diffus time=1.7 temp=926.966 dryo2
press=0.984283 hcl.pc=3
```

4.1.3 Adjustment on Threshold Voltage for the Short Channel MOSFET

The threshold voltage equation is written in the following form:

$$V_{th} = V_{FB} + 2\Phi_F + Q_d / C_{ox} \qquad \text{(Equation 10)}$$

Where V_{FB} is flat band voltage, Φ_F is reference voltage related to semiconductor doping concentration, Q_d is charge density at capacitor plate, while C_{ox} is oxide capacitance. Φ_F is obtained from $V_t(\ln N_A/n_i)$, in which N_A is doping concentration[13].

Based on the Equation 10, the MOSFET threshold voltage depends on the doping level in the channel region. Thus , ion implantation enables precise adjustment of the threshold voltage. By increasing a little bit of the boron doping concentration, the effect on the V_{th} had been observed. The final dose concentration value can be seen as below:

```
# Threshold Voltage Adjust implant (250nm)
implant boron dose=3.35e12 energy=8
rotation=31 crystal lat.ratio1=1.0 \
lat.ratio2=1.0
structure outfile=Vth.str
```

```
# Threshold Voltage Adjust implant (180nm)
implant boron dose=3.50e12 energy=6
rotation=31 crystal lat.ratio1=1.0 \
lat.ratio2=1.0
structure outfile=Vth.str
```

The threshold voltage had been decreased as the gate length been reduced to 250nm and 180nm, which follows the expected result of the Equation 9 (threshold voltage directly proportional to the gate length). The V_{th} obtained during ATHENA simulation needs to be a bit higher than the optimum values stated by the ITRS since it will be reduced when the voltage soon is applied to the device during ATLAS simulation. The adjustment of boron dose implantation helps a lot in the V_{th} alteration (yet reducing the short channel effect) , been tabulated in Table 4.2 .While, Figure 4.3(a)-(e) plotted the result of boron implantation dose adjustment graphically.

Table 4.2: Effect of changing Boron Implantation Dose on the Threshold Voltage

Gate Length	Before Adjustment			After Adjustment		
	Implantation Dose	Threshold Voltage (ATHENA)	Threshold Voltage (ATLAS)	Implantation Dose	Threshold Voltage (ATHENA)	Threshold Voltage (ATLAS)
250nm	2.80E+12	0.555 V	0.435 V	3.35E+12	0.625 V	0.526 V
180nm	2.80E+12	0.438 V	0.268V	3.50E+12	0.526 V	0.392 V

Downscaling had caused the threshold voltage to be reduced, but not in very direct scale. Data shown on Table 4.3 proved this statement since the 0.616 is a bit out-ranged as compared to the expected value, that is 0.72. As been said earlier, the results obtained however been improved, by increasing the value of threshold voltage, that makes the scale nearer to 0.72 which is 0.745

Table 4.3: Comparison between MOSFET with gate length of 250nm and 180nm(scaled by 0.72)

Before V_{th} adjustment				After V_{th} adjustment			
V_{th} - 250nm	V_{th} - 180nm	Scale	Efficiency	V_{th} - 250nm	V_{th} - 180nm	Scale	Efficiency
0.435	0.268	0.268/0.435 = 0.616	85.55 %	0.526	0.392	0.392/0.526 = 0.745	103.50%

4.2 ATLAS Simulation

4.2.1 Threshold voltage reduction (V_{th})

Higher V_{th} obtained (indicated by 1dvt) during ATHENA simulation when compared to the result obtained during the ATLAS simulation (indicated by vt). The reduction of V_{th} during the ATLAS simulation is because 1dvt is grossly obtained by measuring the donor/acceptor levels in the doped area. The vt is much more accurate since it is obtained by "applying" voltage to the transistor. Thus the values are not the same between the two, the more accurate one would by vt that is obtained during ATLAS simulation.

For the V_{th} extraction, I_d-V_{gs} curve is plotted and the sequence of solve statements then set to ramp the gate bias with drain voltage=0.1V. Solutions are obtained in the intervals from 0V to 4.4V for the gate voltage. As the gate lengths been downscaled from 500nm to 250nm and 180nm, it is observable that the V_{th} had been decreased as well.

Thus, in order to optimize the V_{th} value, as stated by ITRS, the implantation adjustment had been done which exhibits better results.

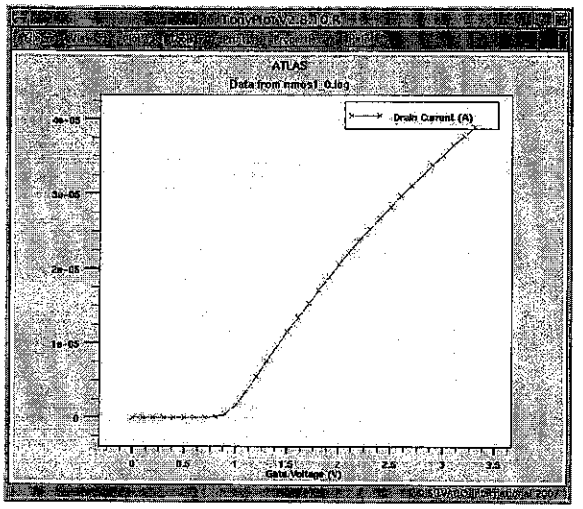


Figure 4.3(a): I_d-V_{gs} curve for 500nm
(ATHENA V_{th} = 0.989 V)
(ATLAS V_{th} = 0.883 V)

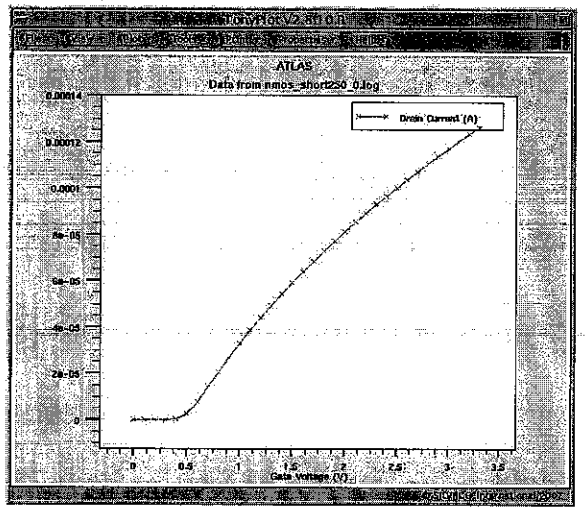


Figure 4.3(b) : I_d-V_{gs} curve for 250nm
(before implantation adjustment)
(ATHENA V_{th} = 0.552 V)
(ATLAS V_{th} = 0.435 V)

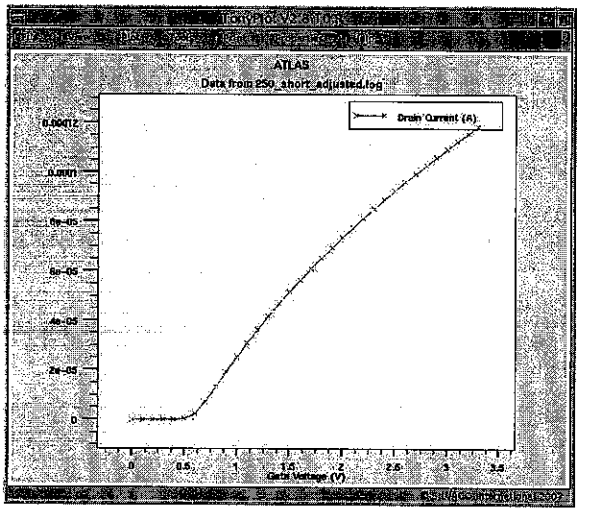


Figure 4.3(c) : I_d-V_{gs} curve for 250nm
(after implantation adjustment
(ATHENA V_{th} = 0.626 V)
(ATLAS V_{th} = 0.526 V)

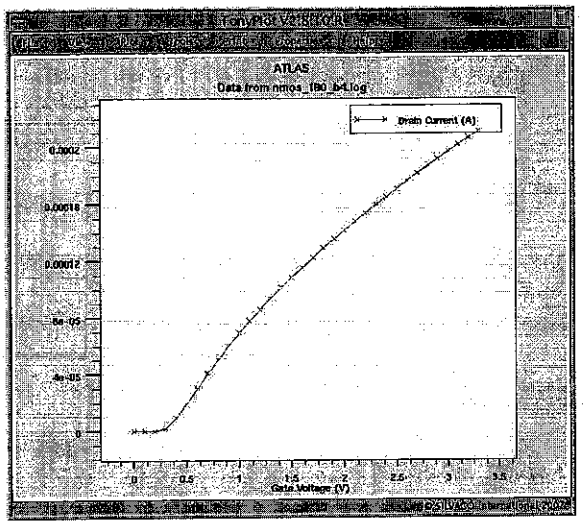


Figure 4.3(d): I_d-V_{gs} curve for 180nm (before implantation adjustment (ATHENA V_{th} = 0.438 V) (ATLAS V_{th} = 0.337 V)

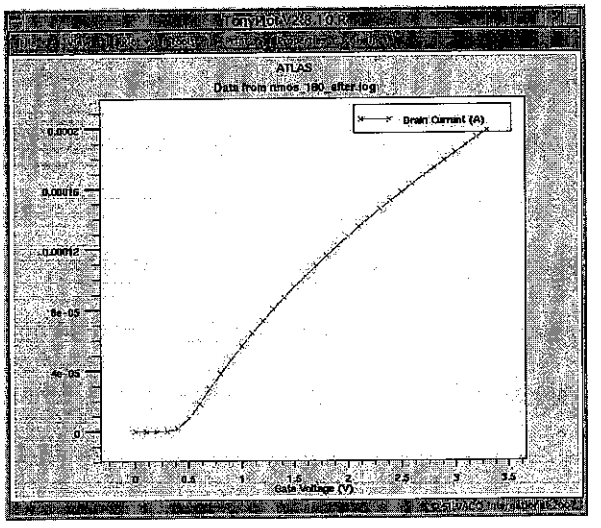


Figure 4.3(e): I_d-V_{gs} curve for 180nm (after implantation adjustment) (ATHENA V_{th} = 0.526V) (ATLAS V_{th} = 0.392 V)

4.2.2 Reduction of Saturation Current

Saturation current is also known as Id_{sat} or I_{on} that refers how much current is carried in the "ON" state of a MOSFET. For this part, I_d-V_{ds} curves been plotted at 4 different V_{gs}. For 500nm, V_{gs} been set to 1.1V, 2.2V ,3.3V and 4.4V with V_{ds} been fixed to 0V. As the device scaled down to 250nm, the V_{gs} also been reduced to 0.625V, 1.25V, 1.875V and 2.5V. The same goes to 180nm that been reduced to the V_{gs} values of 0.45V, 0.9V, 1.35V and 1.8V.

Phenomenon of channel length modulation should be more severe for short channel devices compared to long channel's that happen because of increasing depletion region ratio compared to channel length. The curves obtained however do not show many differences between the long and short channel device. But, it shows very minor differences as the value of Id saturation been extracted that been tabulated in Table 4.4.

Table 4.4 : The I_d saturation for different gate lengths

Gate Length/ Parameters	500nm	250nm		180nm	
		Before V_{th} adjustment	After V_{th} adjustment	Before V_{th} adjustment	After V_{th} adjustment
Id sat (μA/μm)	687.866	680.353	633.992	636.179	608.967

As expected, the saturation current extracted been reduced as the device been downscaled. The increases of V_{th} do not help in increasing the I_d saturation. Instead, the saturation current had been further reduced. The increase in V_{th} can only helped in the reduction of I_{off}. The I_{on} only can be increased by reducing subthreshold swing, S_t that will be explained in that particular part later.

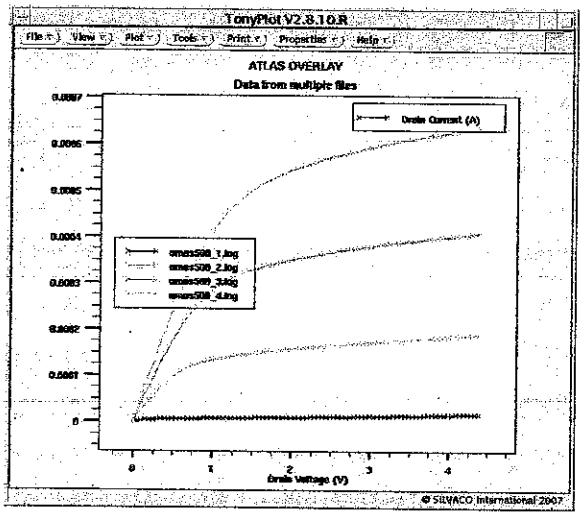


Figure 4.4(a): I_d-V_{ds} curve for 500nm with different V_{gs} to obtain the I_d saturation

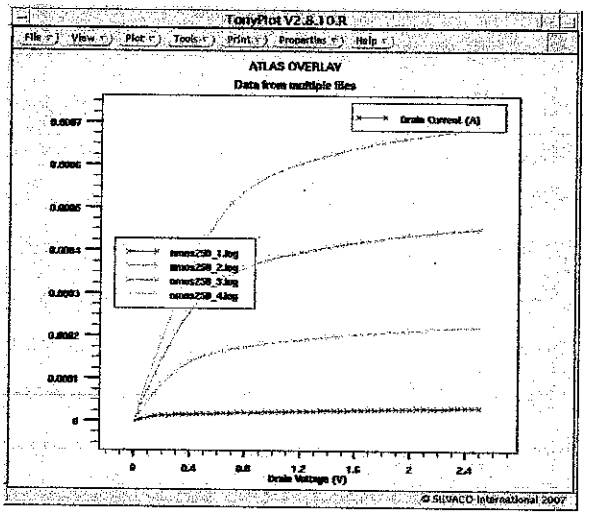


Figure 4.4(b):I_{ds}-V_{ds} curve for 250nm with different V_{gs} to obtain the I_d saturation

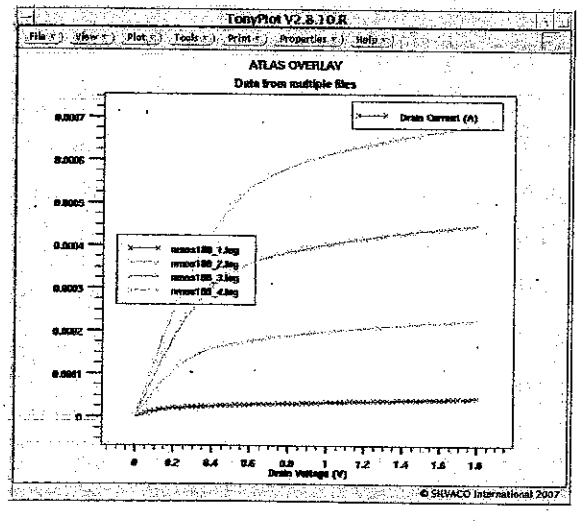


Figure 4.4(c): I_{ds}-V_{ds} curve for 180nm with different V_{gs} to obtain the I_d saturation

Legend (V_{gs} values)		
nmos_500_1= 1.1V	nmos_250_1 =0.625V	nmos_180_1= 0.45V
nmos_500_2= 2.2V	nmos_250_2 =1.25V	nmos_180_2= 0.9V
nmos_500_3= 3.3V	nmos_250_3 =1.875V	nmos_180_3= 1.35V
nmos_500_4= 4.4V	nmos_250_4 = 2.5V	nmos_180_4= 1.8V

4.2.3 Increase in Off-state Leakage Current

At $V_{gs} < V_{th}$, an N-channel MOSFET is in the off-state. However, an undesirable leakage current can flow between the drain and the source. The MOSFET current observed at $V_{gs} < V_{th}$ is called the subthreshold current or off-state current, I_{off}. I_{off} is the I_d measured at $V_{gs}=0$ and $V_{ds}=V_{dd}$ [14].

For given W and L, there are two ways to minimize I_{off} , illustrated in Figure 4.5. The first is to choose large V_{th} which is already done by the researcher ,that is by doing the adjustment on the implantation dose. The second way is to reduce the subthreshold swing that will be explained in the next part.

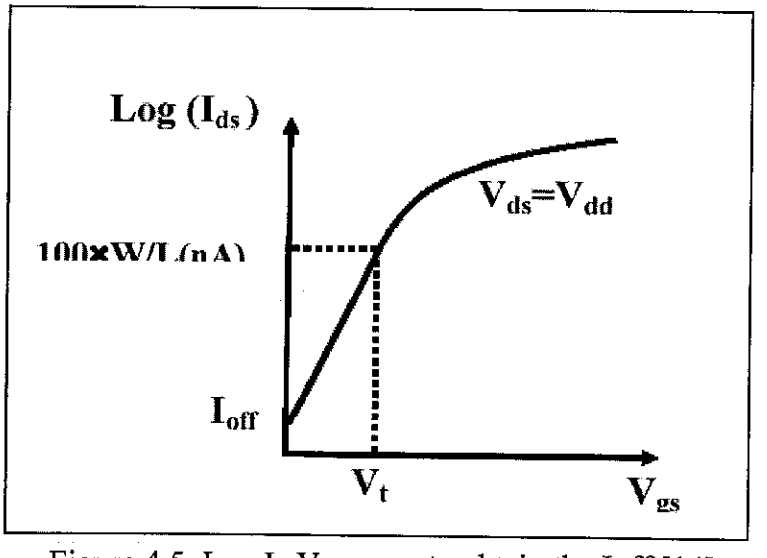


Figure 4.5: Log I_d-V_{gs} curve to obtain the Ioff [14]

The I_{off} had been extracted from subthreshold characteristics. A simple $\log I_d$-V_{gs} curve is generated with V_{ds}=4.4V for 500nm, V_{ds}=2.5V for 250nm and V_{ds}=180nm device. The V_g is then ramped from 0 to specified V_{ds} in incremental steps of 0.1V. The I_d that corresponds to V_g=0V is taken as the off-state leakage current, I_{off}. The I_{off} can be obtained by antilog the value of y-axis interception. The whole results are illustrated in the Table 4.5.

The values obtained does meet expected result in which the I_{off} had increased as the gate lengths been reduced. An increase in I_{off} does imply that gate does not have full control of turning the device off. This undesirable effect had been reduced by increasing a bit the implantation dose that cause the V_{th} to be increased, and yet lowering the I_{off}.

Table 4.5 : I_{off} obtained for 500nm,250nm and 180nm devices

Gate Length/ Parameters	**500nm**	**250nm**		**180nm**	
		Before V_{th} adjustment	**After V_{th} adjustment**	**Before V_{th} adjustment**	**After V_{th} adjustment**
Log I_d	-12	-11.8	-12.2	-7.125	-7.25
I_{off}	1pA/μm	1.58pA/μm	0.631pA/μm	74.99nA/μm	56.23nA/μm

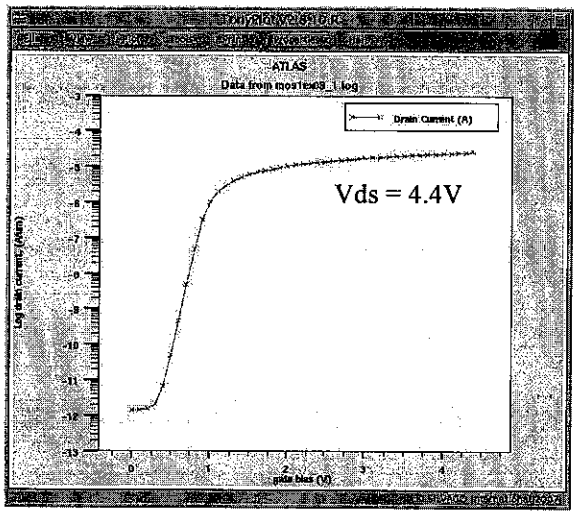


Figure 4.6(a) : Log I_d-V_{gs} with Vds=4.4 V for 500nm

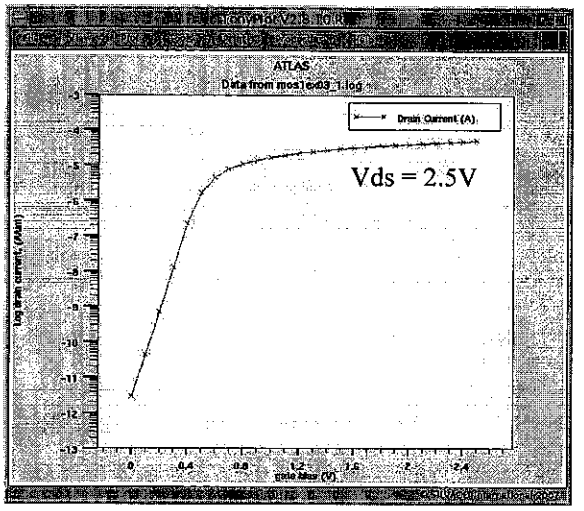


Figure 4.6(b) : Log I_d-V_{gs} with Vds= 2.5 V for 250nm(before implantation adjustment)

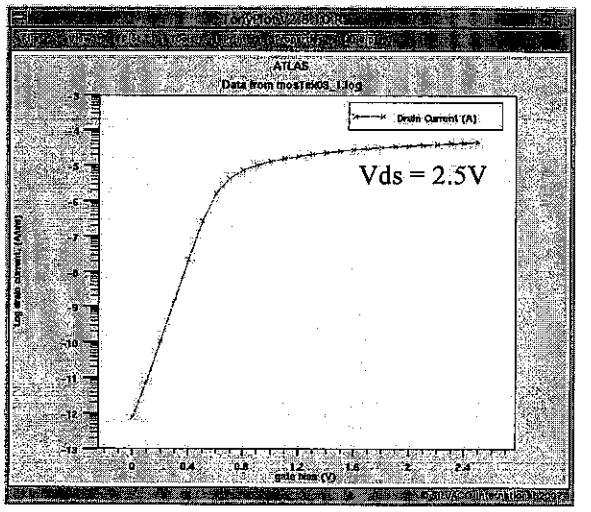


Figure 4.6(c) : Log I_d-V_{gs} with Vds=2.5 V for 250nm (after implantation adjustment)

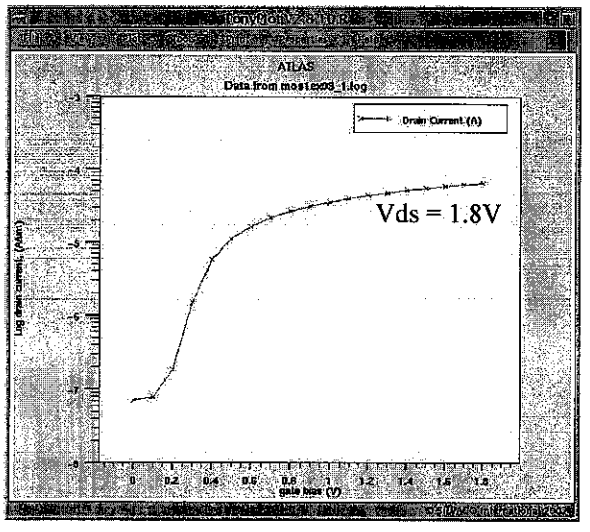


Figure 4.6(d) : Log I_d-V_{gs} curve with Vds=1.8 V for 180nm (before implantation adjustment)

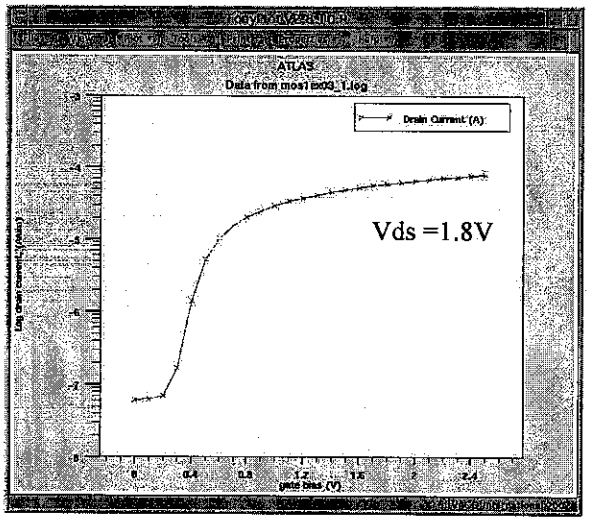


Figure 4.6(e) : Log I_d-V_{gs} curve with Vds=1.8V for 180nm (after implantation adjustment)

4.2.4 Increase of Subthreshold Swing, S_t

The subthreshold swing , S_t is a measure of how much a change in V_g(below V_{th}) is required to change the off current in device by a decade. A small value of S_t is desirable as it implicate that only a small reduction of V_g below V_{th} can effectively turn off the device while a large S_t value implicates that a significantly large I_d may still flow in the OFF state when V_g=0V [14] .

The subthreshold swing $S_t = d(V_g) / d \log[10]I_d$ in a MOSFET is expected to be decreased significantly as gate length is reduced before finally increasing catastrophically when gate length becomes so short that punchthrough current flows [15]. Based on the results obtained, the S_t values decreased as the gate length been reduced from 500nm to 250 nm. Punchthrough occurred, as the gate length been further reduced to 180nm, in which the S_t observed to increase to 108.894mV/dec. Results obtained meet expected result, shown in Table 4.6.

Table 4.6: Subthreshold swing(S_t) obtained for 500nm,250nm and 180nm devices

Gate Length/ Parameters	500nm	250nm		180nm	
		Before V_{th} adjustment	After V_{th} adjustment	Before V_{th} adjustment	After V_{th} adjustment
S_t (mV/dec)	99.098	79.723	86.293	108.894	109.038

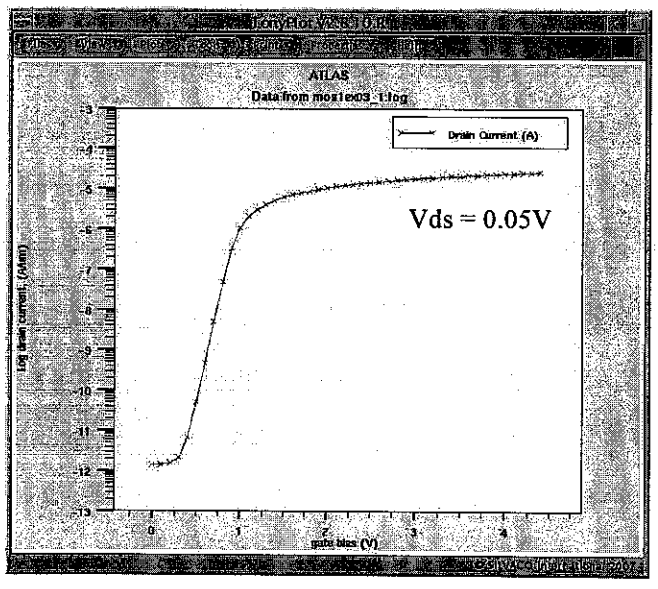


Figure 4.7(a) : Log I_d-V_{gs} curve with Vds=0.05V

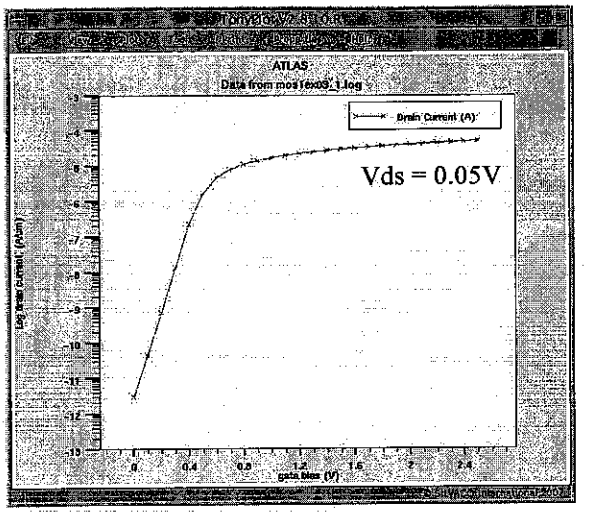


Figure 4.7(b) : Log I_d-V_{gs} curve with Vds=0.05V for 250nm(before implantation adjustment)

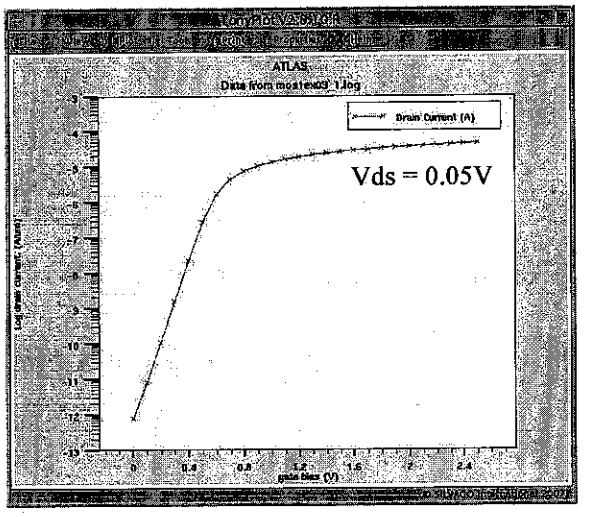


Figure 4.7(c) : Log I_d-V_{gs} curve with Vds=0.05V for 250nm (after implantation adjustment)

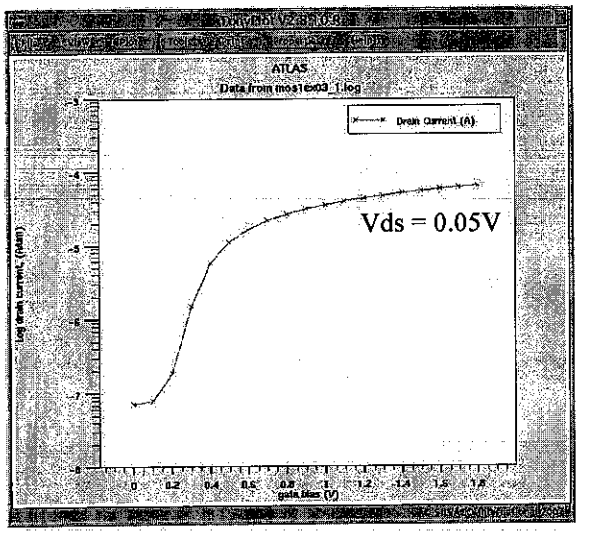


Figure 4.7(d) : Log I_d-V_{gs} curve with Vds=0.05V for 180nm (before implantation adjustment)

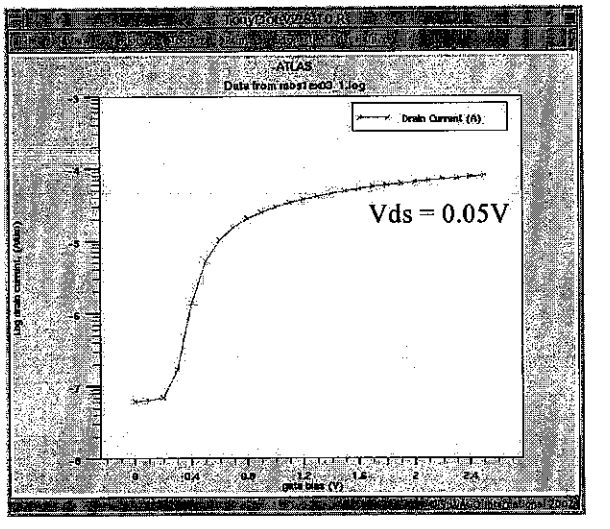


Figure 4.7(e) : Log I_d-V_{gs} curve with Vds=0.05V for 180nm (after implantation adjustment)

Large V_{th} is desirable in order to reduce I_{off}. But, it cannot solve the I_{on} reduction problem. Instead, the higher V_{th} had caused the I_{on} to be reduced as the device been scaled down. That is the reason why the S_t results been obtained for the adjusted V_{th} had been increased. As been said earlier, high S_t should be avoided since higher value means that the device had lower speed to turn off. Hence, to reduce S_t, it can be done by increasing oxide capacitance that is by using a thinner oxide thickness. An additional way to reduce S_t, is to operate the transistors at a lower temperature. This approach is valid in principal but rarely used because cooling adds considerable cost.

Based on overall results obtained, it is realized as well that there is trade-off between I_{on} and I_{off}. Higher I_{on} goes hand-in-hand with larger I_{off} [14]. During the threshold voltage adjustment, I_{off} was reduced , resulting the I_{on} to be reduced as well. The low I_{on} values were undesirable but still acceptable as it fall between the ranges been specified by the ITRS.

There are several techniques at the border between device technology and circuit design that can help to relax the conflict between I_{on} and I_{off}. In a large circuit such as a microprocessor, only some circuit blocks need to operate at high speed at a given time and other circuit blocks operate at lower speed or are idle. Circuit designer can set circuit to two or three (or even more) V_{th} to be chosen. V_{th} can thus be set relatively low to produce large I_{on} so that circuits that need to operate at high speed can do so, and vice versa.

A similar strategy is to provide multiple V_{dd} rather than multiple V_{th}. A higher V_{dd} is provided to a small number of circuits that need speed while a lower V_{dd} is used in the other circuits. This would allow a relatively large V_{th} to be used in order to suppress leakage.

CHAPTER 5

CONCLUSIONS & RECOMMENDATIONS

This chapter summarizes and concludes the project, together with recommendations for future studies.

5.1 Conclusions

Overall, the biggest challenge in completing this project was to find the best recipe for device fabrication. However, at the end of the semester, the researcher had successfully reached the objectives by initially fabricating, followed by conducting the device simulation to prove that SCE had occurred on the short channel devices. Among SCEs verified are; V_{th} and I_d saturation (I_{on}) reduction, as well as increase in off-state leakage and subthreshold slope. However, some of them had been tackled by increasing the V_{th} that lead to a lower I_{off} . That is the benefit gained by doing the adjustment during the boron implantation. Nevertheless, as the I_{off} been reduced, the I_{on} been reduced as well, which is not preferable. Thus, I_d saturation can be maintained high by lowering the subthreshold slope, S_t. This trade-off is critical and needs thorough judgment in order to maintain the device to the best requirement been set by ITRS.

In short, scaling improves cost, speed, and power per function with every new technology generation. All of these attributes have been improved by 10 to 100 million times in four decades and is expected to continue. Though a direct scaling approach is feasible in performing the device miniaturization, it is still insufficient. Rather, new structures or techniques need to be implied during the design to obtain an optimized performance which been further explained in the recommendations part .

5.2 Recommendations for Future Works

5.2.1 Use of high 'K' dielectrics

Based on Figure 5.1, the thickness of the SiO_2 as the gate insulator for silicon MOSFET since 1960's decreases as the technologies is scaled down [14]. The thin oxide layer is desirable. But to some extent, due to the decreased thickness, the oxide layer fails to act as a perfect insulator and the current flows through it, called tunneling leakage.

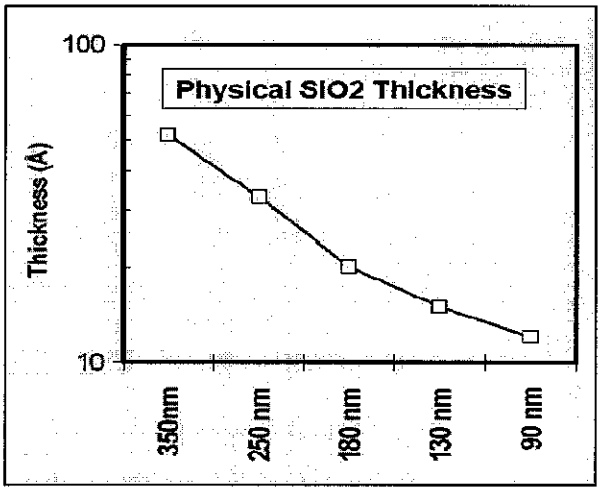


Figure 5.1 : Scales of oxide thickness versus channel length [14].

By using thick oxides with high dielectric it can help to optimize gate control over the channel. These thick oxide layers reduce the tunneling leakage. That means, the thickness of the oxide layer can be increased without any change in the capacitive affect produced. High-k dielectrics such as Hafnium Oxide(HfO2) can be used to replace SiO_2 which has a relative dielectric constant (k) of approximately 24, six times large than that of SiO_2. A 6nm thick HfO2 film is equivalent to 1nm thick SiO_2 in the sense that both films produce the same oxide capacitance. Other high-k gate dielectric can be used are Aluminium Oxide(Al2O3) and Zirconium Oxide(ZrO2) [14].

5.2.2 Use of silicide to replace polysilicon

Polysilicon cannot meet the demand of submicron device because it has high resistance when the size is small. The impact is, it used more power and also increased the time of resistor-capacitor, RC. Silicide is introduced to overcome this problem. It has high resistivity compared to polysilicon. Silicide layer is fabricated above the polysilicon gate. Metal will be located above the polysilicon layer with moderately high temperature application, then the silicide metal will be designed [10].

5.2.3 Halo implantation

Halo implantation is introduced to overcome or minimize the short channel effect such as threshold-voltage roll off. As illustrated in the Figure 5.2, large angle tilt, LAT is introduced. This will produce the P region, looks like semielliptical at both active region, n^+ of the transistor [10].

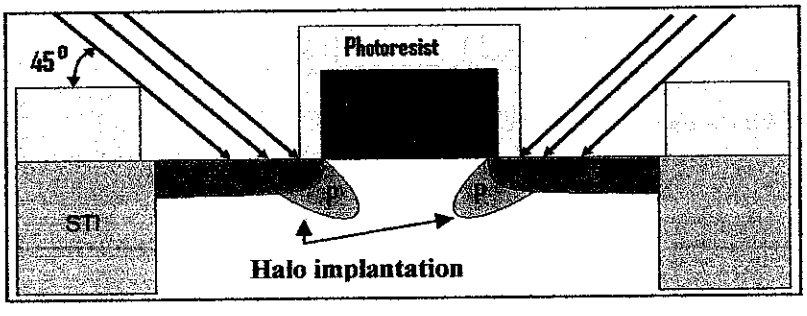


Figure 5.2: Halo Implantation Process [10]

The threshold voltage for halo devices is high based on Figure 5.3 ,which is a desirable phenomenon. This occurs due to the interaction between the halo charges with those implanted for V_{th} adjusts. On the other hand, the no halo transistors show a clear degradation of V_{th} with channel length reduction, due to short-channel effects, which is not desirable.

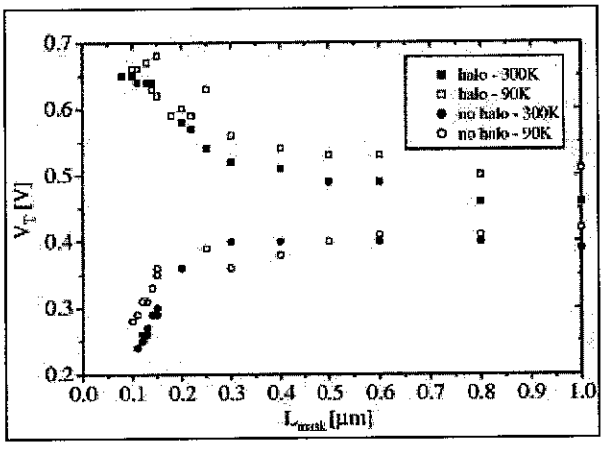


Figure 5.3: The extracted threshold voltage as a function of channel length (L_{mask}) for different temperature [14].

Another way to improve threshold voltage roll-off is by decreasing the temperature down to 90 K, as observed in the above figure. The temperature decrease causes a reduction in the horizontal electric field and the minimum channel length for a similar threshold voltage degradation decreases to about 0.15 µm.

From the above, it can be concluded that there is still a wide area waiting to be explored in the domain of MOS devices, all with the aim to produce a high performance device.

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APPENDICES

ATHENA and ATLAS simulation for 500nm device

```
go athena

# Non-Uniform Grid(0.6umx0.8um)
line x loc=0.00 spac=0.10
line x loc=0.20 spac=0.01
line x loc=0.60 spac=0.01
#
line y loc=0.00 spac=0.008
line y loc=0.2 spac=0.01
line y loc=0.5 spac=0.05
line y loc=0.8 spac=0.15

# Initial Silicon Structure with <100> Orientation
init silicon c.boron=1.0e14 orientation=100 two.d

# Gate Oxidation
diffus time=11 temp=926.966 dryo2 press=0.984283 hcl.pc=3

#
extract name="Gateoxide" thickness material="SiO~2" mat.occno=1 x.val=0.3

# Threshold Voltage Adjust implant
implant boron dose=2.8e12 energy=10 rotation=31 crystal lat.ratio1=1.0 \
     lat.ratio2=1.0
structure outfile=boron_doping.str

# Conformal Polysilicon Deposition
deposit poly thick=0.20 divisions=10
structure outfile=poly.str

# Poly Definition
etch poly left p1.x=0.35
structure outfile=poly2.str

# Polysilicon Oxidation
method compress init.time=0.10 fermi
diffus time=3 temp=900 weto2 press=1.00 hcl.pc=0
structure outfile=poly_oxidation.str

# Polysilicon Doping
implant phosphor dose=3.0e13 energy=20 rotation=31 crystal lat.ratio1=1.0 \
     lat.ratio2=1.0
structure outfile=poly_doping.str

# Spacer Oxide Deposition
deposit oxide thick=0.12 divisions=10
structure outfile=spacer_deposition.str
```

```
# Spacer Oxide Etch
etch oxide dry thick=0.12
structure outfile=spacer.str

# Source/Drain Implant
implant arsenic dose=5.0e15 energy=50 rotation=31 crystal lat.ratio1=1.0 \
      lat.ratio2=1.0
structure outfile=oxide_etch.str

# Source/Drain Annealing
method vertical init.time=0.06 fermi
diffus time=1 temp=900 nitro press=1.00
structure outfile=source_drain_anneal.str

# Open Contact Window
etch oxide left p1.x=0.20
structure outfile=etch_left.str

# Aluminium Deposition
deposit alumin thick=0.03 divisions=2
structure outfile=aluminium_depo.str

# Etch Aluminium
etch aluminum right p1.x=0.18
structure outfile=aluminium_etch.str

#
extract name="nxj" xj material="Silicon" mat.occno=1 x.val=0.2 junc.occno=1
#
extract name="n++ sheet res" sheet.res material="Silicon" mat.occno=1 \
      x.val=0.05 region.occno=1
#
extract name="ldd sheet resistance" sheet.res material="Silicon" mat.occno=1 \
      x.val=0.3 region.occno=1
#
extract name="1dvt" 1dvt ntype qss=1e10 x.val=0.5
#
struct mirror right
#
electrode name=source x=0.10 y=0
#
electrode name=drain x=1.10 y=0
#
electrode name=gate x=0.60 y=-0.20
#
electrode name=backside backside
#
# plot the structure
structure outfile=mos1ex01_0.str
```

```
############ Vt Test : Returns Vt################
go atlas

# set material models
models cvt srh print

contact name=gate n.poly
interface qf=3e10

method newton
solve init

# Bias the drain
solve vdrain=0.1

# Ramp the gate
log outf=mos1ex01_1.log master
solve vgate=0 vstep=0.1 vfinal=4.4 name=gate
save outf=mos1ex01_1.str

# plot results
tonyplot  mos1ex01_1.log -set mos1ex01_1_log.set

# extract device parameters
extract name="nvt" (xintercept(maxslope(curve(abs(v."gate"),abs(i."drain")))) \
        - abs(ave(v."drain"))/2.0)


################################Id-Vd for 500 nm#########################
go atlas
#

Define the Gate Qss
Interface qf=1e10

#Use the cvt mobility model for MOS
models cvt srh print  numcarr=2

#method gummel  newton

solve init
solve vdrain=0

solve vgate=1.1 outf=solve1
solve vgate=2.2 outf=solve2
solve vgate=3.3 outf=solve3
solve vgate=4.4 outf=solve4

#load  infile=solve1
log outf= nmos_500_1
solve name=drain vdrain=0 vfinal=4.4 vstep=0.05
```

```
#load  infile=solve2
log outf= nmos_500_2
solve name=drain vdrain=0 vfinal=4.4 vstep=0.05

#load  infile=solve3
log outf= nmos_500_3
solve name=drain vdrain=0 vfinal=4.4 vstep=0.05

#load infile=solve4
log outf= nmos_500_4
solve name=drain vdrain=0 vfinal=4.4 vstep=0.05

tonyplot -overlay nmos_500_1.log nmos_500_2.log nmos_500_3.log nmos_500_4-set nmos.set
quit

################ Ioff ###################
go atlas

# set material models
models cvt srh print
contact name=gate n.poly
interface qf=3e10

# get initial solution

solve init

method gummel newton
solve prev

# Bias the drain a bit...
solve vdrain=0 vstep=0.05 vfinal=4.4 name=drain

#Ramp the gate to a volt
log outf=mos1ex04_1.log master
solve name=gate vgate=0 vfinal=4.4 vstep=0.1
save outf=mos1ex04_1.str

#extract the device parameter Ioff
extract init inf="mos1ex04_1.log"
extract name="loff" 10^(y.val from curve (v."gate",log10(i."drain"))\
where x.val=0)
tonyplot mos1ex04_1.log -set mos1ex04_1_log.set

################SubV,###################
go atlas

# set material models
models cvt srh print
contact name=gate n.poly
interface qf=3e10
```

```
# get initial solution
solve init

method gummel newton
solve prev

# Bias the drain a bit...
solve vdrain=0 vstep=0.01 vfinal=0.05 name=drain

#Ramp the gate to a volt
log outf=mos1ex04_1.log master
solve name=gate vgate=0 vfinal=4.4 vstep=0.1
save outf=mos1ex04_1.str

#extract the device parameter SubVt
extract init inf="mos1ex04_1.log"
extract name="nsubvt" 1.0/slope(maxslope(curve(abs(v."gate"),log10(abs(i."drain")))))
tonyplot mos1ex04_1.log -set mos1ex04_1_log.set
```

ATHENA and ATLAS simulation for 250nm device

```
go athena

# Non-Uniform Grid(0.3umx0.4um)
line x loc=0.00 spac=0.05
line x loc=0.10 spac=0.005
line x loc=0.30 spac=0.005
#
line y loc=0.00 spac=0.004
line y loc=0.1 spac=0.005
line y loc=0.25 spac=0.025
line y loc=0.4 spac=0.075

# Initial Silicon Structure with <100> Orientation
init silicon c.boron=1.0e14 orientation=100 two.d

# Gate Oxidation
diffus time=3.5 temp=926.966 dryo2 press=0.984283 hcl.pc=3

#extract name="Gateoxide" thickness material="SiO~2" mat.occno=1 x.val=0.15

# Threshold Voltage Adjust implant
implant boron dose=2.8e12 energy=8 rotation=31 crystal lat.ratio1=1.0 \
     lat.ratio2=1.0
structure outfile=boron_doping1.str

# Conformal Polysilicon Deposition
deposit poly thick=0.10 divisions=10
structure outfile=polys1.str
```

```
# Poly Definition
etch poly left p1.x=0.175
structure outfile=poly21.str

# Polysilicon Oxidation
method compress init.time=0.10 fermi
diffus time=1.5 temp=900 weto2 press=1.00 hcl.pc=0
structure outfile=poly_oxidation1.str

# Polysilicon Doping
implant phosphor dose=3.0e13 energy=10 rotation=31 crystal lat.ratio1=1.0 \
      lat.ratio2=1.0
structure outfile=poly_doping1.str

# Spacer Oxide Deposition
deposit oxide thick=0.06 divisions=10
structure outfile=spacer_deposition1.str

# Spacer Oxide Etch
etch oxide dry thick=0.06
structure outfile=spacer1.str

# Source/Drain Implant
implant arsenic dose=5.0e15 energy=25 rotation=31 crystal lat.ratio1=1.0 \
      lat.ratio2=1.0
structure outfile=oxide_etch1.str

# Source/Drain Annealing
method vertical init.time=0.06 fermi
diffus time=1 temp=900 nitro press=1.00
structure outfile=source_drain_anneal1.str

# Open Contact Window
etch oxide left p1.x=0.1
structure outfile=etch_left1.str

# Aluminium Deposition
deposit alumin thick=0.015 divisions=1
structure outfile=aluminium_depo1.str

# Etch Aluminium
etch aluminum right p1.x=0.09
structure outfile=aluminium_etch1.str

#extract name="nxj" xj material="Silicon" mat.occno=1 x.val=0.1 junc.occno=1

#extract name="n++ sheet res" sheet.res material="Silicon" mat.occno=1 \
      x.val=0.025 region.occno=1

#extract name="ldd sheet resistance" sheet.res material="Silicon" mat.occno=1 \
      x.val=0.15 region.occno=1
```

```
#
extract name="1dvt" 1dvt ntype qss=1e10 x.val=0.25
#
struct mirror right
#
electrode name=source x=0.05 y=0
#
electrode name=drain x=0.55 y=0
#
electrode name=gate x=0.30 y=-0.05
#
electrode name=backside backside
#
# plot the structure
structure outfile=mos1ex01_0.str

############## Vt Test : Returns Vt#################
go atlas

# set material models
models cvt srh print

contact name=gate n.poly
interface qf=3e10

method newton
solve init

# Bias the drain
solve vdrain=0.1

# Ramp the gate
log outf=mos1ex01_1.log master
solve vgate=0 vstep=0.1 vfinal=2.5 name=gate
save outf=mos1ex01_1.str

# plot results
tonyplot  mos1ex01_1.log -set mos1ex01_1_log.set

# extract device parameters
extract name="nvt" (xintercept(maxslope(curve(abs(v."gate"),abs(i."drain")))) \
            -    abs(ave(v."drain"))/2.0)

#################################Id-Vd for 250 nm#########################
go atlas
#Define the Gate Qss
Interface qf=1e10

#Use the cvt mobility model for MOS
models cvt srh print  numcarr=2
#method gummel  newton
```

```
solve init
solve vdrain=0

solve vgate=0.625 outf=solve1
solve vgate=1.25  outf=solve2
solve vgate=1.875 outf=solve3
solve vgate=2.5   outf=solve4

#load  infile=solve1
log outf= nmos_250_1
solve name=drain vdrain=0 vfinal=2.5 vstep=0.05

#load  infile=solve2
log outf= nmos_250_2
solve name=drain vdrain=0 vfinal=2.5 vstep=0.05

#load  infile=solve3
log outf= nmos_250_3
solve name=drain vdrain=0 vfinal=2.5 vstep=0.05

#load infile=solve4
log outf= nmos_250_4
solve name=drain vdrain=0 vfinal=2.5 vstep=0.05

tonyplot -overlay nmos_250_1.log nmos_250_2.log nmos_250_3.log nmos_250_4-set nmos.set
quit

################## Ioff ####################
go atlas

# set material models
models cvt srh print
contact name=gate n.poly
interface qf=3e10

# get initial solution
solve init

method gummel newton
solve prev
# Bias the drain a bit...
solve vdrain=0 vstep=0.05 vfinal=2.5 name=drain

#Ramp the gate to a volt
log outf=mos1ex04_1.log master
solve name=gate vgate=0 vfinal=2.5 vstep=0.1
save outf=mos1ex04_1.str

#extract the device parameter Ioff
extract init inf="mos1ex04_1.log"
extract name="Ioff" 10^(y.val from curve (v."gate",log10(i."drain"))\
```

```
where x.val=0)
tonyplot mos1ex04_1.log -set mos1ex04_1_log.set

##################SubVt####################
go atlas

# set material models
models cvt srh print
contact name=gate n.poly
interface qf=3e10

# get initial solution
solve init

method gummel newton
solve prev

# Bias the drain a bit...
solve vdrain=0 vstep=0.01 vfinal=0.05 name=drain

#Ramp the gate to a volt
log outf=mos1ex04_1.log master
solve name=gate vgate=0 vfinal=2.5 vstep=0.1
save outf=mos1ex04_1.str

#extract the device parameter SubVt
extract init inf="mos1ex04_1.log"
extract name="nsubvt" 1.0/slope(maxslope(curve(abs(v."gate"),log10(abs(i."drain")))))
tonyplot mos1ex04_1.log -set mos1ex04_1_log.set
```

ATHENA and ATLAS simulation for 180nm device

```
go athena

# Non-Uniform Grid(0.216umx0.2879um)
line x loc=0.00 spac=0.0359
line x loc=0.072 spac=0.00359
line x loc=0.216 spac=0.00359
#
line y loc=0.00 spac=0.00288
line y loc=0.0719 spac=0.00359
line y loc=0.1799 spac=0.0179
line y loc=0.2879 spac=0.0539

# Initial Silicon Structure with <100> Orientation
init silicon c.boron=1.0e14 orientation=100 two.d

# Gate Oxidation
diffus time=1.7 temp=926.966 dryo2 press=0.984283 hcl.pc=3
```

```
#extract name="Gateoxide" thickness material="SiO~2" mat.occno=1 x.val=0.108

# Threshold Voltage Adjust implant
implant boron dose=2.8e12 energy=6 rotation=31 crystal lat.ratio1=1.0 \
      lat.ratio2=1.0
structure outfile=boron_doping2.str

# Conformal Polysilicon Deposition
deposit poly thick=0.0719 divisions=10
structure outfile=polys2.str

# Poly Definition
etch poly left p1.x=0.126
structure outfile=poly22.str

# Polysilicon Oxidation
method compress init.time=0.10 fermi
diffus time=1.079 temp=900 weto2 press=1.00 hcl.pc=0
structure outfile=poly_oxidation2.str

# Polysilicon Doping
implant phosphor dose=3.0e13 energy=7.199 rotation=31 crystal lat.ratio1=1.0 \
      lat.ratio2=1.0
structure outfile=poly_doping2.str

# Spacer Oxide Deposition
deposit oxide thick=0.0432 divisions=10
structure outfile=spacer_deposition2.str

# Spacer Oxide Etch
etch oxide dry thick=0.0432
structure outfile=spacer2.str

# Source/Drain Implant
implant arsenic dose=5.0e15 energy=17.99 rotation=31 crystal lat.ratio1=1.0 \
      lat.ratio2=1.0
structure outfile=oxide_etch2.str

# Source/Drain Annealing
method vertical init.time=0.06 fermi
diffus time=1 temp=900 nitro press=1.00
structure outfile=source_drain_anneal2.str

# Open Contact Window
etch oxide left p1.x=0.0719
structure outfile=etch_left2.str

# Aluminium Deposition
deposit alumin thick=0.01079 divisions=1
structure outfile=aluminium_depo2.str
```

```
# Etch Aluminium
etch aluminum right p1.x=0.0648
structure outfile=aluminium_etch2.str

#extract name="nxj" xj material="Silicon" mat.occno=1 x.val=0.0719 junc.occno=1

#extract name="n++ sheet res" sheet.res material="Silicon" mat.occno=1 \
      x.val=0.0179 region.occno=1

#extract name="ldd sheet resistance" sheet.res material="Silicon" mat.occno=1 \
      x.val=0.108 region.occno=1
#
extract name="1dvt" 1dvt ntype qss=1e10 x.val=0.1799
#
struct mirror right
#
electrode name=source x=0.0359 y=0
#
electrode name=drain x=0.396 y=0
#
electrode name=gate x=0.216 y=-0.04
#
electrode name=backside backside
#
# plot the structure
structure outfile=mos1ex01_0.str

############## Vt Test : Returns Vt#################
go atlas

# set material models
models cvt srh print

contact name=gate n.poly
interface qf=3e10

method newton
solve init

# Bias the drain
solve vdrain=0.1

# Ramp the gate
log outf=mos1ex01_1.log master
solve vgate=0 vstep=0.1 vfinal=1.8 name=gate
save outf=mos1ex01_1.str

# plot results
tonyplot  mos1ex01_1.log -set mos1ex01_1_log.set

# extract device parameters
```

```
extract name="nvt" (xintercept(maxslope(curve(abs(v."gate"),abs(i."drain")))) \
        - abs(ave(v."drain"))/2.0)

##################################Id-Vd for 180 nm##########################
go atlas
#
Define the Gate Qss
Interface qf=1e10

#Use the cvt mobility model for MOS
models cvt srh print  numcarr=2

#method gummel  newton

solve init
solve vdrain=0

solve vgate=0.45 outf=solve1
solve vgate=0.9   outf=solve2
solve vgate=1.35 outf=solve3
solve vgate=1.8   outf=solve4

#load   infile=solve1
log outf= nmos_180_1
solve name=drain vdrain=0 vfinal=1.8 vstep=0.025

#load   infile=solve2
log outf= nmos_180_2
solve name=drain vdrain=0 vfinal=1.8 vstep=0.025

#load   infile=solve3
log outf= nmos_180_3
solve name=drain vdrain=0 vfinal=1.8 vstep=0.025

#load infile=solve4
log outf= nmos_180_4
solve name=drain vdrain=0 vfinal=1.8 vstep=0.025

tonyplot -overlay nmos_180_1.log nmos_180_2.log nmos_180_3.log nmos_180_4-set nmos.set
quit

################ Ioff ####################
go atlas

# set material models
models cvt srh print
contact name=gate n.poly
interface qf=3e10

# get initial solution
```

```
solve init
method gummel newton
solve prev
# Bias the drain a bit...
solve vdrain=0 vstep=0.05 vfinal=1.8 name=drain

#Ramp the gate to a volt
log outf=mos1ex04_1.log master
solve name=gate vgate=0 vfinal=1.8 vstep=0.1
save outf=mos1ex04_1.str

#extract the device parameter Ioff
extract init inf="mos1ex04_1.log"
extract name="Ioff" 10^(y.val from curve (v."gate",log10(i."drain"))\
where x.val=0)
tonyplot mos1ex04_1.log -set mos1ex04_1_log.set

##################SubVt####################
go atlas

# set material models
models cvt srh print
contact name=gate n.poly
interface qf=3e10

# get initial solution

solve init
method gummel newton
solve prev

# Bias the drain a bit...
solve vdrain=0 vstep=0.01 vfinal=0.05 name=drain

#Ramp the gate to a volt
log outf=mos1ex04_1.log master
solve name=gate vgate=0 vfinal=1.8 vstep=0.1
save outf=mos1ex04_1.str

#extract the device parameter SubVt
extract init inf="mos1ex04_1.log"
extract name="nsubvt" 1.0/slope(maxslope(curve(abs(v."gate"),log10(abs(i."drain")))))
tonyplot mos1ex04_1.log -set mos1ex04_1_log.set
```

Results Obtained(result.final)

#500 (boron implantation = 28e11)

Gateoxide=101.656 angstroms (0.0101656 um) X.val=0.3
nxj=0.573334 um from top of first Silicon layer X.val=0.2
n++ sheet res=28.8225 ohm/square X.val=0.05
ldd sheet resistance=1680.01 ohm/square X.val=0.3
1dvt=0.989772V X.val=0.5
vt = 0.882935 V

****

#250_b4 adjustment (boron implantation = 28e11)

nxj=0.371302 um from top of first Silicon layer X.val=0.1
n++ sheet res=36.0535 ohm/square X.val=0.025
ldd sheet resistance=1993.37 ohm/square X.val=0.15
1dvt=0.55019 V X.val=0.25
vt = 0.4346 V

****

#250_after_adjustment (boron implantation = 33.5e11)

Gateoxide=50.1269 angstroms (0.00501269 um) X.val=0.15
nxj=0.371064 um from top of first Silicon layer X.val=0.1
n++ sheet res=36.0584 ohm/square X.val=0.025
ldd sheet resistance=2032 ohm/square X.val=0.15
1dvt=0.625647 V X.val=0.25
vt=0.526026 V

****

#180_b4 (boron implantation = 28e11)

Gateoxide=35.3394 angstroms (0.00353394 um) X.val=0.108
n++ sheet res=39.3576 ohm/square X.val=0.0179
ldd sheet resistance=826.959 ohm/square X.val=0.108
1dvt=0.437878 V X.val=0.1799
vt=0.336977 V

****

#180_after_adjustment ((boron implantation = 35e11)

Gateoxide=35.3394 angstroms (0.00353394 um) X.val=0.108
n++ sheet res=39.3612 ohm/square X.val=0.0179
ldd sheet resistance=833.366 ohm/square X.val=0.108
1dvt=0.52558 V X.val=0.1799
vt=0.391928V

Table 1: Key characteristics of MOS Device Models for different technology generation

Technology Generation	600nm	350nm	250nm	180nm	130nm	100nm	70nm	50nm
L_{DRAWN} (nm)	600	350	250	140	90	65	45	32
V_{DD} (V)	5.0	3.3	2.5	1.8	1.5	1.2	0.9	0.6
TOX (nm)	11	7.6	4.0	2.5	1.9	1.5	1.2	0.8
V_{TH} (V)	1.0	0.735	0.596	0.466	0.407	0.344	0.277	0.205

Source : http://www.cs.utexas.edu/users/cart

Table 2: Parameters specified by ITRS dan BPTM

Technology	**L_G (µm)**	**T_{OX} (nm)**	**V_{TH} (V)**	**V_{DD} (V)**
			NMOS	
130nm	0.13±15%	3.3±4%	0.33±12.7%	1.5±10%
90nm	0.09±15%	2.5±4%	0.26±12.7%	1.2±10%
70nm	0.07±15%	1.7±4%	0.20±12.7%	0.9±10%

Source : California University 2002

Table 3: 250nm scaling parameters from ITRS Roadmap

I_{ON}	600 µA/µm	T_{ox}	40 - 50 Å
I_{OFF}	1 nA/µm	X_J (shallow LDD)	50 – 100 nm
$Log(I_{ON} / I_{OFF})$	5.75 decades	N_D (LDD)	$2 - 5 \times 10^{18}$ cm^{-3}
SS	85 mV/decade	R_S (LDD)	400 – 850 Ω/sq
DIBL	< 100 mV/V	X_J (contact)	135 – 265 nm
V_{DD}	1.8 – 2.5 V	N_D (contact)	1×10^{20} cm^{-3}
$\lvert V_T \rvert$	0.5 V	X_J (SSRW channel)	50 – 100 nm

Source : L.Widson,ed , "The National Technology Roadmap for Semiconductors: 1997 Edition, Semiconductor Industry Association, San Jose California

* Note: The threshold voltage for 500nm,250nm and 180nm devices been referred to Table 1, Table 2 and Table 3 above