DESIGNING LOW VOLTAGE AND POWER CMOS OP AMP

By

Mohd Ridzuan Bin Yusoff

Final Project Report
Submitted to the Electrical & Electronics Engineering Programme
In partial fulfillment of
The requirements for the
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CERTIFICATION OF APPROVAL

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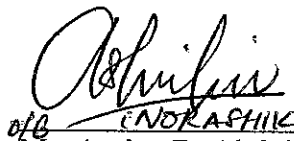
Approved by:



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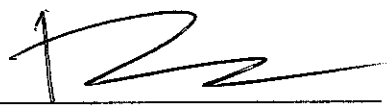
June 2007

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.



MOHD RIDZUAN BIN YUSOFF

ABSTRACT

The importance of using low supply voltage for analogue circuit has enormously increased in recent past. The recent trend shows that a supply voltage can be degraded until 1.5 V. Low power consumption also important to increase the battery life, the packaging density and circuit reliability. CMOS op amp technology today can have power consumption lower than 200 μW. The objective of this project is to design low supply voltage and low power consumption CMOS operational amplifier.

Low supply voltage op amp with 1.6 V has been successfully designed. The design was using bulk-driven PMOS transistors as an input differential of the op amp. The compensation capacitor was also used to control the power consumption. The op amp is capable of producing low power consumption of 20 μW. The layout was design using 0.35 μm technology and have gone through DRC and LVS check. Software Virtuoso Schematic Capture and Virtuoso Spectre Circuit Simulator from cadence have been used for schematic capture and design simulation. For layout design, DRC and LVS check, softwere Calibre from Mentor Graphic have been used.

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First of all, the deepest gratitude to Allah S.W.T. for his blessing and mercy, I managed to complete this Final Year Project.

Designing CMOS op amp is a great experience. From low level of knowledge about CMOS op amp I managed to complete this project. Special thank to my project supervisor, Ms Azrina Bt Abdul Aziz. Without her support and guidance, it is impossible to complete this project on time.

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Mohd Ridzuan Bin Yusoff

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LIST OF ABBREVIATIONS

Op amp	Operational Amplifier
CMOS	Complementary Metal Oxide Semiconductor
FET	Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
DC	Direct Current
IC	Integrated Circuit
CMRR	Common Mode Rejection Ratio
SR	Slew Rate
ICMR	Input Common Mode Range
W	Width of Transistor
L	Length of Transistor
CPU	Central Processing Unit
DRC	Design Rule Check
LVS	Layout Versus Schematic
g_m	Transconductance
C_c	Compensation Capacitor
A_v	Voltage Gain
A_d	Differential Gain
A_c	Common Mode Gain

CHAPTER 1

INTRODUCTION

1.1. Background of Study

An operational amplifier, usually referred to as an "op-amp", is a DC-coupled high-gain electronic voltage amplifier with differential inputs and, usually, a single output. In its ordinary usage, the output of the op-amp is controlled by negative feedback which, because of the amplifier's high gain, almost completely determines the output voltage for any given input.

The operational amplifier was originally designed to perform mathematical operations by using voltage as an analogue of another quantity. This is the basis of the analogue computer where op-amps were used to model the basic mathematical operations (addition, subtraction, integration, differentiation, and so on). However, an ideal operational amplifier has many applications beyond mathematical operations [7].

Op amps were originally developed in the vacuum tube era, where they were used in analog computers. Op amps are now normally implemented as integrated circuits (ICs), though versions with discrete components are used when performance beyond that attainable with ICs is required [7]. Figure 1 shows an image of vacuum tube era op amp.

The first integrated op amp available is the bipolar Fairchild μA709 in the late 1960. It was rapidly out of date by the 741, which has better performance and is more stable and easier to use. Introducing design based on FET on late 1970 and MOSFET on early 1980 have rapidly increased the performance of op amp [7]. Integrated circuit based on the MOSFET is called CMOS.

CMOS is currently the most widely used IC technology for both analog and digital as well as combined analog and digital technology (or mixed-signal) applications. CMOS technology has rapidly embraced the field of analog integrated circuit, providing low cost, high performance solutions and rising to dominate the market. While silicon bipolar and III-IV devices still find recess application, only CMOS processes have emerged as a viable choice for integration for today's complex mixed signal systems [5].

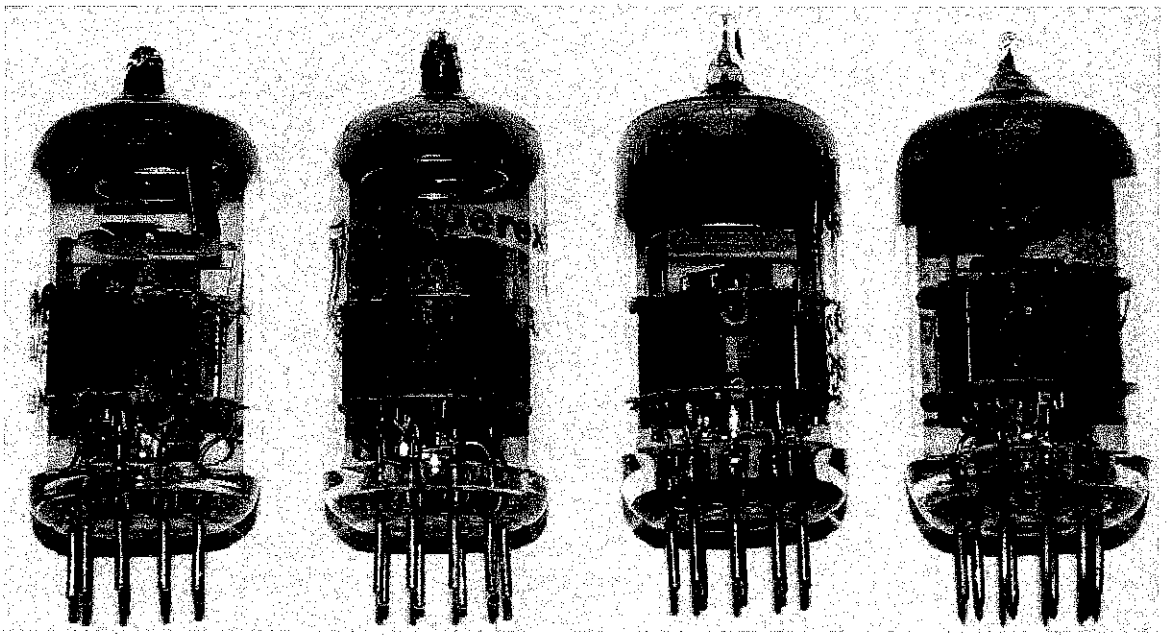

Figure 1: Vacuum tube op amp

According to Moore's Law, engineers can double the number of transistor on a chip every two years, largely by shrinking the size of existing transistor. Adding more transistors allows engineers to increase performance or integrate new functions [8]. It can also reduce power. Moore pointed out in his original paper that the doubling of the number of components on an integrated circuit was due to three factors. First, and most significant, half of the increase is derived from improvement in lithographic resolution. Second, 25% of the increase is due to larger chip sizes, made possible by enhanced manufacturing techniques and better lithography. Third, the remaining 25% is due to innovation, such as more creative techniques for forming the components,

predominantly transistors, on a chip. These three factors are the driving forces behind the trend for increasing the number of components on a chip [11]. With today's technology that can scale down channel length to 0.1 μm, low dc supply voltage is required [5]. Figure 2 shows the growth of transistors in Intel CPU's according to Moore's Law

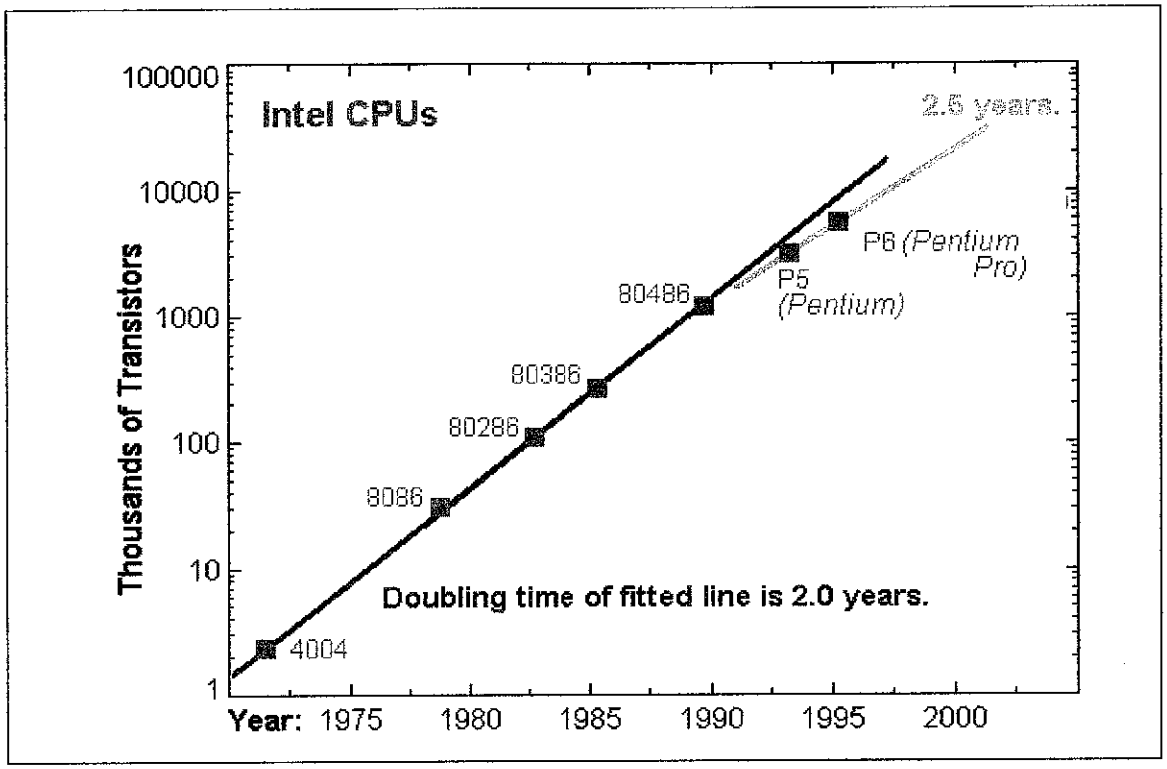

Figure 2: Growth of transistor for Intel CPU's according to Moore's law [8]

1.2. Problem Statement

Packaging a large number of devices on the same IC chip require a very small device dimensions. Today CMOS process technologies are capable of producing devices with 0.1μm channel length. Such small devices need to operate with dc voltage supplies close to 1 V [5]. Typical supply voltage used in analog circuit today is 2.5 – 3 V [3]. But the latest trend suggested that supply voltage can go down to 1.5 V and may less even [1], [3]. In my project, I will design the op amp that can operate with supply voltage in the range of 1 – 1.75 V.

Low power consumption is crucial to support such large component density. Low power consumption is important to ensure battery lives longer. The power consumption can be minimized by either reduced supply voltage or supply current. But the transistor noise is dependent on current. For current, there is certain limit of reduction. The best approach is by reducing supply voltage. The recent technology has reported that the power dissipation can be reduced till 200 μW [2]. For my design, the power consumption must be lowered than 200 μW.

1.3. Objective and Scope of Study

The objective of this project is to design CMOS op amp that has the following characteristics, low supply voltage below 1.75 V and low power consumption below 200 μW. The specification for the op amp must be defined first before designing the schematic. The important specifications are load capacitance, DC gain, unity gain frequency, phase margin, input common mode range and many more. The schematic will be designed based on the specification define earlier. The schematic drawn will then be simulated using software Virtuoso Schematic Editor and Virtuoso Spectre Circuit Simulator from Cadence.

The second part of the project is to design the layout of the op amp based on the schematic drawn before. The layout then will undergo the verification processes which are Design Rule Check (DRC) and Layout Versus Schematic (LVS) check. The layout design is then extracted. These procedures are performed using software Calibre from Mentor Graphic. The other objective of this project is to expose the author to the completed IC design flow process starting from the specification, design, validation, layout, verification until extraction.

CHAPTER 2

LITERATURE REVIEW AND THEORY

2.1. Low Voltage Op Amp

As CMOS technology continue to shrink in size, the supply voltage, threshold voltage and minimum channel length also decrease. The two critical problems in low supply voltage design are providing rail-to-rail common mode input range and output swing. The reduced in supply voltage also decrease circuit performance like bandwith and input/output swing. Reduction in supply voltage also will reduce the power consumption. Based on the references [1], [2], and [3], the lowest voltage supplied designed for the analog signal was 1.5 V.

My objective is to produce low voltage op amp in the range of 1-1.75 V. In an operational amplifier, when aiming for low supply voltage operation, the most critical part is to design the input stage. Due to this, I will adopt the design in reference [1] which is using the bulk-driven input. Figure 3 shows the MOSFET which is driven by the bulk.

The operation of bulk-driven MOSFET is of depletion type. The gate-source voltage is set to a value sufficient to turn on the transistor. Input voltage is then applied to the bulk terminal of the transistor to modulate the current flow through the resistor. The advantage of the bulk-driven device over a gate-driven device is that the threshold voltage limitation disappears and both positive and negative bias voltage is possible. This is especially important in analog circuits where the dynamic range of the signal should be maximize with respect to the supply voltage in order to maximize the performance of the circuit [1].

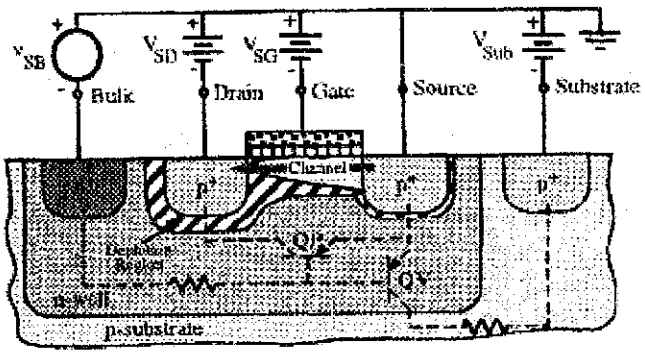

Figure 3: Cross section of a bulk driven MOSFET

There are also some drawbacks of bulk-driven devices compared to gate-driven devices, such as smaller transconductance (g_{mb} instead of g_m) because of smaller control capacitance of the depletion layer, larger parasitic capacitance to the substrate, which results in lower f_t, and higher input referred noise, because of smaller transconductance [1].

2.2. Low Power Op Amp

I will adopt the design in reference [2] to obtain low power consumption. This design employs the Miller effect by connecting a compensation capacitor C_c across the high gain stage. A design procedure for this type of op amp can be found in [9]. The value of compensation capacitor effect the noise error and power consumption. Decreasing the compensation capacitor causes reduced in power consumption but increases the noise level [2]. However, due to unintentional feed-forward path through the miller capacitor, a right half plane zero is also created and the phase margin is degraded. Such a zero can be removed if a proper nullifying resistor is inserted in series with the Miller capacitor [9].

The Miller effect describes the fact that a capacitance between input and output of an amplifier is multiplied by a factor of $(1 - A_v)$, where A_v is the voltage gain of the amplifier. Since, intuitively, a gain represents a voltage multiplication between points, any capacitor across these points will charge and discharge with a current which is multiplied by $(1 - A_v)$. In an amplifier with a negative gain, this effectively increases the apparent capacitance by a factor of $(1 - |A_v|)$ [12].

Consider an inverting amplifier with the voltage gain A_v, thus $V_2 = -A_v V_1$. Impedance Z_3 added between the input and output of the amplifier will exhibit the Miller effect. The input current is given by

$$I_1 = \frac{V_1 - V_2}{Z_3} \tag{2.1}$$

And the input impedance is

$$Z_{IN} = \frac{V_1}{I_1} = \frac{V_1 Z_3}{V_1(1 - A_v)} = \frac{Z_3}{1 - A_v} \tag{2.2}$$

Using $Z_3 = (j\omega C)^{-1}$, the resulting input impedance is

$$Z_{IN} = \frac{1}{j\omega C(1 - A_v)} \tag{2.3}$$

This means that the capacitance is effectively multiplied by the factor $(1 - A_v)$.

2.3. Basic Circuit in CMOS Op Amp

Basically all op amps have same the same subcircuit inside it which consists of current mirror, differential amplifier and class AB output stage. The basic characteristics of the subcircuit used in this project will be explained.

2.3.1. Differential Amplifier

A differential amplifier is a type of an amplifier that multiplies the difference between two inputs by some constant factor (the differential gain). A differential amplifier is the input stage of operational amplifiers. Figure 4 shows the differential amplifier formed from two identical transistor put in sideway as shown in the transistor M3 and M4.. While most differential amplifier circuits use two separate voltage supplies, the circuit can also operate using one voltage supply. A number of input signals are possible:

1. If an input signal is applied to either input with the other input connected to the ground, the operation is referred to as "single-ended"
2. If two opposite polarity input signal are applied, the operation is referred to as "double-ended"
3. If the same input is applied to both inputs, the operation is called "common mode"

In single ended operation, a single input signal is applied. However, due to the common-drain connection, the input signal operates both transistors, resulting an output from both sources.

In double-ended operation, two input signals are applied, the difference of the input resulting in outputs from both sources are produced. This is due to the difference signal applied to both inputs.

In common-mode operation, the common input signal results in opposite signal at each source. These signals canceling each other so that the resulting output signal is zero. As a practical matter, the opposite signals do not completely cancel and a small signal results.

The main feature of the differential amplifier is the very large gain when opposite signals is applied to the inputs as compared to the very small gain resulting from common inputs. Given two inputs V_{in}^{+} and V_{in}^{-}, a practical differential amplifier gives an output V_{out}:

$$V_{out} = A_d(V_{in}^{+} - V_{in}^{-}) + A_c\left(\frac{V_{in}^{+} + V_{in}^{-}}{2}\right) \tag{2.4}$$

where A_d is the differential-mode gain and A_c is the common-mode gain.

The common-mode rejection ratio is usually defined as the ratio between differential-mode gain and common-mode gain:

$$\mathrm{CMRR} = \frac{A_d}{A_c} \tag{2.5}$$

From the above equation, we can see that as A_c approaches zero, CMRR approaches infinity. The higher the resistance of the current source, R_e, the lower A_c is, and the better the CMRR. Thus, for a perfectly symmetrical differential amplifier with A_c = 0, the output voltage is given by,

$$V_{out} = A_d(V_{in}^{+} - V_{in}^{-}) \tag{2.6}$$

2.3.2. Current Mirror

The function of current mirror is to provide a constant current. The constant current is obtained from an output current, which is the reflection or mirror of a constant current developed on one side of the circuit. The circuit requires that the transistor have identical gate-source voltage drops [4].

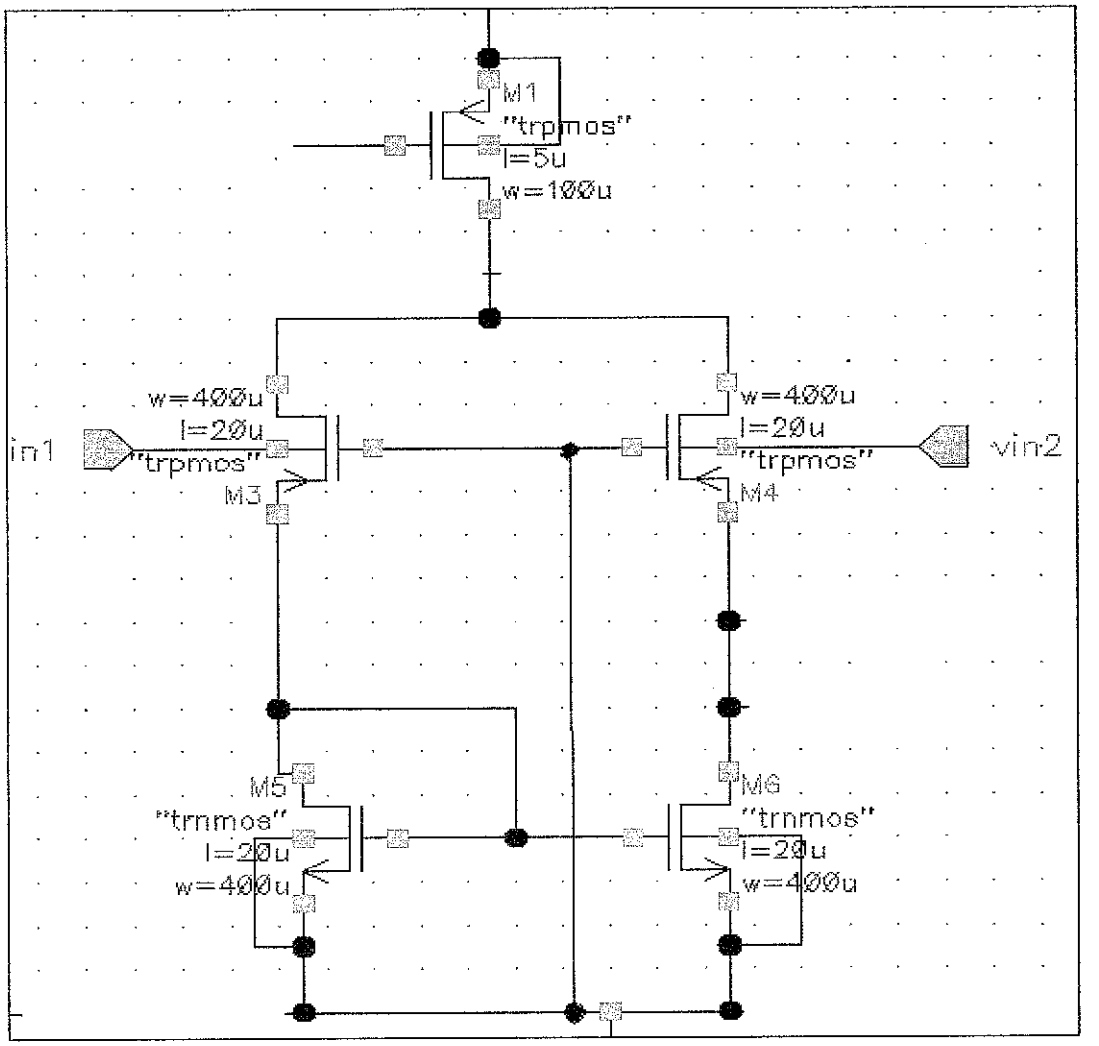

Figure 4: Subcircuit of differential amplifier and current mirror

The structure consisting of M5 and M6 in Figure 4 is a basic current mirror. In general case, the devices need not be identical. The current equation can be written as:

$$I_{m3} = 1/2 * \mu_n C_{ox} (W/L)_5 (V_{gs} - V_{th}) \tag{2.7}$$

$$I_{m4} = 1/2 * \mu_n C_{ox} (W/L)_6 (V_{gs} - V_{th}) \tag{2.8}$$

Obtaining

$$I_{m4} = \left[\left(W/L\right)_6 / \left(W/L\right)_5 \right] * I_{m3} \tag{2.9}$$

The key property of this topology is that it allows precise copying of current with no dependence on process and temperature. The ratio of I_{m4} and I_{m3} is given by the ratio of device dimensions, a quantity that can be controlled with reasonable accuracy.

2.3.3. Class AB Output Stage

Figure 5 shows the structure of class AB amplifier. Class AB amplifier functions like combination of class A and class B amplifier. Class AB used complementary transistor instead of class B which used one transistor only. Each transistor is amplified halves of the signal and recombined later at the output. Such a circuit behaves as a class A amplifier in the region where both devices are in the linear region. However the circuit cannot strictly be called class A if the signal passes outside this region, since beyond that point only one device will remain in its linear region and the transients typical of class B operation will occur.

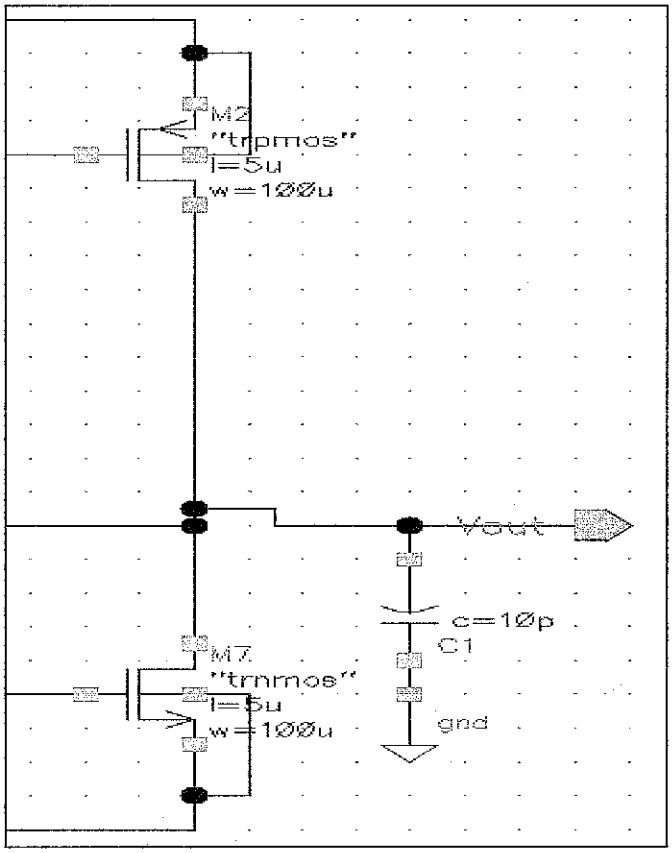

Figure 5: Class AB output stage

2.4. The Design Op Amp

The complete op amp with bulk driven is shown in Figure 6. In this case an n-well CMOS process been chosen, so that the bulk driven is of PMOS type. By applying the input signal to the bulk terminal of the input transistor, the threshold voltage limitations disappear. Other advantage is to minimize the current consumption and input referred noise. The large channel length in input stage results in large output impedance of the input stages which increases the gain but decrease the bandwidth of the op amp [1].

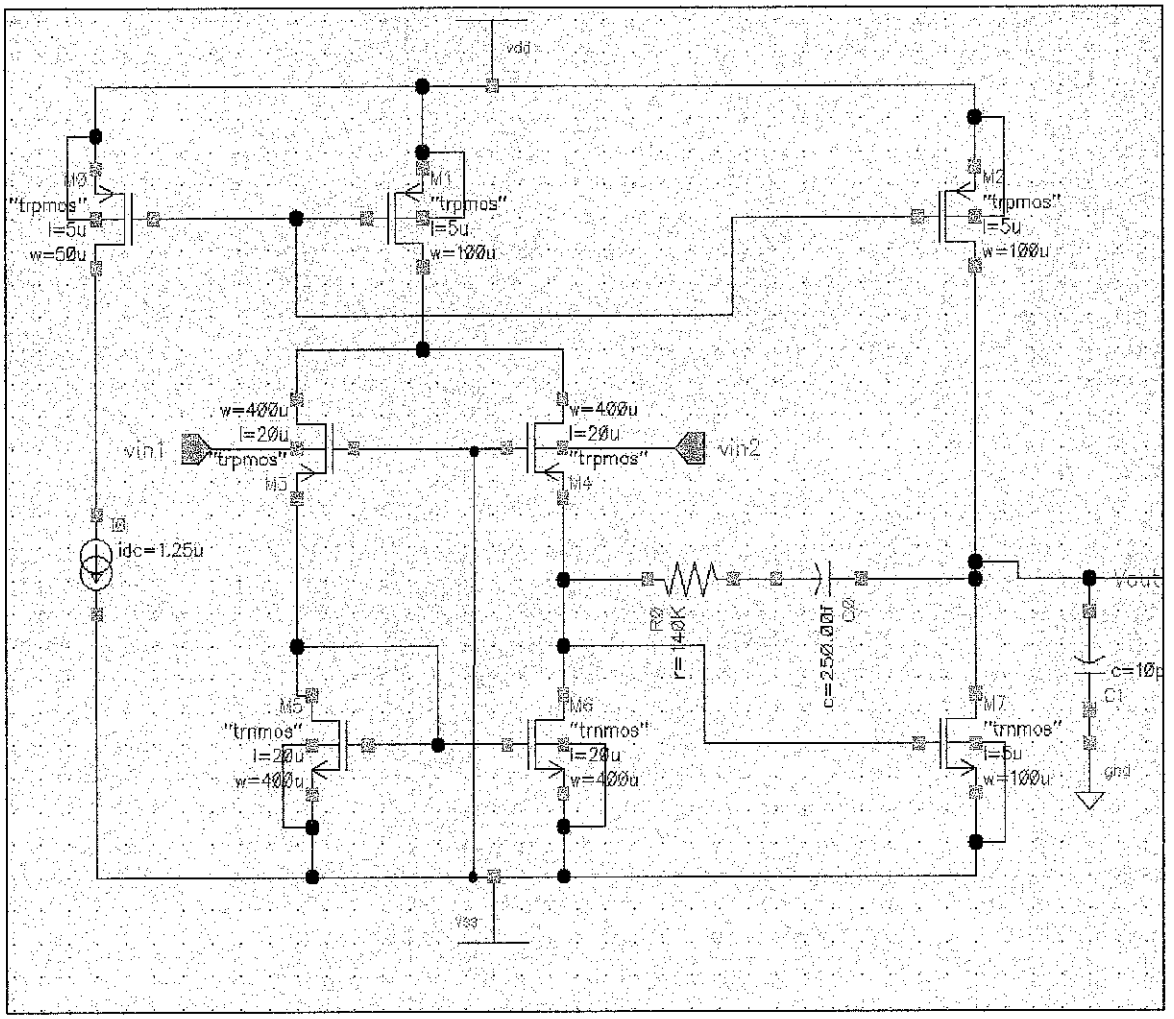

Figure 6: The design op amp

The R-C Miller compensation is used to provide the stability of the op amp. The compensation capacitor is connected between the output of the input stage and the output stages in order to achieve a single low frequency higher than the gain bandwidth product. Resistor is included to transform the right half-plane zero that arises from the feedforward signal path through the compensating capacitor into high frequency left half plane zero [3].

2.5. Layout Design

Integrated circuit layout, also known IC layout or IC mask layout is the representation of an integrated circuit in terms of planar geometric shapes which correspond to the patterns of metal, oxide, or semiconductor layers that make up the components of the integrated circuit [13].

When using a standard process, where the interaction of the many chemical, thermal, and photographic variables are known and carefully controlled, the behavior of the final integrated circuit depends largely on the positions and interconnections of the geometric shapes. A layout engineer's job is to place and connect all the components that make up a chip so that they meet all criteria.

The layout must pass a series of checks in a process known as verification. The two most common checks in the verification process are Design Rule Checking (DRC), and Layout Versus Schematic (LVS). When all verification is complete the data is translated into an industry standard format, typically GDSII, and sent to a semiconductor foundry. The process of sending this data to the foundry is called tapeout due to the fact the data used to be shipped out on a magnetic tape. The foundry converts the data into another format and uses it to generate the photomasks used in a photolithographic process of semiconductor device fabrication [13].

2.6. Design Rule Check (DRC)

The created mask layout must conform to a set of design rules, in order to ensure a lower probability of fabrication defect. This rule is known as Design Rule Check (DRC). DRC is a major step during physical verification of the design, which also involves Layout Versus schematic (LVS). DRC used for this project is provided in the Appendix C.

Design rules are specific to a particular semiconductor manufacturing process. A design rule set specifies certain geometric and connectivity restrictions to ensure sufficient margins to account for variability in semiconductor manufacturing processes, so as to ensure that most of the parts work correctly.

The main objective of design rule checking (DRC) is to achieve a high overall yield and reliability for the design. If design rules are violated the design may not be functional. To meet this goal of improving die yields, DRC has evolved from simple measurement and Boolean checks, to more involved rules that modify existing features, insert new features, and check the entire design for process limitations such as layer density. A completed layout consists not only of the geometric representation of the design, but also data that provide support for manufacture of the design. While design rule checks do not validate that the design will operate correctly, they are constructed to verify that the structure meets the process constraints for a given design type and process technology [10].

2.7. Layout Versus Schematic (LVS)

The Layout Versus Schematic (LVS) determines whether a particular integrated circuit layout corresponds to the original schematic or circuit diagram of the design. A successful DRC ensures that the layout conforms to the rules required for faultless fabrication. However, it does not guarantee if it really represents the circuit you desire to fabricate. This is where an LVS check is used. The LVS netlist is provided in appendix D.

LVS check recognizes the electrical components of the layout, as well as the connections between them, and compares them with the schematic or circuit diagram [14].

LVS Checking involves following three steps:

1. Extraction: The software program takes a database file containing all the layers drawn to represent the circuit during layout. It then runs the database through many logic operations to determine the semiconductor components represented in the drawing by their layers of construction. It then examines the various drawn metal layers and finds how each of these components connects to others.
2. Reduction: During reduction the software generates a netlist representation of the layout database.
3. Comparison: The extracted layout netlist is then compared to the netlist taken from the circuit schematic. If the two netlists match, then the circuit passes the LVS check. At this point it is said to be "LVS clean."

In most cases the layout will not pass LVS the first time requiring the layout engineer to examine the LVS software's reports and make changes to the layout. Typical errors encounters during LVS include:

1. Shorts: Two or more wires that should not be connected together have been and must be separated.
2. Opens: Wires or components that should be connected are left dangling or only partially connected. These must be connected properly to fix this.
3. Component Mismatches: Components of an incorrect type have been used.
4. Missing Components: An expected component has been left out of the layout.
5. Property Errors: A component is the wrong size compared to the schematic.

2.7. Design Specification

The specification of the op amp is defined before the schematic design is performed. The important specification data are provided in Table 2. These values are obtained from the recent trend of op amp nowadays [1], [2], [3], [9] and [15].

Table 1: Specification of CMOS op amp

Electrical parameters	**Expected value**
Supply voltage (V)	1- 1.75
Load capacitance: C_L(pF)	5-10
DC gain: A_o (dB)	≥50
Unity-gain frequency: F_u (MHz)	>1
Phase margin: $\acute{o}_m$ (deg)	65
Slew rate: SR (V/μsec)	+5/-5
Input common range: ICMR (V)	+1/-1

2.7.1. Supply Voltage

While most digital circuit use a single polarity power supply, (e.g., V_{DD} and ground), many analog circuits, especially op amps, are powered by a dual polarity power supply (e.g., V_{DD}, V_{SS} and ground). By convention, V_{DD} is positive relative to ground (e.g., +1V) and V_{SS} is negative relative to ground (e.g., -1V). The use of dual polarity power supplies allows us to center ac signals at ground and build circuits capable of generating signals that swing above and below ground by a few volts [16]. [15] Has design supply voltage till 1.75V and [1], has reported that the supply voltage can go down till 1 V supply voltage. My objective is to design the supply voltage in the range of this two, 1 – 1.75V.

2.7.2. Load Capacitance

In real circuit, op amp's output will drive some other circuit or instrument either on-chip or off-chip. The addition of another circuit will load the op amp with some capacitance and resistance. This can be representing in simulation by adding capacitor and resistor in parallel to the op amp output. For driving the gate of a CMOS transistor (a typical on-chip load), the load is purely capacitive, no need to add the load resistor [15]. From design in [2], and [9], the expected load capacitance is in range of 5 – 10 pF.

2.7.3. DC Gain

The open loop gain of an operational amplifier is the gain obtained when no feedback is used the circuit. Open loop gain is usually exceedingly high; in fact, an ideal operational amplifier has infinite open loop gain. Normally, feedback is applied around the op-amp so that the gain of the overall circuit is defined and kept to a figure which is more usable. Normally people aim to obtain higher than 80 dB. For 1 V supply voltage in [1], the gain is 44.6 dB. My objective is to obtain the gain higher than 50 dB.

2.7.4. Unity Gain Frequency

Unity gain frequency of the amplifier is the frequency at which the gain drops to one, or 0 dB. It indicates the highest usable frequency. It is important because it equals the gainbandwidth product. It is such frequency of operation for a device where the gain of the component drops to unity. The unity gain frequency [1] is 1.3 MHz while in [2] is 5 MHz. For this design, the specification for the unity gain frequency is higher than 1 MHz.

2.7.5. Phase Margin

In electronic amplifiers, phase margin is the difference, measured in degrees, between the phase angle of the amplifier's output signal and -360°. In feedback amplifiers, the phase margin is measured at the frequency at which the gain drops to one, or 0 dB. Based on [1], [2] and [3], the phase margin specifies is 65°.

2.7.6. Slew Rate

The speed of the amplifier is often limited by large-signal effects such as slew rate. Slew rate is the maximum speed at which an op amp can charge or discharge its load for all possible input signals. Based on [2], the predicted slew rate is -5 to +5 V/μsec.

2.7.7. Input Common Mode Range

Ideally, an op amp should work the same regardless of the dc levels of the input voltages. Only the difference in two voltages between the two inputs should affect the output. But, real circuit never behave this well. Input common mode range (ICMR) is the range of input voltage where the circuit has a gain of approximately one. The specification for the ICMR is -1 to +1 V.

CHAPTER 3

METHODOLOGY AND PROJECT WORK

3.1. Procedure

The first step in designing the op amp is to define the specification required for the design. In industry, this specification is defined by the customer. From this specification, the architecture for the op amp will be proposed. Then, the conceptual design will be done by hand calculation. To optimize the design, the schematic then simulate was simulated using cadence software. Once the simulation is done, the layout of the op amp was drawn. After that, the layout design will be resimulated until verification and extraction process are successful. The complete process of op amp IC design is shown in Figure 7.

3.2. Tool Required

The tools that will be used for this project are cadence IC design software for schematic capture and circuit simulation and Mentor Graphic for layout design, layout verification and extraction. The detail for the software used is provided in Table 2.

Table 2: Process Vs the software used

Process	Software
Schematic capture	Virtuoso Schematic Editor
Circuit simulation	Virtuoso Spectre Circuit Simulator
Layout design, Verification and extraction	Mentor Graphic Calibre

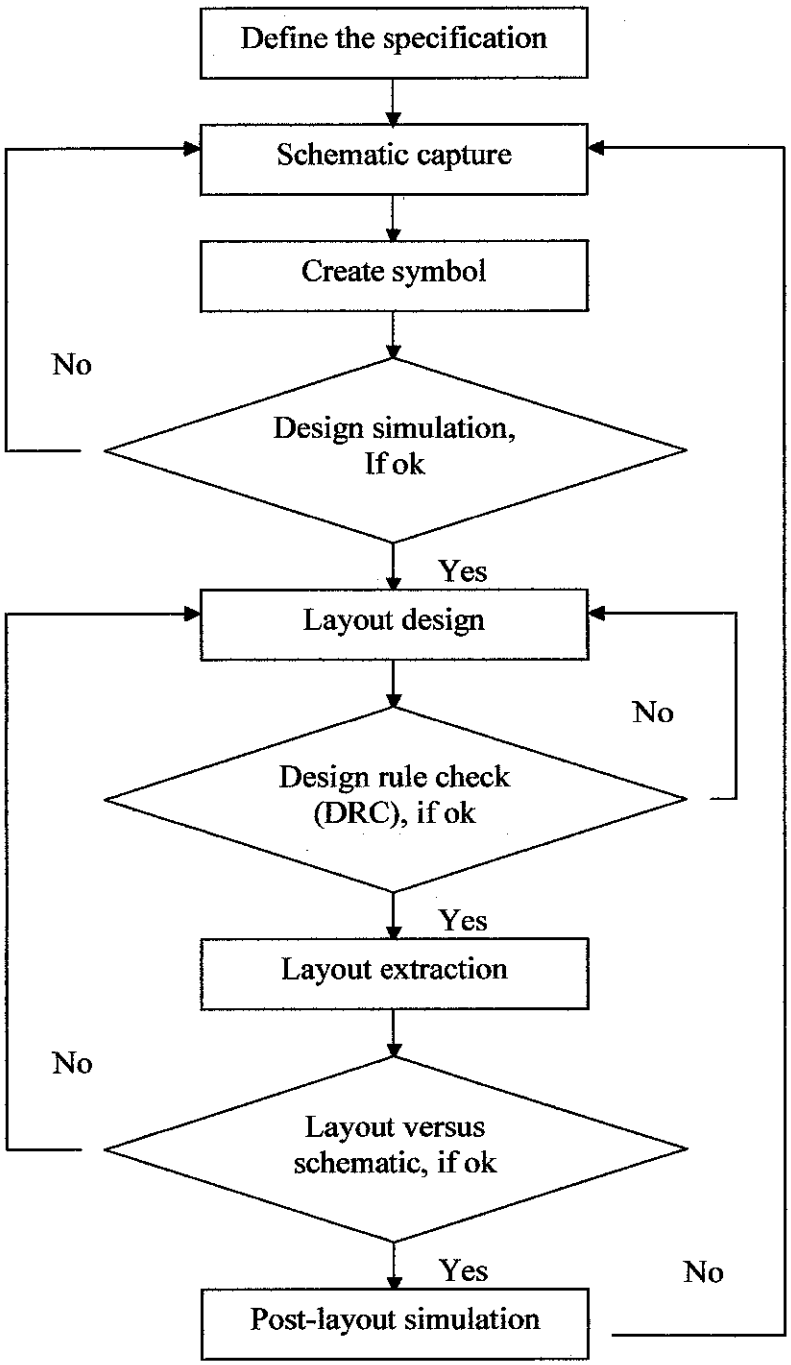

Figure 7: Flowchart of the project

CHAPTER 4

RESULTS AND DISCUSSION

The schematic design has been simulated with Virtuoso Spectre Circuit Simulator software from Cadence while layout have been designed, verified and extracted using the Mentor Graphic Calibre software. The result of simulation have been obtained and shown in Table 3.

4.1. Schematic Result

The results of simulation are listed in table 3. The positive supply voltage, V_{DD} is set to 0.8 V while V_{SS} is set to -0.8 V. The op amp is capable of operating at 1.6 V supply voltage. This value had satisfied the project objective which is operate the op amp with supply voltage in the range of 1 -1.75 V. This has been verified by setting the op amp to function as a basic unity gain buffer. Figure 8 shows the plot for transient response of input and output waveforms. The figure shows that the output waveform follows the input waveform closely.

Table 3: Simulated results of a 1.6 V op amp

Electrical parameters	Value
Supply voltage (V)	1.6
DC gain: A_o (dB)	23
Unity-gain frequency: F_u (MHz)	0.1
Phase margin: $\acute{o}_m$ (deg)	69
Positive slew rate: SR (V/μsec)	0.125
Negative slew rate: SR (V/μsec)	0.15
Input common range: CMR (mV)	-250 to 700
Common mode rejection ration: CMRR (dB)	57.62
Power consumption (μW)	20

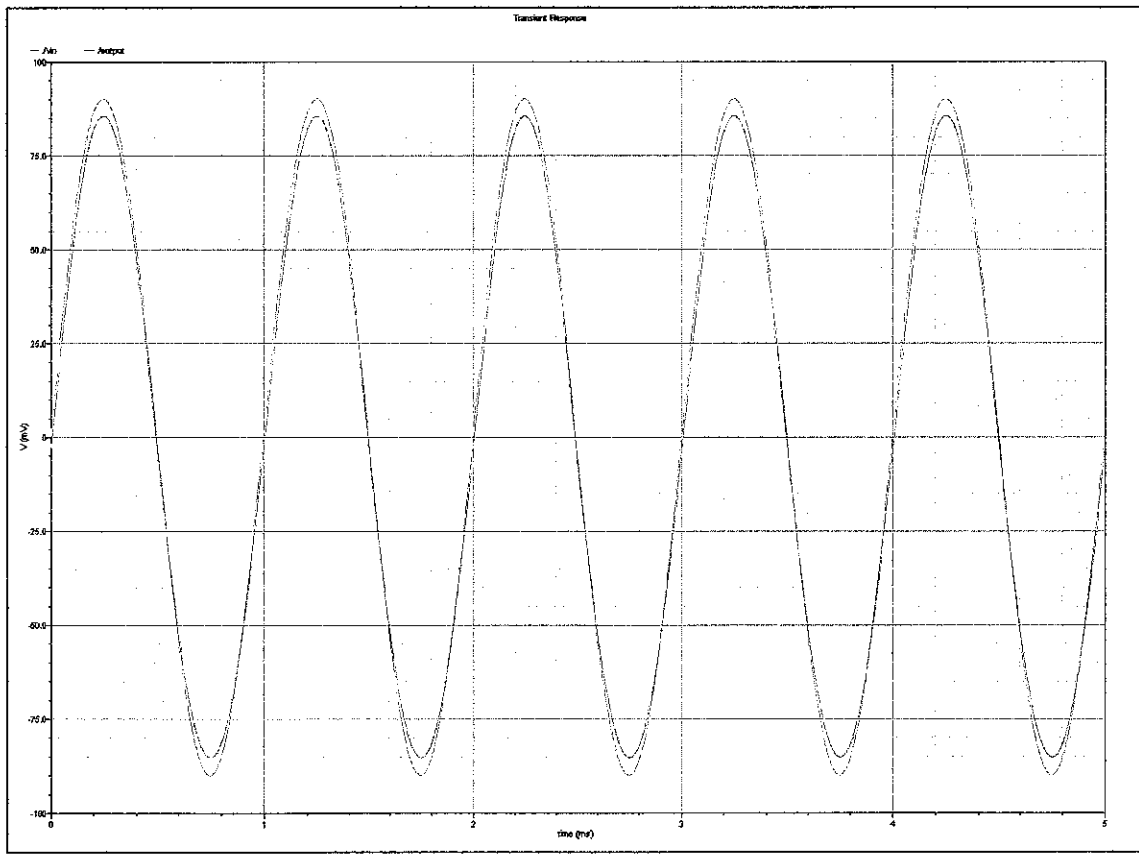

Figure 8: Graph of input and output waveform function as unity gain

Input common mode range (ICMR) was also measured when the op amp function in unity gain mode. ICMR specify over what range of common mode voltage the differential amplifier continues to sense and amplify the difference signal with same gain. Ideally, the op amp should work the same regardless of the DC level of input stages. The ICMR obtained is in range of -250 mV to 700 mV, very much smaller compared to specify value which is -1 V to 1 V range. This value much lower is because of the effect of reduced the power supply. The ICMR is important because it determine if the output of a stage can interface with the input of another different or similar stage. Figure 9 shows the plot output voltage versus input voltage to measure ICMR.

The frequency response of the op amp is shown in Figure 10. The measurement is taken when the op amp is in differential mode with one of the input is grounded. The open loop gain, A_o obtained is 23 dB. This value is small compared to specify value which is 50 dB. Increase the power supply will increase the gain, but this will not satisfied the project objective. Reduce the (W/L) of input stage also will increase the gain but at the expense, other characteristics will be distorted. The unity gain frequency, the frequency at which the gain drop to one or zero dB is 0.1 MHz. The phase margin at 0.1 MHz is 69°. It is important for phase margin to have a value greater than 0° in order to make sure that the amplifier are theoretically stable. It is desirable to have a phase margin of at least 45°, with 60° is preferable in most situation. Therefore, the phase margin obtained is very close to specify value, 65° and preferable value. An amplifier with lower phase margin will ring for longer and an amplifier with more phase margin will take a long time on the initial rise.

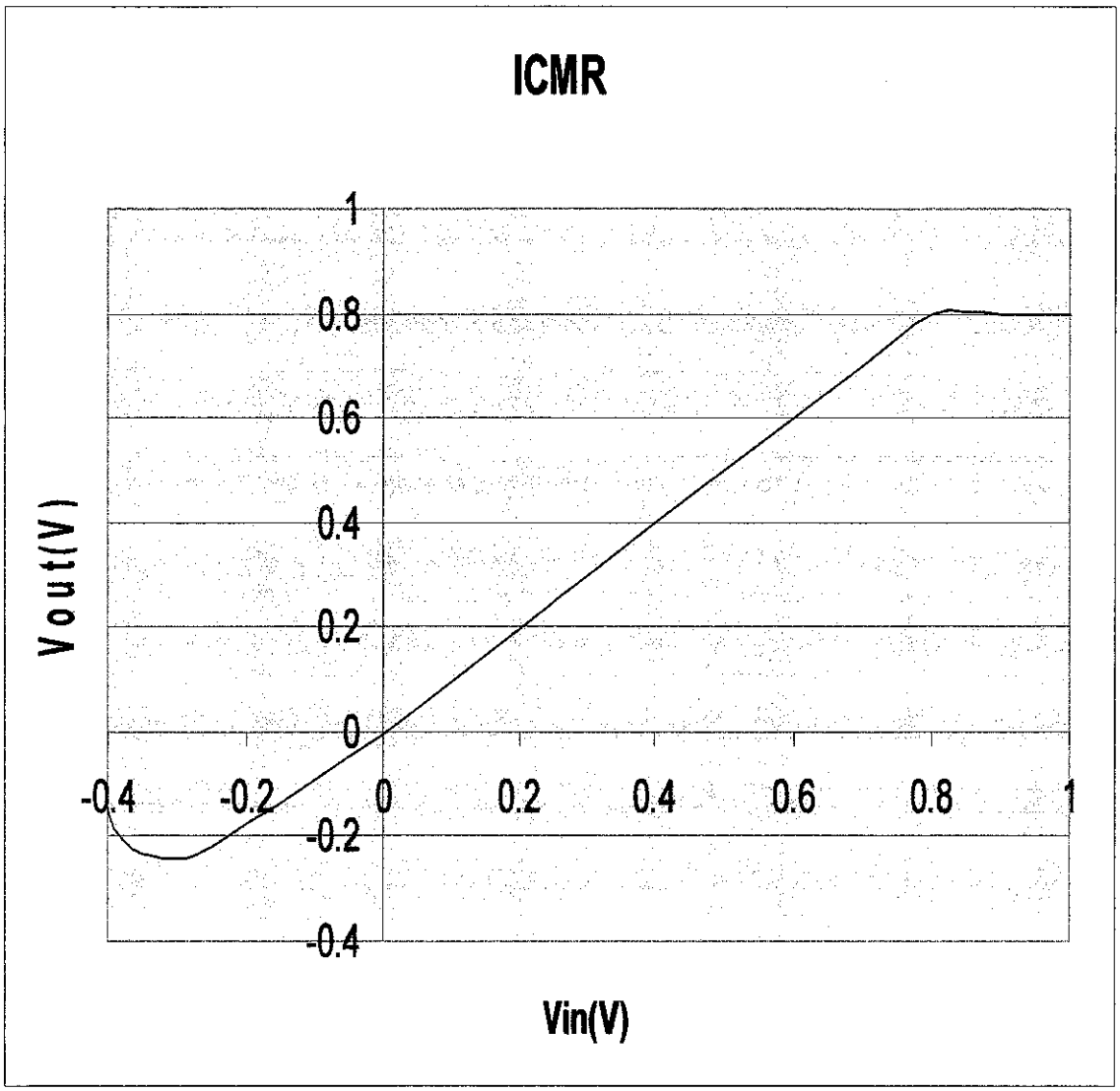

Figure 9: Graph of ICMR

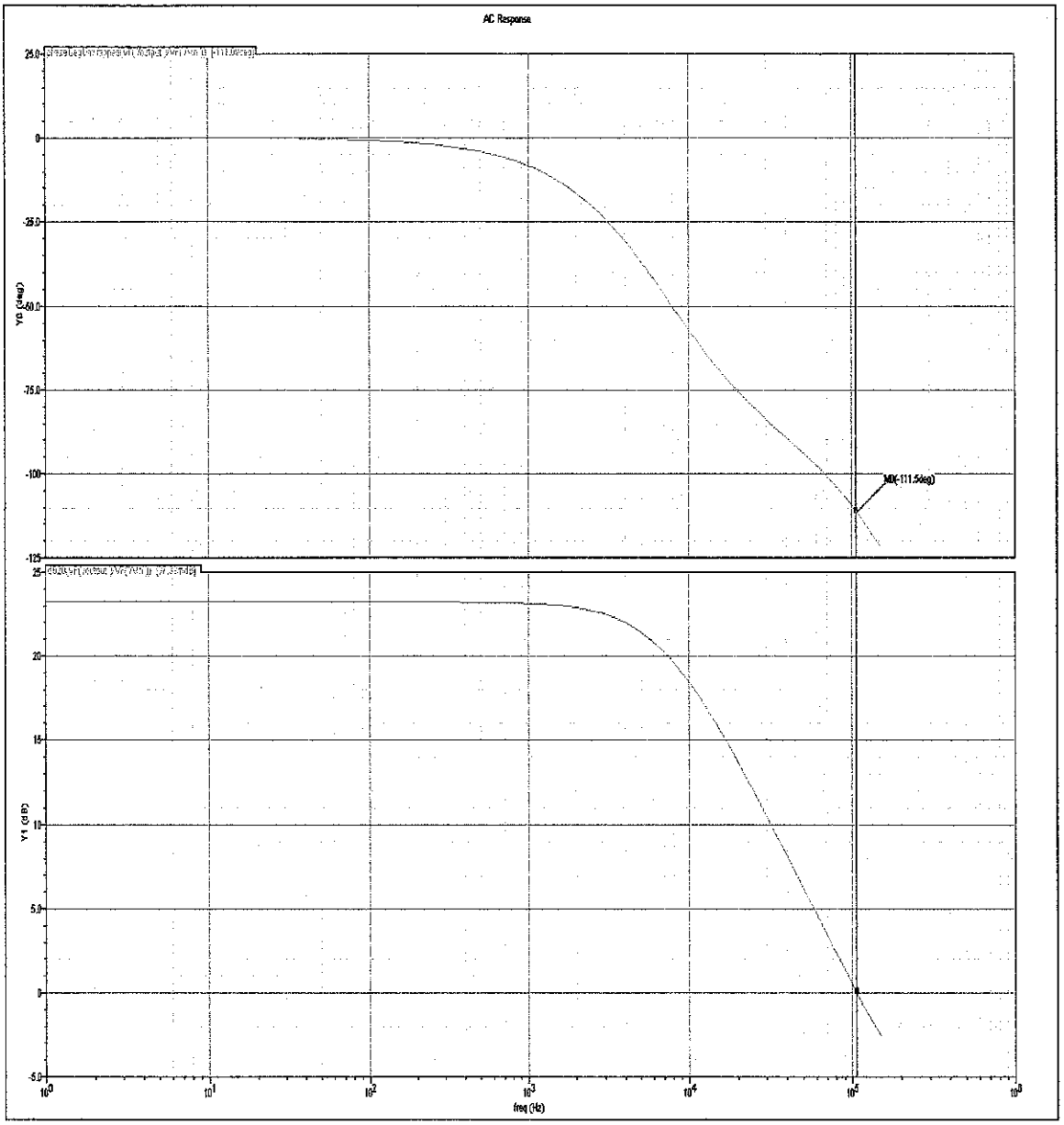

Figure 10: Graph of frequency response

Common mode gain measures how much the output changes in response to a change in the common mode input level. Ideally common mode gain of an op amp is zero. The amplifier should ignore the common mode level and amplify only the differential mode signal. Common mode rejection ratio (CMRR) is defined as the differential mode gain divided by the common mode gain. Common mode gain obtained is -34.3 dB like shown in Figure 11 and differential gain is 23 dB. Subtracting these two values will give CMRR of 57.3 dB. Ideally an amplifier should have an infinite CMRR. Practically, most designer will aim for CMRR > 60 dB. A high CMRR is important in applications where the signal of interest is represented by a small voltage fluctuation superimposed on a (possibly large) voltage offset, or when relevant information is contained in the voltage difference between two signals.

The speed of amplifier often limited by large signal effect such as slew rate. Slew rate is the maximum rate at which the output voltage of an operational amplifier changes for a square-wave or step-signal input. To measure slew rate, the op amp must be configure as unity gain buffer. The slew rate obtain are 0.125 V/μsec for positive slew rate and 0.15 V/μsec for negative slew rate. The graph of slew rate is shown in Figure 12.

The power consumption was measured when op amp was configured as unity gain buffer and both the inputs were set to ground. The total power dissipation is given by the equation:

$$p = |V_{DD} I_{DD}| + |V_{SS} I_{SS}| \tag{4.1}$$

Where;

$$I_{DD} = I_{M0} + I_{M1} + I_{M2} \tag{4.2}$$

$$I_{DD} = 1.25 + 2.514 + 2.524 = 6.288\mu A$$

$$I_{SS} = I_{M0} + I_{M5} + I_{M6} + I_{M7} \tag{4.3}$$

$$I_{SS} = 1.25 + 1.257 + 1.257 + 2.524 = 6.288\mu A$$

So,

$$P = 0.6 * 6.288\mu + 0.6 * 6.288\mu = 20.1215\mu W$$

From the simulation, the current obtained were I_{DD}=I_{SS}=6.288 μA. From the calculation, the power consumption obtained was 20 μW. Most low power op amp work in the weak inversion region in order to reduce the dissipation. It was seen that a low power could be obtained at the expense of frequency response and other desirable characteristics.

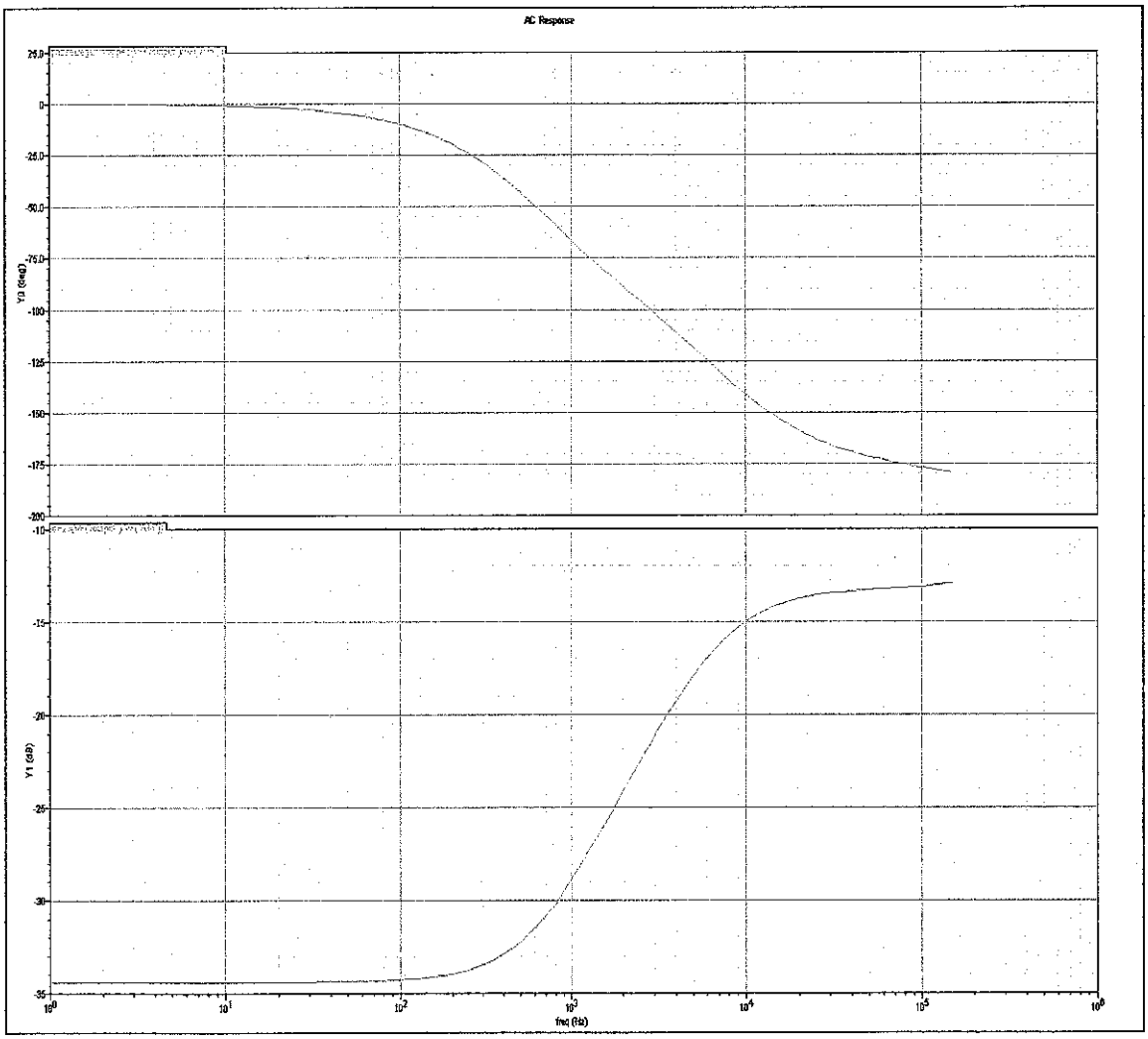

Figure 11: Graph of common mode gain

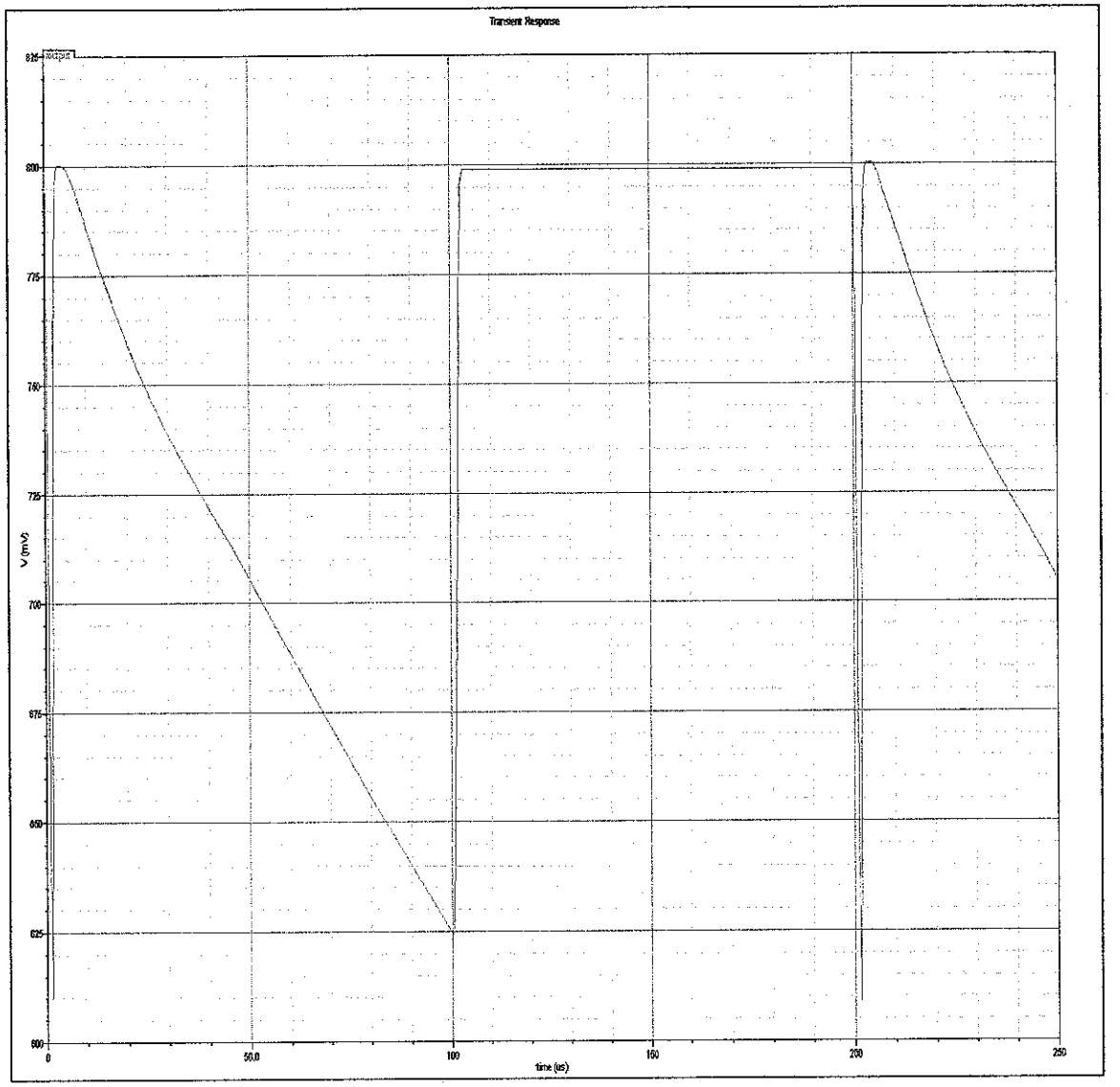

Figure 12: Graph of slew rate

4.2. Layout Design

After developing the schematic of the design, the next step is to create a layout. A layout describes the mask from which the design will be fabricated. The layers in a layout describe the physical characteristics of the device and have more details than a schematic. Therefore, layout verification of the design is critical. The layout design used 0.35μm technology using software Calibre from Mentor Graphic. The design has successfully undergone the DRC and LVS check. Figure 13 shows the complete view of layout design and Figure 14 shows only the transistor view of layout design. The layout after DRC check is shown in Figure 15 while the layout after LVS check is shown in Figure 16.

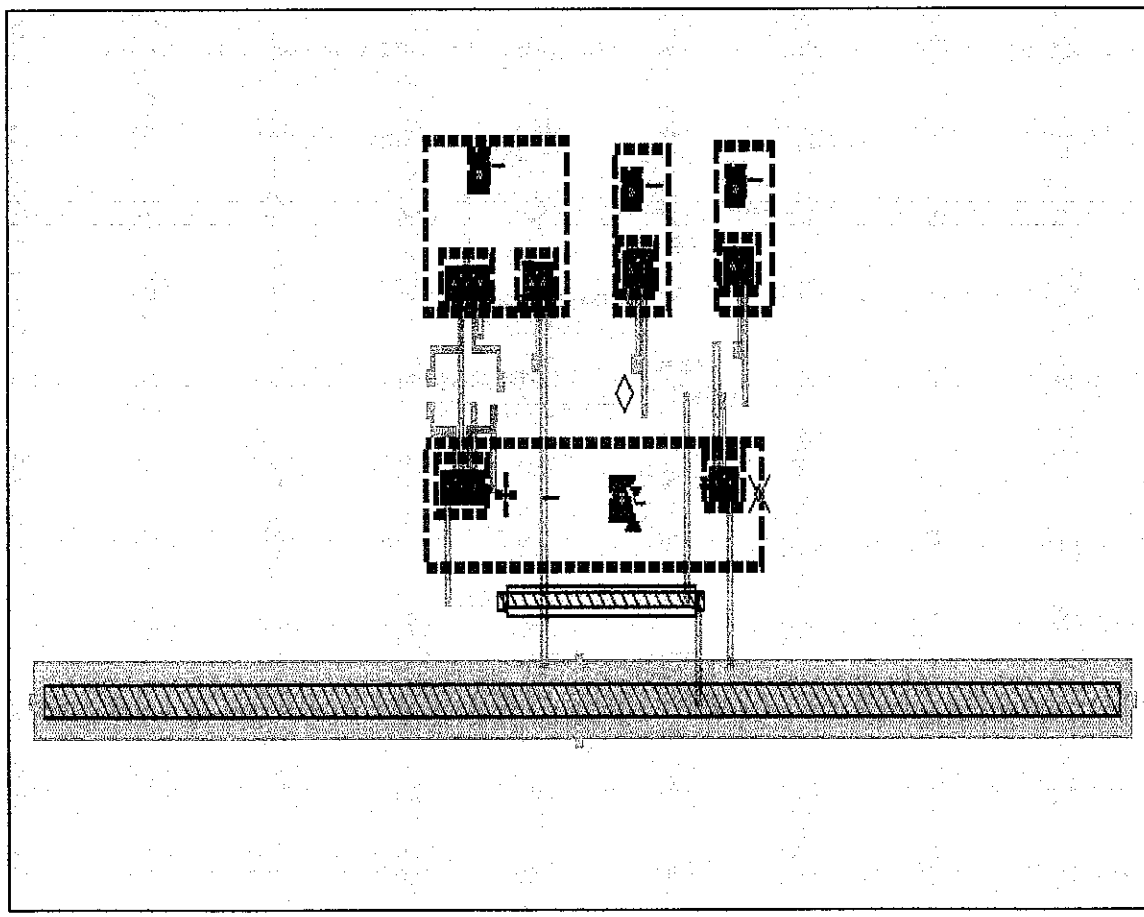

Figure 13: Full layout view

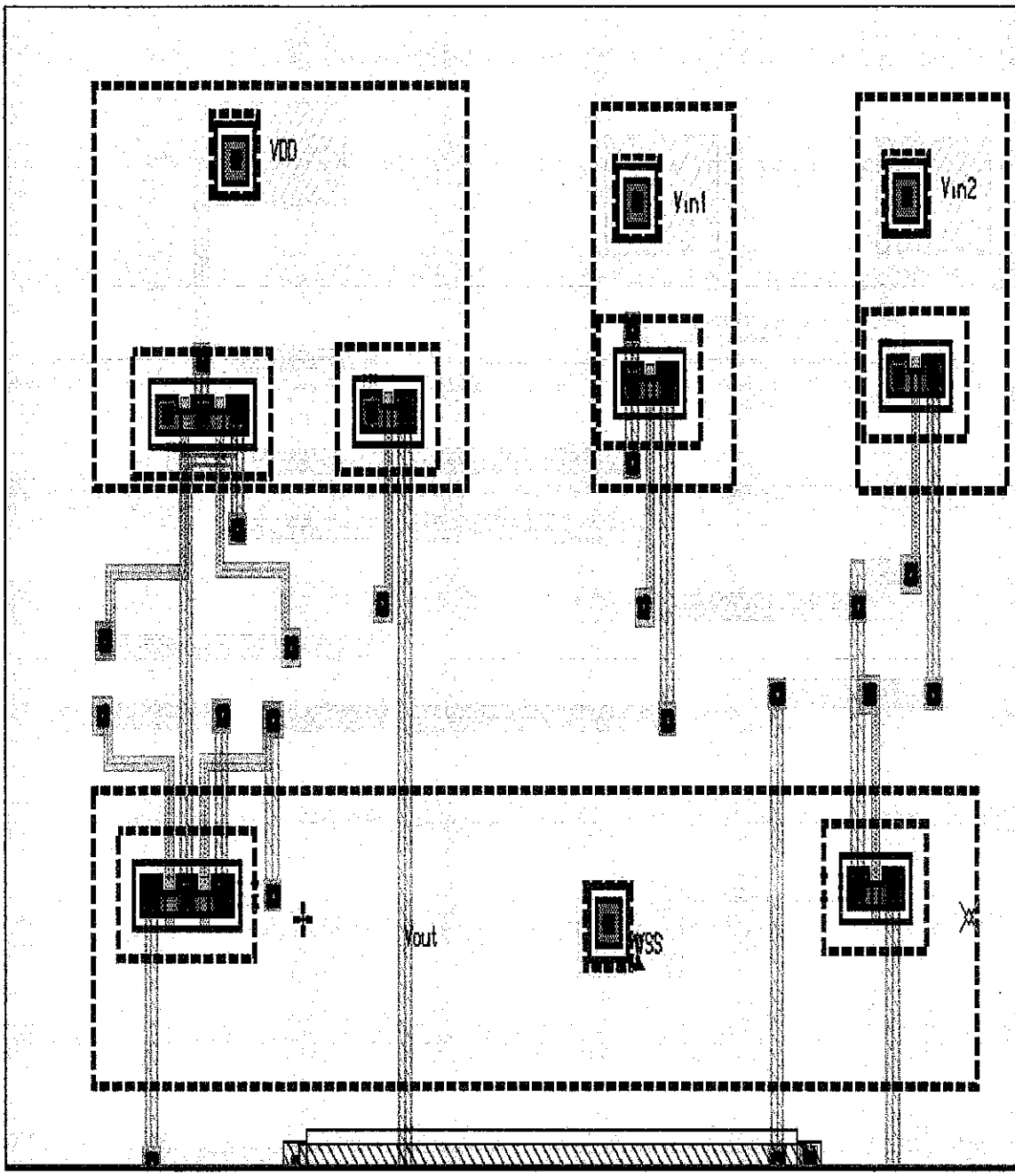

Figure 14: Transistor layout view

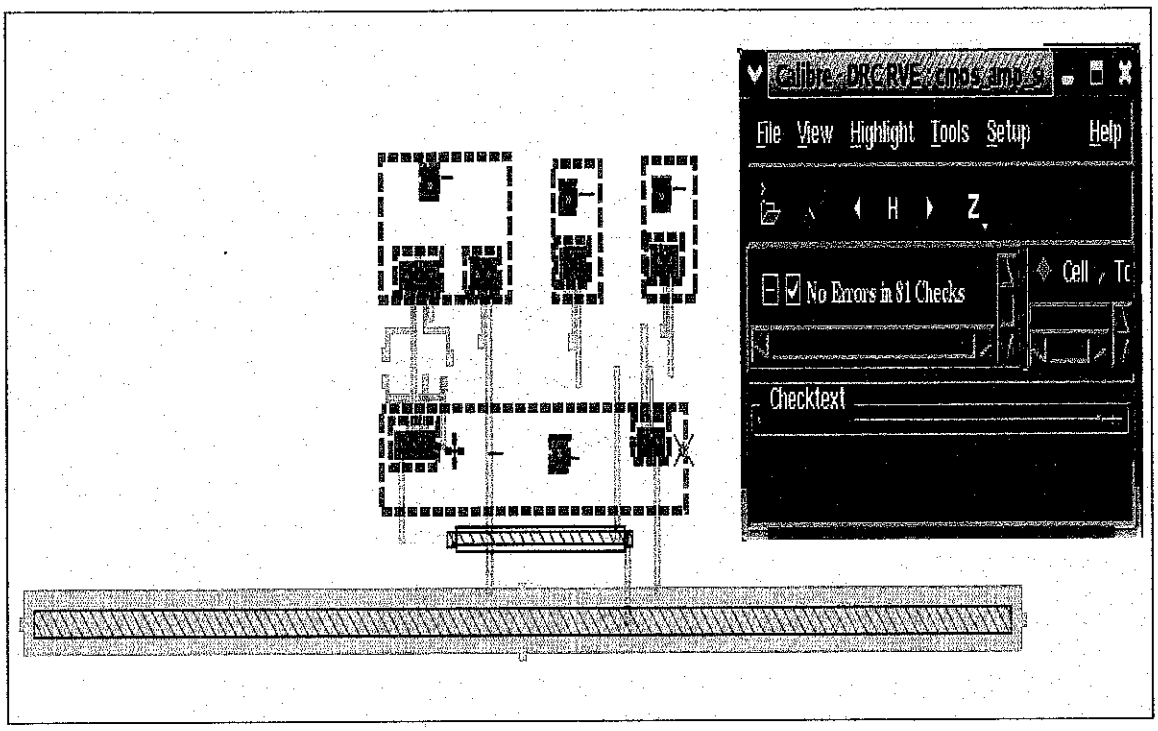

Figure 15: Layout view after DRC check

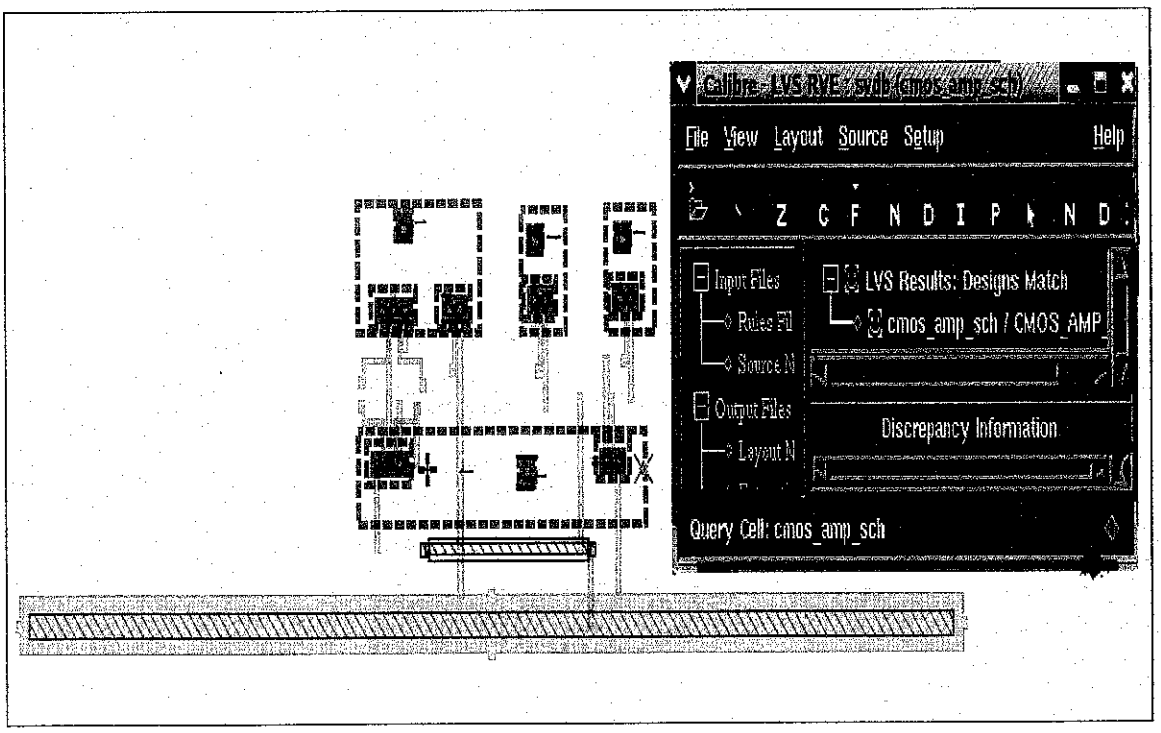

Figure 16: Layout view after LVS check

CHAPTER 5

CONCLUSION AND RECOMMENDATION

5.1. Conclusion

The low voltage and low power CMOS op amp have been successfully designed and simulated. The simulated result shows that this op amp can properly function as low as 1.6 V supply voltage. Power consumed by this design is 20 μW. The use of bulk-driven input transistor make it possible to design low voltage and low power op amp. Both these value have satisfied the project objective which is obtained low supply voltage and low power consumption op amp. The gain of the op amp is 23 dB, unity gain frequency is 0.1 MHz. the phase margin obtained is 69°. The load capacitance used was 10 pF. The layout design for the schematic has been performed using 0.35 μm technology. The layout design has successfully undergone the DRC and LVS check.

5.2. Recommendation

All the result obtained have satisfied the define specification except the open loop which is 23 dB. The open loop gain can be increase by increase the supply voltage. Reduce the (W/L) of the input stage also will increase the gain but at expense, other characteristics will be distorted. Furthermore, this design also can be fabricate in smaller technology to obtain a better result. The next process after this is tape out. If budget and equipment is available, this op amp is ready to be tape out.

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APPENDICES

APPENDIX A

SCHEMATIC NETLIST

```
.subckt CMOS_AMP_SCH

*
* Globals.
*
.global VSS VDD

        R1 N$9 N$214 hr 1.4k
        C1 N$214 VOUT notchedrow 250f
        MN3 VOUT N$9 VSS VSS n L=5u W=100u
        MP5 VOUT N$5 VDD VDD p L=5u W=100u
        MN2 N$9 N$7 VSS VSS n L=20u W=400u
        MN1 N$7 N$7 VSS VSS n L=20u W=400u
        MP4 N$9 VSS N$8 VIN2 p L=20u W=400u
        MP3 N$7 VSS N$8 VIN1 p L=20u W=400u
        MP2 N$8 N$5 VDD VDD p L=5u W=100u
        MP1 VSS N$5 VDD VDD p L=5u W=50u
.ends CMOS_AMP_SCH
```

APPENDIX B

LAYOUT NETLIST

```
* SPICE NETLIST
**************************************

.SUBCKT via
** N=1 EP=0 IP=0 FDC=0
.ENDS
**************************************
.SUBCKT nwell_contact
** N=2 EP=0 IP=0 FDC=0
.ENDS
**************************************
.SUBCKT cmos_amp_sch VDD VSS
** N=25 EP=2 IP=32 FDC=10
M0 VSS 4 2 VSS N L=4e-07 W=6e-07 AD=1.24e-12 AS=1.12e-12 $X=-35000 $Y=1000 $D=1
M1 4 4 VSS VSS N L=4e-07 W=6e-07 AD=1.12e-12 AS=1.24e-12 $X=-26000 $Y=1000 $D=1
M2 6 2 VSS VSS N L=4e-07 W=6e-07 AD=1.12e-12 AS=1.12e-12 $X=147000 $Y=2000 $D=1
M3 VDD 1 7 VDD P L=4e-07 W=6e-07 AD=1.24e-12 AS=1.12e-12 $X=-31000 $Y=66000 $D=0
M4 VSS 1 VDD VDD P L=4e-07 W=6e-07 AD=1.12e-12 AS=1.24e-12 $X=-22000 $Y=66000 $D=0
M5 6 1 VDD VDD P L=4e-07 W=6e-07 AD=1.12e-12 AS=1.12e-12 $X=21300 $Y=66500 $D=0
M6 4 VSS 7 9 P L=4e-07 W=6e-07 AD=1.12e-12 AS=1.12e-12 $X=89300 $Y=70250 $D=0
M7 2 VSS 7 10 P L=4e-07 W=6e-07 AD=1.12e-12 AS=1.12e-12 $X=157300 $Y=71200 $D=0
R8 2 8 1292.86 $X=1000 $Y=-35000 $D=3
C9 6 8 2.50042e-13 $X=-310500 $Y=-69000 $D=2
.ENDS
**************************************
```

APPENDIX C

DESIGN RULE CHECK (DRC) RULE

```
//  ADK v3.0
//
//  MOSIS Scalable CMOS Submicron Design Rules (as of Rev. 7.3 with half lambda rules)
//
// TSMC 0.35 u parameters for double-poly, 4-level metal process: SCN4ME

UNIT LENGTH       u
UNIT CAPACITANCE ff
UNIT RESISTANCE  ohm
UNIT TIME         ns

INCLUDE "$ADK/technology/ic/process/layers_tsmc035"

DRC_0 = EXTENT
BULK = SIZE DRC_0 BY 1.0

PSUB    =   BULK    NOT    NWELL
DIFF    =   ACTIVE  NOT    POLY
PDIFF   =   DIFF    AND    P_PLUS_SELECT
NDIFF   =   DIFF    AND    N_PLUS_SELECT
NWTIE   =   NDIFF   AND    NWELL
PSUBTIE =   PDIFF   AND    PSUB
GATES   =   POLY    AND    ACTIVE
NGATE   =   GATES   AND    N_PLUS_SELECT
PGATE   =   GATES   AND    P_PLUS_SELECT

SGATES  =   SIZE    GATES  BY       2
GPOLY   =   POLY    AND    SGATES
FPOLY   =   POLY    NOT    GPOLY

dfcnt   =   CONTACT_TO_ACTIVE INSIDE DIFFUSED_RESISTOR
dfcnto  =   size dfcnt by 2
dfrs    =   dfr NOT dfcnto
psdt    =   pdiff not poly
nsdt    =   ndiff not poly
PSRCDRN =   psdt not dfrs
NSRCDRN =   nsdt not dfrs

pres    =   POLY and P_PLUS_SELECT
respin  =   POLY and N_PLUS_SELECT

HR      =   ELECTRODE AND HI_RES_IMPLANT
HR_pin  =   ELECTRODE NOT HI_RES_IMPLANT

CAP     =   POLY    AND    ELECTRODE
CAP_pin =   METAL1 AND ELECTRODE

SELECT  = N_PLUS_SELECT OR P_PLUS_SELECT
BOTH_CONTACT = CONTACT_TO_POLY OR CONTACT_TO_ACTIVE
ACT_CONTACT = CONTACT_TO_ACTIVE OR CONTACT
POL_CONTACT = CONTACT_TO_POLY OR CONTACT

CONNECT METAL3 METAL4 BY VIA3
CONNECT METAL2 METAL3 BY VIA2
CONNECT METAL1 METAL2 BY VIA
CONNECT METAL1 POLY BY CONTACT_TO_POLY
CONNECT METAL1 POLY BY CONTACT

CONNECT METAL4 METAL4.PORT
CONNECT METAL3 METAL3.PORT
CONNECT METAL2 METAL2.PORT
CONNECT METAL1 METAL1.PORT
CONNECT POLY
```

```
CONNECT METAL1 HR_pin by CONTACT_TO_ELECTRODE
CONNECT METAL1 CAP_pin by CONTACT_TO_ELECTRODE
CONNECT METAL1 pres by CONTACT_TO_POLY
CONNECT METAL1 respin by CONTACT_TO_POLY

CONNECT METAL1 ACTIVE by CONTACT_TO_ACTIVE          DIRECT
CONNECT METAL1 N_WELL P_WELL by CONTACT_TO_ACTIVE   DIRECT
CONNECT METAL1 ACTIVE by CONTACT                    DIRECT
CONNECT METAL1 N_WELL P_WELL by CONTACT                     DIRECT


//
// Mask ICtrace Rules
//
CONNECT METAL1 NSRCDRN PSRCDRN BY CONTACT_TO_ACTIVE         mask
CONNECT METAL1 NSRCDRN PSRCDRN BY CONTACT                   mask
CONNECT PSRCDRN PSUB                                        mask
CONNECT NSRCDRN NWELL                                       mask
CONNECT N_PLUS_SELECT                                       mask
CONNECT P_PLUS_SELECT                                       mask
CONNECT NPLUS                                               mask
CONNECT PPLUS                                               mask

VIRTUAL CONNECT NAME VSS
VIRTUAL CONNECT NAME Ring_VSS
VIRTUAL CONNECT NAME VDD
VIRTUAL CONNECT NAME Ring_VDD
VIRTUAL CONNECT NAME GND
VIRTUAL CONNECT NAME ground


//
// Technology specific information.
//


//
// ICtrace Device Definitions
//


DEVICE MP PGATE POLY(G) PSRCDRN(S) PSRCDRN(D) NWELL(B) (S D) NETLIST MODEL p
[
  prop w, l, AS, AD
  w = ( perim_co(pgate,s) + perim_co(pgate,d) ) * 0.1 // factor is .5 * lambda
  l = ( perim(pgate) -  perim_co(pgate,s) - perim_in(pgate,s) - perim_co(pgate,d) -
perim_in(pgate,d) ) * 0.1
  AS = area(S) * 0.04
  AD = area(D) * 0.04
]

DEVICE MN NGATE POLY(G) NSRCDRN(S) NSRCDRN(D) PSUB(B) (S D) NETLIST MODEL n
[
   prop w, l, AS, AD
   w = ( perim_co(ngate,s) + perim_co(ngate,d) ) * 0.1 // factor is .5 * lambda
   l = ( perim(ngate) -  perim_co(ngate,s) - perim_in(ngate,s) - perim_co(ngate,d) -
perim_in(ngate,d) ) * 0.1
  AS = area(S) * 0.04
  AD = area(D) * 0.04
]

DEVICE C CAP POLY CAP_pin (POS NEG) [0.03456 0]

//DEVICE R pres respin respin [7.9]

DEVICE R HR HR_pin HR_pin [50.9]

//
// ICextract Rule Definitions
//
```

```
capacitance order     POLY METAL1 METAL2 METAL3 METAL4 direct mask

capacitance intrinsic METAL4 [0.0004 0.0026]
capacitance intrinsic METAL3 [0.0003 0.0100]
capacitance intrinsic METAL2 [0.0006 0.0060]
capacitance intrinsic METAL1 [0.0011 0.0090]
capacitance intrinsic POLY   [0.0044 0]

capacitance crossover METAL4 METAL3  [0.0032 0.0096 0]
capacitance crossover METAL4 METAL2  [0.0013 0.0068 0]
capacitance crossover METAL4 METAL1  [0.0007 0.0052 0]
capacitance crossover METAL4 POLY    [0.0005 0.0046 0]
capacitance crossover METAL3 METAL2  [0.0032 0.0106 0]
capacitance crossover METAL3 METAL1  [0.0012 0.0070 0]
capacitance crossover METAL3 POLY    [0.0008 0.0056 0]
capacitance crossover METAL2 METAL1  [0.0030 0.0100 0]
capacitance crossover METAL2 POLY    [0.0014 0.0074 0]
capacitance crossover METAL1 POLY    [0.0043 0.0124 0]

resistance  sheet      METAL4  [0.04 0]
resistance  sheet      METAL3  [0.07 0]
resistance  sheet      METAL2  [0.07 0]
resistance  sheet      METAL1  [0.07 0]
resistance  sheet      POLY    [8.9 0]
resistance  sheet      HR_pin  [50.9 0]                              mask
resistance  sheet      PSRCDRN [144.2 0]                          mask
resistance  sheet      NSRCDRN [81.1 0]                           mask

resistance connection METAL1 POLY    [6.9 0]
resistance connection METAL1 METAL2  [1.26 0]
resistance connection METAL2 METAL3  [1.39 0]
resistance connection METAL3 METAL4  [1.26 0]
resistance connection METAL1 PSRCDRN [120.0 0]                  mask
resistance connection METAL1 NSRCDRN [61.4 0]                   mask
resistance connection METAL1 HR_pin  [33.7 0]                      mask

//
// END OF TECHNOLOGY SPECIFIC INFORMATION

//
// ICrules Rule Definitions
//
subcont = EXT CONTACT_TO_ACTIVE (active) < 2 ABUT == 0 OVERLAP OPPOSITE
wellcont = EXT CONTACT_TO_ACTIVE (active) < 2 ABUT == 0 OVERLAP OPPOSITE

bad_active_area { @ Active area must be covered by a select
              x = active NOT P_PLUS_SELECT
              x NOT N_PLUS_SELECT
}
bad_contact_poly { @ Contact to poly must consist of poly, CONTACT_TO_POLY, and METAL1
                   CONTACT_TO_POLY NOT INSIDE poly
                   CONTACT_TO_POLY NOT INSIDE METAL1
}
bad_contact_ELECTRODE { @ Contact to ELECTRODE must consist of ELECTRODE,
CONTACT_TO_ELECTRODE, and METAL1
                   CONTACT_TO_ELECTRODE NOT INSIDE ELECTRODE
                   CONTACT_TO_ELECTRODE NOT INSIDE METAL1
}
bad_contact_active { @ Contact to active must consist of active, CONTACT_TO_ACTIVE, and
METAL1
                   CONTACT_TO_ACTIVE NOT INSIDE active
                   CONTACT_TO_ACTIVE NOT INSIDE METAL1
}
bad_contact_gate { @ Contact to poly may not be on gate region.
                   CONTACT_TO_POLY AND active
}
bad_via {@ Via must consist of METAL1, via, and METAL2
         via NOT INSIDE METAL1
         via NOT INSIDE METAL2
}
bad_via2 {@ Via2 must consist of METAL2, via2, and METAL3
```

```
        via2 NOT INSIDE METAL2
        via2 NOT INSIDE METAL3
}
bad_via3 {@ Via3 must consist of METAL3, via3, and METAL4
        via3 NOT INSIDE METAL3
        via3 NOT INSIDE METAL4
}

select_overlap { @ Overlap of N+ and P+ not allowed
        AND P_PLUS_SELECT N_PLUS_SELECT
}
bad_nwell { @ Nwell must have well contact
       x = ACT_CONTACT AND nwtie
       nwell NOT ENCLOSE x
}
bad_psubstrate { @ Psubstrate must have a substrate contact
       x = ACT_CONTACT AND psubtie
       psub NOT ENCLOSE x
}
bad_pgate { @ P-type gate must not be in psubstrate
        pgate AND psub
}
bad_ngate { @ N-type gate must not be in nwell
        ngate AND nwell
}
bad_port { @ Port must be completely covered with Metal
       METAL1.PORT NOT INSIDE METAL1
       METAL2.PORT NOT INSIDE METAL2
       METAL3.PORT NOT INSIDE METAL3
}
DRC1_1 { @ N-Well width = 12L
        INT nwell < 12 SQUARE REGION SINGULAR
}
DRC1_2 { @ N-well spacing (different potential) = 18L
        EXT nwell < 18 NOT CONNECTED SQUARE REGION SINGULAR
}

DRC2_1 { @ Active area width = 3L
        INT active < 3 SQUARE REGION
}
DRC2_2 { @ Active area spacing = 3L
        EXT active < 3 SQUARE REGION
}
DRC2_3 { @ Source/Drain Active to Well Edge = 6L
        EXT nwell ndiff < 6 SQUARE REGION SINGULAR
        ENC pdiff nwell < 6 ABUT == 0 OVERLAP SQUARE REGION SINGULAR
}
DRC2_4 { @ Substrate/Well Contact, Active to Well Edge = 3L
        ENC ndiff nwell < 3 ABUT == 0 OVERLAP REGION SINGULAR
        EXT nwell pdiff < 3 REGION SINGULAR
}
DRC3_1 { @ Poly width = 2L
        INT poly < 2 SINGULAR
}
DRC3_2 { @ Poly spacing = 3L
        EXT poly < 3 SINGULAR
}
DRC3_3 { @ Gate poly overlap of active = 2L
        pgate TOUCH psrcdrn == 1
        ngate TOUCH nsrcdrn == 1
        ENC active poly < 2 ABUT == 0 SQUARE REGION
}
DRC3_4 { @ Active overlap of gate poly = 3L
        ENC poly active < 3 ABUT == 0 SQUARE REGION
}
DRC3_5 { @ Field poly to active = 1L
        EXT poly active < 1 SQUARE REGION ABUT == 0
}
DRC4.1p {
       nxtor = NSRCDRN OR GATES
       ENCLOSURE GATES nxtor < 3
```

```
        }                                       // nselect overlap of gate
DRC4.1n {
        pxtor = PSRCDRN OR GATES
        ENCLOSURE GATES pxtor < 3
        }                                       // pselect overlap of gate
DRC4.2  {
         ENCLOSURE ACTIVE SELECT < 2 ABUT == 0 OVERLAP SINGULAR
         } // select overlap of active
           // use of both selects implies space
DRC4.3p {
        ENCLOSURE CONTACT_TO_ACTIVE P_PLUS_SELECT < 1 ABUT == 0 OVERLAP SINGULAR
        } // pselect overlap of actcont
DRC4.3n {
        ENCLOSURE CONTACT_TO_ACTIVE N_PLUS_SELECT < 1 ABUT == 0 OVERLAP SINGULAR
        } // nselect overlap of actcont
DRC4.4pw { INTERNAL P_PLUS_SELECT < 2 }             // width
DRC4.4ps {
        EXTERNAL P_PLUS_SELECT < 2 NOT CONNECTED
        }               // space
DRC4.4nw { INTERNAL N_PLUS_SELECT < 2 }             // width
DRC4.4ns {
        EXTERNAL N_PLUS_SELECT < 2 NOT CONNECTED
        }               // space
DRC4.4np { AND N_PLUS_SELECT P_PLUS_SELECT } // p and n selects overlap


DRC5_1 { @ Contact to poly size exactly 2L X 2L
          NOT RECTANGLE CONTACT_TO_POLY == 2 BY == 2
}
//
// This rule is violated in MOSIS pads.  This rule set utilizes the half
// lambda grid rules. Therefore, to ignore the violation, a new layer
// (PADS) has been introduced to ignore this violation if present.
//
DRC5_2 { @ Poly overlap for contact = 1.5L
          x = CONTACT_TO_POLY NOT PADS
          ENC x poly < 1.5 ABUT == 0 SQUARE REGION OVERLAP
}
DRC5_3 { @ Contact to poly spacing = 3L
          EXT CONTACT_TO_POLY < 3 SINGULAR SQUARE
}
DRC5_4 { @ Contact to active space to gate of transistor = 2L
          EXT CONTACT_TO_POLY gates < 2 ABUT == 0  REGION SINGULAR
}
DRC6_1 { @ Contact to active exactly 2L X 2L
          NOT RECTANGLE CONTACT_TO_ACTIVE == 2 BY == 2
}
//
// This rule is violated in MOSIS pads.  This rule set utilizes the half
// lambda grid rules. Therefore, to ignore the violation, a new layer
// (PADS) has been introduced to ignore this violation if present.
//
DRC6_2 { @ Active overlap for contact = 1.5L
          x = CONTACT_TO_ACTIVE NOT PADS
          ENC x active < 1.5 ABUT == 0 OVERLAP REGION
}
DRC6_3 { @ Contact to active spacing = 3L
          EXT CONTACT_TO_ACTIVE < 3 SINGULAR SQUARE REGION
}
DRC6_4 { @ Contact to active space to gate of transistor = 2L
          EXT CONTACT_TO_ACTIVE gates < 2 ABUT == 0 SQUARE REGION SINGULAR
}
DRC7_1 { @ Metal1 width = 3L
         INT METAL1 < 3 SINGULAR
}
DRC7_2 { @ Metal1 spacing = 3L
         EXT METAL1 < 3 SINGULAR
}
DRC7_3 { @ Metal1 overlap of contact to poly or contact to active = 1L
         ENC BOTH_CONTACT METAL1 < 1 ABUT == 0 SQUARE REGION
}
```

```
DRC7_4 { @ Metal1 spacing = 6L if width > 10L
         widem = METAL1 WITH WIDTH > 10
         thinm = METAL1 WITH WIDTH <= 10
         EXT widem < 6 SINGULAR
         EXT widem thinm < 6 SINGULAR
}
DRC8_1 { @ Via size exactly 2L X 2L
         x = NOT RECTANGLE via == 2 BY == 2
         x OUTSIDE overglass
}
DRC8_2 { @ Via spacing = 3L
         EXT via < 3 SINGULAR SQUARE REGION
}
DRC8_3 { @ Via overlap by METAL1 = 1L
         ENC via METAL1 < 1 ABUT == 0 SQUARE REGION
}
DRC9_1 { @ Metal2 width = 3L
         INT METAL2 < 3 SINGULAR
}
DRC9_2 { @ Metal2 spacing = 3L
         EXT METAL2 < 3 SINGULAR
}
DRC9_3 { @ Metal2 overlap of via = 1L
         ENC via METAL2 < 1 ABUT == 0 SQUARE REGION
}
DRC9_4 { @ Metal2 spacing = 6L if width > 10L
         widem = METAL2 WITH WIDTH > 10
         thinm = METAL2 WITH WIDTH <= 10
         EXT widem < 6 SINGULAR
         EXT widem thinm < 6 SINGULAR
}
DRC11_1 { @ ELECTRODE width = 7L ON CAP
          INT CAP < 7 SQUARE REGION SINGULAR
}
DRC11_2 { @ ELECTRODE spacing = 3L ON CAP
          EXT CAP < 3 SQUARE REGION SINGULAR
}
DRC11_3 { @ Poly overlap of ELECTRODE = 5L
          ENC CAP poly < 5 ABUT == 0 SQUARE REGION OVERLAP
}
DRC11_4 { @ ELECTRODE spacing to active or well = 2L
          EXT ELECTRODE active < 2 SQUARE REGION SINGULAR
          EXT ELECTRODE nwell < 2 SQUARE REGION SINGULAR
}
DRC11_5 { @ ELECTRODE spacing to Contact to Poly = 6L
          EXT CAP CONTACT_TO_POLY < 6 SQUARE REGION SINGULAR
}
DRC11_sel { @ Capacitor and Select may not intersect
            x = poly TOUCH cap
            y = ELECTRODE TOUCH cap
            z = x OR y
            z AND N_PLUS_SELECT
            z AND P_PLUS_SELECT
}
DRC12_1 { @ ELECTRODE width = 2L
          x = ELECTRODE NOT cap
          EXT x < 2 SQUARE REGION SINGULAR
}
DRC12_2 { @ ELECTRODE spacing = 3L
          EXT ELECTRODE < 3 SQUARE REGION SINGULAR
}
DRC13_1 { @ Contact to ELECTRODE size exactly 2L X 2L
          NOT RECTANGLE CONTACT_TO_ELECTRODE == 2 BY == 2
}
DRC13_2 { @ Contact to ELECTRODE spacing = 3L
          EXT CONTACT_TO_ELECTRODE < 3 SQUARE SINGULAR
}
DRC13_3 { @ ELECTRODE overlap for contact = 3L ON CAP PLATE
          x = cap AND CONTACT_TO_ELECTRODE
          ENC x ELECTRODE < 3 ABUT == 0 SQUARE REGION OVERLAP
}
```

```
DRC13_4 { @ ELECTRODE overlap for contact = 2L NOT ON CAP PLATE
          x = CONTACT_TO_ELECTRODE NOT cap
          ENC x ELECTRODE < 2 ABUT == 0 SQUARE REGION OVERLAP
}
DRC13_5 { @ Contact to ELECTRODE space to Poly or Active = 3L
          EXT CONTACT_TO_ELECTRODE poly < 3 SQUARE REGION SINGULAR
          EXT CONTACT_TO_ELECTRODE active < 3 SQUARE REGION SINGULAR
}

DRC14_1 { @ Via2 size exactly 2L X 2L
         x = NOT RECTANGLE via2 == 2 BY == 2
         x OUTSIDE overglass
}
DRC14_2 { @ Via2 spacing = 3L
         EXT via2 < 3 SINGULAR SQUARE REGION
}
DRC14_3 { @ Via2 overlap by METAL2 = 1L
         ENC via2 METAL2 < 1 ABUT == 0 SQUARE REGION
}
DRC15_1 { @ Metal3 width = 3L
         INT metal3 < 3 SINGULAR
}
DRC15_2 { @ Metal3 spacing = 3L
         EXT metal3 < 3 SINGULAR
}
DRC15_3 { @ Metal3 overlap of via2 = 1L
         ENC via2 metal3 < 1 ABUT == 0 SQUARE REGION
}
DRC15_4 { @ Metal3 spacing = 6L if width > 10L
         widem = METAL3 WITH WIDTH > 10
         thinm = METAL3 WITH WIDTH <= 10
         EXT widem < 6 SINGULAR
         EXT widem thinm < 6 SINGULAR
}
DRC21_1 { @ Via3 size exactly 2L X 2L
         x = NOT RECTANGLE via3 == 2 BY == 2
         x OUTSIDE overglass
}
DRC21_2 { @ Via3 spacing = 3L
         EXT via3 < 3 SINGULAR SQUARE REGION
}
DRC21_3 { @ Via3 overlap by METAL3 = 1L
         ENC via3 METAL3 < 1 ABUT == 0 SQUARE REGION
}
DRC22_1 { @ Metal4 width = 6L
         INT metal4 < 6 SINGULAR
}
DRC22_2 { @ Metal4 spacing = 6L
         EXT metal4 < 6 SINGULAR
}
DRC22_3 { @ Metal4 overlap of via3 = 2L
         ENC via3 metal4 < 2 ABUT == 0 SQUARE REGION
}
DRC22_4 { @ Metal4 spacing = 12L if width > 10L
         widem = METAL4 WITH WIDTH > 10
         thinm = METAL4 WITH WIDTH <= 10
         EXT widem < 12 SINGULAR
         EXT widem thinm < 12 SINGULAR
}


//
// Miscellaneous
//

TEXT LAYER METAL1.PORT
TEXT LAYER METAL2.PORT
TEXT LAYER METAL3.PORT
TEXT LAYER METAL4.PORT

ATTACH METAL1.PORT METAL1     mask
```

```
ATTACH METAL2.PORT METAL2      mask
ATTACH METAL3.PORT METAL3      mask
ATTACH METAL4.PORT METAL4      mask

PORT LAYER TEXT METAL1.PORT
PORT LAYER TEXT METAL2.PORT
PORT LAYER TEXT METAL3.PORT
PORT LAYER TEXT METAL4.PORT


LVS FILTER sch_filter_direct_open OPEN SOURCE DIRECT
LVS FILTER sch_filter_direct_short SHORT SOURCE DIRECT
LVS FILTER sch_filter_mask_open OPEN SOURCE MASK
LVS FILTER sch_filter_mask_short SHORT SOURCE MASK
LVS FILTER lay_filter_direct_open OPEN LAYOUT DIRECT
LVS FILTER lay_filter_direct_short SHORT LAYOUT DIRECT
// Filter out all Voltage and Current sources from LVS reports
LVS FILTER v OPEN
LVS FILTER i OPEN
LVS FILTER e OPEN
LVS FILTER f OPEN
LVS FILTER g OPEN

GROUP CONTINUOUS_DRC
          DRC3_1
          DRC3_2
          DRC7_1
          DRC7_2
          DRC9_1
          DRC9_2
          DRC15_1
          DRC15_2
          DRC22_1
          DRC22_2
```

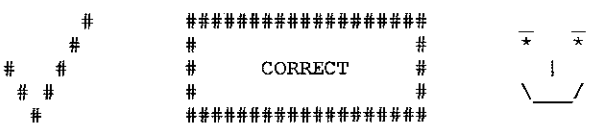
APPENDIX D

LAYOUT VERSUS SCHEMATIC (LVS) NETLIST

```
################################################
##                                            ##
##         C A L I B R E    S Y S T E M       ##
##                                            ##
##             L V S   R E P O R T            ##
##                                            ##
################################################
```

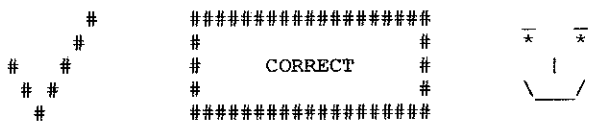
```
REPORT FILE NAME:          cmos_amp_sch.lvs.report
LAYOUT NAME:               cmos_amp_sch.lay.net ('cmos_amp_sch')
SOURCE NAME:               /home/student/cmos_amp_sch/tsmc035a/cmos_amp_sch_tsmc035a.spi
('cmos_amp_sch')
RULE FILE:                 /home/student/_tsmc035.rules_
CREATION TIME:             Mon Apr 16 11:07:53 2007
CURRENT DIRECTORY:         /home/student
USER NAME:                 student
CALIBRE VERSION:           v2004.3_9.21    Thu Sep 30 11:25:17 PDT 2004
```

OVERALL COMPARISON RESULTS




```
********************************************************************************
**********************
                                  CELL  SUMMARY
********************************************************************************
**********************

  Result          Layout                      Source
  ~~~~~~~~~~~     ~~~~~~~~~~~                 ~~~~~~~~~~~~~~
  CORRECT         cmos_amp_sch                CMOS_AMP_SCH


********************************************************************************
**********************
                                 LVS PARAMETERS
********************************************************************************
**********************


o LVS Setup:

   // LVS COMPONENT TYPE PROPERTY
   // LVS COMPONENT SUBTYPE PROPERTY
   // LVS PIN NAME PROPERTY
   // LVS POWER NAME
   // LVS GROUND NAME
   LVS RECOGNIZE GATES                    ALL
```

```
LVS IGNORE PORTS                          NO
LVS CHECK PORT NAMES                      NO
LVS BUILTIN DEVICE PIN SWAP               YES
LVS ALL CAPACITOR PINS SWAPPABLE          NO
LVS DISCARD PINS BY DEVICE                NO
LVS SOFT SUBSTRATE PINS                   NO
LVS INJECT LOGIC                          NO
LVS EXPAND UNBALANCED CELLS               YES
LVS EXPAND SEED PROMOTIONS                NO
LVS PRESERVE PARAMETERIZED CELLS          NO
LVS GLOBALS ARE PORTS                     YES
LVS REVERSE WL                            NO
LVS SPICE PREFER PINS                     NO
LVS SPICE SLASH IS SPACE                  YES
LVS SPICE ALLOW FLOATING PINS             YES
LVS SPICE ALLOW UNQUOTED STRINGS          NO
LVS SPICE CONDITIONAL LDD                 NO
LVS SPICE CULL PRIMITIVE SUBCIRCUITS      NO
LVS SPICE IMPLIED MOS AREA                NO
// LVS SPICE MULTIPLIER NAME
LVS SPICE OVERRIDE GLOBALS                NO
LVS SPICE REDEFINE PARAM                  NO
LVS SPICE REPLICATE DEVICES               NO
LVS SPICE STRICT WL                       NO
// LVS SPICE OPTION
LVS STRICT SUBTYPES                       NO
LAYOUT CASE                               NO
SOURCE CASE                               NO
LVS COMPARE CASE                          NO
LVS DOWNCASE DEVICE                       NO
LVS REPORT MAXIMUM                        50
LVS PROPERTY RESOLUTION MAXIMUM           32
// LVS SIGNATURE MAXIMUM
// LVS FILTER UNUSED OPTION
// LVS REPORT OPTION
LVS REPORT UNITS                          YES
// LVS NON USER NAME PORT
// LVS NON USER NAME NET
// LVS NON USER NAME INSTANCE

// Reduction

LVS REDUCE SERIES MOS                     NO
LVS REDUCE PARALLEL MOS                   YES
LVS REDUCE SEMI SERIES MOS                NO
LVS REDUCE SPLIT GATES                    YES
LVS REDUCE PARALLEL BIPOLAR               YES
LVS REDUCE SERIES CAPACITORS              YES
LVS REDUCE PARALLEL CAPACITORS            YES
LVS REDUCE SERIES RESISTORS               YES
LVS REDUCE PARALLEL RESISTORS             YES
LVS REDUCE PARALLEL DIODES                YES

// Filter

LVS FILTER  sch_filter_direct_open  OPEN SOURCE DIRECT
LVS FILTER  sch_filter_direct_short  SHORT SOURCE DIRECT
LVS FILTER  sch_filter_mask_open  OPEN SOURCE MASK
LVS FILTER  sch_filter_mask_short  SHORT SOURCE MASK
LVS FILTER  lay_filter_direct_open  OPEN LAYOUT DIRECT
LVS FILTER  lay_filter_direct_short  SHORT LAYOUT DIRECT
LVS FILTER  v  OPEN
LVS FILTER  i  OPEN
LVS FILTER  e  OPEN
LVS FILTER  f  OPEN
LVS FILTER  g  OPEN


                CELL COMPARISON RESULTS ( TOP LEVEL )
```



LAYOUT CELL NAME: cmos_amp_sch
SOURCE CELL NAME: CMOS_AMP_SCH

NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	2	2	
Nets:	10	10	
Instances:	3	3	MN (4 pins)
	5	5	MP (4 pins)
	1	1	C (2 pins)
	1	1	R (2 pins)
Total Inst:	10	10	

****
INFORMATION AND WARNINGS
****

	Matched Layout	Matched Source	Unmatched Layout	Unmatched Source	Component Type
Ports:	2	2	0	0	
Nets:	10	10	0	0	
Instances:	3	3	0	0	MN(N)
	5	5	0	0	MP(P)
	1	1	0	0	C(NOTCHEDROW)
	1	1	0	0	R(HR)
Total Inst:	10	10	0	0	

o Initial Correspondence Points:

Ports: VDD VSS

****
SUMMARY
****

Total CPU Time: 0 sec
Total Elapsed Time: 0 sec