

**DIRECT DIGITAL CONTROL OF PERMANENT MAGNET BLDC MOTOR
FOR AIR CONDITIONING**

By

HARYATTIE BINTI AZIZI

FINAL YEAR PROJECT REPORT

**Submitted to the Department of Electrical & Electronics Engineering
in Partial Fulfillment of the Requirements
for the Degree
Bachelor of Engineering (Hons)
(Electrical & Electronics Engineering)**

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CERTIFICATION OF APPROVAL

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A project dissertation submitted to the
Electrical & Electronics Engineering Programme
Universiti Teknologi PETRONAS
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Approved:



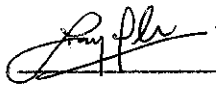
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**UNIVERSITI TEKNOLOGI PETRONAS
TRONOH, PERAK**

June 2007

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.



Haryattie binti Azizi

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ABSTRACT

This is a design project which to design a direct digital control of permanent magnet BLDC motor for air conditioning. Mainly the task of this to developed a control to the speed of BLDC motor that will determine the speed of compressor inside in an air-conditioner. The project is divided into two main tasks; the simulation part and circuitry part. This report will delivered results, discussion and feedbacks of the both parts that had been handled. The simulation is build inside MATLAB/SIMULINK while the circuitry part is built by using equipments of Lab-Volt. It composed from blocks that are mainly based on calculation or theoretical value. So it is completely logical blocks and shall not interface with other Power Electronic block set components inside MATLAB. From here the author learns relationship between Sensorless BLDC motor and BLDC motor with Hall Sensor. In circuitry part, the IGBT inverter by supplying PWM control signals. From here the author learns that the output voltage depends on switching process and the DC input. Due to lots of advantages deliver by BLDC motor, this project brings a lot of benefit.

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LIST OF ABBREVIATIONS

DDC – Direct Digital Control

AC – Alternating Current

DC – Direct Current

BLDC motor – Brushless DC Motor

PWM – Pulse Width Modulation

EMF - Electromotive Force

L- Inductor

C- Capacitor

CHAPTER 1

INTRODUCTION

1.1 Background of Project

BLDC abbreviation for Brushless DC motor had been widely used due to its advantages. In air conditioning, BLDC motor had been used in compressor to enable the compressor to start at high revolution speed as soon the air conditioning system is turned on. [1] This project mainly focused on the application of BLDC motor for compact and small car air conditioner.

The drive system, use Direct Digital Control or DDC as electronic control interface for BLDC motor. Under DDC, microcontroller is implemented. This system had contributed to hybrid vehicle such as Toyota's new Prius, Toyota Harrier Hybrid and Toyota Kluger Hybrid. This system had many advantages over universal DC motor or brushed DC motor as stated under "Permanent Magnet Brushless DC motors for Consumer Products". [2]

1.2 Problem Statement

Originally, the most common brushed motor had been widely used in many facilities such as in vacuum cleaners and washing machines as the manufacturing cost being quite low. However, many flaw arise such as relatively inefficient and having high acoustic noise emissions. The BLDC motor had offers with potential of increasing the efficiency and reliability.

Basically the purpose of this project is to control the speed of a BLDC motor for a car air conditioner.

1.3 Objectives

The objectives of this project are as follow:

- To develop a digital controller to control the speed of BLDC motor for a car air conditioner
- To design the control circuit, power circuit to operate the BLDC motor from a battery source
- To model and simulate design with MATLAB/SIMULINK
- To construct the digital controller and power circuits

1.4 Project Planning

During this semester, it is proposed to design and construct the controller for BLDC motor. The process also involves simulation of the drive system using MATLAB/SIMULINK. Also it is proposed to implement the microcontroller for direct digital control. The full Gantt chart for the plan time frame is presented in Appendix.

CHAPTER 2

LITERATURE REVIEW AND THEORY

In continuation of preliminary report submitted in the first semester, the following chapters explain the project objectives of the second semester. Figure 1 show the BLDC drive system.

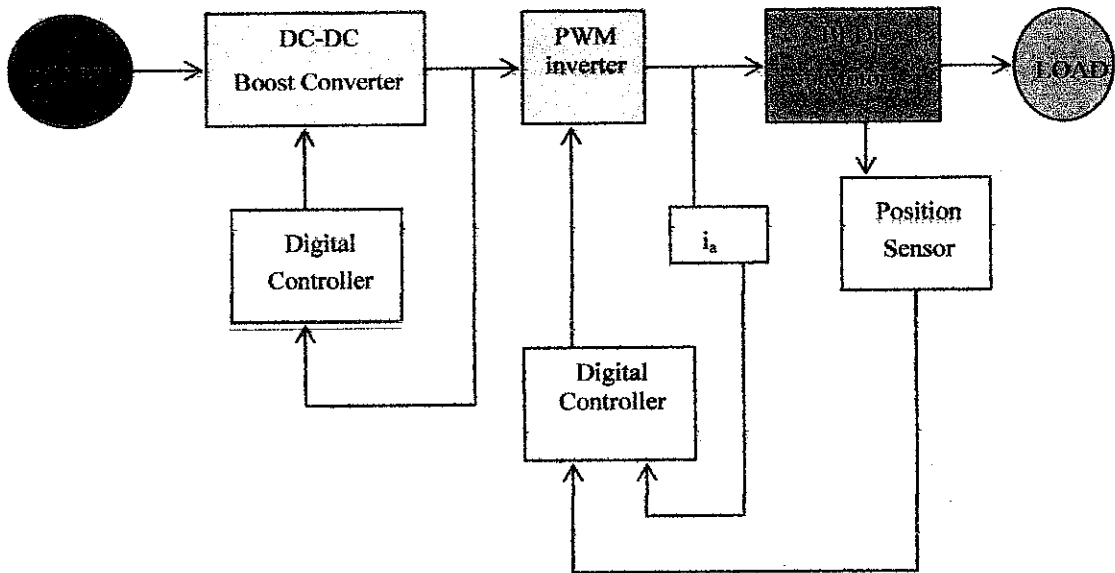


Figure 1 BLDC drive system

2.1 Brushless DC Motor

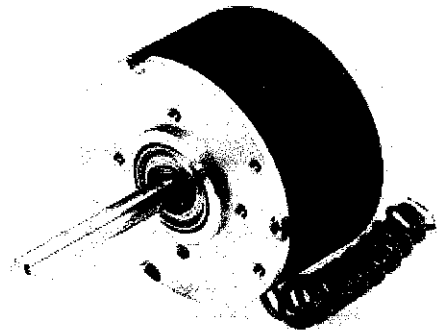


Figure 2 BLDC motor

The information provided by a vendor for a Brushless DC motor with integral Electronics as shown in Figure 2 published [3] that it is typical for scientific applications (stirring equipment, pumps, mixing machine) and industrial applications (fans and conveyor). The motor itself is already equipped with internal drive electronics that provides control. There are two main components inside the motor; internal speed regulation and electronic commutation. The full specification of the motor are listed in the Appendix.

Generally the motor's speed can be controlled by changing the terminal voltage. As shown in Figure 3 it is observed that by increasing the terminal voltage, the speed will also increase. [7]

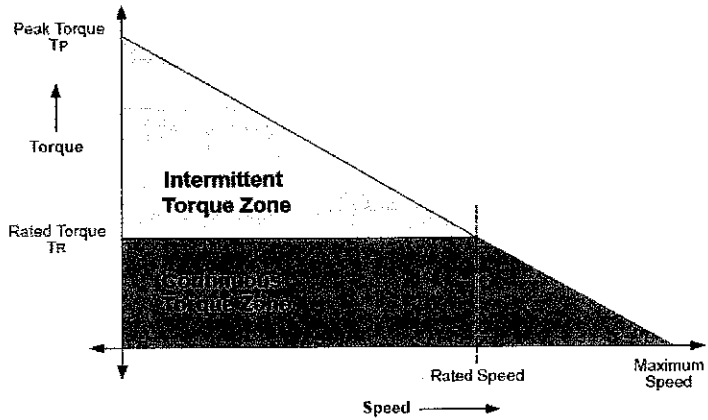


Figure 3 Torque-speed characteristic for BLDC motor.

A BLDC motor is a type of synchronous motor. As usual it consists of two main parts- stator and rotor. The stator, it consists of piled steel laminations with windings placed in the slots that are axially cut along the inner periphery. [7]

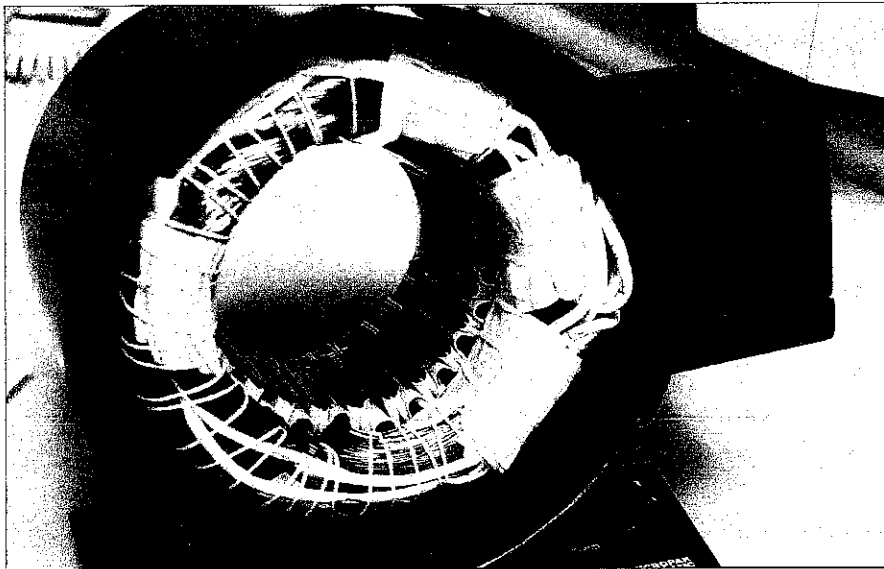


Figure 4 Stator of BLDC motor.

The rotor, it is made from permanent magnets that can vary from two to eight pole pairs with alternate North (N) and South (S) poles. [7]. Figure 5 show the arrangement of permanent magnets in rotor.

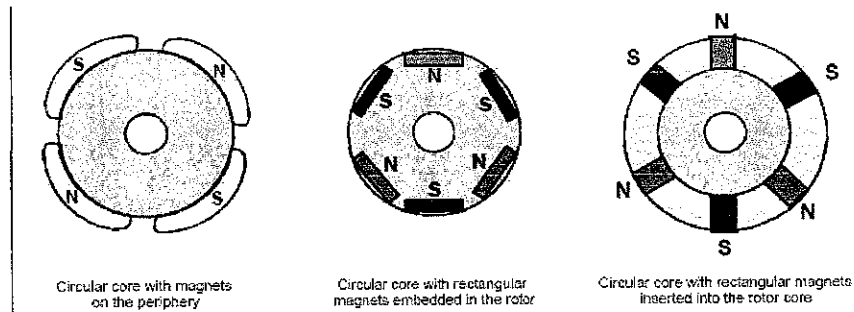


Figure 5 Arrangement of permanent magnet in rotor.

2.2 Simulation Tools

As explained earlier, the main simulation tools that will be used are PSPICE and Matlab/Simulink. The project will be concentrated on first part; the simulation. Matlab/Simulink is the most suitable simulation tools for an electromechanical system. It is essential to develop the simulation model.

For a drive system such as a BLDC motor drive, the simulation tool would be Matlab/Simulink to model the control aspects.

2.3 Pulse Width Modulation Inverter

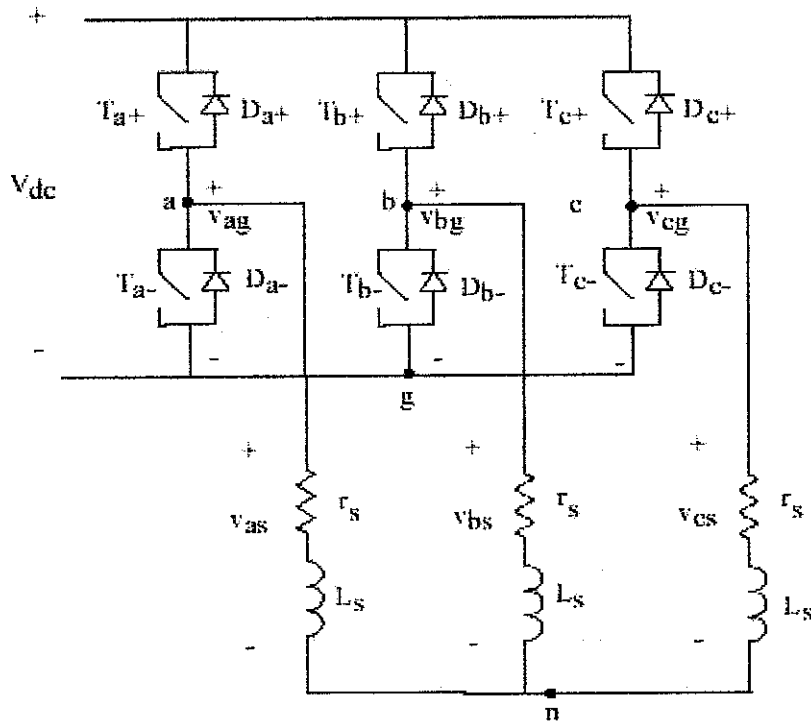


Figure 6 PWM inverter with R-L load

A PWM inverter as shown in Figure 6 is a part of the BLDC drive system. The purpose of inverter itself is simply to invert DC to AC. The objective of using specifically PWM inverter is to shape and control the three-phase output voltages in magnitude and frequency with respect to the DC input voltage. The stator of the motor is represented by the three phase loads. The input source voltage to inverter is DC voltage, V_{DC} . The output will be displaced by 120° with respect to each other. The output voltage for each leg (V_{ag} , V_{bg} , V_{cg}) depends on the input voltage, V_{DC} and the switch status and independent of the output current. It also means that the output voltage is independent of direction of the load current.

2.3.1 Operation of PWM Inverter

The inverter is fed by a dc voltage and has three phase-legs each consisting of two transistors and two diodes (labeled with subscripts a, b, c). With Sine-Triangle Pulse Width Modulated (STPWM) control, the switches of the inverter are controlled based on a comparison of the sinusoidal control signal and a triangular switching signal. The sinusoidal control waveform establishes the desired fundamental frequency of the inverter output, while the triangular waveform establishes the switching frequency of the inverter. The ratio between the frequencies of the triangle wave and the sinusoid is referred to as the modulation frequency ratio. The switches of the phase legs are controlled based on the following comparison [10]:

$$\begin{aligned}
 v_{control(phase-a)} > v_{triangle}, T_{a+} \text{ is on} \\
 v_{control(phase-a)} < v_{triangle}, T_{a-} \text{ is on} \\
 v_{control(phase-b)} > v_{triangle}, T_{b+} \text{ is on} \\
 v_{control(phase-b)} < v_{triangle}, T_{b-} \text{ is on} \\
 v_{control(phase-c)} > v_{triangle}, T_{c+} \text{ is on} \\
 v_{control(phase-c)} < v_{triangle}, T_{c-} \text{ is on}
 \end{aligned}$$

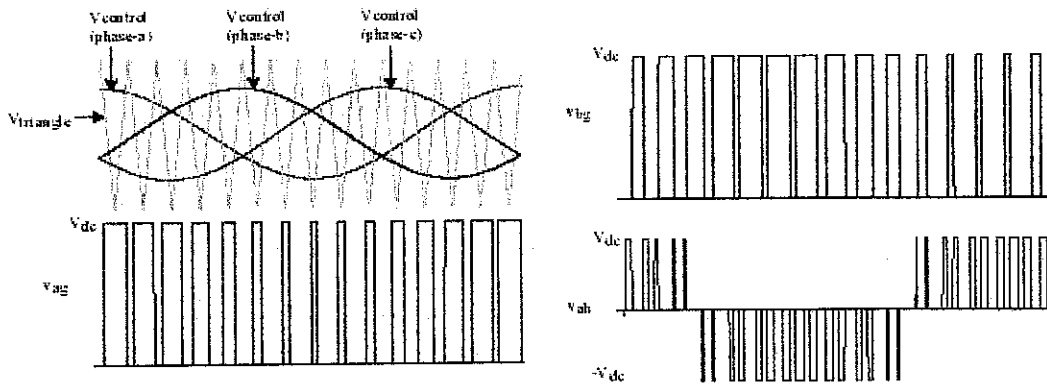


Figure 7 Sine-triangle, pulse-width-modulated control waveforms, phase voltages V_{ag} and V_{bg} , and line voltage V_{ab}

As shown in Figure 7, when the comparison is made, the output voltage range varies from the input voltage value and zero. For the line voltage, the dc components will cancel out. Thus the range will be from $+V_{DC}$ to $-V_{DC}$.

CHAPTER 3 METHODOLOGY

3.1 Flowchart

The flowchart shown in Figure 8 indicates the methodology of this project.

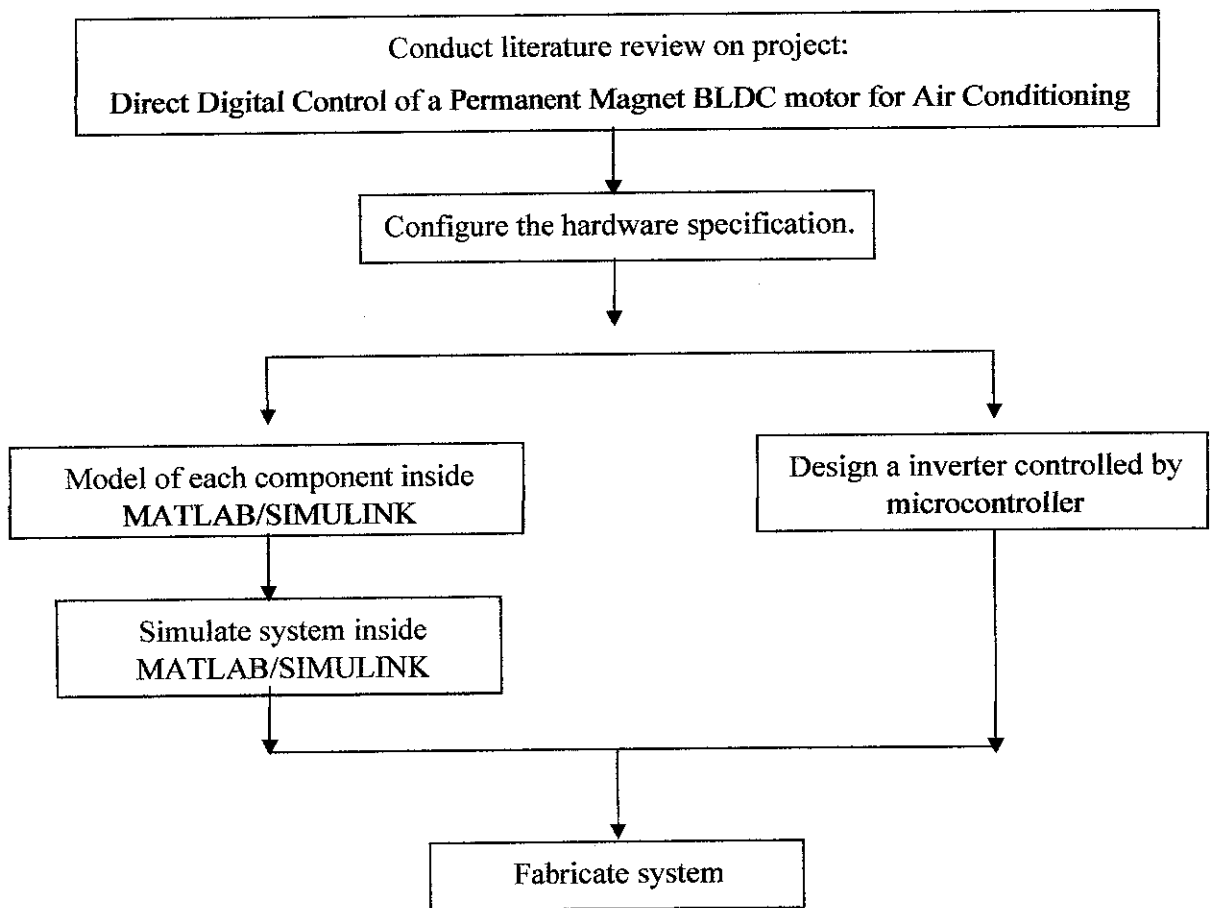


Figure 8 Flowchart

3.2 Tools

The following tools are used for software and hardware requirements of the project:

- Matlab/Simulink
- Lab-Volt Power Electronics Equipment

The simulation is conducted using Matlab/Simulink. The results of the simulation are discussed in Chapter 4 where the usage of this software is optimized. Most of the circuits for this project are built in the Power Electronics laboratory using the Lab-Volt Power Electronics Equipment. The prototype circuit is built from the available modules in the laboratory and the motor purchased from vendors.

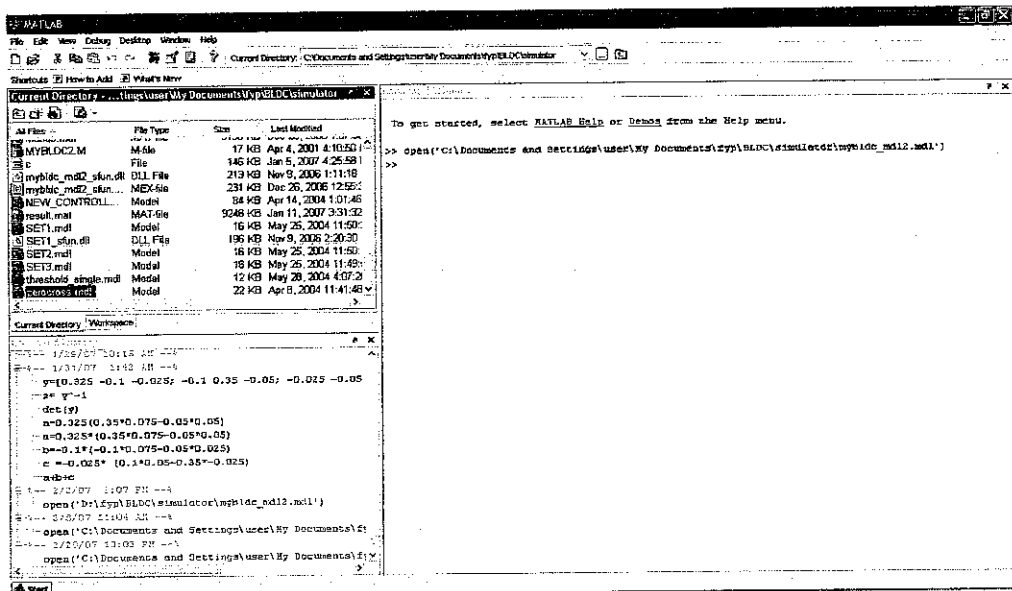
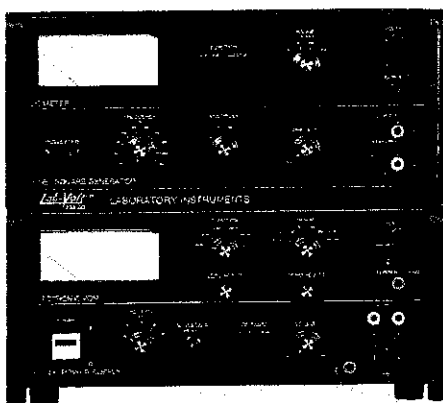


Figure 9 Matlab software



Laboratory Instrumentation System (438)

Figure 10 Lab-Volt Power Electronics Equipment

CHAPTER 4

RESULTS AND DISCUSSION

4.1 Simulation with Matlab/Simulink

The main task of simulation is to handle the model and run it with the specified design requirements. Initially the simulation is run for the inverter and BLDC motor parts. The converter part is then simulated separately. Following is the explanation of each block that is used for the simulation. The blocks are:

- myblcdc block
- estimation block
- zero crossing block
- IC block
- 120 deg trigger block
- Controller block
- All phase block

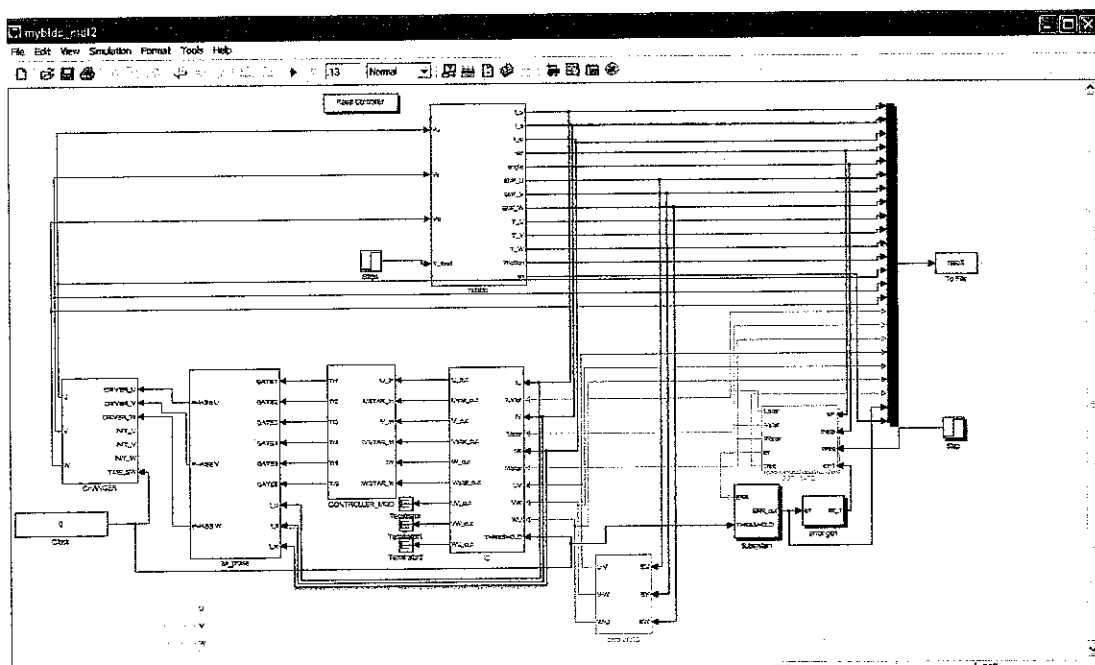


Figure 11 BLDC motor simulator

4.1.1 The mybldc block

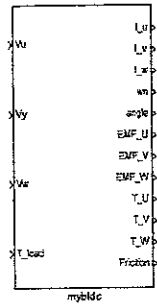


Figure 12 mybldc block

This block act as a BLDC motor, where it will take inputs of three-phase voltage and load torque values. This block consists of two sub blocks; my state-space and S function. The state space model is developed from the mathematical model representing the motor equations.

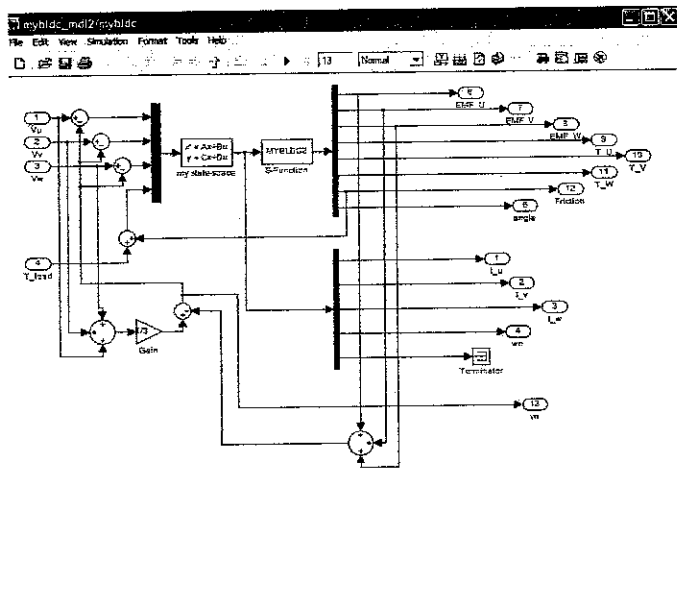


Figure 13 Inside of mybldc block

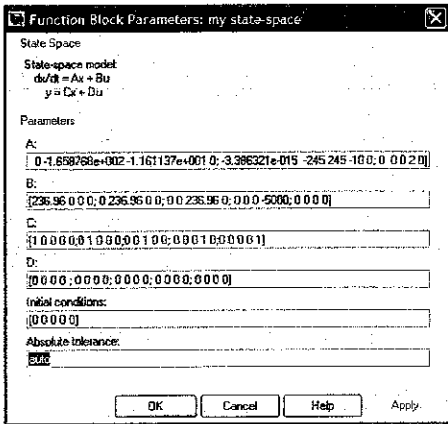


Figure 14 my state space parameters

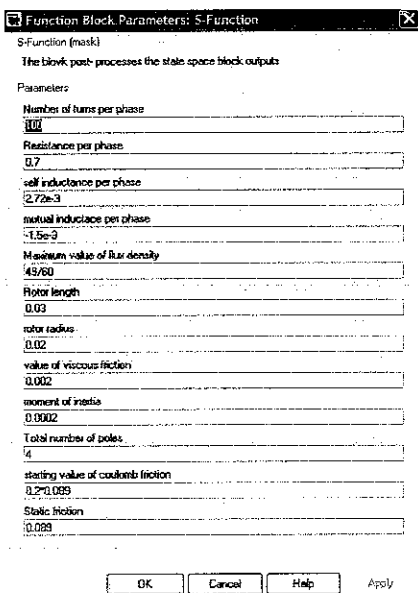


Figure 15 S function parameters

If the models of the BLDC motor changes, the armature resistance and inductance will need to change. However due to lack of information, the changes will be made on resistance only. This are the outputs that produce from myblcdc block:

- I_u, I_v, I_w are the individual phase currents
- ω_n is the rotor electrical speed in rad/s
- $angle$ is the rotor electrical position as compared to the initial position
- EMF_U, EMF_V, EMF_W are the back emf values generated in the three phases.
- T_U, T_V, T_W are the individual phase torques.

- *Friction*: the values of the friction faced by the rotor. Contains both static and coulomb friction.
- *vn* is the neutral point node voltage.

4.1.2 The estimation block

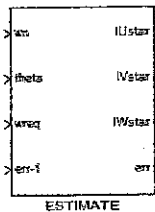


Figure 16 Estimation block

This block calculates the error between the actual and command speed. The input to this block is taken from the mybldc block and error gen block. The inputs will be the actual value of the motor speed, rotor shaft position, the required rotor speed and lastly the fed back from the output. From this block the outputs such as command phase currents, error between command speed and actual speed and value of torque to be generated are observed.

This block can be considered to be inside the BLDC motor itself in real world and cooperates with the next block to perform the Hall Sensor part of the motor.

4.1.3 Zero crossing block

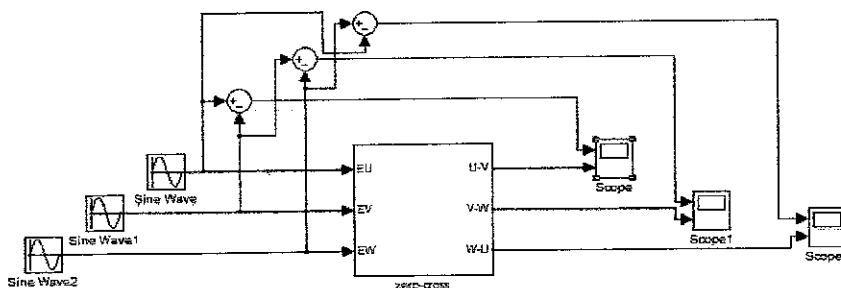


Figure 17 Zero crossing block

This block performs the translation of Hall Sensor inside the BLDC motor. The input parameters to this block are the back EMF for all the three phases from the motor. Then the zero crossing will translate the input into 1 and 0 output only. The inputs and output of all three phases are shown in Figure 18 to 20.

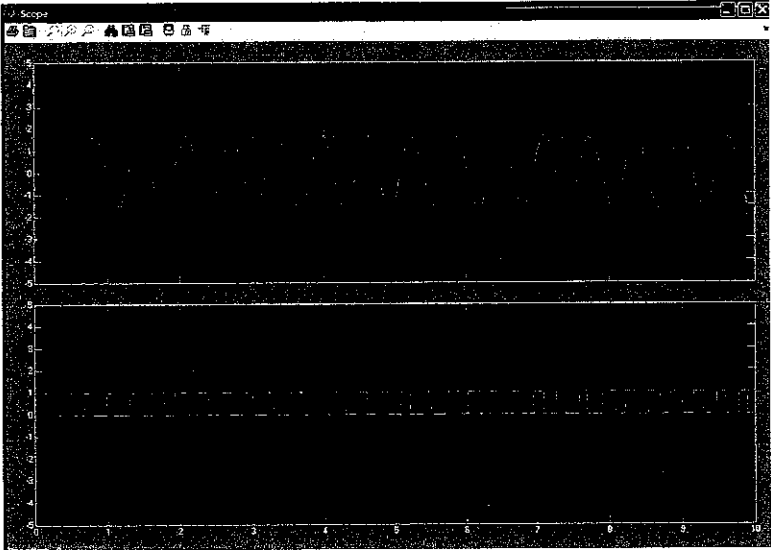


Figure 18 Zero crossing detection for Back EMF phase U and phase V

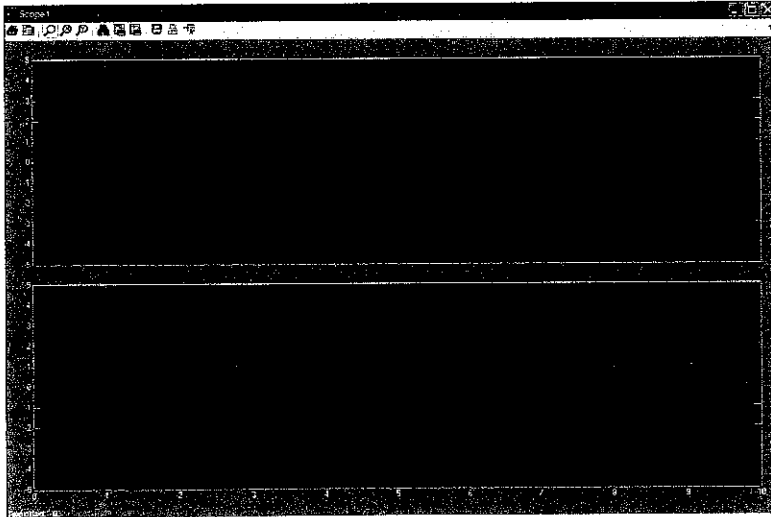


Figure 19 Zero crossing detection for Back EMF phase V and phase W

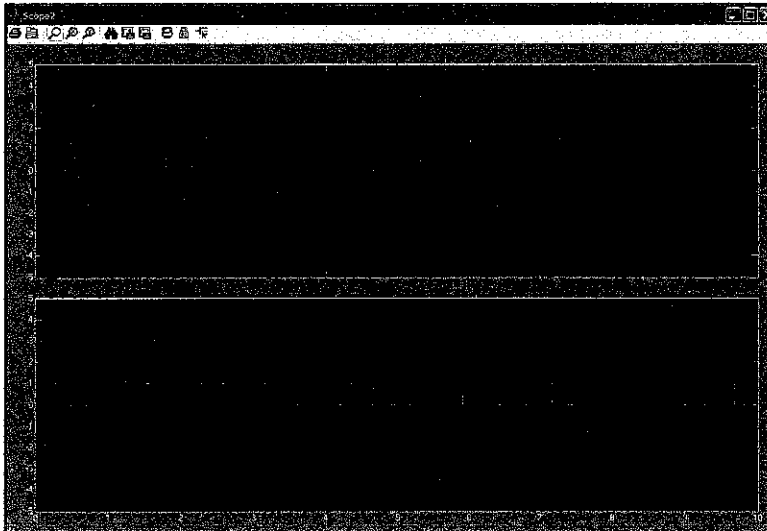


Figure 20 Zero crossing detection for Back EMF phase U and phase W

4.1.4 IC and 120 deg trigger blocks

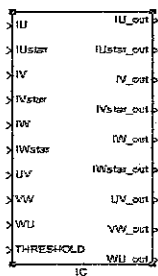


Figure 21 IC block

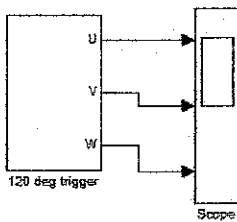


Figure 22 120 deg trigger block

According to the author [9], the 'IC' block is used to hold the controller to its initial state till the time motor picks up sufficient speed and the back EMF voltages are significant. This system however resembles the sensorless BLDC. But it still would

be significant for the use of the present work. Inside the IC block, there are a number of switches to select the output. These switches will be changing with the threshold time that had been set.

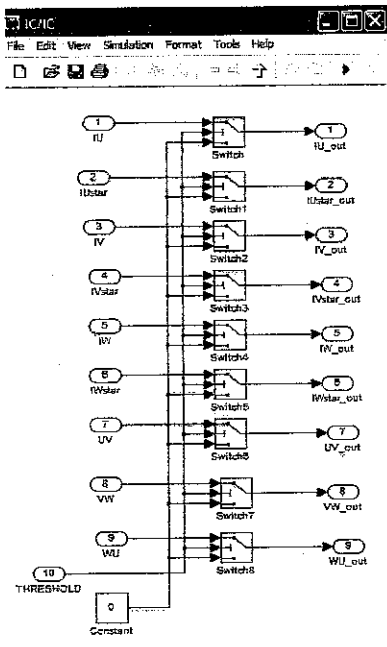


Figure 23 Sub block of IC

Next would be the 120 deg trigger block which will give initial value to the system to ramp up the motor for a threshold time. Then it will disconnect the 120 deg trigger block from the system to perform the closed loop operation.

4.1.5 The Controller block

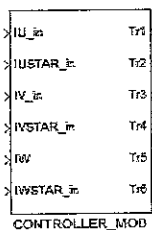


Figure 24 Controller block

The controller block takes the output of the IC block and triggers the appropriate gates of inverter. This system will work as inverter to supply the input voltages to the BLDC motor. The reference of inverter structure is as shown in Figure 25:

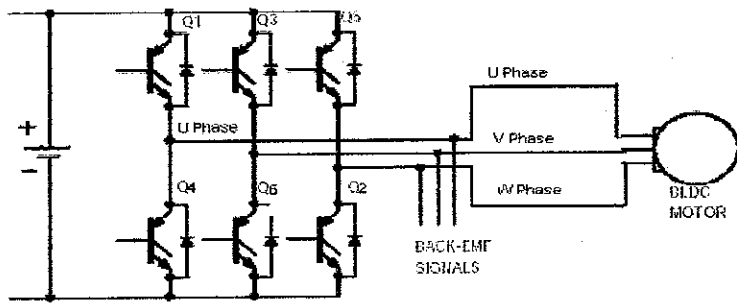


Figure 25 Reference structure of Inverter

The sub system of the controller block can be viewed in Figure 26:

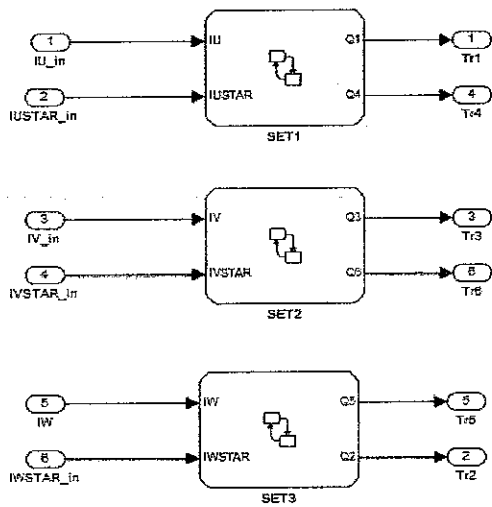


Figure 26 Sub system of controller block

4.1.6 The All Phase block

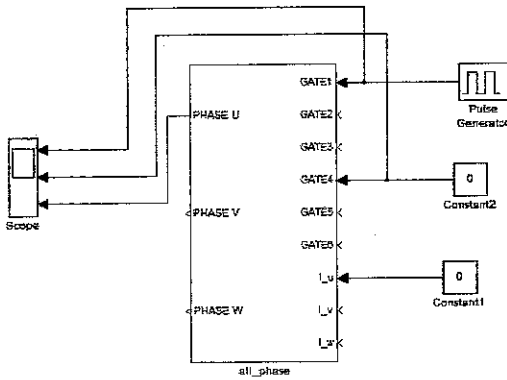


Figure 27 All Phase Block

This block takes input from the controller which is meant for the gates of the inverter. The output voltage at Phase U is observed. The results can be seen below. Due to constant value in Gate 4, the phase voltage will take the positive terminal of the voltage source.

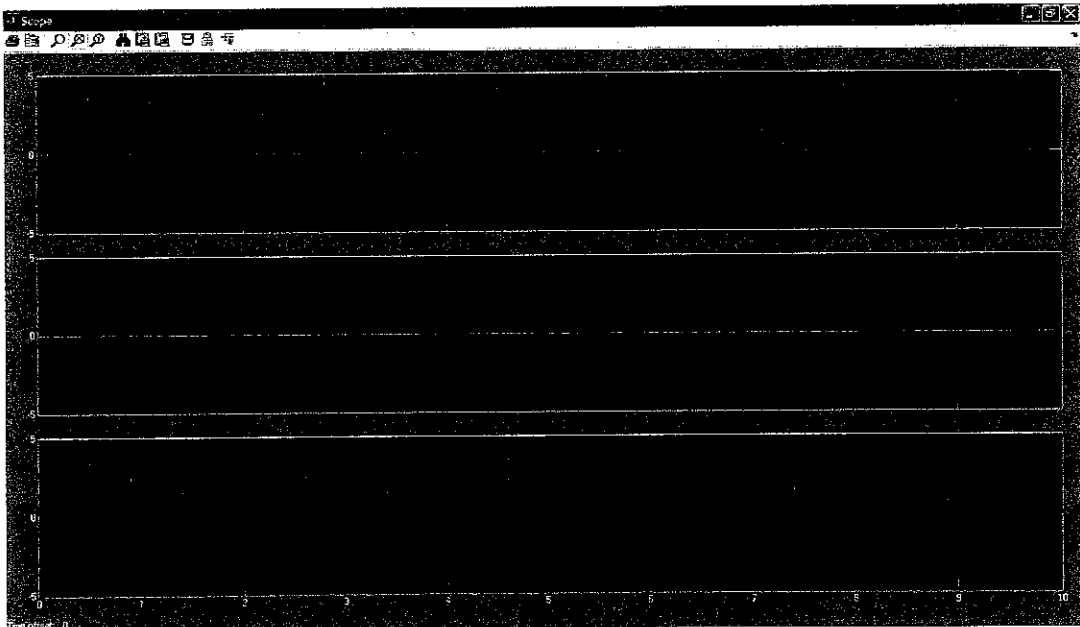


Figure 28 Output of voltage at phase U

4.2 Results and Discussion of simulation

The simulation is initiated with a specific amount of DC input voltage to the inverter. In this simulation it is assumed that the output from the converter is ideal and without any losses. The specified amount that has been changed in the model are the excitation voltage, resistance per phase, inductance per phase and speed reference.

4.2.1 Stator phase currents

Figure 29 shows the result of simulation of stator phase currents. These stator currents support the equation given where they will pass through resistance and inductance. These currents are also proportional to the torque load on the motor shaft.

$$V_t = IR + pLI + BEMF \dots\dots(1)$$

$$Torque = K_t \times I \dots\dots(2)$$

V_t = Voltage applied to motor per phase

I = Stator currents per phase

$p = d/dt$

L = Inductance per phase

R = Resistance per phase

BEMF = back EMF per phase

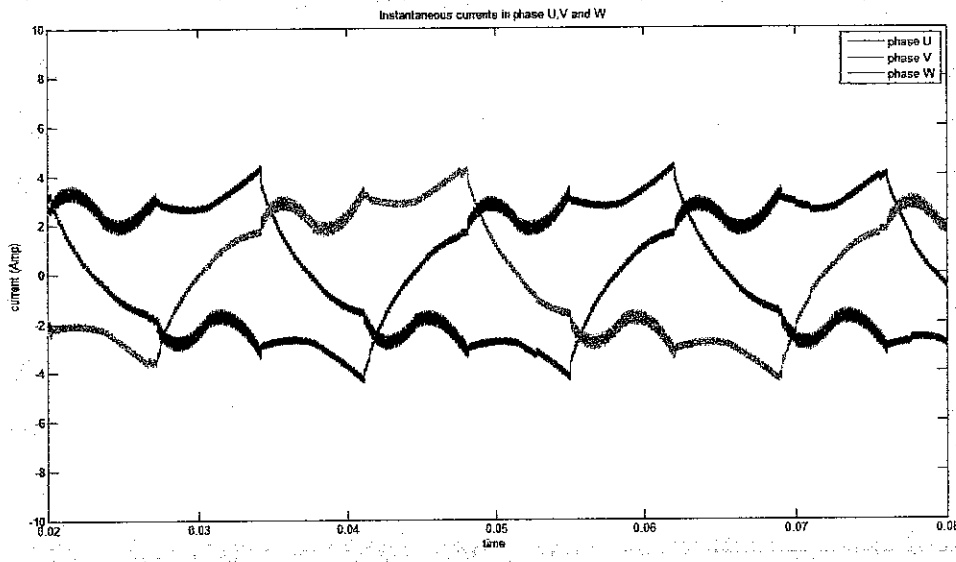


Figure 29 Instantaneous currents in phase U,V and W

4.2.2 Rotor speed

The BLDC motor must produce speed that is equivalent to the reference speed. This reference speed is entered into the estimate block. For this analysis the value had been chosen to be 75 rad/s. Inside the estimate block, it will calculate error (difference of actual to reference speed). Next, a simple PID controller will give required torque. This will directly pass the information to BLDC motor that will force the motor to require reference speed. Figure 30 show the rotor speed.

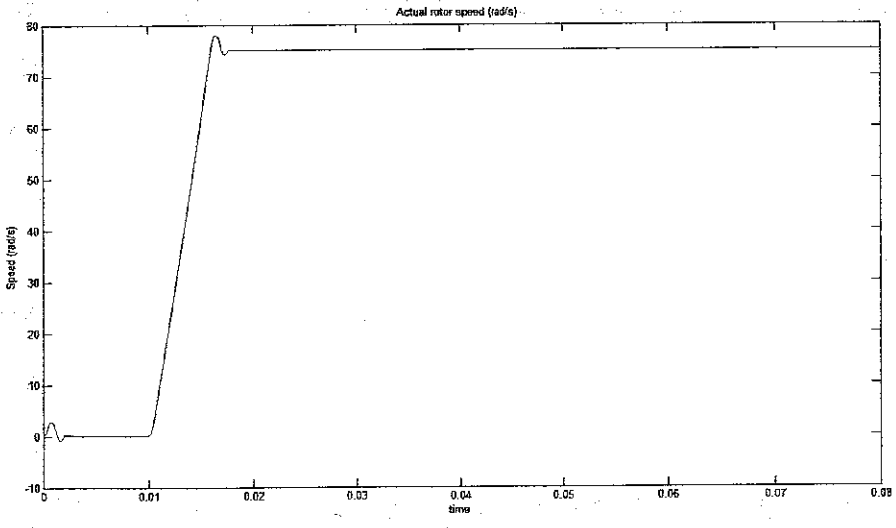


Figure 30 Actual rotor speed

At the early period, the motor does not react to any changes. At time 0.01, the speed started to increase and experienced some overshoot. The overshoot maybe due to the PID controller that had been used but the speed does not have oscillations and able to achieve required speed at 0.02 sec.

4.2.3 Voltage applied to BLDC motor

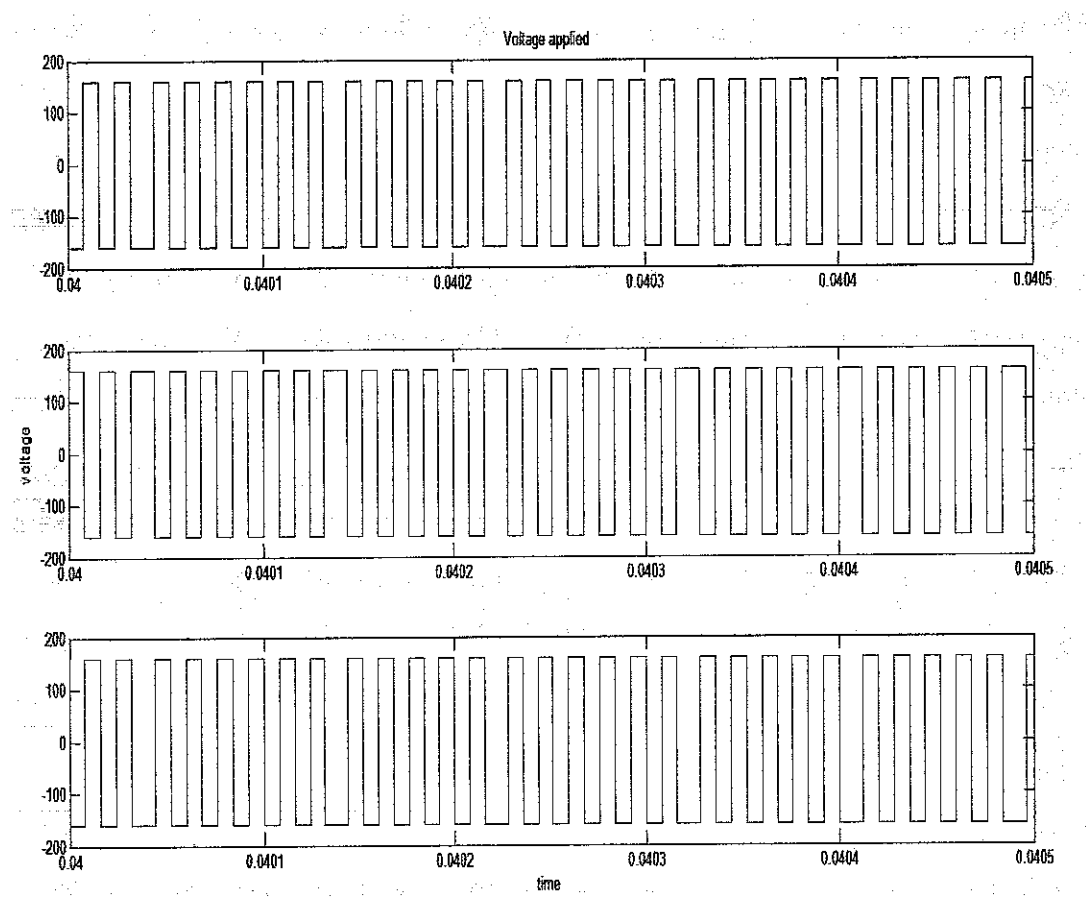


Figure 31 Voltage applied to Phase U, V and W

The voltage applied to motor is the output from changer block and all_phase block. This combination of blocks can be defined as inverter. The output will have variation in frequency. This can be seen from Figure 31. The output is affected by Pulse Width Modulation (PWM) which is based on voltage to frequency ratio. For a fixed voltage, the frequency can be varied. The voltage is varied from +160V to -160V. This will be same to the other two phases.

4.2.4 Back Electromotive Force

Back EMF or Back Electromotive Force is the potential difference experienced by the stator coils induced by rotating permanent magnet of BLDC motor. Back EMF is produced when the motor starts to spin. It will be directly proportional to the speed. Figure 32 shows the shape of back EMF produced in the three phases. Each of the phases will experience +3.65 V to -3.65 V. The back EMFs' also experience difference of 120° with each phase. For an ideal motor, assuming that the impedance is equal to zero from equation 1 the back EMF will be equal to voltage supplied.

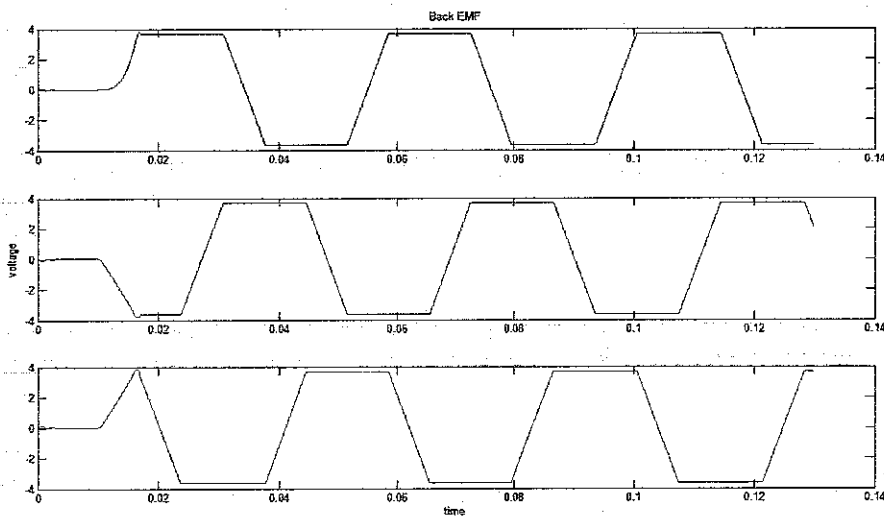


Figure 32 Back EMF for Phase U,V and W

4.2.5 Currents after controller

The currents from the controller are shown in Figure 33 as affected by PWM. The PWM is acting as a limiter to affect the excessive current which is limited by the applied voltage at start up. The torque required is evaluated from the PID controller. The output current is bounded together with the base current. To simplify the simulation, only one phase is calculated and the other two is only repeated but shifted by 120° . The currents generated from the controller is labeled as I_{Ustar} , I_{Vstar} and I_{Wstar} .

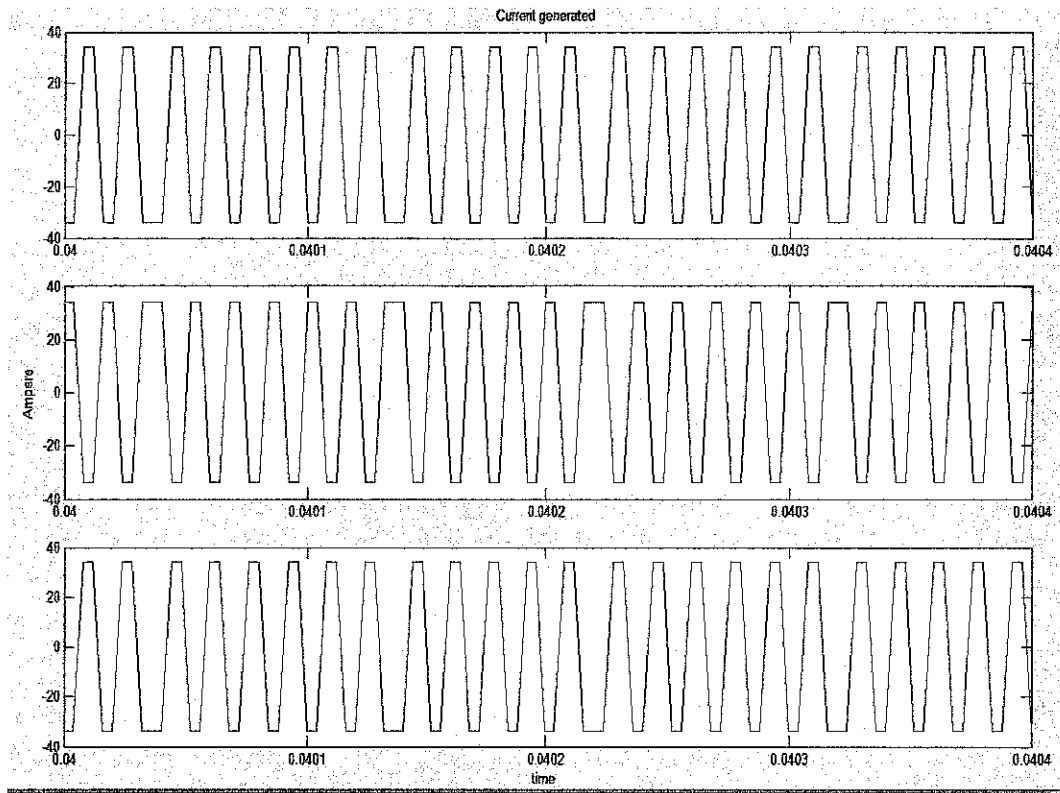


Figure 33 Current generated after controller to Phase U, V and W

4.2.6 Zero crossing

Zero crossing is to evaluate the zero crossing between two phases of back EMF. This also will act like output from Hall sensor that gives 1 and 0. This signal can help to synchronize the inverter and controller.

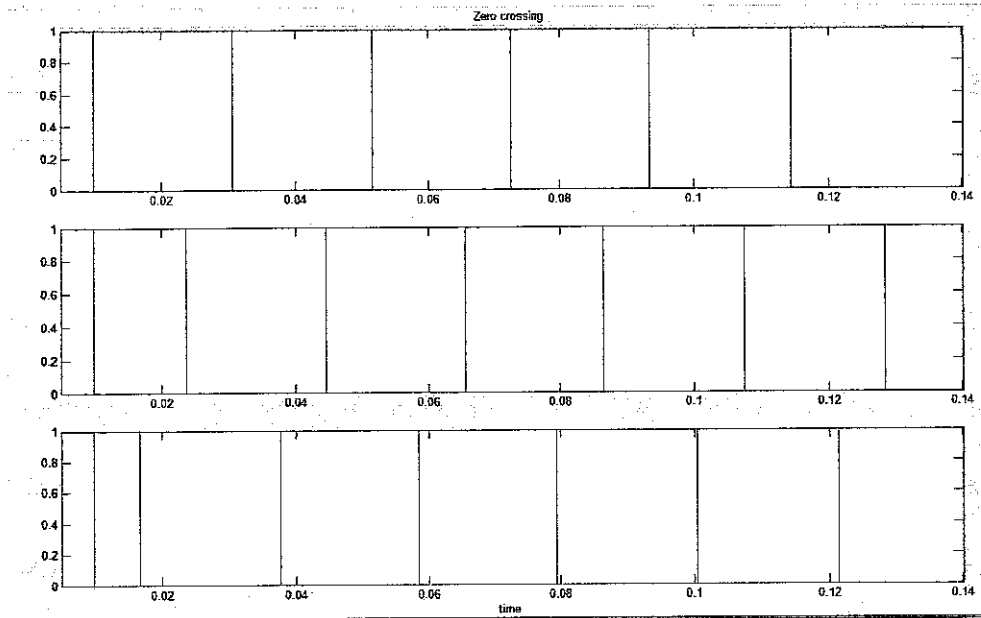


Figure 34 Zero crossing to Phase U, V and W

In Appendix C, the output waveforms of the whole simulation are presented. The steady state simulation results are satisfactory and as expected.

4.3 Construct the digital controller and power circuits

4.3.1 Designing boost converter

A dc-dc boost converter with a controller connected to the gate of the MOSFET is shown in Figure 35. The circuit is a type of flyback circuit. The basic concept is easy to understand. When the MOSFET, Q, turns on, the current flows through the inductor, L, begins to ramp up linearly resulting in energy storage in the inductor. The MOSFET turns off before the inductor saturates. At this time, the inductor releases its energy to the storage capacitor, C, and the load. Thus the output voltage is more than the input voltage.

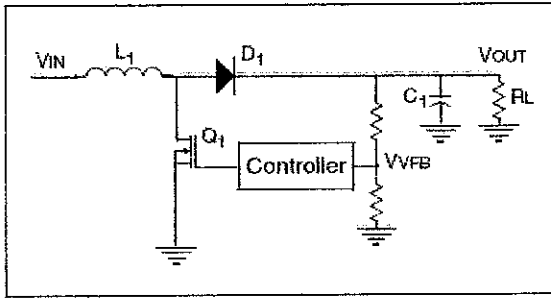


Figure 35 Boost converter topology

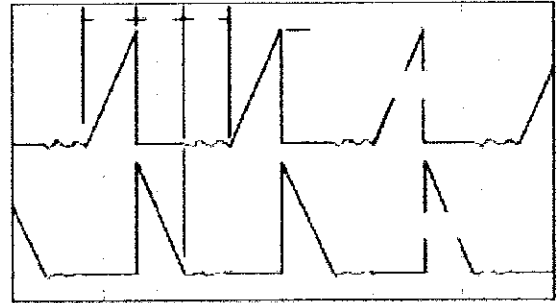


Figure 36 The switch and diode current

The proposed design parameters for the boost converter are listed in Table 1.

Table 1 Design parameters

Parameters	Value
V_{IN}	12V
V_{OUT}	30V
P_{OUT}	40W
$F = 1/T$	1.5 kHz
η (efficiency)	80%
ΔV_{DROP} (output ripple voltage)	50 mV (2%)

From the parameters, the L and C components are designed for continuous current operation as follows:

Duty cycle, D:

$$D = 1 - \frac{V_{in}}{V_{out}} = 1 - \frac{12}{30} = 0.6 \dots \dots (3)$$

The inductance minimum value, L_{CRIT} :

$$L_{crit} = \frac{RT}{2}(1-D)^2 D \dots\dots(4)$$

$$T = 0.6667ms$$

$$R = \frac{V_{out}^2}{P_{out}} = \frac{(30)^2}{40} = 22.5\Omega \dots\dots(5)$$

$$L_{crit} = 720\mu H$$

L = 1 mH, since L must be greater than L_{CRIT}.

Output ripple voltage:

$$\frac{\Delta V_{drop}}{V_o} = \frac{D}{RCf} \dots\dots(6)$$

$$0.02 = \frac{0.6}{(22.5)C(1.5k)}$$

$$C = 888\mu F$$

The values of capacitor and inductor are implemented from above calculation to design the boost converter for the system. The converter is connected to the inverter to supply a constant value of voltage. The boost converter is assumed to work in continuous conduction mode.

4.3.2 Experimental test on BLDC motor

The experimental setup for testing the BLDC motor is as shown in Figure 37. The power supply as mentioned earlier comes from boost converter providing a fixed value of DC voltage to the inverter. For this project, the main aim is to build a controller that will be able to control the speed of BLDC motor, which takes the response of BLDC motor and reference speed as input to the controller.

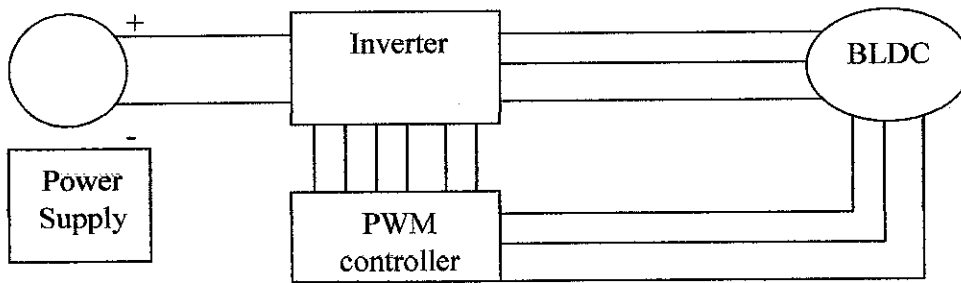


Figure 37 Experimental setup

The PWM controller provides gating pulses to turn-on the IGBT/MOSFET switches of the inverter. These pulses correspond to the signals generated by the Hall Sensor of BLDC motor. Finally the inverter converts the DC voltage to an AC voltage translated by the effect of pulses provided by the controller. This procedure continues until the speed of BLDC motor match the reference speed.

Three types of tests are conducted on BLDC motor.

- Test BLDC motor without Hall Sensors feedback to the Lab-Volt controller
- Test BLDC motor while Hall Sensor are attached along with constructed controller
- Test BLDC motor with designed controller

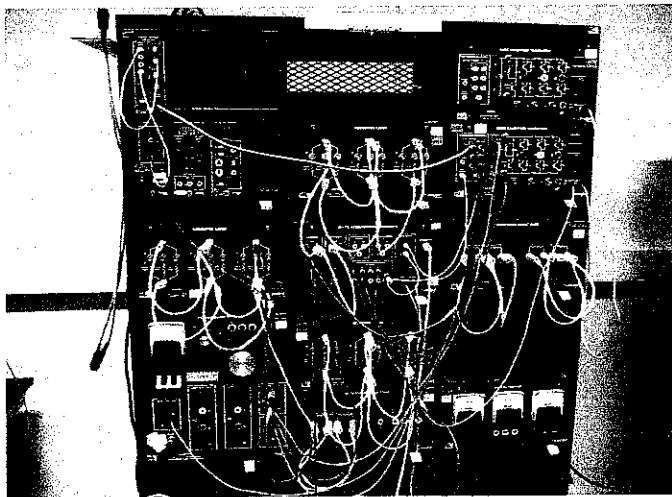


Figure 38 Lab-Volt control unit and inverter

4.3.3 Test BLDC motor without Hall Sensor feedback to the Lab-Volt controller

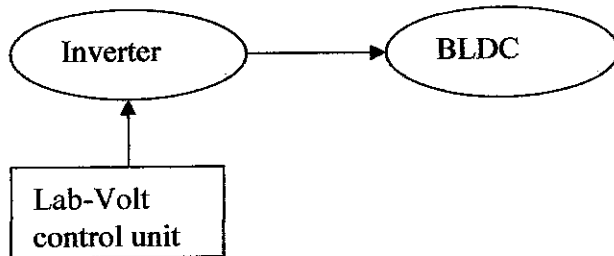


Figure 39 Test BLDC motor without Hall Sensor feedback to controller

In the first part, the test is conducted in the Power Electronics laboratory where the Lab-Volts equipments are being used. The equipments that are involved in testing are:

- Mobile Workstation (8110)
- Power Supply (8821-2X)
- Enclosure/power supply (8840)
- Connection leads and accessories (8951)
- Chopper/Inverter Control Unit (9029)
- Resistive loads (8311)
- Smoothing Inductors (8325-1X)
- IGBT Chopper/inverter module (8837-AX)

A variable DC voltage power supply is selected where the DC input can be varied from zero to 315V. In the Chopper/Inverter control unit, the mode is chosen to be V/F to obtain PWM response. The responses of pulses trigger the IGBT switches of the controlled inverter by the control unit. There will be a knob call DC SOURCE 1 that will regulate the duty cycle which will correspond to the frequency of the voltage applied to the BLDC motor. Figure below show the Chopper/Inverter control unit.

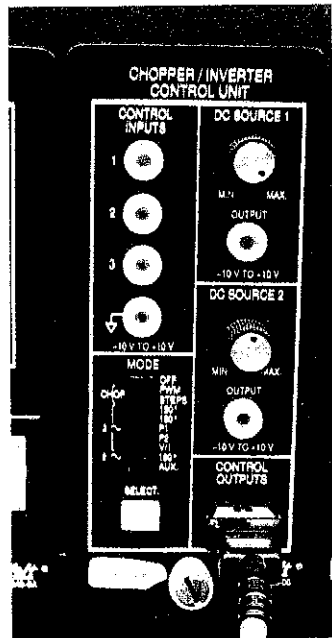


Figure 40 Chopper/Inverter control unit

When DC SOURCE 1 is tuned from minimum to middle range of the knob, the shaft of BLDC motor will turn in clockwise, and when turned from middle to maximum, the shaft turns anticlockwise. From the conducted test the waveforms observed are voltage supply, voltage from inverter, current from inverter and speed of motor. For this part, the test is conducted in anticlockwise manner.

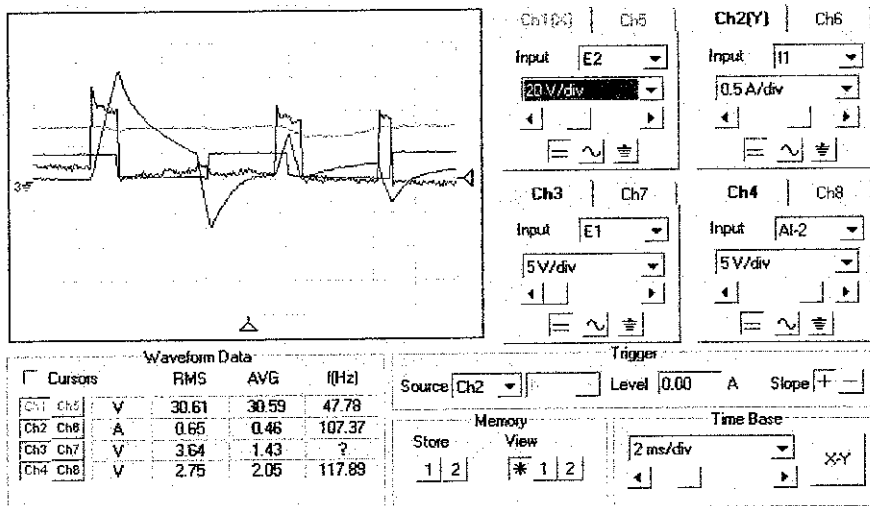


Figure 41 At 20% duty cycle

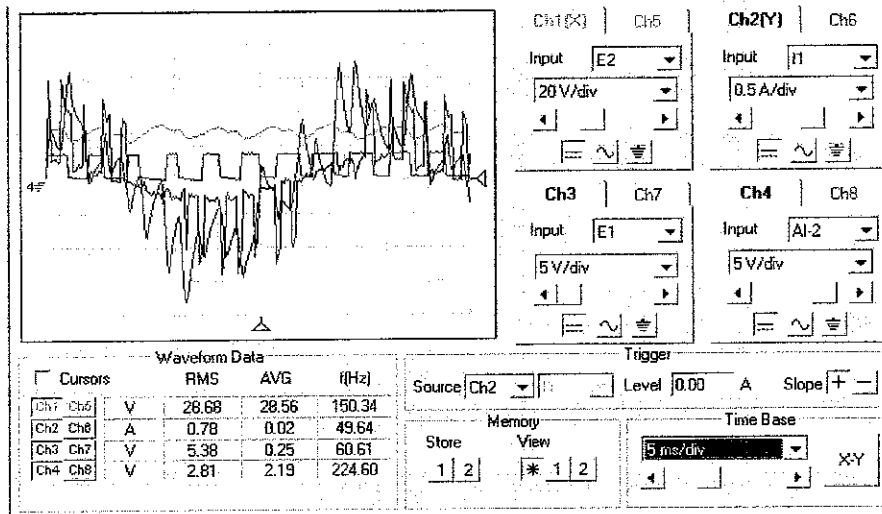


Figure 42 At 30% duty cycle

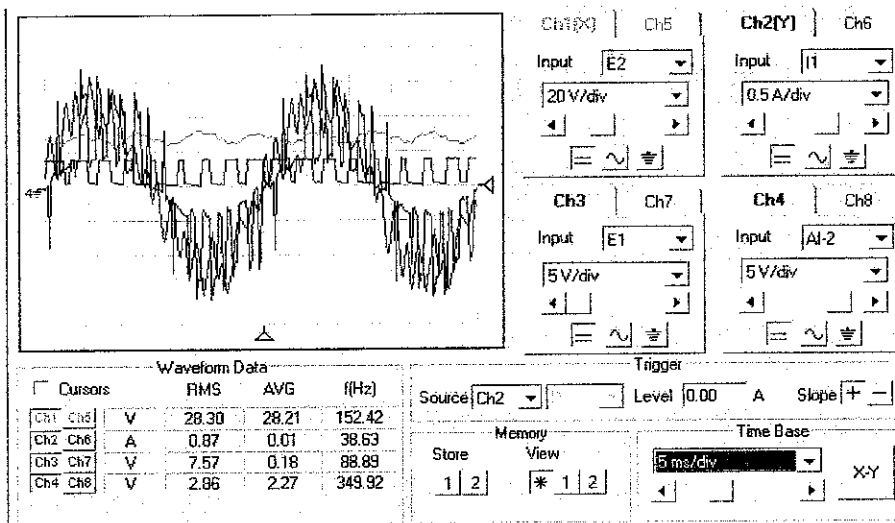


Figure 43 At 40% duty cycle

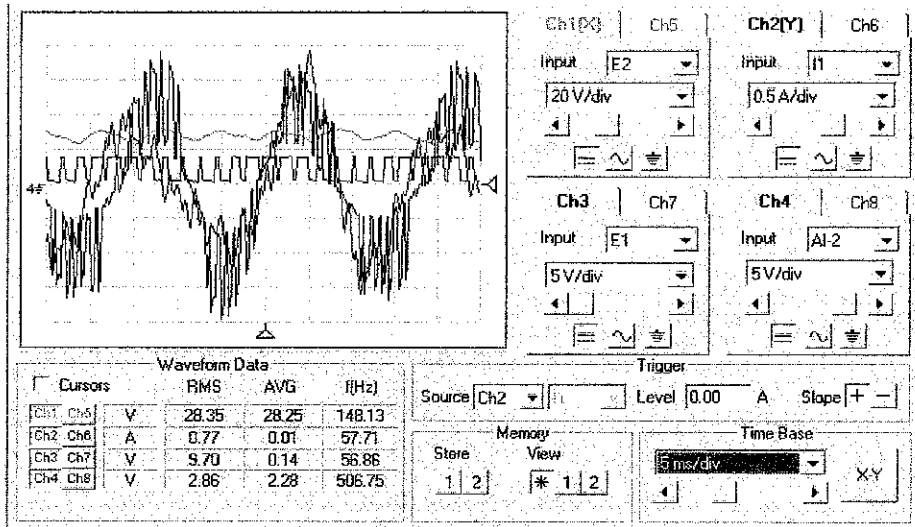


Figure 44 At 50% duty cycle

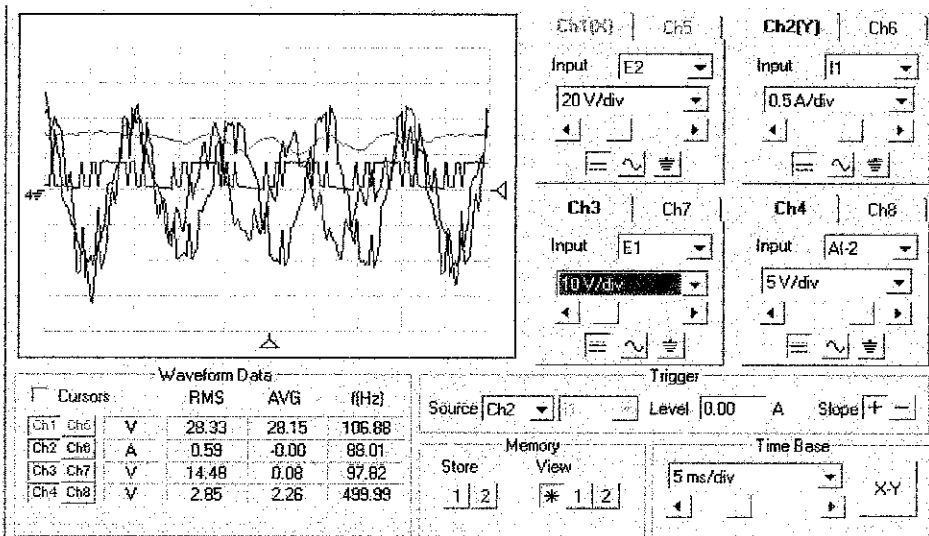


Figure 45 At 60% duty cycle

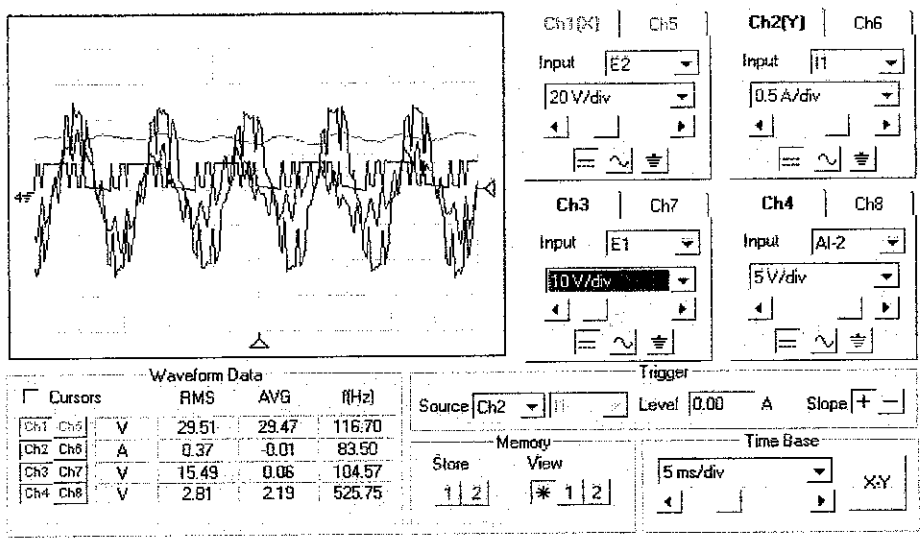


Figure 46 At 80% duty cycle

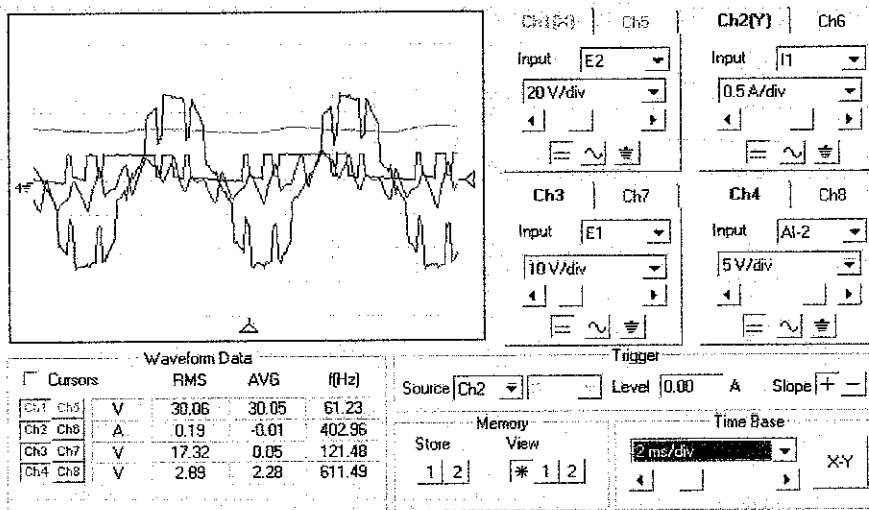


Figure 47 At 100% duty cycle

Table 2 Results of test

Duty Cycle	Input Voltage	Voltage line to line	Speed (rpm)
20%	30V	3.64V	390.3
30%	30V	5.38V	746.3
40%	30V	7.57V	1173.2
50%	30V	9.70V	1700.1
70%	30V	14.48V	310.25
80%	30V	15.49V	3646.7
100%	30V	17.32V	3805.1

The input voltage applied is 30 V but due to some losses the output display is less. The control unit provides the PWM pulses to the IGBT inverter module. The controller had established internally the triangular-wave and sine-wave signals to generate the PWM control signals.

The difference can be detected from the duty cycle where the frequencies of PWM control signals are changing. From reference, the frequency that supplied to motor must be at least 10 times more than the frequency inside motor. So if the output frequency from inverter is 600Hz, the exact motor frequency responds to this only 60Hz. To calculate the speed, equation 7 below will be used

$$N = \frac{120 f}{P}$$

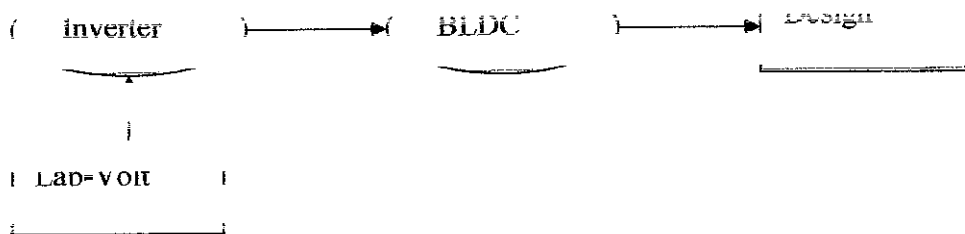


Figure 48 Test BLDC motor while Hall Sensor are attached to designed

Figure 48 describes how the test is conducted. The Hall Sensor signals from motor are passed on to the designed controller. The performance of the controller is explained in the following section.

4.3.4.1 Designed controller hardware

The designed controller circuit diagram is constructed based on the report of Microchip AN857. The circuit is easy to design and to be implemented.

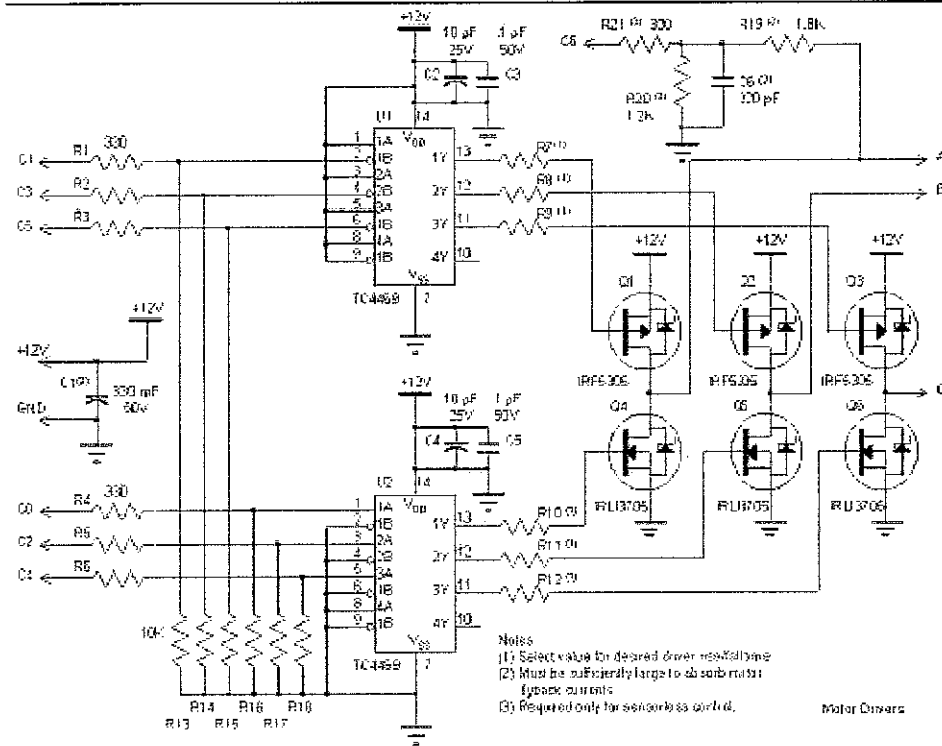


Figure 49 Circuit diagram-part1

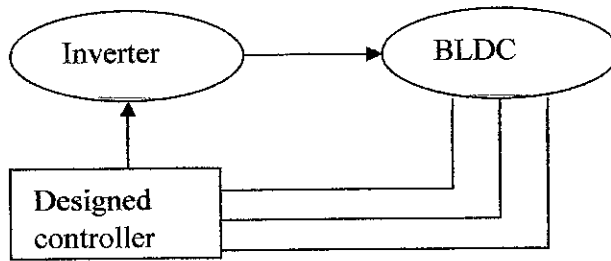


Figure 51 Test BLDC motor with designed controller alone

4.3.6 Correction to the controller

The reference of Microchip AN857 had some error that gives some flaw to the performance of the controller. Following is the correction to the controller circuit. From previous circuit we can see that there is fatal error where the Vcc is connected directly to ground. This will cause fault to the circuit where it will give overload reading at the power supply. The correction below shows that there will be diode with parallel capacitor and together with resistor between Vcc and ground connection. This will overcome the problems that arise. Due to time constraint, the author only

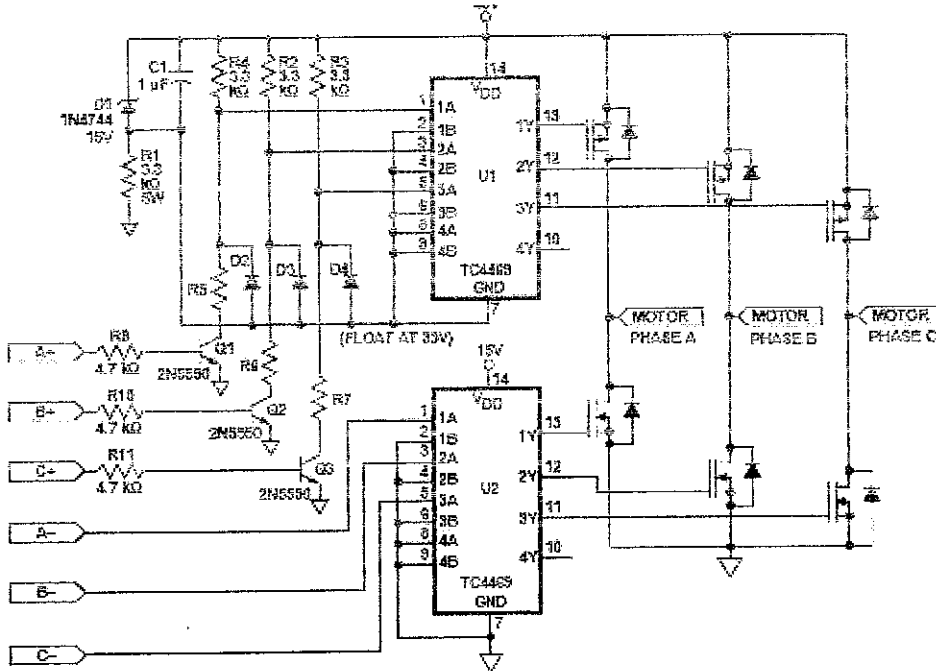


Figure 52 The correction of controller circuit

CHAPTER 5

CONCLUSION AND RECOMMENDATION

BLDC motor had started to take over in industrial applications due to its advantages over the conventional motor. This project presents one of BLDC motor application in every day life. The project task is to control the speed of a permanent magnet BLDC motor for air conditioning. The project is divided into two parts; simulation and design of power and control circuits.

The simulation of the drive system is performed with Matlab/Simulink and the circuitry part is being assembled in the Power Electronics laboratory. From the simulation results, the author observed the similarity between Sensorless BLDC motor and BLDC motor with Hall Sensors. The system of sensorless drive takes the value back EMF and translate it as a parameter to control the motor but a BLDC motor with sensor control takes the output of Hall Sensors. The simulation mainly depends on the reference speed and impedance together with the excitation voltage supply to the simulation block. This would directly give the correct output of actual speed from the BLDC motor.

In designing the power circuit, there are a few considerations that must be taken into consideration. The supply is from 12V battery which shows that this circuit is efficiently able to work inside an air conditioner of a car. The design starts with designing the boost converter provides an exact output of voltage. This voltage will then supplied to inverter that controlled by PWM controller. The PWM control signals play a main role to determine the output voltage of the inverter. To complete it the system will be attach to a BLDC motor. From here, the author learned that the output voltage is dependent on input voltage. To vary the output means to vary the DC input voltage.

The Lab-Volt modules had been the main components in designing hardware of the

system circuits. In control circuits, the PIC microcontroller is fully used to create control to system drive. The tests are done with two bases; first with Lab-Volt control unit and second with designed controller. Most of the electronics components are provided from Microchips Company. The BLDC motor is bought from LIN Engineering.

As the design of the circuit is made in open loop manner, a closed-loop control can be made for future work. Although there is some reference value added but there is no implementation of PID controller for the feedback loop. Due to time constraint, the tests could not be conducted on closed loop system. In closed loop method, the tasks will be quite the same with additional work to find the proportional, integral and derivative gain. Next is to fine tune each of the gains to get the best result.

REFERENCES

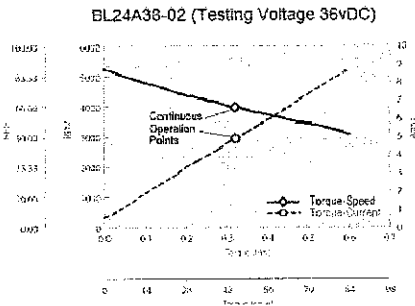
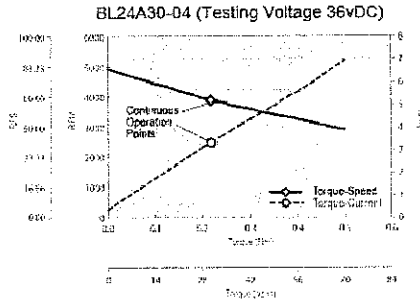
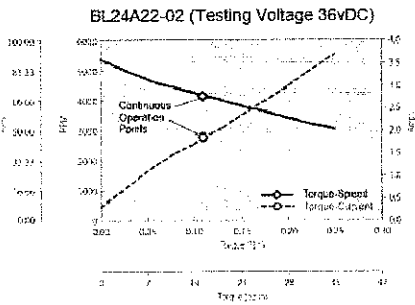
- [1] http://globaldensoproducts.com/cc/cacs/electrical_compressor.html
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- [13] <http://ww1.microchip.com/downloads/en/DeviceDoc/21425b.pdf>

**APPENDIX A
GANTT CHART**

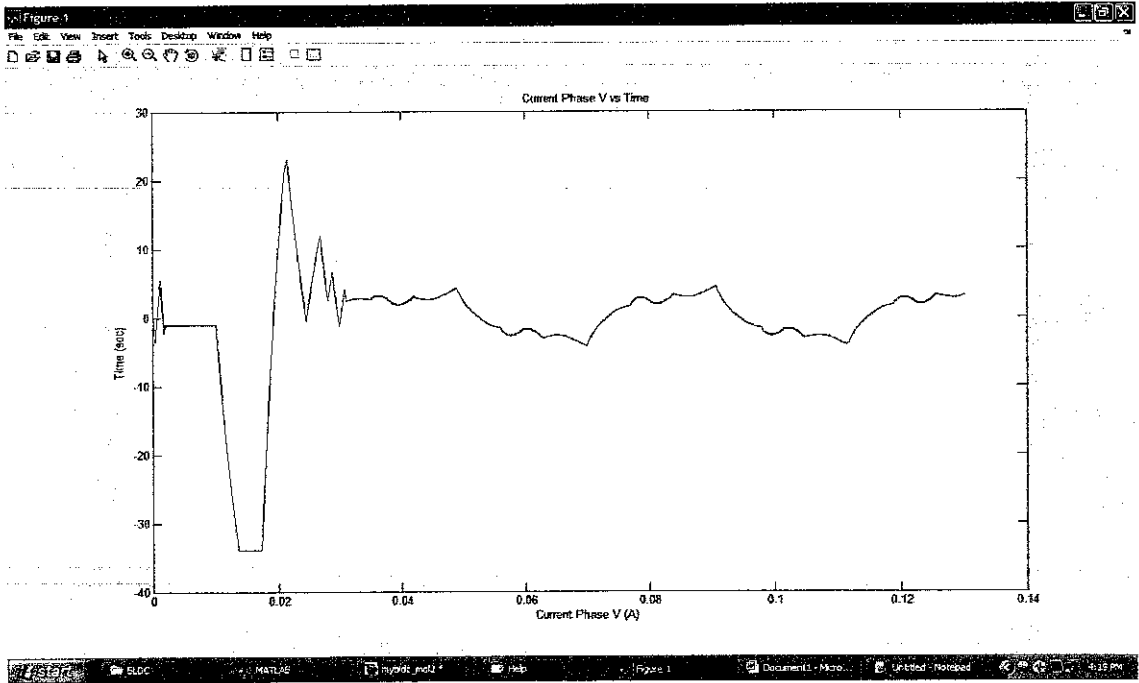
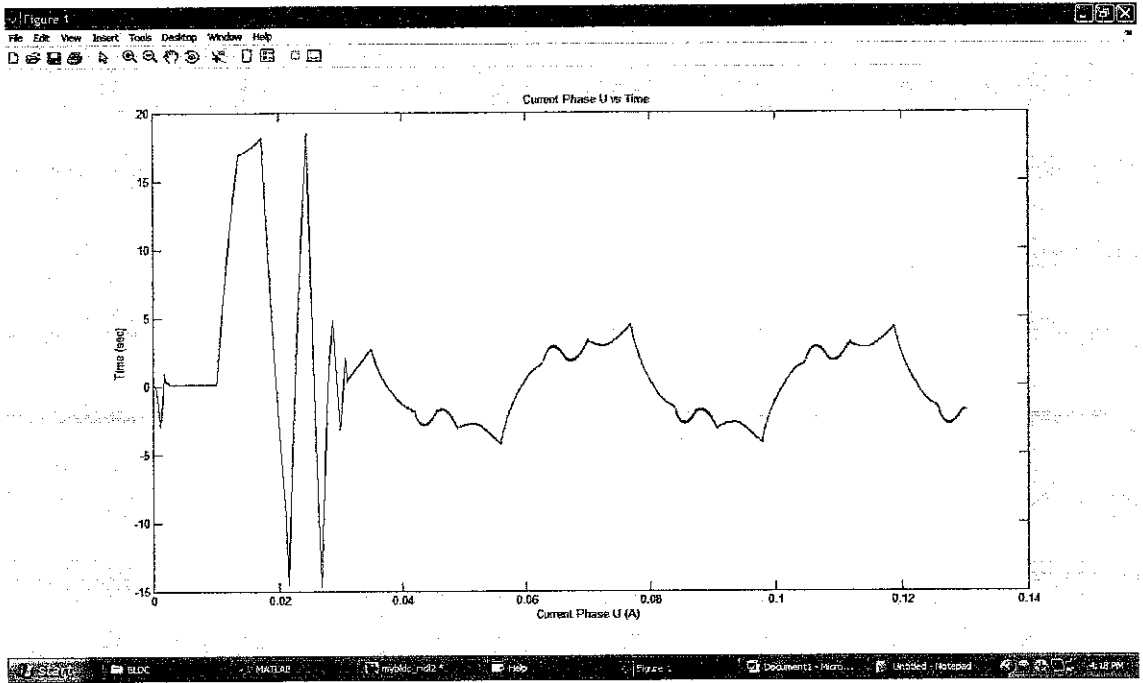
Activities		WEEKS													
		2	3	4	5	6	7	8	9	10	11	12	13	14	
1	Conduct literature review on project														
2	Configure the hardware specification.														
3	Simulate system inside MATLAB/SIMULINK														
4	Model of each component inside MATLAB (mathematical model)														
5	Using microcontroller to design a direct digital control for motor														
6	Fabricate system														
7	Documentation of project														

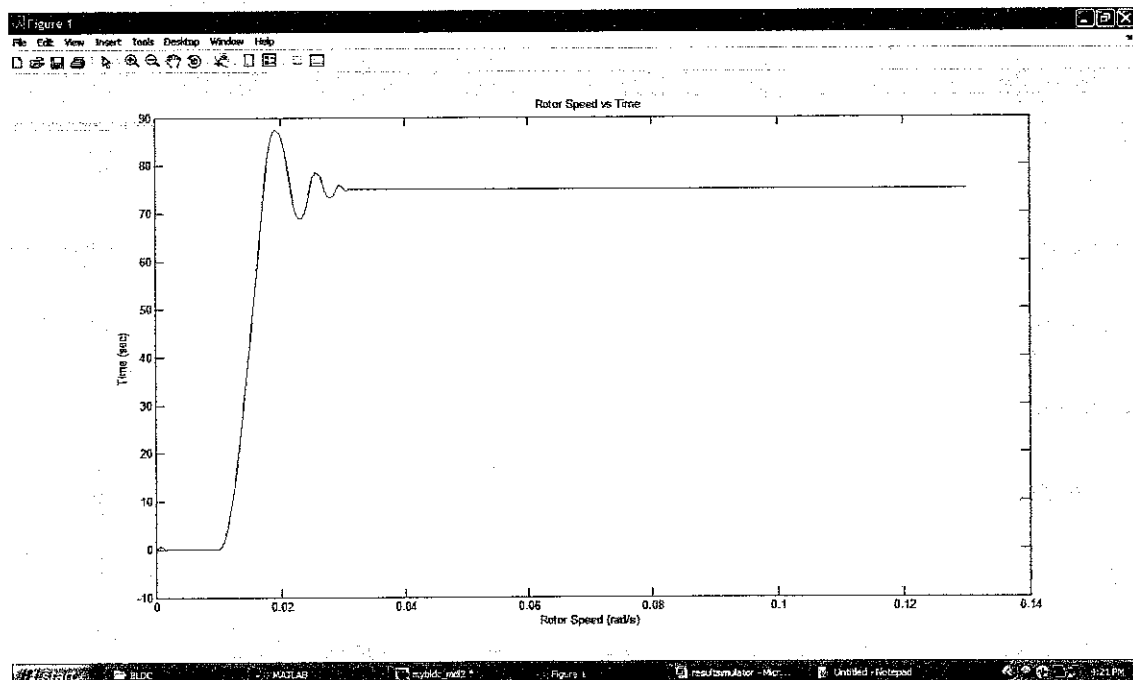
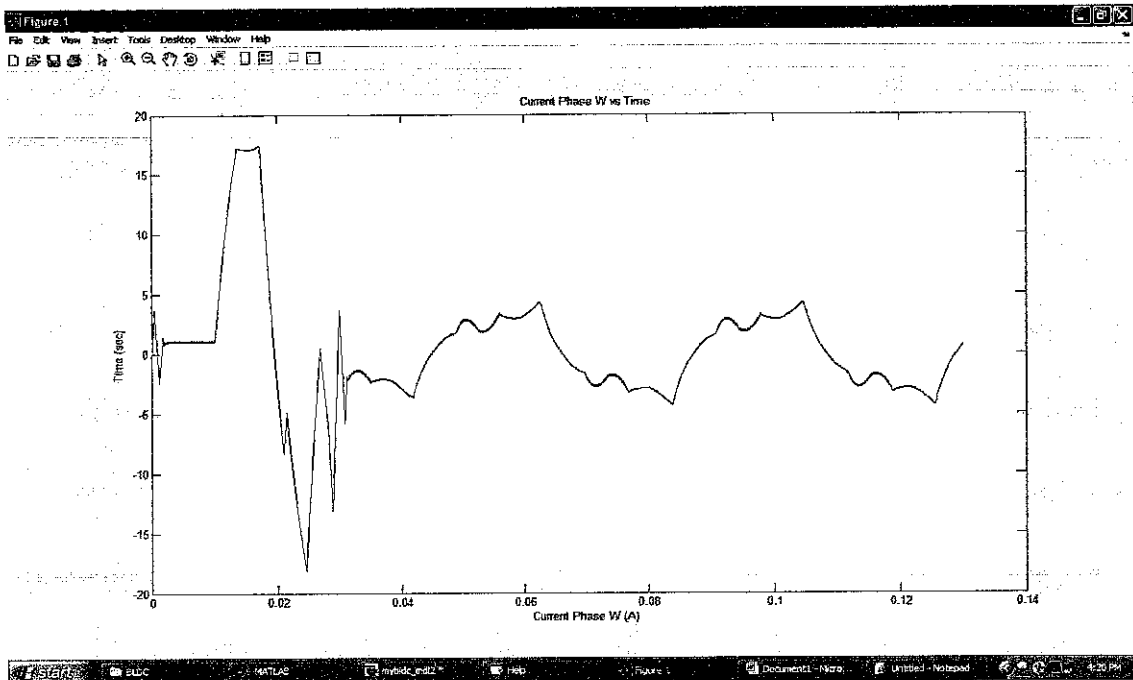
APPENDIX B BLDC MOTOR SPECIFICATION

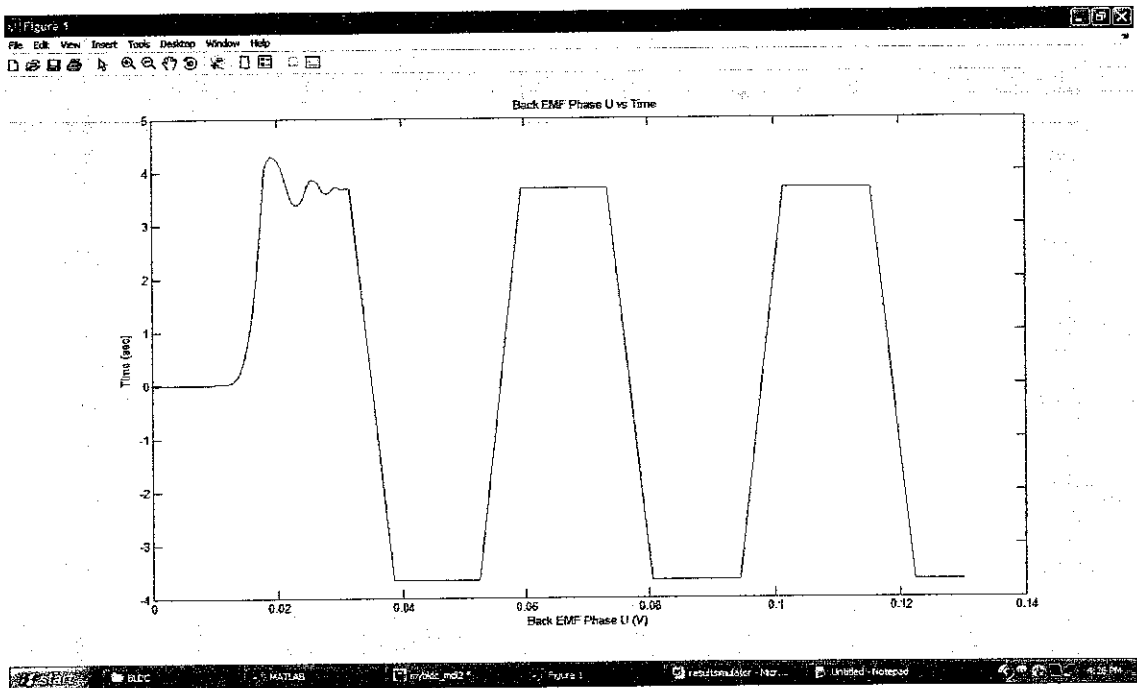
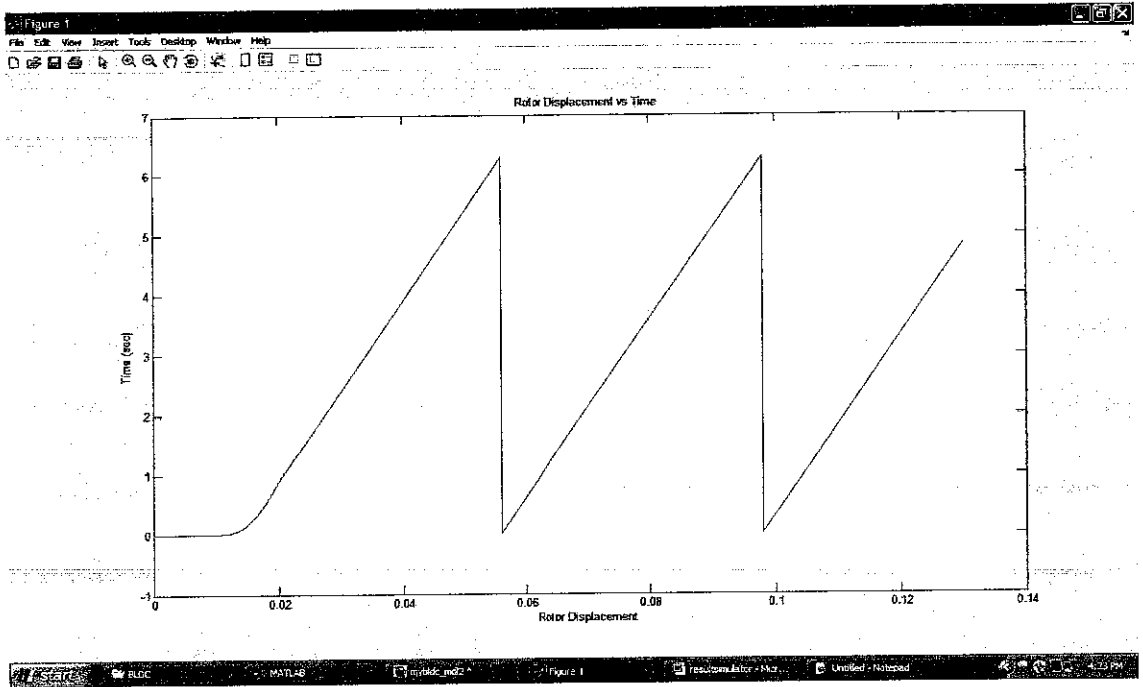
Model	BL24A22-02	BL24A30-04	BL24A38-02
Number of Poles	4	4	4
Number of Phase	3	3	3
Rated Voltage (VDC)	36	36	36
Rated Speed (RPM)	4000	4000	4000
Rated Torque (Oz-in)	15.58	31.15	45.32
Power (W)	46	92	133
Peak Torque (Oz-in)	55.23	99.13	141.61
Peak Current (A)	6.8	14.5	17.6
Torque Constant (Oz-in/A)	8.92	8.92	8.92
Back E.M.F. (V/KRPM)	6.6	6.6	6.6
Rotor Inertia (oz.in²)	0.41	0.65	0.94
Body Length (mm)	55	75	95
Body Length (in)-Dimension A	2.17	2.95	3.74
Mass (Kg)	0.5	0.75	1

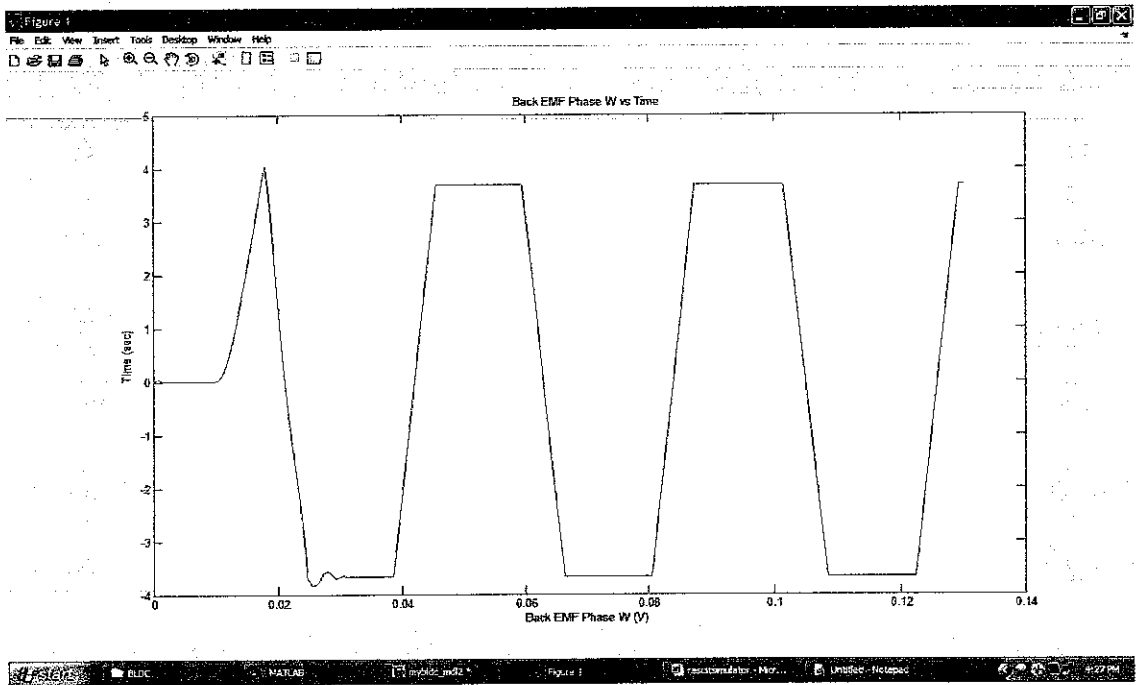
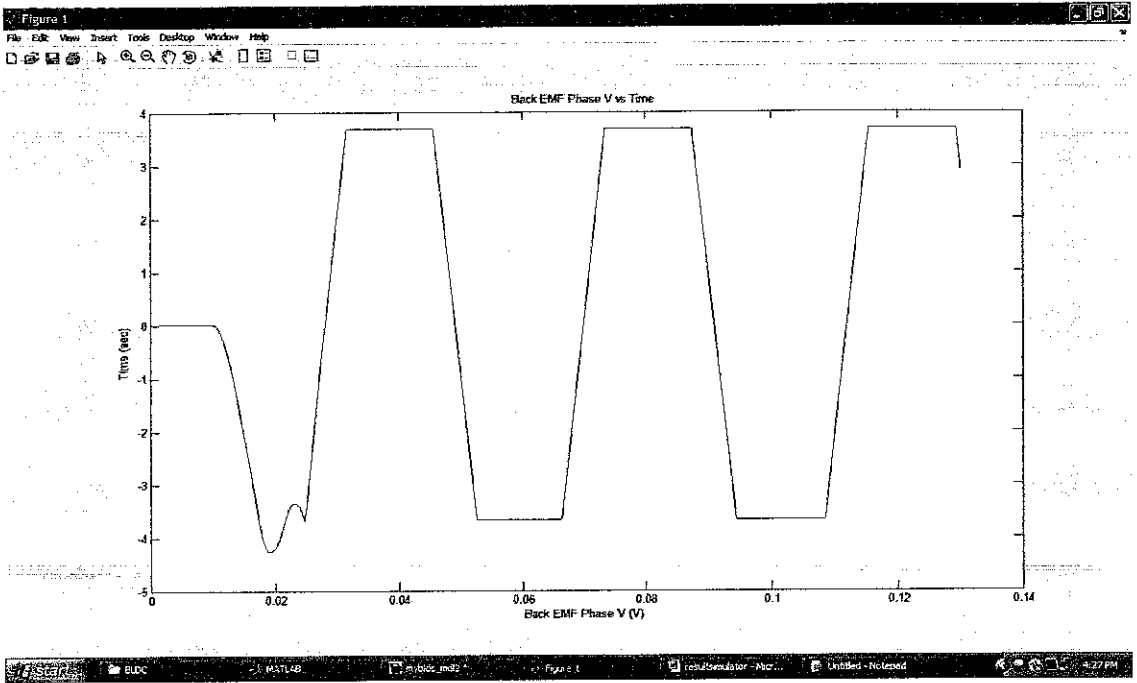


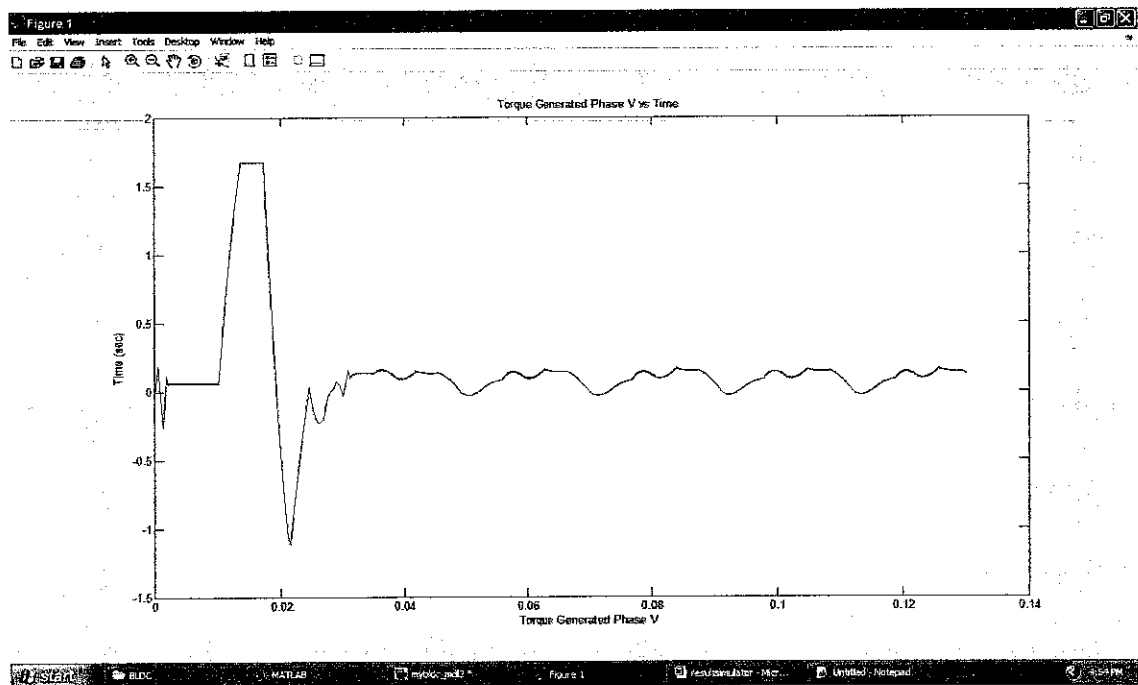
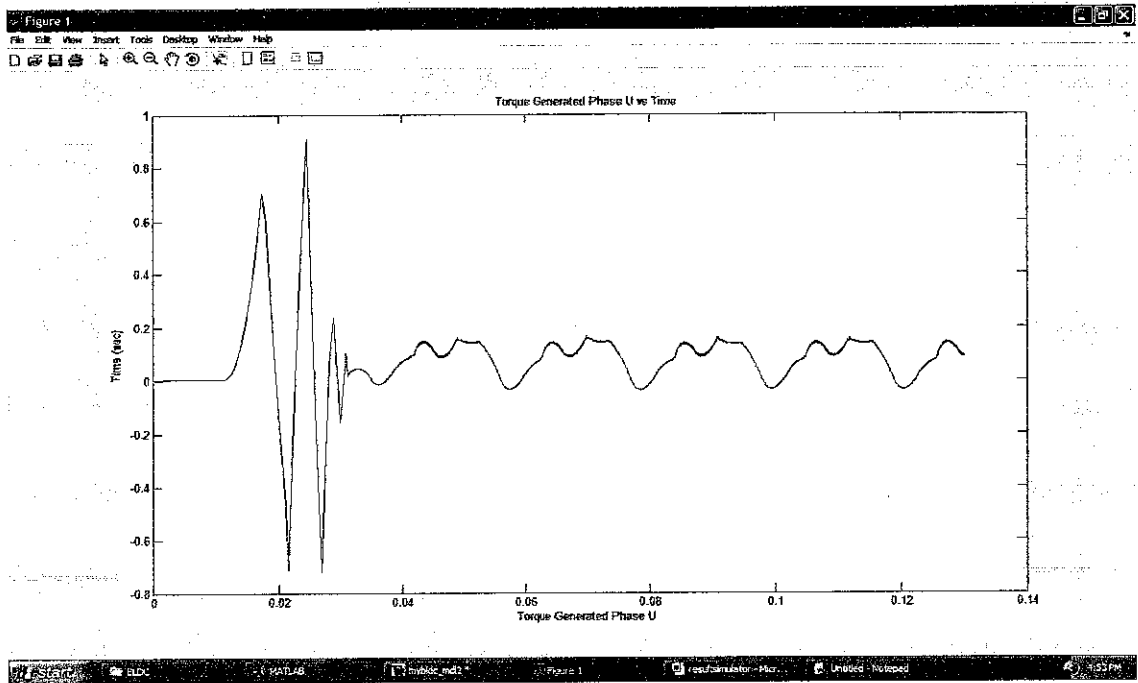
APPENDIX C RESULTS OF SIMULATION

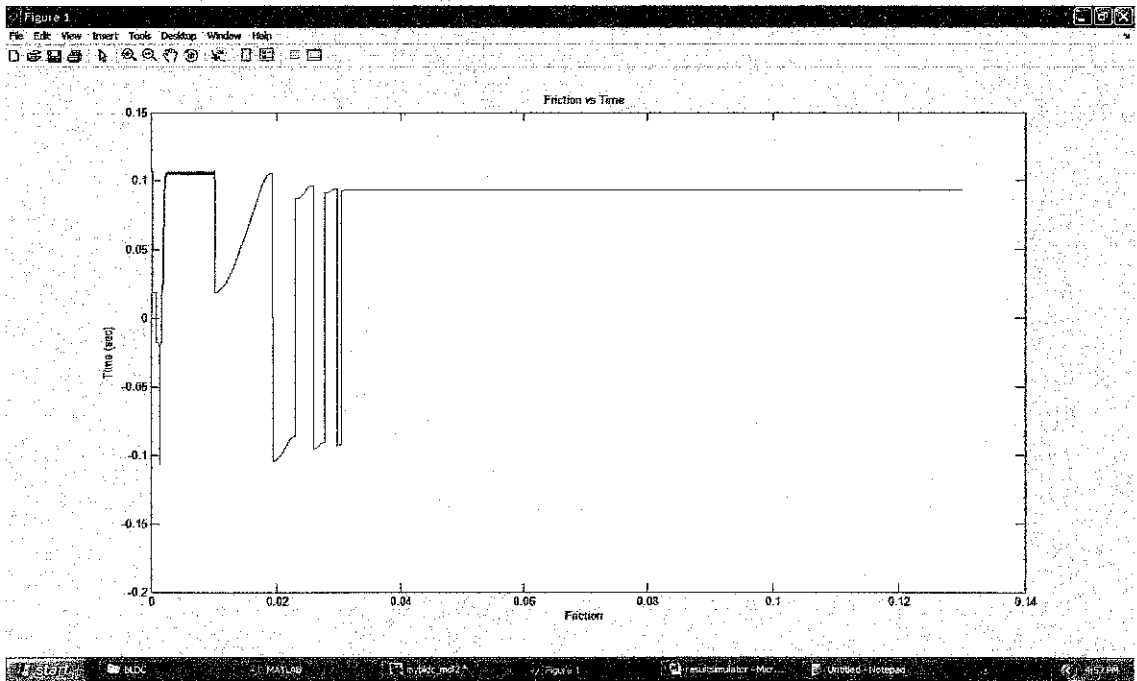
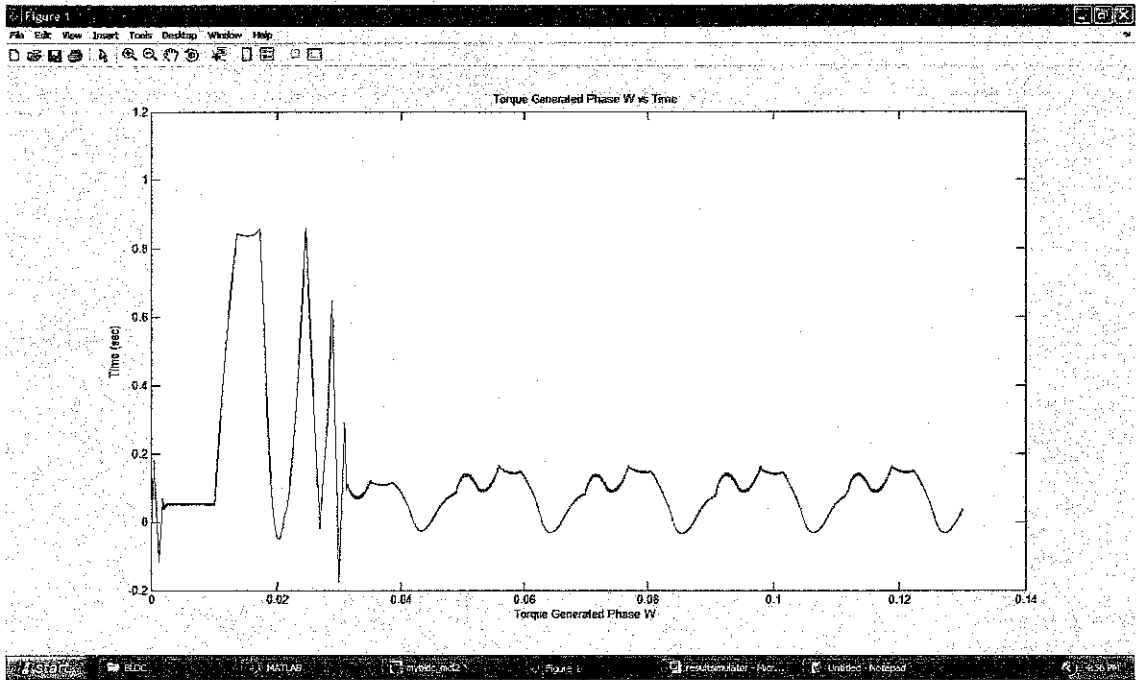


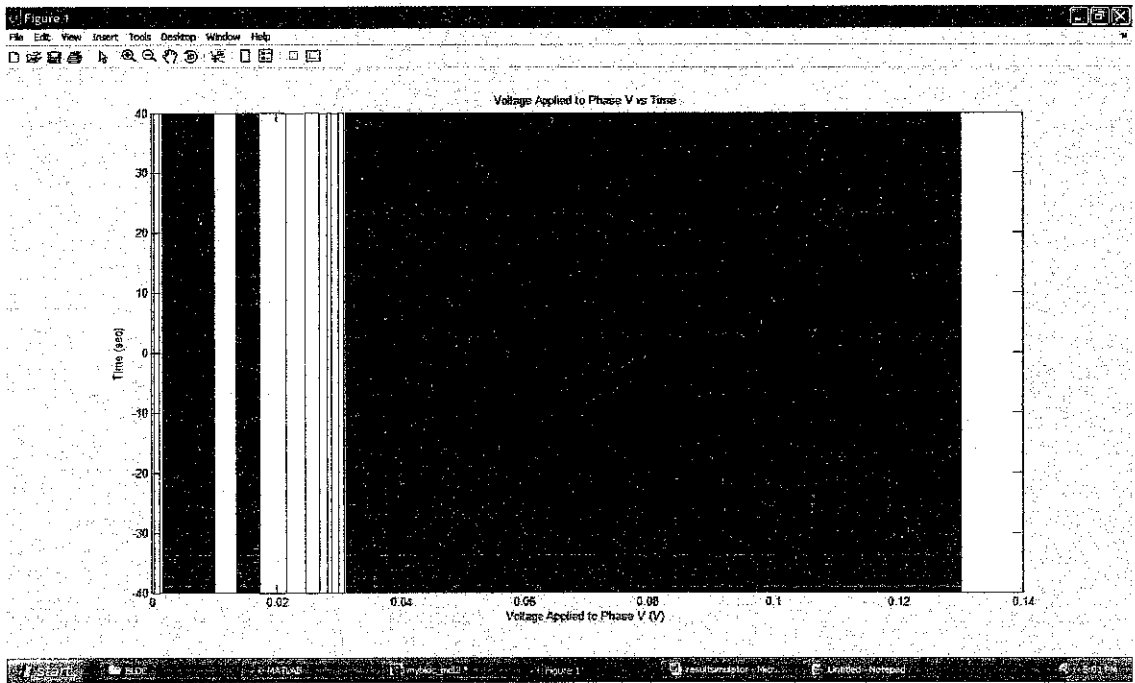
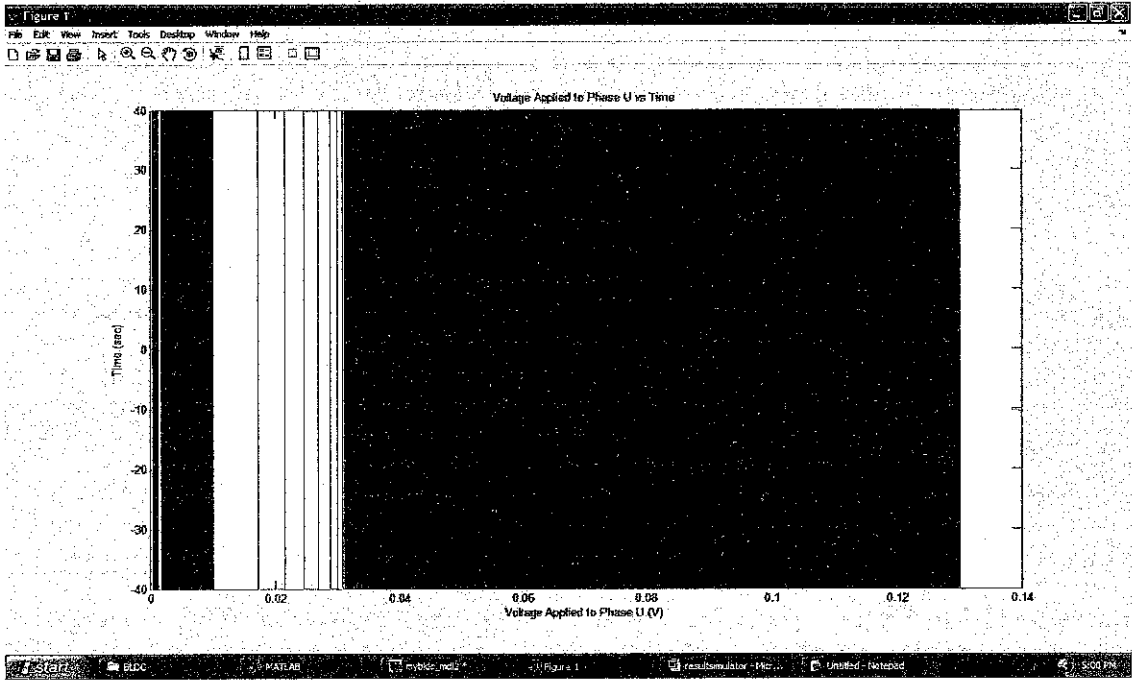


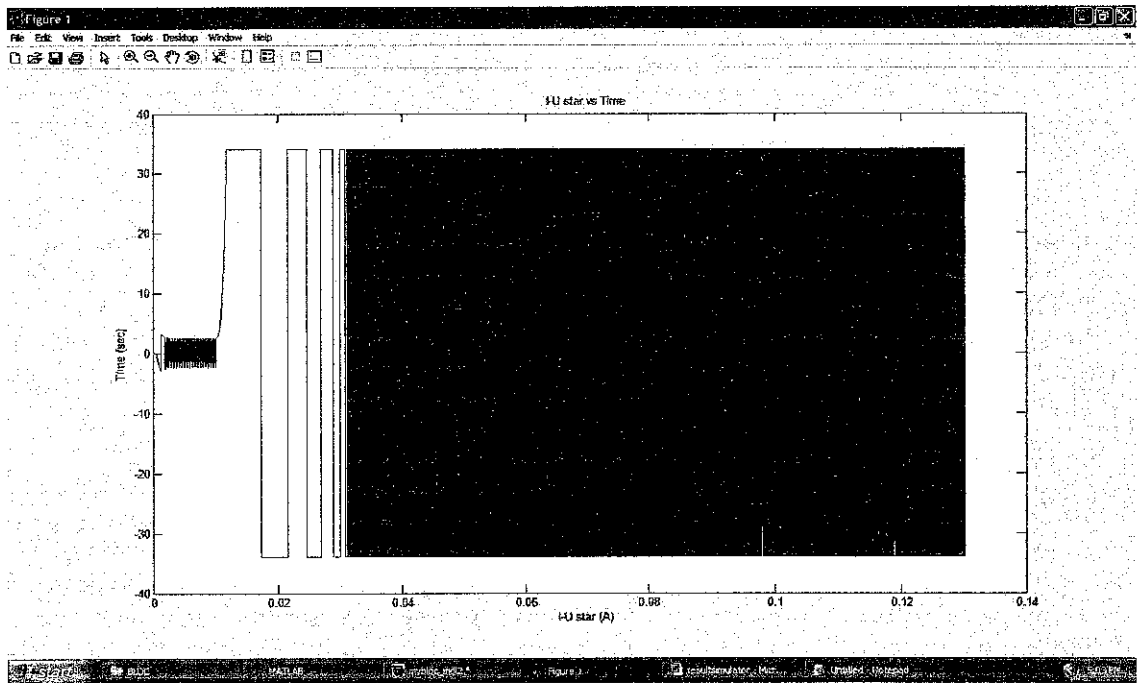
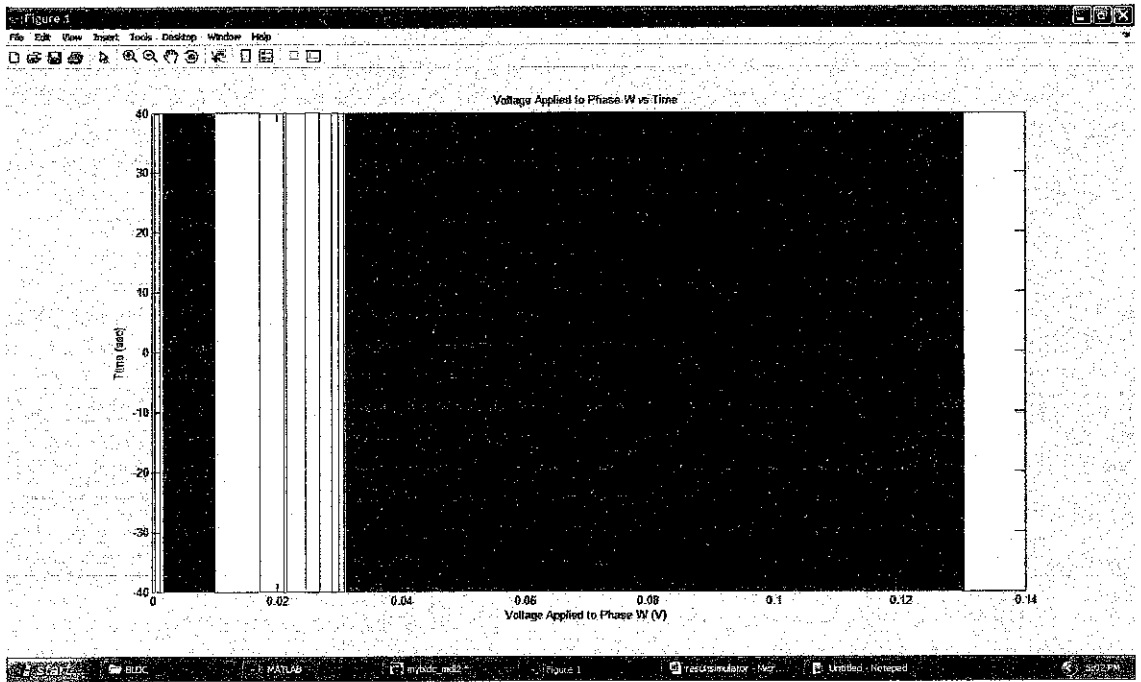


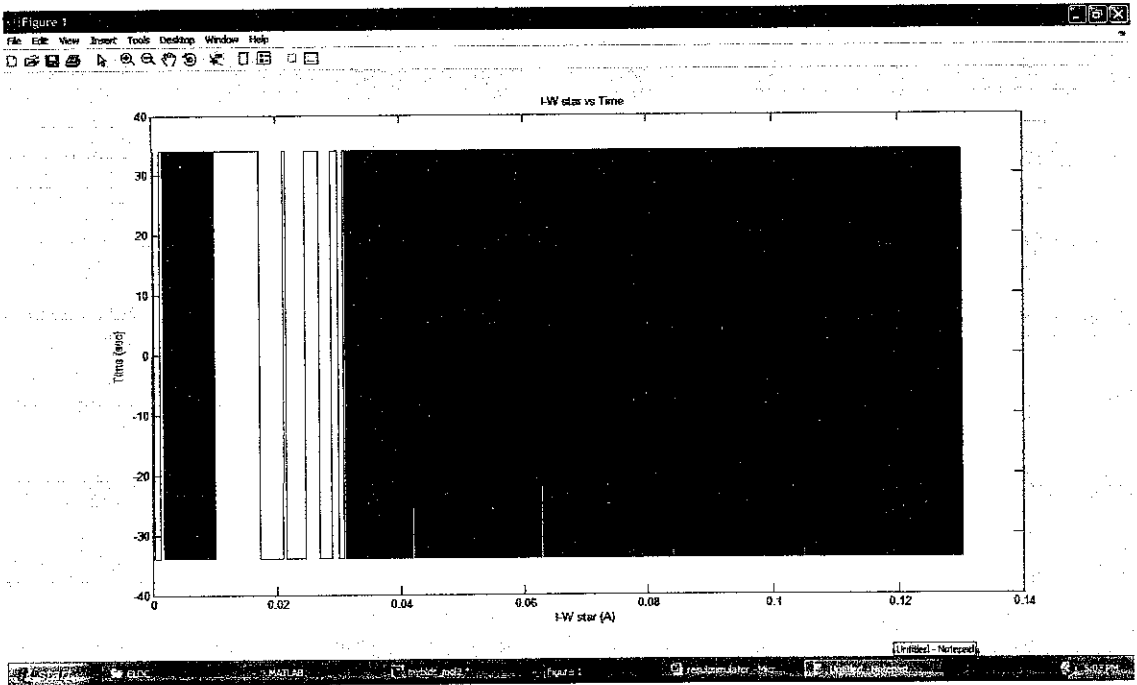
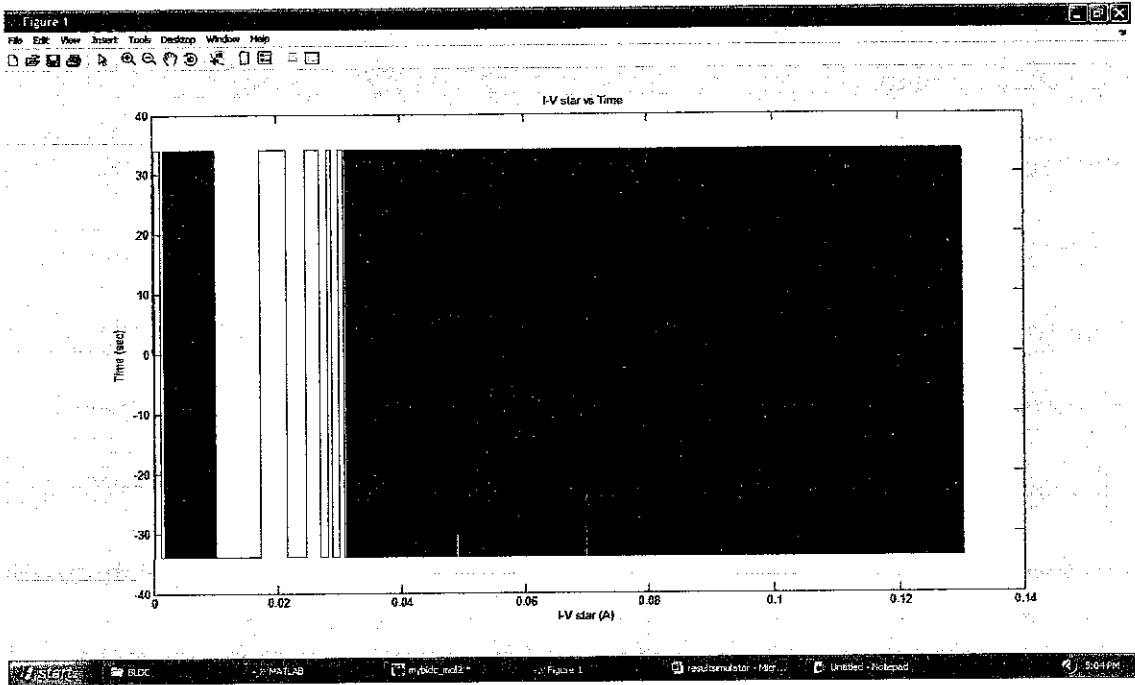


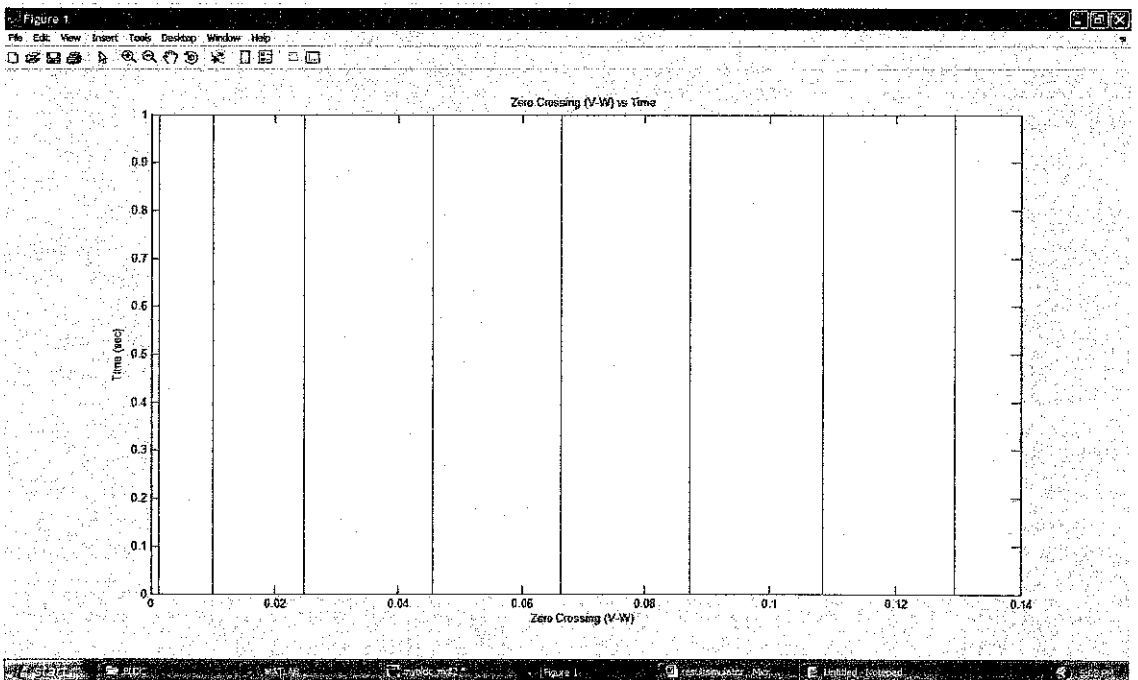
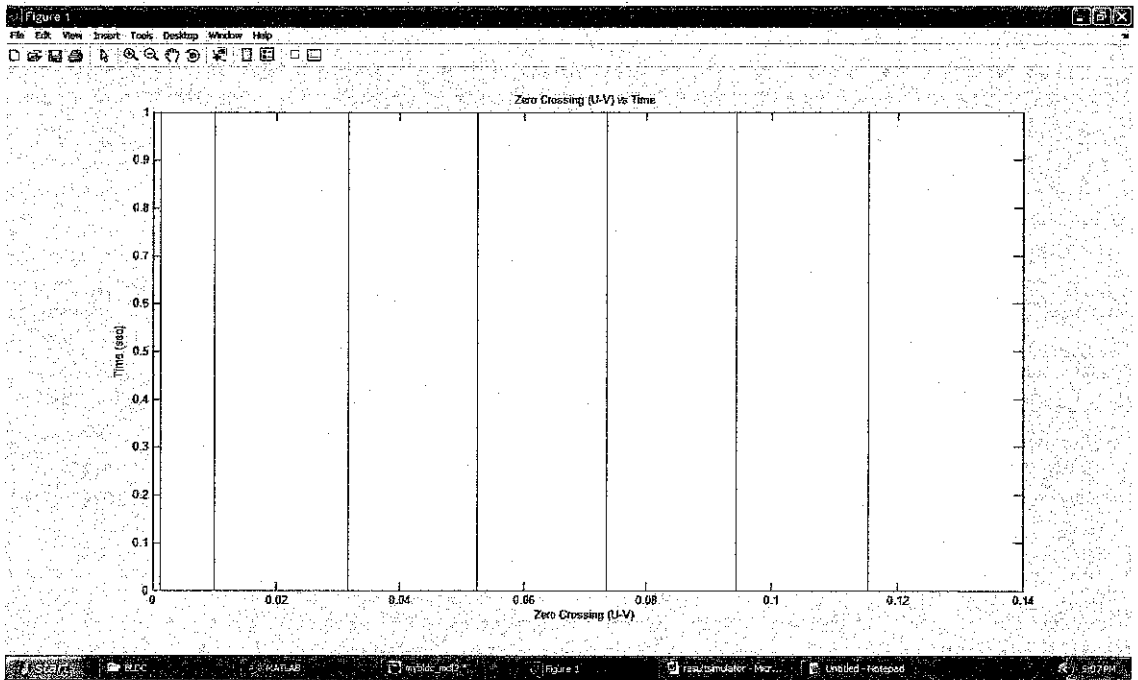


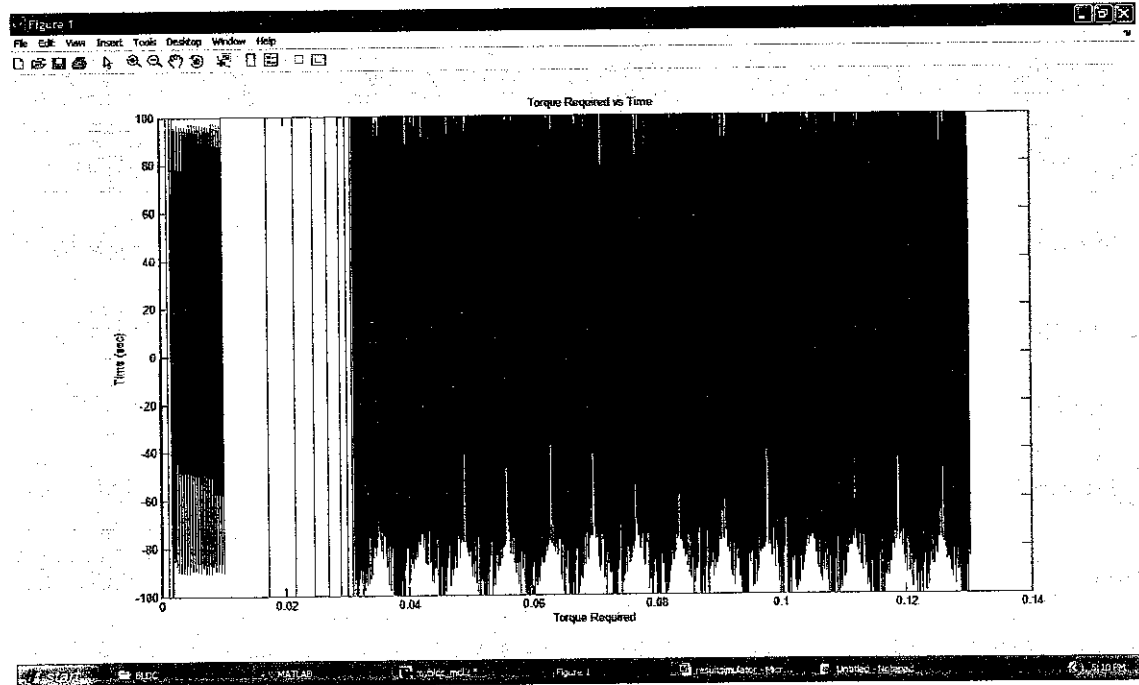
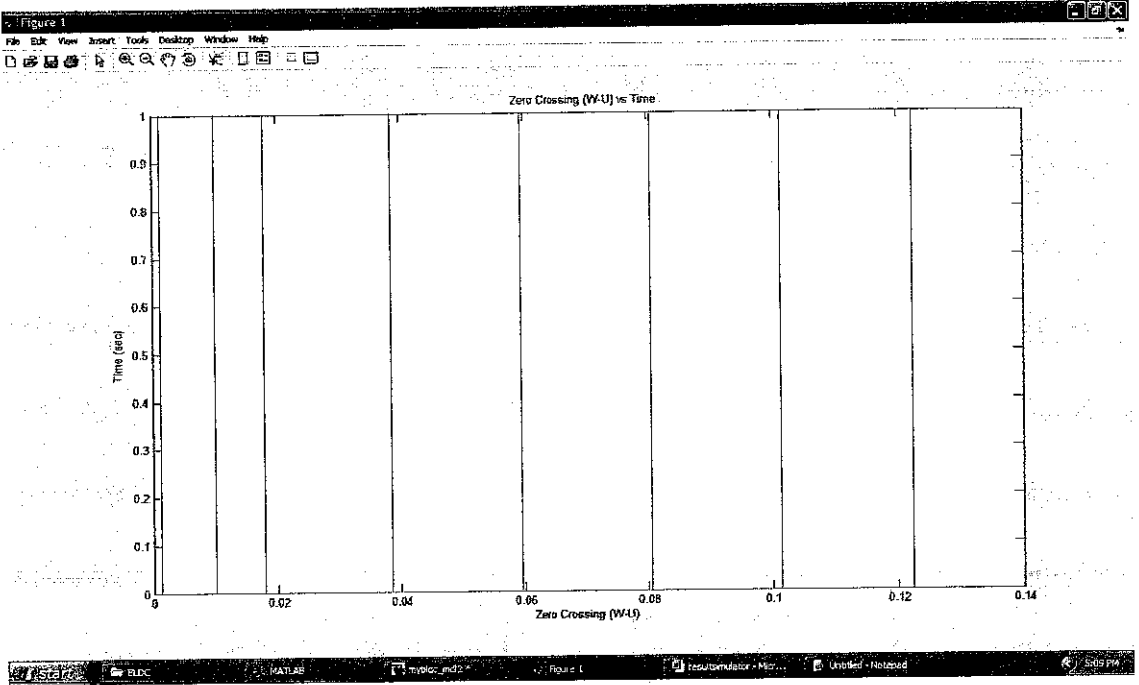


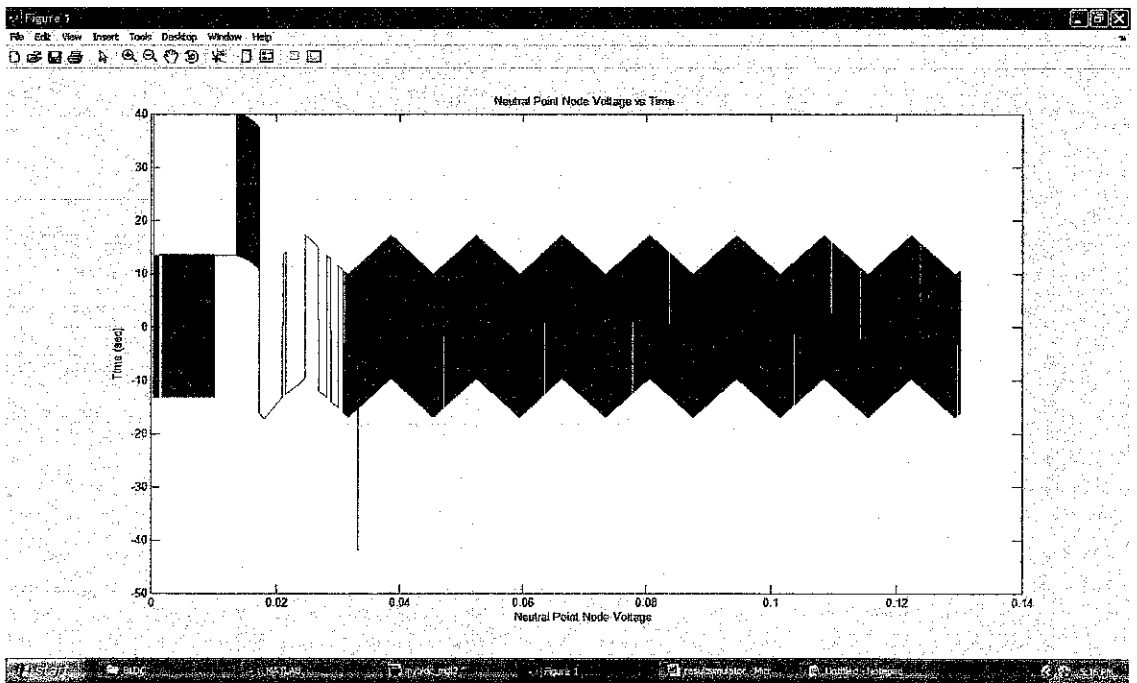
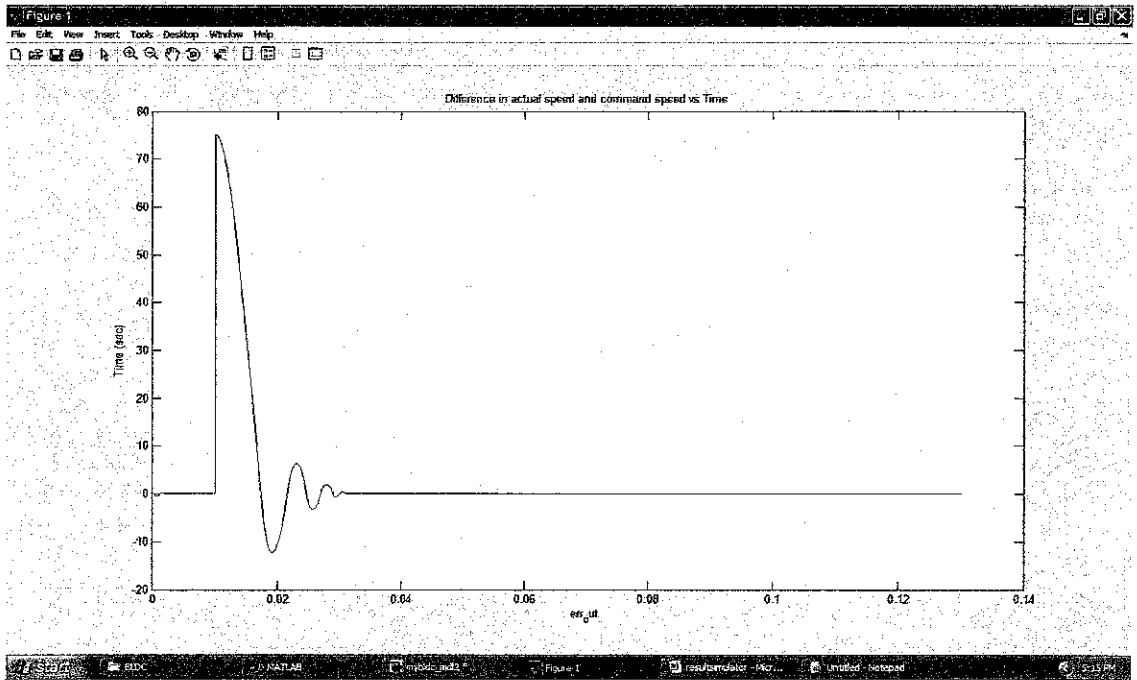












APPENDIX D CODING FOR MICROCONTROLLER

```

;*****
; *
; Filename: sensed.asm *
; Date: 11 Feb. 2002 *
; File Version: 1.0 *
; *
; Author: W.R. Brown *
; Company: Microchip Technology Incorporated *
; *
; *
;*****
; *
; Files required: p16f877.inc *
; *
; *
; *
;*****
; *
; Notes: Sensed brushless motor control Main loop uses 3-bit *
; sensor input as index for drive word output. PWM based on *
; Timer0 controls average motor voltage. PWM level is determined *
; PWM level is determined from ADC reading of potentiometer. *
; *
;*****
list p=16f877 ; list directive to define processor
#include <p16f877.inc> ; processor specific variable definitions
__CONFIG _CP_OFF & _WDT_OFF & _BODEN_ON & _PWRTE_ON & _HS_OSC & _WRT_ENABLE_OFF &
_LVP_ON &
_DEBUG_OFF & _CPD_OFF
;*****
; *
; * Define variable storage
; *
CBLOCK 0x20
ADC ; PWM threshold is ADC result
lastSensor ; last read motor sensor data
DriveWord ; six bit motor drive data
ENDC

;*****
; *
; * Define I/O
; *
#define OffMask B'11010101'
#define DrivePort PORTC
#define DrivePortTris TRISC
#define SensorMask B'00000111'
#define SensorPort PORTE
#define DirectionBit PORTA,1
;*****
org 0x000 ; startup vector
nop ; required for ICD operation
clrf PCLATH ; ensure page bits are cleared
goto Initialize ; go to beginning of program
ORG 0x004 ; interrupt vector location
retfie ; return from interrupt
;*****
; *
; * Initialize I/O ports and peripherals
; *
Initialize
clrf DrivePort ; all drivers off
banksel TRISA
; setup I/O
clrf DrivePortTris ; set motor drivers as outputs
movlw B'00000111' ; A/D on RA0, Direction on RA1, Motor sensors on RE<2:0>
movwf TRISA ;
; setup Timer0
movlw B'11010000' ; Timer0: Fosc, 1:2

```

```

movwf OPTION_REG
; Setup ADC (bank1)
movlw B'00001110' ; ADC left justified, AN0 only
movwf ADCON1
banksel ADCON0
; setup ADC (bank0)
movlw B'11000001' ; ADC clock from int RC, AN0, ADC on
movwf ADCON0
bsf ADCON0,GO ; start ADC
clrf LastSensor ; initialize last sensor reading
call Commutate ; determine present motor position
clrf ADC ; start speed control threshold at zero until first ADC
reading
;*****
;*
;* Main control loop
;*
Loop
call ReadADC ; get the speed control from the ADC
incfsz ADC,w ; if ADC is 0xFF we're at full speed - skip timer add
goto PWM ; add Timer0 to ADC for PWM
movf DriveWord,w ; force on condition
goto Drive ; continue
PWM
movf ADC,w ; restore ADC reading
addwf TMR0,w ; add it to current Timer0
movf DriveWord,w ; restore commutation drive data
btfss STATUS,C ; test if ADC + Timer0 resulted in carry
andlw OffMask ; no carry - suppress high drivers
Drive
movwf DrivePort ; enable motor drivers
call Commutate ; test for commutation change
goto Loop ; repeat loop
ReadADC
;*****
;*
;* If the ADC is ready then read the speed control potentiometer
;* and start the next reading
;*
btfsc ADCON0,NOT_DONE ; is ADC ready?
return ; no - return
movf ADRESH,w ; get ADC result
bsf ADCON0,GO ; restart ADC
movwf ADC ; save result in speed control threshold
return ;
;*****
;*
;* Read the sensor inputs and if a change is sensed then get the
;* corresponding drive word from the drive table
;*
Commutate
movlw SensorMask ; retain only the sensor bits
andwf SensorPort,w ; get sensor data
xorwf LastSensor,w ; test if motion sensed
btfsc STATUS,Z ; zero if no change
return ; no change - back to the PWM loop
xorwf LastSensor,f ; replace last sensor data with current
btfss DirectionBit ; test direction bit
goto FwdCom ; bit is zero - do forward commutation
; reverse commutation
movlw HIGH RevTable ; get MS byte of table
movwf PCLATH ; prepare for computed GOTO
movlw LOW RevTable ; get LS byte of table
goto Com2
FwdCom ; forward commutation
movlw HIGH FwdTable ; get MS byte of table
movwf PCLATH ; prepare for computed GOTO
movlw LOW FwdTable ; get LS byte of table
Com2
addwf LastSensor,w ; add sensor offset
btfsc STATUS,C ; page change in table?
incf PCLATH,f ; yes - adjust MS byte
call GetDrive ; get drive word from table
movwf DriveWord ; save as current drive word
return
GetDrive
movwf PCL

```

```

;*****
;*
;* The drive tables are built based on the following assumptions:
;* 1) There are six drivers in three pairs of two
;* 2) Each driver pair consists of a high side (+V to motor) and low side (motor to
ground) drive
;* 3) A 1 in the drive word will turn the corresponding driver on
;* 4) The three driver pairs correspond to the three motor windings: A, B and C
;* 5) Winding A is driven by bits <1> and <0> where <1> is A's high side drive
;* 6) Winding B is driven by bits <3> and <2> where <3> is B's high side drive
;* 7) Winding C is driven by bits <5> and <4> where <5> is C's high side drive
;* 8) Three sensor bits constitute the address offset to the drive table
;* 9) A sensor bit transitions from a 0 to 1 at the moment that the corresponding
;* winding's high side forward drive begins.
;* 10) Sensor bit <0> corresponds to winding A
;* 11) Sensor bit <1> corresponds to winding B
;* 12) Sensor bit <2> corresponds to winding C
;*
FwdTable
retlw B'00000000' ; invalid
retlw B'00010010' ; phase 6
retlw B'00001001' ; phase 4
retlw B'00011000' ; phase 5
retlw B'00100100' ; phase 2
retlw B'00000110' ; phase 1
retlw B'00100001' ; phase 3
retlw B'00000000' ; invalid
RevTable
retlw B'00000000' ; invalid
retlw B'00100001' ; phase /6
retlw B'00000110' ; phase /4
retlw B'00100100' ; phase /5
retlw B'00011000' ; phase /2
retlw B'00001001' ; phase /1
retlw B'00010010' ; phase /3
retlw B'00000000' ; invalid
END ; directive 'end of progra

```

CMOS LOGIC-INPUT CMOS QUAD DRIVERS

FEATURES

- High Peak Output Current 1.2A
- Wide Operating Range 4.5 to 18V
- Symmetrical Rise and Fall Times 25nsec
- Short, Equal Delay Times 75nsec
- Latchproof! Withstands 500mA Inductive Kickback
- 3 Input Logic Choices
 - AND / NAND / AND + Inv
- 1kV ESD Protection on All Pins

APPLICATIONS

- General-Purpose CMOS Logic Buffer
- Driving All Four MOSFETs in an H-Bridge
- Direct Small Motor Driver
- Relay or Peripheral Drivers
- LCD Driver
- Pin-Switching Network Driver

GENERAL DESCRIPTION

The TC446X family of four-output CMOS buffer/drivers are an expansion from our earlier single- and dual-output drivers. Each driver has been equipped with a two-input logic gate for added flexibility.

The TC446X drivers can source up to 250 mA into loads referenced to ground. Heavily loaded clock lines, coaxial cables, and piezoelectric transducers can all be easily driven with the 446X series drivers. The only limitation on loading is that total power dissipation in the IC must be kept within the power dissipation limits of the package.

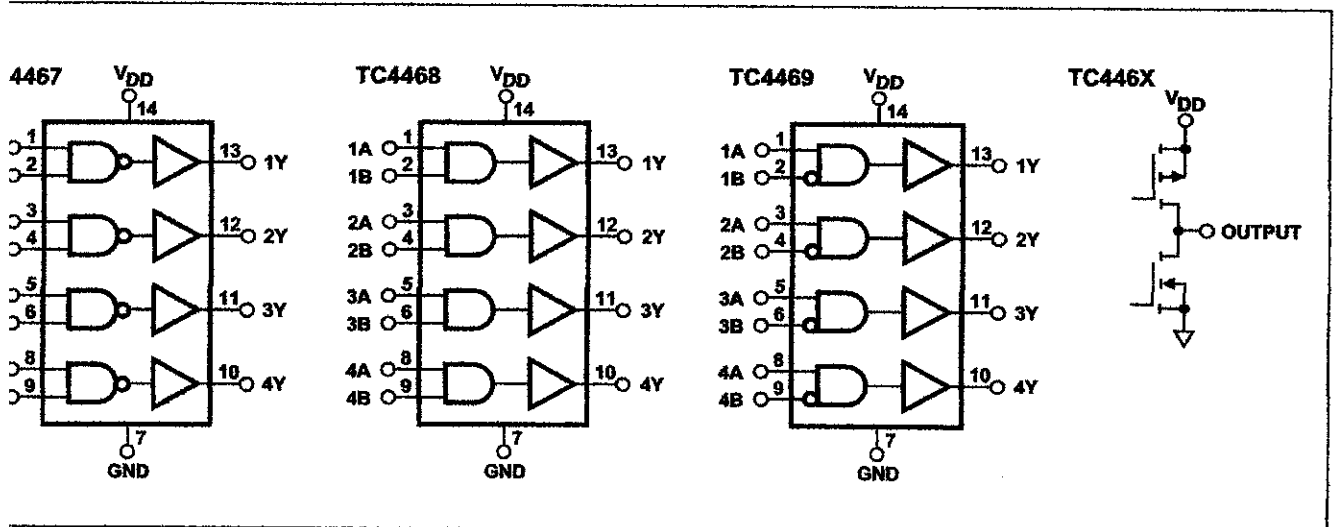
The TC446X series will not latch under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking (either polarity) occurs on the ground line. They can accept up to half an amp of inductive kickback current (either polarity) into their outputs without damage or logic upset. In addition, all terminals are protected against ESD to at least 2000V.

ORDERING INFORMATION

Part No.	Package	Temp. Range
TC446xCOE	16-Pin SOIC (Wide)	0° to +70°C
TC446xCPD	14-Pin Plastic DIP	0° to +70°C
TC446xEJD	14-Pin CerDIP	-40° to +85°C
TC446xMJD	14-Pin CerDIP	-55° to +125°C

*A digit must be added in the "x" position to define the device input configuration: TC446x — 7 NAND
8 AND
9 AND with INV

IC DIAGRAMS



LOGIC-INPUT CMOS QUAD DRIVERS

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ABSOLUTE MAXIMUM RATINGS*

V _{DD} Voltage	+20V
V _{IN} Voltage	(GND – 5V) to (V _{DD} + 0.3V)
Maximum Junction Temperature	+150°C
Operating Storage Temperature	– 65° to +150°C
Maximum Lead Temperature (Soldering, 10 sec)	+300°C
Operating Ambient Temperature Range	0° to +70°C
Device Storage Temperature	– 40° to +85°C
Device Storage Temperature	– 55° to +125°C
Maximum Power Dissipation (T _A ≤ 70°C)	
14-Pin CerDIP	840mW
14-Pin Plastic DIP	800mW
16-Pin Wide SOIC	760mW

Package Thermal Resistance

14-Pin CerDIP	R _{θJA}	100°C/W
	R _{θJC}	23°C/W
14-Pin Plastic DIP	R _{θJA}	80°C/W
	R _{θJC}	35°C/W
16-Pin Wide SOIC	R _{θJA}	95°C/W
	R _{θJC}	28°C/W

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

OPERATIONAL CHARACTERISTICS: Measured at T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
	Logic 1, High Input Voltage	Note 3	2.4	—	V _{DD}	V
	Logic 0, Low Input Voltage	Note 3	0	—	0.8	V
	Input Current	0V ≤ V _{IN} ≤ V _{DD}	– 1	—	1	μA
	Output Voltage					
	High Output Voltage	I _{LOAD} = 100μA (Note 1)	V _{DD} – 0.025	—	—	V
	Low Output Voltage	I _{LOAD} = 10mA (Note 1)	—	—	0.15	V
	Output Resistance	I _{OUT} = 10mA, V _{DD} = 18V	—	10	15	Ω
	Peak Output Current		—	1.2	—	A
	Continuous Output Current	Single Output Total Package	—	—	300 500	mA
	Latch-Up Protection Withstand Reverse Current	4.5V ≤ V _{DD} ≤ 16V	500	—	—	mA
	Timing Time					
	Rise Time	Figure 1	—	15	25	nsec
	Fall Time	Figure 1	—	15	25	nsec
	Delay Time	Figure 1	—	40	75	nsec
	Delay Time	Figure 1	—	40	75	nsec
	Supply					
	Power Supply Current		—	1.5	4	mA
	Power Supply Voltage	Note 2	4.5	—	18	V

TRUTH TABLE

Inputs	TC4467 NAND				TC4468 AND				TC4469 AND/INV			
A	H	H	L	L	H	H	L	L	H	H	L	L
B	H	L	H	L	H	L	H	L	H	L	H	L
JTS TC446X	L	H	H	H	H	L	L	L	L	H	L	L

H = High, L = Low

GIC-INPUT CMOS QUAD DRIVERS

TC4467
TC4468
TC4469

ELECTRICAL CHARACTERISTICS: Measured throughout operating temperature range with $4.5V \leq V_{DD} \leq 18V$, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Logic 1, High Input Voltage	(Note 3)	2.4	—	—	V
V_{IL}	Logic 0, Low Input Voltage	(Note 3)	—	—	0.8	V
I_{IN}	Input Current	$0V \leq V_{IN} \leq V_{DD}$	-10	—	10	μA

V_{OH}	High Output Voltage	$I_{LOAD} = 100\mu A$ (Note 1)	$V_{DD} - 0.025$	—	—	V
V_{OL}	Low Output Voltage	$I_{LOAD} = 10mA$ (Note 1)	—	—	0.30	V
R_{OUT}	Output Resistance	$I_{OUT} = 10mA, V_{DD} = 18V$	—	20	30	Ω
I_{OC}	Peak Output Current		—	1.2	—	A
I_{LUP}	Latch-Up Protection Withstand Reverse Current	$4.5V \leq V_{DD} \leq 16V$	500	—	—	mA

Switching Time

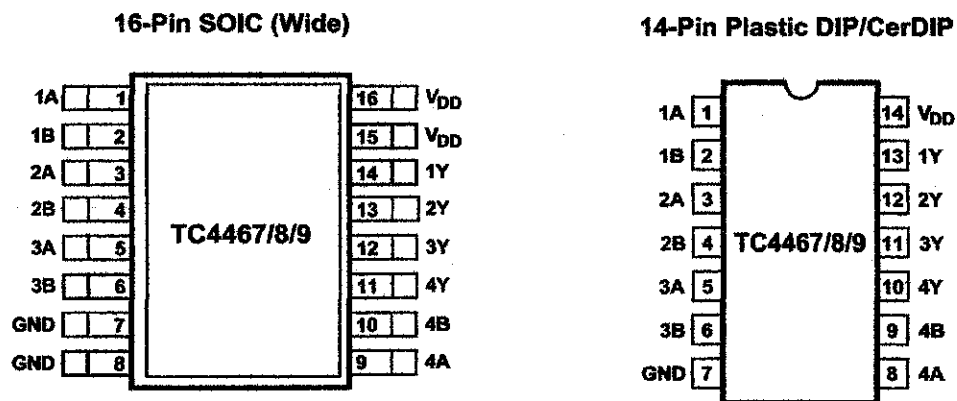
t_{Rise}	Rise Time	Figure 1	—	—	50	nsec
t_{Fall}	Fall Time	Figure 1	—	—	50	nsec
t_{DLY}	Delay Time	Figure 1	—	—	100	nsec
t_{DLY}	Delay Time	Figure 1	—	—	100	nsec

Power Supply

I_{DD}	Power Supply Current		—	—	8	mA
V_{DD}	Power Supply Voltage	Note 2	4.5	—	18	V

- ES:**
1. Totem-pole outputs should not be paralleled because the propagation delay differences from one to the other could cause one driver to drive high a few nanoseconds before another. The resulting current spike, although short, may decrease the life of the device.
 2. When driving all four outputs simultaneously in the same direction, V_{DD} shall be limited to 16V. This reduces the chance that internal dv/dt will cause high-power dissipation in the device.
 3. The input threshold has about 50mV of hysteresis centered at approximately 1.5V. Slow moving inputs will force the device to dissipate high peak currents as the input transitions through this band. Input rise times should be kept below 5 μ sec to avoid high internal peak currents during input transitions. Static input levels should also be maintained above the maximum or below the minimum input levels specified in the "Electrical Characteristics" to avoid increased power dissipation in the device.

CONFIGURATIONS



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Highly Bypassing

Large currents are required to charge and discharge capacitive loads quickly. For example, charging a 100 pF load to 18V in 25nsec requires 0.72A from the driver's power supply.

To guarantee low supply impedance over a wide frequency range, a 1 μF film capacitor in parallel with one or two low inductance 0.1 μF ceramic disk capacitors with short lead lengths (<0.5 in.) normally provide adequate bypassing.

Input Buffering

The TC4467 and TC4469 contain inverting drivers. Signal drops developed in common ground impedances from input to output will appear as negative feedback and affect the switching speed characteristics. Instead, individual ground returns for input and output circuits, or a ground plane should be used.

Input Stage

The input voltage level changes the no-load or quiescent supply current. The N-channel MOSFET input stage drives a 2.5mA current source load. With logic "0" inputs, maximum quiescent supply current is 4mA. Logic input level signals reduce quiescent current to 1.4mA maximum. Unused driver inputs must be connected to V_{DD} or GND. Minimum power dissipation occurs for logic "1" inputs.

The drivers are designed with 50mV of hysteresis. This ensures clean transitions and minimizes output stage current-spike when changing states. Input voltage thresholds are approximately 1.5V, making any voltage greater than 1.5V to V_{DD} a logic 1 input. Input current is less than 1 μA in any range.

Power Dissipation

The supply current versus frequency and supply current versus capacitive load characteristic curves will aid in determining power dissipation calculations. TelCom Semiconductors' CMOS drivers have greatly reduced quiescent DC consumption.

Output signal duty cycle, power supply voltage and load impedance influence package power dissipation. Given power dissipation and package thermal resistance, the maximum operating temperature is easily calculated. The plastic package junction-to-ambient thermal resistance is 83.3°C/W. At +70°C, the package is rated at 1W maximum dissipation. Maximum allowable chip temperature is +150°C.

Three components make up total package power dissipation:

- (1) Load-caused dissipation (P_L)
- (2) Quiescent power (P_Q)
- (3) Transition power (P_T).

A capacitive-load-caused dissipation (driving MOSFET gates), is a direct function of frequency, capacitive load, and supply voltage. The power dissipation is:

$$P_L = f C V_S^2,$$

where: f = Switching frequency
C = Capacitive load
V_S = Supply voltage.

A resistive-load-caused dissipation for ground-referenced loads is a function of duty cycle, load current, and load voltage. The power dissipation is:

$$P_L = D (V_S - V_L) I_L,$$

where: D = Duty cycle
V_S = Supply voltage
V_L = Load voltage
I_L = Load current.

A resistive-load-caused dissipation for supply-referenced loads is a function of duty cycle, load current, and output voltage. The power dissipation is:

$$P_L = D V_O I_L,$$

where: f = Switching frequency
V_O = Device output voltage
I_L = Load current.

Quiescent power dissipation depends on input signal duty cycle. Logic HIGH outputs result in a lower power dissipation mode, with only 0.6 mA total current drain (all devices driven). Logic LOW outputs raise the current to 4 mA maximum. The quiescent power dissipation is:

$$P_Q = V_S (D(I_H) + (1-D)I_L),$$

where: I_H = Quiescent current with all outputs LOW (4 mA max)
I_L = Quiescent current with all outputs HIGH (0.6mA max)
D = Duty cycle
V_S = Supply voltage.

GIC-INPUT CMOS QUAD DRIVERS

TC4467
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TC4469

Transition power dissipation arises in the complementary configuration (TC446X) because the output stage N-channel and P-channel MOS transistors turn ON simultaneously for a very short period when the output changes. The transition power dissipation is approximately:

$$P_T = f V_S (10 \times 10^{-9})$$

Package power dissipation is the sum of load, quiescent and transition power dissipations. An example shows relative magnitude for each term:

$C = 1000\text{pF}$ capacitive load

$V_S = 15\text{V}$

$D = 50\%$

$f = 200\text{kHz}$

$P_D = \text{Package Power Dissipation} = P_L + P_Q + P_T$
 $= 45\text{mW} + 35\text{mW} + 30\text{mW} = 110\text{mW}$.

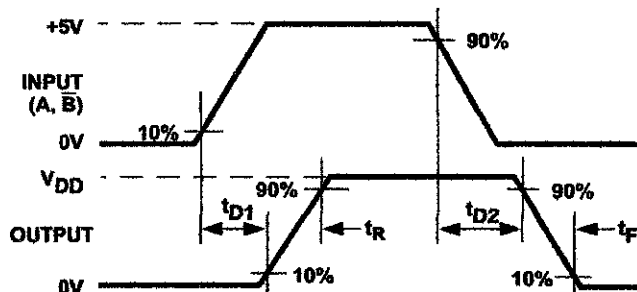
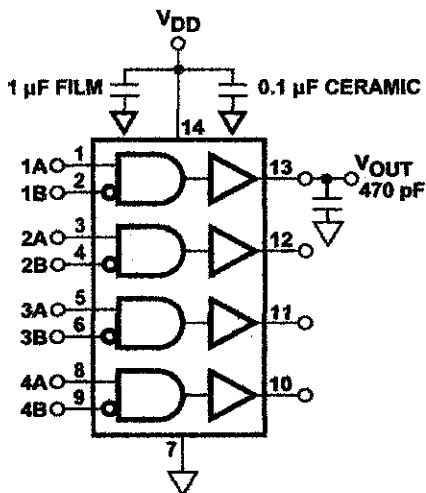
Maximum operating temperature:

$$T_J - \theta_{JA} (P_D) = 141^\circ\text{C},$$

where: $T_J =$ Maximum allowable junction temperature (+150°C)

$\theta_{JA} =$ Junction-to-ambient thermal resistance (83.3°C/W) 14-pin plastic package.

NOTE: Ambient operating temperature should not exceed +85°C for "EJD" device or +125°C for "MJD" device.



Input: 100 kHz, square wave,
 $t_{RISE} = t_{FALL} \leq 10\text{nsec}$

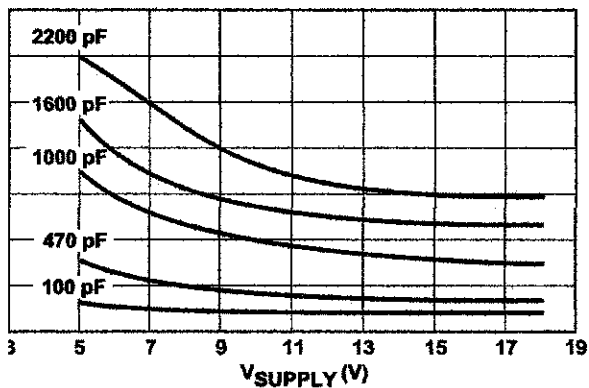
Figure 1. Switching Time Test Circuit

LOGIC-INPUT CMOS QUAD DRIVERS

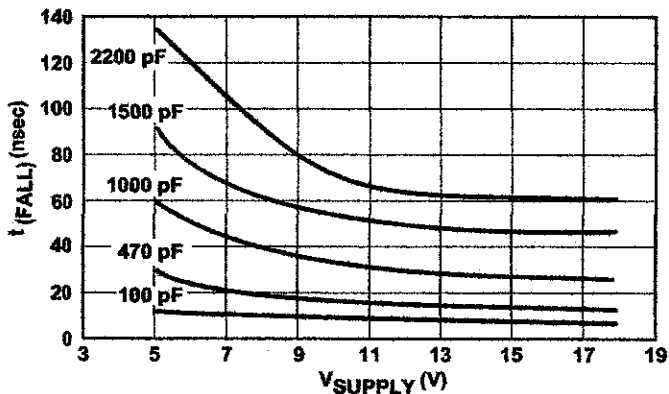
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CAL CHARACTERISTICS

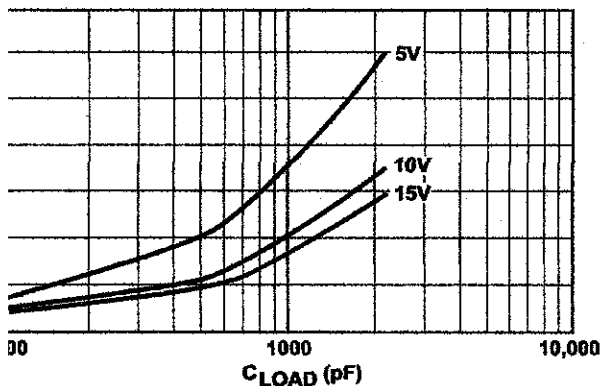
Rise Time vs. Supply Voltage



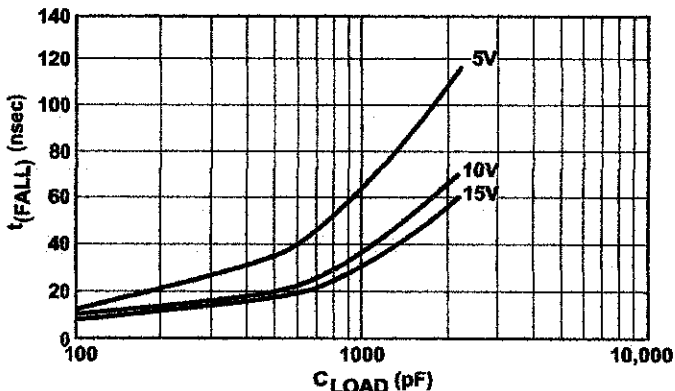
Fall Time vs. Supply Voltage



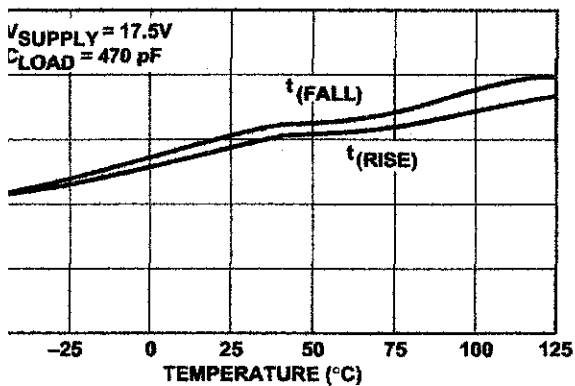
Rise Time vs. Capacitive Load



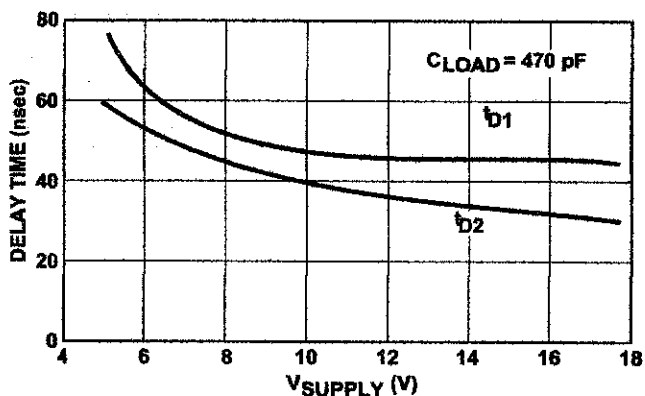
Fall Time vs. Capacitive Load



Rise/Fall Times vs. Temperature



Propagation Delay Time vs. Supply Voltage

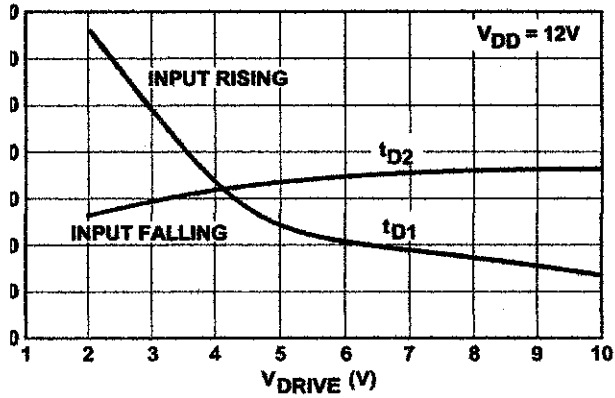


CMOS-INPUT CMOS QUAD DRIVERS

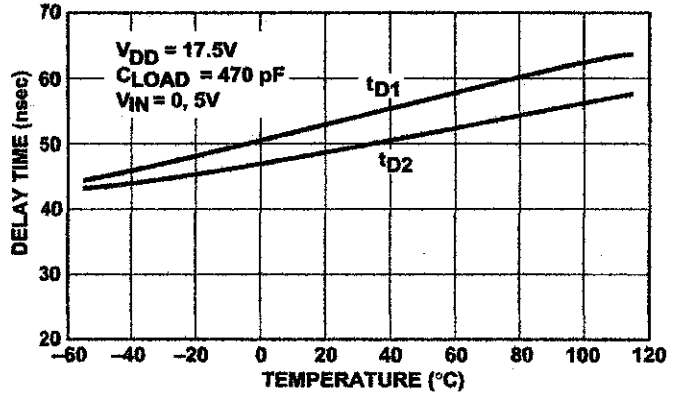
TC4467
TC4468
TC4469

TYPICAL CHARACTERISTICS (Cont.)

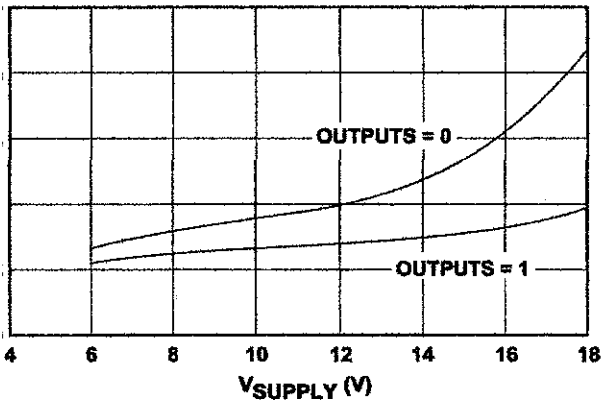
Input Amplitude vs. Delay Times



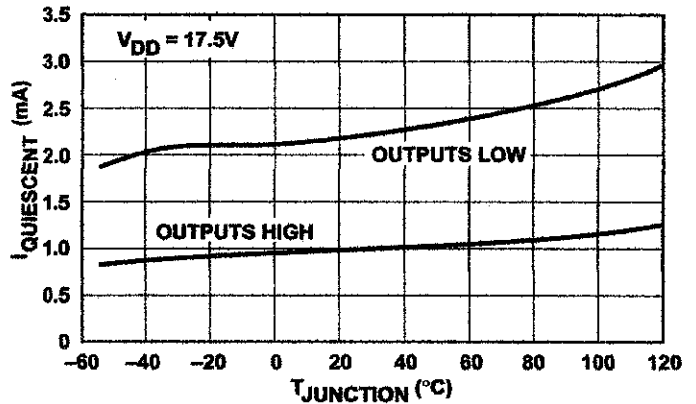
Propagation Delay Times vs. Temperature



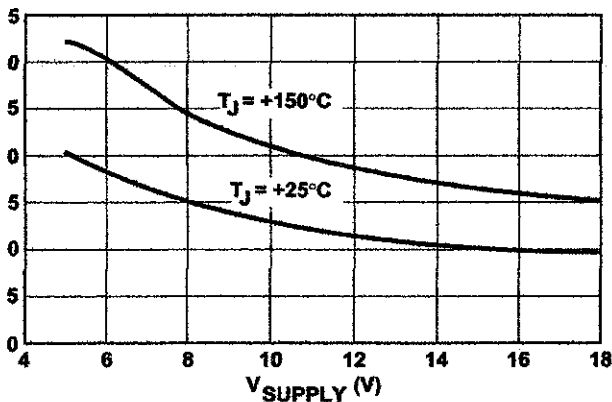
Quiescent Supply Current vs. Supply Voltage



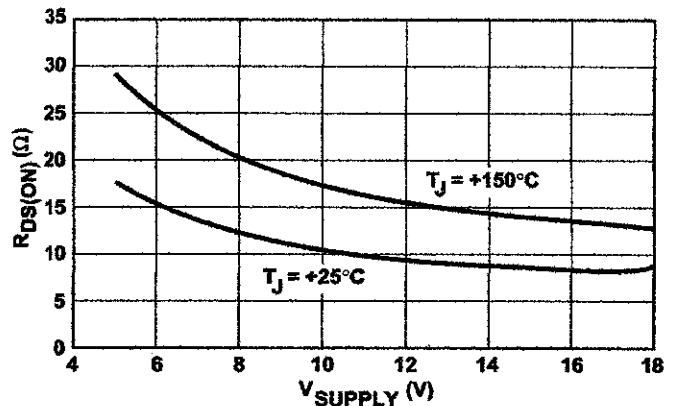
Quiescent Supply Current vs. Temperature



High-State Output Resistance



Low-State Output Resistance

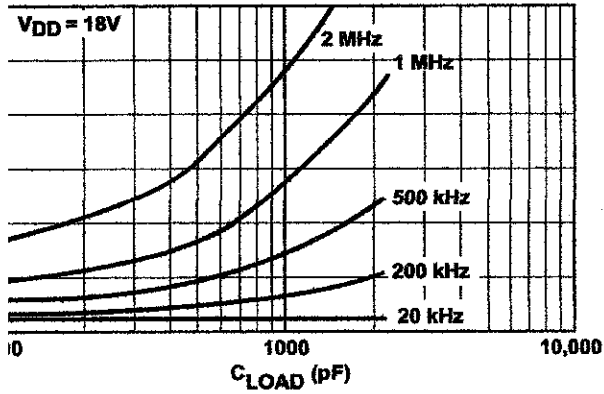


LOGIC-INPUT CMOS QUAD DRIVERS

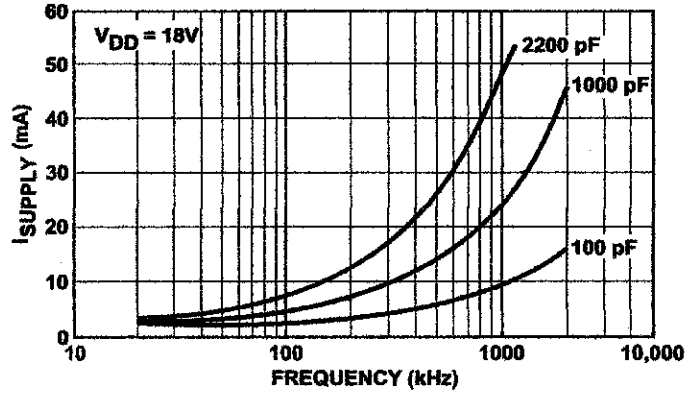
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PLY CURRENT CHARACTERISTICS (Load on Single Output Only)

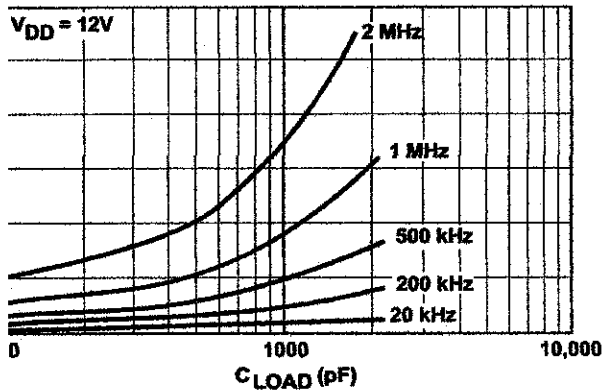
Supply Current vs. Capacitive Load



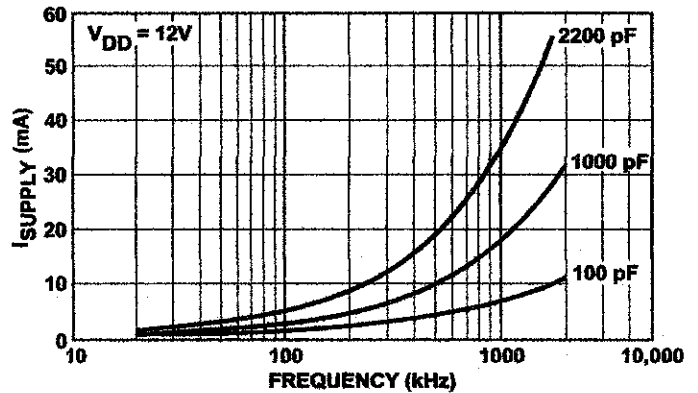
Supply Current vs. Frequency



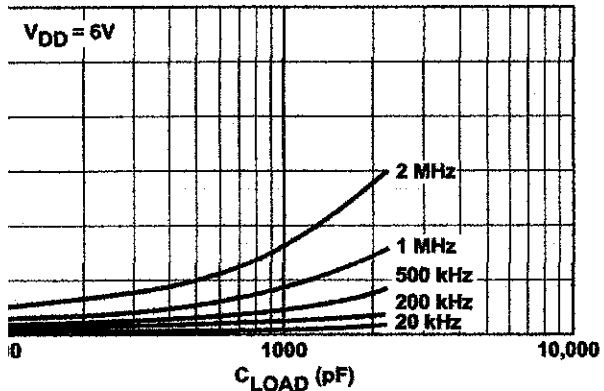
Supply Current vs. Capacitive Load



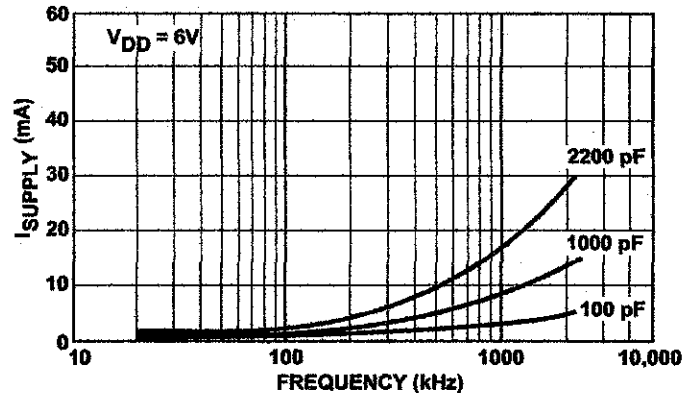
Supply Current vs. Frequency



Supply Current vs. Capacitive Load

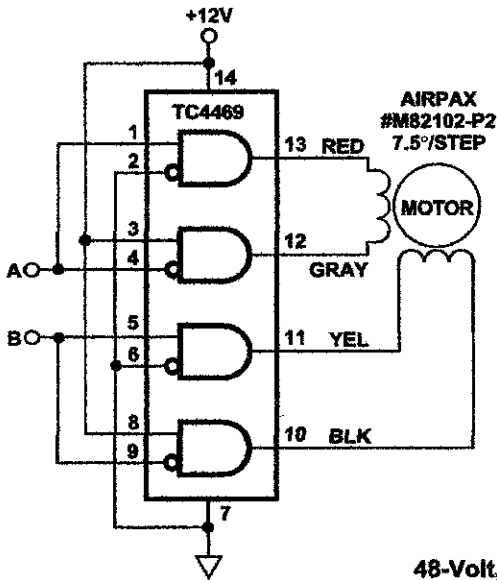


Supply Current vs. Frequency

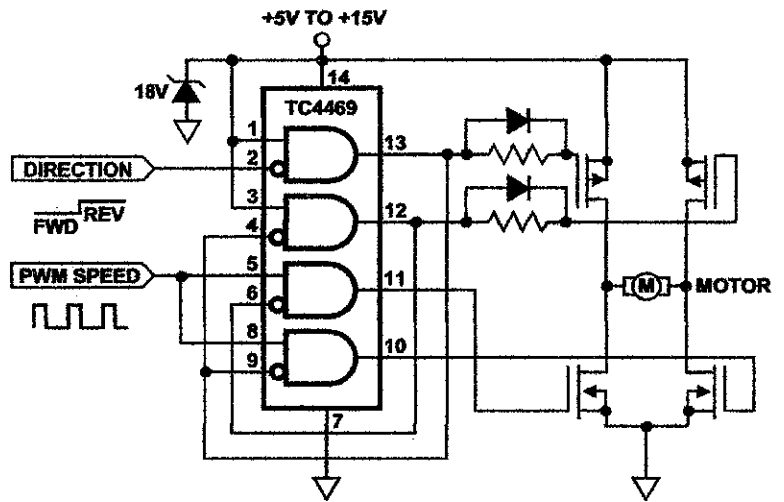


TYPICAL APPLICATIONS

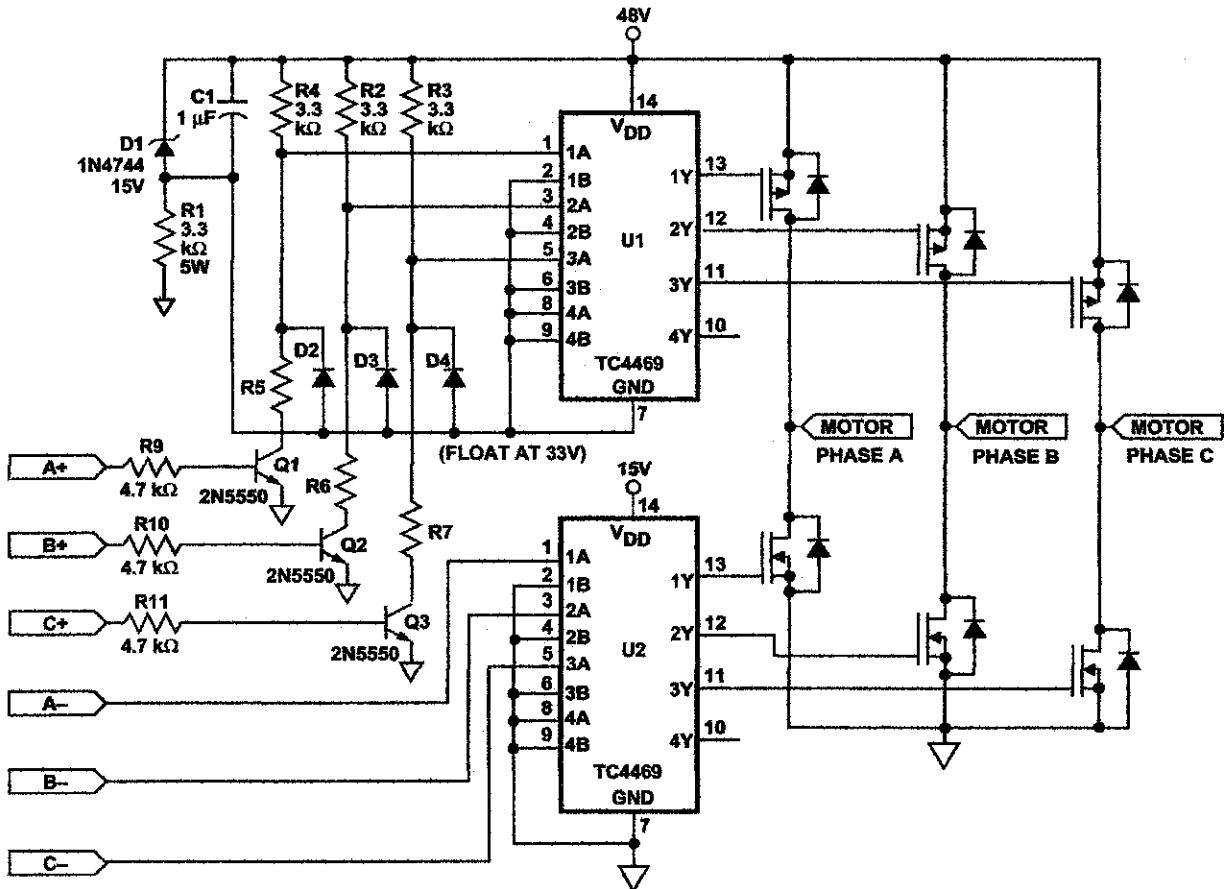
Stepper Motor Drive



Quad Driver for H-Bridge Motor Control



48-Volt, 3-Phase Brushless Output Stage

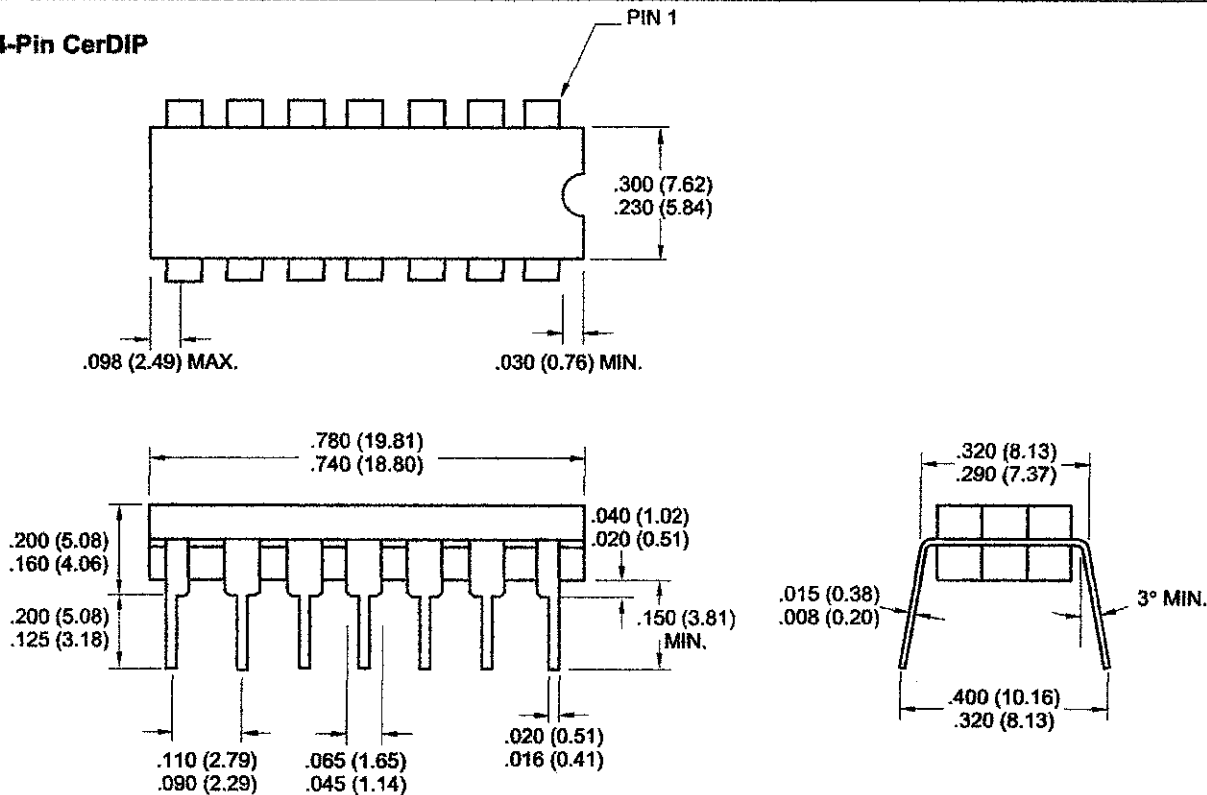


LOGIC-INPUT CMOS QUAD DRIVERS

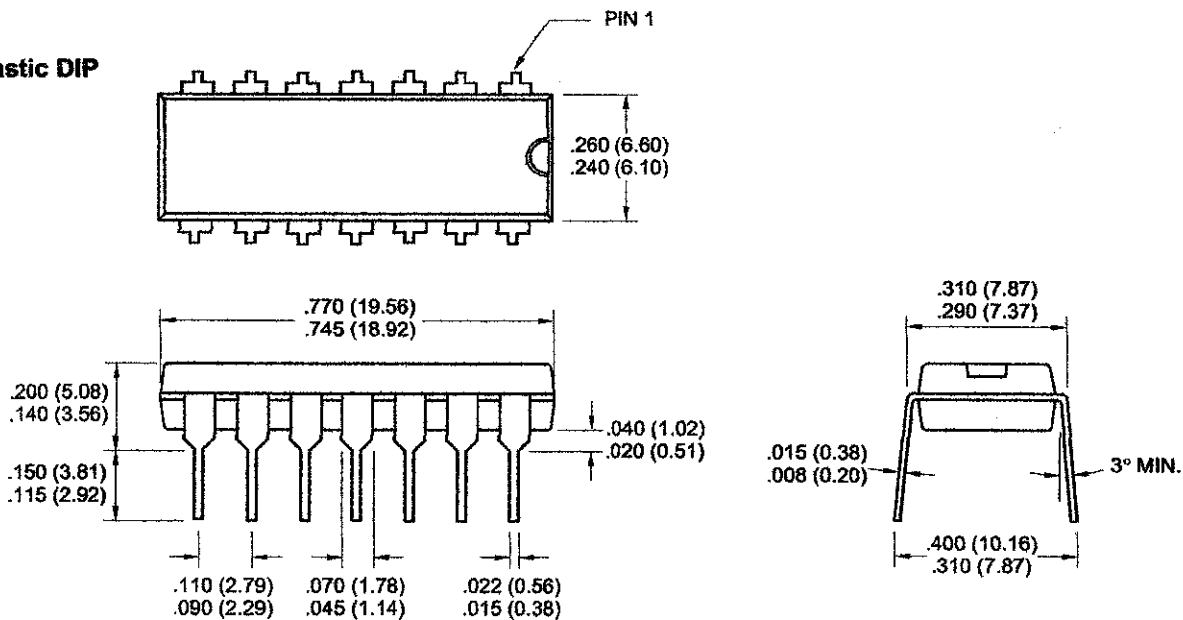
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PAGE DIMENSIONS

14-Pin CerDIP



14-Pin Plastic DIP



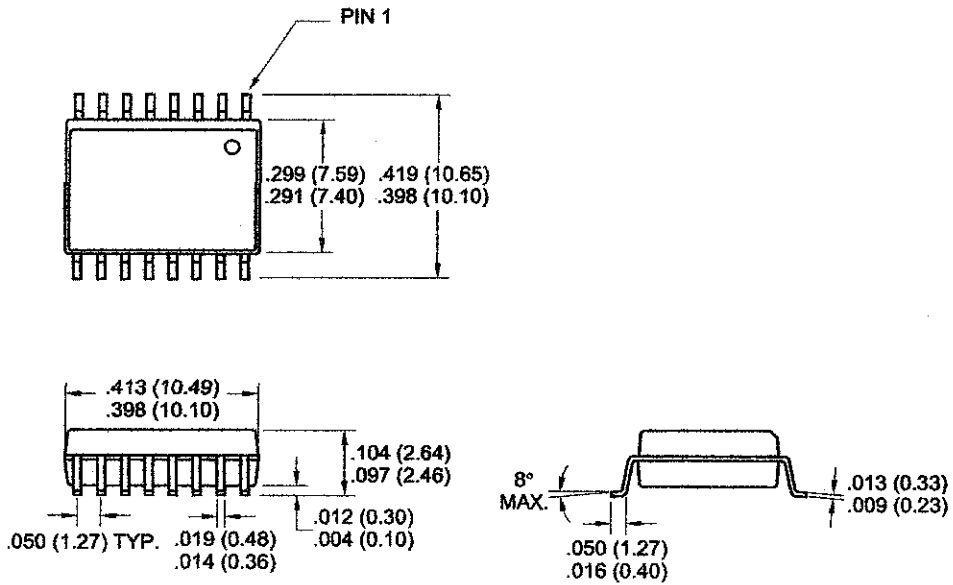
Dimensions: inches (mm)

LOGIC-INPUT CMOS QUAD DRIVERS

TC4467
TC4468
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PACKAGE DIMENSIONS (Cont.)

16-Pin SOIC (Wide)



Dimensions: inches (mm)



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