THE STUDY AND EVALUATION OF OUTPUT PARAMETERS IN SRBC

By

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FINAL REPORT

Submitted to the Electrical & Electronics Engineering Programme
in Partial Fulfillment of the Requirements
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Bachelor of Engineering (Hons)
(Electrical & Electronics Engineering)

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CERTIFICATION OF APPROVAL

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Approved by,
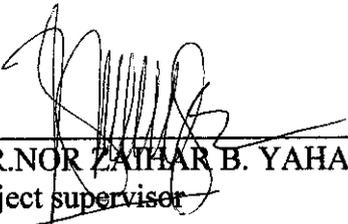
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MAY 2011

CERTIFICATION OF ORIGINALITY

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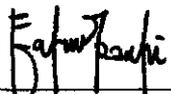
NUR FATIN 'IZZATI BT AHMAD

ABSTRACT

In era of technology, rapid advancement of low-loss converter design has become a major challenge to designers. Synchronous Rectifier Buck Converter (SRBC) is one of them. It is perceived that the development of low power converters in future must have the capability to operate in megahertz switching frequency. In this work, the study and evaluation of parameters in SRBC for two conditions: Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) will be carried out. This will help in search of the optimized parameter values for both conditions. This project will be based on simulation circuit using PSPICE software. The simulation will involve the study of the data sheet, circuit operation and the fundamental of SRBC circuit. Then, the results will be evaluated in terms of its losses, ripple and also body diode conduction. At the end of the project, the comparison between Conventional SRBC with Adaptive Gate Drive (AGD), Compensator and AGD, MOSFET Parallelism and Maximum Power Point Tracking (MPPT) are done to analyze on the performance of the circuit. It is found that the optimized parameter values for CCM are L=15 μH, C=0.625 μF and R=3.5 Ω while for DCM the value are L=1 μH, C=9.375 μF and R=4 Ω. Comparatively, it is proven that the Conventional SRBC is best when implementing using MPPT controller due to its ability in improving the output voltage and current and also reducing the losses which are voltage ripple, current ripple and body diode conduction.

ACKNOWLEDGEMENT

First and foremost, I would like to praise to Allah the Almighty for His guidance and time given to me for completing this course. With His guidance and blessings upon me, I managed to overcome all obstacles in completing this project. Here, I would like to use this opportunity to express my heartfelt thanks to everyone that has contributed to the completion of this project.

My deepest appreciation and gratitude for my Final Year Project Supervisor, Dr. Nor Zaihar B. Yahaya for his supervision, commitment, professionalism, advice and guidance throughout the success this project.

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Last but not least, special thanks to those who had helped me directly or indirectly in undertaking this project throughout the year. The contribution and insights are highly appreciated.

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LIST OF ABBREVIATIONS

CCM   Continuous Conduction mode

DCM   Discontinuous Conduction mode

MOSFET   Metal Oxide Field Effect Transistor

PWM   Pulse Width Modulation

SRBC   Synchronous Rectifier Buck Converter

CHAPTER 1

INTRODUCTION

1.1   Background of Study

In the advancement of technology development, the power converters are becoming widely used in the electrical industry. Nowadays, almost all electronic applications are demanding ever-increasing functionality in producing lower input and output voltages, higher currents and minimum losses from their power supply systems. Therefore, Synchronous Rectification Buck Converter (SRBC) is used having MOSFET acted as a switch to achieve the rectification function typically performed by diode. SRBC improves the performance, power density, manufacturability and reliability and decreases the overall system cost of power supply systems. Thus, this project intends to study the relationship among the inductor, capacitor and resistor in SRBC and to find the optimized values of the parameters in both CCM and DCM conditions. The results obtained from simulation will then be analyzed.

1.2   Problem Statement

The semiconductor industry has recently developed low-cost DC/DC converters that employ synchronous rectification in most applications. The designers have many trade-offs to consider such as losses improvement without cost, size, accuracy and outputs.

Even though the demand on producing high output current and low output voltage is high, it is difficult to generate and achieve the results. Due to this, the

study of the relationship between the inductor (*L*), capacitor (*C*) and resistor (*R*) in the SRBC is required. Moreover, the study will look into how far these parameters can influence the operation in CCM and DCM based on the optimized values.

1.3   Research rational of Fundamental SRBC circuit design

The lower resistance in overall circuit, the lower voltage spike on the switch node terminal v_N as shown in Figure 1 can be acheived. This node is also a point to observe the conduction of S_2 body diode.
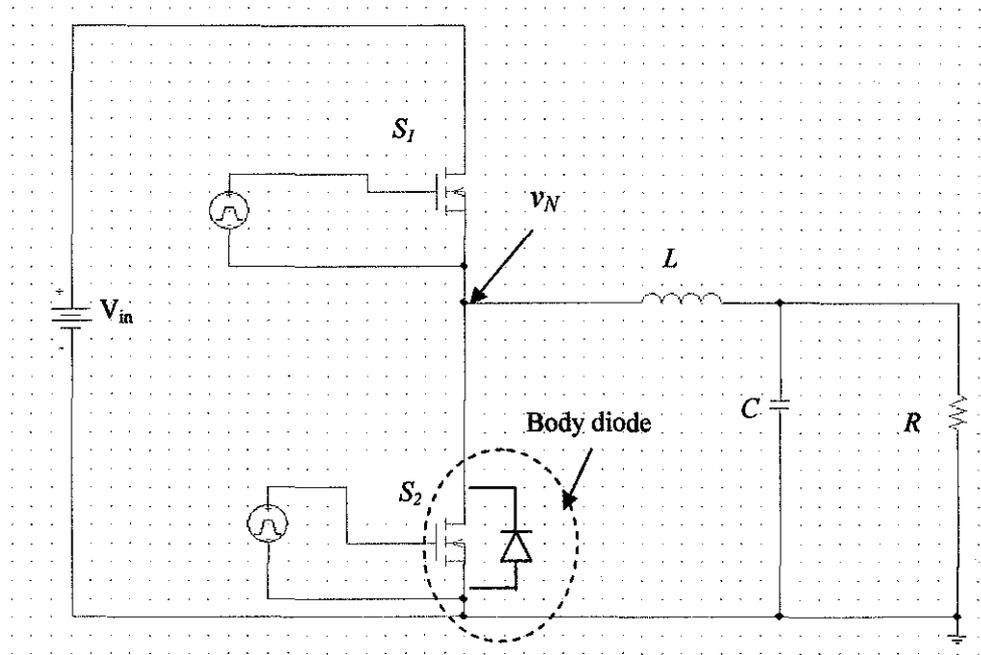
Figure 1: Conventional SRBC circuit

1.3.1   Effects of DCM and CCM

The switching loss in the switch S_1 and the reverse recovery loss in S_2 body diode can be minimized by allowing inductor current i_L to operate in DCM . A high output inductance (*L*) value can be used so that i_L flow will allow S_1 body diode to turn on before S_1 conducts during dead time , *Td* [1]. In CCM, i_L never touches zero, so this may cause switch S_1 to experience hard switching but the operation of S_2 current can easily reverse and reduce the body diode recovery loss.

Therefore, different load currents (varying load resistance) definitely will influence the total loss in the SRBC circuit.

1.4 Objectives

The objectives of the project are:

i.   To study the relationship of L, R and C of conventional SRBC design circuit.

ii.   To see the impact of these parameters to the output current and voltage.

iii. To determine the optimized output current for both CCM and DCM.

iv.   To compare and analyze the results of conventional SRBC with controlled SRBC.

1.5 Scope of Study

The scope of study will involve PSPICE simulation in the design of SRBC circuit where the setting the parameters is required. The SRBC's characteristics are important in determining the best results of the project. Overall, the project scope is divided into two stages whereby the first stage is the theoretical study of the parameters in the SRBC. The second stage will be to model and simulate the design of SRBC circuit using PSPICE. The simulation will illustrate the waveform of SRBC circuit indicating the best output current and voltage. Besides, the studies also concentrate on the CCM and DCM to see the impact on the SRBC performance. This circuit uses the frequency of 1 MHz, time delay of 15 ns and 250 ns duty cycle for 3 V output voltage generation.

CHAPTER 2

LITERATURE REVIEW

2.1 Pulse Width Modulation (PWM)

Conventional Pulse Width Modulation (PWM) technique is a process of interrupting power flow and controlling duty cycle of the converter. The use of PWM structure operating at a switching frequency more than 500 kHz normally can cause considerable losses due to the switching on the semiconductor device [2] where high switching stress will develop.

PWM is a method of transmitting information on a series of pulses. The data transmitted is determined based on the width of these pulses to control the amount of power being sent to the load. In other words, PWM is a modulation technique for generating variable width pulses to represent the amplitude of a wave. PWM is used to reduce the total power delivered to a load without resulting in loss, which normally occurs when a power source is limited by a resistive element. The fundamental principle in the whole process is that the average power delivered is directly proportional to the modulation duty cycle [3].

High frequency PWM power control systems can be realized using semiconductor switches. Here, the discrete ON or OFF state of the modulation can be used to control the switches, thereby controlling the voltage or current across the load. The major advantage with these types of switches is that the voltage drop across it during conducting and non-conducting states is ideally zero. PWM is widely used in voltage regulators. It works by switching the voltage to the load with the appropriate duty cycle, D as in Figure 2 whereby the output voltage is regulated at the desired level [3].

5.1V

D

ON

3.0V

OFF

0V

238.75µs   239.60µs   248.40µs   241.20µs

Time
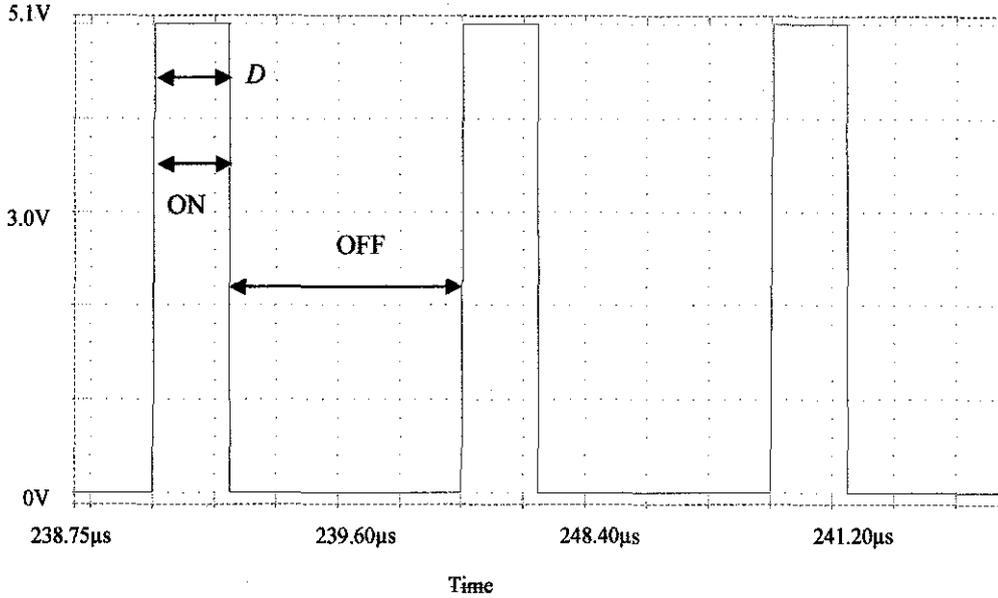
Figure 2: Example of PWM signal

2.2   Synchronous Rectifier Buck Converter (SRBC)

SRBC as opposed to conventional buck converters can achieve high efficiency in today's low-voltage, high-current applications because they replace the schottky diode of buck converters with a MOSFET as shown in Figure 3. As a result, the power they dissipate in the off-period is reduced significantly [4].

On the other hand, the use of MOSFET in replace of the schottky diode prohibits the converter from entering the discontinuous conduction mode (DCM) and reduces the conduction loss. In this circuit, a control switch, S_1 and synchronous switch, S_2 are conducting in complementary manner. Here, the charging and discharging of inductor current, i_L will produce an output voltage based on duty cycle set by S_1. More importantly, issues related to dead time will greatly result in lower efficiency and affect the performance of the converter [4,5].

The SRBC can operate in CCM, even down to no load. During the dead time periods, the i_L flows through the S_2 body diode. This body diode usually has a very slow reverse recovery characteristic that can adversely affect the converter's efficiency. An external Schottky diode can be placed in parallel with

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S_2 to shunt the body diode and prevent it from affecting the converter's performance. The added diode can have a much lower current rating because it only conducts during the small dead time (which is typically less than a few percent of the switching cycle) when both MOSFETs are off [6].
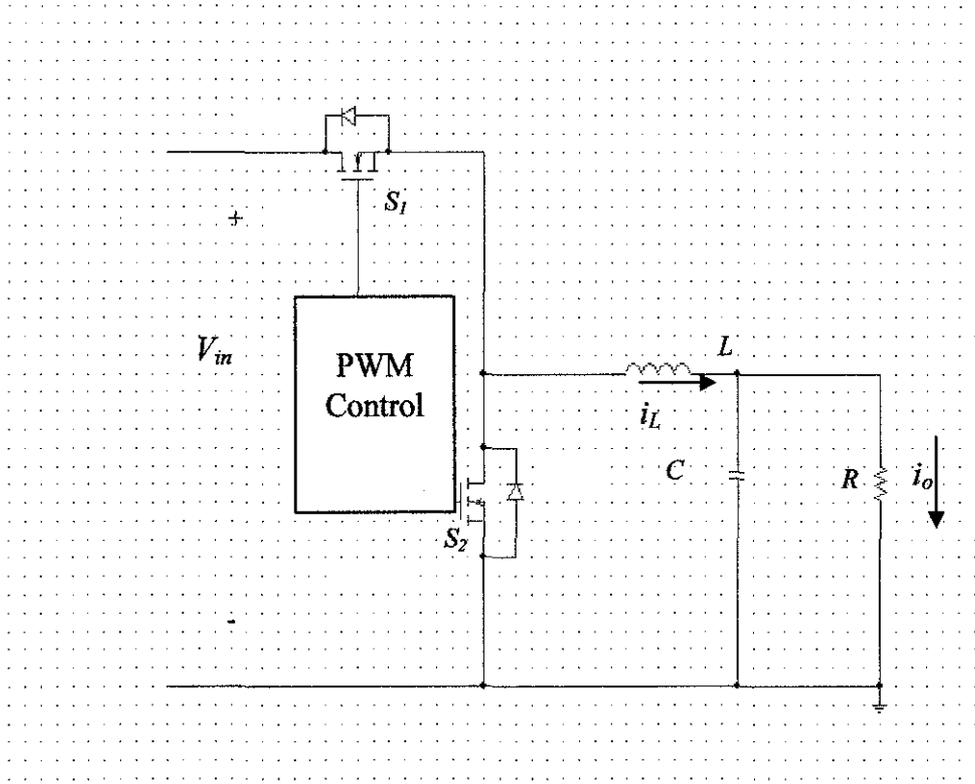
Figure 3: Conventional SRBC with schottky diode

2.2.1 Review of SRBC circuit

A buck converter is shown in Figure 4. It is a step-down circuit which produces a lower output voltage than its DC input. In this circuit, the freewheeling diode turns on shortly after the switch turns off which results in a voltage rise across the diode. The diode's capacitance is charged during switch turn-on which gives power dissipation, P_d in diode given by Eq. (1) and the voltage drop, V_d associated with this is defined by Eq. (2)

$$P_{c(diode)} = \frac{1}{2} \times C_{diode} \times V_s^2 \times f_s \qquad (1)$$

$$P_d = V_d \times (1 - D) \times i_L \qquad (2)$$
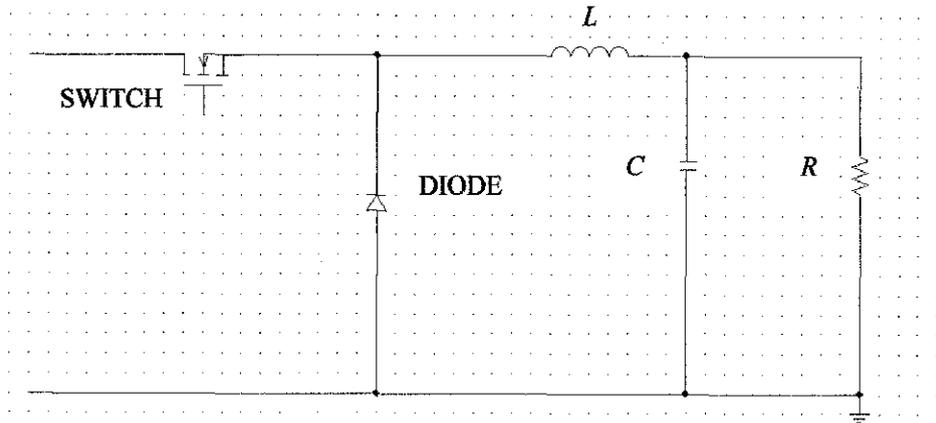
Figure 4:Buck Converter with Rectifier Diode

Figure 5 shows the SRBC inheriting a modified version of the basic buck converter circuit topology where the diode is replaced with a second switch, S_2. This modification is a trade-off between increased cost and improved efficiency.
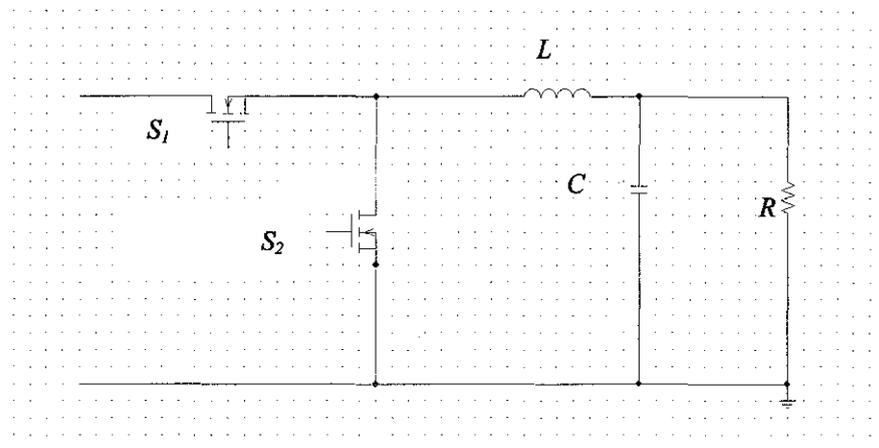
Figure 5 :Modified Buck Converter (Adding S_2 Switch)

The conventional SRBC circuit with gate drive block is shown in Figure 6. The circuit consists of a S_1, S_2, an inductor, a capacitor, and a resistor. When S_2 is used, it may degrade the efficiency of the converter at light load by disallowing i_L from entering the DCM and maintaining operation in CCM. This happens because MOSFET allows bidirectional flow of i_L. In short, SRBC enables high frequency operation but produces low efficiency at low output power. At lighter loads than i_o, efficiency degrades because the switching loss dominates the total input power. At

heavier loads, the efficiency decreases due to higher conduction losses associated with the inductor and bridge resistances [5,7].
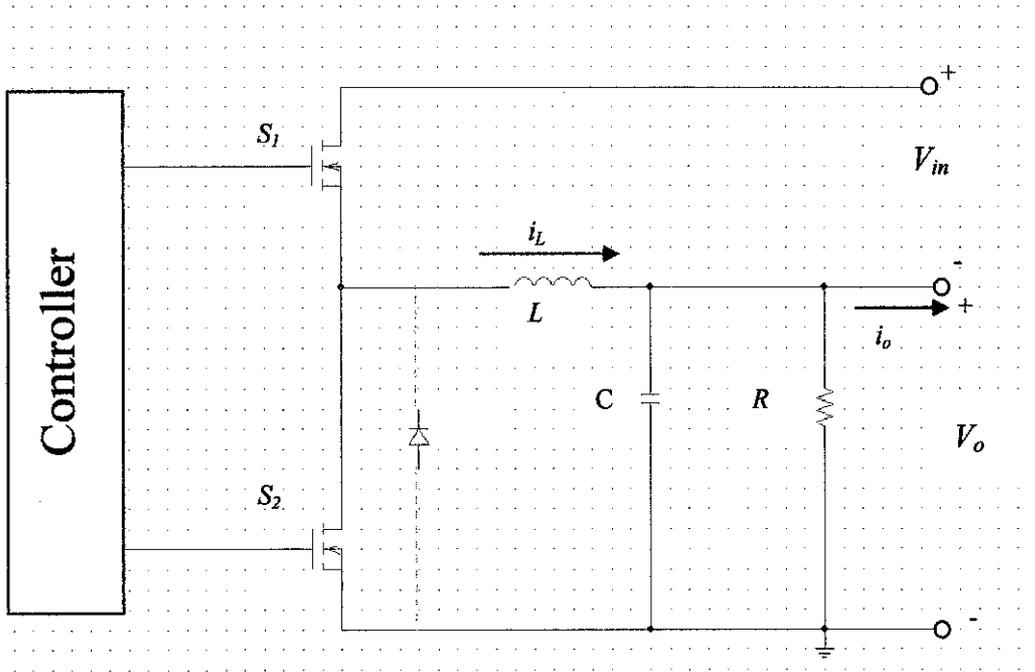
Figure 6: Conventional SRBC Circuit with gate drive

2.2.2   Advantages and disadvantages of SRBC

Replacing the diode with S_2 which advantageously selected for lowering conduction loss, will reduce the voltage spike of gate voltage of S_2 and improve the performance of the converter. Some advantages and disadvantages in having S_2 are as shown in the Table 2.1 [8]:

Table 2.1: Advantage and Disadvantages of S_2

ADVANTAGES	DISADVANTAGES
a) Allows bidirectional power flow b) Efficiency can increase because on-state voltage drops of S_2 is less than forward voltage of diode. c) Control can be simplified.	a) Both switches, S_1 and S_2 are always conducting even if there is no energy being transferred. b) Higher losses are present in switches and also in L. c) May cause additional ripple overshoot in drain voltage of S_2. d) Will introduce an induced dv/dt switching, which may degrade the performance [9].

2.2.3 Issues in SRBC

In designing the SRBC circuit, the performance of the circuit is important in order to maintain the circuit in stable operation. Here, some issues in SRBC are presented in Table 2.2.

Table 2.2: Summary of issues in SRBC

COMPONENTS	PAPER	ISSUES
PWM	[2]	-The use of PWM structure operating at a switching frequency more than 500 kHz normally can cause considerable losses due to the switching on the semiconductor device where high switching stress will develop.
INDUCTOR	[5]	-A higher L produces larger voltage swing at the load, leading to the reduction of switching time due to smaller gate voltage value, increase in $trise$ and $trec$ and also switching loss. -Even though, large L will reduce ripple, it limits the energy transfer speed but a small value can produce a faster slew rate.
	[13]	-With a smaller L, the gate drive speed improves as this will increase transient time but with the cost of high power loss.
	[14]	-Smaller L can help increase faster transient response and high power density.
	[19]	-A smaller inductor value enables a faster transient response; it also results in larger current ripple, which causes higher conduction losses in the switches. -The smaller inductor also requires a larger filter capacitor to decrease the output voltage ripple.
CAPACITOR	[19]	-Lower in capacitor value causes in large overshoot and large voltage ripple. -It effects the voltage during the time the switch is off.
RESISTOR	[10]	-The advantage of this method is that it provides the highest tolerance accuracy. -The disadvantage is that it lowers the system efficiency.

2.2.4 Ideal Operating Waveforms of SRBC in CCM
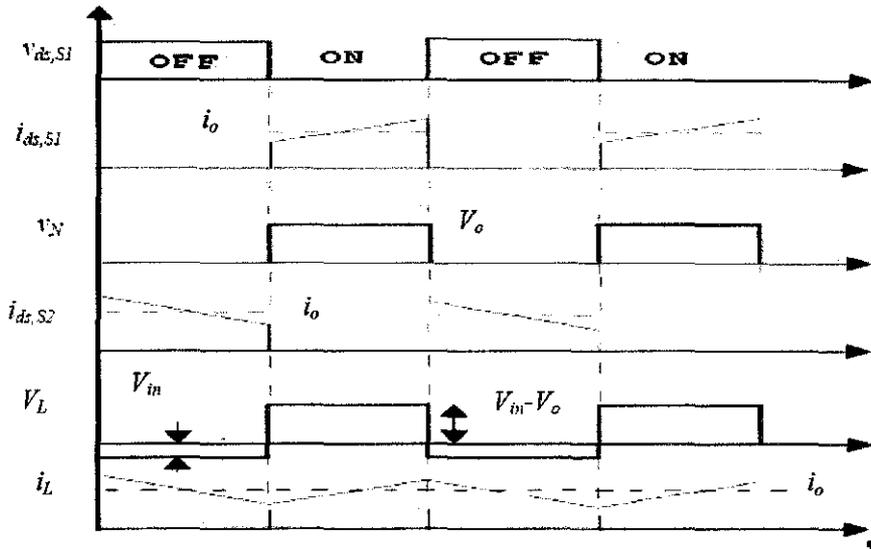
Figure 7 : Operating Waveforms of SRBC Circuit (with no *Td*) [11]

Figure 7 shows the ideal operating waveforms for SRBC circuit. Depending on the applicable *L* value, the load current operates in CCM mode where heavy load current is expected to drive the output. Ideally, there will be no cross conduction . The drain current of S_1 and S_2 are charging during turn-on of S_1 and S_2 respectively. Clearly by referring to the node switch, v_N waveform in the figure, there is no negative region indicating zero body diode conduction. Details in calculating the parameter values are described in details in [11] which is briefly explained below.

a) Switching frequency, *fs*

The switching frequency, *fs* influences the efficiency of the system. At higher switching frequency, more power will be dissipated in the SRBC. The efficiency is calculated using Eq. (3)

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{V_0 I_0}{V_{IN} I_{IN}} = \frac{P_0 + P_{TLOSS}}{P_{IN}} \tag{3}$$

Where P_{TLoss} = total power loss

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b)   Output capacitance, C

Output capacitor, C is used to reduce the voltage ripple at the load. The charge of the capacitance used also depends on load current ripple, Δi_L and the switching frequency, Eq. (4). From here, the voltage ripple, Δv_o and the minimum capacitance value can be calculated using Eq. (5) and Eq. (6). The waveform is shown in Figure 8. C must be large in order to regulate output voltage level.

$$q = \frac{1}{2} \times \Delta i_L \times \frac{t_{sw}}{2} \tag{4}$$

Where $q = 2 \times C \times \Delta v_0$

$$(2\Delta v_o) = \frac{\Delta i_L}{4 \times f_s \times C} \tag{5}$$

Rearraging

$$C > \frac{\Delta i_L}{8 \times f_s \times \Delta v_0} \tag{6}$$
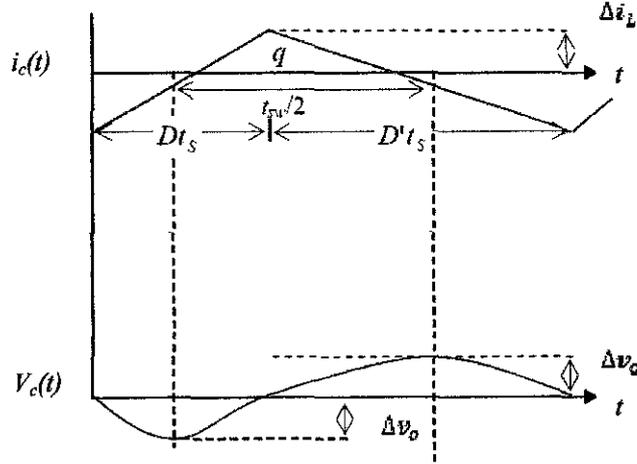
Figure 8: Capacitor current and voltage output waveform of SRBC circuit

c)   Output Inductance, L

The function of the inductor is to limit the current through the load when the switch is conducting. The inductor can control the percentage of ripple. The current ripple magnitude, Δi_L can be found from Eq. (7) resulting L to be Eq. (8). Smaller L can help increase faster transient response and high power density [12]. In addition, it can determine the circuit operation either in CCM or DCM.

$$\Delta i_L = \frac{V_{in} - V_o}{L \times f_s} \ (D) \tag{7}$$

$$L = \frac{D \times (V_{in} - V_o)}{\Delta i_L \times f_s} \tag{8}$$

With a smaller L, the gate drive speed improves as this will increase transient time [13] but with the cost of high power loss. Peak current will increase and this eventually adds to the losses of the gate driver. The optimized L value given by Eq. (8) [14]. Nevertheless, this L is subject to manufacturing variation.

A higher L produces larger voltage swing at the load. In addition, this will lead to the reduction of switching time due to smaller gate voltage value and switching loss. Even though, large L will reduce ripple, it limits the energy transfer speed but having a small value can produce a faster slew rate. So, this is one of the reasons why L has to be optimized [5,14].

2.2.5 Body Diode Conduction Loss

When S_1 and S_2 are off, parasitic body diode of S_2 is forward biased due to the continuity of i_L, and thus generating an undershoot of approximately - 0.7 V at v_N. This whole negative duration indicates the duration of body diode conduction. S_2 body diode is turned on by a circulating current that flows into L as soon as S_1 is turned off. However, S_2 can concurrently conduct with its body diode, creating stored charge that must be removed before S_2 can support voltage. This leads to high switching loss in S_1 and an increase in reverse recovery loss in S_2 body diode. So, S_2 needs to be turned off completely before S_1 starts to conduct during Td [5,15].

After Td delay ends, S_2 will start to conduct. Since the forward voltage drop across S_2 is much lower than its body diode voltage drop, this will allow i_L to flow through S_2 instead [16]. Figure 9 shows the effect of the body diode conduction.
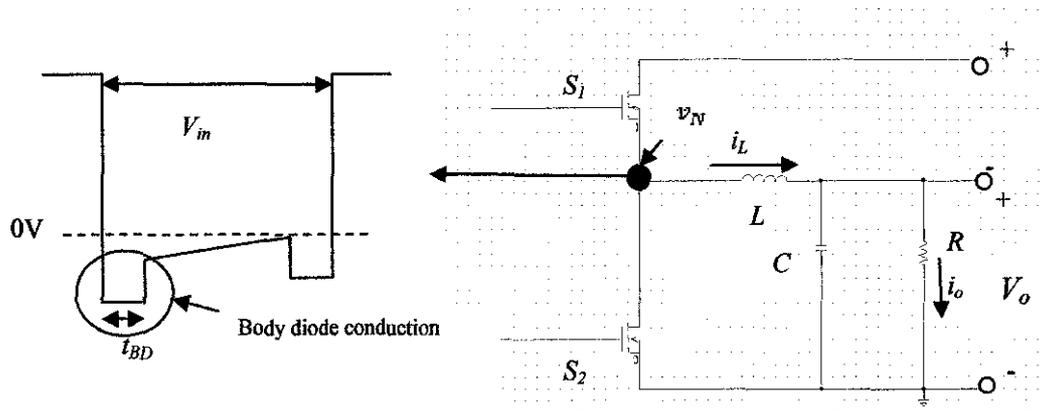
Figure 9 : Body Diode Conduction

The effect of body diode is circled in the Figure 9. The period of the body diode conduction is related to Td. The longer Td is, the longer body diode conduction period will be. Allowing the i_L to flow through the body diode of S_2 switch has a degrading effect on the overall converter's performance since it contributes to the losses. Note that the t_{BD} increases with Td and so does the body

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diode conduction loss [9,17]. This shows that as *Td* value increases, the power losses will increase. The equation is given by Eq. (9),

$$P_{BD} = V_F \times t_{BD} \times f_s \times i_o \qquad (9)$$

where

V_F = body diode forward voltage drop
t_{BD} = body diode conduction time

The losses are proportional to the body diode conduction time. A smaller body diode conduction time will have smaller conduction losses. Thus, in order to have a low body diode loss, a shorter *Td* delay is required. In high frequency low output voltage powerstage, the additional loss due to body diode conduction can be as high as 6 % from overall loss [18].

2.2.6 Continuous Conduction Mode (CCM) in SRBC

Current flows continuously in the inductor during the entire switching cycle in steady state operation. In most SRBC applications, overall performance is usually better using continuous mode, and it allows maximum output power to be obtained from a given input voltage and switch current rating. The current through the inductor is rising linearly [19].

CCM is when the inductor current always is at positive region. The inductor current flows in the positive direction toward the output during an entire switching cycle, constantly supplying current to the load. In this mode, the S_2 is on whenever S_1 is off, so the current always flows through a low impedance switch channel, minimizing voltage drop and conduction loss. This is the most efficient operation mode however, the conduction losses in the power devices are usually dominant. The ripple current depends on inductor value, switching frequency and output voltage, but is constant regardless of load as long as the converter remains in constant frequency operation. The small value of R will maintain the SRBC circuit operating in CCM [20] as in Figure 10.

Figure 10 : CCM [19]

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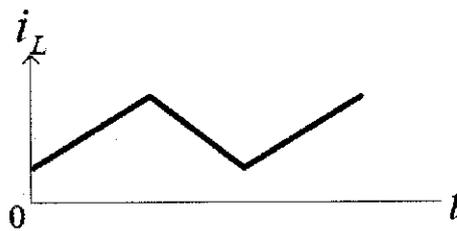
2.2.7 Discontinuous Conduction Mode (DCM) in SRBC

In DCM, the inductor current falls to zero and remains at zero for some portion of the switching cycle. It starts at zero, reaches a peak value, and returns to zero during each switching cycle. In applications where the maximum load current is fairly low, it can be advantageous to design for discontinuous mode operation. In these cases, operating in DCM can result in a smaller overall converter size (because a smaller inductor can be used). Often the output capacitor must be large to keep the voltage constant. This is because MOSFET switch, unlike a diode based rectifier, allows negative inductor current i_L, indicating a reverse leakage current from the load to ground. This current leakage costs an additional power loss and undermines the light load efficiency [19, 21]. The DCM typically occurs with large inductor current ripple in a converter operating at light load which means it requires low output current to drive the load containing current-unidirectional switches. [22]

The resistance value R influences the operation mode in the SRBC .When R is increased, the dc load current is decreased and it will go into DCM as in Figure 11. The dc component of inductor current i_L will then decrease, but the ripple magnitude Δi_L will remain unchanged. But, by allowing inductor current i_L to operate in DCM, these will minimize the losses caused by the switches in such way S_1 will experience swithing loss and reverse recovery loss in S_2 switch body diode [5, 23].

Figure 11: DCM [19]

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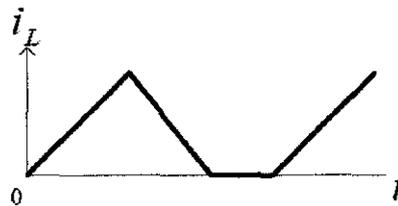
CHAPTER 3

METHODOLOGY

3.1   Project identification

The overall design methodology throughout this project is shown in Figure 12 below:
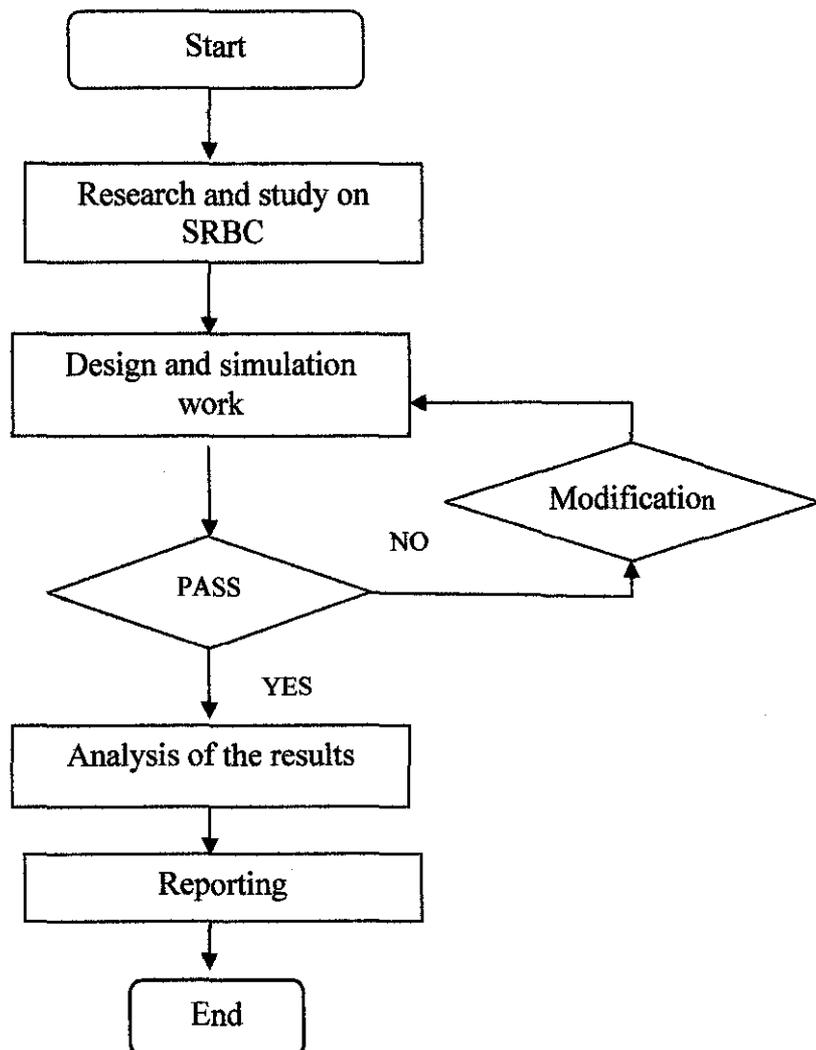
Figure 12: Flow of the project

3.2 Research and study on SRBC

The study is done based on basic operation and concept of conventional SRBC circuit. All information such as related waveforms, issues, and associated techniques in designing the gate drivers are gathered from the internet, journals and thesis. The purpose of this step is to understand the basic concept, investigate the issues and also be able to differentiate the CCM and DCM operations.

3.3 Design and simulation works

The project starts with designing and simulating the basic conventional SRBC. The circuit used for this project is indicated in Figure 1. In designing the circuit, all related topologies, selection of the suitable components, parameters and calculations will be determined. Here, the conventional SRBC circuits are designed based on the design specifications that have been stated as follows:

a) D : 0.25

b) V_{in} : 12 V

c) V_o: 3 V

d) Switching frequency, f_s = 1 MHz

There are limiting parameters that need to be checked and ensured in order to get the best outputs. The limiting parameters are the duty ratio, D, inductor, L, capacitor, C and resistor, R. The optimized values of all parameters are chosen wisely with regards to the objectives of this project.

After the SRBC circuit is drawn using PSPICE software, the PWM setting of S_1 and S_2 are first set-up with duty ratio of 250 ns for 1 MHz frequency. Then, all optimized values of the L, C and R that produce high output current with 3 V output voltage are substituted in the circuit. As all the settings are completed, the circuit is simulated and parameters such as node voltage, v_N, output current, i_o inductor current, i_L and output voltage, V_o are observed and evaluated.

3.1.1 Optimization of the duty ratio, D

The variation of *PWM 1* and *PWM 2* can influent the duty ratio, *D*. Duty ratio determines the length of conduction time power MOSFET S_1 and it must provide sufficient on-time for i_L to completely charge and discharge. Otherwise, this eventually results in oscillation during turn-off and hence generates power loss. Table 3.1 shows the settings of *PWM 1* and *PWM 2* used in SRBC circuit.

Table 3.1: Setting of pulse width of S_1 and S_2

	PWM 1	*PWM 2*
V1	0 V	0 V
V2	5 V	5 V
TD	0 ns	265 ns
TR	5 ns	5 ns
TF	5 ns	5 ns
PW	240 ns	710 ns
PER	1000 ns	1000 ns

In 1 MHz switching frequency, pulse width duration of 250 ns is chosen as a benchmark in the design, resulting in a duty ratio of 25 %. The duty ratio is important as it controls the charging and discharging of the inductor current during the conduction of S_1 and S_2.

Voltage, V_{in}
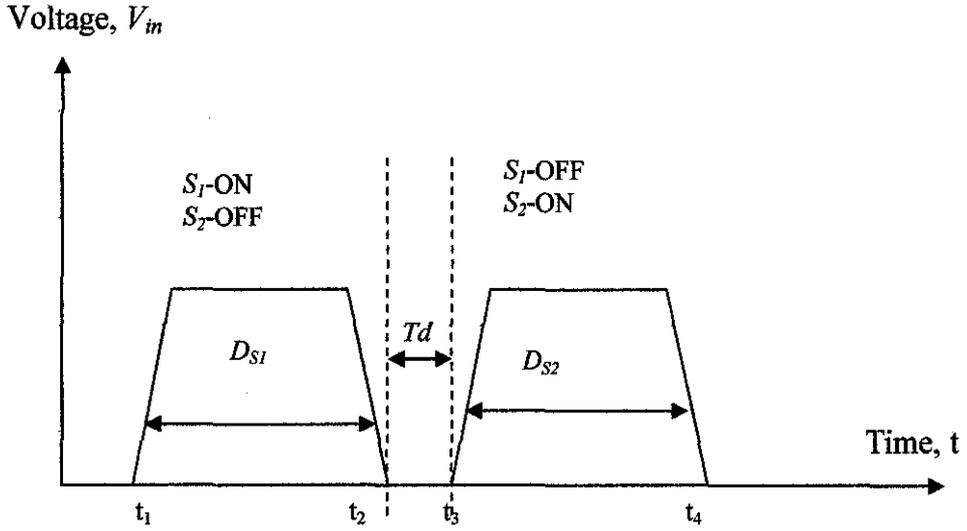
Figure 13: Duty ratio

As shown in Figure 13, the duty ratio, D is provided in each PWM of S_1 with the applicable dead time, Td in between. The Td is set to 15 ns to avoid S_1 and S_2 from overlapping. The duty ratio for both S_1 and S_2 is calculated as Eq. (10) and Eq. (11) below:

$$\text{Duty ratio for } S_1, D_{S1} = \frac{t_2 - t_1}{t_4 - t_1} \qquad (10)$$

$$\text{Duty ratio for } S_2, D_{S2} = \frac{t_4 - t_3}{t_4 - t_1} \qquad (11)$$

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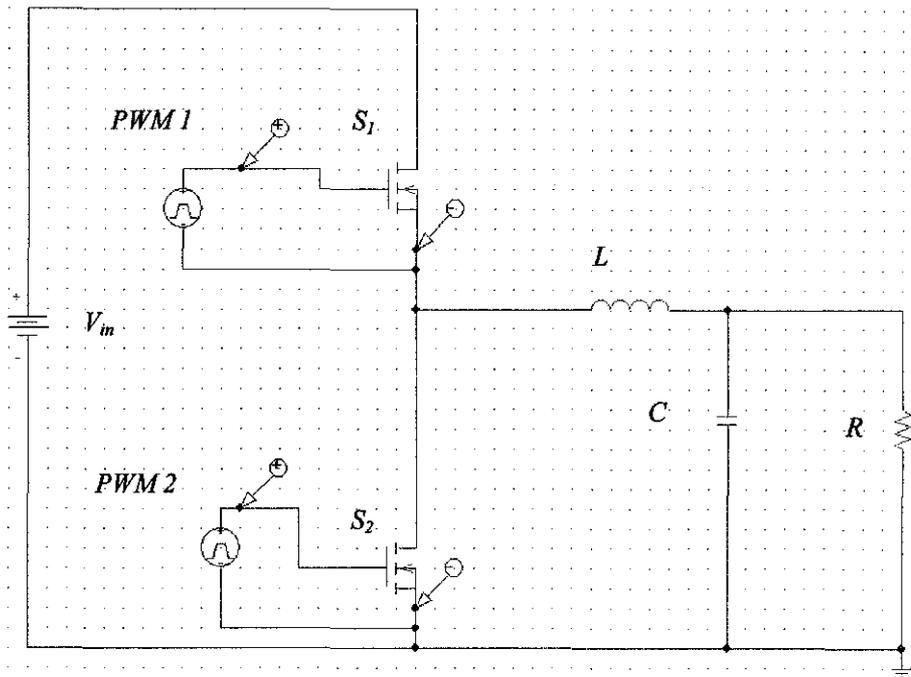
Figure 14: PWM measured points in PSPICE

Figure 14 shows where the PWM is measured in PSPICE. Using the voltage differential maker, the voltage and the waveform of the PWM are checked to make sure the circuit is operated at correct duty ratio.

3.3.2 Optimization of L, C, and R

The correct parameter values are important in order to get the output current and voltage. Equation (5) until Eq. (8) are the equations used to calculate the parameters required in designing the circuit. The equations also determine the boundary of CCM and DCM.

To determine the value of inductor and capacitor, it is assumed that the output ripple voltage is within ± 1 % of the V_o, which is equal to 0.03 V. The value of the inductor is fixed and then substituted into Eq. (6) to obtain the value of capacitor. The load resistor is chosen based on 3 V output voltage. For CCM, the optimized value of inductor is chosen to be 15 µH, capacitor is 0.625 µF and 3.5 Ω for resistor. For DCM, the same step is repeated and the optimized values

are 1 μH of inductor, 9.375 μF of capacitor and 4 Ω of resistor. The value of resistor for DCM is chosen to be higher than CCM to control the output voltage of 3 V. After the values of all parameters are determined, the circuit is simulated and the node voltage, output voltage, current and also the inductor current are measured. Node voltage is observed to ensure the PWM or switching pulses are generated correctly. Meanwhile, the output voltage and current are measured based on their average values. Then the inductor current is obtained to check the operation of the SBC whether it is in CCM or DCM.

Figure 15 and Figure 16 show the optimized values of CCM and DCM for PSPICE simulation respectively.
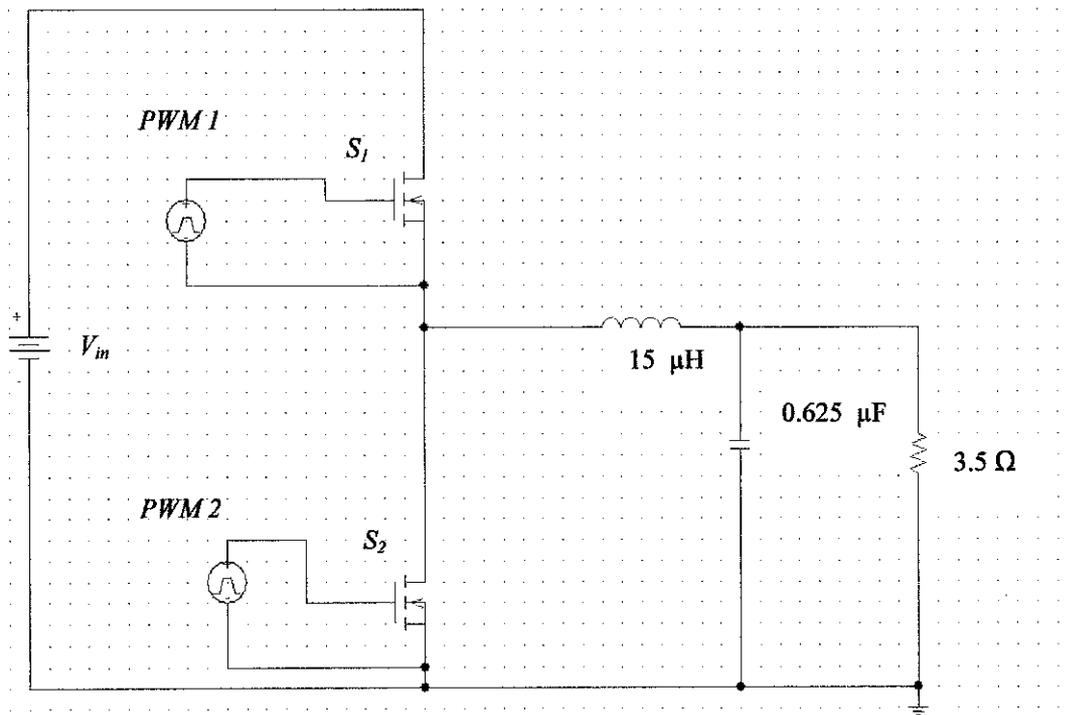
Figure 15: CCM circuit of optimized parameters
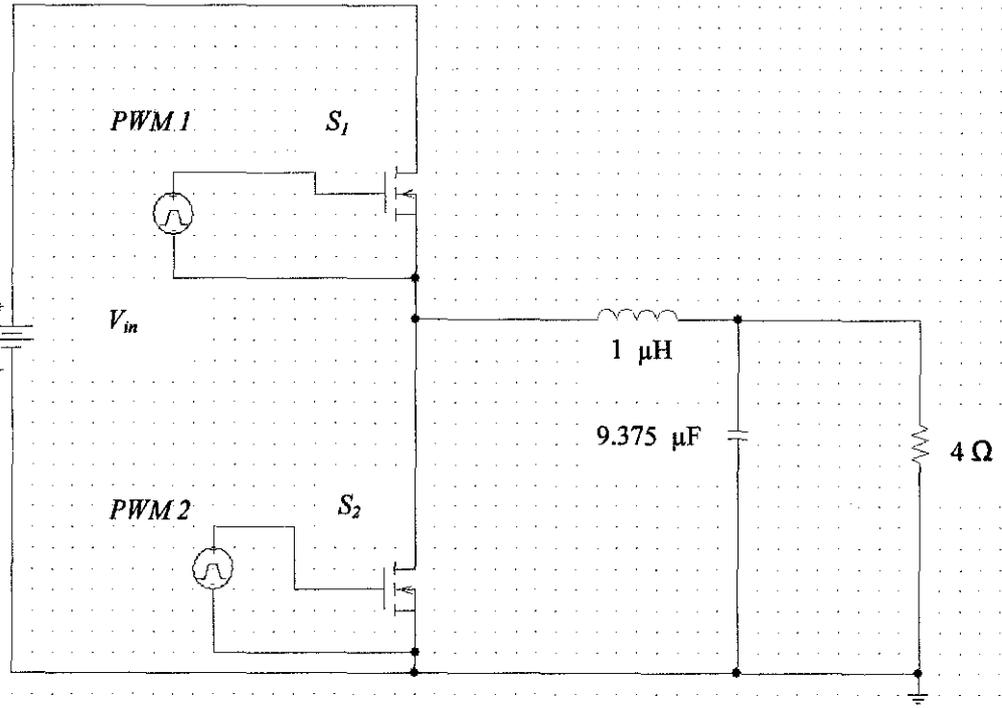
Figure 16: DCM circuit of optimized parameters

3.4 PSPICE simulation

The simulation is required to check whether the designed circuit meets the expectation and produces the desired output. Here the outputs are determined by the PSPICE simulation. The graphs obtained will be observed and analyzed. This is to ensure the correct output from the designed circuit can be determined. If simulation results are not correct, the circuit will be re-designed using different values of L, C and R. Table 3.2 shows the optimized parameters simulated in PSPICE.

Table 3.2: Simulation Parameters of SRBC for f_s: 1MHz

	CCM	DCM
Inductor, L	15 µH	1 µH
Capacitor, C	0.625 µF	9.375 µH
Resistor, R	3.5 Ω	4 Ω
MOSFET, S_1 & S_2	IRFP250	IRFP250
V_{in}	12 V	12 V

Figure 17 shows all the points of all parameters measured in PSPICE. First, the output voltage is checked to be 3 V or almost 3 V. Then, the voltage node is observed to make sure the correct voltage is produced as the input of 12 V. Then, the inductor current is observed whether it enters CCM or DCM mode. In addition, the peak and average of inductor currents are recorded. All results of conventional SRBC are tabled in Table 4.6.
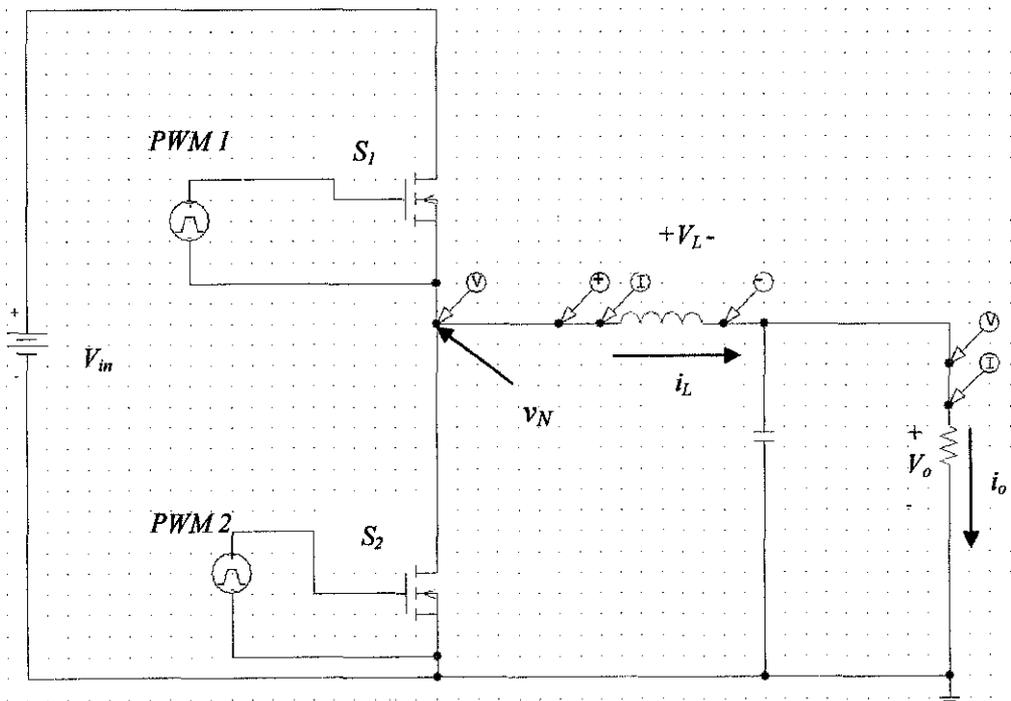
Figure 17: The points of all parameters measured in PSPICE

3.5   Analysis of results

In this step, all graphs and data are obtained from the PSPICE simulation. They are collected for the analysis purposes to meet the objectives of this project. The comparisons are based on the outputs characteristics, advantages and disadvantages of SRBC circuit. The evaluations refer to node voltage, inductor current output voltage and current waveform pattern of the SRBC, the power losses and also the ripple for both voltage and current. The analyses are based on two conditions: CCM and DCM. Lastly, the results of conventional SRBC are compared with the results of Adaptive Gated Drive (AGD) [25], AGD and compensator [25], MOSFET parallelism [26] and MPPT [27]. The comparisons are made to analyze the performance of the conventional SRBC circuit in term of the average output voltage $V_{o(avg)}$, average output current, i_{oavg}, average current ripple, i_o ripple peak-peak, average voltage ripple, V_o ripple peak-peak and body diode conduction loss, P_{BD}.

The average current ripple, i_o ripple peak-peak, average voltage ripple, V_o ripple peak-peak and body diode conduction loss, P_{BD} is given by Eq.(12) and Eq.(9):

$$V_O, i_o \ ripple \ peak - peak = \frac{peak - avrg}{avrg} \times 2 \times 100 \qquad (12)$$

3.6   Reporting

In this part, all the analysis and findings are then be written and compiled in a thesis and summarized in technical report.

3.7   Tools and Equipment Required

For the accomplishment of the project, there is a need for a certain software application especially for Modelling and Simulation process for my design project. In this project, I am required to model, design and simulate the circuit using PSPICE software which is Microsim Design Manager, Version 8.0. In addition, I also used OriginPro software, version 8.0 to plot the graphs.

CHAPTER 4

RESULT AND DISCUSSION

4.1 Chapter overview

The simulation results are comprehensively discussed which include the optimization of the parameters value and performance analysis of the circuit. The SRBC circuit is evaluated in terms of its output current, output voltage, voltage node, body diode conduction loss, voltage ripple and also current ripple. The analyses are divided into two conditions which are CCM and DCM. In addition, all results of the conventional SRBC will be compared with the result of SRBC using controller.

4.2 Optimization of parameters in SRBC

Based on the conventional SRBC shown in Figure 1, the limiting parameters to be measured are D, L, C and R. These parameters are determined using Eq. (5) until Eq. (8) and simulated using PSPICE software

4.2.1 Optimization of duty ratio, D
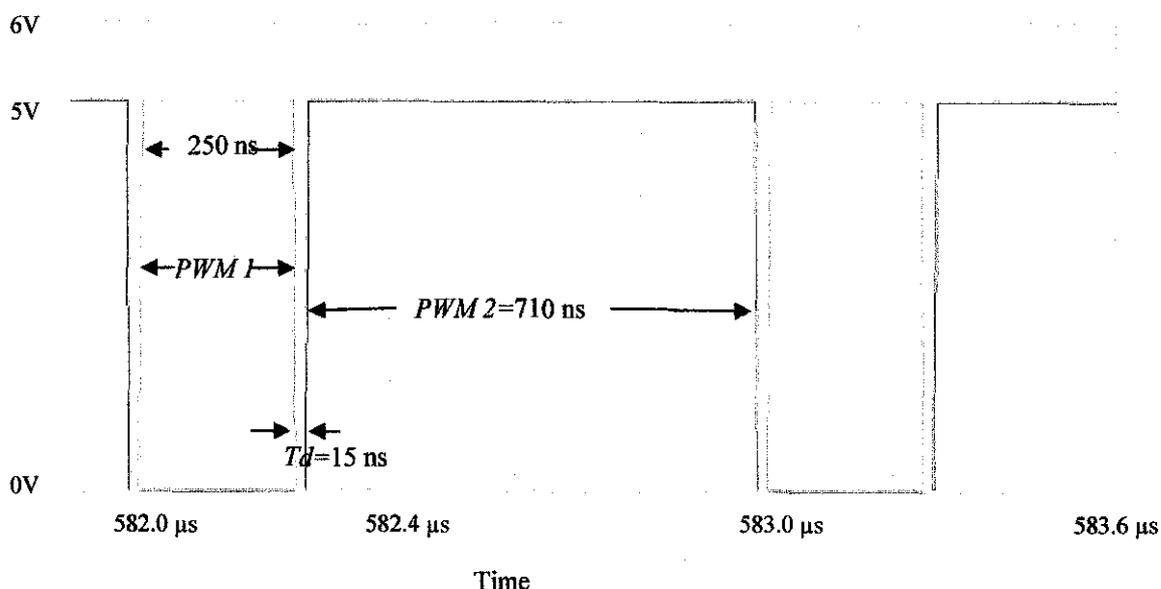
Figure 18: Indication of pulse width, dead time and delay time for S_1 and S_2
MOSFET for Td =15 ns.

The minimum D is required as it controls the output of the circuit. As shown in Figure 18, 250 ns pulse width of 1 MHz switching frequency indicates a portion of 25 % turn-on time from one cycle. The graph of Figure 18 is generated from the simulation of $Vgs,_{S1}$ and $Vgs,_{S2}$. 250 ns indicate the turn-on time of S_1 and 710 ns is the turn-on of S_2. The other settings of S_1 and S_2 are tabulated in Table 3.

Both S_1 and S_2 MOSFETs conduct complementarily of each other. The time when the both MOSFETs are not conducting is known as the dead time, Td. $PWM\ 1$ is the pulse width of S_1 and similarly is $PWM\ 2$ the pulse width of S_2. Td is set at the constant value of 15 ns indicating the delay time before S_2 starts to conduct. With this Td, the SRBC will not experience cross conduction loss when both of the switches are partially or fully turned on.

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4.2.2 Optimization of L, C and R

The dc-dc converters can be operated in two distinct modes which are CCM and DCM with respect to the inductor current i_L. It can be determined by looking at the lower peak of the inductor current.
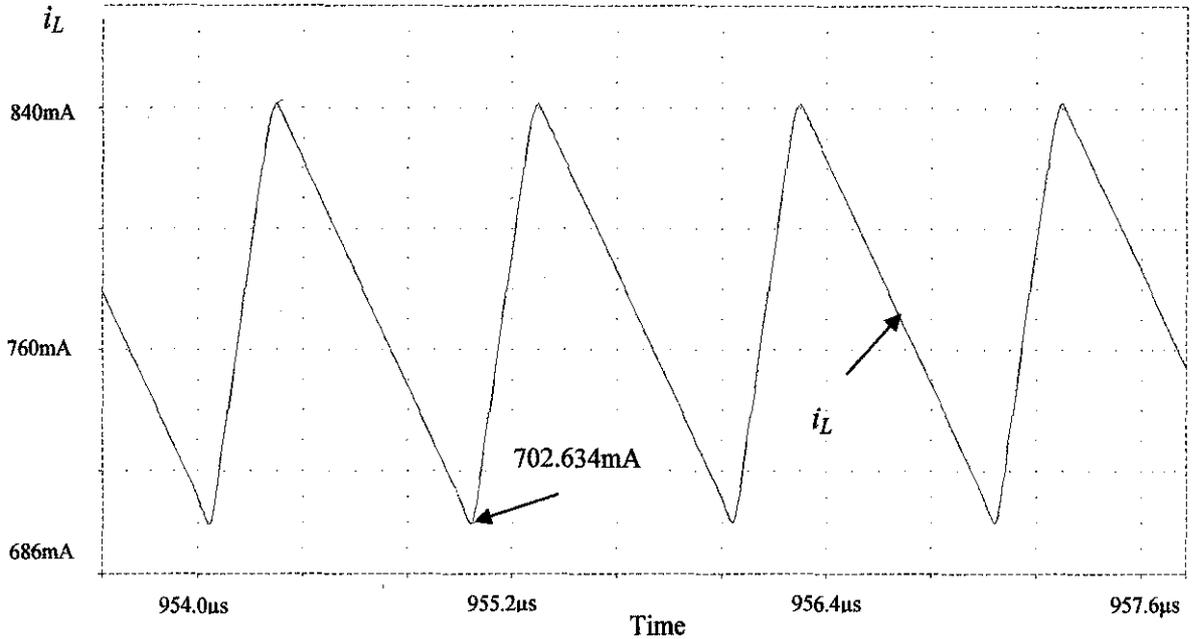
Figure 19: CCM with respect to inductor current i_L.

Figure 19 depicts the CCM in which inductor current is always greater than zero. In Figure 19, the lower peak of inductor current is 702.634 mA. This proves that the operation is in CCM. Meanwhile, Figure 20 shows the inductor current entering DCM as the lower peak indicates -333.001 mA which is below than zero.

The value of L, C and R can be determined using Eq. (5) until Eq. (8). For CCM, the value of L is fixed to 15 µH. Then using Eq. (6) C is equal to 0.625 µF and R of 3.5 Ω is chosen to maintain the value of the output voltage. For both conditions in CCM and DCM, the value of voltage ripple, ΔV_L is assumed to be 1% of the V_o, therefore $\Delta V_L = 0.03$ V. The same step is applied for DCM, and we get the value of 1 µH of L, 9.375 µF of C and R of 4 Ω.

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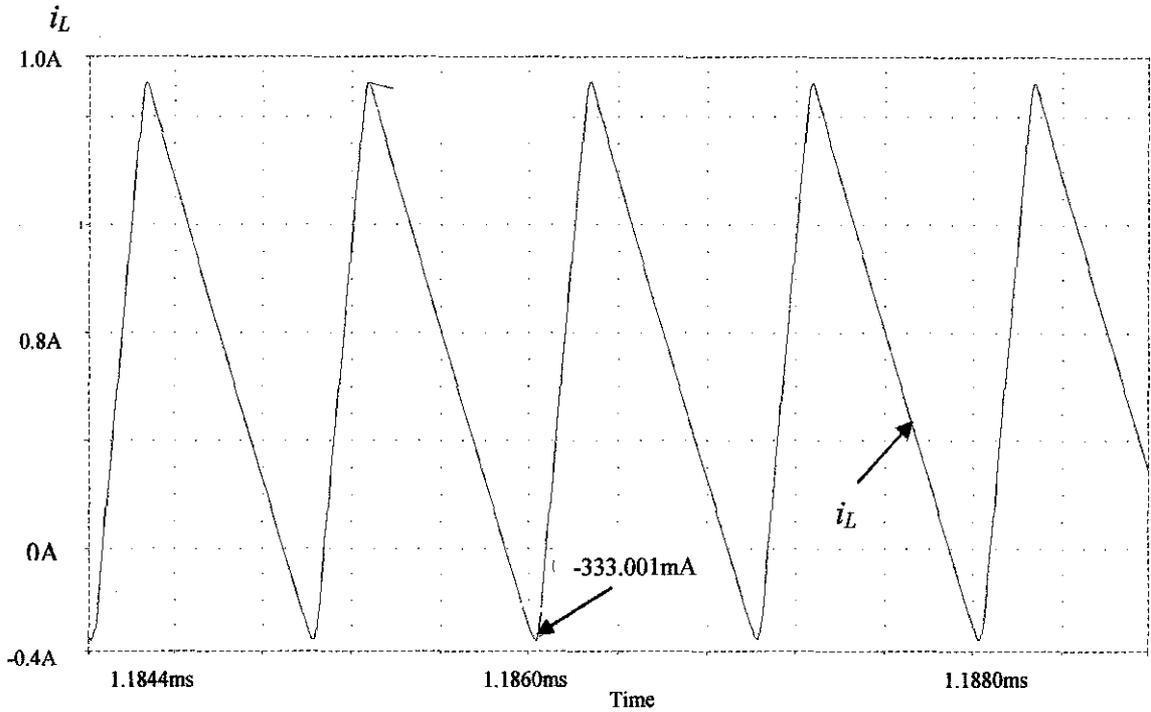
Figure 20: DCM with respect to inductor current i_L.

For SRBC, the value of L determines the boundary between CCM and DCM is given by Eq. (8). The inductor current i_L in CCM consists of a dc component i_o with superimposed triangular ac components. Current i_c causes a small voltage ripple across the dc output voltage, V_o. Therefore, to limit the peak-to-peak value of the ripple voltage below a certain value ΔV_L, C must be greater than as in Eq. (6).
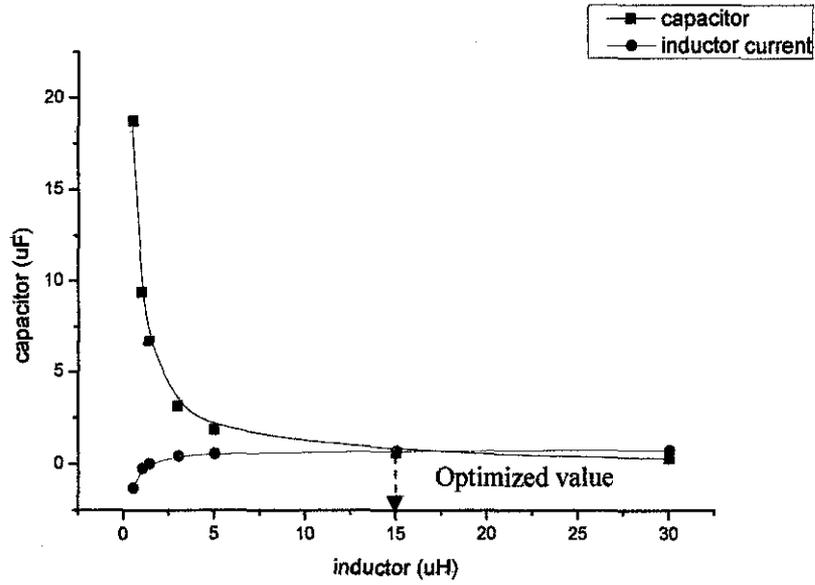
Figure 21: Graph of DCM vs CCM values at R=3.5 Ω

Table 4.1: Data of CCM and DCM values at R=3.5 Ω

L (μH)	C (μF)	i_L (A) at lower peak
0.5	18.75	-1.2965
1	9.375	-0.243
1.4	6.696	0.0194
3	3.125	0.4166
5	1.875	0.559
15	0.625	0.7026
30	0.3125	0.742

Figure 21 represents all data in Table 4.1. It shows that as L value goes smaller, i_L is going to negative region. The value of C depends on the value of L based on Eq. (6) and Eq. (8). Based on Table 4.1, we can see that it enters DCM when the value of L is smaller than C and vice versa for CCM. The highlighted region in Table 4.1 shows the optimized value for L and C for this circuit. The intersection in Figure 21 represents the optimized value for CCM. Both of these chosen values meet the objectives in producing high output voltage and output current.

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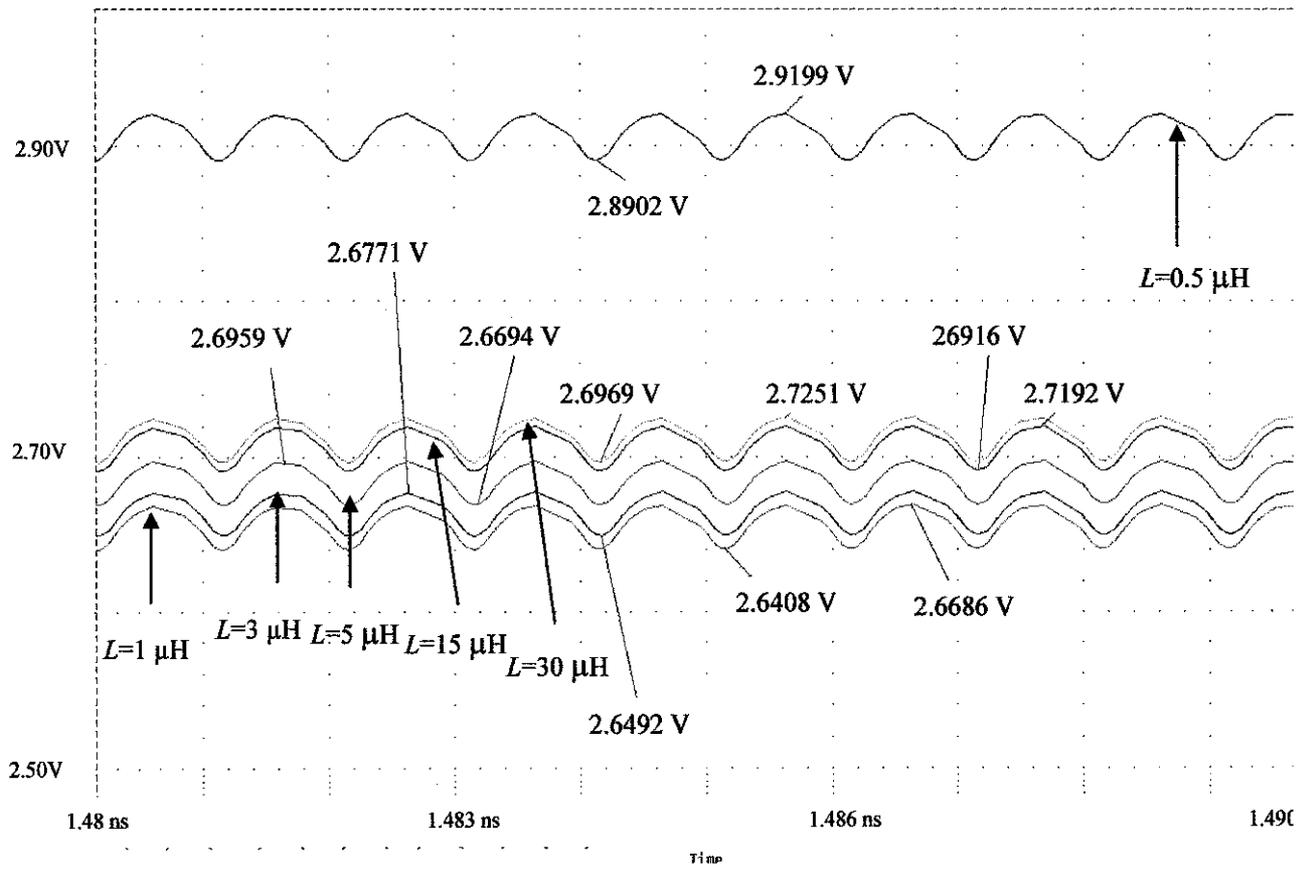
Figure 22: Output voltage at various values of inductor at R=3.5Ω
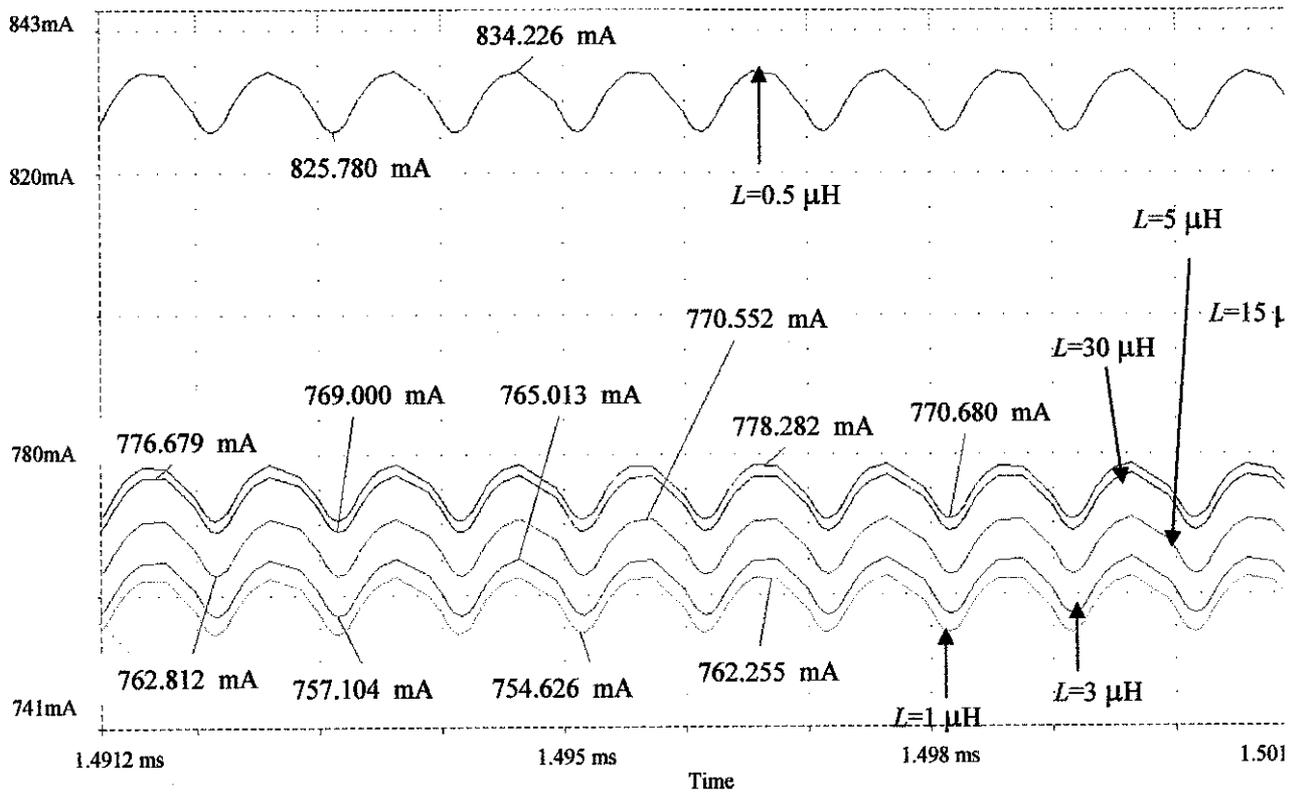
Figure 23: Output current of varies values of inductor at R=3.5Ω

Table 4.2: Average output voltage and output current for various values of

inductor at $R=3.5\Omega$

L (μH)	Average output voltage, (V) $V_O = [\frac{V_{upper\ peak} - V_{lower\ peak}}{2}]$	Average output current, (A) $i_o = [\frac{i_{upper\ peak} - i_{lower\ peak}}{2}]$
0.5	2.9	0.827
1	2.65	0.758
3	2.66	0.760
5	2.68	0.766
15	2.70	0.773
30	2.70	0.771

The summary of the average output voltage and current of Figure 22 and 23 are summarized in Table 4.2. Even though the average current and voltage for 0.5 μH is higher than the 1 μH of L, the optimized value of 1 μH is chosen for the boundary condition of DCM. Meanwhile for CCM, even though the average output voltage for 15 μH and 30 μH are the same, 15 μH of L is chosen as the optimized value since the value of the output current is higher than for 30 μH .

Based on Table 4.2, DCM average voltage is 2.65 V which is 10 % $[\frac{(3-2.65)V}{3} \times 100]$ from the actual value of 3 V. Hence, the value of the resistor needs to be increased as it controls the output voltage and current.
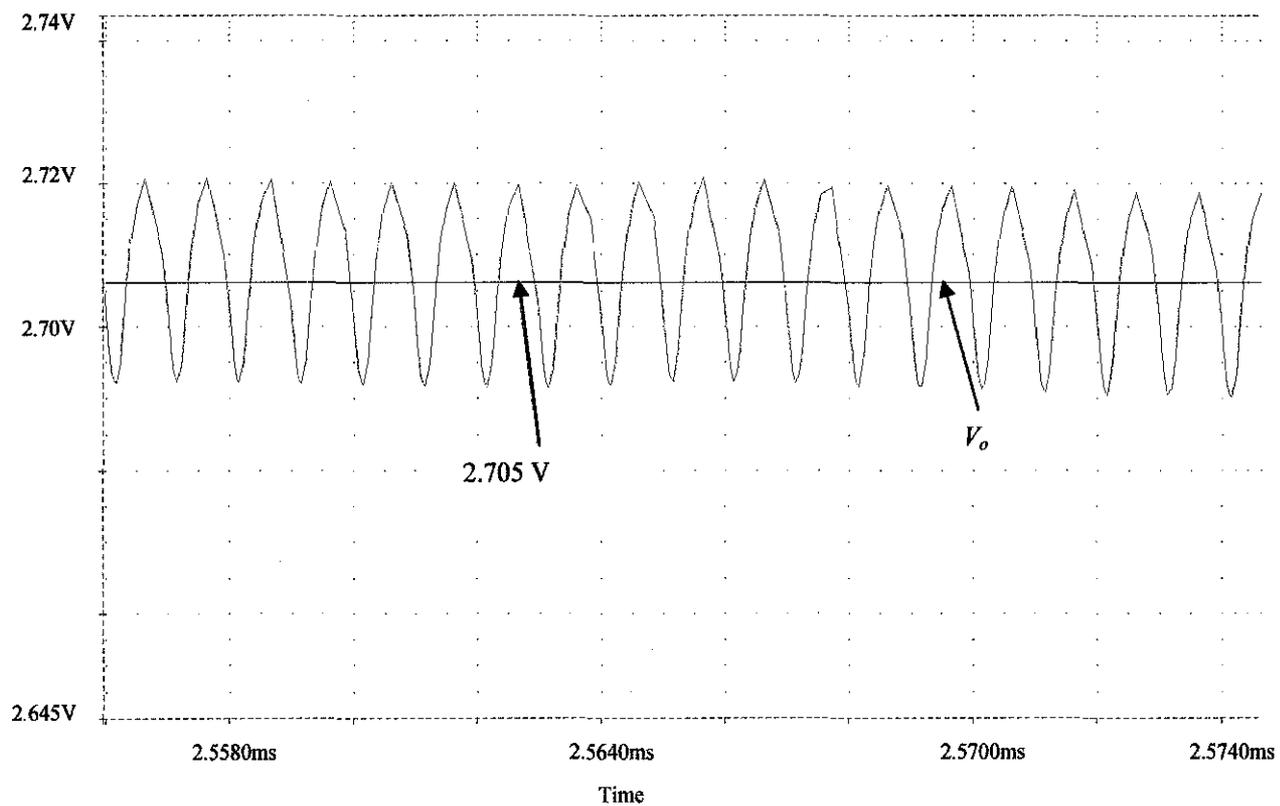
Figure 24: Output voltage of $L= 1$ μH at $R=4$ Ω for DCM
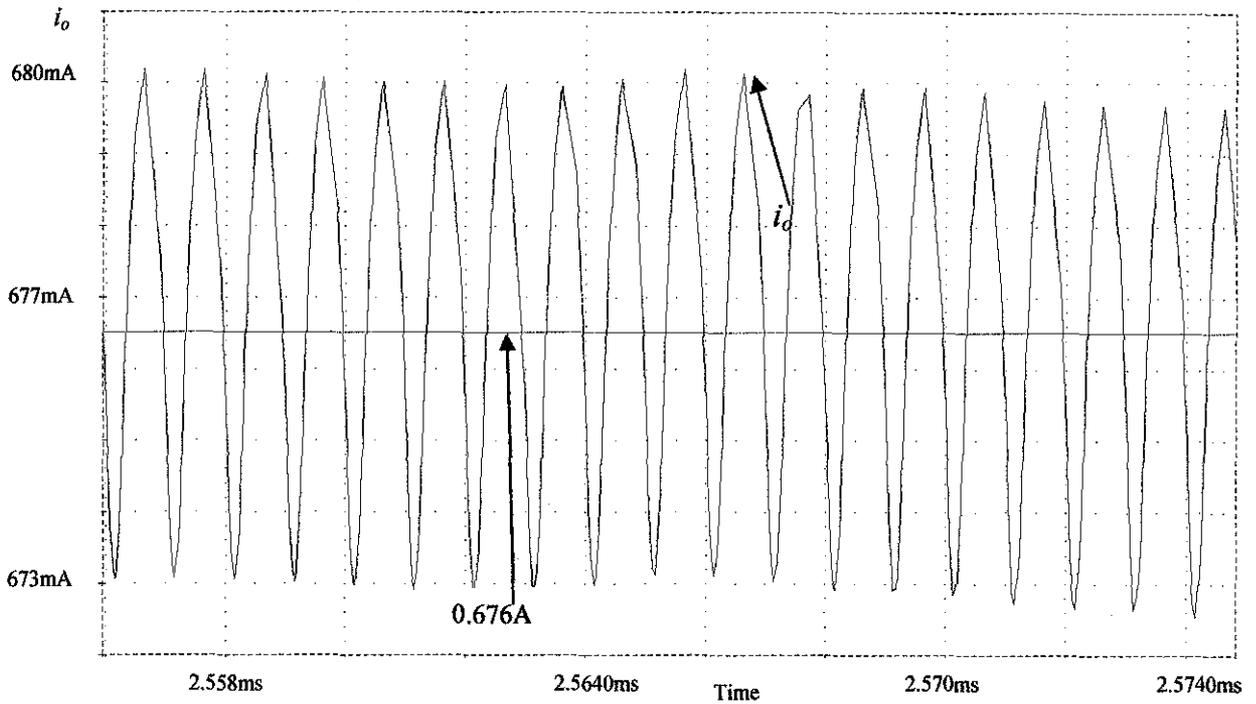
Figure 25: Output current of $L=1$ μH at $R=4$ Ω for DCM

Figure 24 and Figure 25 show the output current and output voltage for DCM when the resistor value is changed to 4 Ω. Hence, the value of voltage is also changed to 2.705 V as in Figure 24 but it gives impact on the average output current shown in Figure 25. The average output current drops to 0.676 A. It follows the Ohm's law which states that value of resistance is inversely proportional to the current. In SRBC, resistor acts as load. When the value of resistance is high, the average current produced is low and the converter may enter DCM.

Table 4.3: Values of resistor, average output current and voltage for CCM

Resistor (Ω)	Average output current (A)	Average output voltage (V)
3.0	0.85	2.60
3.5	0.77	2.70
4.0	0.66	2.80
5.0	0.55	2.90
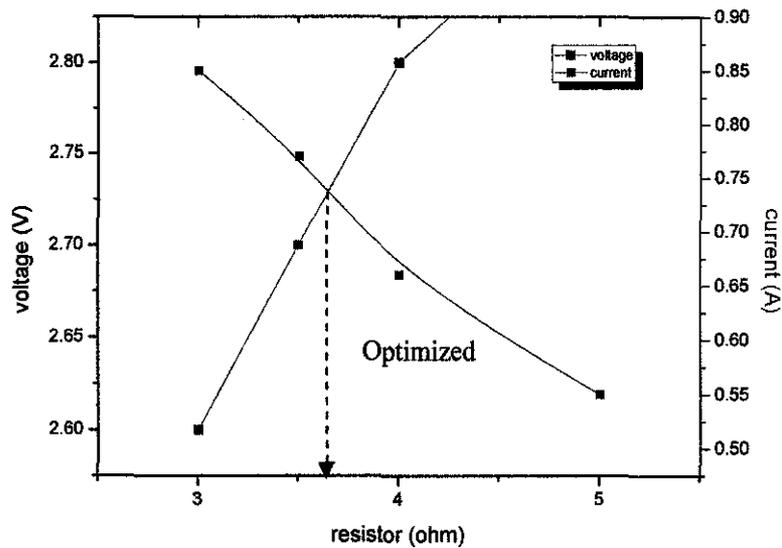
Figure 26: CCM intersection of optimized value

Table 4.3 and Figure 26 show the data and the graph of average output current and voltage at several resistor values. This is to find the optimized value of the resistor in CCM. As we can see in Figure 26, the intersection between the voltage and current is at resistor value of 3.6 Ω. The value of 3.6 Ω is not common. So, the value of 3.5 Ω is chosen as the optimized value in CCM instead of 4 Ω because the value of current and voltage at 3.5 Ω is higher than at 4 Ω.

Table 4.4: Values of Resistor, average output current and voltage for DCM

Resistor (Ω)	Average output current (A)	Average output voltage (V)
3.0	0.850	2.60
3.5	0.750	2.65
4.0	0.678	2.71
5.0	0.505	2.80
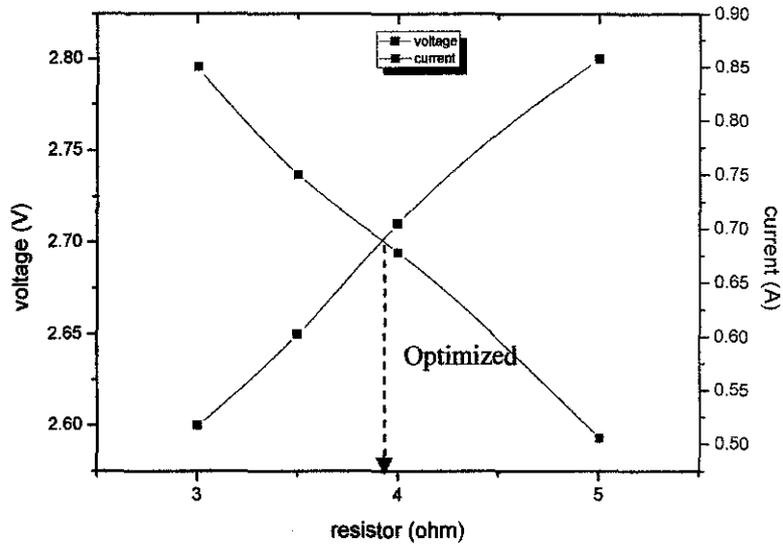
Figure 27: DCM intersection of optimized value

The graph of Figure 27 represents all data in Table 4.4 of DCM. Based on Figure 27, it shows that the intersection is at 3.95 Ω ≈ 4 Ω. This proves that 4 Ω is the optimized value of DCM.

The summary of the optimized values of all parameters for CCM and DCM are summarized in Table 4.5.

Table 4.5: Optimized parameters value for CCM and DCM

Parameters	CCM	DCM
Inductor, L	15 μH	1 μH
Capacitor, C	0.625 μF	9.375 μF
Resistor, R	3.5 Ω	4 Ω

4.2.3 Simulation results of optimized parameters of CCM
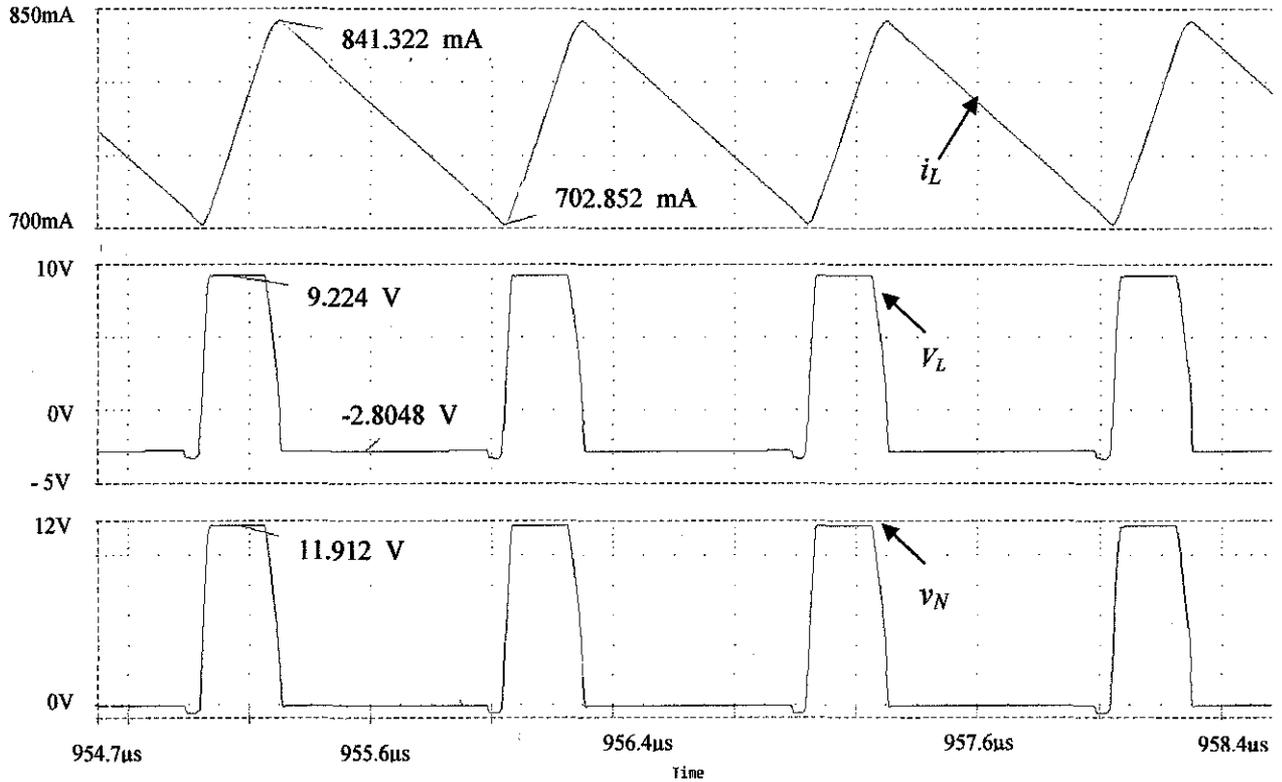
Figure 28: v_N, V_L, i_L of the SRBC for CCM

Figure 28 shows the node voltage, v_N, inductor voltage, V_L and current, i_L of SRBC in CCM where i_L is 702.852 mA . v_N is nearly equal to the input voltage, 12 V which is 11.912 V and hence the PWM signals that feed into the SRBC are correct. CCM is preferred for high performance and good utilization of semiconductor switches [22]. In this project, the SRBC is designed with a small value of the resistor which is 3.5 Ω in order to maintain the converter outputs. Meanwhile for inductor voltage, V_L is 9.224 V$\approx$9 V is almost equal to theory and V_L falls to -2.8048V where it is not sufficient to produce output voltage of 3 V.
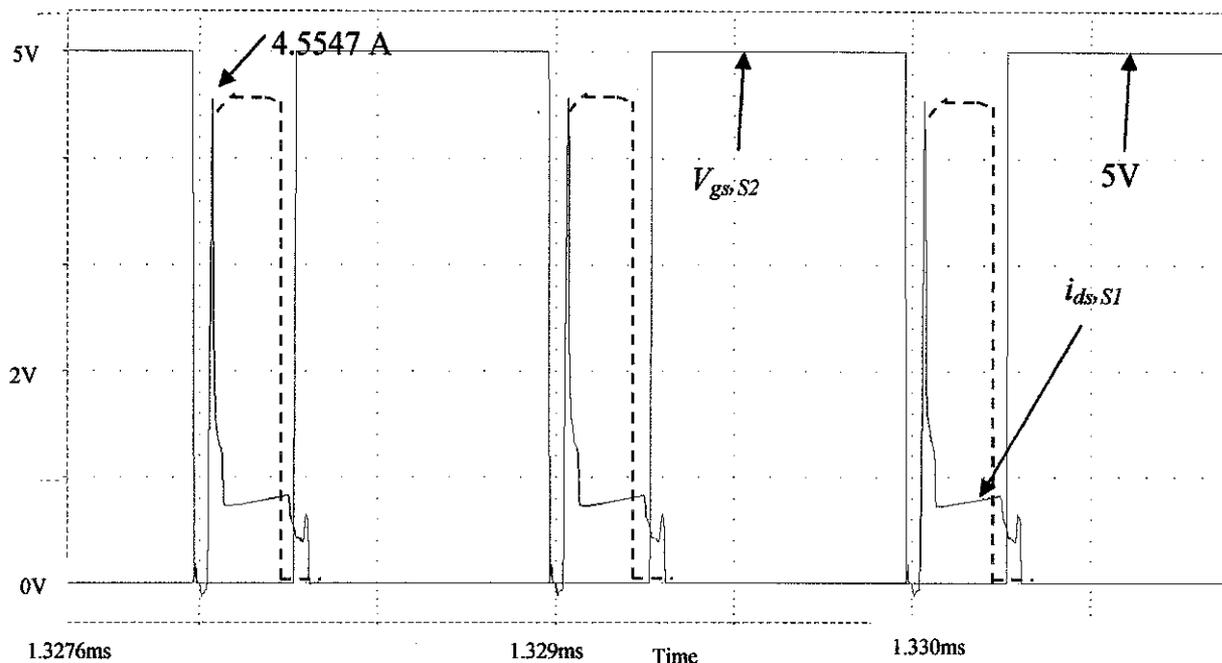
Figure 29: $V_{gs,S2}$ and $i_{ds,S1}$ for CCM

Figure 29 shows $V_{gs,S2}$ and $i_{ds,S1}$ for CCM condition. The drain current of S_1 in Figure 29 shows the charging operation during its turn-on. The i_{ds} charges fast to maximum after Td as S_1 turns on. The current, $i_{ds,S1}$ overshoots to 4.5547 A and then drops drastically. This causes current loss in the circuit since the correct current should be as red dotted line. This leakage current loss will flow to the body diode during Td. When $V_{gs,S2}$ is conducting, it shows that $i_{ds,S1}$ is discharged to zero as in Figure 29.
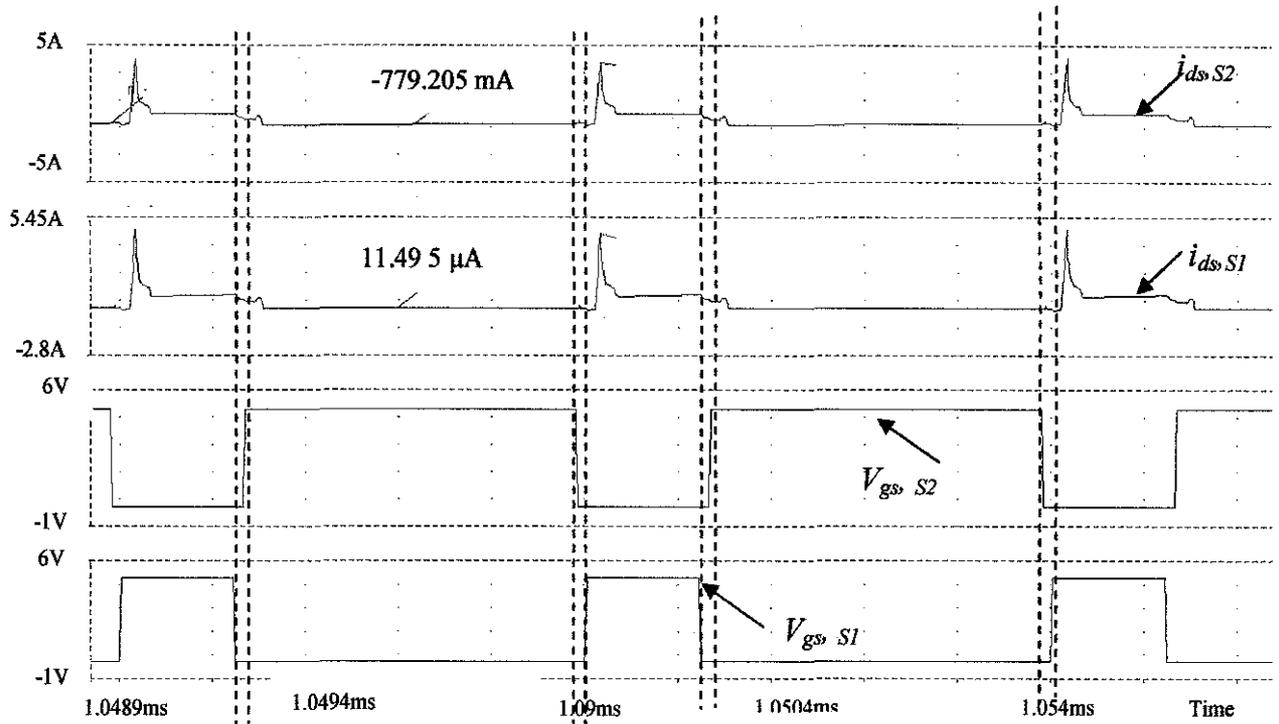
Figure 30: $V_{gs,S1}$, $V_{gs,S2}$, $i_{ds,S1}$ and $i_{ds,S2}$ of CCM

Figure 30 shows $V_{gs,S1}$, $V_{gs,S2}$, $i_{ds,S1}$ and $i_{ds,S2}$ of CCM. It clearly shows that $i_{ds,S2}$ will continue to discharge even though S_2 is already turned-off. Despite to the impact of loss portion in $i_{ds,S1}$ signal. The $i_{ds,S2}$ will continue flowing in S_2 body diode producing small amount of body diode conduction loss. When the S_1 is conducting, it shows that the current $i_{ds,S1}$ is fully discharged to ground as the value states is 11.495 μA $\approx$ 0. Meanwhile when S_2 is conducting, it shows in Figure 30 that the current $i_{ds,S2}$ is -779.205 mA indicates that the current is not fully discharged to ground.
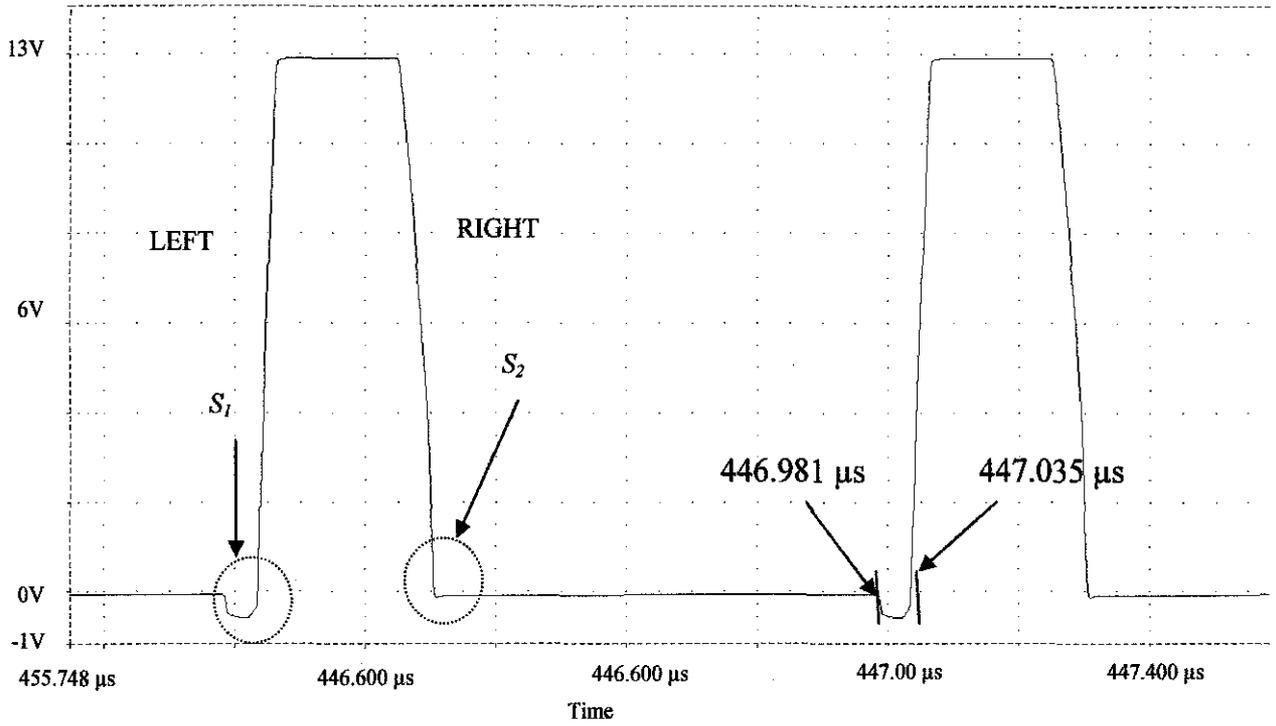
Figure 31: Node voltage, v_N of CCM

The body diode conduction loss is measured from node voltage, v_N as shown in Figure 31. The right side of node voltage shows the body diode of S_2 whereas at the left side is for S_1. S_2 body diode is turned on by circulating current that flows into L as soon as S_1 turns off. The period of the body diode conduction is related to Td. The longer Td is, the longer the body diode conduction period will be. This allows i_L to flow through body diode S_2 switch which degrades the overall performance since it contributes to loss. The result obtained shows the recovery time for node voltage is 0.054 us (447.035 µs - 446.981 µs) for S_1. Meanwhile for S_2, it is assumed there is no body diode conduction since the body diode conducts below -0.3 V.
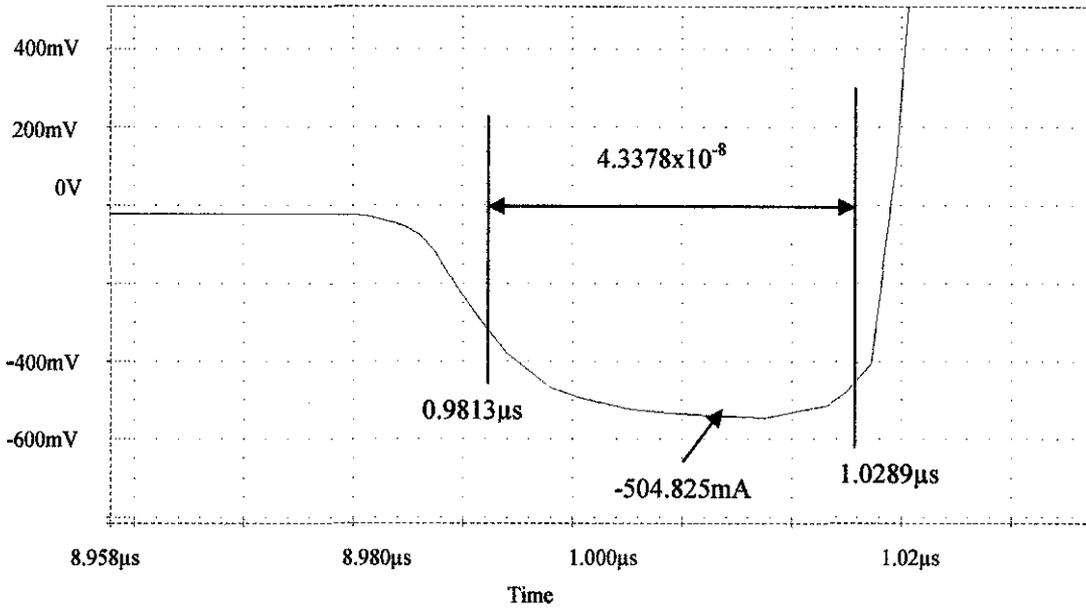
Figure 32: Body diode conduction for DCM

Figure 32 shows the body diode conduction for CCM. The body diode occurs during dead time, Td. Body diode conduction loss is one of the losses in the SRBC circuit. t_{BD} is 4.3378×10^{-8} s (1.0289 µs -0.9813 µs), i_o is 770.260 mA taken in Figure 33. Therefore, the amount of losses obtained is approximately 16.87 mW ($|-504.825$ mA$|$ x 770.260 mA x 1 MHz x 4.3378×10^{-8}) which is calculated using Eq. (12).
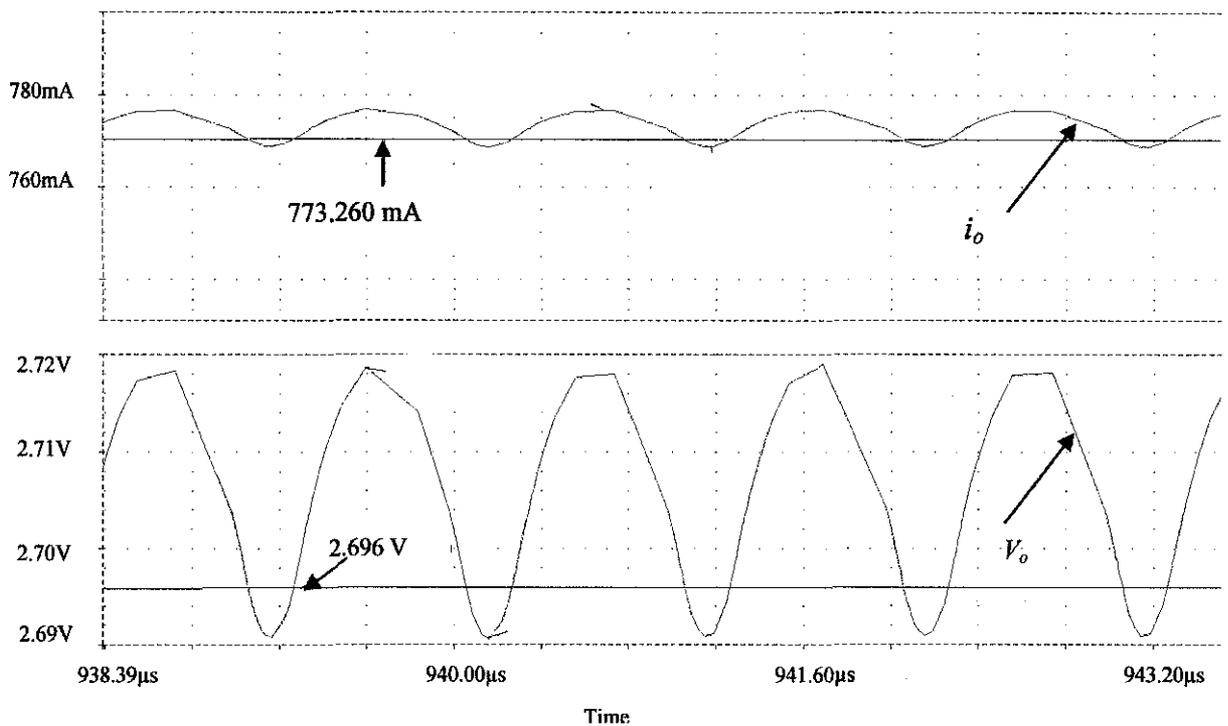
Figure 33: V_o and i_o of the SRBC for CCM

As in Figure 33, it shows that the output waveforms experience ripple. Hence, the average output voltage; V_o and i_o are taken into account. The average output voltage for SRBC is 2.696 V, which is slightly different from the theoretical value of 3 V. The Figure 14 also shows the average output current produced by this circuit is 773.260 mA where it is the maximum current produced by conventional SRBC for CCM. The average output current is lower than the value of inductor current which is 841.322 mA in Figure 28. This shows that some amount of current is consumed by the capacitor.

4.1.4 Simulation results of optimized parameters of DCM
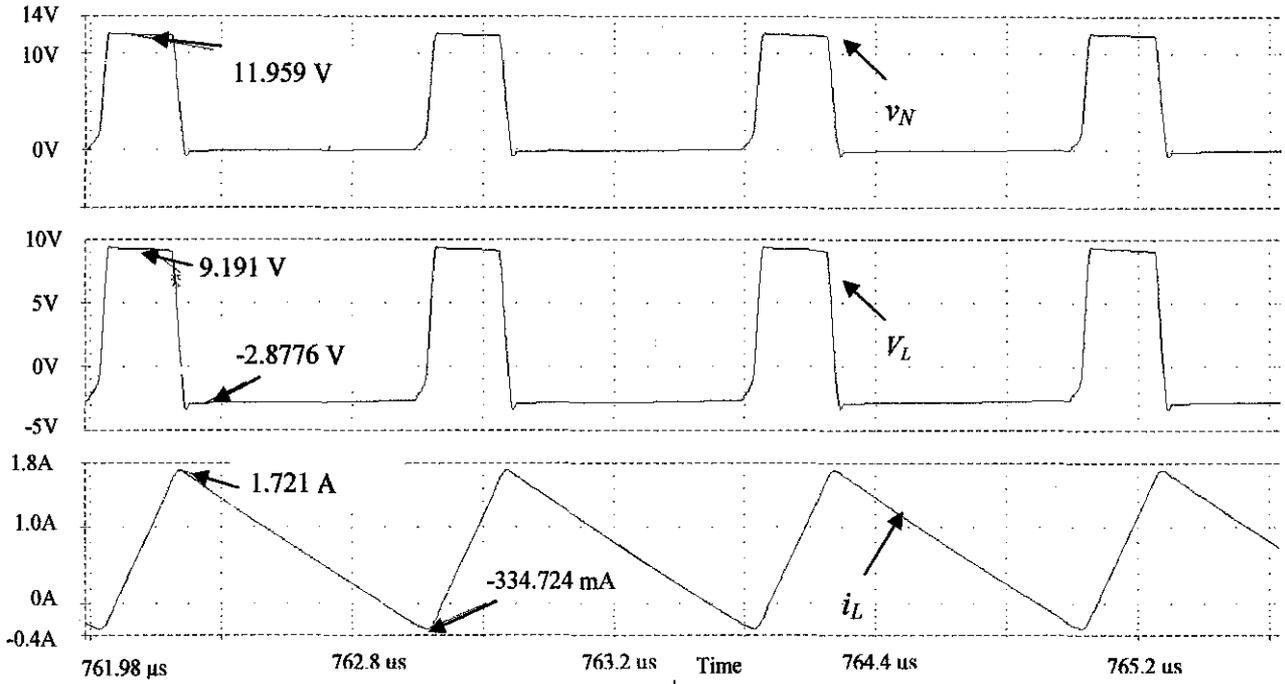
Figure 34: v_N, V_L, i_L of the SRBC for DCM

Figure 34 shows the node voltage, v_N, inductor voltage, V_L and current, i_L of SRBC in DCM. Node voltage controlled by PWM is correct since node voltage is 11.959 V $\approx$ 12 V. With 12 V input, the inductor voltage, V_L manages to get 9.191 V which means only 2.8776 V is transferred to the output resulting the output voltage not exactly 3 V. DCM which is defined by the inductor current, generates -332.724 mA at the lower peak shown in Figure 34. The DCM is chosen at the boundary because it can generate high current at i_L.

44
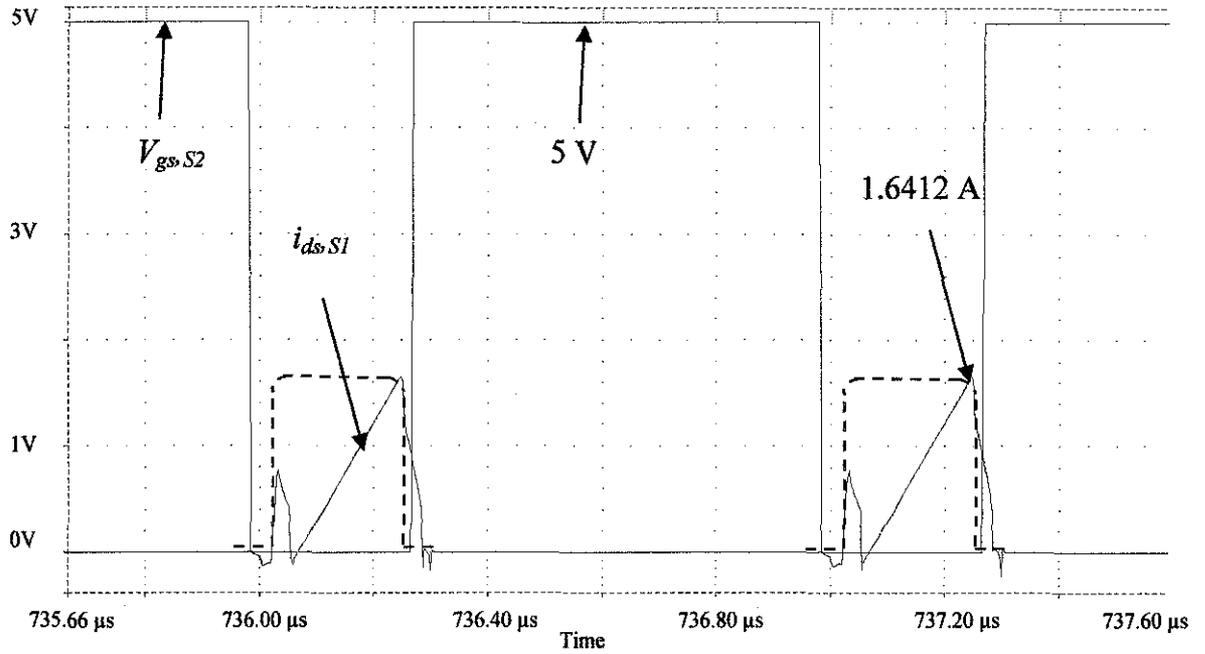
Figure 35 : $V_{gs,S2}$ and $i_{ds,S1}$ for DCM

Figure 35 shows $V_{gs,S2}$ and $i_{ds,S1}$ for DCM .The drain current of S_1 shows the charging operation during its turn on. The $i_{ds,S1}$ charges slow at the beginning and then it charges fast to maximum as S_1 turns on. The increase in switching speed causes overshoot current to 1.6412 A. This causes losses and this current flows to the body diode of both switches leading to small loss in body diode conduction during Td [4]. The dotted line represents the correct waveform of $i_{ds,S1}$.
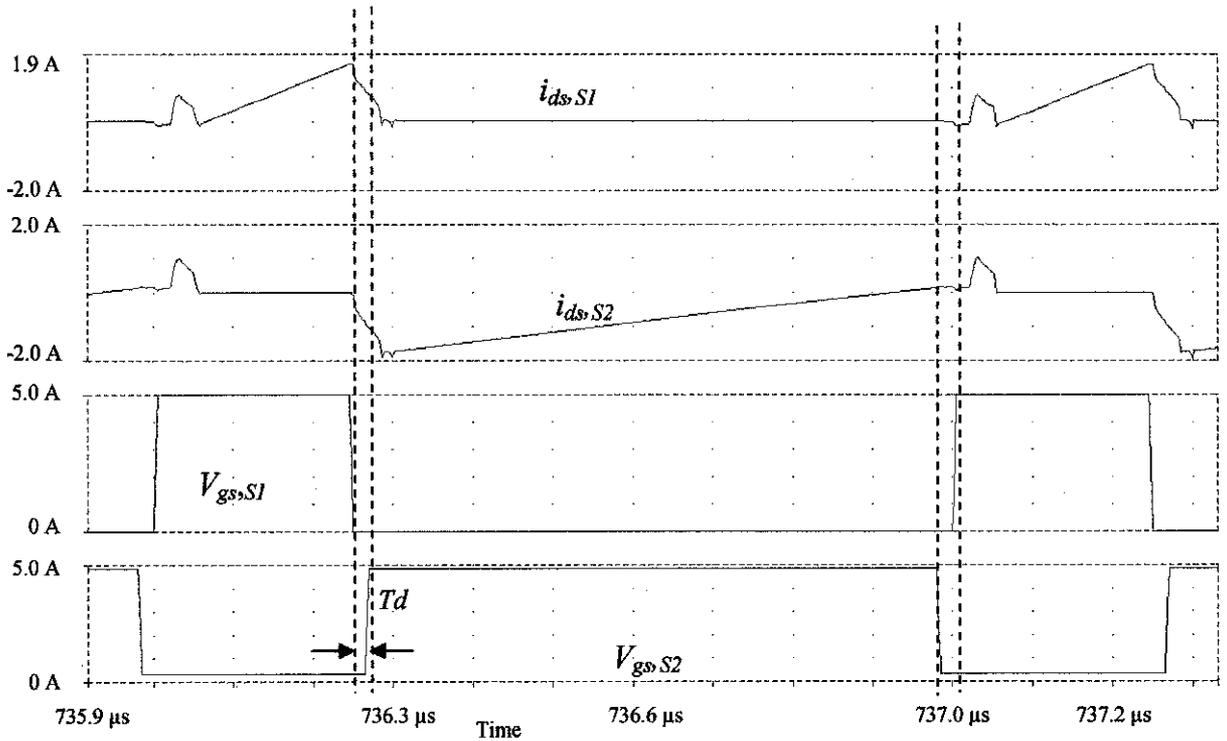
Figure 36: $V_{gs,S1}$, $V_{gs,S2}$, $i_{ds,S1}$ and $i_{ds,S2}$ of DCM

Figure 36 shows $V_{gs,S1}$, $V_{gs,S2}$, $i_{ds,S1}$ and $i_{ds,S2}$ of DCM. It proves that $i_{ds,S2}$ will continue to discharge even though S_2 is already turned off. Despite to the impact of loss portion in $i_{ds,S1}$ signal, the $i_{ds,S2}$ will continue flowing in S_2 body diode producing small amount of body diode conduction loss as Figure 38. When the S_2 is conducting, the current is not fully discharged to ground.
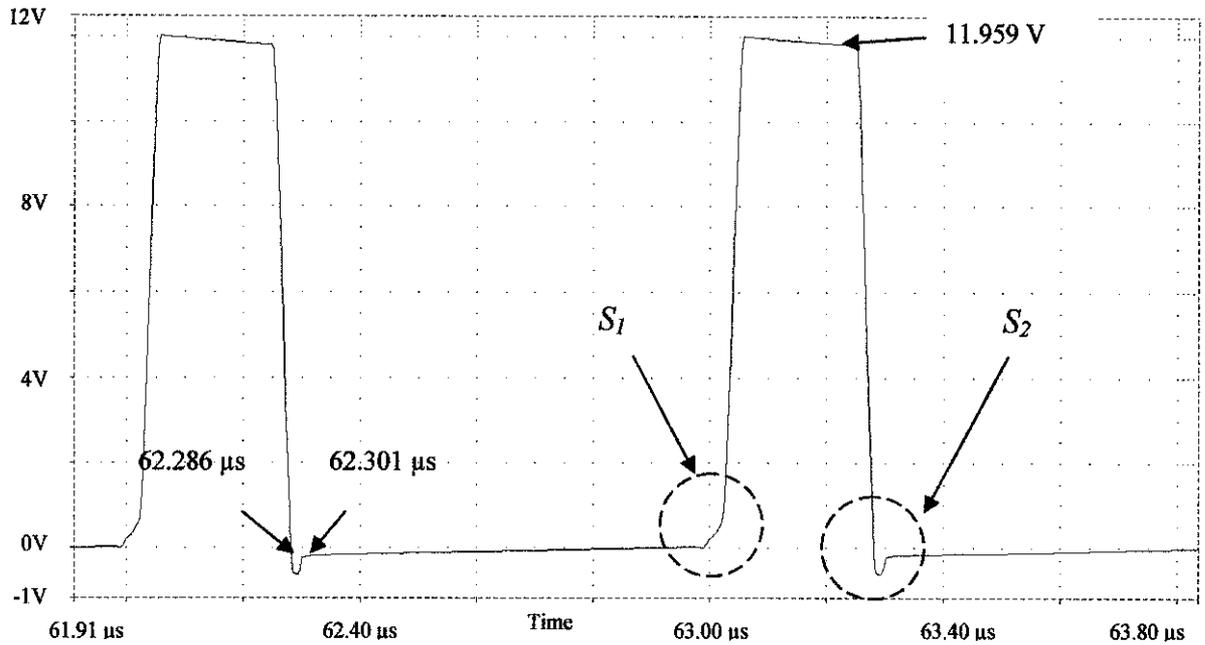
Figure 37: Node voltage, v_N of DCM

Figure 37 shows the peak voltage of node voltage is 11.959 V where it is approximated to be closed to 12 V input voltage. But it experiences losses as the slope of the graph differs from the theory. These losses of voltage node are related to the MOSFET switch and the value of the inductor and capacitor .When the value of the capacitor is larger than inductor, the capacitor tends to store larger amount of voltage. S_2 experiences body diode conduction loss of 15 ns (62.301 μs - 062.286 μs) which is the same as Td. On the other hand, S_1 is free from body diode conduction loss.
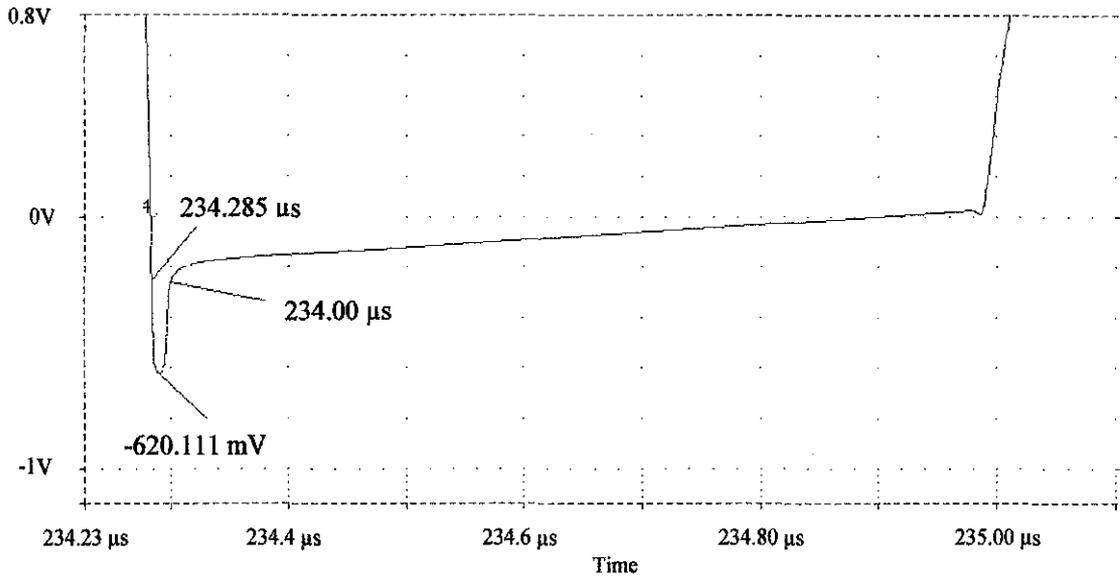
Figure 38: Body diode conduction for DCM

Body diode conduction for DCM as shown in Figure 38 contributes the losses in the circuit. The t_{BD} is equal to 1.5×10^{-8} s (234.00 µs -234.285 µs) and the i_o is 676.129 mA taken in Figure 39. Substituting into Eq. (12), the body diode conduction of DCM is 6.29 mW (|-620.111 mA| $\times$ 1.5×10^{-8} s $\times$ 676.129 mA $\times$ 1MHz). The body diode conduction occurs during the Td when S_1 is fully turned off. When the lower peak is below than -0.3 V, there is possibility the current flow back to the switch.
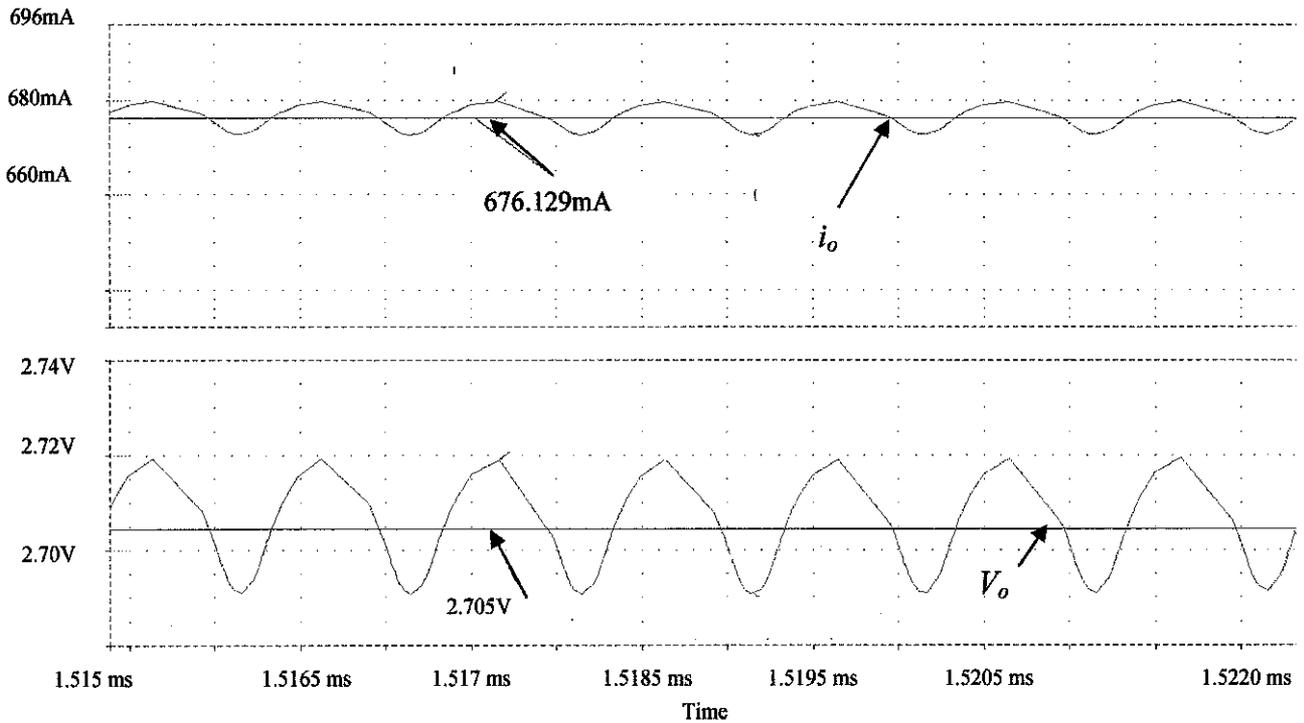
Figure 39 : V_o and i_o of the SRBC for DCM

As shown in Figure 39 above, the ripple causes the output waveforms to be inconsistent. The average output voltage for DCM is 2.705 V, which is slightly 10 % $\left[\frac{3-2.705}{3}\times100\right]$ in difference from the theoretical value of 3 V. Figure 39 above also shows the average output current produced by this circuit is 676.129 mA where it is the maximum current produced by conventional SRBC for DCM. Even though the inductor current produced is high of 1.7212 A, the output current drops drastically because of the value of the capacitor is larger than the inductor value.

Summary of results for both CCM and DCM are recorded in the Table 4.6 below.

Table 4.6: Summary of results for Conventional SRBC

	CCM	DCM
Node voltage, v_N	11.912 V	11.959 V
Peak Inductor Voltage, V_L	9.224 V	9.191 V
Peak Inductor Current, i_L	841.322 mA	1.721 A
Average Output Voltage, V_o	2.696 V	2.705 V
Average Output Current, i_o	773.260 mA	676.129 mA

4.2 Comparative Assessment

The comparison between Conventional SRBC with Adaptive Gate Drive (AGD), Compensator and AGD, MOSFET Parallelism and Maximum Power point tracking (MPPT) are carried out on the performance of the circuit. All results of the circuits are taken from [25], [26] and [27] which are shown in Appendices.

4.2.1 Comparison between Conventional SRBC and AGD control scheme

Table 4.7: comparison of Conventional SRBC and AGD control scheme for CCM

CCM			
	Conventional SRBC	AGD [25]	% improvement of Conventional SRBC to AGD
$V_{o(avg)}$, (V)	2.70	2.68	0.74
i_{oavg}, (mA)	770.26	765.76	0.58
V_o ripple peak-peak (%)	1.66	2.23	25.56
i_o ripple peak-peak (%)	1.62	2.21	26.70
P_{BD} (mW)	16.87	20.79	18.86

Table 4.7 shows the results of Conventional SRBC and AGD for CCM. I can conclude that the performance of Conventional SRBC is better compared to AGD. In the Conventional SRBC, the average voltage and current have increased by 0.74 % and 0.58 % respectively. In designing the circuit, the ripple should be smaller as it affects the performance of the circuit. In this case, ripple voltage and current of the Conventional SRBC are lowered by 25.56 % and 26.70 % of AGD respectively. Furthermore, for the body diode conduction of Conventional SRBC gives a difference of 18.86 % compared to AGD. Therefore, for overall performance of CCM between Conventional SRBC and AGD, it has proves that Conventional SRBC gives better performance in all aspects compared to AGD.

Table 4.8: Comparison of Conventional SRBC and AGD control scheme for DCM

DCM			
	Conventional SRBC	AGD [25]	% improvement of Conventional SRBC to AGD
$V_{o(avg)}$, (V)	2.70	2.68	0.74
i_{oavg} (mA)	676.13	670.60	0.82
V_o ripple peak-peak (%)	1.02	1.65	38.18
i_o ripple peak-peak (%)	1.06	1.62	34.56
P_{BD} (mW)	6.29	4.63	-35.85

For DCM condition between Conventional SRBC and AGD in Table 4.8, the average voltage and current of Conventional SRBC are 0.74 % and 0.82 % higher than AGD. Meanwhile, for the ripple voltage and current of Conventional SRBC are also higher than AGD by 38.18 % and 34.56 % respectively. But, the body conduction loss between the Conventional SRBC and AGD experiences reduction of 35.85 %. It can be concluded that, in DCM operation, the average and ripple voltage and current of Conventional SRBC are better than AGD. However, body diode conduction loss is high.

4.2.2   Conventional SRBC and Compensator and AGD

Table 4.9: Comparison of Conventional SRBC and Compensator and AGD for CCM

CCM			
	Conventional SRBC	Compensator and AGD [25]	% improvement of Conventional SRBC to Compensator and AGD
$V_{o(avg)}$ (V)	2.70	2.99	-9.70
i_{oavg} (mA)	770.26	853.77	-9.78
$V_{o\ ripple\ peak-peak}$ (%)	1.66	2.10	20.95
$i_{o\ ripple\ peak-peak}$ (%)	1.62	2.08	22.12
P_{BD} (mW)	16.87	0.00	-100.00

Table 4.9 shows the comparison of Conventional SRBC and Compensator and AGD for CCM. The results in Table 8 show 9.70 %   improvement of voltage of the Compensator and AGD. Similiarly goes to the average current of Compensator and AGD where they have increased by 9.78 %. In contrast, for ripple voltage and current, the Compensator and AGD give higher ripple of 20.95 % and 22.12 % which may affect the circuit performance. In term of body diode conduction, there is zero body diode conduction loss for Compensator and AGD which minimizes the losses of the circuit

Table 4.10: Comparison of Conventional SRBC and Compensator and AGD for DCM

DCM			
	Conventional SRBC	Compensator and AGD [25]	% improvement of Conventional SRBC to Compensator and AGD
$V_{o(avg)}$ (V)	2.70	2.99	-9.70
i_{oavg} (mA)	676.13	748.86	-9.71
$V_{o\ ripple\ peak-peak}$ (%)	1.02	3.48	70.69
$i_{o\ ripple\ peak-peak}$ (%)	1.06	3.41	68.91
P_{BD} (mW)	6.29	0.00	-100.00

Table 4.10 shows the comparison between the Conventional SRBC and Compensator and AGD for DCM. The Compensator and AGD gives improvement of 9.70 % and 9.71 % than Conventional SRBC for average output

voltage and current respectively. Meanwhile the Compensator and AGD generates high ripple voltage and current of 70.69 % and 68.91 % compared to Conventional SRBC. Compensator and AGD gives better results of body diode conduction loss which is zero compared to conventional SRBC.

4.2.3 Conventional SRBC and MOSFET Parallelism

Table 4.11: Comparison of Conventional SRBC and MOSFET Parallelism for CCM

CCM			
	Conventional SRBC	MOSFET Parallelism [26]	% improvement of Conventional SRBC to MOSFET Parallelism
$V_{o(avg)}$ (V)	2.70	2.69	0.37
i_{oavg} (mA)	770.26	863.84	-10.83
V_{o} ripple peak-peak (%)	1.66	1.86	10.75
i_{o} ripple peak-peak (%)	1.62	2.36	31.36
P_{BD} (mW)	16.87	10.70	-57.66

Comparison between Conventional SRBC and MOSFET Parallelism for CCM is shows in Table 4.11. MOSFET parallelism experiences reduction of 0.37 % in average output voltage compared to Conventional SRBC but it gives improvement of 10.83 % of average output current. Besides that, MOSFET parallelism has higher voltage ripple and current which are 10.75 % and 31.36 % with the reduction of 57.66 % of body diode conduction loss compared to Conventional SRBC. This shows MOSFET parallelism has minimized the losses in the circuit.

Table 4.12: Comparison of Conventional SRBC and MOSFET Parallelism for DCM

DCM			
	Conventional SRBC	MOSFET Parallelism [26]	% improvement of Conventional SRBC to MOSFET Parallelism
$V_{o(avg)}$ (V)	2.70	2.74	-1.46
i_{oavg} (mA)	676.13	758.52	-10.86
V_{o} ripple peak-peak (%)	1.02	1.34	23.88
i_{o} ripple peak-peak (%)	1.06	1.00	-6.00
P_{BD} (mW)	6.29	0.00	-100.00

Table 4.12 shows the comparison of Conventional SRBC and MOSFET parallelism in DCM. I can see that MOSFET parallelism gives improvement in term of average voltage, average current, current ripple and body diode conduction loss which are 1.46 %, 10.86 %, 6 % and 100 % respectively. But, it gives drawbacks of voltage ripple with an increase of 23.88 % when MOSFET parallelism is implemented to SRBC circuit.

4.2.4 Conventional SRBC and Maximum Power Point Tracking (MPPT) control scheme

Table 4.13: Comparison of Conventional SRBC and MPPT for CCM

CCM			
	Conventional SRBC	MPPT [27]	% improvement of Conventional SRBC to MPPT
$V_{o(avg),}$ (V)	2.70	3.09	-12.62
$i_{oavg,}$ (mA)	770.26	882.27	-12.70
$V_{o \text{ ripple peak-peak}}$ (%)	1.66	0.95	-74.74
$i_{o \text{ ripple peak-peak}}$ (%)	1.62	0.95	-70.53
P_{BD} (mW)	16.87	0.00	-100.00

Comparison between Conventional SRBC and MPPT for CCM is shown in Table 4.13. It shows that MPPT contributes better performance as the results are better than the Conventional SRBC. Average voltage and current give improvement of 12.62 % and 12.70 % and it lowers the value of ripple voltage and current by 74.74 % and 70.53 % compared to Conventional SRBC. In addition, body diode conduction loss for MPPT is zero which is 100 % better than the Conventional SRBC. This proves that for CCM, MPPT gives better performance than Conventional SRBC in all aspects.

Table 4.14: Comparison of Conventional SRBC and MPPT DCM

DCM			
	Conventional SRBC	MPPT [25]	% improvement of Conventional SRBC to MPPT
$V_{o(avg)}$, (V)	2.70	3.11	13.18
i_{oavg}, (mA)	676.13	777.81	13.07
V_{o} ripple peak-peak (%)	1.02	1.35	24.44
i_{o} ripple peak-peak (%)	1.06	1.35	21.48
P_{BD} (mW)	6.29	0.00	-100.00

For DCM, the comparison between Conventional SRBC and MPPT is shown in Table 4.14. For DCM, MPPT results in higher voltage ripple and current than Conventional SRBC which are 24.44 % and 21.48 % respectively. The average output voltage and current gives improvement of 13.18 % and 13.07 % compared to Conventional SRBC. In addition, the body diode conduction loss of MPPT has reduced to zero that is much better than Conventional SRBC. I can conclude that the performance of MPPT is only affected by its ripple voltage and current. All other results of the controllers are summarized in the Table 4.15.

Table 4.15: Summary of Conventional SRBC, AGD, Compensator and AGD, MOSFET Parallelism and MPPT for CCM ad DCM

	CCM				
	Conventional SRBC	AGD [25]	Compensator and AGD [25]	MOSFET Parallelism [26]	MPPT [27]
$V_{o(avg)}$ (V)	2.70	2.68	2.99	2.69	3.09
i_{oavg} (mA)	770.26	765.76	853.77	863.84	882.27
V_o ripple peak-peak (%)	1.66	2.23	2.10	1.86	0.95
i_o ripple peak-peak (%)	1.62	2.21	2.08	2.36	0.95
P_{BD} (mW)	16.87	20.79	0.00	10.70	0.00

	DCM				
	Conventional SRBC	AGD [25]	Compensator and AGD [25]	MOSFET Parallelism [26]	MPPT [27]
$V_{o(avg)}$ (V)	2.70	2.68	2.99	2.7362	3.11
i_{oavg} (mA)	676.13	670.60	748.86	758.52	777.81
V_o ripple peak-peak (%)	1.02	1.65	3.48	1.34	1.35
i_o ripple peak-peak (%)	1.06	1.62	3.41	1.00	1.35
P_{BD} (mW)	6.29	4.63	0.00	0.00	0.0

CHAPTER 5

CONCLUSION AND RECOMMENDATION

5.1 Conclusion

In conclusion, the simulation work is performed to illustrate the performance of Synchronous Rectifier Buck Converter (SRBC). In addition, the relationship among the inductor, resistor and capacitor in the SRBC circuit is important in order to obtain the best values. Therefore, studies of the relationship among these parameters are carried out in order to improve the design of SRBC and the results gained have been discussed completely. The study of the parameters will help in designing the circuit and this will give big impact to the technology development in producing more efficient SRBC in the industry. The comparison between the conventional SRBC shows how far the performance of the Conventional SRBC to the application can achieved when it is not connected to a controller.

Based on the results, it is found that the Conventional SRBC has advantages and drawbacks in the design. For CCM condition, it proves that the circuit produces high output voltage and current but gives high ripple peak to peak voltage and current which contributes losses in the circuit. As for DCM condition, it gives low output voltage and current but the peak to peak ripple voltage and current are low which help minimize the losses in circuit design. Therefore, the CCM condition can be used for application with high output voltage and current whereas the applications that consider losses in the circuit design, DCM condition is suitable to be used.

As for comparison between Conventional SRBC with the others controller, it shows that comparison between the Conventional SRBC with AGD shows that Conventional SRBC gives the best outputs in CCM and DCM, AGD only improves in minimizing the body diode conduction loss, P_{BD}. Meanwhile for Conventional SRBC versus Compensator with AGD, Conventional SRBC results in low voltage and current peak-to-peak in both CCM and DCM. Conventional SRBC is compared with MOSFET parallelism in CCM which shows improvement in producing improvement in average output current and minimizes the body diode conduction loss, P_{BD} while in DCM, Conventional SRBC only be able to give lower ripple peak-to-peak current. Lastly, for comparison between Conventional SRBC with MPPT, it shows that MPPT controller results in better improvement in all criteria in CCM but in DCM, it produces high voltage and current peak-to-peak ripple. Therefore, this shows that the MPPT controller is the best among all others controller.

5.2   Recommendation

Throughout this project, I am able to understand and know how to determine the parameters in the SRBC circuit using the correct equations. For future enhancement, it is recommended that the prototype is made in order to compare the experimental and simulation work.

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APPENDICES

APPENDIX A-1: AGD [25]
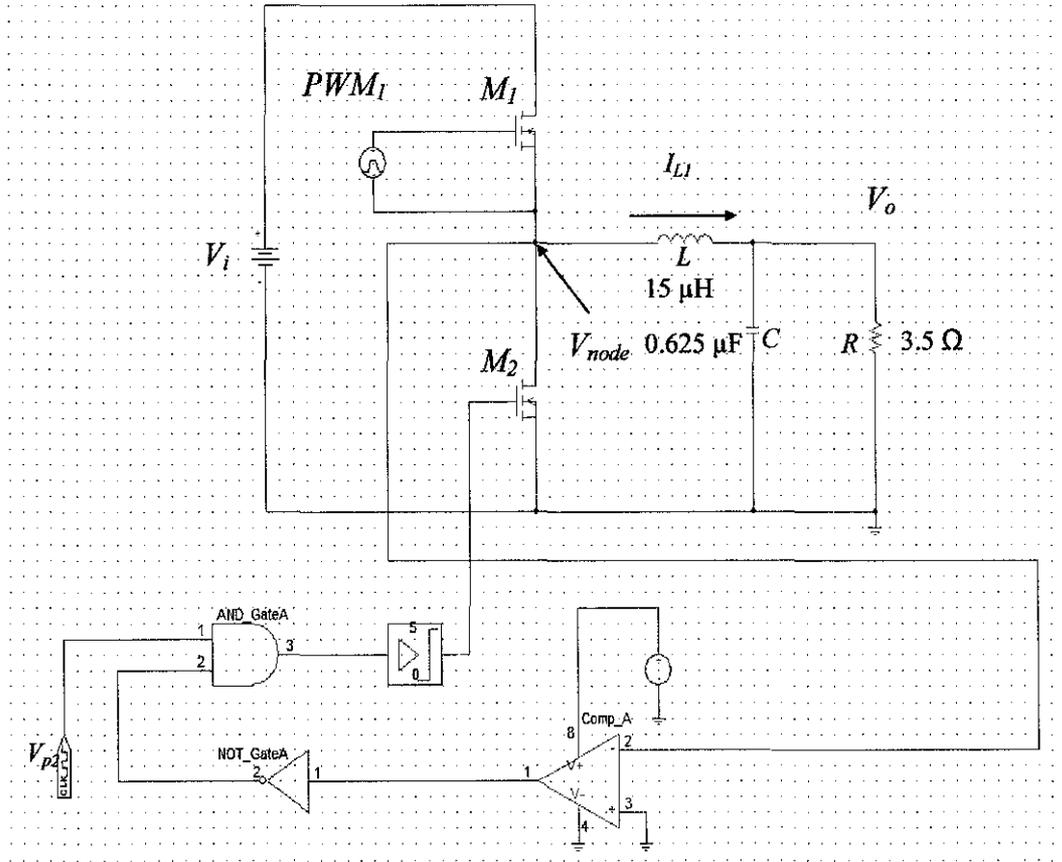
Figure 40: AGD circuit for CCM
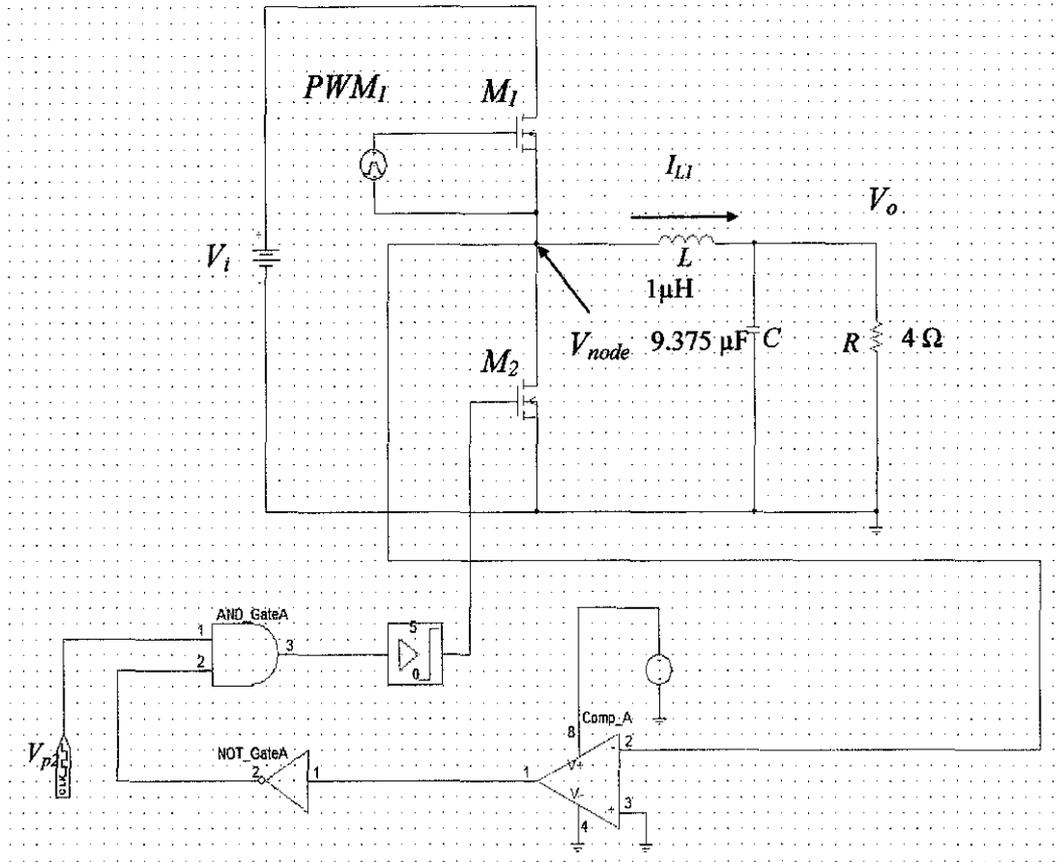
Figure 41: AGD circuit for DCM

APPENDIX A-2: AGD and Compensator [25]
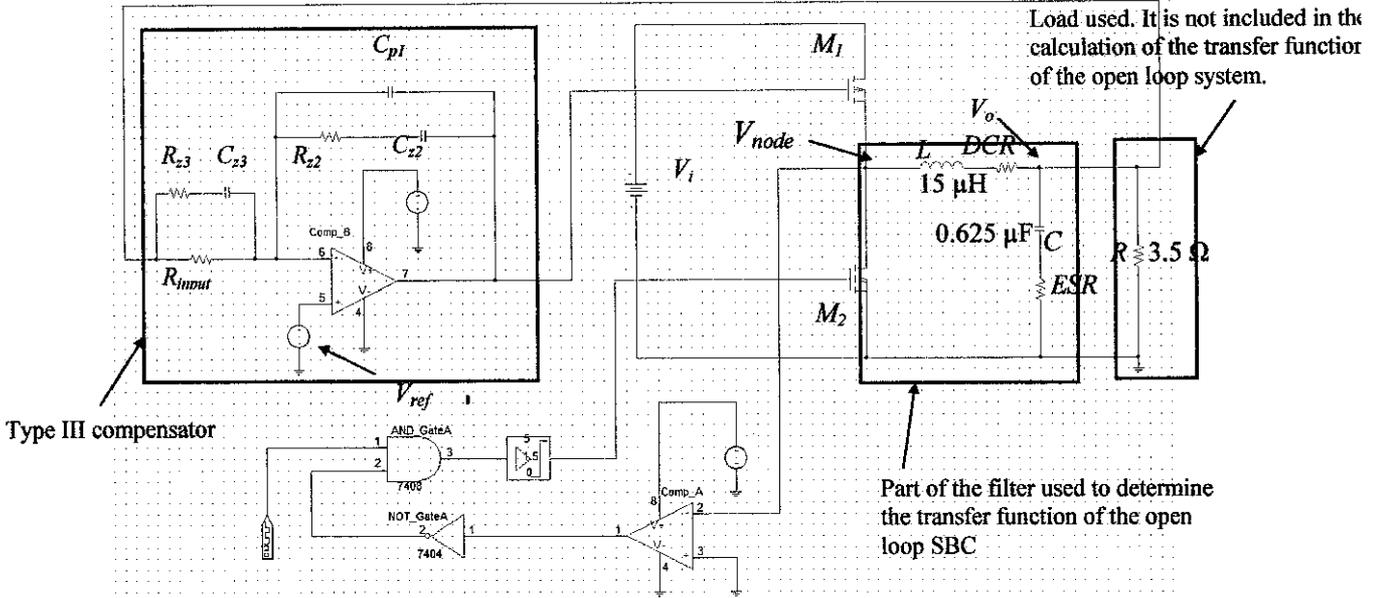
Figure 42: AGD and Compensator for CCM
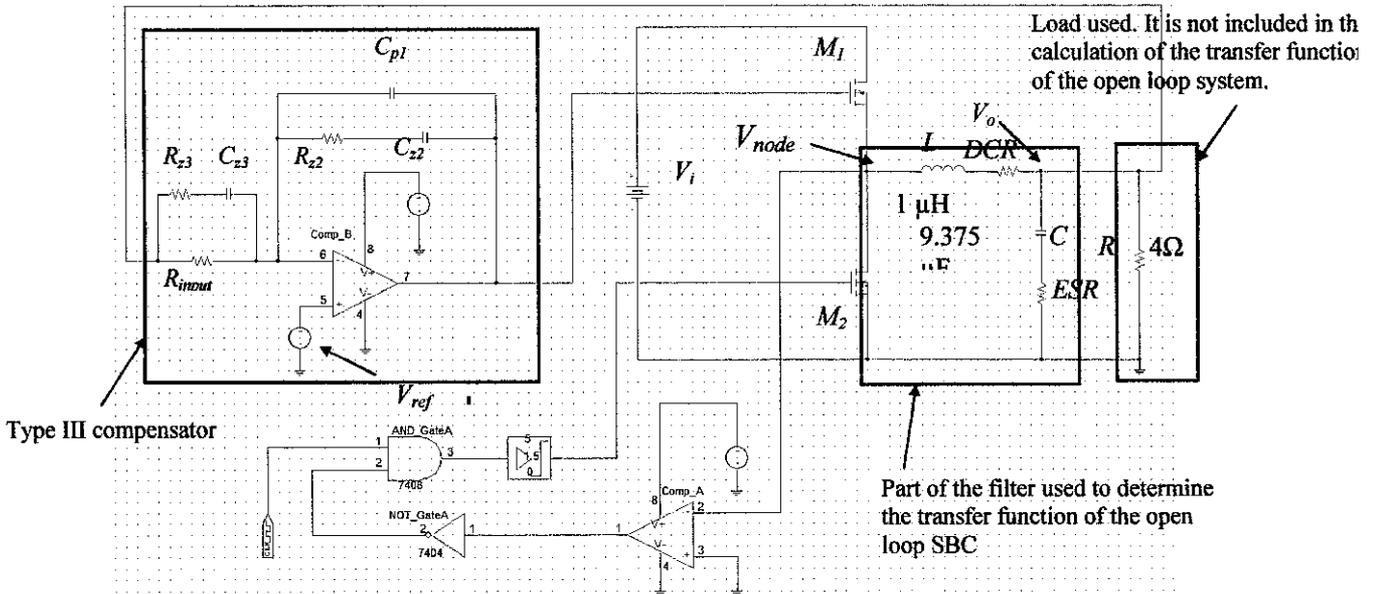
Figure 43: AGD and Compensator for DCM

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APPENDIX A-3: MOSFET PARALLELISM [26]
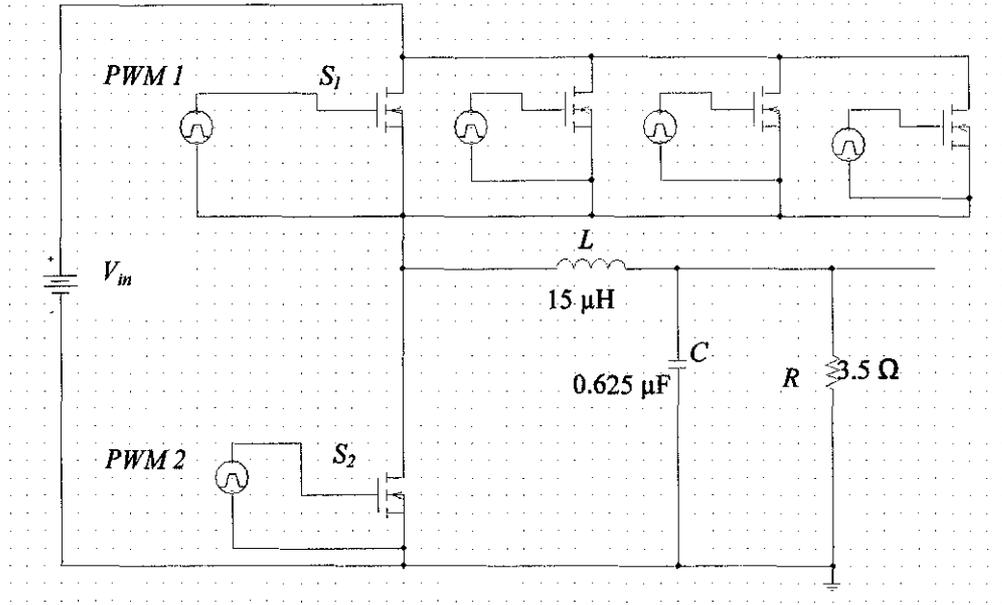
Figure 44 : Circuit (S1:4; S2:3) for CCM
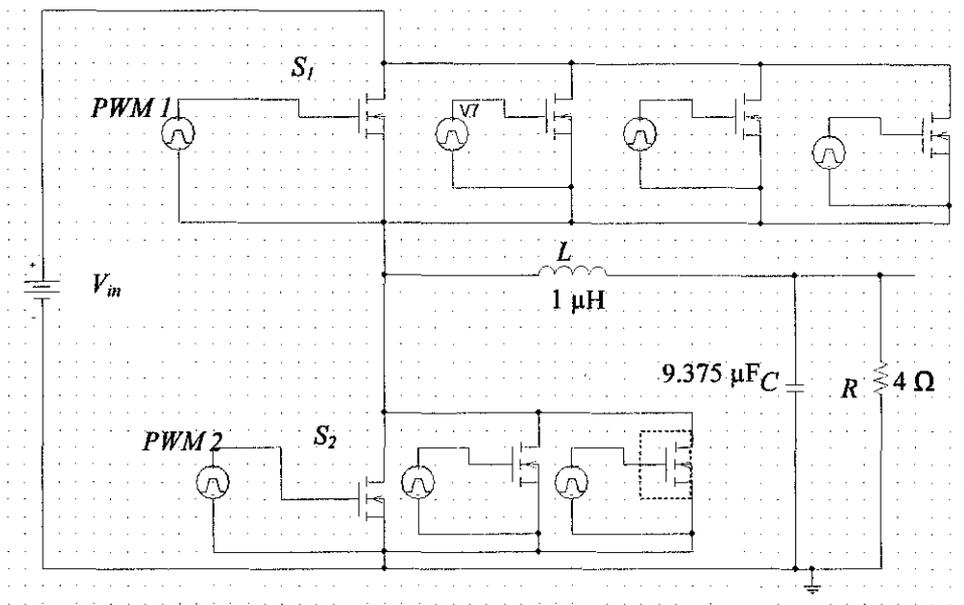
Figure 45 :Circuit (*S1*:4; *S2*:3) for DCM

APPENDIX A-4: MPPT [27]
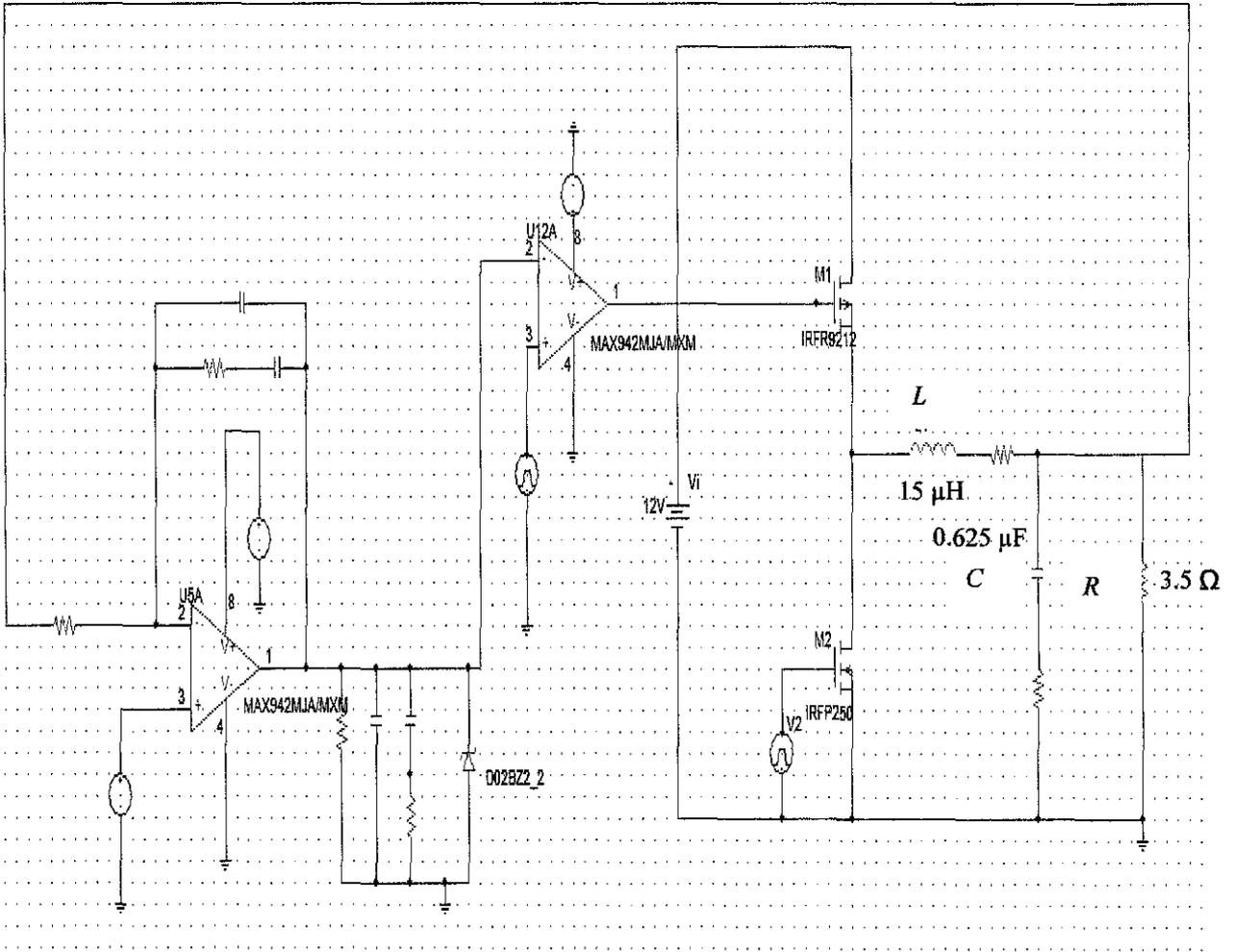
Figure 46 : SRBC circuit connected with MPPT controller in CCM
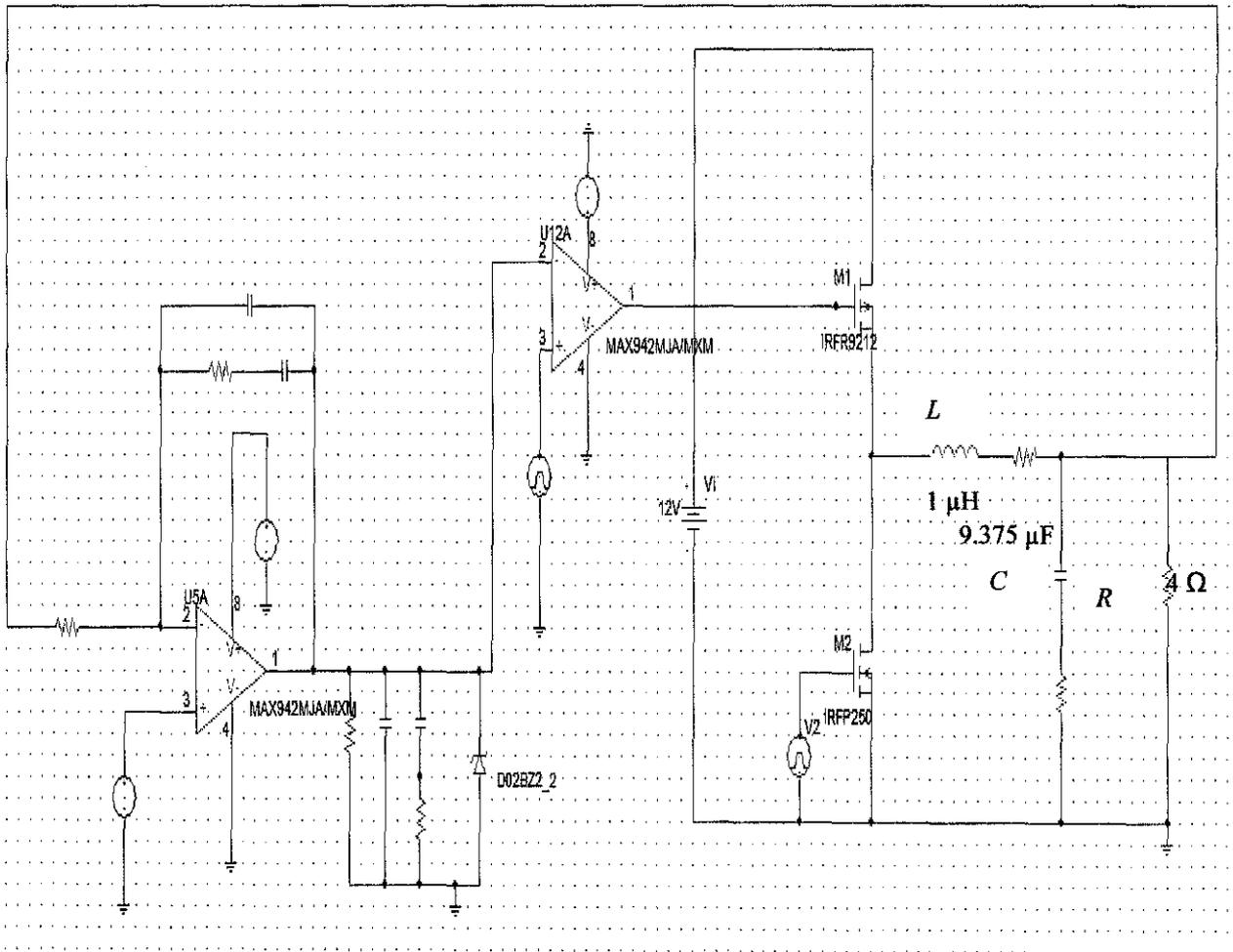
Figure 47 : SRBC circuit connected with MPPT controller in DCM

No.	Detail/ Week	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
1	Selection and Confirmation of Project Title	�░						M								S		E		
2	Gathering information on SRBC	▒	▒	▒	▒			I								T		X		
3	Submission of Preliminary Report				●			D								U		A		
4	Study on SRBC and PSPICE software				▒	▒	▒	S								D		M		
5	Submission of Progress Report							E	●							Y				
								M	●											
6	Design modelling and simulation in PSPICE					▒	▒	E	▒	▒	▒	▒	▒			W		W		
7	Seminar							S T		●						E		E		
								E								E		E		
8	Finalize project work							R				▒	▒			K		K		
9	Submission of Interim Draft Report							B						●						
								R												
10	Submission of Interim Final Report							E								●				
								A												
11	Oral Presentation							K												●

Week 7: MID SEMESTER BREAK
Weeks 15–16: STUDY WEEK
Weeks 17–18: EXAM WEEK

APPENDIX A-6: GANTT CHART FOR FYP II

No	Details/Week	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	Analyse the results	■	■	■	■										
2	Comparison with others gate drives			■	■	■	■	■							
3	Submission of Progress Report								●						
4	Work on draft report									■	■				
5	Pre-EDX											●			
6	Submission of Draft Report												●		
7	Submission of Final Report + Technical Report													●	
8	Oral Presentation														●

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