THE EXPERIMENTAL ANALYSIS OF PREDICTIVE CONTROL SCHEME IN HIGH FREQUENCY GATE DRIVER DESIGN

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The Experimental Analysis of Predictive Control Scheme in High Frequency Gate Driver Design

by

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Dissertation submitted in partial fulfillment of
the requirements for the
Bachelor of Engineering (Hons)
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CERTIFICATION OF APPROVAL

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Approved by,

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TRONOH, PERAK

June 2010

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

MUHAMMAD AMIN BIN AB LATIF

ABSTRACT

Predictive Dead Time Control Scheme is used in gate driver to overcome the problems relating to the t_d. This control scheme applies the prediction concept based on the feedback output from the circuit to predict and reduce the t_d on the switching cycle of the gate driver. Therefore by using the application of the predictive dead time control scheme, the problem related with the t_d can be minimized. The simulation of the Prediction Dead Time Control Scheme circuit was done by Mr. Khalil Azhan Bin Ahmad Zaini, previous final year student. This project will verify the simulation circuit by doing experimental circuit analysis. The results of the experimental analysis will be compared to the simulation results. The project will verify the analysis of predictive controller converter's performance by doing circuit experimental verification. The experimental verification will involve the study of data sheet, circuit operation, and construction of the circuit for experimental analysis and this experimental verification is conducted using appropriate electrical devices and electronics. After the circuit constructed, the project analysis will concentrate on variation of V_{ref} to comparator input. The results of the experimental verification by using predictive dead time control application will show the improvement of the converter's efficiency compared to the conventional gate driver.

ACKNOWLEDGEMENT

First and foremost, I would like to praise to Allah the Almighty for His guidance and time given to me for completing this course. With His guidance and blessings upon me, I managed to overcome all obstacles in completing this project. Here, I would like to use this special opportunity to express my heartfelt gratitude to everyone that has contributed to the success of this project.

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LIST OF ABBREVIATIONS

SRBC	Synchronous Rectifier Buck Converter
PWM	Pulse Width Modulation
MOSFET	Metal Oxide Field Effect Transistor
PDC	Predictive Delay Control
PGD	Predictive Gate Driver
FDR	Fixed Duty Ratio
ADC	Adaptive Delay Control
t_d	Dead Time Delay

CHAPTER 1

INTRODUCTION

1.1 Background of Study

Usually, the PWM principle is commonly used in power electronics applications for controlling gate driver of power converters. Generally the conventional power converter operates at high switching frequency and the signal of PWM is used to turn ON and OFF the MOSFET to get the desired output for the gate driver signal. Implementation of common PWM as the gate driver input may contribute to unstable performance of the High Frequency Gate Driver Design. Hence the desired performance cannot be achieved by using conventional techniques that made up from PWM. This project intends to mainly construct the experimental circuit and verify the circuit by experimental analysis of the Predictive Control Scheme implemented on the SRBC.

1.2 Problem Statement

Generally, most of the power converter using PWM technique as the gate driver input signal. However, when come to the high frequency switching input signal application, conventional PWM is unable to do the job as the gate driver efficiently. This inefficiency will reduce the reliability of the entire system.

For high frequency gate driver, the t_d becomes more critical aspect to focus on. When the period of t_d is longer, more conduction losses are introduced in the circuit and when there is no t_d in system, the cross conduction will occurs and the effect will be an increase switching losses.

To rectify this problem, the application of Predictive Control Scheme has been introduced and the problem relate with the t_d delay can be minimized as much as possible. The constructed circuit will be verified by doing experimental analysis.

1.3 Objective

Upon completing the project, a few objectives need to be achieved. The objectives of the project are as follows:

1. To study and understand on the Predictive Control Scheme for High Frequency Gate Driver.
2. To construct the Predictive Control Scheme Circuit for experimental verification.
3. To integrate the constructed circuit with the Synchronous Rectifier Buck Converter.
4. To analyze the efficiency of the Predictive Control Scheme Circuit by experimental test.

1.4 Scope of Study

The study is divided into three main stages as follows:

i. Literature Review

   All the information regarding on the Predictive Control Scheme is compiled and studied.

ii. Design and Construction the Circuit

   The Predictive Control Scheme Circuit based on simulation circuit will be constructed and integrated to the Synchronous Rectifier Buck and Proposed Gate Driver.

iii. Analysis of The Circuit Performance

The Predictive Control Scheme circuit will be implemented to SRBC and PGD for experimental test and verification. Result obtained from the experimental analysis will be analyzed and concluded.

CHAPTER 2

LITERATURE REVIEW

2.1 Gate Driver

Gate driver is used to turn ON and OFF the MOSFET on the power electronic converter. The conventional technique is using PWM as the gate driver. The PWM signals as the input signals for the gate drivers are shown by the Figure 1.

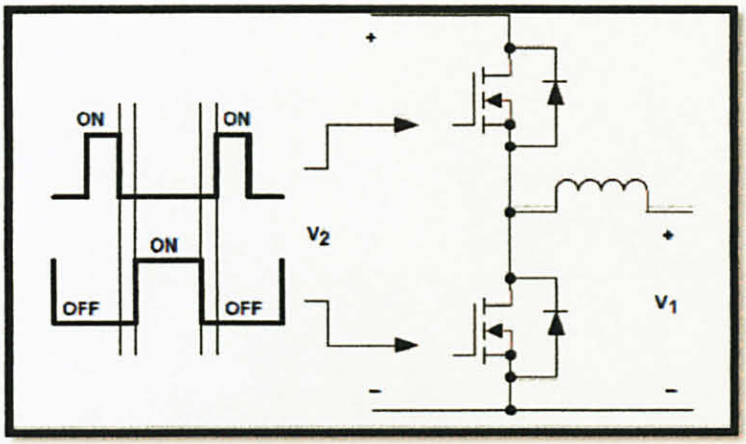

Figure 1: PWM Signal as the Gate Driver [1]

2.2 Pulse Width Modulation

PWM is a very efficient way of providing intermediate amounts of electrical power between fully ON and OFF. A simple power switch with a typical power source provides full power only, when switched ON. PWM is a comparatively recent technique, made practical by modern electronic power switches. Figure 2 shows how the PWM signal is produced by comparing

rectangular pulse wave with the straight line as the reference voltage. In this example there are three different colours for different PWM output signal. When V_{ref} is higher (RED line), the period of ON time is shorter and when the V_{ref} is lower (BLUE line), the period of ON time of PWM is longer.

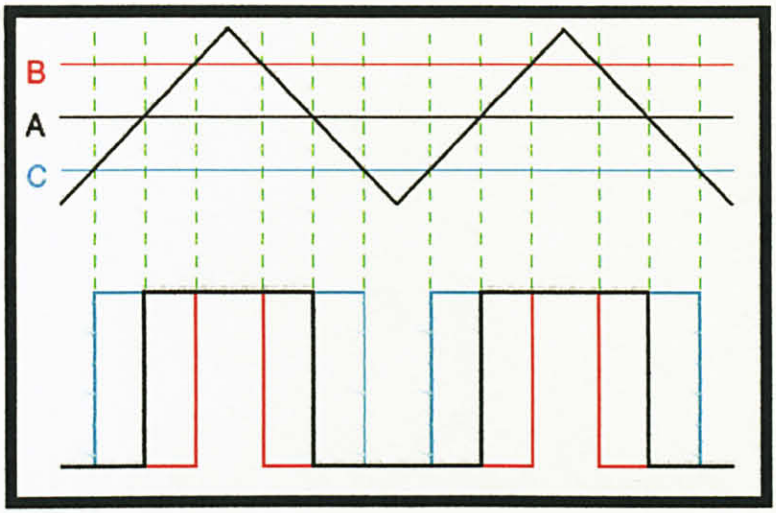

Figure 2 : Example how the PWM Signal Produced

2.3 Dead Time Delay, td

A t_d can be described as the period which neither one of the switch (MOSFET) is turned ON. The t_d is the time gap where no signal is applied to the MOSFET. This is called the Dead Time. Too long t_d will introduce losses due to body diode conduction [2]. In addition, t_d is used to avoid shoot through currents in converters with synchronous rectifier [3]. Figure 3 shows the location of the t_d in PWM between the input signals.

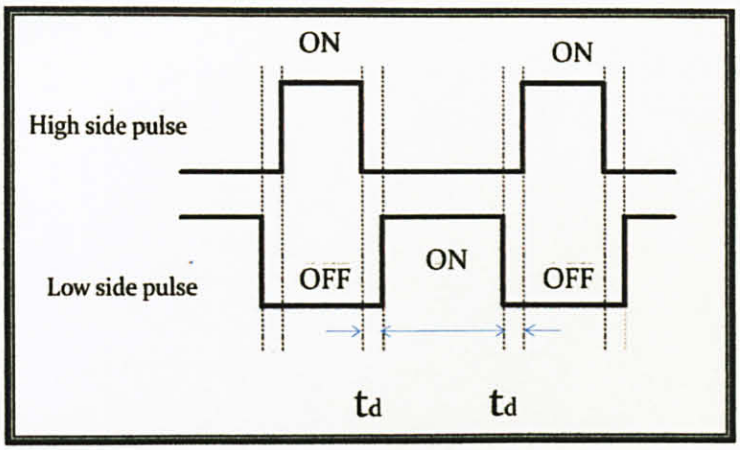

Figure 3 : Dead Time between the PWM Input Pulses

2.4 Body Diode Conduction

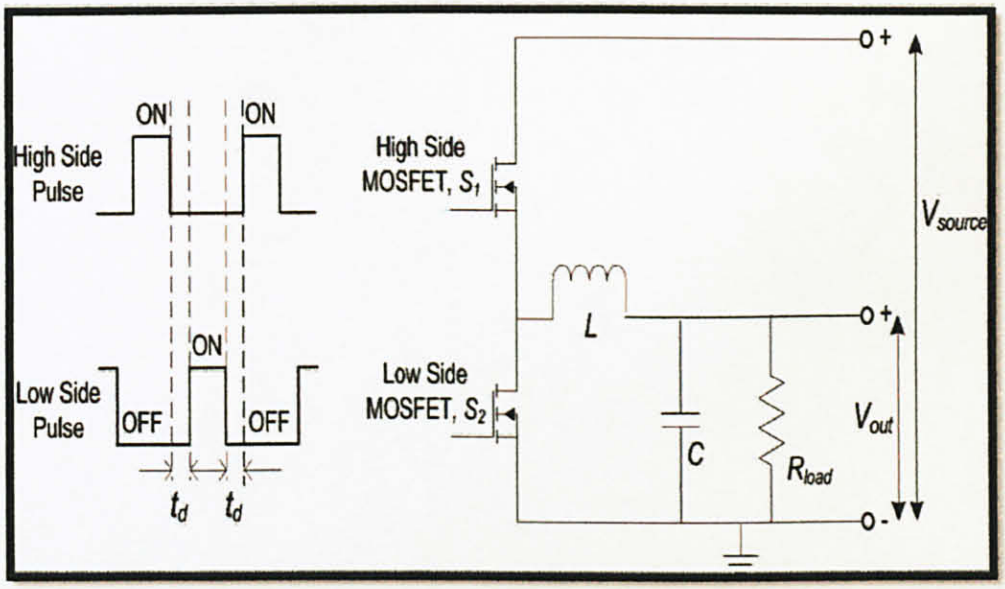

Figure 4 : Example of the Synchronous Switching by PWM Signal

From Figure 4, during MOSFET switching ON and OFF, there will be a time interval where both MOSFETs are not conducting. This time interval is the dead time, t_d which has been discussed previously.

During S_1 is ON and S_2 is OFF, the energy will be transferred to the load. Before S_1 is to be turned OFF and S_2 is still turned OFF, there will be a period where both of the MOSFETs are turned OFF.

Although S_1 and S_2 are turned OFF, the current from the inductor will keep flowing through body diode of S_2 due to the effect of inductive load. S_2 will turn ON after t_d ends and since the forward voltage drop across $S_{2\,(RD,ON)}$ is lower than the body diode voltage drop, this will allow the inductor current to flow through S_2 rather than body diode. [4]

The t_d is related to the body diode conduction, longer t_d will contributes to longer body diode conduction period. The longer period of body diode conduction, the larger losses for the circuit will be and will reduce the overall efficiency of the system. This loss is known as the body diode conduction losses, P_{bd}. In order to get a low body diode loss, shorter t_d is required in the system. Figure 5 shows how the body diode conduction occurs in the given circuit.

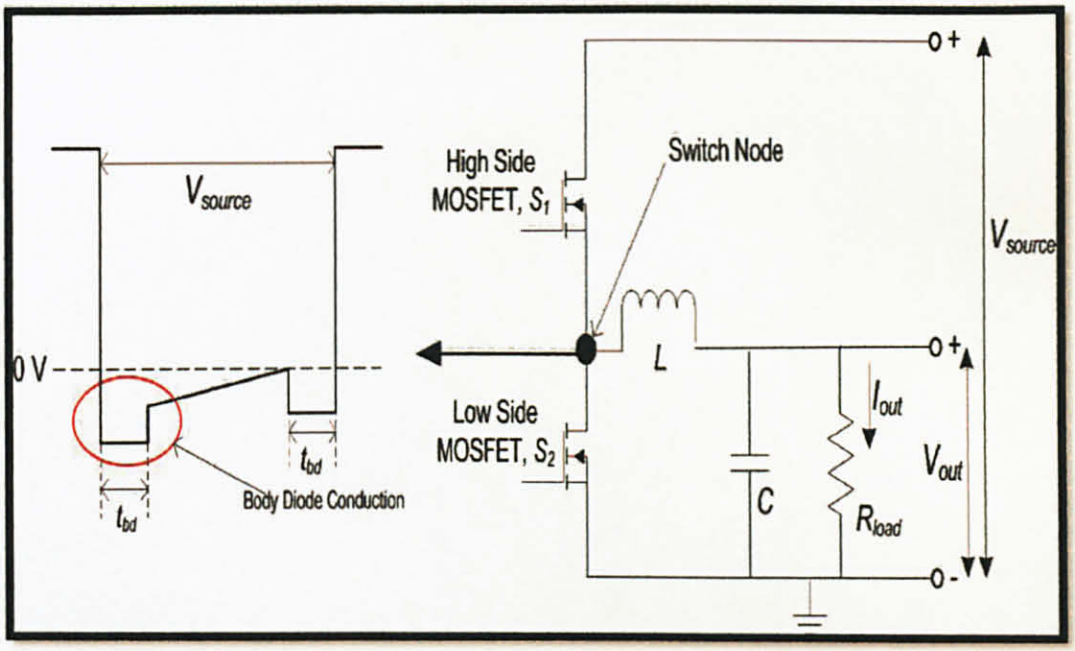

Figure 5 : Body Diode Conduction [5]

Below are the formulas how to calculate the body diode conduction loss. The body diode is circled in the figure.

$$P_{bd} = Vf \times Iout \times fsw \times (t_{bd(rise)} + t_{bd(fall)}) \quad (1)$$

Assuming that $t_{bd(rise)} = t_{bd(fall)}$

$$P_{bd} = V_f \times I_{out} \times f_{sw} \times 2 \times t_{bd} \quad (2)$$

Where :

V_f = body diode forward voltage drop

I_{out} = output current

f_{sw} = switching frequency

t_{bd} = body diode conduction period

2.5 Cross Conduction

Cross conduction occurs when both of the high side and low side MOSFETs are partially or fully turned OFF at the same time. When this occurs, it will provide the path for current to "shoot through" from voltage supply directly to the ground. Besides that, V_{gs} may also lead to the cross conduction and if this induced V_{gs} is greater than gate threshold voltage, S_2 could turn ON automatically. Since the "shoot through" current [6] flows directly to the ground without flowing to the loads, this excessive power will dissipate in both MOSFETs and it can damage one or both MOSFETs. In order to prevent the damage of these components, the application of t_d is essential.

2.6 Previous Technologies of Gate Driver

2.6.1 Fixed Duty Ratio

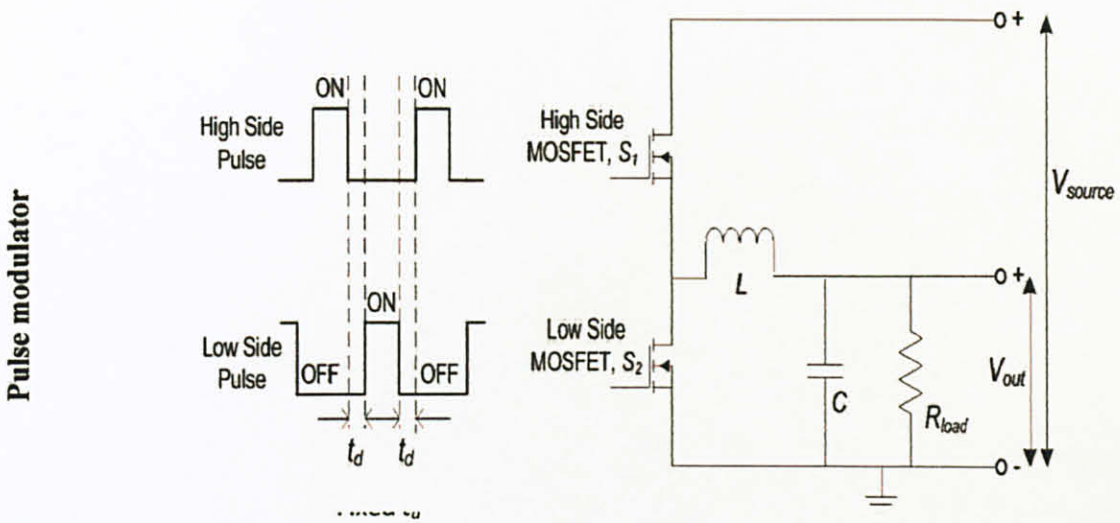

Figure 6 : The Fixed Duty Cycle Scheme (FDC)

The Fixed Duty Ratio (FDR) Control Scheme is the first technology of generating the gate driver control scheme. This control scheme has constant turn on delay between the two gate drivers in order to avoid cross conduction. In other words, this control scheme has predetermined t_d where it should be long enough to cover the entire application of the device, the temperature, and also the variation of the t_d. Based on [5] the optimized t_d for a fixed duty cycle is 15 ns. However, this control scheme has limitation during the operation. The voltage drop and reverse recovery associated with the synchronous rectifier body diode becomes a great percentage of the total synchronous rectifier power loss as the designed output voltage decrease [7].

As the switching frequency increases, finite t_d associated with the fixed scheme starts to become a significant part of the switching cycle, which make the efficiency decrease drastically.

2.6.2 *Adaptive Delay Control Scheme*

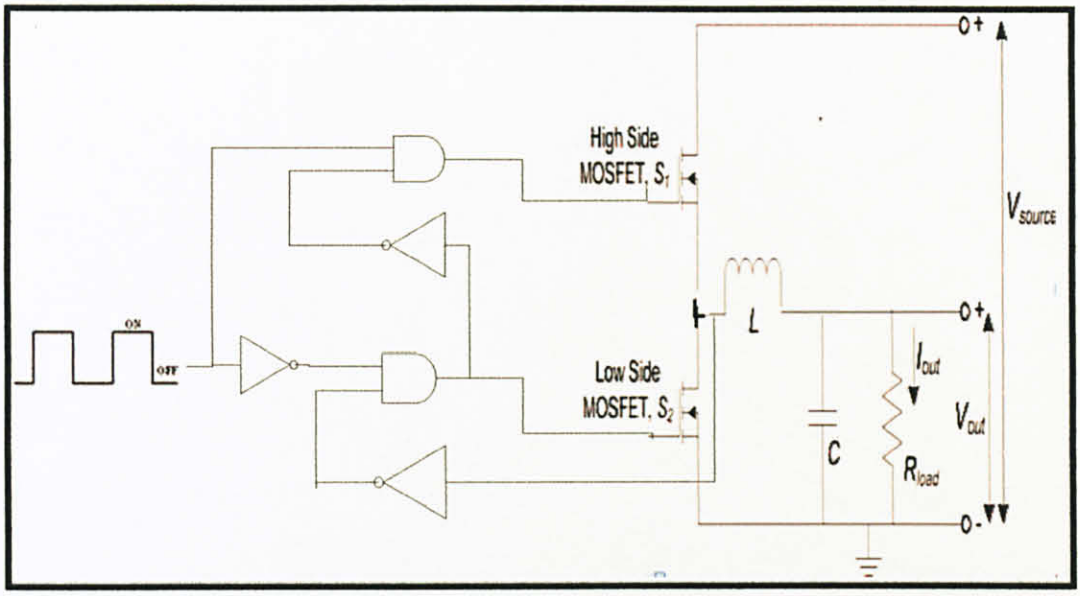

Figure 7 : Adaptive Delay Control Scheme (ADC).

The Adaptive Delay Control (ADC) is the second generation of the gate control scheme. This scheme was introduced to overcome the limitation of the FDR control scheme. ADC uses control loop that includes a digital delay line. The control loop will senses the drain to source voltage (V_{ds}) of the S_2 and adjust the digital delay line according to the amount of delay that should be applied to turn on the S_2. S_2 is turned ON only when the switch node voltage is equal to zero [8].

The advantage of using this scheme is the adjustment of the delay can be made adaptively according to type of MOSFET. However, there are also disadvantage of this control scheme which including the variation of body diode conduction time interval. This is due to the logic components that are used as the feedback. Each of the components has their own propagation delay. This propagation delay will indirectly increase the t_d between the pulses.

2.7 The idea of Predictive Control Scheme

Due to limitation in FDR and ADC Scheme, the Predictive Delay Control (PDC) scheme is introduced. This scheme is able to change the t_d from time to time according to the feedback from the circuit. As an example, Figure 8 shows when t_d is very small during S_1 is ON and S_2 is OFF, the PDC will detects the signal from the circuit to increase value of t_d for the next switching.

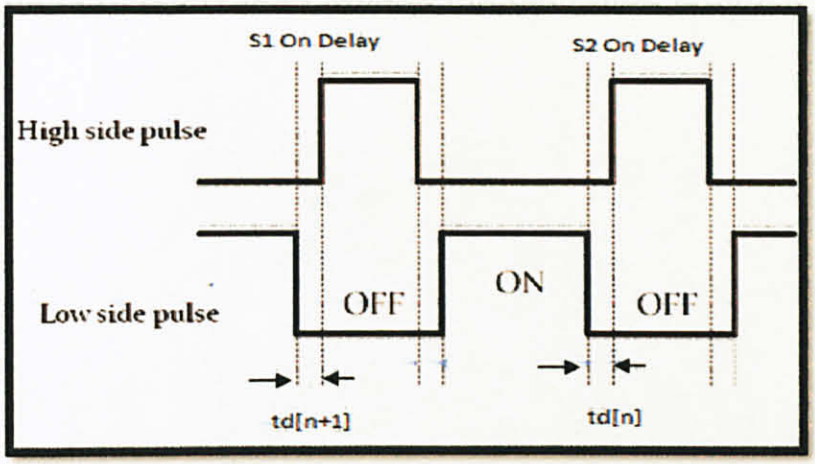

Figure 8 : Time Delay

Predictive delay control scheme is a combination of a predictive circuit integrated with PWM where it may vary the t_d during operation according to the feedback signal. This circuit will detect voltage or current from SRBC. Figure 9 shows the block diagram of how the PDC is working theoretically.

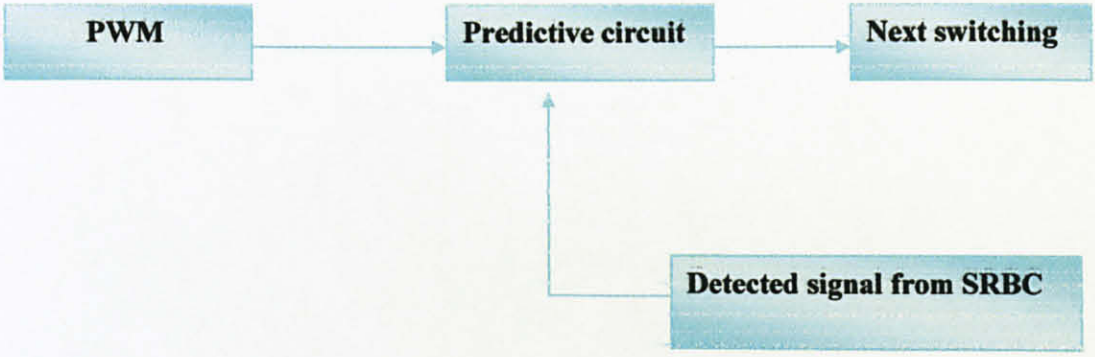

Figure 9 : PDC Scheme Block Diagram

As an example of the feedback input for the next switching signal is by using the NOR gate to compare the signals from the SRBC to the predictive circuit. During high side pulse transition of the current cycle, the circuit's feedback NOR gate will detect the V_{ds} and V_{gs} voltages of S_2 [6]. If the output result is high, it will indicate t_d can be decreased. For next switching cycle, t_d during S_1 turned OFF and S_2 turned ON will be reduced until output of NOR gate is low. After the output of NOR gate is low, circuit will predict that the delay can no longer be reduced or else cross conduction will occur. The inputs and output of NOR gate is shown in the Figure 10.

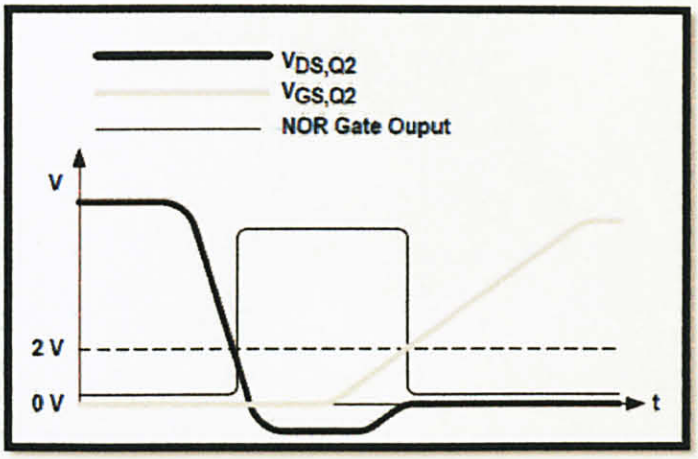

Figure 10 : The Operation of NOR Gate in Feedback Loop [9]

For transition from low to high, a comparator will perform the feedback operation. This comparator will sense the V_{ds} and V_{gs} voltages of S_2. When the body diode conduction is detected, the comparator output becomes high and the predictive circuit will reduce the delay between S_1 turn ON and S_2 turn OFF. The circuit will keep decreasing the delay until the body diode conduction is not detected anymore. Then, the predictive circuit starts to increase the delay to avoid cross conduction on the circuit [9]. The operation of the comparator is shown in the Figure 11.

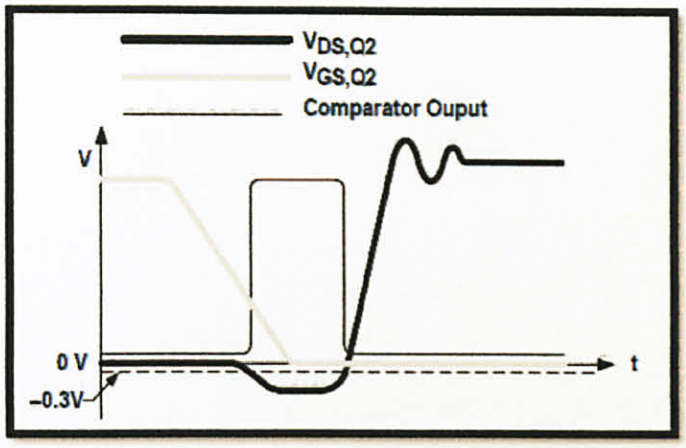

Figure 11: The Operation of the Comparator on Feedback Loop [9]

2.8 Simulation Circuit of the PDC Integrated to SRBC

Figure 12 shows the simulation circuit of Predictive Control Scheme that was done by the previous FYP student. The experimental circuit construction will be based on this circuit and will have additional circuits and modification in the future if needed.

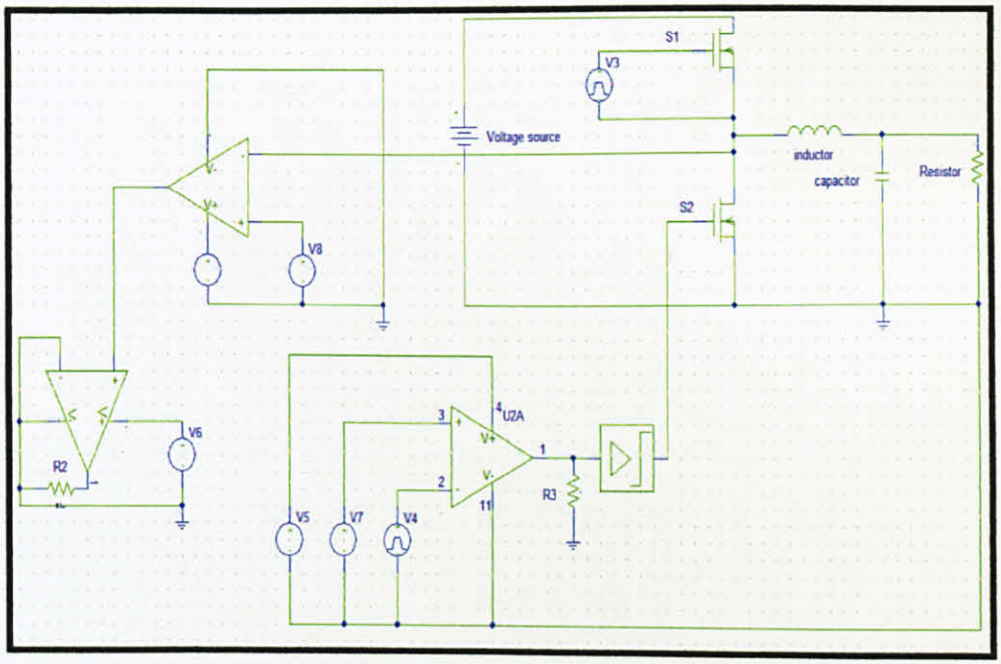

Figure 12: Simulation Circuit of Predictive Control Scheme

2.9 Synchronous Rectifier Buck Converter

In this project, SRBC will be used as the test circuit for the Predictive Control Scheme circuit output. The SRBC is essentially the same as the buck converter with the substitution of the diode for another MOSFET switch. The top MOSFET switch operates the same way as the buck converter in charging the inductor current. When the switch control is off, the lower MOSFET switch will turns on to provide a current path for the inductor when discharging. Although requiring more components and additional switch logic sequencing, this topology improves efficiency with faster switch turn on time and lower MOSFET series resistance $R_{DS\,(ON)}$ versus the diode [10]. Figure 13 below shows the schematic of a conventional SRBC.

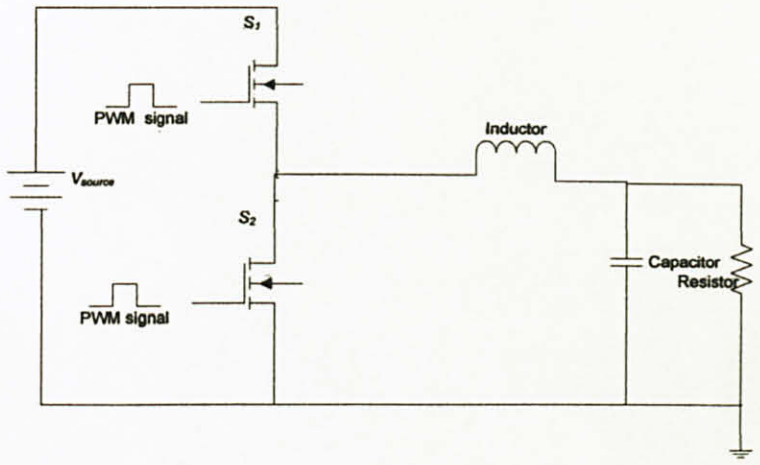

Figure 13: Schematic Diagram of a Conventional SRBC

2.10 Losses in the circuits to be focused in the experiment

2.10.1 Switching Losses

The switching losses happen when the current and the voltage across the MOSFETs overlap to each other. It Occurs at the MOSFETs transition between the fully ON and OFF states. Figure 14 shows how the switching losses occur.

$$P_{SW} = \frac{1}{2} \times t_{SW} \times \text{Peak Power} \times f_{sw} \quad (3)$$

Total switching losses, $P_{sw} = P_{sw1} + P_{sw2}$ (4)

Where:

P_{sw1} = Power losses during switch OFF

P_{sw2} = Power losses during switch ON

fsw = Switching frequency

t_{sw} = Switching time

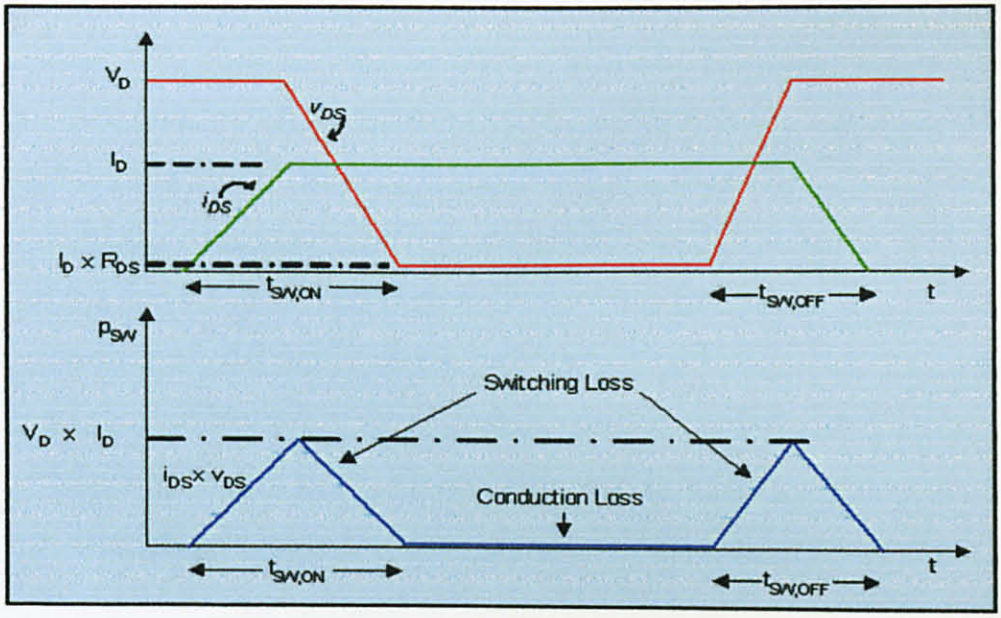

Figure 14: Switching Losses occur at the MOSFETs

2.10.2 Conduction Losses

During the MOSFET turn ON, it will have the static drain-source resistance. When the current is flowing through across the MOSFET, it will dissipate the power. This dissipated power is known as the Conduction Loss, P_{cond}.

$$P_{cond} = (I_{out})^2 \times R_{DS\,(ON)} \times (1-D) \quad (5)$$

$$\text{Since } D = \frac{Vout}{Vsource} \quad (6)$$

$$P_{cond} = (I_{out})^2 \times R_{DS\,(ON)} \times \left(1-\frac{Vout}{Vsource}\right) \quad (7)$$

Where:

I_{out} = output current

$R_{DS\,(ON)}$ = Static-drain ON resistance

D = Duty cycle

V_{out} = output voltage

V_{source} = Input voltage

$R_{DS\,(ON)}$ = Resistance between Drain to Source in the MOSFET during ON state.

CHAPTER 3

METHODOLOGY

3.1 Procedure Identification

Figure 15 showing the flow of the process in order to complete the project. The Gantt chart is attached in the Appendix A.

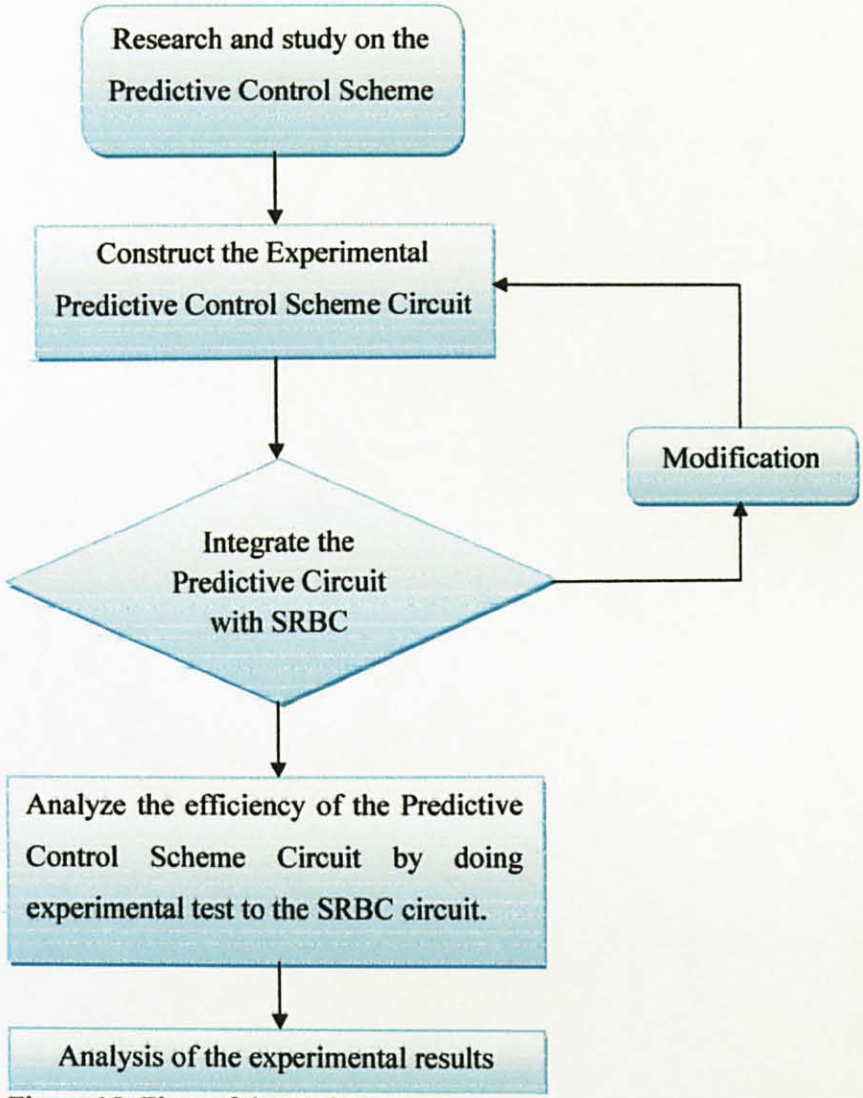

Figure 15: Flow of the Project

3.2 Block Diagram of the Experimental Circuit

Figure 16 shows the experimental circuit diagram of Predictive Control Scheme integrated with SRBC. The two different sources of sawtooth signals are synchronized prior to have same starting time. These output signals from synchronization circuit will have same starting time, duty cycles and frequencies. The synchronized signals will be the input of the voltage comparators in order to produce PWM signal with different duty cycle. From the voltage comparators, the PWM signal will going through the MOSFET Drive Circuit in order to increase the amplitude of the PWM signal. The input for S_1 have no adjustment and directly driven by the output of voltage comparator. For low side pulse, pulse width needs to be varied so that the dead time, t_d between pulses can be varied.

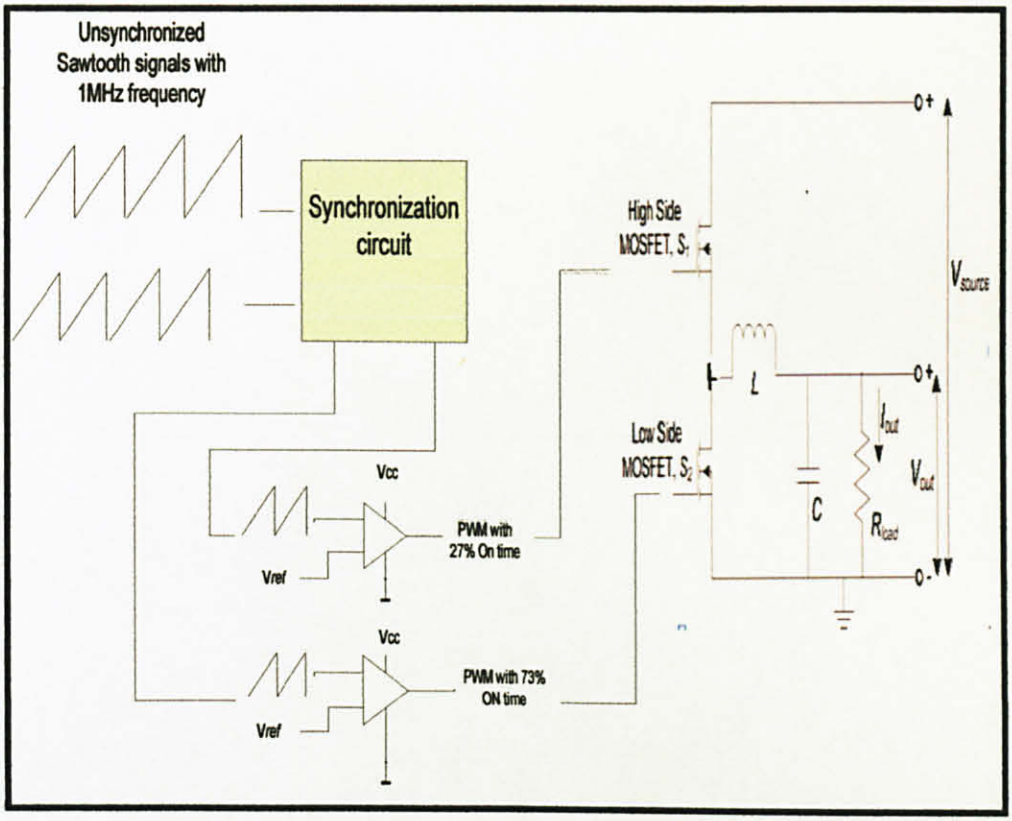

Figure 16: Block diagram of the PDC circuit integrated to SRBC

3.3 Components Used in Experiment

3.3.1 Voltage Comparator

There are few reasons that have been considered in choosing the suitable voltage comparator for the experimental circuit. Most of them have very high dissipation powers which will contribute to the inefficiency of the system. MAX944 voltage comparator has 1mW to 3.6mW power dissipation. These values can be considered as very little power is dissipated compared to the power dissipations on the other voltage comparators. The most important thing to be considered in choosing the voltage comparator for this experiment is the frequency that the device can operate.

MAX944 has four voltage comparators built in. Figure 17 shows the connection diagram of MAX944 [11].

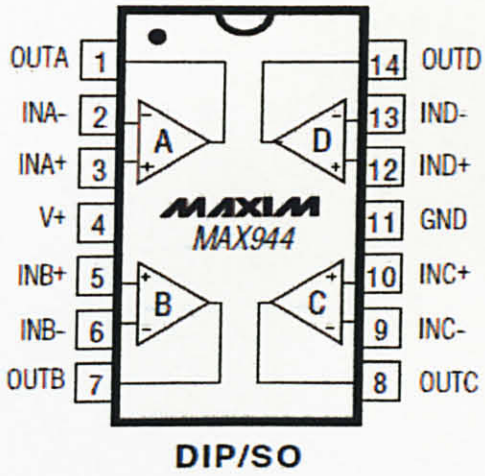

Figure 17 : MAX 944

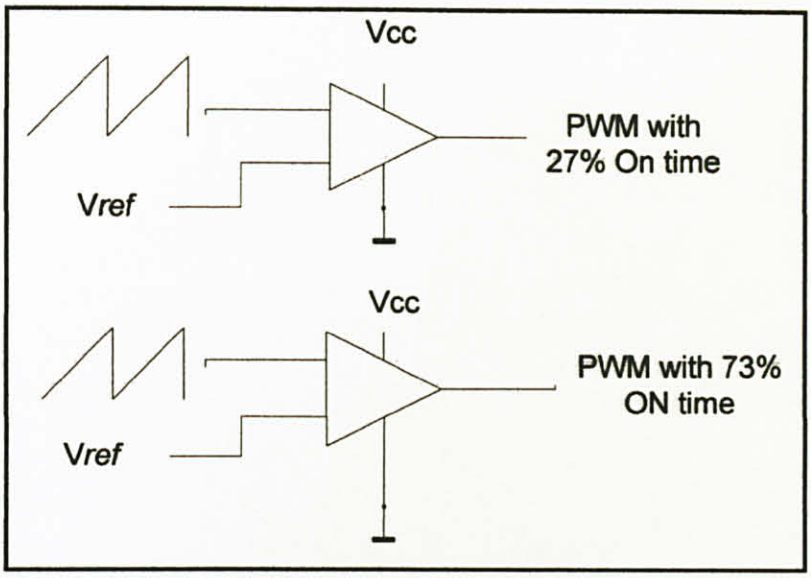

Figure 18 : Simplified Circuit Diagram for PWM Generation using Voltage Comparator

In the Figure 18, the PWM signal will be produced by using voltage comparator MAX942. The synchronized V_{tri} is compared with V_{ref} and PWM is produced. The 27% duty cycle will be applied to S_1 and the PWM with 73% duty cycle will be applied at S_2 at SRBC.

In order to produce another PWM signal with the inverted duty cycle is by swapping the inputs of the voltage comparator. As an example, let say the voltage comparator inputs have A (positive) and B (negative). In order to produce 27 % duty cycle PWM is by connecting about 3.2V DC at input A and sawtooth signal at input B. Therefore, to produce 73% duty cycle of the PWM is only by swapping the V_{ref} and V_{tri} at the voltage comparator inputs.

3.3.2 MOSFET

IRF620 MOSFET will be used as the switch and it is available in EE-store. This is the N-channel MOSFET and has $R_{DS} \leq 0.8\ \Omega$. This MOSFET can stand up to $V_{DD} = 200$ V and $I_D = 6$A. Figure 19 shows the IRF620 MOSFET.

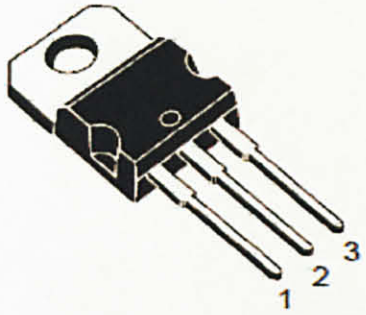

Figure 19 : IRF620 MOSFET [12]

Table 1 : The Legs Description of IRF620

Legs of MOSFET	**Description**
Leg 1	Gate
Leg 2	Drain
Leg 3	Source

3.3.3 *Synchronization Circuit*

In order to provide PWM input signal at S_1 and S_2 by using two different sources, these signals must be synchronized before supplied to the gates driver.

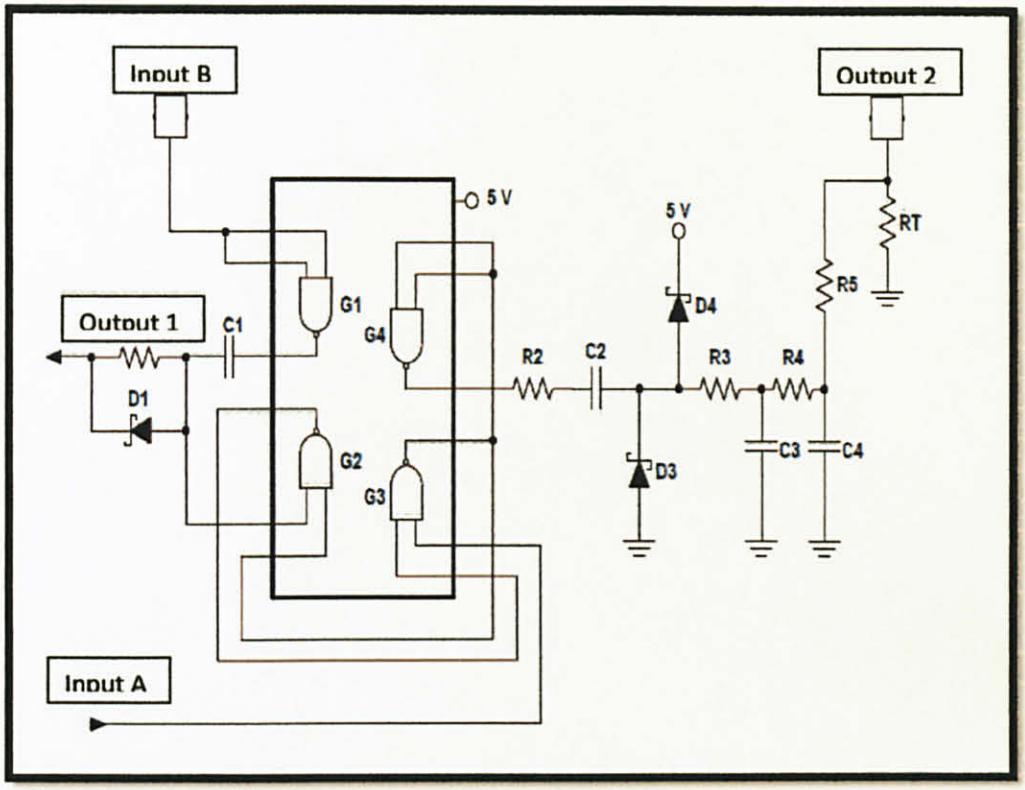

Figure 20: The Synchronization Circuit [13]

From the circuit in Figure 20, two different inputs with different duty cycle will be synchronized to be two signal that have same duty cycle and starting at the same time.

Since the output signal of this circuit will be similar to each other, the easiest way to produce PWM with different duty cycle is by supplying sawtooth signal to the synchronization circuit. These sawtooth signals will be synchronized and both outputs will go to the respective voltage comparators to produce PWMs

with different duty cycles. After that, one of the signals will be adjusted to have 27% turn ON time and the other one is 73% turn ON time.

The sawtooth signals are applied to the Input A and Input B in the circuit. The output of the synchronization circuit is from the Output 1 and Output 2 in the circuit.

Table 2: Values of Components used in Synchronous Circuit

Component	Value
R1	1KΩ
R2	1KΩ
R3	1KΩ
R4	6.2KΩ
R5	327KΩ
RT	400KΩ
C1	1nF
C2	1nF
C3	1nF
C4	100pF
D1	5V
D2	5V
D3	5V
D4	5V

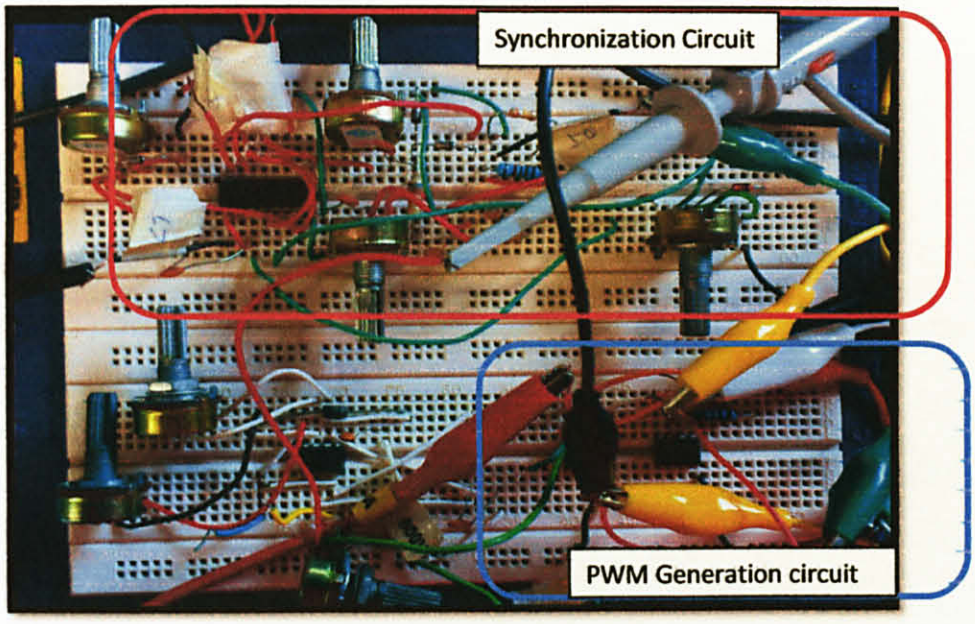

Figure 21 : The Synchronization Circuit connected with the Voltage Comparators during test.

From the circuit in Figure 21, the output from synchronization circuit is applied to the voltage comparator to produce PWM with different duty cycles. In the RED box is the synchronization circuit and the BLUE box is the PWM generation circuit. PWM signal is generated by using voltage comparator MAX942. Figure 22 shows the NAND Gate used in the Synchronization Circuit.

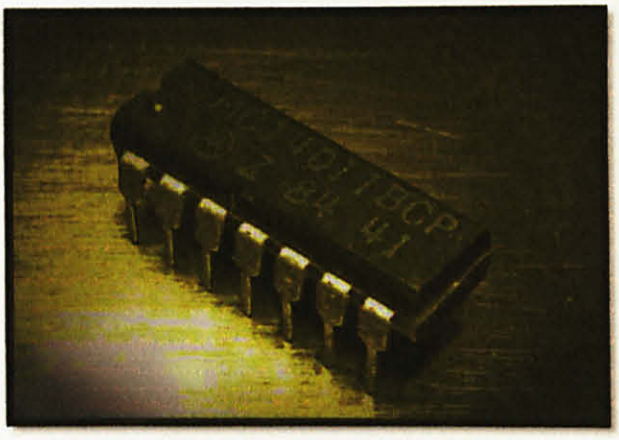

Figure 22: NAND Gate used in the Synchronization Circuit

3.3.4 *MOSFET Drive Circuit*

Due to the MOSFET is unable to be turned ON and OFF by using the output from voltage comparator directly, a MOSFET Drive Circuit needs to be added in the experiment. The signal from voltage comparator will go through this drive circuit and the output from this circuit will fed to the SRBC. Basically the function of this circuit is to amplify the magnitude of the PWM signal. Once the amplitude is of the PWM is higher than the threshold voltage of the MOSFET, the MOSFET is able to be turned ON.

Figure 23 shows the circuit diagram of the MOSFET driver circuit. The PWM signal from the voltage comparator will be the input A and the output is at B. The outputs of voltage comparator must be connected to the diode before going to this circuit to prevent the current of the MOSFET Drive circuit from going back to the voltage comparator since the resistance at the voltage comparator is lower than resistance in MOSFET drive circuit.

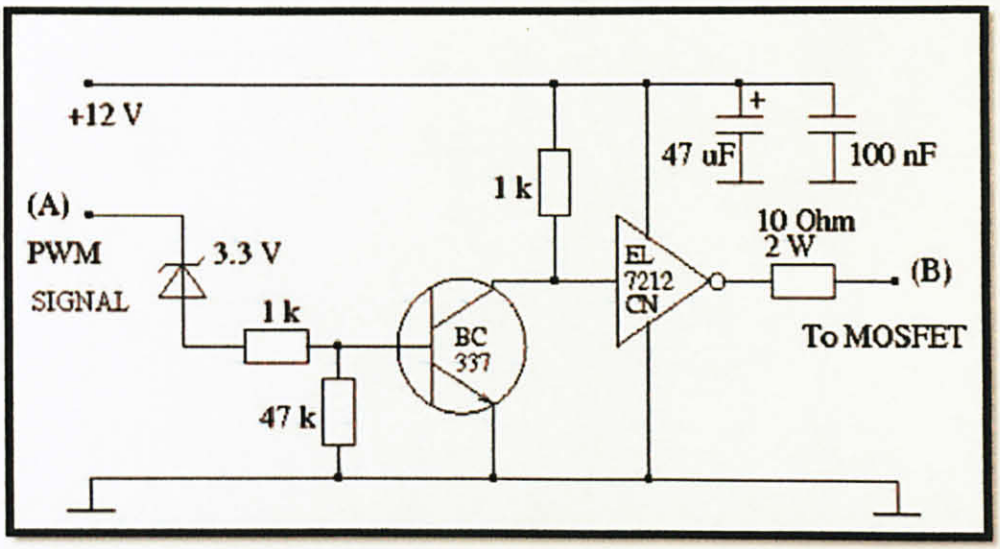

Figure 23: The MOSFET Drive circuit to turn ON the MOSFETs.[14]

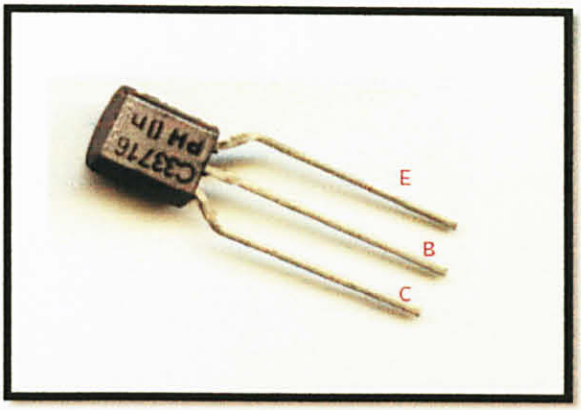

Figure 24: BC337 NPN type transistor used in MOSFET Drive Circuit

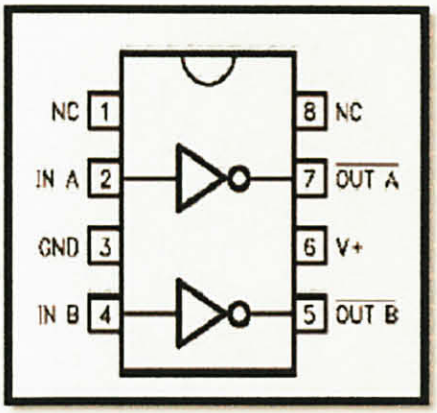

Figure 25: EL7212, Dual Channel Power MOSFET Drivers used in MOSFET Drive Circuit. [15]

3.3.5 Synchronous Rectifier Buck Converter

SRBC is used in this experiment as the test circuit for the Predictive Control Scheme circuit output. The SRBC is basically similar as the buck converter with the substitution of the diode for another MOSFET switch which is S_2. The top MOSFET switch operates the same way as the buck converter in charging the inductor current. The lower MOSFET is to provide a current path for the inductor when discharging.

Table 3 : The Components use in SRBC Circuit

Component	Value	Unit(s)
Resistor	1 kΩ	2
	10 Ω	1
Capacitor	100 µH	1
Inductor	1.8 µH	1

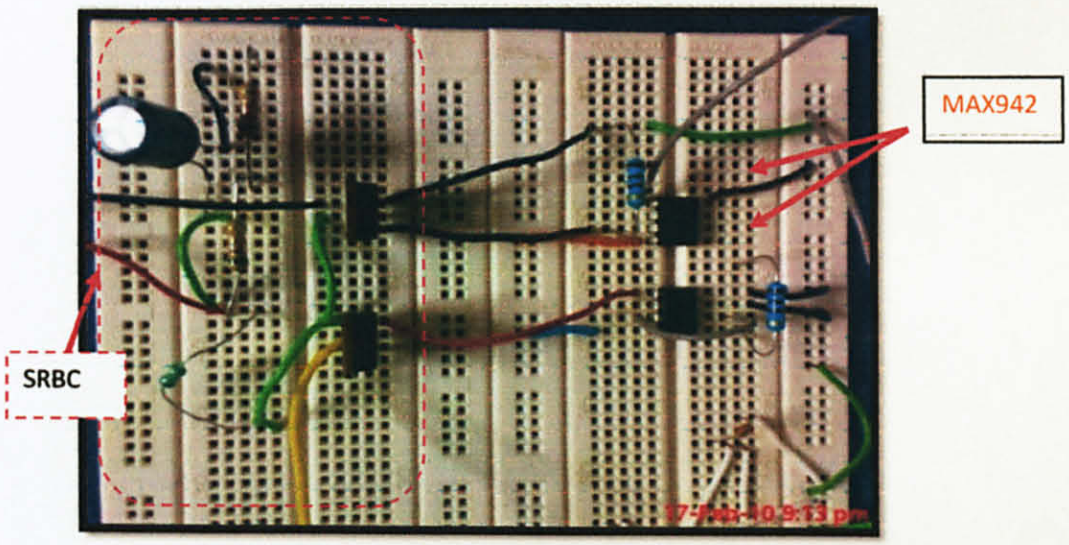

Figure 26: Synchronous Rectifier Buck Converter

CHAPTER 4

RESULT AND DISCUSSION

4.1 Result

4.1.1 Synchronized Sawtooth Signals

The synchronization circuit is used to synchronize both sawtooth signals from the function generator. Figure 27 shows the synchronized sawtooth signals. The value of the frequency and the duty cycle should be similar but there are some unavoidable noises or losses at the output signal that slightly contributing to unstable reading for frequency and duty cycle. However the noises are still can be tolerated.

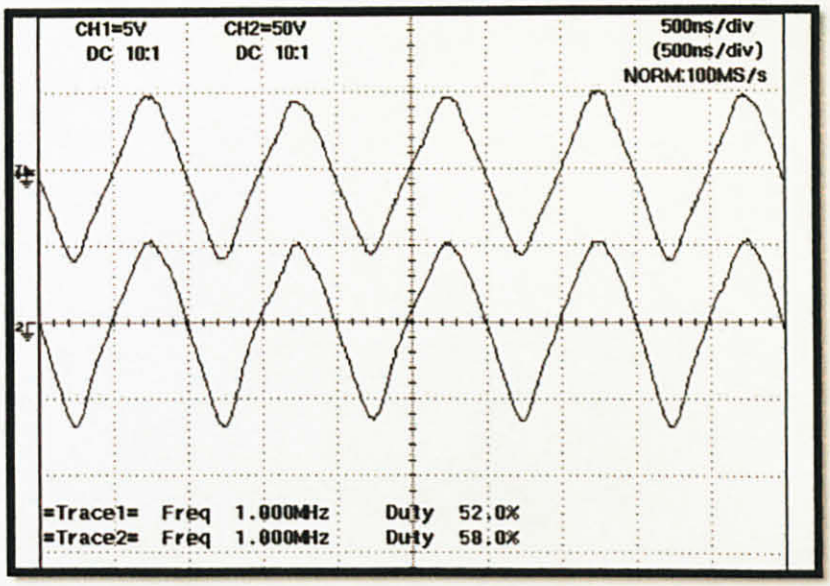

Figure 27: The Synchronized Sawtooth Signal (V_{tri})

4.1.2 PWM

Figure 28 shows how the PWM is produced. The straight line in the figure is the DC voltage (V_{ref}) and the sawtooth signal (V_{tri}) is the output from the function generator. Both of these signals will be the input at the voltage comparator. The value of the V_{ref} can be adjusted in order to vary the duty cycle of the PWM signal. In experiment, the amplitude of the V_{tri} is 5 V with and the V_{ref} vary from 0 V up to 5 V in order to have 27% duty cycle.

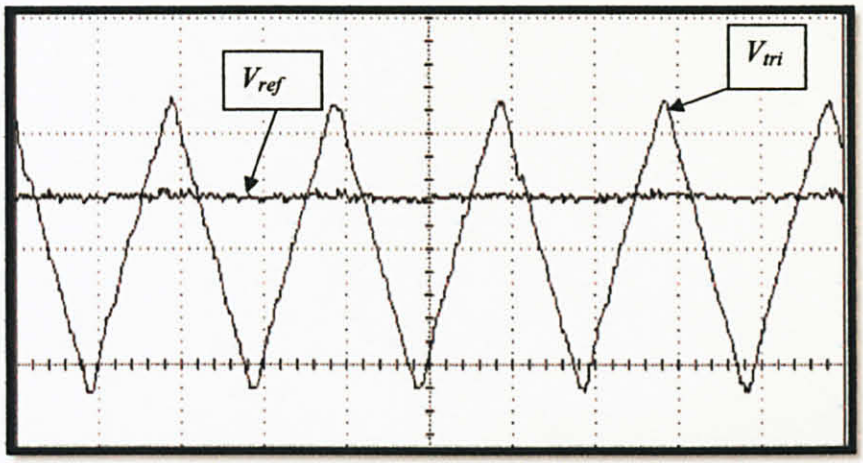

Figure 28: V_{ref} and the V_{tri} used as the Voltage Comparator Inputs

Figures 29 shows the PWM signals with 27% duty cycle waveform and 73% duty cycle waveform. These waveforms are the output of MAX942 voltage comparator. The generation of PWM is by comparing the triangle voltage (V_{tri}) signal with reference voltage (V_{ref}). PWM signal will be generated when V_{tri} is greater than V_{ref} .The duty cycle of the PWM signal can be varied by changing the value of V_{ref}.The value of frequency and duty cycles slightly unstable with value sometime fluctuate in range of 1% - 3% but still acceptable. The detail on how the PWM is generated by using voltage comparator was discussed in the section 2.2.

In order to produce another PWM signal with the inverted duty cycle is by swapping the inputs of the voltage comparator. For example, let say the voltage comparator have the inputs A (positive) and B (negative). To produce 27 % duty cycle PWM is by connecting about 3.2 V DC at input A and sawtooth signal at input B. On the other hand, to produce 73% duty cycle of the PWM is only by swapping the V_{ref} and V_{tri} at the voltage comparator inputs. Figure 29 shows the PWM signal with different duty cycles. Since the signal is unstable, the PWM duty cycle will slightly fluctuate during experiment but it is still can be tolerated.

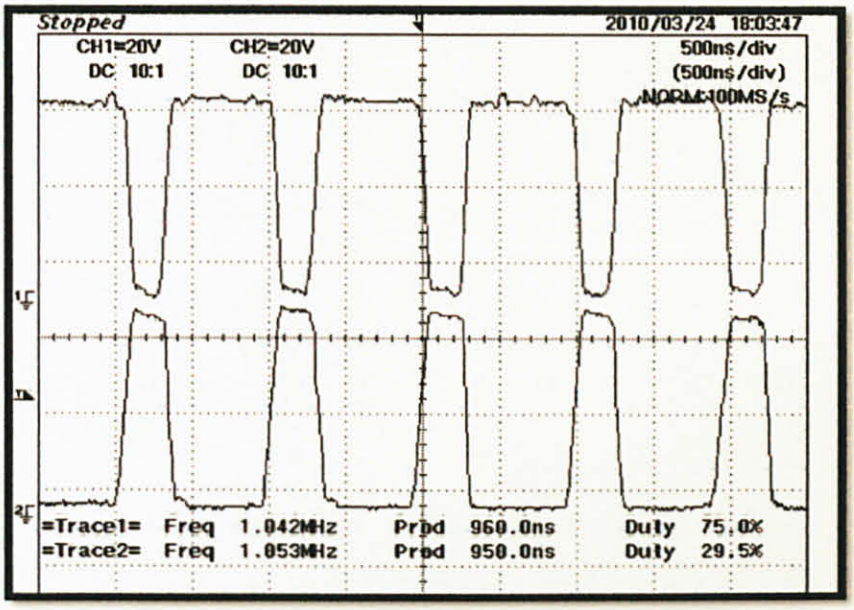

Figure 29: 29.5% and 75% duty cycle PWM waveform at 500 ns per division and 2 V per division

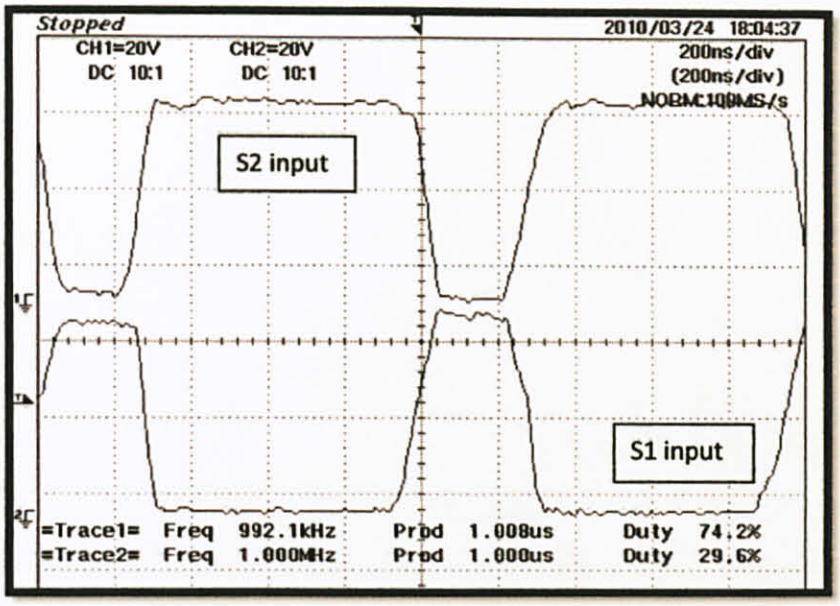

Figure 30: 27% and 73% Duty Cycle PWM waveform with 200 ns per division and 2V per division.

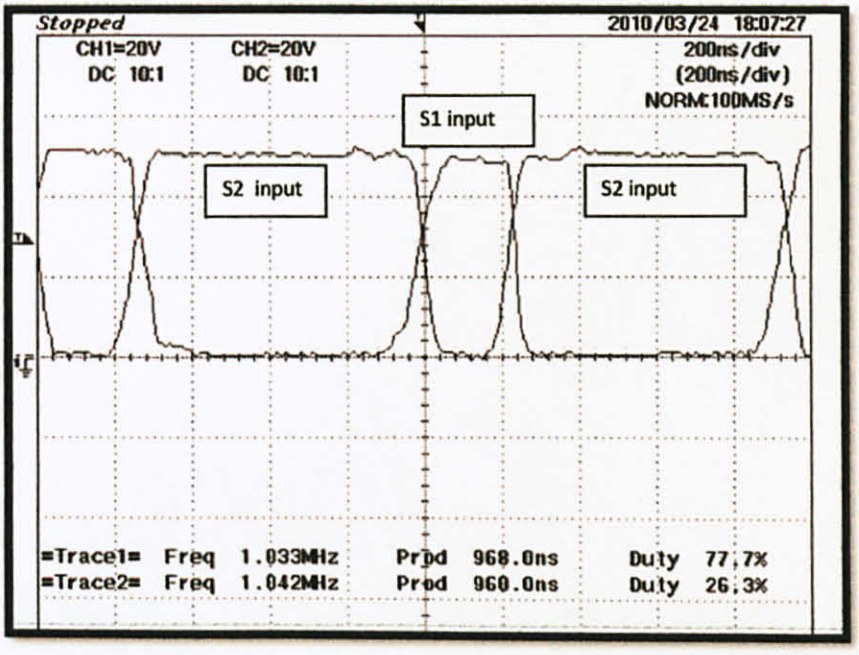

Figure 31: The 27% and 73% Duty Cycle PWM waveforms applied to the switches

For the analysis, both PWM with 27% and 73% duty cycle will be applied to the S_1 and S_2 respectively. During the experiment, the S_1 and S_2 of SRBC is connected to the PWM signals from voltage comparators and V_{gs} of the both MOSFETs are recorded. In the figure below, the low side waveform is the V_{gs} of the S_1 and the high side waveform is the V_{gs} of the S_2.

Before the PWM signal from the voltage comparator going to the Synchronous Rectifier Buck Converter Circuit, the amplitude of these PWM signals has to be increased in order to turn ON the MOSFET. From the datasheet of IRF620 MOSFET, the input for the gate voltage (V_G) must be at least 10 V for the MOSFET to be turned ON. Figure 32 shows the PWM signals from the MOSFET Drive Circuit. Due to unstable PWM signal from the MOSFET Drive Circuit, the duty cycle of the both PWMs slightly fluctuated, however the duty cycle still can be adjusted by varying the value of the V_{ref} at the voltage comparator input.

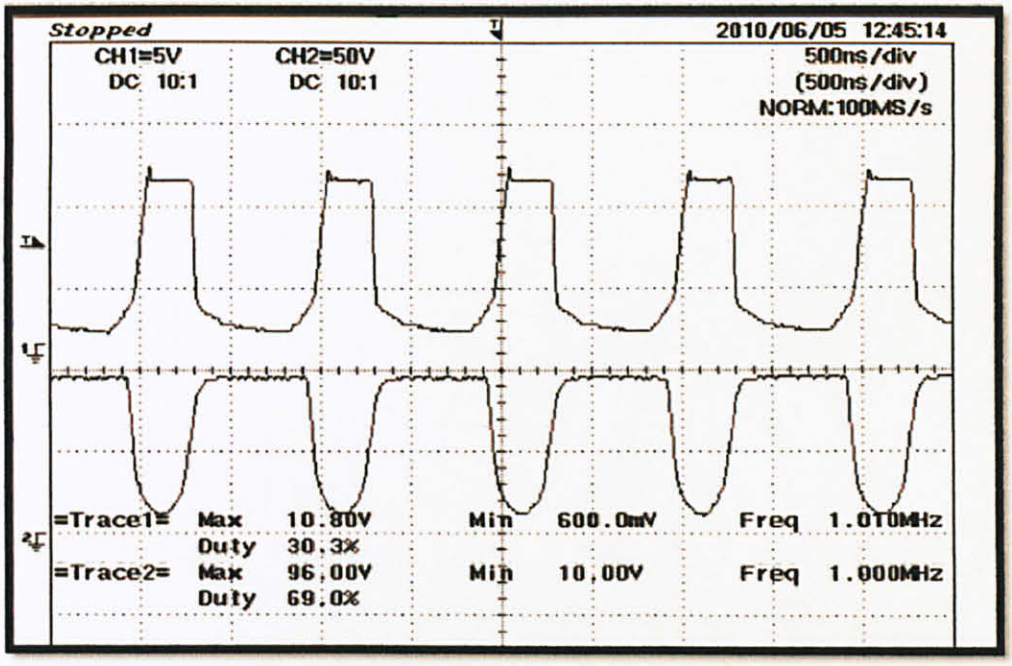

Figure 32 : PWM from the Synchronization Circuit

The Figure 33 shows the V_{gs} at the both side MOSFETs. The high side waveform is the V_{gs} at the S_1 and the low side waveform in the figure is the V_{gs} at the S_2. From the waveform signal in the Figure 33, notice that the waveform is not smooth compared to the gate voltage input due to internal losses in the MOSFET.

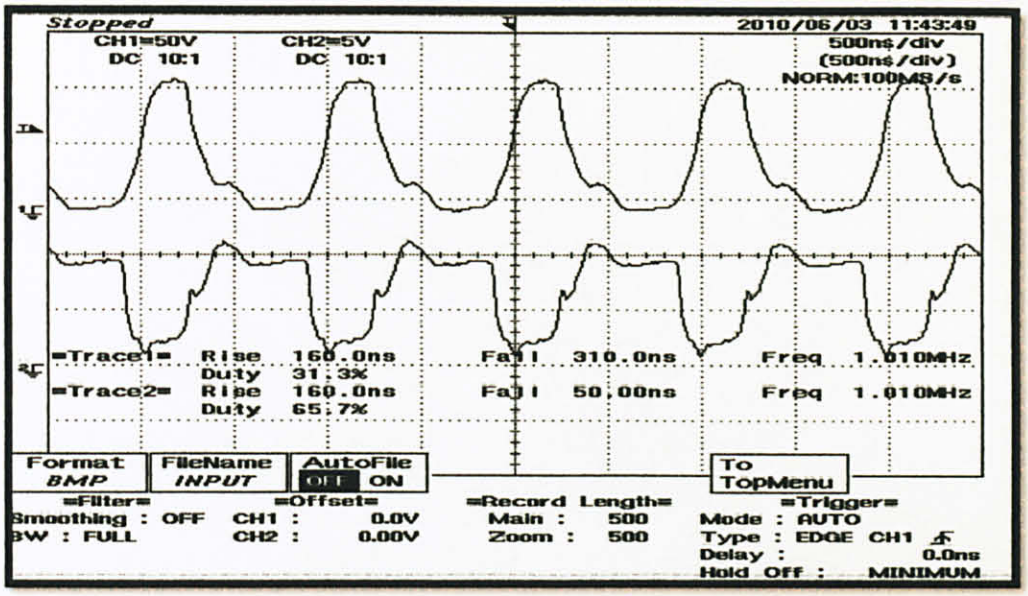

Figure 33: V_{gs} of the high side and low side MOSFETs at 1 MHz switching frequency

Even though the input for the SRBC circuit is successfully generated and integrated to the SRBC input, the MOSFET at the low side of the SRBC still having problem where the S_2 is unable to operate as desired. Because of the MOSFET at the low side in the SRBC is unable to function as the switch during the 1 MHz switching frequency, so the low side MOSFET has been replaced with a diode. The SRBC circuit now becomes the conventional buck converter circuit since the MOSFET at the low side in this experiment is unable to operate as desired. Figure 34 shows the circuit when S_2 is replaced with a diode.

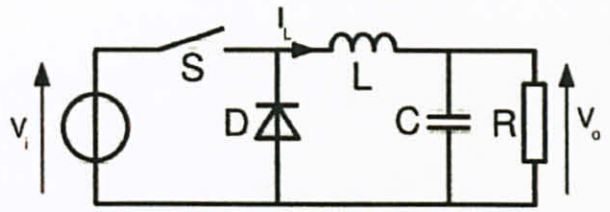

Figure 34: S_2 in SRBC replaced with the diode

Figure 35 shows the waveform of the output voltage (V_{out}) and output current (I_{out}) during the operation with 27% duty cycle input at the S_1. The circuit manages to step down the voltage source. The PWM signal is applied at the high side MOSFET have 27 % duty cycle. The V_{out} is about 5V and I_{out} is about 0.8A. The theoretical value should be about 12.96 V. The different for output voltage is significant and shows that this buck converter have low efficiency in high frequency switching operation.

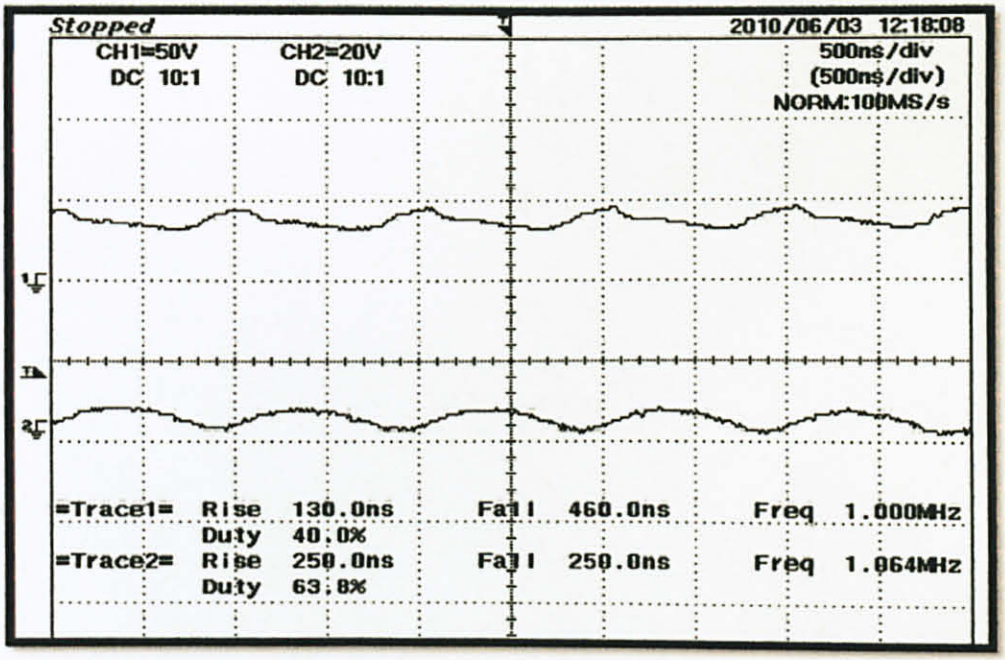

Figure 35: V_{out} and I_{out} in the converter circuit

Figure 36 shows the switching losses occurs at the high side MOSFET with the switching duration about 320ns. During the high side MOSFET is operating as the switch, there will be the switching loss occurs in the circuit. This switching loss can be calculated by using the formulae (3).

$$P_{SW} = \frac{1}{2} \times t_{SW} \times \text{Peak Power} \times f_{sw}$$

$$= \frac{1}{2} \times t_{SW} \times V_d \times I_d \times f_{sw}$$

$$= \frac{1}{2} \times 320\text{ns} \times 48\text{V} \times 1.5\text{A} \times 1\text{MHz}$$

$$= 11.52 \text{ Watt}$$

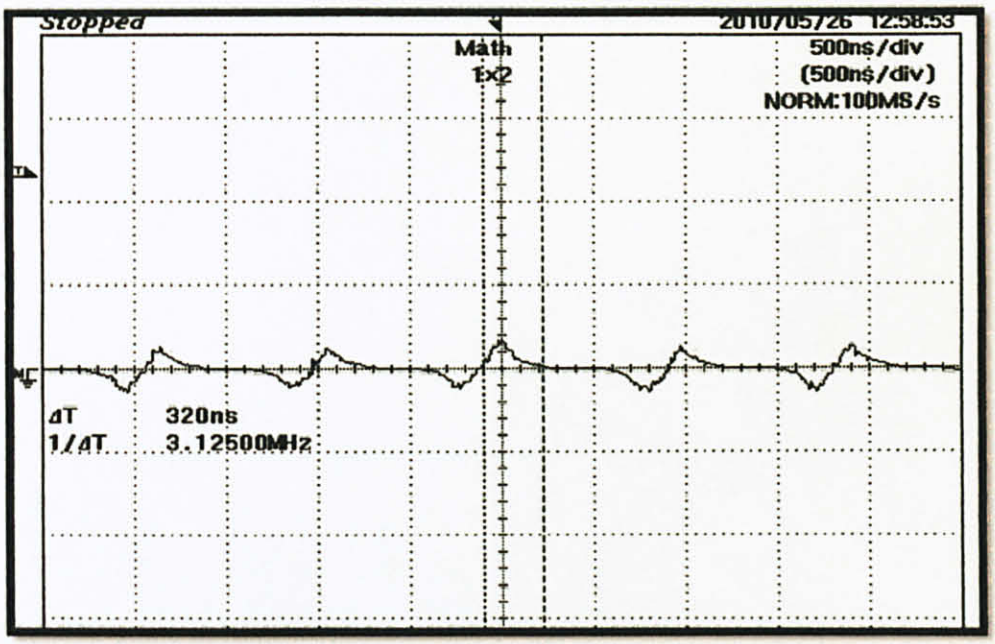

Figure 36: Switching loss occurs at the high side MOSFET

During high side MOSFET is turned ON, the current will flow through the drain–source resistance ($R_{DS(ON)}$). During the current flowing through the MOSFET, it dissipates power which is known as the conduction loss. The typical value of the $R_{DS(ON)}$ MOSFET used in this experiment is about 0.6 Ω. This conduction loss (P_{cond}) can be calculated by using the formulae (5).

$$P_{cond} = (I_{out})^2 \times R_{DS\,(ON)} \times (1\text{-}D)$$

$$\text{Since } D = \frac{Vout}{Vsource}$$

$$P_{cond} = (I_{out})^2 \times R_{DS\,(ON)} \times (1 - \frac{Vout}{Vsource})$$

$$= 0.8^2 \times 0.6 \times (1 - 5/48)$$

$$= 0.258 \text{ Watt}$$

Since the experimental circuit unable to display dead time delay due to problem at the S_2, the losses due to body diode is unable to be calculated. Total losses will be the summation of the P_{cond} and P_{sw}.

$$\text{Total losses} = P_{cond} + P_{sw}$$

$$= 11.78 \text{ Watt}$$

From the converter circuit, the input power for the circuit is about 469.6 Watt and the output power is about 4 Watt. The efficiency of the system is about 5.7% which is very low since the buck converter has low efficiency when operating in high frequency.

The table below show the comparison between the results of PDC experimental analysis and simulation analysis during the condition where duty cycle at S_1 is 27%.

Table 4 : Parameters measured in Simulation Analysis.

Parameters	Simulation Value		
Reference Voltage at comparator V_{ref}	0.27 V	0.4 V	0.8 V
Output voltage, V_{out}	11.074 V	13.226 V	14.23 V
Output current, I_{out}	1.1074 A	1.3226 A	1.423 A
Input Power, P_{in}	17.67 W	22.46 W	27.306 W
Output Power, P_{out}	11.533 W	14.991W	15.605 W
Dead Time Delay, t_d	0 ns	66 ns	260 ns
Body diode conduction period, t_{bd}	25 ns	82.5 ns	350 ns
Conduction Loss, P_{cond}	0.0689 W	0.092511 W	0.103997 W
Body Diode Losss, P_{bd}	0.0886 W	0.3490 W	1.5900 W
Total Switching Loss, P_{sw}	2.258 W	2.665 W	2.662 W
Total Loss, P_{total}	2.42 W	3.11 W	4.36 W

Table 5 : The experimental result

Parameters	Experimental Value
V_{out}	5 V
I_{out}	0.8 A
P_{in}	69.6 W
P_{out}	4 W
P_{cond}	0.258 W
P_{sw}	11.52 W
P_{total}	11.77 W

From the simulation results in Table 4, notice that when the V_{ref} is increase, the losses will also increase. This happen because the duty cycle of the PWM at S_2 will reduce when V_{ref} is increase, so the body diode conduction period will increase and the losses due to body diode conduction will increase as well.

Even though the low side switch in SRBC is unable to operate as desired, the analysis still continued by replacing the MOSFET at the low side with a diode. The losses due to body diode conduction unable to be calculated but the expected performance is highest during S_2 is at 73% or slightly less since the Dead Time is approximately zero during that condition.

4.2 Discussion

At the moment, the 27 % duty cycle and 73% duty cycle PWM have been applied to the S_1 and S_2 respectively at the Synchronous Rectifier Buck Converter (SRBC) switches. These PWM signals are able to be supplied at the right timing which is S_1 and S_2 is turned ON and turned OFF simultaneously.

The PWM signals with improved amplitudes have been produced and the MOSFETs are able to be turned ON and OFF. The problem is the S_2 unable to operate as the switch perfectly, so a diode used to replace the MOSFET. In simulation, the V_{ref} is changed in order to vary the duty cycle of the PWM at the S_2 but in the experimental verification, the main focus will be only on PWM duty cycle. This is because the values of V_{ref} in experimental totally are not similar with the simulation since there are few additional circuits in the experimental affecting the PWM duty cycle and because of the hardware limitation. Even though the experiment is not focusing on V_{ref}, the PWM still can be varied and the duty cycle still can be adjusted by varying the value of V_{ref}.

Even though the low side switch in SRBC is unable to operate as the switch, the analysis has been carried out by replacing the MOSFET at the low side with a diode. The efficiency of the converter is about 5% after replacing the MOSFET at the low side with the diode. The efficiency is low because the conventional buck converter is not suitable to operate in high frequency system. The overall losses are calculated by summation of switching loss and conduction loss which is about 11.77 W. The loss due to body diode conduction unable to be calculated but the highest performance expected during S_2 is at 73% duty cycle or slightly less since the Dead Time is approximately zero during that condition.

CHAPTER 5

CONCLUSSION AND RECOMMENDATION

5.1 Conclusion

The study is about to verify Predictive Control Scheme by doing experimental analysis of PDC in the gate driver design. From the study, theoretically the predictive concept uses the feedback to sense and adjust the dead time delay in the circuit wether to increase or decrease. The predictive part or the delay controller is unable to operate which explains why the duty cycle of the input at S_2 has to be adjusted manually.

In the experiment, the input or the Predictive Control Scheme part have been constructed and successfully able to generate the PWM with different duty cycle which is the t_d can be varied and measured. However, the MOSFET at the low side is unable to operate as it has been replaced with a diode. This occurs due to unstable signal of PWM when going through the MOSFET and *shoot through* phenomenon is happened. The analysis for the experimental is done without the P_{bd} losses due to the low side MOSFET in SRBC is unable to work as desired.

Since the main contribution of the losses in the PDC is on Body Diode Conduction Loss, the expected result for the experimental analysis in order to have highest efficiency is when the PWM at S_2 is 73% since the PWM at S_1 is fixed at 27%. This is because of the approximately there are no Dead Time during that condition.

5.2 Recommendations

There are several recommendations for future work:

1. Redesign the simulation circuit with to have the Delay Controller in order for predicting and adjusting the Dead Time $_{in}$ the circuit design.
2. Since the experimental circuit for the Predictive Control Scheme has been constructed and the problem is the S_2 at the SRBC, the circuit for SRBC has to be reconstructed by using high speed and high efficiency MOSFET.
3. The experimental circuit for SRBC also has to be designed by using the equipments that can stand up to 3A operation since the temperature of the components increasing significantly during operation.

REFERENCES

[1] S. Mappus, "Predictive Gate Drive Boost Synchronous DC/DC Power converter Efficiency", Texas Instruments, Inc. *App. Report SLUA281*, pp 1 – 25, Feb 2003.

[2] B. Ramachandran & D. Maksimovic, "Dynamic Operation of Sensorless Dead – *CoPEC Annual meeting*, pp.1 – 15, Nov 9 2006.

[3] S. Y. Liang, H. S. Chu & K. C. Hung, "Circuit Method for Predicting Dead Time", *United States Patent,* Patent No: US 7053632b1, pp. 1-11, May 2006.

[4] A. Elbanhawy, "Cross Conduction in Modern Power MOSFETs", *Maplesoft Inc., Application Demonstration*, pp 1-10, March 9 2008.

[5] N.Z. Yahaya, K.M. Begam & M. Awan, " Investigation of High Frequency Effects on Soft-Switched Synchronous Rectifier Buck Converter", *IEEE Symposium on Industrial Electronics and Applications (ISIEA 2009)*, pp 1 – 5, October 2009.

[6] A. Elbanhawy, "MOSFET Susceptibility to Cross Conduction", *Power Electronics Technology*, pp 1-10, March 9, 2008.

[7] M. Xu, J. Zhou, Y. Qiu, K. Yao and F. C. Lee, " Resonant Synchronous Rectification for High Frequency DC/DC Converter", *Applied Power Electronics Conferences and Exposition*, Vol. 2, pp 865 – 871, 2004

[8] M.L. Chiang, L.C. Fu, "Adaptive Control of Switched Systems with Application to HVAC Systems", *Control Application, 2007, IEEE International Conference,* pp 367-372, Oct.2007.

[9] S. Mappus, "predictive Gate Drive Boost Synchronous DC/DC Power converter Efficiency", Texas Instruments, Inc. *App. Report SLUA281*, pp 1 – 25, Feb 2003.

[10] Altera Corporation. (2009, Oct. 28). *Power Supply Regulation* [Online]. Available: http://www.altera.com/support/devices/power/regulators/pow-regulators.html.

[11] Maxim Integrated Products, "High-Speed, Low-Power, 3V/5V, Rail-to-Rail Single-Supply Comparators", MAX944 data sheet.

[12] Fairchild Semiconductor, "33A, 200V, 0.085 Ohm, N-Channel Power MOSFET", IRF620 MOSFET data sheet.

[13] John Bottrill, " Synchronization Circuit for Power Converters", Texas Instruments, Inc., *App. Report SLUA296,* pp 1- 7, Oct 2003.

[14] Stefan Spannare. (2010, May 7). *Power PWM Drivers* [Online]. Available:http://www.picotech.com/applications/pwm_drivers/.

APPENDICES

Appendix A

Gantt chart for FYP 1

Activities/Milestone	Week Number	1	2	3	4	5	6	7	8	9		10	11	12	13	14	15
		20/07-26/07	27/07-02/08	03/07-09/07	10/08-16/08	17/08-23/08	24/08-30/08	31/08-06/09	07/09-13/09	14/09-20/09	21/09-27/09	28/09-04/10	05/10-11/10	12/10-18/10	19/10-25/10	26/10-01/11	02/11-08/11
Confirmation of Title selection				H1N1 EMERGENCY BREAK							MID SEMESTER BREAK						
Literature Review																	
Preparation and Submission of the Preliminary Report																	
Project Work (Research and Circuit Design)																	
Preparation and Submission of Progress Report																	
Continue on Project (Circuit Construction)																	
Seminar of FYP1																	
Preparation and Submission of Interim Report																	
Submission of Draft Report																	
Oral Presentation																	

Appendix B: Gantt Chart for FYP II

Week 1 Activities/Milestone	1 25/1 – 31/1	2 1/2 – 7/2	3 8/2-14/2	4 15/2 – 21/2	5 22/2 – 28/2	6 1/3 – 7/3	7 8/3 – 14/3	8 15/3 – 21/3	9 22/3 – 28/3	10 29/3 – 4/4	11 5/4 – 11/4	12 12/4 – 18/4	13 19/4 -25/4	14 26/4 – 2/5	15 3/5 – 9/5	17 10/5 – 16/5	21 7/6 – 13/6	22 14/6 – 20/6	23 21/6 – 26/6
Continuation of Project								MID SEMESTER BREAK											
Literature Review and Methodology																			
Preparation and Submission of Progress Report 1																			
Preparation and Submission of Progress Report 2																			
Preparation and Submission of Draft																			
Preparation and Submission of Final Report (Soft)																			
Technical Report																			
Oral Presentation																			
Preparation and Submission of Thesis (Hard)																			