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Improved Reliability Tool for Fault Tolerance Computation

by

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Dissertation submitted in partial fulfillment of the
requirements for the
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CERTIFICATION OF APPROVAL

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Approved by,

(Mr. Narinderjit Singh)

UNIVERSITI TEKNOLOGI PETRONAS
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May 2014

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the reference and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

AKMURAT AGAMAMEDOV

ABSTRACT

As a size of CMOS transistors in electronic circuits reduced, certainly, the reliability of circuit will decrease as well. Therefore, during designing stage measuring reliability becomes important subject as it will save time and cost of manufacturing. In current literature several reliability models are available. From these models Probabilistic Transfer Matrix (PTM) model gives results more quicker and more accurate compare to others. But these tools measures circuit reliability on manual basis. This project aims to generalize PTM model by creating a tool using Matlab programming language that will measure reliability on Auto-basis. For circuits reliability computation user need to provide netlist of circuit in the form of Gate Sequence Matrix (GSM), Circuit Specification Matrix (CSM) and Gate Location Matrix (GLM). Number of inputs, number of outputs, types of logic gates, their interconnection and layout of logic gates in the circuit described in the netlist of circuit. Reliability tool measures circuit performance in a short period of time compare to conventional manual calculations. Several benchmark test circuits such as C17, Full Adder and 2-4 Decoder simulated in order to calculate reliability of the circuit.

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ABBREVIATION AND NOMENCLATURES:

PTM	-	Probabilistic Transfer Matrix
ITM	-	Ideal Transfer Matrix
CMOS	-	Complementary Metal-Oxide-Semiconductor
FTC	-	Fault Tolerant Computing
VLSI	-	Very Large Scale Integrated Circuit
IEEE	-	Institute of Electrical and Electronics Engineering
MATLAB	-	MATLAB programming language
PGM	-	Probabilistic Gate Model
BDEC	-	Boolean Difference-based Error Calculator
BN	-	Boolean Network
CSM	-	Circuit Specification Matrix
GSM	-	Gate Sequence Matrix
GLM	-	Gate Location Matrix
Rel	-	Reliability

CHAPTER 1

INTRODUCTION

As a number of logic gates in ICs increasing and size of CMOS transistors reduced into nano-scale, performance of Integrated Circuit decreases, thus at the same time the reliability also will decrease. This is becoming a challenge for designers to design more reliable circuits with nano-scale CMOS transistors [1]. That is why the importance of measure circuit's reliability at designing stage of circuit manufacturing becomes serious attention [2]. There are several tools in a literature used to measure the reliability of circuit. Among these tools Probabilistic Transfer Matrix (PTM) is the most accurate and less time consuming compare to others [3].

1.1 Background study

Fault Tolerant Computing (FTC) researches gained attention starting from 1950s. A wide area of researches done related to Fault tolerant computation and Probabilistic analysis of logic circuits. Especially research on analysis of logic gate probability can be classified into 3 areas [4] : modeling of circuits in probabilistically behavioral analysis, circuit simulations, fault-tolerant structure. For computing reliability of circuits some works done in the different modeling such as Bayesian Network model, Probabilistic Gate Model, Boolean Network and Boolean difference based error calculation.

Another work which is described in [5], this model concentrates on physical effect of transient errors to the Very Large Scale Integrated Circuits (VLSI). In this model simulator with timing datas used to inserting faults to each of the logic gate separately, individually.

For a moment manner, measurement of reliability of the circuit performing on manual basis. Therefore, it is consuming more time to measure reliability. By generalizing PTM model it is possible to reduce computation time.

1.2 Problem Statement

Performance and quality of any system depends on it`s reliability. Available reliability evaluation tools in current literature able to measure on manual basis. In order to save time that wasted for calculation, need to create a tool that able to measure on auto-basis. By generalizing Probabilistic Transfer Matrix (PTM) method which represents the errors of the logic gate in the form of matrix, we can significantly decrease the time for calculation of reliability of the circuit [3].

1.3 Objectives:

1. To develop a Matlab-based simulation tool in the form of PTM model to measure reliability of circuit system.

1.4 Scope of study

In electronic systems 2 types of transistors are available. They are analog and digital transistors. This research paper focuses on reliability measure of digital transistors. Needed to create a tool, which is able to calculate reliability of a given circuit by using PTM method. In methodology explanation will be provided for details described above.. Identifying the type of failure, fault and challenges with dealing them are not covered in this research paper.

CHAPTER 2

LITERATURE REVIEW

Electronic circuit consists of semiconductor components such as transistors, resistors, capacitors and so on. These components describe the logic gates that can perform logical operations. Logic gate have one or more inputs and one output. To compute the reliability of logic gates and circuit various types of reliability tools have been developed such as Bayesian Network model, Probabilistic Gate Model, Boolean Network and Boolean difference based error calculation [3,5]. PTM method is used in our project because PTM gives significantly adequate reliability measure compare to other models [2,7]. PTM is based on matrix representation at which rows at matrix represents inputs of logic gate and columns of matrix represents outputs of logic gate [2,3,4].

In order to ensure the success of the project, it is necessary to understand the components of circuit and connection of wires so that tool will give correct solution. As the circuit is going to be described in **PTM** (Probabilistic Transfer Matrix) model, criterias such as: **ITM** (Ideal Transfer Matrix), **PTM**, **Fan out**, **Wire Swapping**, **Sub-circuit**, **Tensor** (Kronecker) **Product** explained below.

2.1 ITM :

If logic gate is ideal which means No fault occur, then it called (ITM) Ideal Transfer Matrix [4]. According to the logic gate operation, PTM and ITM is possible to apply to any logic gate in the circuit [7,10]. ITM of logic gates of circuit in *FIGURE 1* is shown in Eq.(1-6). Rows represent the input values of Logic gates and columns represent the output value.

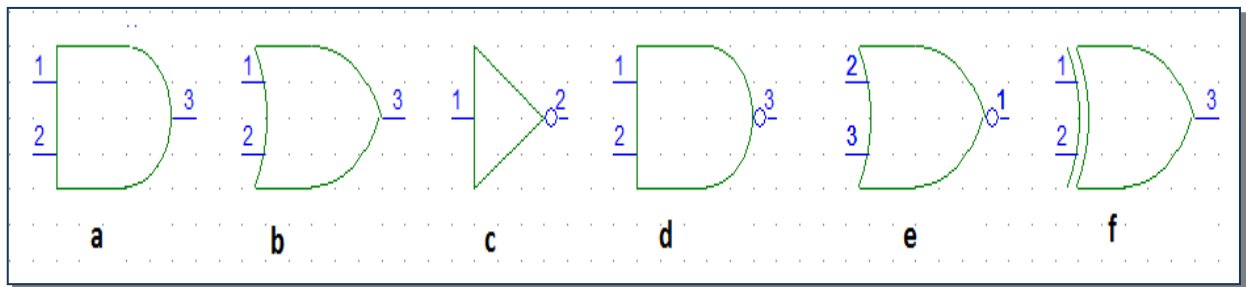


FIGURE 1. Logic Gates

a)AND gate, b)OR gate, c)NOT gate, d)NAND gate, e)NOR gate and f)XOR gate

$$\text{ITM(AND gate)} = \begin{bmatrix} 1 & 0 \\ 1 & 0 \\ 1 & 0 \\ 0 & 1 \end{bmatrix} \quad (1)$$

$$\text{ITM(OR gate)} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ 0 & 1 \\ 0 & 1 \end{bmatrix} \quad (2)$$

$$\text{ITM (NOT gate)} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \quad (3)$$

$$\text{ITM (NAND gate)} = \begin{bmatrix} 0 & 1 \\ 0 & 1 \\ 0 & 1 \\ 1 & 0 \end{bmatrix} \quad (4)$$

$$\text{ITM(NOR gate)} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \\ 1 & 0 \\ 1 & 0 \end{bmatrix} \quad (5)$$

$$\text{ITM (XOR gate)} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ 0 & 1 \\ 1 & 0 \end{bmatrix} \quad (6)$$

2.2 PTM

PTM differs from ITM with its error probability value representation in matrix. Character “e” in the matrix means the “error” probability of circuit. Following matrices (7-12) are representation of PTM of the logic gates.

$$\text{PTM(AND gate)} = \begin{bmatrix} 1-e & e \\ 1-e & e \\ 1-e & e \\ e & 1-e \end{bmatrix} \quad (7)$$

$$\text{PTM(OR gate)} = \begin{bmatrix} 1-e & e \\ e & 1-e \\ e & 1-e \\ e & 1-e \end{bmatrix} \quad (8)$$

$$\text{PTM(NOT gate)} = \begin{bmatrix} e & 1-e \\ 1-e & e \end{bmatrix} \quad (9)$$

$$\text{PTM(NAND gate)} = \begin{bmatrix} e & 1-e \\ e & 1-e \\ e & 1-e \\ 1-e & e \end{bmatrix} \quad (10)$$

$$\text{PTM(NOR gate)} = \begin{bmatrix} e & 1-e \\ 1-e & e \\ 1-e & e \\ 1-e & e \end{bmatrix} \quad (11)$$

$$\text{PTM}(\text{XOR gate}) = \begin{bmatrix} 1-e & e \\ e & 1-e \\ e & 1-e \\ 1-e & e \end{bmatrix} \quad (12)$$

2.3 Fan out and Swapping

Fan-out is an output of logic gate that can feed input of another logic gates more than one. [12], FIGURE2. N number of output fan-out gate written as F_n

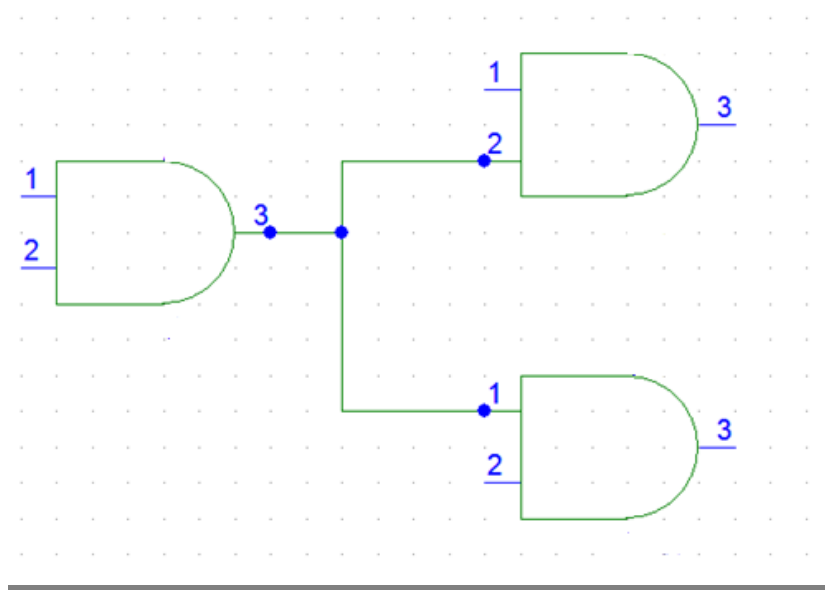


FIGURE 2. AND gate output Fan out feeds another 2 AND gate

Only wires can be fan out, that is why we assume that wires has no error, ITM of Fan-out is in Eq.(13), There is no PTM of Fan-out.

$$\text{ITM}(\text{Fan out}) = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \quad (13)$$

Wire Swapping is the crossing of wires across each other Figure 3. As same as Fan out, Wire swapping also assumed to be No error. ITM of Swap is given in Eq. (14)

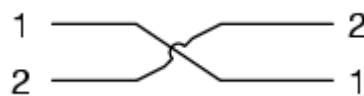


FIGURE 3. Wire Swapping

$$\text{ITM}(\text{Swap}) = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \quad (14)$$

2.4 Sub-circuit

In order to calculate reliability of circuit, the circuit need to be divided manually into parts or sub-circuit properly. In *FIGURE 4* shows division of simple circuit into parts.

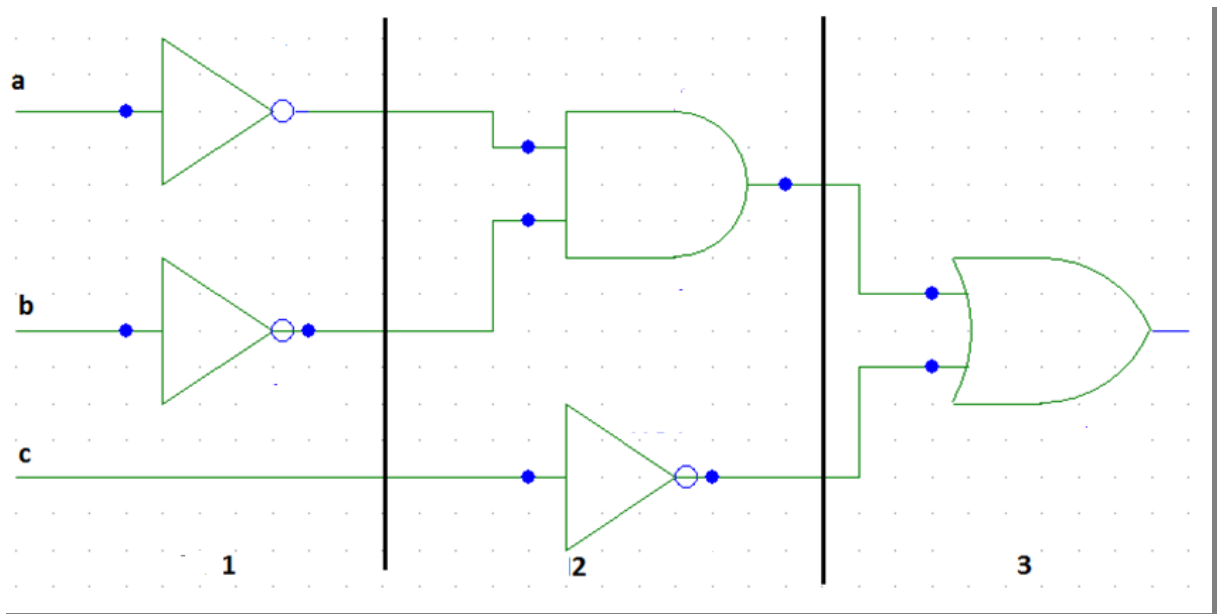


FIGURE 4. Circuit and Its Sub-circuits 1,2,3

2.5 Tensor (Kronecker) Product

Components in the circuit are connected in different layouts. Components which are connected serial we use straightforward multiplication of component PTM, for Parallel connected components we use tensor product of PTMs [13]. *FIGURE 5*.

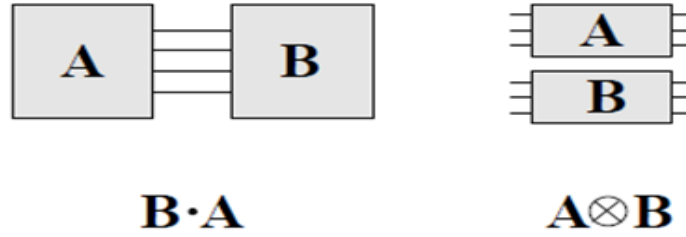


FIGURE 5. Connection of Components of Circuit

Tensor product or another name is Kronecker product is denoted by \otimes symbol. Kronecker product of 2x2 A matrix and 2x2 B matrix, explained briefly in Eq. (15).

$$A = \begin{bmatrix} a1 & a2 \\ a3 & a4 \end{bmatrix}, B = \begin{bmatrix} b1 & b2 \\ b3 & b4 \end{bmatrix}, A \otimes B = \begin{bmatrix} a1b1 & a1b2 & a2b1 & a2b2 \\ a1b3 & a1b4 & a2b3 & a2b4 \\ a3b1 & a3b2 & a4b1 & a4b2 \\ a3b3 & a3b4 & a4b3 & a4b4 \end{bmatrix} \quad (15)$$

Thus PTM for circuit in *FIGURE 5* will be as shown in Eq.(16-18). Number at the end of gate naming means number of inputs to that gate, for example AND2 means AND gate with 2 inputs. I stands for Identity wire.

$$PTM1 = NOT \otimes NOT \otimes I \quad (16)$$

$$PTM2 = AND2 \otimes NOT \quad (17)$$

$$PTM3 = OR2$$

$$\text{Overall PTM} = (PTM1)(PTM2)(PTM3) = (NOT \otimes NOT \otimes I)(AND_2 \otimes NOT)(OR_2) \quad (18)$$

CHAPTER 3

METHODOLOGY

After identifying the type of problem that needs to be faced and defining the project objective (Introduction Section), basic ideas of the overall work layout was obtained through research (Literature Review Section). Now it is clearly understood the principle of computing Reliability of the circuit.

In this Methodology section, planning of the future project work is briefly discussed and elaborated. Project flow chart, components of circuit, their interconnection and necessary equations for calculating reliability in the form of PTM model will be clearly identified and evaluated.

3.1. Project Flow chart

The flowchart below in *FIGURE 6* shows the step-by-step progress of the project starting from the Circuit Netlist up to the calculation of Reliability of Circuit. Closely following these steps is the only way to achieve satisfactory results.

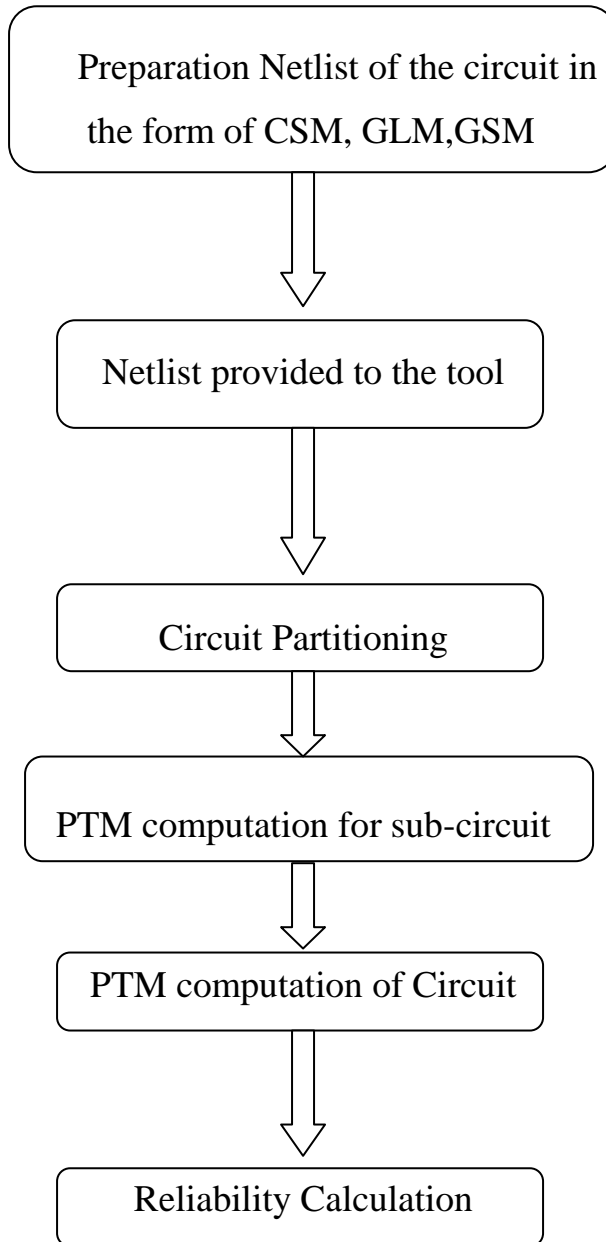


FIGURE 6. Project Flow Chart

3.2 Circuit Netlist

Circuit specification and components are provided in the form of Netlist. Netlist of C17 should be provided in the form of CSP, GSM and GLM. To each of this matrices we will look through C17 circuit as shown in FIGURE 7.

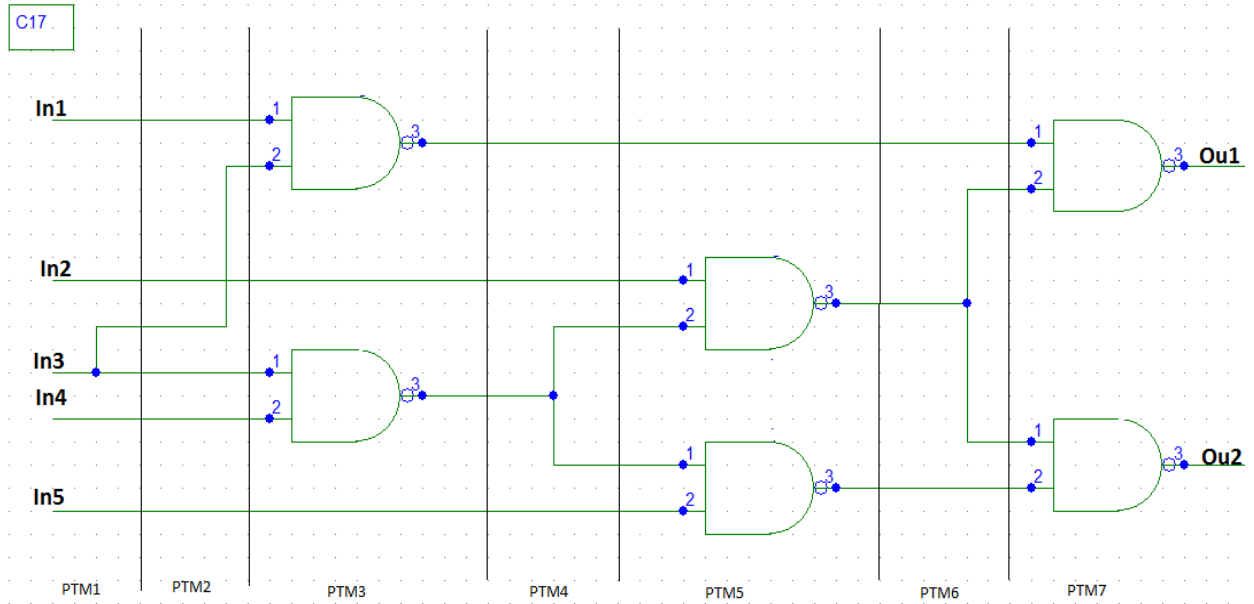


FIGURE 7. C17 Circuit

CSM: Circuit Specification Matrix is the description of interconnection of logic gates between each other and interconnection with input and outputs in C17 circuit. In the CSM as shown below in Eq.(19), “1” denotes a connection between logic gates and “0” denotes that there is no-connection.

Rows from top to down representing the input signals, types of logic gates and number of outputs of the circuit. Columns from left to right representing the types of logic gates and number of outputs [2,4].

	NA1	NA2	NA3	NA4	NA5	NA6	OU1	OU2
IN1	1	0	0	0	0	0	0	0
IN2	0	0	1	0	0	0	0	0
IN3	1	1	0	0	0	0	0	0
IN4	0	1	0	0	0	0	0	0
IN5	0	0	0	1	0	0	0	0
CSM = NA1	0	0	0	0	1	0	0	0
NA2	0	0	1	1	0	0	0	0
NA3	0	0	0	0	1	1	0	0
NA4	0	0	0	0	0	1	0	0
NA5	0	0	0	0	0	0	1	0
NA6	0	0	0	0	0	0	0	1
OU1	0	0	0	0	0	0	0	0
OU2	0	0	0	0	0	0	0	0

(19)

GSM: Gate Sequence Matrix describes types of gates in the circuit from left to right. Logic gates represented by first 2 alphabets [3,4,7]. NA for NAND gate, AN for AND gate, XO for XOR (Exclusive OR) gate, OU for Output. In Eq.(20) shown GPM of C17 benchmark test circuit.

$$\text{GSM} = [\text{NA}, \text{NA}, \text{NA}, \text{NA}, \text{NA}, \text{NA}, \text{OU}, \text{OU}] \quad (20)$$

GLM: Gate Location Matrix represents number of logic gates in each sub-circuit. In C17, sub-circuits PTM3 has 2 logic gates, PTM5 has 2 logic gates and PTM7 has 2 logic gates at each. In matrix eq (21) it shows how GLM is written.

$$\text{GLM} = [2 \ 2 \ 2] \quad (21)$$

At the beginning as we mentioned , Netlist of circuit will be given in the form of CSM, GLM and GSM. Code shown below determines number of input, types of logic gates and number of logic gates from given Netlist of circuit C17.

```
GSM=['NA','NA','NA','NA','NA','NA','OU','OU']
CSM=[1 0 0 0 0 0 0 0;0 0 1 0 0 0 0 0;1 1 0 0 0 0 0 0;0 1 0 0 0 0 0 0;0 0 0 1 0 0 0 0;0 0 0 0 1 0 0 0;0 0 1 0 0 0 0 0;0 0 1 1 0 0 0 0;0 0 0 0 1 1 0 0;0 0 0 0 0 1 0 0;0 0 0 0 0 0 1 0;0 0 0 0 0 0 0 1;0 0 0 0 0 0 0 0;0 0 0 0 0 0 0 0]
GLM=[2 2 2]

F2=[1 0 0 0;0 0 0 1];
F3=[1 0 0 0 0 0 0 0;0 0 0 0 0 0 0 1];
I=[1 0;0 1];
S=[1 0 0 0;0 0 1 0;0 1 0 0;0 0 0 1];

e=0.05;
AN=[1-e e;1-e e;1-e e;e 1-e];
OR=[1-e e;e 1-e;e 1-e;e 1-e];
XO=[1-e e;e 1-e;e 1-e;1-e e];
NA=[e 1-e;e 1-e;e 1-e;1-e e];
NO=[e 1-e;1-e e];

[m,n]=size(CSM);

IdxOU=strfind(GSM,'OU');
NoOutput=length(IdxOU);
[t,z1]=size(GSM);
z=z1/2;
LogGates=z-NoOutput

for i=1:2:LogGates*2 only
    fprintf('LogicGate%d=%s\n',floor(i/2)+1,GSM(i:i+1));
end
NoInput=m-n
[q,t]=size(GLM);
```

Next step is, Tool determines division of circuit into sub-circuits. Tool divides C17 into 7 sub-circuits as shown in *FIGURE 7*.

Tool computes PTM of each component starting from sub-circuit 1 (PTM1). From top to down it calculates Tensor Product of components. Each sub-circuit's PTM tool calculates separately and computes overall PTM of Circuit. From Overall PTM it calculates the Reliability of the circuit. Let's look to first 3 sub-stages which are PTM1, PTM2 and PTM3. How tool determines components and their interconnection briefly explained below.

PTM 1 :

This is wires only and Fan-out stage. *FIGURE 8*. Tool determines only the identity wire and Fan-out at that stage. Program code shown below determines whether only line of fan-out. The same code computes reliability PTM1 for 1st sub-circuit.

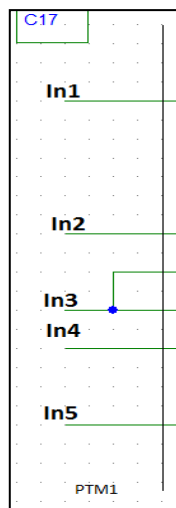


FIGURE 8. PTM1of C17 circuit

```
Z=1;
D=[];
for i=1:NoInput
    b = sum(CSM(i,:));
    if b == 1
```

```

        y = I;
        D = [D;{y}];
        Z=sort([Z i]);
    else
        y = F2;
        D = [D;{y}];
        Z=sort([Z i i]);
    end
    Z
    [a,b]=size(Z);
    A=Z(1,2:b);
end
A
D;
[ai,aj]=size(A)

c = size(D, 1);
PTM1 = 1;
if c > 1
    for i = 1:c-1
        if i > 1
            PTM1 = kron(PTM1, D{i+1,1});
        else
            PTM1 = kron (D{i,1}, D{i+1,1});
        end
        PTM1;
    end
end
PTM1;

```

Code creates at the output of PTM1 a matrix A, shown in Eq. (23). This matrix represents the number of inputs to next stage and their relationship with PTM1 stage. Here in matrix A has digits from 1 to 5, means number of inputs into PTM1, but total number of elements in A is 6, which is digit 3 repeated 2 times. It means that input 3 is fan-out. Tool computes the PTM of stage as (22). The same procedure goes to PTM4 as well.

$$PTM1= I \otimes I \otimes F2 \otimes I \otimes I \quad (22)$$

$$A = \begin{bmatrix} 1 \\ 2 \\ 3 \\ 3 \\ 4 \\ 5 \end{bmatrix} \quad (23)$$

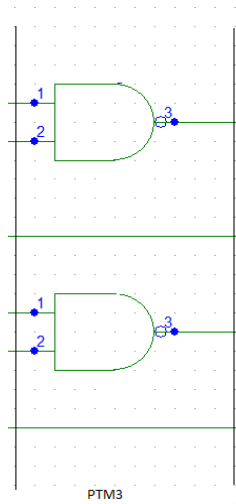


FIGURE 9. PTM3 of C17 circuit.

PTM 3:

This is Logic gates and identity wires stage. Code shown below identifies type of logic gate and identity wire.

```

if GLM(1)==2;
  for j=1:2;
    for i=1:NoInput
      if CSM(i,j) == 1
        s=sum(CSM(i:NoInput,j));
        if s == 2
          g = GSM(2*j-1:2*j);
          y = eval(g);
          F = [F;{y}];
        end
      elseif CSM(i,j) == 0;
        if CSM(i,j+2) == 1;
          y = I;
          F = [F;{y}];
        end
      end
    end
  end
end
end
end
end
end
end

```

```

c = size(F, 1);
PTM3 = 1;
if c > 1
    for i = 1:c-1;
        if i > 1;
            PTM3 = kron(PTM3, F{i+1,1});
        else
            PTM3 = kron(F{i,1}, F{i+1,1});
        end
        PTM3;
    end
end
PTM3;

```

Code computes the Kronecker product of that stage as Eq (24). Code creates a matrix B , which represent the Input of that stage in Eq (25). In matrix from top to down , numbers represents to which input of circuit connected components of PTM3. Elements of matrix from top to down 1st element 1 is connected to Input 1 of the circuit, 2nd element 3 is connected to Input 3 of circuit, 3rd element 2 is connected to Input 2 of circuit and so on. Same procedure goes to PTM5 and PTM7.

$$PTM3 = NA \otimes I \otimes NA \otimes I \tag{24}$$

$$B = \begin{bmatrix} 1 \\ 3 \\ 2 \\ 3 \\ 4 \\ 5 \end{bmatrix} \tag{25}$$

PTM 2:

This is the interconnection stage, which consists of identity wires and swaps. FIGURE 10. Fan-out and swaps can not be placed in the same stage , because tensor product of the stage and following stage will not be possible to be multiplied, thus will give us

incorrect result. Tool Compares each location value of matrix A with the same location value of matrix B.

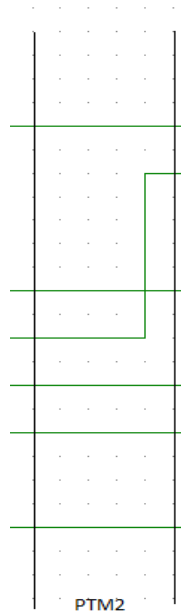


FIGURE 10. PTM2 of C17 circuit

According to comparison identifies swap and identity wire. In matrix A (23) and matrix B (25) only 2nd and 3rd elements are Not same, thus means Swapping of wires occur. The rest elements are same which means identity wire. Thus at the end tool gives us PTM of the stage as Eq (26). Following code makes comparison of matrices A and B, and computes PTM2 for 2nd sub-circuit of C17. This same procedure applied for following swaps and wires stages as well.

```

for i=1
    E=[];
    for j=1:bj;
        if A(1,j)==B(1,j)
            y = I;
            E = [E;{y}];
        elseif A(1,j)~=B(1,j);
            if A(1,j+1)~=B(1,j+1);
                y = S;
                E = [E;{y}];
            end
        end
    end
end
end

```

```

end
E
c = size(E, 1);
PTM2 = 1;
if c > 1
    for i = 1:c-1;
        if i > 1;
            PTM2 = kron(PTM2, E{i+1,1});
        else
            PTM2 = kron (E{i,1}, E{i+1,1});
        end
        PTM2;
    end
end
PTM2;

```

$$PTM2= I \otimes S \otimes I \otimes I \otimes I \quad (26)$$

Tool identifies components and their interconnection in the following stages in similar way as described above. Number of sub-circuits tool determines from GLM elements and its size.

For C17 Tool computes Circuit Overall PTM as (27) and Reliability of Circuit with 5% logic gate error probability ($e=0.05$) with the code shown below:

$$PTM=PTM1*PTM2*PTM3*PTM4*PTM5*PTM6*PTM7 \quad (27)$$

0	0	0	0	0	0.0025	0	0.0475	0	0	0	0
0	0	0	0	0.0475	0	0.0025	0	0	0	0	0
0	0	0	0	0	0.0475	0	0.0025	0	0	0	0
0.0025	0	0.0475	0	0	0	0	0	0.0475	0	0.9025	0
0	0.0025	0	0.0475	0	0	0	0	0	0.0475	0	0.9025
0.0025	0	0.0475	0	0	0	0	0	0.0475	0	0.9025	0
0	0.0025	0	0.0475	0	0	0	0	0	0.0475	0	0.9025
0.0025	0	0.0475	0	0	0	0	0	0.0475	0	0.9025	0
0	0.0025	0	0.0475	0	0	0	0	0	0.0475	0	0.9025
0.0475	0	0.0025	0	0	0	0	0	0.9025	0	0.0475	0
0	0.0475	0	0.0025	0	0	0	0	0	0.9025	0	0.0475
0	0	0	0	0.0025	0	0.0475	0	0	0	0	0
0	0	0	0	0	0.0025	0	0.0475	0	0	0	0
0	0	0	0	0.0025	0	0.0475	0	0	0	0	0
0	0	0	0	0	0.0025	0	0.0475	0	0	0	0
0	0	0	0	0	0.0025	0	0.0475	0	0	0	0
0	0	0	0	0	0.0025	0	0.0475	0	0	0	0
0	0	0	0	0	0.0475	0	0.0025	0	0	0	0
0	0	0	0	0	0.0475	0	0.0025	0	0	0	0
0.0475	0	0.9025	0	0	0	0	0	0.0025	0	0.0475	0
0	0.0475	0	0.9025	0	0	0	0	0	0.0025	0	0.0475
0.0475	0	0.9025	0	0	0	0	0	0.0025	0	0.0475	0
0	0.0475	0	0.9025	0	0	0	0	0	0.0025	0	0.0475
0.0475	0	0.9025	0	0	0	0	0	0.0025	0	0.0475	0
0	0.0475	0	0.9025	0	0	0	0	0	0.0025	0	0.0475
0.9025	0	0.0475	0	0	0	0	0	0.0475	0	0.0025	0
0	0.9025	0	0.0475	0	0	0	0	0	0.0475	0	0.0025
0	0	0	0	0.0475	0	0.9025	0	0	0	0	0
0	0	0	0	0	0.0475	0	0.9025	0	0	0	0
0	0	0	0	0.0475	0	0.9025	0	0	0	0	0
0	0	0	0	0	0.0475	0	0.9025	0	0	0	0
0	0	0	0	0	0.0475	0	0.9025	0	0	0	0
0	0	0	0	0	0.0475	0	0.9025	0	0	0	0
0	0	0	0	0.9025	0	0.0475	0	0	0	0	0
0	0	0	0	0	0.9025	0	0.0475	0	0	0	0

Columns 13 through 16

0	0	0	0
0	0	0	0
0	0	0	0
0	0	0	0
0	0	0	0
0	0	0	0
0	0	0	0
0	0	0	0
0.0475	0	0.9025	0
0	0.0475	0	0.9025
0.0475	0	0.9025	0
0	0.0475	0	0.9025
0.0475	0	0.9025	0
0	0.0475	0	0.9025
0.9025	0	0.0475	0
0	0.9025	0	0.0475
0	0	0	0
0	0	0	0
0	0	0	0
0	0	0	0
0	0	0	0
0	0	0	0
0	0	0	0
0	0	0	0
0	0	0	0
0.0475	0	0.9025	0
0	0.0475	0	0.9025
0.0475	0	0.9025	0
0	0.0475	0	0.9025
0.0475	0	0.9025	0
0	0.0475	0	0.9025
0.9025	0	0.0475	0
0	0.9025	0	0.0475

```

0      0      0      0
0      0      0      0
0      0      0      0
0      0      0      0
0      0      0      0
0      0      0      0
0      0      0      0
0      0      0      0
0      0      0      0
0.0475 0 0.9025 0
0 0.0475 0 0.9025
0.0475 0 0.9025 0
0 0.0475 0 0.9025
0.0475 0 0.9025 0
0 0.0475 0 0.9025
0.9025 0 0.0475 0
0 0.9025 0 0.0475
0      0      0      0
0      0      0      0
0      0      0      0
0      0      0      0
0      0      0      0
0      0      0      0
0      0      0      0
0      0      0      0
0.0025 0 0.0475 0
0 0.0025 0 0.0475
0.0025 0 0.0475 0
0 0.0025 0 0.0475
0.0025 0 0.0475 0
0 0.0025 0 0.0475
0.0475 0 0.0025 0
0 0.0475 0 0.0025

```

Tool gives result for PTM4 (in code given as PTMa2) is 16x32 matrix:

PTMa2 =

Columns 1 through 20

```

1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0

```

Columns 21 through 32

```

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

```

```

0 0 1 0 0 0 0 0 0 0 0 0
0 0 0 1 0 0 0 0 0 0 0 0
0 0 0 0 1 0 0 0 0 0 0 0
0 0 0 0 0 1 0 0 0 0 0 0
0 0 0 0 0 0 1 0 0 0 0 0
0 0 0 0 0 0 0 1 0 0 0 0
0 0 0 0 0 0 0 0 1 0 0 0
0 0 0 0 0 0 0 0 0 1 0 0
0 0 0 0 0 0 0 0 0 0 1 0
0 0 0 0 0 0 0 0 0 0 0 1

```

Tool gives result for PTM5 (in code it given as PTMc2) is 32x32 matrix:

PTMc2 =

```

0.0025 0.0475 0.0475 0.9025 0 0 0 0
0.0025 0.0475 0.0475 0.9025 0 0 0 0
0.0025 0.0475 0.0475 0.9025 0 0 0 0
0.0475 0.0025 0.9025 0.0475 0 0 0 0
0.0025 0.0475 0.0475 0.9025 0 0 0 0
0.0025 0.0475 0.0475 0.9025 0 0 0 0
0.0025 0.0475 0.0475 0.9025 0 0 0 0
0.0475 0.0025 0.9025 0.0475 0 0 0 0
0.0025 0.0475 0.0475 0.9025 0 0 0 0
0.0025 0.0475 0.0475 0.9025 0 0 0 0
0.0475 0.0025 0.9025 0.0475 0 0 0 0
0.0475 0.9025 0.0025 0.0475 0 0 0 0
0.0475 0.9025 0.0025 0.0475 0 0 0 0
0.9025 0.0475 0.0475 0.0025 0 0 0 0
0 0 0 0 0.0025 0.0475 0.0475 0.9025
0 0 0 0 0.0025 0.0475 0.0475 0.9025
0 0 0 0 0.0025 0.0475 0.0475 0.9025
0 0 0 0 0.0475 0.0025 0.9025 0.0475
0 0 0 0 0.0025 0.0475 0.0475 0.9025
0 0 0 0 0.0025 0.0475 0.0475 0.9025
0 0 0 0 0.0025 0.0475 0.0475 0.9025
0 0 0 0 0.0475 0.0025 0.9025 0.0475
0 0 0 0 0.0025 0.0475 0.0475 0.9025
0 0 0 0 0.0025 0.0475 0.0475 0.9025
0 0 0 0 0.0475 0.0025 0.9025 0.0475
0 0 0 0 0.0475 0.9025 0.0025 0.0475
0 0 0 0 0.0475 0.9025 0.0025 0.0475
0 0 0 0 0.9025 0.0475 0.0475 0.0025

```

Tool gives result for PTM6 (in code it given as PTMa3) is 32x8 matrix:

PTMa3 =

```

1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

```

Tool gives result for PTM7 (in code it given as PTMc3) is 8x4 matrix:

PTMc3 =

```

0.0025 0.0475 0.0475 0.9025
0.0025 0.0475 0.0475 0.9025
0.0025 0.0475 0.0475 0.9025
0.0475 0.0025 0.9025 0.0475
0.0025 0.0475 0.0475 0.9025

```

0.0025 0.0475 0.0475 0.9025
 0.0025 0.0475 0.0475 0.9025
 0.0475 0.0025 0.9025 0.0475
 0.0025 0.0475 0.0475 0.9025
 0.0025 0.0475 0.0475 0.9025
 0.0025 0.0475 0.0475 0.9025
 0.0475 0.0025 0.9025 0.0475
 0.0475 0.9025 0.0025 0.0475
 0.0475 0.9025 0.0025 0.0475
 0.0475 0.9025 0.0025 0.0475
 0.9025 0.0475 0.0475 0.0025

TABLE 1. PTM of sub-circuits of C17

Sub-circuit	PTM	Matrix dimension
1	PTM1	32x64
2	PTM2	64x64
3	PTM3	64x16
4	PTM4	16x32
5	PTM5	32x32
6	PTM6	32x8
7	PTM7	8x4

Tool gives us result of Overall PTM matrix with dimensions 32x4 for C17 as below:

PTM =

0.7782 0.0841 0.0841 0.0537
 0.1166 0.7456 0.0146 0.1231
 0.7782 0.0841 0.0841 0.0537
 0.1166 0.7456 0.0146 0.1231
 0.7782 0.0841 0.0841 0.0537
 0.1166 0.7456 0.0146 0.1231
 0.7782 0.0841 0.0841 0.0537
 0.7434 0.1189 0.0804 0.0574
 0.0801 0.0512 0.0512 0.8176

0.0452	0.0860	0.0475	0.8213
0.0801	0.0512	0.0512	0.8176
0.0452	0.0860	0.0475	0.8213
0.0801	0.0512	0.0512	0.8176
0.0452	0.0860	0.0475	0.8213
0.7415	0.0823	0.0823	0.0939
0.7396	0.0842	0.0821	0.0941
0.7782	0.0841	0.0841	0.0537
0.1166	0.7456	0.0146	0.1231
0.7782	0.0841	0.0841	0.0537
0.1166	0.7456	0.0146	0.1231
0.0818	0.0109	0.7804	0.1268
0.0124	0.0804	0.1189	0.7884
0.0818	0.0109	0.7804	0.1268
0.0781	0.0146	0.7456	0.1616
0.0801	0.0512	0.0512	0.8176
0.0452	0.0860	0.0475	0.8213
0.0801	0.0512	0.0512	0.8176
0.0452	0.0860	0.0475	0.8213
0.0104	0.0438	0.1208	0.8249
0.0068	0.0475	0.0860	0.8597
0.0780	0.0127	0.7457	0.1635
0.0779	0.0129	0.7439	0.1654

For calculating reliability code detects numbers greater than 0.5 in each row and sum up them as in Eq (28). “y” is the number of rows of PTM matrix. Tool gives us Reliability of C17 benchmark test circuit as in Eq (29).

$$R=0.7782+0.7456+0.7782+0.7456+0.7782+0.7456+0.7782+0.7434+0.8176+0.8213+0.8176+0.8213+0.8176+0.8213+0.7415+0.7396+0.7782+0.7456+0.7782+0.7456+0.7804+0.7884+0.7804+0.7456+0.8176+0.8213=25.0855 \quad (28)$$

$$\text{Reliability} = 25.0855/y = 25.0855/32 = 0.7839 \quad (29)$$

To be sure that tool calculates correct Reliability, Manual Calculation of reliability performed by simple MATLAB code. The following code is for manual calculation of reliability of C17:

```
e=0.05;
F2=[1 0 0 0;0 0 0 1];
I=[1 0;0 1];
S=[1 0 0 0;0 0 1 0;0 1 0 0;0 0 0 1];

AN=[1-e e;1-e e;1-e e;e 1-e];
OR=[1-e e;e 1-e;e 1-e;e 1-e];
XO=[1-e e;e 1-e;e 1-e;1-e e];
NA=[e 1-e;e 1-e;e 1-e;1-e e];
NO=[e 1-e;1-e e];

P1=kron(kron(kron(kron(I,I),F2),I),I)
P2=kron(kron(kron(kron(I,S),I),I),I)
P3=kron(kron(kron(NA,I),NA),I)
P4=kron(kron(kron(I,I),F2),I)
P5=kron(kron(I,NA),NA)
P6=kron(kron(I,F2),I)
P7=kron(NA,NA)

OverallPTM=P1*P2*P3*P4*P5*P6*P7
[y,z]=size(OverallPTM)
Reliability=(sum(OverallPTM(OverallPTM>0.5)))/y)*100

-----

Reliability =

    78.3921
```

In the code, F2 is the matrix of ITM of Fan-out of wire. I is the Identity wire ITM. S is for wire Swapping ITM. AN,OR,XO,NA,NO are logic gates PTMs with 5% logic gate error. P1-P7 represents PTM of each stages.

Result for Manual calculation also same as tool calculated. It proves that tool measured Reliability of C17 circuit correct.

Below is the table of Reliability measurement with same tool applied on several benchmark test circuits with gate error probability of 5% ($e=0.05$)

TABLE 2. Benchmark Test Circuit Reliability Measures

Benchmark Test Circuit	Number of logic gates	Reliability (%)
C17	6	78.39
Full Adder	5	79.98
NAND based Full adder	9	69.15
2-to-4 Decoder	6	75.66

Logic gate error probability we took as 5% for our project, because in current literature this value is accepted for most of the benchmark test circuits.

As we can see from the table above, as number of logic gates increase in Integrated circuits, the reliability decreases. The result gives as analysis that less number of logic gates more reliable circuit.

CHAPTER 5

CONCLUSION AND RECCOMENDATION:

5.1 Conclusion

This project aimed to create a Tool to calculate Reliability of Circuit. Probabilistic Transfer Matrix model was used to calculate Circuit Reliability. In this paper Reliability Tool is developed using MATLAB language programming. This tool has ability to measure reliability of any given circuit. Netlist of Circuit should be provided in the form of Circuit Specification Matrix (CSM), Gate Sequence Matrix (GSM) and Gate Location Matrix (GLM). This tool helps to users to speed-up their calculation, thus it means save of time without any extra hardwork .

As a Conclusion project was able to perform Objective of the work.

5.2 Recommendations

Since the project has successfully completed. Future work should be considered in order to develop the Reliability Tool for larger benchmark test circuits. It would save time, save money.

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