

Development of the RF Energy Harvester Circuit

by

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16718

Dissertation submitted in partial fulfilment of
the requirements for the
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CERTIFICATION OF APPROVAL

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A project dissertation submitted to the
Electrical & Electronics Engineering Programme
Universiti Teknologi PETRONAS
in partial fulfilment of the requirement for the
BACHELOR OF ENGINEERING (Hons)
(ELECTRICAL & ELECTRONICS)

Approved by,

(AP. DR. Zuhairi B. Hj. Baharudin)

UNIVERSITI TEKNOLOGI PETRONAS

TRONOH, PERAK

September 2014

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

REJINAH JESSY A/P SAVARIMUTHU

ABSTRACT

Energy Harvesting is motivated by the urge to address the issue of climate change and global warming also brought to an inspiration to use RF energy harvester circuit as an alternative for battery usage on the fire fighter wearable GPS tracking sensor to avoid the cause of explosion. This project is based on the idea of harvesting the ambient RF energy. The desired RF energy (GSM-900) will be captured by a receiver antenna in which it will be harvested as a DC voltage levels by the well designed RF energy harvester circuit. The receiver antenna is not considered as part of this project due to a critical stipulated time frame provided. The RF energy harvester circuit is formed by the stages integration of ceramic capacitors and Schottky diodes. Many models of the conventional rectifier circuit have been considered however an optimal stages design of RF energy harvester circuit are developed in this project from the analysis done on Dickson's voltage doubler topology. The harvested energy from the output of the RF voltage rectifier circuit will then be used to energize the electronics devices with small electrical specifications. By using GSM-900 frequency band as the source of energy, both uplink and downlink frequencies are taking part in the RF energy harvesting. Nevertheless the most suited printed circuit board are investigated and its criteria is taken into consideration in designing the entire system of harvester circuit to achieve a lower loss output.

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ABBREVIATIONS AND NOMENCLATURES

AC	Alternative Current
ADS	Advance Design System
CW	Cockcroft Walton
DC	Direct Current
EAGLE	Easily Application Graphical Layout Editor
EH	Energy Harvester
FYP	Final Year Project
GSM	Global System For Mobile Communications
I/O	Input And Output
LPF	Low Pass Filter
PCB	Printed Circuit Board
PTFE	Polytetrafluoroethylene
RF	Radio Frequency
RF4	Flame Retardant – 4
SEDEX	Science And Engineering Design Exhibition
SMA	Sub Miniature version A
SMS	Short Message Service
UTP	Universiti Teknologi PETRONAS
VS	Versus
WIFI	Wireless Fidelity

CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

The dispensation of energy harvesting involved extraction and derivation of external input which will then be properly saved in term of electrical energy [1]. The energy harvested is usually nominal around μW to mW , though capability of generating it in a right time can add a meaningful innovative value whenever consumer is in the location that is far away from the national grid. Energy harvesting process will then be very convenient without the necessity of power adapter and batteries which it can happen in a wireless mode [2].

GSM-900 has chosen to be the best source of the energy harvesting due to its rapid growth of GSM subscription around the world. An article was found in Cellular News website, by the year 2007, it has reaches 3 billion cellular phone user worldwide derived from the GSM family which declared by 3G Americas as the trade body. This research statistic shown that the GSM subscriptions are almost triple the figure of users which accessing internet worldwide [3]. Also taking consideration of the coverage area of the GSM technology, Table 1.1.1 shows the statistic obtain from the GSMA website proven that by 2009 all the Asia countries has reaches the surface area coverage for GSM signal and its percentage are speedily increase from year 2007 to 2009 although some country still maintain on certain percentage [4]. This critical bridging between an express expansion of GSM subscriber and the coverage area by GSM technology as well as the close association to RF energy harvester which uses the GSM-900 band frequencies as the source of

energy has evidently proven the marketable opportunity for RF Energy Harvester circuit.

Nevertheless energy harvesting can convey towards improvement in technology development with no doubt that noteworthy contribution will occur towards environment by energy saving [1].

Table 1.1.1 2007 - 2009 Statistic of GSM Coverage Area in Asia Region (%)

Country	Region	2007	2008	2009
Afghanistan	Asia			25
Armenia	Asia	84		84
Azerbaijan	Asia	37		49
Bangladesh	Asia	75		75
Bhutan	Asia	6		6
Cambodia	Asia	21		43
China	Asia	25		25
Georgia	Asia	81		81
India	Asia	39		56
Indonesia	Asia	8		8
Iran	Asia	17		17
Iraq	Asia	21		26
Jordan	Asia	74		74
Kazakhstan	Asia	7		7
Kyrgyzstan	Asia	6		6
Lebanon	Asia	100		100
Malaysia	Asia	45		47
Maldives	Asia	84		84
Mongolia	Asia	2		3
Myanmar	Asia	2		2
Nepal	Asia			8
Pakistan	Asia	7		7
Philippines	Asia	84		84
Sri Lanka	Asia	49		82
Syria	Asia	59		77
Tajikistan	Asia	1		1
Thailand	Asia	33	64	64
Turkmenistan	Asia	1		1

1.2 PROBLEM STATEMENT

Due to a fairly high consumption of power supply on electronic devices, a recharging process is required. However, recharging process will not be convenient if outdoor activities are involved. Thus, RF energy harvester is developed to solve the problem by providing continuous power supply with the existence of the high attainability GSM signal

1.3 OBJECTIVES

- i. To investigate the fundamental of the RF signals and the suitable signal range in energy harvesting.
- ii. To inspect the characteristic of the printed circuit board (PCB) towards the output quality of RF energy harvester circuit.
- iii. To design, develop and fabricate the RF energy harvester circuit.

1.4 SCOPE OF STUDY

The laboratory investigation on the suitability of GSM-900 signal range in energy harvesting hence to design, develop and fabricate the RF energy harvester circuit by basing on the lower loss PCB material.

1.5 HYPOTHESIS

- i. Higher stage of any voltage multiplier topology circuit produces higher output voltage which is correct only before the saturation mode is reached.
- ii. The higher the dielectric constant of PCB the higher the output loss.
- iii. Surface mount component able to reduce loss compare to leaded component.

1.6 RELEVANCY AND FEASIBILITY

Development of the RF energy harvester circuits is an innovative engineering based project which very much related to the concept of authentic learning. Relevancy and

feasibility study on the project scope and time frame is conducted. Project scope is concentrated on the part of developing RF energy harvester circuit specifically for battery charging purpose of electronics devices with small electrical specifications rating. Application of engineering knowledge and skills are needed in this project to provide practical solution on the problem statement set which leads to demonstrating the problem solving skill and the joint effort of critical thinking whenever problems and issues take place while achieving the objective. The feasibility study has shown the possibility of success of the topic chosen by listing the milestone and fixing the timeframe as well addressing and mitigating the factors untimely for which can affect the project. Moreover, project management skills are put in practice in order to achieve a quality outcome as well to make sure that the targeted scope of the development of RF energy harvester circuit can be completed within stipulated time frame.

CHAPTER 2

LITERATURE REVIEW AND THEORY

2.1 GSM IN ENERGY HARVESTING

GSM is the short form of *Global System for Mobile Communications* which is the most viral broadcasted cellular communication in the whole world. GSM not only involve in the voice call system but too providing user with the no voice communication that known as SMS [5]. As shown in Figure 2.1.1 adapted from a research article, it illustrates that 900 MHz is the frequency which reaches the peak point from the range of 0 to 3 GHz that was investigated. The demand of 900 MHz frequency has explained the potential utilization of GSM signal not only for communication purposes but also for energy harvesting [6].

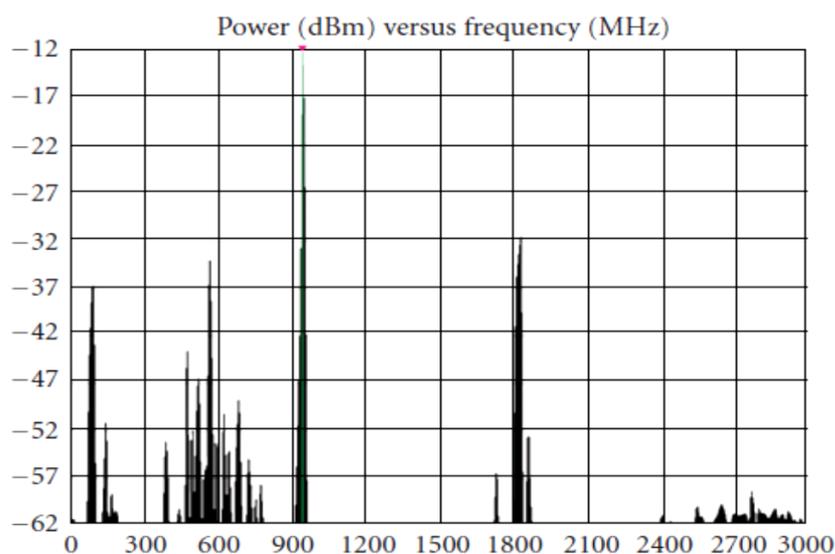


Figure 2.1.1 Ambient RF Signal in Urban Area

2.2 RF –DC RECTIFIER CIRCUIT

To convert from RF to DC level, a RF voltage rectifier circuit is used. In other words, the RF voltage rectifier is actually the energy harvesting circuit by converting the GSM downlink or uplink signals to a small value of direct current voltage. A single rectifier is sufficient to produce the output. However, to produce a desired output, repetitions of rectifier circuit stages need to be implemented. Repetition of the rectifier will provide a higher normalized output in which energy harvested will eventually be higher. According to literature [7], to obtain a close to pure DC voltage output, a multiplier of the rectifier is essential to lessen the ripple yet the noise of the voltage and current will also be multiplied.

Theoretically, the multiplier circuit that contains n stages of the rectifier will produce $2nV_{in}$ of voltage output as described by the following formula [8].

$$V_o = nV_{in} - \frac{n-1}{f_c} * I_{load} \quad (1)$$

Referring back to report [7], all the stages capacitor used in CW or Villard's circuit is of equal capacitance however a contradicting statement was made in literature [8]. In accordance with the literature declared in [8], the model which uses equal capacitance in stages of the rectifier will lead to a non-optimal effect of design hence, by using the Cockcroft-Walton voltage multiplier model, evaluations are done on the variable of capacitance to prove the declared phenomenon and hence to mitigate the DC output voltage drop [9].

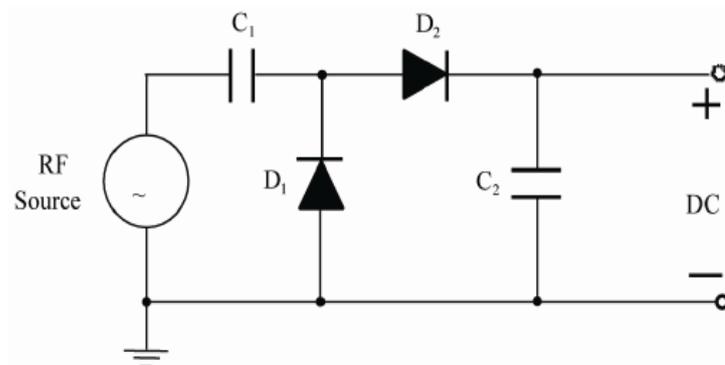


Figure 2.2.1 Single Stage Dickson's Model

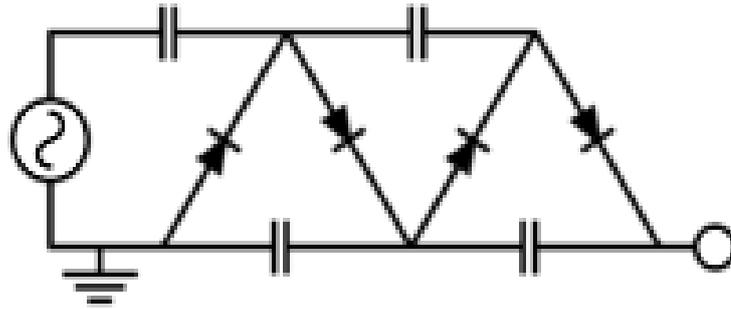


Figure 2.2.2 Two Stage CW's Model

Meanwhile, the energy conversion by the Dickson's model is able to double up the input signal voltage headed to the ground by a singular output as shown in Figure 2.2.1. Thus, Dickson's model is more achievable compare to the Cockcroft Walton's model in terms of the voltage output as shown in Figure 2.2.2 [10].

RF-DC rectifier stages also playing a crucial role in producing a higher voltage output. Author in reference [11] presented that the 7 stages Cockcroft Walton voltage multiplier model is the stage where it can produce a maximum output voltage and any stage's voltage above this stage will not further increased due to the reaching of saturation mode. Though, a more increased voltage output can be achieved if the model is integrated with the Bassel LPF.

2.3 CRITICAL ANALYSIS

Table 2.3.1 Critical Analysis on Energy Harvester

	RF Energy Harvester	Electrodynamics Energy Harvester	Piezoelectric Energy Harvester
Source	Ambient Radio Frequency [13].	Human energy. (e.g.: hand crank torchlight) [14].	Human Force (e.g.: Piezoelectric shoes) [17].
Process	Capturing frequency of interest using any type of receiver. RF voltage regulator is used to convert RF to DC level [8].	Electrodynamics generation is caused by movement of a magnet across a coil, the field being induced [15].	A piezoelectric disk generates a voltage when deformed by external force [16, 18].
Size of the end product	Small due to very few components needed [7].	Slightly bigger due to the size of the generator/ dynamo [15].	Thin layer but wider surface. (depend on type) [17].
Cost	Slightly Higher than Electrodynamics energy harvester [7].	Low (< RM50 for the complete system) [15].	High (> RM80 for only the piezoelectric) [18].
Output	Small magnitude, but sufficient for low power rating wearable electronics [8].	Magnitude of the induction is limited in small devices [14].	Slightly higher magnitude compares to RF energy harvester. [18].
Portability	High degree of portability [13].	Up to a certain freedom of portability due to the generator size [16].	Fairly portable [17].
Durability	Low fragility, hence higher durability [13].	Better durability compares to piezoelectric [16].	Above the optimal resonance, they can break relatively easily [18].
Dependency	Independent.	Dependent on human energy	Dependent on human energy

Table 2.3.2 Critical Analysis on RF Energy Harvester

	GSM -900 RF Energy Harvester¹	WIFI - 2.4GHz RF Energy Harvester
Voltage produced (V)	2.9V at ~50m away from the cell tower.	1.5V at 2.4m from the router.
Current produced (I)	~0.8 μ A at ~50m away from the cell tower.	1.16 μ A at 2.4m from the router. (calculated from given voltage and power)
Power produced (P)	~2.32 μ W ~50m away from the cell tower. (calculated from given voltage and current)	1.74 μ W at 2.4m from the router.
Efficiency (η%)	<i>*Data not provided</i>	9.76% of total efficiency at 2.4m from the router.
Reference	[7]	[12]

¹ Data in Table 2.4.2 for GSM -900 RF Energy Harvester with symbol “~” indicates the value is an approximation which it is taken exactly from the reference cited.

Table 2.3.3 Critical Analysis on Printed Circuit Board

	Flame Retardant – 4 (FR-4)	RT/Duroid® 5880 (RO5880)
Dielectric Constant, ϵ_r	4.2	2.2 ± 0.02 spec
Copper Thickness, t	0.1mm	17µm ± 0.5µm
Substrate Thickness, h	1.4mm	0.787mm ± 0.003mm
Material	Woven fibreglass cloth with an epoxy resin binder.	Woven glass reinforced PTFE laminates
Source of Reference	Data Sheet	Data Sheet

CHAPTER 3

METHODOLOGY

3.1 RESEARCH METHOD OVERVIEW

The method used in this project is simulate and analytical technique. In this project, simulate technique is used to performed simulation by using certain software for modelling and to forecast the voltage output of the RF energy harvester circuit in a virtual manner, whereas analytical technique is used due to the involvement of laboratory testing on the RF energy harvester circuit. Details regarding each project research measure are elaborated at the following sections in this chapter. Contingent upon the criteria of analysis and evaluation on the subject matter, the following research techniques are used to gather a quality outcome.

Simulate technique:

- i. Modelling
 - Modelling of the RF energy harvester circuit based on Dickson's topology.
- ii. Simulation
 - Simulation on the Dickson's model cascading stage, to select the optimal stage based on the highest output voltage simulated.

Analytical technique:

- i. Laboratory experiment
 - Testing is performed in order for data collection for further analysis.
- ii. Calculation

- Width of PCB microstrip track is calculated to fit with the input impedance matching of the RF energy.
- iii. Tabulation
- Tabulation is done on the results obtained through simulation and laboratory testing from various design of circuit. Hence a good design can be choose based on the different parameter tested on the simulation for a desired output.
 - Tabulation also made easy on the critical analysis section as part of the research on justifying the characteristic of certain analysis.

3.2 PROJECT ACTIVITIES

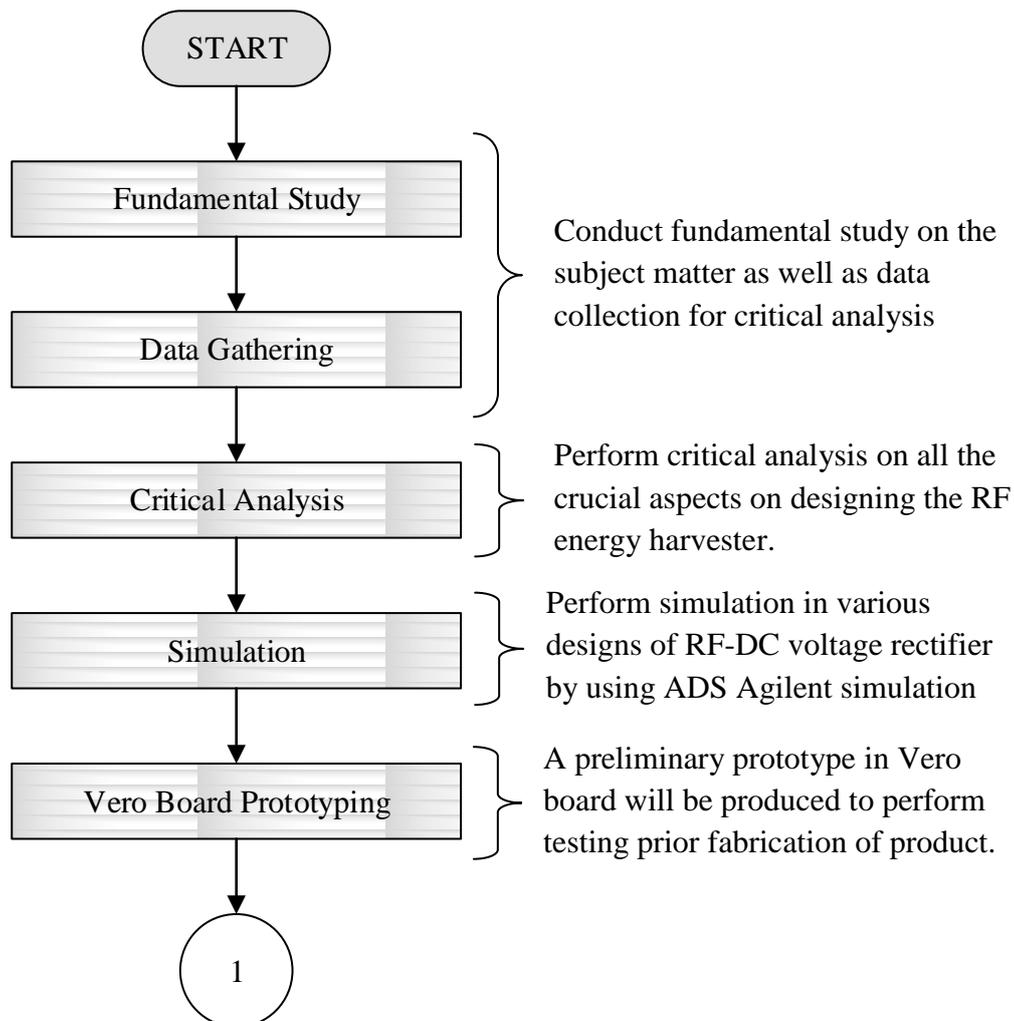


Figure 3.2.1 Project Flow Chart 1 of

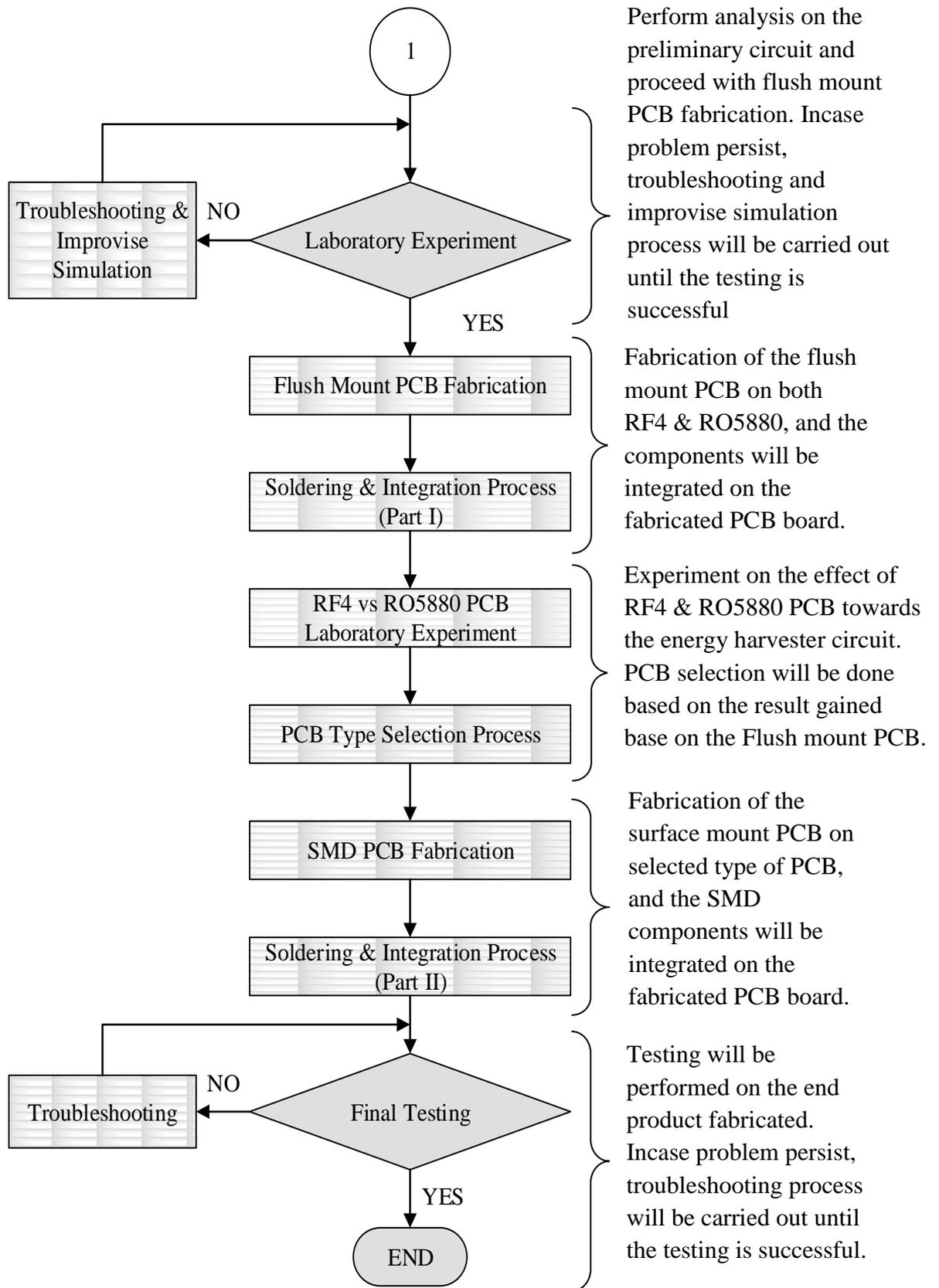


Figure 3.2.2 Project Flow Chart 2 of 2

3.3 TOOLS & SOFTWARE REQUIRED

3.3.1 Software

- i. Agilent ADS Software:



Figure 3.3.1.1 Advanced Design System by Agilent

Advance Design System is electronic design automation software. Prior confirm the design of the RF voltage regulator circuit; all possible parameter will be analyzed to produce an optimized circuit.

- ii. EAGLE PCB Software:



Figure 3.3.1.2 EAGLE by Cadsoft

Easily Application Graphical Layout Editor is a software program that will be used in the project in designing the circuit PCB layout.

This software provides back annotation to schematic and connects traces based on the desired connection defined by the user.

3.3.2 Hardware/ Equipment

i. PCB Fabrication Machine:



Figure 3.3.2.1 PCB Fabrication Machine

This machine is to convert a soft bound of a PCB layout obtained from the EAGLE PCB software into a hard bound PCB board.

ii. ESG Series Signal Generator:

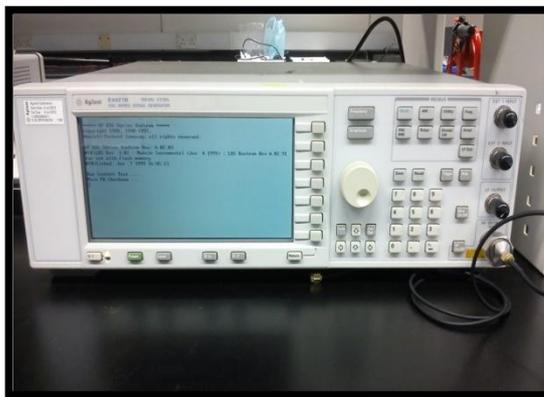


Figure 3.3.2.2 Agilent ESG Series Signal Generator

This equipment is able to generate the desired RF signal. Hence it will be connected to the circuit through coaxial cable via SMA connector

for testing and measurement purpose. For a free space transmission, a transmitter antenna can be connected to this equipment.

iii. Mixed Domain Oscilloscope:



Figure 3.3.2.3 Tektronix Mixed Domain Oscilloscope

This equipment is able to take the measurement and display of the DC output with imposed AC signal. Hence it is suitable for measuring the voltage and power output of the RF energy harvester

iv. Network Analyzer



Figure 3.3.2.4 ANRITSU VMA Master

This equipment is used to measure the receiver and transmitter antenna network parameter. This measurement can ensure the electrical network is in the desired range.

v. SMD Soldering Equipment:



Figure 3.3.2.5 SMD Soldering Equipment

Soldering iron will be used as a hand tool to integrate the electronic components with the PCB board so that a complete circuitry system will be produced.

vi. Measurement Tape



Figure 3.3.2.6 Measurement Tape

Measurement tape is used during the measurement which involved unguided transmission medium. This is to ensure the distance between the transmitter and receiver is properly defined.

vii. Wire Cutter:



Figure 3.3.2.7 Wire Cutter

Wire cutter will be used to clean the fringing of component's conductors after the soldering process.

3.3.3 Components & Materials

Components and materials used are for testing and measurement as well as for prototyping purposes.

Table 3.3.3.1 List of Components & Materials

No.	Component / Material	Brand	Type	Description	Unit
1.	FR4-86 UV Block (PCB)	Nan Ya	-	6cm x 4.5cm	1
2.	RO5880 (PCB)	Rogers	-	12.5cm x 10cm	1
3.	Connector	Johnson	SMA	50Ω	5
4.	Microcoaxial Connector Recept Vertical	Molex	SMD	50Ω	1
5.	Small Signal Schottky Diode	ST Micoelectronics	Leaded	1N5711	12
6.	Ceramic Capacitor	Multicomp	Leaded	1μF	12
7.	Microwave Schottky Detector Diodes	Avago Technologies	SMD	HSMS-286C	12
8.	Multilayer Ceramic Chip Capacitors (MLCCs)	KEMET	SMD	1μf, 25V	24
9.	Helical Antenna GSM	RF solution	SMA	90 ⁰ , 2dBi, 50Ω	2
10.	Cellular Standalone Antenna	Molex	SMD	6-Band, 50Ω	1

3.4 DESCRIPTION OF METHODOLOGY

3.4.1 Circuit Design Procedure

Simulations are initially done on Cockcroft Walton voltage multiplier model on analysing the most suitable stages that are able to produce the maximum output. At the beginning 10 stages of the mentioned model were simulated and later on each stage is reduced at a time to analyse the output variation. The similar approach is taken for the Dickson voltage doubler circuit model.

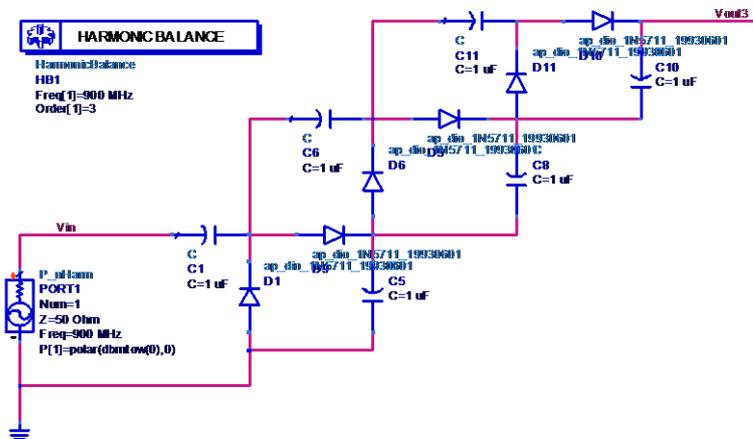


Figure 3.4.1.1 CW / Villard Voltage Multiplier

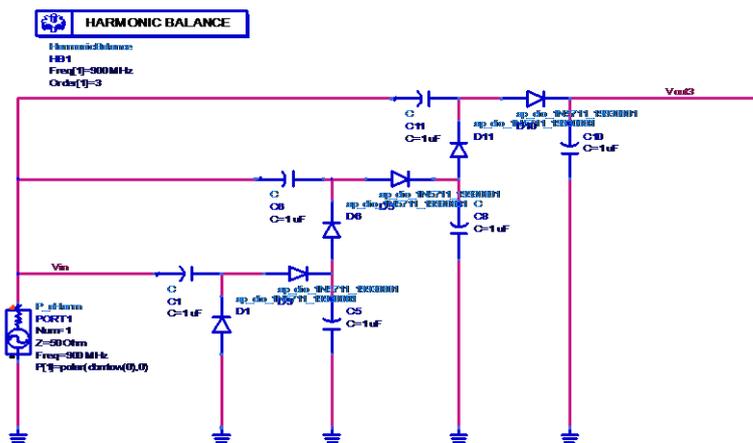


Figure 3.4.1.2 Dickson Voltage Doubler Circuit

3.4.2 PCB Transmission Line Design Procedure

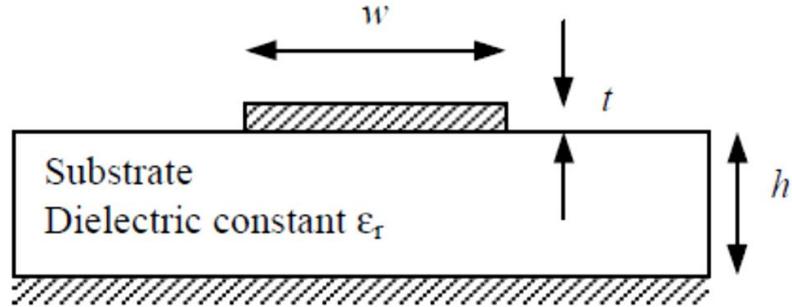


Figure 3.4.2.1 Cross Sectional Area of PCB

The transmission microstrip line on the PCB is properly designed with a precise calculation done. This is to ensure that the 50Ω impedance from the source to the first functional component of the circuit is matched. Rearranging the equation (2) from reference [20], a newly ordered equation (3) is formed as following for the computation of the width of the microstrip transmission line. All the parameters required in computing the transmission line width are justified in Figure 3.4.2.1. The reason for impedance matching only concentrated from the SMA connected to the first component is due to its nature of the signal is no longer at RF after the first component. Even though the signal after the first component is imposed with it is imposed with a higher ripple it is still considered as a rippled DC voltage with an offset from zero.

$$Z_0 = \left[\frac{87.0}{(\epsilon_r + 1.41)^{\frac{1}{2}}} \right] \times \ln \left[\frac{5.98h}{0.8w + t} \right] \quad (2)$$

$$w = \left[\frac{5.98h}{e^{\frac{Z_0(\epsilon_r + 1.41)^{\frac{1}{2}}}{87.0}}} - t \right] \times \frac{1}{0.8} \quad (3)$$

3.4.3 Measurement Procedure by Guided Transmission Medium

This measurement is performed by connecting the ESG Series Signal Generator to the SMA input of RF Energy Harvester using the method of direct connection via coaxial cable (guided transmission medium).

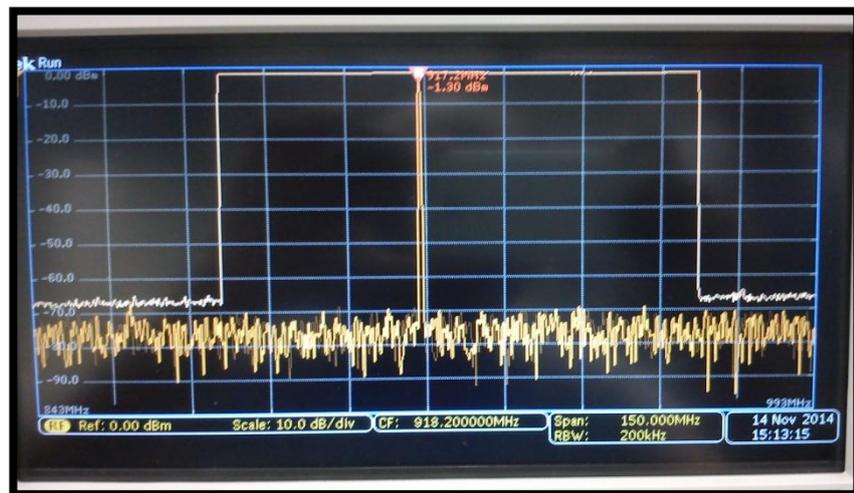


Figure 3.4.3.1 Cable Insertion Loss Screen Snap Shoot

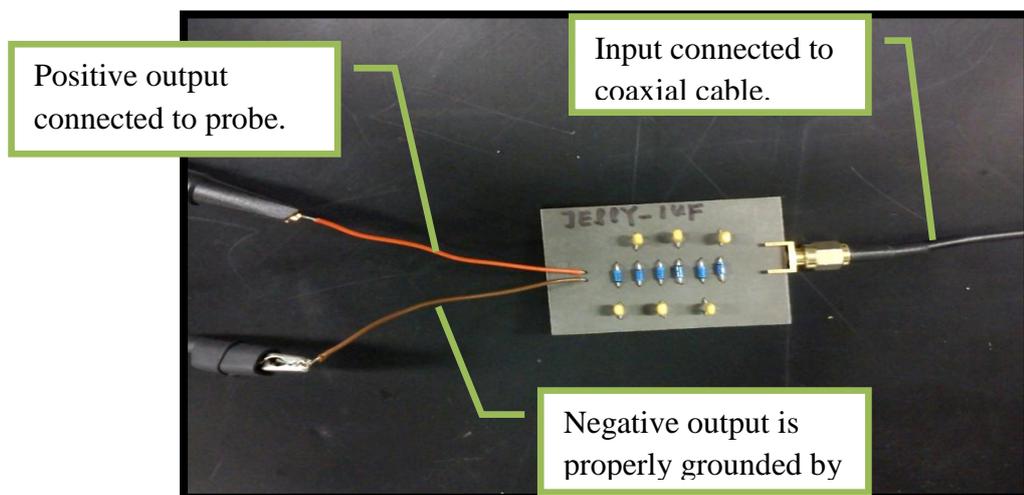


Figure 3.4.3.2 I/O Connection of RF Energy Harvester Circuit

- i. The ESG series signal generator and mixed domain oscilloscope are powered on.
- ii. Then the coaxial cable from the ESG series signal generator is connected to the mixed domain oscilloscope to determine the cable

insertion loss as shown in Figure 3.4.3.1. The cable insertion loss is recorded.

- iii. After that, the ESG series signal generator's coaxial cable is disconnected from and mixed domain oscilloscope and initial frequency value of the ESG series signal generator is set to 890 MHz whereas the initial power amplitude is set to 0dBm.
- iv. The coaxial cable of the ESG series signal generator is then connected to the RF energy harvester circuit via SMA connector.
- v. Output terminal of the circuit is connected to the mixed domain oscilloscope via probe and the circuit is properly grounded as shown in Figure 3.4.3.2.
- vi. Before taking the measurement, the ESG series signal generator button is pushed to make sure the desired signal will be generated.
- vii. Outputs from the oscilloscope are recorded by increasing the RF frequency from the initial value to 960 MHz with 10 MHz increment. The same process of this step is repeated with 1dBm increment every each time the RF signal are increased to the maximum value fixed.

3.4.4 Measurement Procedure by Unguided Transmission Medium

Free space (unguided transmission medium) is used instead of coaxial cable for the purpose of measurement by using antenna.



Figure 3.4.4.1 Receiver Antenna Return Loss (S11)

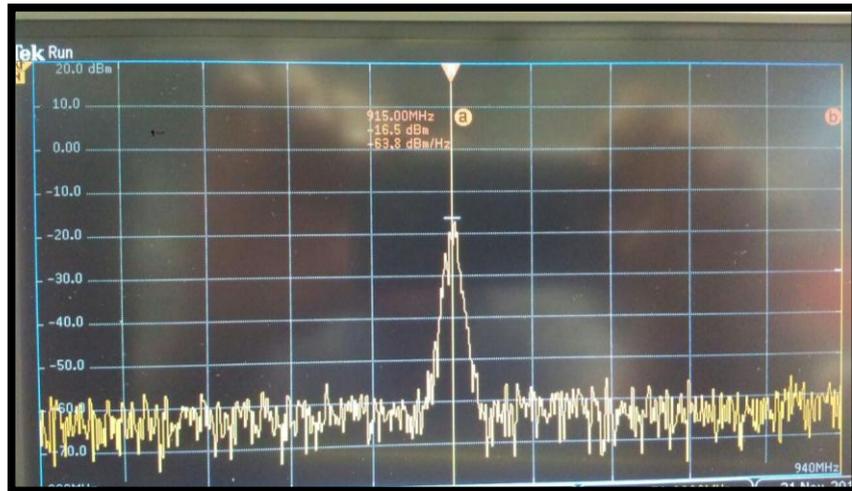


Figure 3.4.4.2 Transmitter Antenna Return Loss (S11)

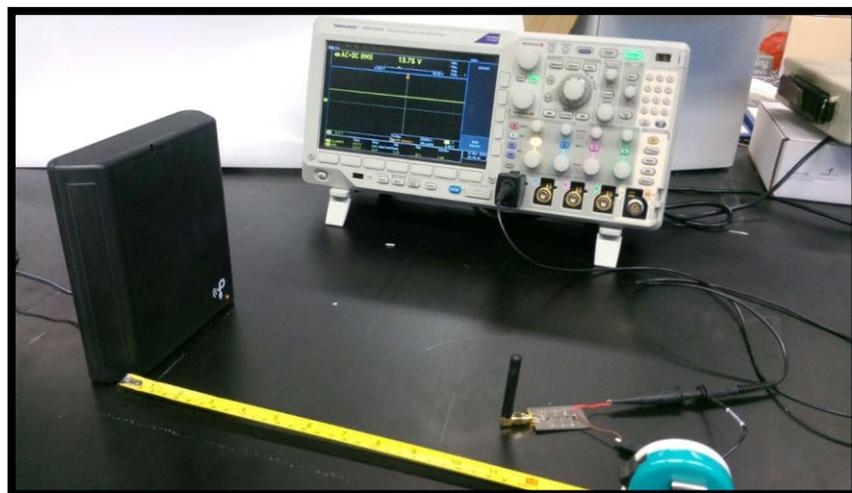


Figure 3.4.4.3 Measurement by Unguided Transmission Medium

- i. Prior starting the measurement, the transmitter and receiver antenna are examined by using the network analyzer. This is to check and confirm both of the antennas are operated under GSM frequency range.
- ii. After confirmation is made, the return losses of transmitter and receiver antenna are measured using similar equipment. The results are screen shoot and displayed at Figure 3.4.4.1 and Figure 3.4.4.2.
- iii. Then, the measurement is preceded by turned on the transmitter antenna whereas the receiver antenna is connected to the RF Energy Harvester circuit as shown in Figure 3.4.4.3.

- iv. The output of RF Energy Harvester circuit is connected to the mixed domain oscilloscope for output voltage and power amplitude display. At this point another receiver antenna is connected to the second oscilloscope to capture the power amplitude received by the energy harvester receiver.
- v. Next, the complete RF Energy Harvester circuit and the second oscilloscope is placed 0cm away from the transmission antenna to measure the output voltage and its power amplitude. This step is repeated from 0cm to 500cm of distance variation towards the output voltage with 50cm increment.
- vi. All the data are recorded.

3.5 PROJECT GANTT CHART

The following Gantt chart disclosed the processes duration needed for each project activity to be completed for both FYP I and FYP II.

Table 3.5.1 Gantt Chart of FYP I & FYP II

No.	Project Detail	Week															Session
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
1	FYP Title Selection	█															FYP 1 May 2014
2	Fundamental Study			█	█												
3	Critical Analysis				█	█	█										
4	Extended Proposal		█	█	█	█	█										
5	Simulation (Phase I)							█	█								
6	Proposal Defence								█	█							
7	Simulation (Phase II)										█						
8	Vero Board Prototyping											█	█	█			
9	Interim Report											█	█	█	█		
10	Vero Board Circuit Lab Experiment	█	█	█												FYP 2 September 2014	
11	Improvised Simulation			█	█												
12	PCB Design & Fabrication				█	█	█										
13	Soldering & Integration Process						█										
14	Lab Experiment on FR-4 & RT/Duroid 5880 PCB							█	█	█							
15	Progress Report	█	█	█	█	█	█	█									
16	Energy Harvester Circuit Lab Experiment								█	█	█						
17	Pre- SEDEX Exhibition											█					
18	Technical Paper					█	█	█	█	█	█	█	█				
19	Project Viva													█			
20	Dissertation									█	█	█	█	█	█		

3.6 PROJECT ACTIVITIES AND KEY MILESTONE

The following milestone chart summarized the Final Year Project I & II activities involved with milestone dates for instant viewing.

Table 3.6.1 Key Milestone of FYP I & FYP II

Milestone Code	Project Detail	Milestone Date
A1	Completion of FYP Title Selection	30 th May 2014
A2	Completion of Fundamental Study	13 th June 2014
A3	Completion of Critical Analysis	27 th June 2014
A4	Submission of Extended Proposal	27 th June 2014
A5	Completion of Simulation (Phase I)	11 th July 2014
A6	Completion of Proposal Defence	16 th July 2014
A7	Completion of Simulation (Phase II)	25 th July 2014
A8	Completion of Vero Board Prototyping	8 th August 2014
A9	Submission of Interim Report	15 th August 2014
B1	Completion of Vero Board Circuit Lab Experiment	10 th October 2014
B1	Completion of Improvised Simulation	18 th October 2014
B2	Completion of PCB Design & Fabrication	28 th October 2014
B3	Completion of Soldering & Integration Process	31 st October 2014
B4	Submission of Progress Report	12 th November 2014
B5	Completion of Lab Experiment on FR-4 & RT/Duroid 5880 PCB	14 th November 2014
B6	Completion of Energy Harvester Circuit Lab Experiment	28 th November 2014
B7	Completion of Pre- SEDEX Exhibition	3 rd December 2014
B8	Submission of Technical Paper	22 nd December 2014
B9	Submission of Dissertation (Soft bound)	22 nd December 2014
B10	Completion of Project Viva	2 nd December 2014
B11	Submission of Dissertation (Hardbound)	26 th January 2015

CHAPTER 4

RESULT AND DISCUSSION

4.1 RESULT AND DISCUSSION

4.1.1 Stages Design Analysis

Stages analysis is performed in simulation and the result is recorded with 0dBm for both Cockcroft Walton's Voltage Multiplier and Dickson's Voltage Doubler topologies.

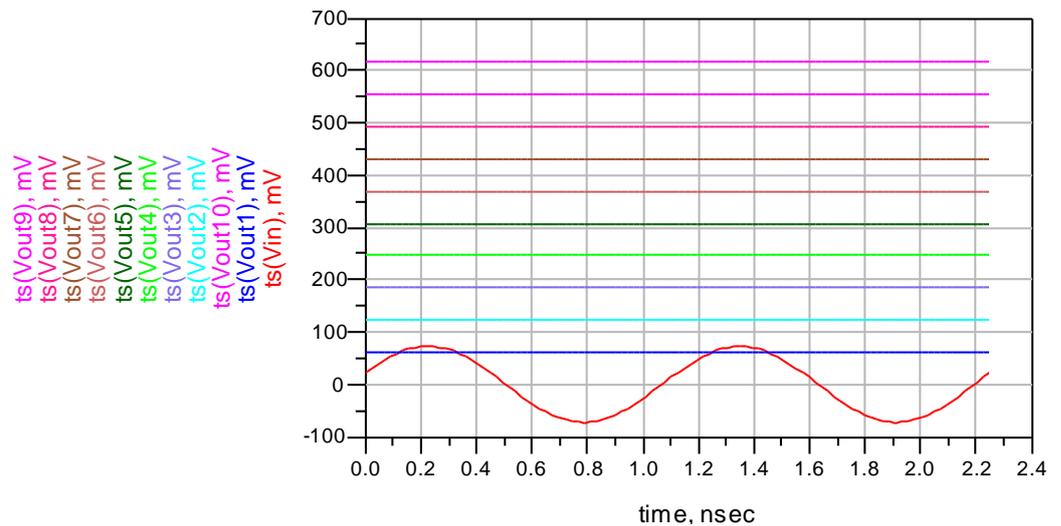


Figure 4.1.1.1 10 stage voltage output analysis on Cockcroft Walton's Voltage Multiplier (Simulation)

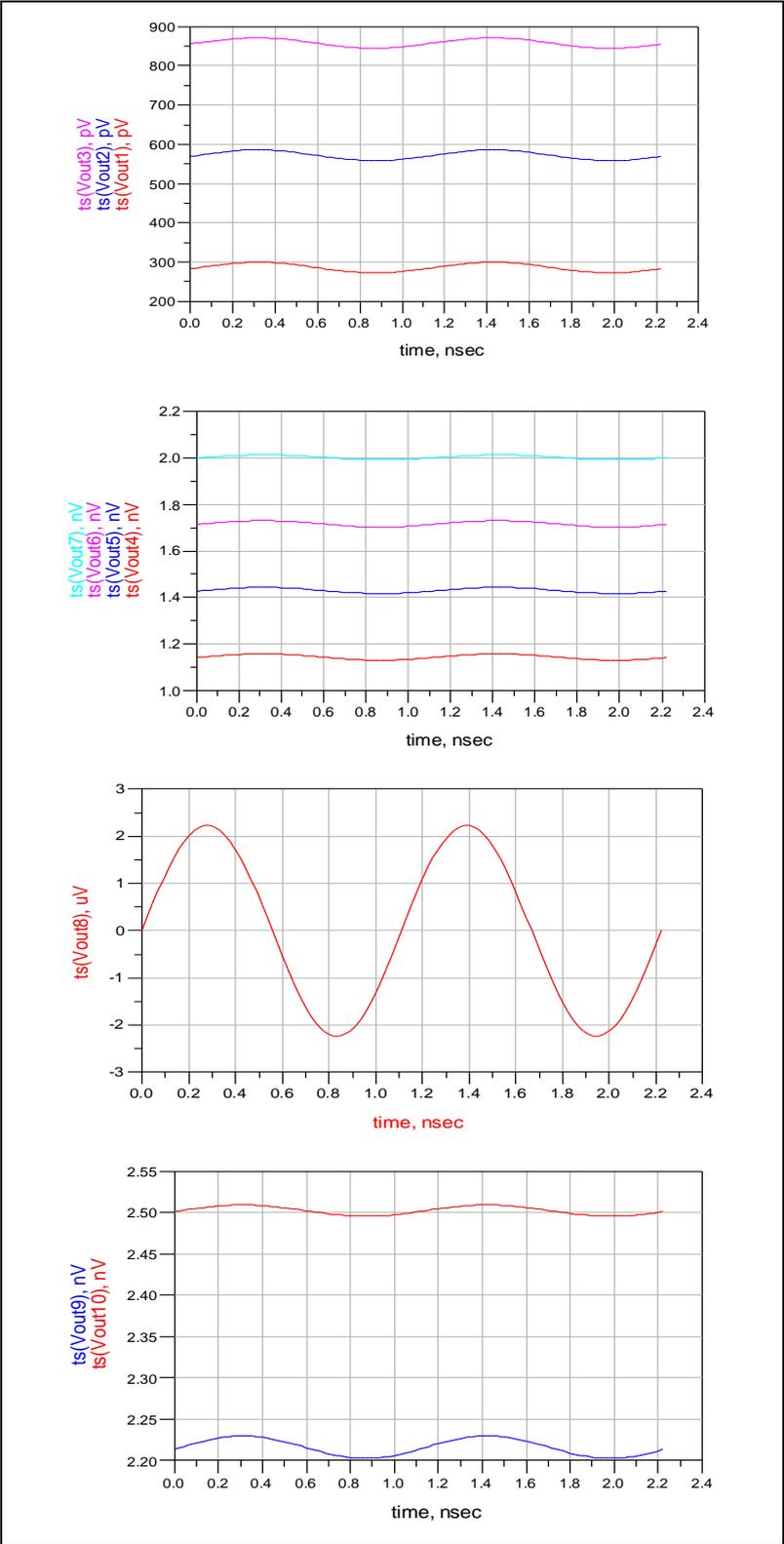


Figure 4.1.1.2 10 stage voltage output analysis on and Dickson's Voltage Doubler (Simulation)

Table 4.1.1.1 Independent Stage Analysis Result

No	Power (dBm)	Stage No.	Output Voltage (V)	
			Cockcroft Walton's / Villard's Voltage Multiplier	Dickson's Voltage Doubler
			Simulation	Simulation
1	0	1	0.356m	0.377m
2	0	2	0.911m	0.927m
3	0	3	0.935m	0.947m
4	0	4	0.895m	0.909m
5	0	5	0.843m	0.867m
6	0	6	0.756m	0.799m
7	0	7	0.522m	0.638m
8	0	8	2.236 μ	0.295m
9	0	9	1.694n	5.678 μ
10	0	10	1.987n	2.76 μ

Referring to Figure 4.1.1.1 and Figure 4.1.1.2, it shows the voltage output obtained from simulation done on the no load Cockcroft Walton's voltage multiplier and Dickson's voltage doubler circuit for 10 stages. The analysis is done with power amplitude of 0dBm which equivalent to 1mW and each of the stage output voltage is displayed. A common assumption that always made by the researchers based on the mentioned figure is the higher the stage of the rectifier hence the higher the voltage output regardless of its model design. From Cockcroft Walton's model the maximum output voltage is at the 10th stage though Dickson's model is able to achieve a maximum output at stage 8 and further increased stages voltage output will start to reduce drastically. However this assumption is proven unreliable when the author discover that stage analysis should be done independently for each stage instead of analysing the output voltage together as shown in mentioned figures. To verify this statement, Table 4.1.1.1 are referred, the tabulated data shows the results obtained from simulation done on the no load Cockcroft Walton's voltage multiplier and Dickson's voltage doubler circuit

for 10 different stages independently. Only focusing on the maximum output produced for each stage of both different models, an interpretation can be done that voltage output is increased up to maximum at stage 3 as highlighted in red, for stages above stage 3 that simulated individually are decreased gradually.

4.1.2 Topology Analysis

In this section both graph and tabulated data from simulation and experimental result are presented. Outstanding topologies will be selected from these results based on 3 stage model. The tabulated data is based on 900MHz RF input source.

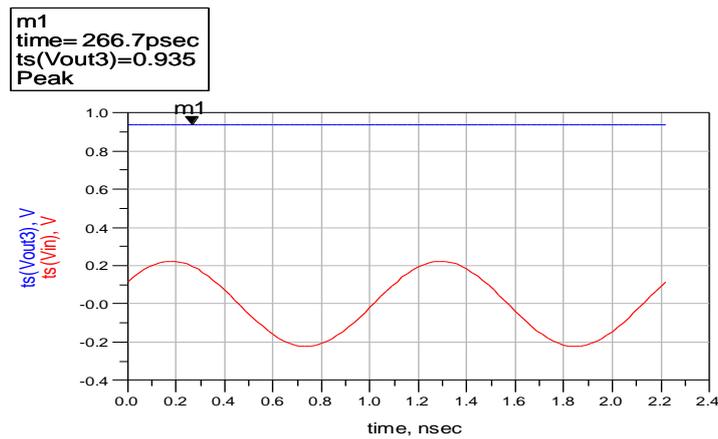


Figure 4.1.2.1 I/O Voltage of CW's Model

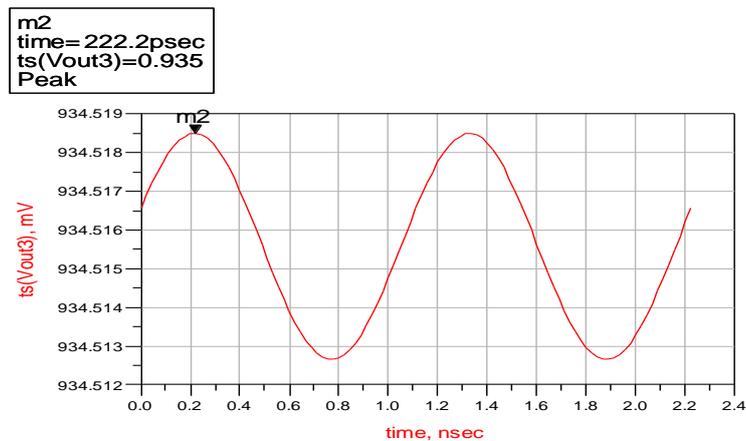


Figure 4.1.2.2 Zoomed Voltage of CW's Model

m2
time= 1.258nsec
ts(Vout)=0.947
Peak

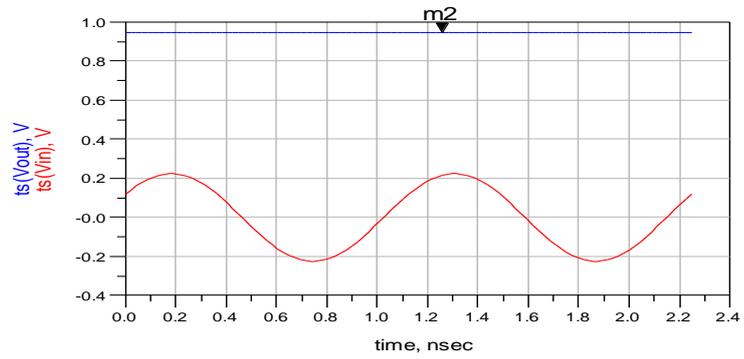


Figure 4.1.2.3 I/O Voltage of Dickson's Model

m1
time= 224.7psec
ts(Vout)=0.947
Max

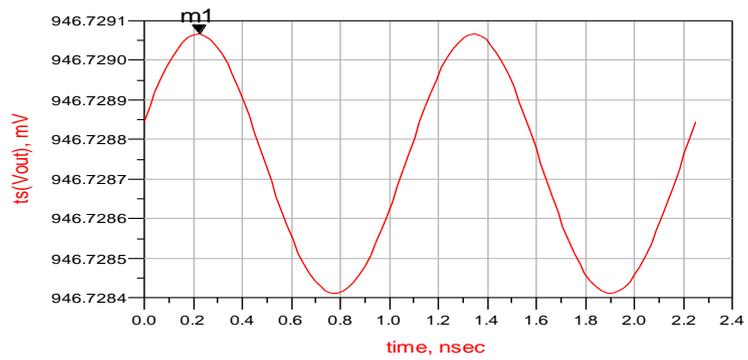


Figure 4.1.2.4 Zoomed Output of Dickson's Model

Table 4.1.2.1 3 Stage Experimental & Simulation Result

No	Power (dBm)	Output Voltage (mV)			
		Cockcroft Walton's Voltage Multiplier		Dickson's Voltage Doubler	
		Measurement	Simulation	Measurement	Simulation
1	0	490.10	935	553.30	947
2	-1	388.10	803	500.00	815
3	-2	306.00	685	470.39	697
4	-3	233.10	583	427.90	595
5	-4	175.30	494	385.65	506
6	-5	134.30	417	300.80	429
7	-6	103.90	350	288.73	362
8	-7	78.23	292	240.16	304
9	-8	58.27	243	110.76	255
10	-9	45.60	201	98.60	213
11	-10	32.93	165	90.01	177
12	-11	22.80	135	70.65	147
13	-12	15.20	110	44.98	112
14	-13	12.67	90	28.73	97
15	-14	7.60	73	16.16	87
16	-15	4.96	59	7.76	67
17	-16	-2.533	47	5.60	50
18	-17	-2.533	38	1.01	48
19	-18	-3.115	30	-2.65	40

During the simulation for topology analysis, the circuit is evaluated using a harmonic balance by providing 900 MHz of RF with 3rd order harmonics waveform into the input. By propagating it throughout the entire circuit, this RF energy that mimicking the form of AC wave are rectified into DC form. In this analysis, total of 3 RF rectifier stages is developed to rectify the RF

energy for both CW's and Dickson's model. In accordance with Figure 4.1.2.1 and Figure 4.1.2.3, it is marked that the output produce for the Cockcroft Walton's model is 935mV whereas Dickson's model produces 947mV for initial power amplitude which are set. Hence Dickson's topology is indeed reliable compare to CW's topology. However when focus are concentrating on the DC output as provided in Figure 4.1.2.2 and Figure 4.1.2.3, the author notice that the output actually wasn't a pure DC voltage instead it is an AC ripples which imitate the DC form. This phenomenon can be interpreted more properly as a close to DC waveform voltage with an offset value from zero.

4.1.3 Dielectric Loss Analysis

In this study of RF energy harvester, the PCB dielectric loss analysis is done to ensure the right type of PCB is chosen for RF Energy Harvester circuit development. The criterion which set as a judgment standard is the dielectric constant (ϵ_r) also known as relative permittivity. This analysis is completed by using two different type and dielectric constant of PCB in the same 3 stage topology model with leaded component which the power amplitude are set to 0dBm. The red variation in Fig 6 indicates RO5880 ($\epsilon_r= 2.2$) as the type of PCB whereas the blue indicates the FR4 ($\epsilon_r= 4.2$). RO5880 is able to produce a higher output voltage variation compares to FR4. This phenomenon has pointed out the importance of selecting the low dielectric constant (ϵ_r) of PCB to mitigate output loss. Output loss is usually occurs due to the absorption of energy especially radio frequency into the substrate. This aspect is considered as one of the improvement done in RF energy harvester.

Meanwhile, dielectric loss can too happen from the effect of components used in the circuit. As per Figure 4.1.3.2, circuit with leaded ceramic capacitor and diode are tested on RO5880 however the result in terms of the output voltage is just too ordinary but a drastic improvement are observe for circuit that uses SMD component of multilayer ceramic chip capacitors (MLCCs) and microwave schottky detector diodes. The reduction of the dielectric structure

in the SMD component reduces the resistance value as well for the inductance and hence able to increase the output voltage by mitigating the dielectric loss.

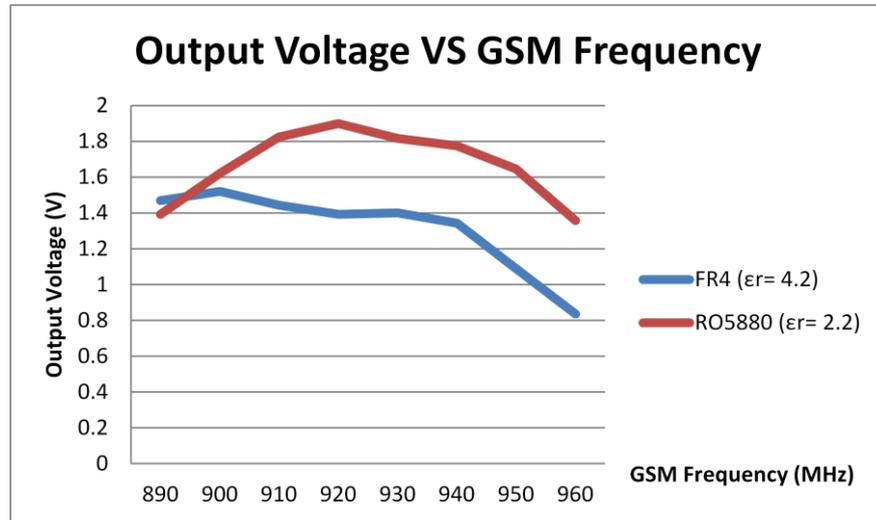


Figure 4.1.3.1 PCB dielectric Loss Analysis Result

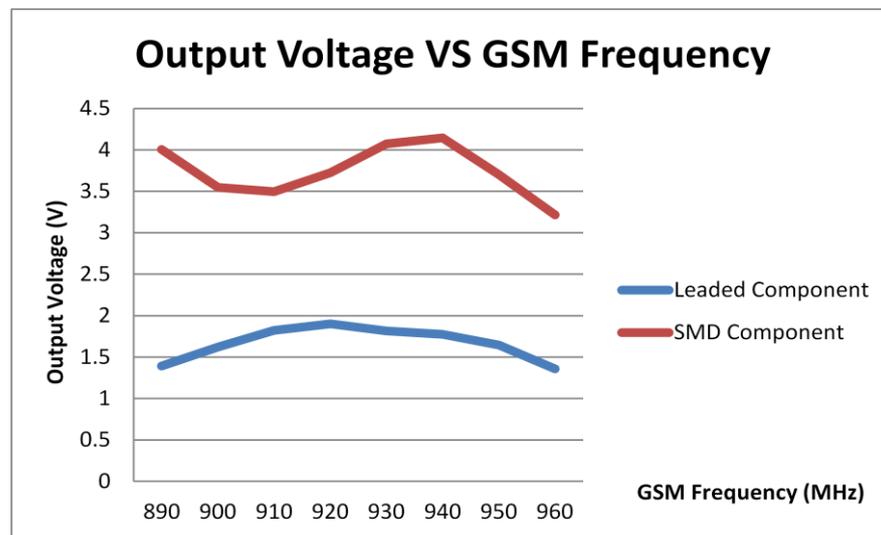


Figure 4.1.3.2 Component Dielectric Loss

4.1.4 3 Stage Dickson's Topology with Load Analysis

In the lab experiment based on free space transmission, the 3 stages Dickson's topology of RF energy harvester is tested with 11 different measurements of distances. An 8dBi transmitter that transmits signal at 915

MHz is used as the RF source where a GSM receiver antenna with 2dBi that connected to the circuit is used to receive the signal. According to Table 4.1.4.1 with approximately close to 0m the energy harvested 22.4V at +4.22dBm with no load. The high output voltage is due to a very minimal free space loss occurred. If it were to compare with energy harvested at 5m from the transmitter the voltage is definitely much lower due to a higher free space loss. However distance should not be the only restriction on RF energy harvesting as the specification of the transmitter and receiver will too need to be superior enough. In case of the receiver can be replaced to what similar to a mobile phones and the signal is transmitted from the cell tower, the possibility of harvesting a higher output voltage is fairly increased. Though, another limitation shall be considered when the circuitry system is loaded. As per Table 4.1.4.2 the output voltage dropped significantly when a 1.5kΩ load is attached to the RF energy harvester. In other words the size of the load will not influence the energy harvested but will manipulate the output voltage after the load.

Table 4.1.4.1 No Load 3 Stage Dickson's Topology Data

Transmitter: 915MHz , 8dBi Receiver: 2dBi Load: N/A				
Distance (m)	Power Ratio (dBm)	Output Voltage (V)	Output Current (mA)	Power Amplitude (W)
0	+4.22	22.400	448	10.035
0.5	-13.20	17.950	359	6.444
1.0	-14.00	7.673	153	1.173
1.5	-17.80	4.455	89	0.396
2.0	-22.50	4.085	81	0.330
2.5	-25.30	1.980	39	0.077
3.0	-29.60	1.857	37	0.068
3.5	-33.70	1.475	29	0.042
4.0	-40.60	1.238	24	0.029
4.5	-42.90	1.980	39	0.077
5.0	-52.00	2.970	59	0.175

Table 4.1.4.2 Loaded 3 Stage Dickson's Topology Data

Transmitter: 915MHz , 8dBi Receiver: 2dBi Load: 1.5k Ω				
Distance (m)	Power Ratio (dBm)	Output Voltage (V)	Output Current (mA)	Power Amplitude (W)
0	+3.58	4.219	2.812	11.8638
0.5	-14.00	1.240	0.820	1.0168
1.0	-37.80	0.620	0.413	0.2560
1.5	-38.70	0.247	0.164	0.0405
2.0	-39.10	0.247	0.164	0.0405
2.5	-35.00	0.312	0.208	0.0648
3.0	-39.30	0.302	0.201	0.0607
3.5	-41.70	0.248	0.166	0.0411
4.0	-37.50	0.247	0.165	0.0410
4.5	-34.60	0.248	0.165	0.0409
5.0	-35.80	0.249	0.166	0.0413

4.2 PRODUCT

RF energy harvester circuit is fabricated using both SMD and leaded component using 3 stages Dickson's topology circuit as well on two different types of PCB board for selection analysis. The end products are displayed as follows.

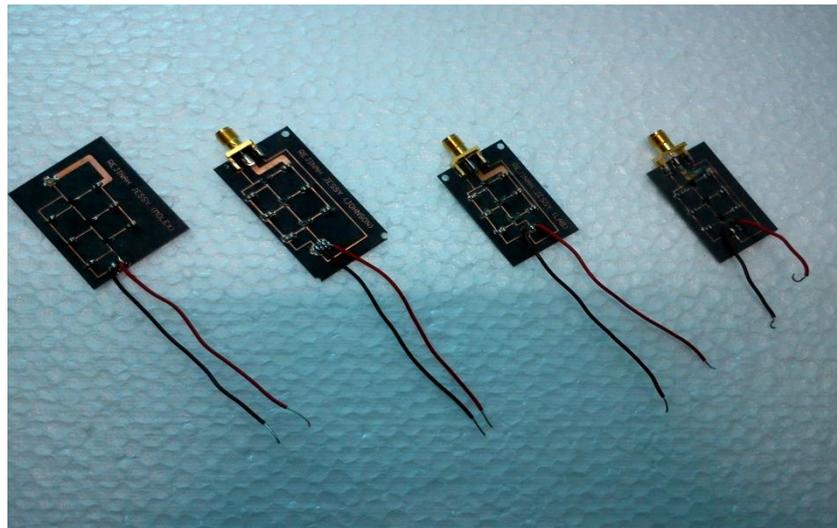


Figure 4.2.1 SMD Component 3 Stages RF Energy Harvester Circuit

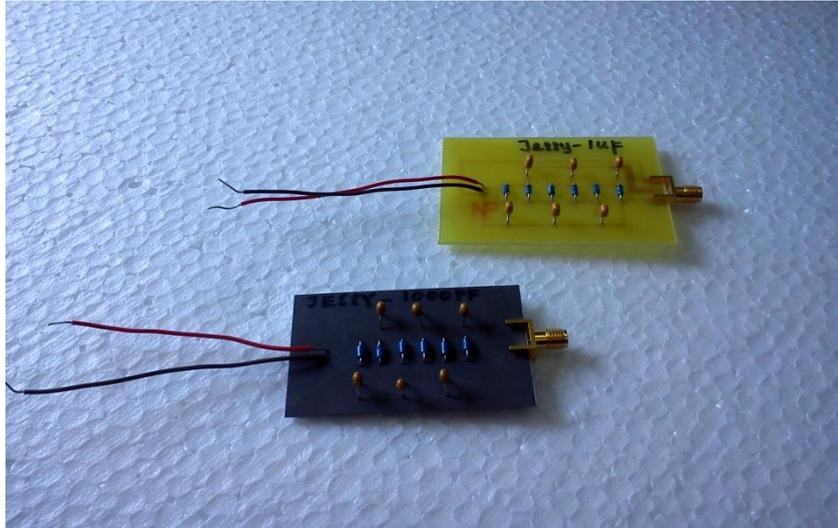


Figure 4.2.2 Leaded Component 3 Stages RF Energy Harvester Circuit

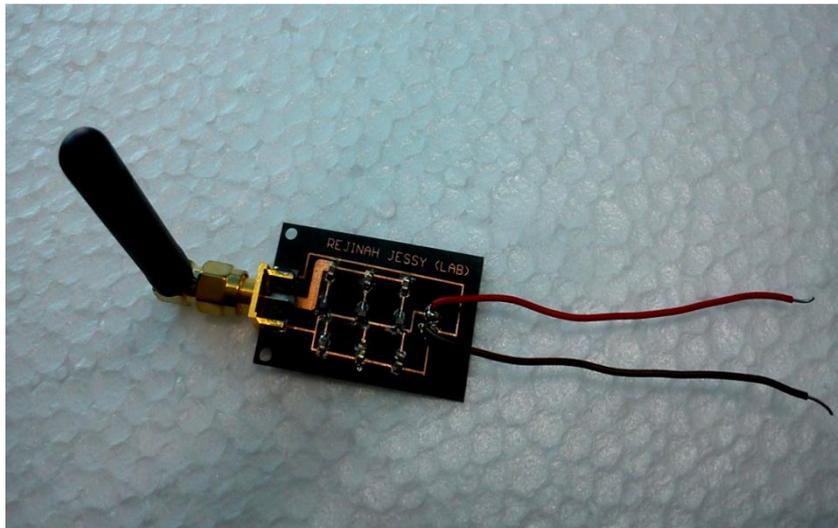


Figure 4.2.3 RF Energy Harvester Circuit with Receiver Antenna

CHAPTER 5

CONCLUSION AND RECOMMENDATION

5.1 CONCLUSIONS

RF Energy Harvester critical analysis, methodology, and its design have been presented in this dissertation. RF energy harvester is chosen above all other energy harvester due to its zero dependency on the human energy and its other surpasses characteristics. Resulting from the critical analysis on the most suited frequency band for energy harvesting, GSM-900 RF energy harvester has potentially excel than the WIFI - 2.4GHz RF energy harvester due to the range of distance that each of the harvester can scavenge from the RF source. Furthermore, an analysis on the PCB by taking deliberation on material influence on output loss is done in which Rogers RO5880 type of PCB is selected. Consequently, a 3 stage Dickson's topology that utilise 890MHz – 960 MHz is imposed on the RF Energy Harvester circuit by using a low resistance and inductance surface mount devices. As a conclusion, all the milestones have been achieved. Hence, with no doubt this project has proven the stated hypothesis and achieved its objectives.

5.2 RECOMMENDATION

In the progress on achieving milestone in this project, the author has implemented Agilent ADS software. Agilent ADS is simulation software that enable user to design the RF electronic product or circuit. The author recommends UTP to use this software for academic purpose in the course of *Electromagnetic Theory* and *Communication System*. High level simulation software like this should be used to improve the UTP undergraduate's designing skills and simulation skill that involved radio frequency which can too cultivate students to become a good quality design engineer in the future.

On the other hand, for future improvement on this project, the author would like to advocate that a current booster shall be integrated into this RF energy harvesting circuit. By doing so, an increased output current can be obtained to charge or to support a higher current rating electronics devices.

Moving forward to a bigger scale, which take consideration on the country economic growth and the increased consumer cost of living, the author are inspired by this miniature system of RF energy harvester which leads to a motivation on to build a RF energy power station with a larger scale that similar to the concept of the current project nearby the cellular base station. If the suggested idea can be implemented, the author believes that the amount of energy recycled is able to leads towards sustainable future. Also, it is capable in preserving the environment by reducing the energy produced by pollutant source such as fossil fuel.

As a strong recommendation, the RF Energy Harvester can be implemented in the fire fighter monitoring system to substitute the battery usage on the fireman. This is because when fire fighters is on duty in hazardous fire breakout environment, the ambient temperature will increased drastically hence will lead to battery explosion if batteries were to be used to energize the sensors which requires to send signal to the monitoring system. By surrogating usage of battery to RF energy Harvester circuit, the safety of fire fighters can be secured.

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APPENDICES

Glass cloth base epoxy resin
Flame retardant copper clad laminate

NAN YA PLASTICS CORPORATION
ELECTRONIC MATERIALS DIVISION
COPPER CLAD LAMINATE DEPARTMENT

FR4-86 UV BLOCK

FEATURES

- UV solder mask may be applied simultaneously in order to increase yields
- Excellent dimensional stability through-hole reliability
- Excellent electrical, chemical and heat resistance properties
- IPC-4101C L21 specification is applicable
- UL designation : ANSI grade FR-4
- UL file number E98983
- Outstanding heat resistance
- High luminance of multi-functionnal Epoxy contrast with copper for A.O.I.
- Traditionnal FR4 method processability
- CAF Resistent laminates

PERFORMANCE LIST

Characteristics		Unit	Conditioning	Test Method	Spec.	Typical values		
ELECTRICAL PROPRIETY	Volume resistivity	MΩ-cm	C-96/35/90	02/05/17	10 ⁶ ↑	5.0x10 ⁸ - 5.0x10 ⁹		
	Surface resistivity	MΩ			10 ⁴ ↑	5.0x10 ⁶ - 5.0x10 ⁷		
	Permittivity 1 Mhz	-	C-24/23/50	2.5.5.9	5.4 ↓	4.5 - 4.7		
	Permittivity 100 Mhz	-	-	-	-	-		
	Permittivity 1 Ghz	-	C-24/23/50	2.5.5.9	-	4.0 - 4.2		
	Permittivity 2 Ghz	-	-	-	-	-		
	Loss tangent 1Mhz	-	C-24/23/50	2.5.5.9	0.035 ↓	0.015-0.020		
	Loss tangent 100 Mhz	-	-	-	-	-		
	Loss tangent 1 Ghz	-	C-24/23/50	2.5.5.9	-	0.012-0.014		
	Loss tangent 2 Ghz	-	-	-	-	-		
	Arc resistance	Seconde	D-48/50+D-05/23	02/05/01	60 ↑	120 ↑		
	Dielectric breakdown	KV	D-48/50	02/05/06	40 ↑	60 ↑		
Electric strength	KV/mm	-	2.5.6.2.	30 ↑	40 ↑			
C.T.I.	-	-	UL94	N/A	3 (175V-249V)			
THERMAL PROP.	Thermal stress	Seconde	288°C solder dipping	2.4.13.1	10 ↑	200 ↑		
	Thermal conductivity	Kcal/mh°C	Hot wire test	JIS R2618	N/A	0,0493		
	Flammability	-	C-24/23/50+E-24/125	UL94	94 V0	94V0		
	Glass transition temp.	°C	DSC	2.4.25	N/A	140 ±5		
	TMA 260°C Delamination	Minute	TMA	2.4.24.1	N/A	> 20'		
	TMA 288°C Delamination	Minute	TMA	2.4.24.1	N/A	>2'		
	Td (5% weight loss)	°C	TGA, 10°C/min	-	N/A	> 310		
	Td (5% weight loss)	-	TGA, 20°C/min	-	N/A	N.A.		
MECHANICAL PROPRIETY	Yield stress test (1mm↑)	-	0.71 MM – 1.3 mm/min (A condition)					
	- Bend strength WD	Kg/cm ²					N/A	4120
	- Bend strength FD	Kg/cm ²					N/A	3553
	- Flexibility WD	Kg/mm ²					N/A	3035
	- Flexibility FD	Kg/mm ²					N/A	2592
	Young's Modulous	-						
	- Pull extend strength WD	Kg/cm ²	0.71 MM – 20 mm/min (A condition)					
	- Pull extend strength FD	Kg/cm ²					N/A	4315
	- Flexibility WD	Kg/mm ²					N/A	3391
	- Flexibility FD	Kg/mm ²					N/A	1001
	- Flexibility FD	Kg/mm ²					N/A	939
	Dimensional stability X-Y axis	%					E 4/105	02/04/39
Z axis expansion	-	-	-	-	-			
C.T.E. :	-	-	-	-	-			
- X-Y axis	-	-	-	-	-			
- Z axis before Tg	ppm/°C	TMA	02/04/24	N/A	50-70			
- Z axis after Tg	ppm/°C	TMA	02/04/24	N/A	250-350			
Others	Moisture absorption	%	D-24/23	2/6/2/1	0.35 ↓	0.05-0.10		
	Peel strength 35µ	lb/in	288°Cx10" solder floating	02/04/08	6 ↑	10.0-14.0		

Data shown are nominal values for reference only.
Test method per IPC-TM-650

Note : The average value in the table refers to samples
0.062 " 1/1

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FR4 86 UV BLOCK

CERTIFICATION UL – UL FILE N° E98983

INDUSTRIAL LAMINATES

industrial laminates furnished as sheets

ANSI Type	Color	Build up Min Thk (mm)	Flame Class	R.T.I. Elec C	Mech C	HWI	HAI	H VTR	CTI	Meets 764E DSR
FR-4	NC	0.18	V-0	130	105	0	0	-	-	yes
		0.38			130					
		0.64			140					
		1.40			140					

ULTRATHIN BUILD UPS

Ultrathin industrial laminates and bonding layers, furnished in sheet form, for use in multilayer printed wiring boards where the thickness is built up to the minimum specified.

Build up				Laminate			Preg		
ANSI Type	Min Thk (mm)	TI Elec	TI Mec	Mtl Dsg	Thk (mic)	TI Elec	Mtl Dsg	Thk (mic)	TI Elec
FR-4	0.18	130	105	FR-4-86, FR-4-TL, UV BLOCK FR-4-86	100	120	NYP-1	50	90
	0.38		130						
	0.64		140						

METAL CLAD INDUSTRIAL LAMINATES

Metal clad industrial laminates for use in multilayer printed wiring boards with copper on one or both sides, furnished as sheets

Laminates Dsg	Prepreg Dsg	ANSI Type	Build up Min Thk (mm)	Clad Cond Thk			Max Area Diam (mm)	Flame Class	Max Oper Temperature (°C)	Solder Lts	
				Min Ext (mic)	Max Ext (mic)	Max Int (mic)				Temp (°C)	Time (Sec)
FR-4-86, FR-4-TL, UV BLOCK FR-4-86	NYP-1	FR-4	0.64	17	102	102	50.8	V-0	130	288	30

Metal clad industrial laminates for use in single layer printed wiring boards with copper on one or both sides, furnished as sheets.

Laminates Dsg	Prepreg Dsg	ANSI Type	Build up Min Thk (mm)	Clad Cond Thk			Max Area Diam (mm)	Flame Class	Max Oper Temperature (°C)	Solder Lts		
				Min Ext (mic)	Max Ext (mic)	Max Int (mic)				Temp (°C)	Time (Sec)	
FR-4-86, FR-4-TL, UV BLOCK FR-4-86	-	FR-4	0.38	17	137	-	50.80	V-0	130	288	30	
			0.64	17	102	-	50.80	V-0	130	180	1200	
											230	120
											260	20

Glass cloth base epoxy resin
Flame retardant copper clad laminate

NAN YA PLASTICS CORPORATION
ELECTRONIC MATERIALS DIVISION
COPPER CLAD LAMINATE DEPARTMENT

NP 140 MD

FEATURES

- UV solder mask may be applied simultaneously in order to Increase yields
- Excellent dimensional stability through-hole reliability
- Excellent electrical, chemical and heat resistance properties
- IPC-4101C L21/121
- UL designation : ANSI grade FR-4
- UL file number E98983
- Outstanding heat resistance
- High luminance of multi-functionnal Epoxy contrast with copper for A.O.I.
- Traditionnal FR4 method processability
- CAF Resistent laminates

PERFORMANCE LIST

Characteristics		Unit	Conditioning	Test Method	Spec.	Typical values
ELECTRICAL PROPRIETY	Volume resistivity	MΩ-cm	C-96/35/90	02/05/17	10 ⁶ ↑	5.0x10 ⁹
	Surface resistivity	MΩ			10 ⁴ ↑	5.0x10 ⁷
	Permittivity 1 Mhz	-	C-24/23/50	2.5.5.9	5.4 ↓	4.2-4.4
	Permittivity 100 Mhz	-			-	
	Permittivity 1 Ghz	-	C-24/23/50	2.5.5.9	-	3.8-4.0
	Permittivity 2 Ghz	-			-	
	Loss tangent 1Mhz	-	C-24/23/50	2.5.5.9	0.035 ↓	0.015-0.020
	Loss tangent 100 Mhz	-			-	
	Loss tangent 1 Ghz	-	C-24/23/50	2.5.5.9	-	0.012-0.014
	Loss tangent 2 Ghz	-			-	
	Arc resistance	Seconde	D-48/50+D-05/23	02/05/01	60 ↑	120 ↑
	Dielectric breakdown	KV	D-48/50	02/05/06	40 ↑	60 ↑
	Electric strength	KV/mm	-	2.5.6.2.	30 ↑	40 ↑
C.T.I.	-	-	UL94	N/A	3 (175V-249V)	
THERMAL PROP.	Thermal stress	Seconde	288°C solder dipping	2.4.13.1	10 ↑	90 ↑
	Thermal conductivity					
	Flammability		C-24/23/50+E-24/125	UL94	94 V0	94V0
	Glass transition temp.	°C	DSC	02/04/25	N/A	135 ±5
	TMA 260°C Delamination	Minute	TMA	2.4.24.1	N/A	> 30'
	TMA 288°C Delamination	Minute	TMA	2.4.24.1	N/A	>5'
	Td (5% weight loss)	°C	TGA, 10°C/min	-	N/A	> 310
	Td (5% weight loss)		TGA, 20°C/min		N/A	N.A.
MECHANICAL PROPRIETY	Yield stress test (1mm↑)		0.71 MM – 1.3 mm/min (A condition)			
	- Bend strength WD	Kg/cm ²			N/A	4120
	- Bend strength FD	Kg/cm ²			N/A	3553
	- Flexibility WD	Kg/mm ²			N/A	3035
	- Flexibility FD	Kg/mm ²			N/A	2592
	Young's Modulous		0.71 MM – 20 mm/min (A condition)			
	- Pull extend strength WD	Kg/cm ²			N/A	4315
	- Pull extend strength FD	Kg/cm ²			N/A	3391
	- Flexibility WD	Kg/mm ²			N/A	1001
	- Flexibility FD	Kg/mm ²			N/A	939
	Dimensional stability X-Y axis	%	E 4/105	02/04/39	0.05 ↓	0.01-0.03
	Z axis expansion	%				
	C.T.E. :					
- X-Y axis						
- Z axis before Tg	ppm/°C	TMA	02/04/24	N/A	50-70	
- Z axis after Tg	ppm/°C	TMA	02/04/24	N/A	250-350	
Others	Moisture absorption	%	D-24/23	2/6/2/1	0.35 ↓	0.20-0.30
	Peel strength 35μ	lb/in	288°Cx10" solder floating	02/04/08	6 ↑	10.0-14.0

Data shown are nominal values for reference only.
 Test method per IPC-TM-650

Note : The average value in the table refers to samples
 0.20 " 1/1

NP140 MD

CONSTRUCTION

Thickness		Construction	
Mm	Mil		
0,10	4	1080	2 plies
0,11	4	2116	1 ply
0,13	5	1080	2 plies
0,13sp	5	2116	1 ply
0,15	6	1506	1 ply
0,16	6	2112	2 plies
0,21	8	7628	1 ply
0,26	10	2116	2 plies
0,30	12	2116	3 plies
0,30sp	12	1506	2 plies
0,35	14	7628	2 plies

Thickness		Construction	
Mm	Mil		
0,38	15	7628	2 plies
0,45	18	7628x2+1080x1	
0,50	20	7628	3 plies
0,53	5	7628	3 plies
0,60	24	7628	3 plies
0,77	30	7628	4 plies
0,80	31	7628	4 plies
0,90	35	7628	5 plies
1,00	39	7628	5 plies
1,10	12	7628	6 plies
1,20	47	7628	6 plies

- 1,2 mm – 1,1 mm – 1,0 mm – 0,9 mm – 0,77 mm Thicknesses include cladding / All others exclude cladding

PRODUCT SIZE & THICKNESS

Thickness		Copper Cladding
Mm	Mil	
0.05 to 1.2	2 to 47	12 micron to 105 micron

Size		Thickness Tolerance
Inch	Mm	
48.8 x 36.6	1240x930	IPC-4101B Spec Class C/M
48.8 x 42.5	1240x1080	

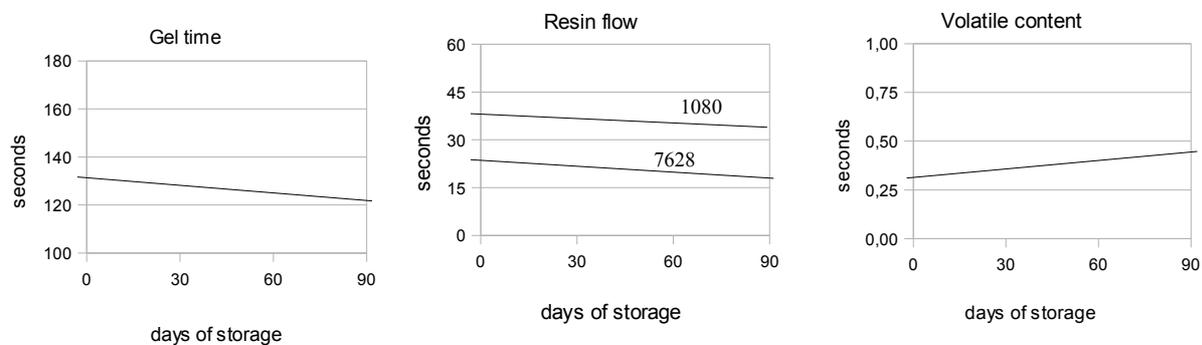
Keeping the core and prepreg in the same grain direction is crucial to ensure the flatness of multilayer boards
Grain direction is shown on the certificate of conformance

NP140 MD

PERFORMANCE LIST

Glass style	RC%	RF%	GT sec (170°C)	VC%	After Pressed Thickness (per ply)	
					mm	Mil
7628 HR	50 ± 3	28 ± 5	130 ± 20	0.75 ↓	0.200 ± 0.010	7.9 ± 0.4
7628 MR	47 ± 3	25 ± 5			0.190 ± 0.010	7.5 ± 0.4
7628	43 ± 3	20 ± 5			0.180 ± 0.010	7.1 ± 0.4
1506 MR	52 ± 3	30 ± 5			0.160 ± 0.010	6.3 ± 0.4
1506	48 ± 3	25 ± 5			0.150 ± 0.010	6.0 ± 0.4
2116HR	58 ± 3	35 ± 5			0.130 ± 0.010	5.0 ± 0.4
2116MR	54 ± 3	30 ± 5			0.118 ± 0.010	4.6 ± 0.4
2116	50 ± 3	25 ± 5			0.105 ± 0.010	4.1 ± 0.4
2313	55 ± 3	30 ± 5			0.090 ± 0.010	3.5 ± 0.4
2113	56 ± 3	30 ± 5			0.090 ± 0.010	3.5 ± 0.4
2112	60 ± 3	35 ± 5			0.075 ± 0.008	3.0 ± 0.3
1080 HR	68 ± 3	45 ± 5			0.071 ± 0.008	2.8 ± 0.3
1080 MR	65 ± 3	40 ± 5			0.068 ± 0.008	2.7 ± 0.3
1080	62 ± 3	35 ± 5			0.065 ± 0.008	2.6 ± 0.3
106	68 ± 3	40 ± 5			0.053 ± 0.008	2.1 ± 0.3

STORAGE STABILITY



Storage Condition : 20°C 50% RH for 3 months, max. 5°C for 6 months

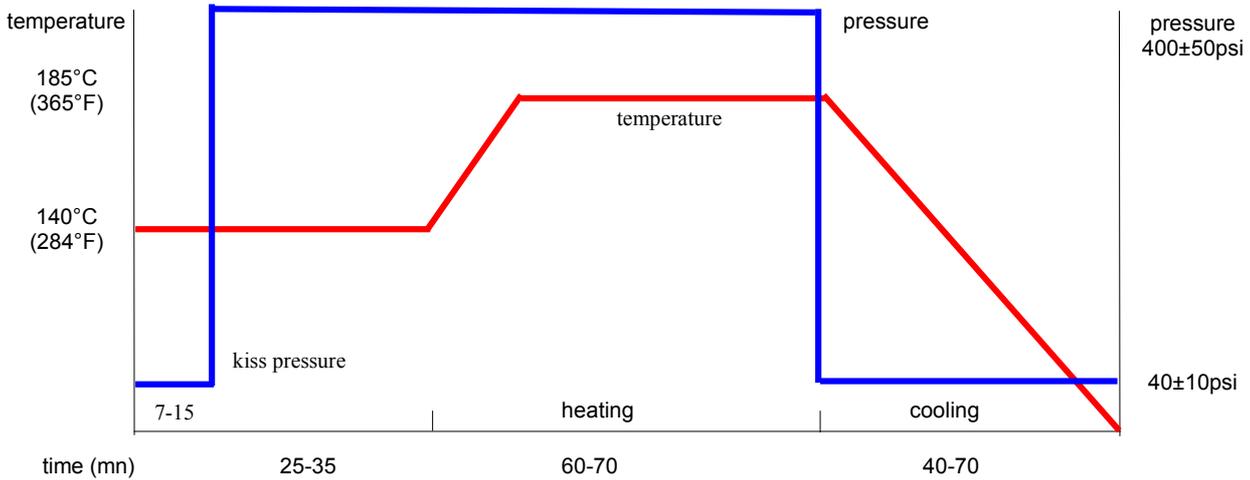
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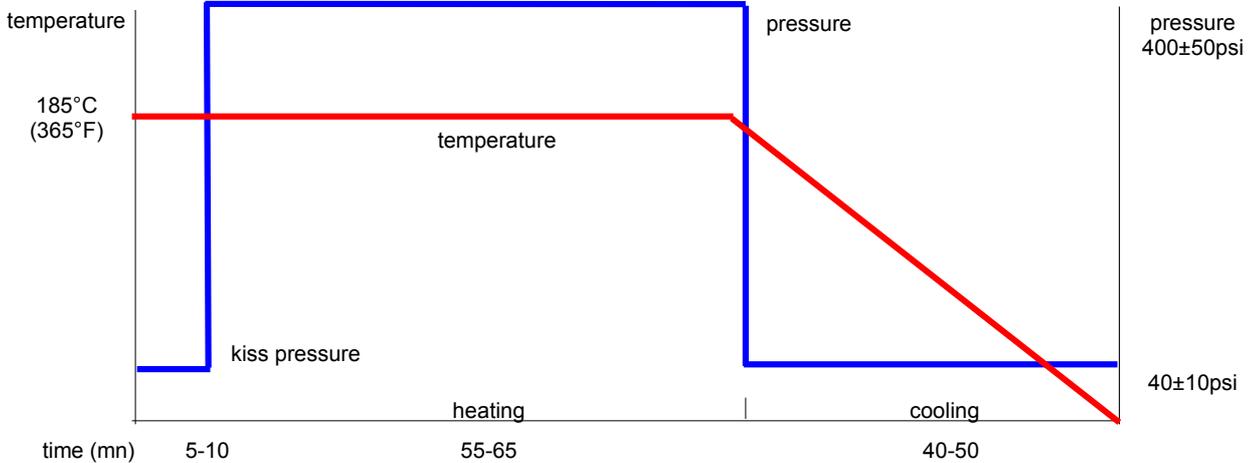
NP140 MD

RECOMMENDED PRESS CYCLE

2 steps



hot press



Suggestions

1. Heating rate of material between 70°C and 140°C
 1-3°C/mn is acceptable
 1.5-2.5°C/min would be better
2. Temperature of material over 170°C must be held for at least 60 minutes to allow epoxy resin to fully cure
3. The pressure should be kept below 7 bars during cooling to ambient temperature
4. Cooling rate of material should be kept under 2.5°C/mn when the temperature of material is over 100°C in order to avoid introducing twist

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NP140 MD UL

CERTIFICATION UL – UL FILE N° E98983

INDUSTRIAL LAMINATES

industrial laminates furnished as sheets

ANSI Type	Color	Build up Min Thk (mm)	Flame Class	R.T.I. Elec C	Mech C	HWI	HAI	H VTR	CTI	Meets 764E DSR
FR-4		0.25	V-0	120	130	3	3	-	-	yes
		0.38		130	130	0	3	-	-	yes
		0.64		130	140	0	3	4	-	yes
		1.40		130	140	0	2	4	3	yes
		0.04		90	90	3	4	-	-	-

ULTRATHIN BUILD UPS

Ultrathin industrial laminates and bonding layers, furnished in sheet form, for use in multilayer printed wiring boards where the thickness is built up to the minimum specified.

ANSI Type	Build up			Laminate			Preg		
	Min Thk (mm)	TI Elec	TI Mec	Mtl Dsg	Thk (mic)	TI Elec	Mtl Dsg	Thk (mic)	TI Elec
FR-4	0.25	120	130	NP-140R, NP-140TL, NP-140MR, NP-140MTL	50	90	NP-140B, NP-140MB	38	50
	0.38	130	130						
	0.64	130	140						

METAL CLAD INDUSTRIAL LAMINATES

Metal clad industrial laminates for use in multilayer printed wiring boards with copper on one or both sides, furnished as sheets

Laminates Dsg	Prepreg Dsg	ANSI Type	Build up Min Thk (mm)	Clad Cond Thk			Max Area Diam (mm)	Flame Class	Max Oper Temperature (°C)	Solder Lts	
				Min Ext (mic)	Max Ext (mic)	Max Int (mic)				Temp (°C)	Time (Sec)
NP-140R, NP-140TL, NP-140MR, NP-140MTL	NP-140B, NP-140MB	FR-4	0.25	17	102	68	50.80	V-0	120	288	30
			0.38						130	288	30
			0.64						130	180	1200
									230	120	
									260	20	

Metal clad industrial laminates for use in single layer printed wiring boards with copper on one or both sides, furnished as sheets.

Laminates Dsg	Prepreg Dsg	ANSI Type	Build up Min Thk (mm)	Clad Cond Thk			Max Area Diam (mm)	Flame Class	Max Oper Temperature (°C)	Solder Lts	
				Min Ext (mic)	Max Ext (mic)	Max Int (mic)				Temp (°C)	Time (Sec)
NP-140R, NP-140TL, NP-140MR, NP-140MTL	-	FR-4	0.25	17	102	-	50.80	V-0	120	288	30
			0.38	17	102	-	50.80	V-0	130	288	30
			0.64	17	102	-	50.80	V-0	130	180	1200
										230	120
										260	20
										260	20
				12	102	-	50.80	V-0	90	288	30

Glass cloth base epoxy resin
 Flame retardant copper clad laminate

NAN YA PLASTICS CORPORATION
 ELECTRONIC MATERIALS DIVISION

NP170

FEATURES

- High Tg 170°C (DSC)
- Excellent dimensional stability through-hole reliability
- Excellent electrical, chemical and heat resistance properties
- IPC-4101C L24/26
- UL designation : ANSI grade FR-4
- UL file number E98983
- Outstanding heat resistance
- High luminance of multi-functionnal Epoxy contrast with copper for A.O.I.
- Traditionnal FR4 method processability
- CAF Resistent laminates

PERFORMANCE LIST

Characteristics		Unit	Conditioning	Test Method	Spec.	Typical values	
ELECTRICAL PROPRIETY	Volume resistivity	MΩ-cm	C-96/35/90	2.5.17.1	10 ⁶ ↑	5.0x10 ⁶ -5.0x10 ⁹	
	Surface resistivity	MΩ			10 ⁴ ↑	5.0x10 ⁶ – 5.0x10 ⁷	
	Permittivity 1 Mhz	-	C-24/23/50	2.5.5.2	5.4 ↓	4.2-4.6	
	Permittivity 100 Mhz	-		2.5.5.3	-	4.1 - 4.3	
	Permittivity 1 Ghz	-	C-24/23/50	2.5.5.9	-	3.9-4.2	
	Permittivity 2 Ghz	-		2.5.5.5	-	3.8-4.2	
	Loss tangent 1Mhz	-	C-24/23/50	2.5.5.2	0.035 ↓	0.020	
	Loss tangent 100 Mhz	-		2.5.5.3	-	0.016 – 0.018	
	Loss tangent 1 Ghz	-	C-24/23/50	2.5.5.9	-	0.012-0.014	
	Loss tangent 2 Ghz	-		2.5.5.5	-	0.011 – 0.013	
	Arc resistance	Seconde	D-48/50+D-05/23	2.5.1	60 ↑	120 ↑	
	Dielectric breakdown	KV	D-48/50	2.5.6	40 ↑	60 ↑	
Electric strength	KV/mm	-	2.5.6.2.	30 ↑	40 ↑		
C.T.I.	-	-	UL94	N/A	4 (100V-174V)		
THERMAL PROP.	Thermal stress	Seconde	288°C solder dipping	2.4.13.1	10 ↑	90 ↑	
	Thermal conductivity	Kcal/mh°C	Hot wire test	JIS R2618	N/A	0,0493	
	Flammability	-	C-24/23/50+E-24/125	UL94	94 V0	94V0	
	Glass transition temp.	°C	DSC	2.4.25	N/A	170 ±5	
	TMA 260°C Delamination	Minute	TMA	2.4.24.1	N/A	25	
	TMA 288°C Delamination	Minute	TMA	2.4.24.1	N/A	3	
	Td (5% weight loss)	°C	TGA, 10°C/min	ASTM D3850	N/A	>320	
	Td (5% weight loss)	°C	TGA, 20°C/min	ASTM D3850	N/A	>330	
MECHANICAL PROPRIETY	Yield stress test (1mm↑)		0.26 MM – 1.3 mm/min (A condition)				
	- Bend strength WD	Kg/cm ²			N/A	N/A	
	- Bend strength FD	Kg/cm ²			N/A	N/A	
	- Flexibility WD	Kg/mm ²			N/A	N/A	
	- Flexibility FD	Kg/mm ²				N/A	N/A
	Young's Modulous		0.26 MM – 20 mm/min (A condition)				
	- Pull extend strength WD	Kg/cm ²			N/A	2987	
	- Pull extend strength FD	Kg/cm ²			N/A	82	
	- Flexibility WD	Kg/mm ²			N/A	3057	
	- Flexibility FD	Kg/mm ²			N/A	80	
	Dimensional stability X-Y axis	%	E 4/105	2.4.39	0.05 ↓	0.01-0.03	
	Z axis expansion	%				4.1 – 4.2	
C.T.E. :		TMA	2.4.24	N/A			
- X-Y axis	ppm/°C				15-18		
- Z axis before Tg	ppm/°C				50-70		
- Z axis after Tg	ppm/°C				270-300		
Others	Moisture absorption	%	D-24/23	2.6.2.1	0.35 ↓	0.20-0.30	
	Peel strength 35μ	N/mm	288°Cx10" solder floating	2.4.8.2	1.05 ↑	1.40 ↑	

Data shown are nominal values for reference only
 Test method per IPC-TM-650

Note : The average value in the table refers to samples
 0.20 " 1/1

NP170

CONSTRUCTION

Thickness		Construction	
Mm	Mil		
0,10	4	1080	2 plies
0,11	4	2116	1 ply
0,13	5	1080	2 plies
0,13sp	5	2116	1 ply
0,15	6	1506	1 ply
0,16	6	2112	2 plies
0,21	8	7628	1 ply
0,26	10	2116	2 plies
0,30	12	2116	3 plies
0,30sp	12	1506	2 plies
0,35	14	7628	2 plies

Thickness		Construction	
Mm	Mil		
0,38	15	7628	2 plies
0,45	18	7628x2+1080x1	
0,50	20	7628	3 plies
0,53	5	7628	3 plies
0,60	24	7628	3 plies
0,77	30	7628	4 plies
0,80	31	7628	4 plies
0,90	35	7628	5 plies
1,00	39	7628	5 plies
1,10	12	7628	6 plies
1,20	47	7628	6 plies

- 1,2 mm – 1,1 mm – 1,0 mm – 0,9 mm – 0,77 mm Thicknesses include cladding / All others exclude cladding

PRODUCT SIZE & THICKNESS

Thickness		Copper Cladding
Mm	Mil	
0.05 to 1.2	2 to 47	12 micron to 105 micron

Size		Thickness Tolerance
Inch	Mm	
48.8 x 36.6	1240x930	IPC-4101B Spec Class C/M
48.8 x 42.5	1240x1080	

Keeping the core and prepreg in the same grain direction is crucial to ensure the flatness of multilayer boards
Grain direction is shown on the certificate of conformance

Glass cloth base epoxy resin
Flame retardant copper clad laminate

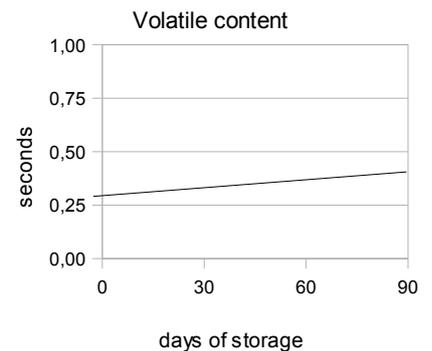
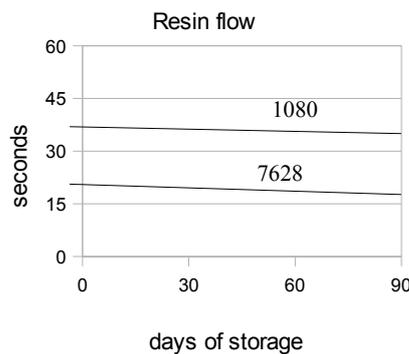
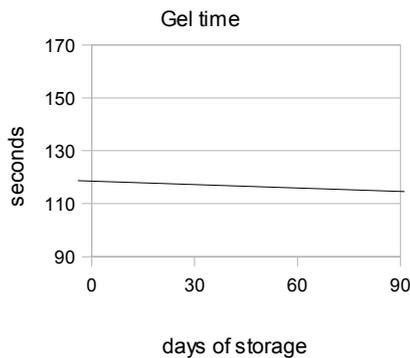
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ELECTRONIC MATERIALS DIVISION
COPPER CLAD LAMINATE DEPARTMENT

NP 170

PERFORMANCE LIST

Glass style	RC%	RF%	GT sec (170°C)	VC%	After Pressed Thickness (per ply)	
					mm	Mil
7628HR	50 ± 3	28 ± 5	120 ± 20	0.75 ↓	0.200 ± 0.01	7.9 ± 0.4
7628MR	47 ± 3	25 ± 5			0.190 ± 0.01	7.5 ± 0.4
7628	43 ± 3	20 ± 5			0.180 ± 0.01	7.1 ± 0.4
1506MR	52 ± 3	30 ± 5			0.160 ± 0.01	6.3 ± 0.4
1506	48 ± 3	25 ± 5			0.150 ± 0.01	6.0 ± 0.4
2116HR	58 ± 3	35 ± 5			0.130 ± 0.01	5.0 ± 0.4
2116MR	54 ± 3	30 ± 5			0.118 ± 0.01	4.6 ± 0.4
2116	50 ± 3	25 ± 5			0.105 ± 0.01	4.1 ± 0.4
2313	55 ± 3	30 ± 5			0.090 ± 0.01	3.5 ± 0.4
2113	56 ± 3	30 ± 5			0.090 ± 0.01	3.5 ± 0.4
2112	60 ± 3	35 ± 5			0.075 ± 0.008	3.0 ± 0.3
1080HR	68 ± 3	45 ± 5			0.071 ± 0.008	2.8 ± 0.3
1080MR	65 ± 3	40 ± 5			0.068 ± 0.008	2.7 ± 0.3
1080	62 ± 3	35 ± 5			0.065 ± 0.008	2.6 ± 0.3
106	68 ± 3	40 ± 5			0.053 ± 0.008	2.1 ± 0.3

STORAGE STABILITY



Storage Condition : 20°C, 50% RH for 3 months, max. 5°C for 6 months

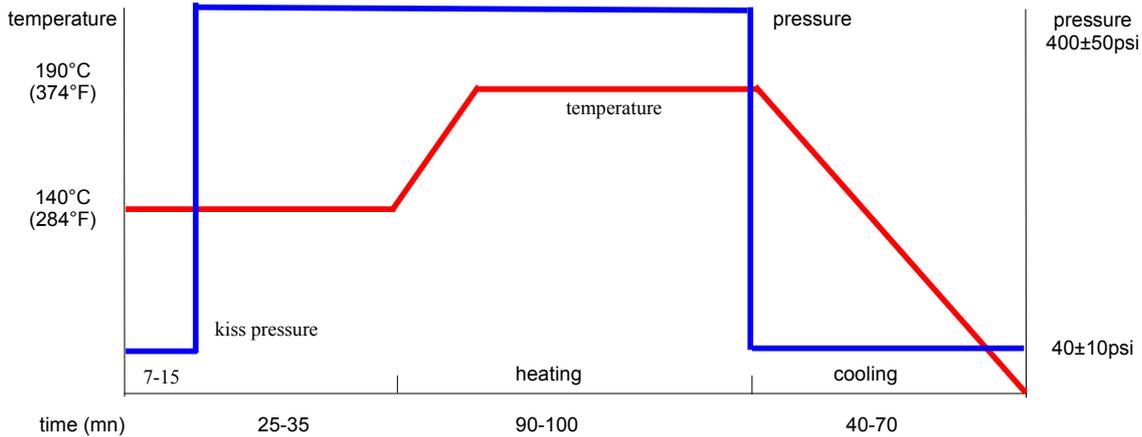
Data shown are nominal values for reference only

Winside – ZI La Marinière – Rue Charles de Gaulle – 91070 Bondoufle
 Contact : Sylvestre Cottard - +33 (0)1 69 11 81 15 - +33 (0)6 13 54 48 46
 Agent NAN YA for Belgium – France – Netherlands – UK

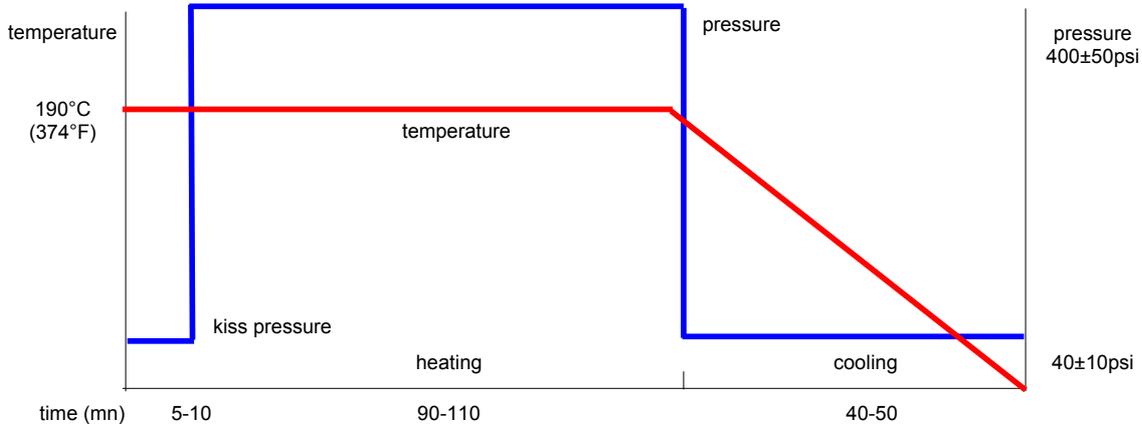
NP170

RECOMMENDED PRESS CYCLE

2 steps



hot press



1. 3°C/mn is acceptable 1.5-2.5°C/min would be better
2. Temperature of material over 170°C must be held for at least 60 minutes to allow epoxy resin to fully cure
3. The pressure should be kept below 7 bars during cooling to ambient temperature
4. Cooling rate of material should be kept under 2.5°C/mn when the temperature of material is over 100°C in order to avoid introducing twist



NP170 UL

CERTIFICATION UL – UL FILE N° E98983

INDUSTRIAL LAMINATES

industrial laminates furnished as sheets

ANSI Type	Color	Build up Min Thk (mm)	Flame Class	R.T.I. Elec C	Mech C	HWI	HAI	H VTR	CTI	Meets 764E DSR
FR-4	NC	0.035	V-0	-	-	-	-	-	-	-
		0.040		90	90	0	4	-	-	-
		0.380		130	130	0	4	-	-	-
		0.640		130	140	0	3	4	-	yes
		1.400		130	140	0	2	4	4	yes

ULTRATHIN BUILD UPS

Ultrathin industrial laminates and bonding layers, furnished in sheet form, for use in multilayer printed wiring boards where the thickness is built up to the minimum specified.

Build up				Laminate			Preg		
ANSI Type	Min Thk (mm)	TI Elec	TI Mec	Mtl Dsg	Thk (mic)	TI Elec	Mtl Dsg	Thk (mic)	TI Elec
FR-4	0.38	130	130	NP-170R, NP-170TL, NP-170SR, NP-170STL	50	90	NP-170B, NP-170SB	50	90
	0.64		140						

METAL CLAD INDUSTRIAL LAMINATES

Metal clad industrial laminates for use in multilayer printed wiring boards with copper on one or both sides, furnished as sheets

Laminates Dsg	Prepreg Dsg	ANSI Type	Build up Min Thk (mm)	Clad Cond Thk			Max Area Diam (mm)	Flame Class	Max Oper Temperature (°C)	Solder Lts	
				Min Ext (mic)	Max Ext (mic)	Max Int (mic)				Temp (°C)	Time (Sec)
NP-170R, NP-170TL, NP-170SR, NP-170STL	NP-170B, NP-170SB	FR-4	0.38	17	102	102	50.80	V-0	130	300	30

Metal clad industrial laminates for use in single layer printed wiring boards with copper on one or both sides, furnished as sheets.

Laminates Dsg	Prepreg Dsg	ANSI Type	Build up Min Thk (mm)	Clad Cond Thk			Max Area Diam (mm)	Flame Class	Max Oper Temperature (°C)	Solder Lts	
				Min Ext (mic)	Max Ext (mic)	Max Int (mic)				Temp (°C)	Time (Sec)
NP-170R, NP-170TL, NP-170SR, NP-170STL	-	FR-4	0.04	12	102	-	50.80	V-0	90	288	30
			0.38	17					130		

**Glass cloth base epoxy resin
Flame retardant copper clad laminate**

NP175 F

FEATURES

- High Tg 170°C (DSC)
- Excellent dimensional stability through-hole reliability
- Excellent electrical, chemical and heat resistance properties
- IPC-4101C L99/126
- DICY Free material
- UL file number E98983
- Outstanding heat resistance
- High luminance of multi-functional Epoxy contrast with copper for A.O.I.
- Fillers added to low the C.T.E.
- CAF Resistent laminates

PERFORMANCE LIST

	Characteristics	Unit	Conditioning	Test Method	Spec.	Typical values
ELECTRICAL PROPRIETY	Volume resistivity	MΩ-cm	C-96/35/90	2.5.17.1	10 ⁶ ↑	5.0x10 ⁹ – 5.0x10 ¹⁰
	Surface resistivity	MΩ			10 ⁴ ↑	5.0x10 ⁸ – 5.0x10 ⁹
	Permittivity 1 Mhz	-	C-24/23/50	2.5.5.2	5.4 ↓	4.2-4.9
	Permittivity 100 Mhz	-		2.5.5.3	-	4.1-4.7
	Permittivity 1 Ghz	-		2.5.5.9	-	4.0-4.6
	Permittivity 2 Ghz	-		2.5.5.5	-	3.9-4.0
	Loss tangent 1Mhz	-		2.5.5.2	0.035 ↓	0.015-0.019
	Loss tangent 100 Mhz	-		2.5.5.3	-	0.012-0.016
	Loss tangent 1 Ghz	-		2.5.5.9	-	0.011-0.013
	Loss tangent 2 Ghz	-		2.5.5.5	-	0.011-0.012
	Arc resistance	Seconde	D-48/50+D-05/23	2.5.1.	60 ↑	120 ↑
	Dielectric breakdown	KV	D-48/50	2.5.6.	40 ↑	60 ↑
	Electric strength	KV/mm	-	2.5.6.2.	30 ↑	40
	C.T.I.	-	-	UL94	N/A	3 (175V – 249V)
THERMAL PROP.	Thermal stress	Seconde	288°C solder dipping	2.4.13.1	10 ↑	600 ↑
	Thermal conductivity	Kcal/mh°C	Hot wire test	JIS R2618	N/A	0.049
	Flammability	-	C-24/23/50+E-24/125	UL94	94V1 ↓	94V0
	Glass transition temp.	°C	DSC	2.4.25.	> 150	170 ±5
	TMA 260°C Delamination	Minute	TMA	2.4.24.1	> 30'	> 60'
	TMA 288°C Delamination	Minute	TMA	2.4.24.1	> 5'	>40'
	Td (5% weight loss)	°C	TGA, 10°C/min	ASTM D3850	> 325	351
	Td (5% weight loss)	°C	TGA, 20°C/min	ASTM D3850	> 325	372
MECHANICAL PROPRIETY	Yield stress test (1mm↑)		0.71 MM – 1.3 mm/min (A condition)			
	- Bend strength WD	Kg/cm ²		N/A	4145	
	- Bend strength FD	Kg/cm ²		N/A	3826	
	- Flexibility WD	Kg/mm ²		N/A	2796	
	- Flexibility FD	Kg/mm ²		N/A	2609	
	Young's Modulous		0.71 MM – 20 mm/min (A condition)			
	- Pull extend strength WD	Kg/cm ²		N/A	3532	
	- Pull extend strength FD	Kg/cm ²		N/A	2943	
	- Flexibility WD	Kg/mm ²		N/A	903	
	- Flexibility FD	Kg/mm ²		N/A	1001	
	Dimensional stability X-Y axis	%	E 4/105	2.4.39.	0.05 ↓	0.01-0.03
	Z axis expansion	%			3,5 ↓	3,0
C.T.E. :		TMA	2.4.24.			
- X-Y axis	ppm/°C			N/A	13-15	
- Z axis before Tg	ppm/°C			60 ↓	40-60	
- Z axis after Tg	ppm/°C			300 ↓	250-270	
Others	Moisture absorption	%	D-24/23	2.6.2.1.	0.35 ↓	0.20 – 0.30
	Peel strength 35µ	N/mm	288°Cx10" solder floating	2.4.8.2.	1.05 ↑	1.40 ↑

Data shown are nominal values for reference only.

Test method per IPC-TM-650

Keeping the core and prepreg in the same grain direction is crucial to ensure the flatness of multilayer boards

Grain direction is shown on the certificate of conformance

Material without logo from 0.05 mm to 1.2 mm

Material with logo from 0.8 mm to 3.2 mm

NP175 F

CONSTRUCTION

Thickness		Construction		Thickness		Construction	
Mm	Mil			Mm	Mil		
0,10	4	1080	2 plies	0,38	15	7628	2 plies
0,11	4	2116	1 ply	0,45	18	7628x2+1080x1	
0,13	5	1080	2 plies	0,50	20	7628	3 plies
0,13sp	5	2116	1 ply	0,53	5	7628	3 plies
0,15	6	1506	1 ply	0,60	24	7628	3 plies
0,16	6	2112	2 plies	0,77	30	7628	4 plies
0,21	8	7628	1 ply	0,80	31	7628	4 plies
0,26	10	2116	2 plies	0,90	35	7628	5 plies
0,30	12	2116	3 plies	1,00	39	7628	5 plies
0,30sp	12	1506	2 plies	1,10	12	7628	6 plies
0,35	14	7628	2 plies	1,20	47	7628	6 plies

- 1,2 mm – 1,1 mm – 1,0 mm – 0,9 mm – 0,77 mm Thicknesses include cladding / All others exclude cladding

PRODUCT SIZE & THICKNESS

Thickness		Copper Cladding	Size		Thickness Tolerance
Mm	Mil		Inch	Mm	
0.05 to 3.2	2 to 126	9 micron to 210 micron	48.8 x 36.6 48.8 x 42.5	1240x930 1240x1080	IPC-4101B Spec Class C/M

Keeping the core and prepreg in the same grain direction is crucial to ensure the flatness of multilayer boards

Grain direction is shown on the certificate of conformance

We recommend to evaluate the drilling property

Different oxide treatment may result in variations in the heat resistance properties of the laminates after processing. Pre-production batch runs are recommended to ensure compatibility of material with chemicals.

Material without logo from 0.05 mm to 1.2 mm

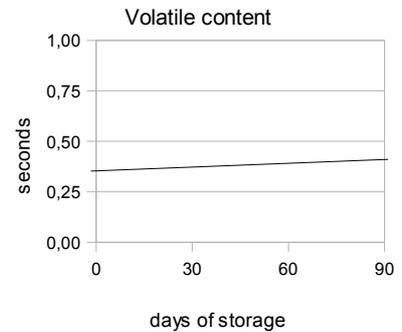
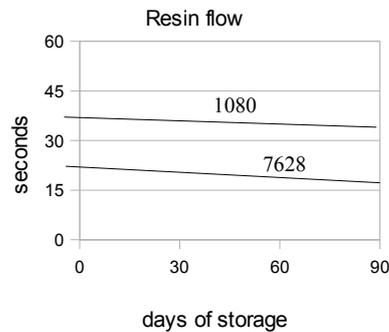
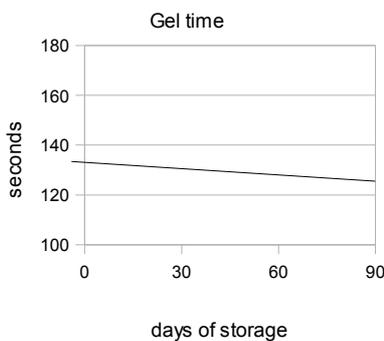
Material with logo from 0.8 mm to 3.2 mm

NP175 F

PERFORMANCE LIST

Glass style	RC%	RF%	GT sec (170°C)	VC%	After Pressed Thickness (per ply)	
					mm	Mil
7628HR	52 ± 3	31 ± 5	170 ± 20	1.5 ↓	0.199 ± 0.01	7.8 ± 0.4
7628MR	49 ± 3	28 ± 5			0.191 ± 0.01	7.5 ± 0.4
7628	45 ± 3	21 ± 5			0.181 ± 0.01	7.1 ± 0.4
1506MR	54 ± 3	34 ± 5			0.160 ± 0.01	6.3 ± 0.4
1506	50 ± 3	27 ± 5			0.150 ± 0.01	5.9 ± 0.4
2116HR	60 ± 3	40 ± 5			0.132 ± 0.01	5.2 ± 0.4
2116MR	56 ± 3	34 ± 5			0.118 ± 0.01	4.6 ± 0.4
2116	52 ± 3	28 ± 5			0.105 ± 0.01	4.1 ± 0.4
2313	57 ± 3	34 ± 5			0.090 ± 0.01	3.5 ± 0.4
2113	58 ± 3	35 ± 5			0.090 ± 0.01	3.5 ± 0.4
2112	62 ± 3	35 ± 5			0.079 ± 0.008	3.1 ± 0.3
1080HR	70 ± 3	50 ± 5			0.076 ± 0.008	3.0 ± 0.3
1080MR	67 ± 3	45 ± 5			0.071 ± 0.008	2.8 ± 0.3
1080	64 ± 3	40 ± 5			0.064 ± 0.008	2.5 ± 0.3
106HR	76 ± 3	54 ± 5			0.053 ± 0.009	2.1 ± 0.3
106MR	74 ± 3	47 ± 5			0.051 ± 0.010	2.0 ± 0.3
106	70 ± 3	42 ± 5			0.048 ± 0.008	1.9 ± 0.3

STORAGE STABILITY



Storage Condition : 20°C – 50% RH : 3 months – 5°C – 50% RH : 6 months

Data shown are nominal values for reference only

Keeping the core and prepreg in the same grain direction is crucial to ensure the flatness of multilayer boards

Grain direction is shown on the certificate of conformance

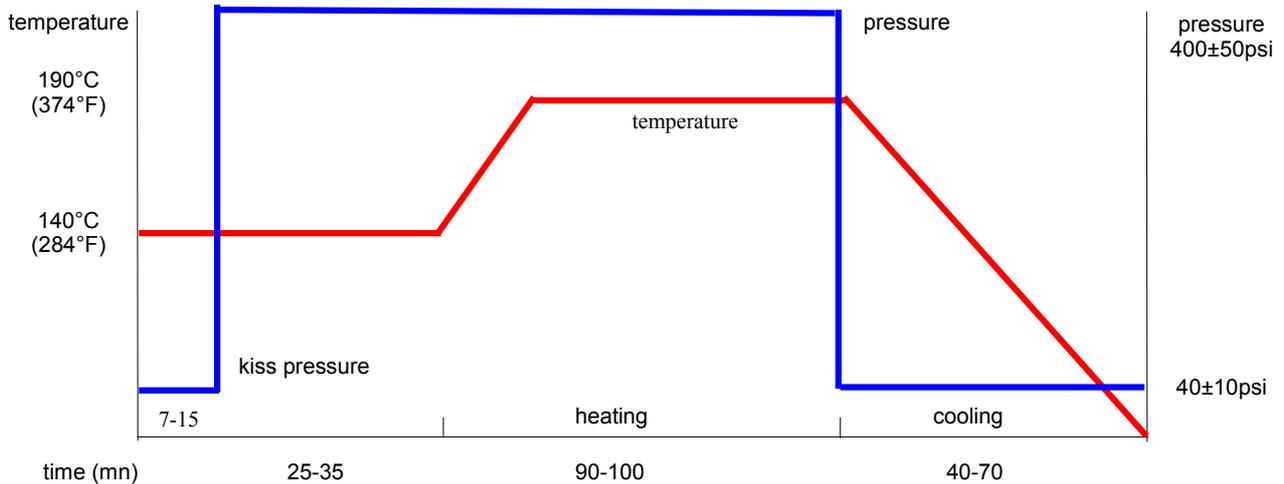
We recommend to evaluate the drilling property

Different oxide treatment may result in variations in the heat resistance properties of the laminates after processing. Pre-production batch runs are recommended to ensure compatibility of material with chemicals.

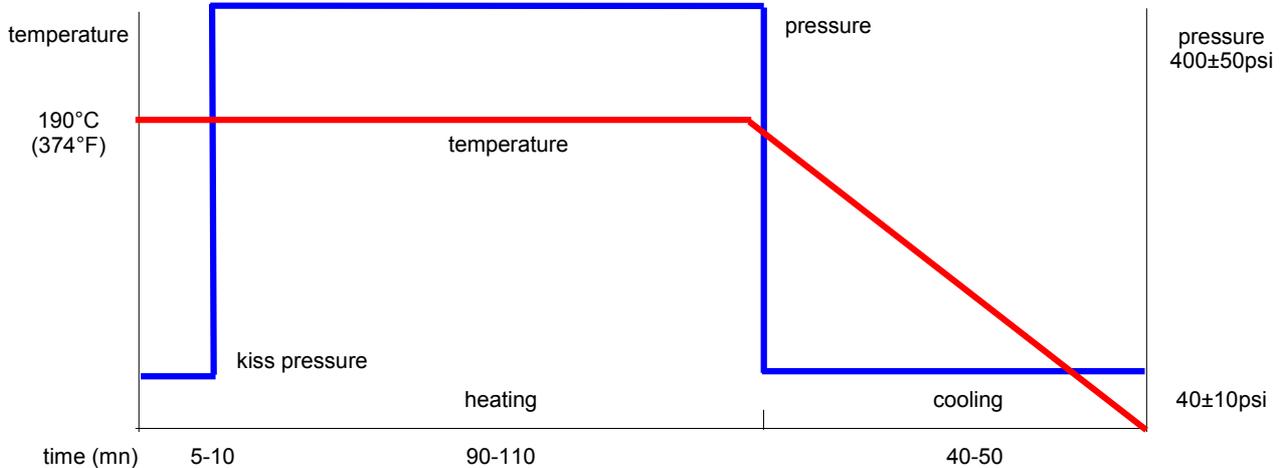
NP175 F

RECOMMENDED PRESS CYCLE

2 steps



hot press



Suggestions

1. Heating rate of material between 70°C and 140°C
1-3°C/mn is acceptable
1.5-2.5°C/min would be better
2. Temperature of material over 170°C must be held for at least 60 minutes to allow epoxy resin to fully cure
3. The pressure should be kept below 7 bars during cooling to ambient temperature
4. Cooling rate of material should be kept under 2.5°C/mn when the temperature of material is over 100°C in order to avoid introducing twist

Keeping the core and prepreg in the same grain direction is crucial to ensure the flatness of multilayer boards
Grain direction is shown on the certificate of conformance

NP175 F

CERTIFICATION UL – UL FILE N° E98983

INDUSTRIAL LAMINATES

industrial laminates furnished as sheets

ANSI Type	Color	Build up Min Thk (mm)	Flame Class	R.T.I. Elec (C)	R.T.I. Mech (C)	HWI	HAI	H VTR	CTI	Meets 764E DSR
FR4	NC	0.38	V-0	130	130	0	0	-	-	Yes
		0.64		130	140	0	0		-	
		1.60		130	140	0	0		3	

ULTRATHIN BUILD UPS

Ultrathin industrial laminates and bonding layers, furnished in sheet form, for use in multilayer printed wiring boards where the thickness is built up to the minimum specified.

Build up			Laminate				Preg		
ANSI Type	Min Thk (mm)	TI Elec	TI Mec	Mtl Dsg	Thk (mic)	TI Elec	Mtl Dsg	Thk (mic)	TI Elec
FR4	0.38	130	130	NP-175FR	50	50	NP-175FB	50	50
	0.38		130	NP-175FTL					

METAL CLAD INDUSTRIAL LAMINATES

Metal clad industrial laminates for use in multilayer printed wiring boards with copper on one or both sides, furnished as sheets

Laminates Dsg	Prepreg Dsg	ANSI Type	Build up Min Thk (mm)	Clad Cond Thk			Max Area Diam (mm)	Flame Class	Max Oper Temperature (°C)	Solder Lts	
				Min Ext (mic)	Max Ext (mic)	Max Int (mic)				Temp (°C)	Time (Sec)
NP-175FR NP-175FTL	NP-175FB	FR4	0.38	9	102	210	50.80	V-0	130	300	30

Metal clad industrial laminates for use in single layer printed wiring boards with copper on one or both sides, furnished as sheets.

Laminates Dsg	Prepreg Dsg	ANSI Type	Build up Min Thk (mm)	Clad Cond Thk			Max Area Diam (mm)	Flame Class	Max Oper Temperature (°C)	Solder Lts	
				Min Ext (mic)	Max Ext (mic)	Max Int (mic)				Temp (°C)	Time (Sec)
NP-175FR NP-175FTL	-	FR4	0.38	9	102	-	50.80	V-0	130	300	30

Keeping the core and prepreg in the same grain direction is crucial to ensure the flatness of multilayer boards
 Grain direction is shown on the certificate of conformance

Material without logo from 0.05 mm to 1.2 mm
 Material with logo from 0.8 mm to 3.2 mm

Glass cloth base epoxy resin
Flame retardant copper clad laminate

NP180 FA

FEATURES

- High Tg 175°C (DSC)
- Excellent dimensional stability through-hole reliability
- Excellent electrical, chemical and heat resistance properties
- IPC-4101C L23/126
- DICY Free material
- UL file number E98983
- Outstanding heat resistance
- High luminance of multi-functional Epoxy contrast with copper for A.O.I.
- Fillers added to low the C.T.E.
- CAF Resistent laminates

PERFORMANCE LIST

Characteristics		Unit	Conditioning	Test Method	Spec.	Typical values
ELECTRICAL PROPRIETY	Volume resistivity	MΩ-cm	C-96/35/90	2.5.17.1	10 ⁶ ↑	5.0x10 ⁹
	Surface resistivity	MΩ			10 ⁴ ↑	5.0x10 ⁸
	Permittivity 1 Mhz	-	C-24/23/50	2.5.5.2	5.4 ↓	4.4-4.7
	Permittivity 100 Mhz	-		2.5.5.3	-	4.2-4.5
	Permittivity 1 Ghz	-		2.5.5.9	-	4.1-4.3
	Permittivity 2 Ghz	-		2.5.5.5	-	4.0-4.1
	Loss tangent 1Mhz	-		2.5.5.2	0.035 ↓	0.019-0.020
	Loss tangent 100 Mhz	-		2.5.5.3	-	0.016-0.018
	Loss tangent 1 Ghz	-		2.5.5.9	-	0.012-0.013
	Loss tangent 2 Ghz	-		2.5.5.5	-	0.011-0.012
	Arc resistance	Seconde	D-48/50+D-05/23	2.5.1.	60 ↑	120 ↑
	Dielectric breakdown	KV	D-48/50	2.5.6.	40 ↑	60 ↑
Electric strength	KV/mm	-	2.5.6.2.	30 ↑	40 ↑	
C.T.I.	-	-	UL94	N/A	3 (175V-249V)	
THERMAL PROP.	Thermal stress	Seconde	288°C solder dipping	2.4.13.1	10 ↑	600 ↑
	Thermal conductivity	Kcal/mh°C	Hot wire test	JIS R2618	N/A	0,0493
	Flammability	-	C-24/23/50+E-24/125	UL94	94V1 ↓	94V0
	Glass transition temp.	°C	DSC	2.4.25.	> 150	175 ±5
	TMA 260°C Delamination	Minute	TMA	2.4.24.1	> 30'	> 60'
	TMA 288°C Delamination	Minute	TMA	2.4.24.1	> 5'	>40'
	Td (5% weight loss)	°C	TGA, 10°C/min	ASTM D3850	> 325	355
Td (5% weight loss)	°C	TGA, 20°C/min	ASTM D3850	> 325	370	
MECHANICAL PROPRIETY	Yield stress test (1mm↑)		0.71 MM – 1.3 mm/min (A condition)			
	- Bend strength WD	Kg/cm ²		N/A	4120	
	- Bend strength FD	Kg/cm ²		N/A	3553	
	- Flexibility WD	Kg/mm ²		N/A	3035	
	- Flexibility FD	Kg/mm ²		N/A	2592	
	Young's Modulous		0.71 MM – 20 mm/min (A condition)			
	- Pull extend strength WD	Kg/cm ²		N/A	4315	
	- Pull extend strength FD	Kg/cm ²		N/A	3391	
	- Flexibility WD	Kg/mm ²		N/A	1001	
	- Flexibility FD	Kg/mm ²		N/A	939	
	Dimensional stability X-Y axis	%	E 4/105	2.4.39.	0.05 ↓	0.01-0.03
	Z axis expansion	%				2.3-2.4
C.T.E. :		TMA	2.4.24.	N/A		
- X-Y axis	ppm/°C				15-18	
- Z axis before Tg	ppm/°C				40-45	
- Z axis after Tg	ppm/°C				150-200	
Others	Moisture absorption	%	D-24/23	2.6.2.1.	0.80 ↓	0.10
	Peel strength 35μ	N/mm	288°Cx10" solder floating	2.4.8.2.	1.05 ↑	1.40 ↑

Data shown are nominal values for reference only.

Test method per IPC-TM-650

Keeping the core and prepreg in the same grain direction is crucial to ensure the flatness of multilayer boards

Grain direction is shown on the certificate of conformance

The material can not be used in horizontal brown oxide process

Material without logo from 0.05 mm to 1.2 mm

Material with logo from 0.8 mm to 3.2 mm

NP180 FA

CONSTRUCTION

Thickness		Construction		Thickness		Construction	
Mm	Mil			Mm	Mil		
0,10	4	1080	2 plies	0,38	15	7628	2 plies
0,11	4	2116	1 ply	0,45	18	7628x2+1080x1	
0,13	5	1080	2 plies	0,50	20	7628	3 plies
0,13sp	5	2116	1 ply	0,53	21	7628	3 plies
0,15	6	1506	1 ply	0,60	24	7628	3 plies
0,16	6	2112	2 plies	0,77	30	7628	4 plies
0,21	8	7628	1 ply	0,80	31	7628	4 plies
0,26	10	2116	2 plies	0,90	35	7628	5 plies
0,30	12	2116	3 plies	1,00	39	7628	5 plies
0,30sp	12	1506	2 plies	1,10	12	7628	6 plies
0,35	14	7628	2 plies	1,20	47	7628	6 plies

- 1,2 mm – 1,1 mm – 1,0 mm – 0,9 mm – 0,77 mm Thicknesses include cladding / All others exclude cladding

PRODUCT SIZE & THICKNESS

Thickness		Copper Cladding	Size		Thickness Tolerance
Mm	Mil		Inch	Mm	
0.05 to 3.2	2 to 126	12 micron to 210 micron	48.8 x 36.6 48.8 x 42.5	1240x930 1240x1080	IPC-4101B Spec Class C/M

Keeping the core and prepreg in the same grain direction is crucial to ensure the flatness of multilayer boards
Grain direction is shown on the certificate of conformance
The material can not be used in horizontal brown oxide process

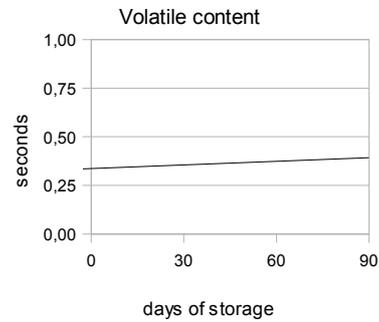
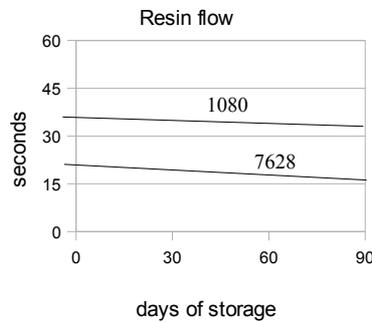
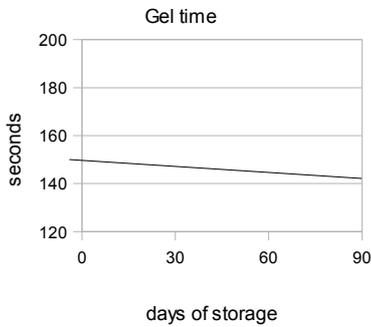
Material without logo from 0.05 mm to 1.2 mm
Material with logo from 0.8 mm to 3.2 mm

NP180 FA

PERFORMANCE LIST

Glass style	RC%	RF%	GT sec (170°C)	VC%	After Pressed Thickness (per ply)	
					mm	Mil
7628HR	50 ± 3	33 ± 5	150 ± 20	0.75 ↓	0.193 ± 0.01	7.6 ± 0.4
7628MR	47 ± 3	34 ± 5			0.183 ± 0.01	7.2 ± 0.4
7628	43 ± 3	35 ± 5			0.173 ± 0.01	6.8 ± 0.4
1506MR	52 ± 3	36 ± 5			0.157 ± 0.01	6.2 ± 0.4
1506	48 ± 3	37 ± 5			0.145 ± 0.01	5.7 ± 0.4
2116HR	58 ± 3	38 ± 5			0.120 ± 0.01	4.7 ± 0.4
2116MR	54 ± 3	32 ± 5			0.109 ± 0.01	4.3 ± 0.4
2116	50 ± 3	26 ± 5			0.097 ± 0.01	3.8 ± 0.4
2313	55 ± 3	33 ± 5			0.081 ± 0.01	3.2 ± 0.4
2113	56 ± 3	32 ± 5			0.081 ± 0.01	3.2 ± 0.4
2112	60 ± 3	38 ± 5			0.069 ± 0.008	2.7 ± 0.3
1080HR	68 ± 3	48 ± 5			0.066 ± 0.008	2.6 ± 0.3
1080MR	65 ± 3	44 ± 5			0.061 ± 0.008	2.4 ± 0.3
1080	62 ± 3	38 ± 5			0.058 ± 0.008	2.3 ± 0.3
106	68 ± 3	41 ± 5			0.046 ± 0.008	1.8 ± 0.3

STORAGE STABILITY



Storage Condition : 20°C – 50% RH : 3 months – 5°C – 50% RH : 6 months

Data shown are nominal values for reference only

Keeping the core and prepreg in the same grain direction is crucial to ensure the flatness of multilayer boards

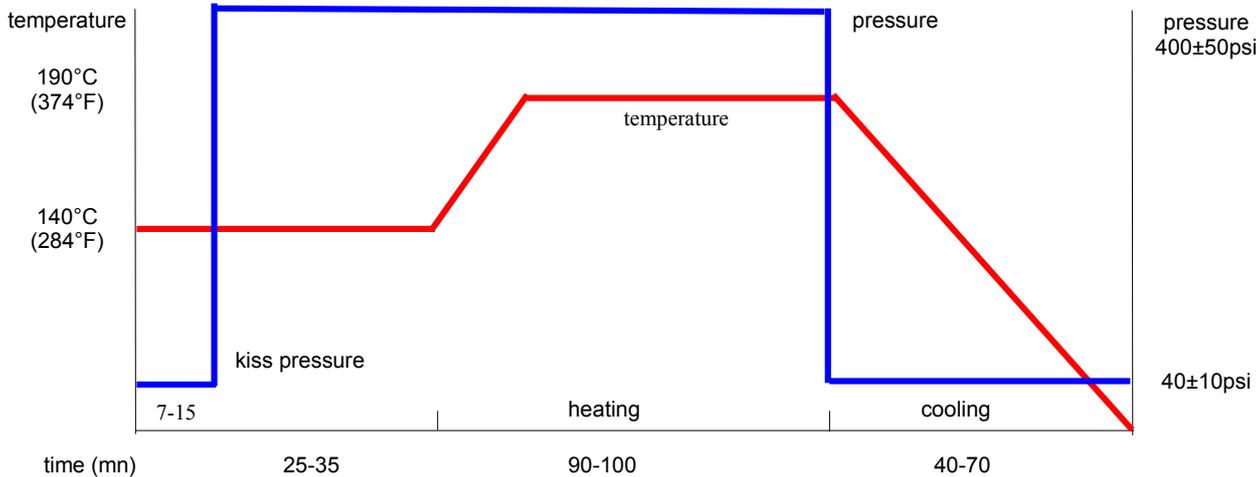
Grain direction is shown on the certificate of conformance

The material can not be used in horizontal brown oxide process

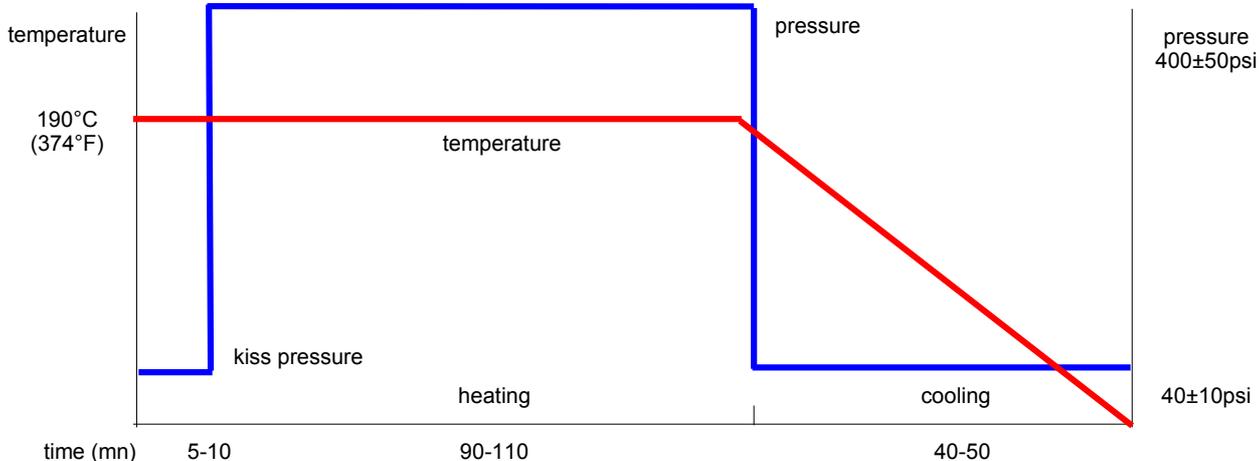
NP180 FA

RECOMMENDED PRESS CYCLE

2 steps



hot press



Suggestions

1. Heating rate of material between 70°C and 140°C
1-3°C/mn is acceptable
1.5-2.5°C/min would be better
2. Temperature of material over 170°C must be held for at least 60 minutes to allow epoxy resin to fully cure
3. The pressure should be kept below 7 bars during cooling to ambient temperature
4. Cooling rate of material should be kept under 2.5°C/mn when the temperature of material is over 100°C in order to avoid introducing twist

Keeping the core and prepreg in the same grain direction is crucial to ensure the flatness of multilayer boards

Grain direction is shown on the certificate of conformance

The material can not be used in horizontal brown oxide process

Material without logo from 0.05 mm to 1.2 mm

Material with logo from 0.8 mm to 3.2 mm



NP180 FA

CERTIFICATION UL – UL FILE N° E98983

INDUSTRIAL LAMINATES

industrial laminates furnished as sheets

ANSI Type	Color	Build up Min Thk (mm)	Flame Class	R.T.I. Elec (C)	R.T.I. Mech (C)	HWI	HAI	H VTR	CTI	Meets 764E DSR
FR4										

ULTRATHIN BUILD UPS

Ultrathin industrial laminates and bonding layers, furnished in sheet form, for use in multilayer printed wiring boards where the thickness is built up to the minimum specified.

Build up				Laminate			Preg		
ANSI Type	Min Thk (mm)	TI Elec	TI Mec	Mtl Dsg	Thk (mic)	TI Elec	Mtl Dsg	Thk (mic)	TI Elec
FR4	0.38	130	130	NP180FR	50	50	NP-180FB	50	50
	0.64		140	NP-180FTL					

METAL CLAD INDUSTRIAL LAMINATES

Metal clad industrial laminates for use in multilayer printed wiring boards with copper on one or both sides, furnished as sheets

Laminates Dsg	Prepreg Dsg	ANSI Type	Build up Min Thk (mm)	Clad Cond Thk			Max Area Diam (mm)	Flame Class	Max Oper Temperature (°C)	Solder Lts	
				Min Ext (mic)	Max Ext (mic)	Max Int (mic)				Temp (°C)	Time (Sec)
NP-180FR NP-180FTL	NP-180FB	FR4	0.38	9	102	210	50.80	V-0	130	300	30

Metal clad industrial laminates for use in single layer printed wiring boards with copper on one or both sides, furnished as sheets.

Laminates Dsg	Prepreg Dsg	ANSI Type	Build up Min Thk (mm)	Clad Cond Thk			Max Area Diam (mm)	Flame Class	Max Oper Temperature (°C)	Solder Lts	
				Min Ext (mic)	Max Ext (mic)	Max Int (mic)				Temp (°C)	Time (Sec)
NP-180FR NP-180FTL	-	FR4	0.38	9	102	-	50.80	V-0	130	300	30

Keeping the core and prepreg in the same grain direction is crucial to ensure the flatness of multilayer boards

Grain direction is shown on the certificate of conformance

The material can not be used in horizontal brown oxide process

Material without logo from 0.05 mm to 1.2 mm

Material with logo from 0.8 mm to 3.2 mm



**High Frequency
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RT/duroid® 5880

Glass Microfiber Reinforced Polytetrafluoroethylene Composite

RT/duroid® 5880 glass microfiber reinforced PTFE composite is designed for exacting stripline and microstrip circuit applications.

Glass reinforcing microfibers are randomly oriented to maximize benefits of fiber reinforcement in the directions most valuable to circuit producers and in the final circuit application.

The dielectric constant of RT/duroid 5880 laminates is uniform from panel to panel and is constant over a wide frequency range. Its low dissipation factor extends the usefulness of RT/duroid 5880 to Ku-band and above.

RT/duroid 5880 laminate is easily cut, sheared and machined to shape. It has excellent dimensional stability and is resistant to all solvents and reagents, hot or cold, normally used in etching printed circuits or in plating edges and holes.

Normally supplied as a laminate with electrodeposited copper of 1/4 to 2 ounces/ ft.² on both sides, RT/duroid 5880 composites can also be clad with rolled copper foil for more critical electrical applications. Cladding with aluminum, copper or brass plate may also be specified.

When ordering RT/duroid 5880 laminates, it is important to specify dielectric thickness, tolerance, rolled or electrodeposited copper foil, and weight of copper foil required.

(See reverse for product data)

RT/duroid 5880 Properties:

PROPERTY	TYPICAL VALUE			DIRECTION	UNITS	CONDITION	TEST METHOD
Dielectric Constant, ϵ_r	2.20			Z	---	C24/23/50	1 MHz IPC-TM-650 2.5.5.3
	2.20 \pm 0.02 spec.			Z		C24/23/50	10 GHz IPC-TM-650 2.5.5.5
Dissipation Factor, $\tan \delta$	0.0004			Z	---	C24/23/50	1 MHz IPC-TM-650 2.5.5.3
	0.0009			Z		C24/23/50	10 GHz IPC-TM-650 2.5.5.5
Volume Resistivity	2 X 10 ⁷			Z	Mohm cm	C93/35/90	ASTM D257
Surface Resistivity	3 X 10 ⁸			Z	Mohm	C93/35/90	ASTM D257
Tensile Modulus	Test at 23 C	Test at 100 C		X Y	MPa (kpsi)	A	ASTM D638
	1070 (156)	450 (65)					
	860 (125)	380 (55)					
ultimate stress	29 (4.2)	20 (2.9)		X Y	MPa (kpsi)	A	ASTM D638
	27 (3.9)	18 (2.6)					
ultimate strain	6.0	7.2		X Y	%	A	ASTM D638
	4.9	5.8					
Compressive Modulus	710 (103)	500 (73)		X Y Z	MPa (kpsi)	A	ASTM D695
	710 (103)	500 (73)					
	940 (136)	670 (97)					
ultimate stress	27(3.9)	22 (3.2)		X Y Z	MPa (kpsi)	A	ASTM D695
		21 (3.1)					
	52 (7.5)	43 (6.3)					
ultimate strain	8.5	8.4		X Y Z	%	A	ASTM D695
	7.7	7.8					
	12.5	17.6					
Deformation Under Load	Test at 150 C 1.0			Z	%	24 hr/14 MPa (2kpsi)	ASTM D621
Water Absorption Thickness = 0.8 mm (0.031) Thickness = 1.6 mm (0.062)	0.9 (0.02)				mg (%)	D24/23	ASTM D570
	13 (0.015)						
Specific Gravity	2.2						ASTM D792
Heat Distortion Temperature	>260 (>500)			X,Y	C (F)	1.82 MPa (264 psi)	ASTM D648
Specific Heat	0.96 (0.23)				J/g/K (BTU/lb/ F)		Calculated
Thermal Conductivity	0.20			Z	W/m/K		ASTM C518
Thermal Expansion	X	Y	Z	<<<	mm/m		ASTM D3386 (10K/min) (Values given are total change from a base temperature of 35 C)
	-6.1	-8.7	-18.7				
	-0.9	-1.8	-6.9				
	-0.5	-0.9	-4.5				
	1.1	1.5	8.7				
	2.3	3.2	28.3				
	3.8	5.5	69.5				

[1] SI unit given first with other frequently used units in parentheses.

[2] References: Internal TR's 1430, 2224, 2854. Test were at 23°C unless otherwise noted. Typical values should not be used for specification limits.

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The above data represents typical values, not statistical minimums. It is not intended to and does not create any warranties, express or implied, including any warranty of merchantability or fitness for a particular purpose. The relative merits of materials for a specific application should be determined by your evaluation.

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