

THERMAL ANALYSIS OF VLSI SYSTEM: A SIMULATION STUDY

By

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16353

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Bachelor of Engineering (Hons)

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CERTIFICATION OF APPROVAL

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A project dissertation submitted to the
Electrical & Electronics Engineering Programme
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in partial fulfilment of the requirement for the
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Approved by,

(Dr. Mohana Sundaram Muthuvalu)

UNIVERSITI TEKNOLOGI PETRONAS
SERI ISKANDAR PERAK

January 2016

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

NIK NUR NAILINI BINTI NIK AB RASHID

ABSTRACT

Smaller size of Very Large Scale Integrated (VLSI) System nowadays increases the on chip power densities causing the rise of temperature in the system. The high temperature produced will eventually affects the clock frequency of the system and changes the timing setup of the component. These lead to lowering the performance and reliability of the system. Due to the negative effects of the high temperature, designers have to determine the thermal profile of the systems in order to understand the temperature distribution, the leakage reduction and estimate the power distribution of the system. This research focuses on analyzing the thermal profile of a VLSI system under steady state condition using numerical techniques and simulation. For the numerical techniques, the governing heat equation for a two-dimensional (2D) model was solved using Finite Difference Method (FDM), Gauss-Seidel (GS) and Successive Over Relaxation (SOR) methods. Simulation based on ANSYS simulator has been conducted for validation purpose. Most commonly material used in VLSI system which is Silicon (Si) is tested under adiabatic condition. The results for numerical techniques and the simulation are compared. SOR method shows better results in terms of number of iterations and the computational time compared to GS method in solving the governing heat equation. Both methods have the same maximum temperature and these temperatures are comparable with the result obtained by using ANSYS.

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ABBREVIATIONS AND NOMENCLATURES

VLSI	Very Large Scale Integrated
IC	Integrated Circuit
MPU	Microprocessor Unit
ITRS	International Technology Roadmap for Semiconductors
Si	Silicon
Ge	Germanium
CMOS	Complementary Metal Oxide Semiconductor
FDM	Finite Difference Method
GS	Gauss Seidel
SOR	Successive Over Relaxation
SSI	Small Scale Integrated
FEM	Finite Element Method
TIM	Thermal Interface Material
PCB	Printed Circuit Board

CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

Nowadays numerous usages of high performance integrated circuits are applied in most of the technologies. Very Large Scale Integrated (VLSI) system is known as the main component in building those advance technologies. VLSI is a system comprises thousands of transistors into a tiny chip which is known as Integrated Circuit (IC). Due to the smaller size and continuous scaling of Complementary Metal Oxide Semiconductor (CMOS) technology, performance and reliability has become two main factors that need attention in the design process of the VLSI systems [1]. Figure 1.1 shows the design development process of the VLSI system.

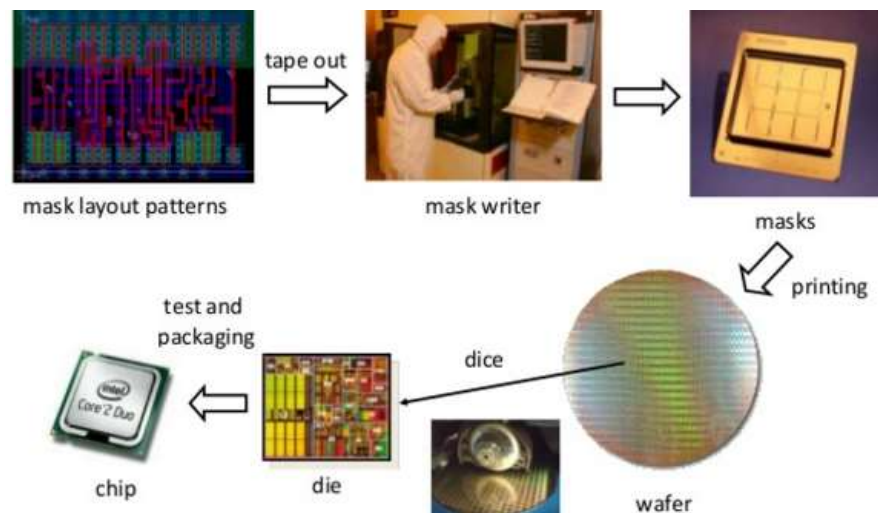


Figure 1.1: Design development of VLSI system

Temperature is one of the main issues related to the VLSI systems. The high temperature produced by this system decreases the performance, the speed and the lifespan of the system from time to time [2, 3, 4]. Therefore, it is important to obtain the thermal profile of the system to maintain its functionality.

Determining the thermal profile for the system is considered as the most challenging part for most designers as VLSI circuits are getting more complex. In old days, the thermal profile of the system is obtained by using many sensors on the chip. The readings were then compared to the reference voltage called ‘overheating level’ [5]. However today, there are lots of ways to obtain the thermal profile and it depends on methods that are used to get better results.

1.2 PROBLEM STATEMENT

Continuous scaling process in VLSI system increases the temperature and causes overheating which usually results in slower device and reduce in performance. Generally, heat is produced during the operation of the VLSI system and the high temperature produced on an IC chip complicates the timing and reduces the reliability of the system [6]. Therefore, accurate thermal profiling is important to simulate the timing in the circuit and ensures the reliability of the system [7].

Table 1.1 shows the characteristics of the highest power and metal layers number for next generation high-performance microprocessor unit (MPU) from year 1999 to 2014 based on the 1999 International Technology Roadmap for Semiconductors (ITRS) which has been the reason for the high temperature in VLSI circuits [8].

Table 1.1 Characteristics of highest power and metal layers number for next generation high-performance microprocessor unit (MPU)

Year	1999	2000	2001	2002	2003	2004	2005	2008	2011	2014
Maximum Power (W)	90	100	115	130	140	150	160	170	174	183
Clock (MHz)	1200	1321	1454	1600	1724	1857	2000	2500	3004	3600
Wiring Levels	7	7	7	8	8	8	9	9	10	10

Based on the analysis discussed in [2], it shows that the increase in the temperature of the system is due to the increment in interconnect delays. Chen *et al.* [7] mentioned that because the electrical resistivity of metal increases linearly with temperature, the interconnect delay eventually causes the temperature of the system to increase. Heat is commonly produced by the current flow within interconnect and has the relationship with root mean square (rms) current density and also the temperature resistivity of the metal thus making these two factors to be the cause of internal heat generation of the VLSI system.

There are various factors that causes heat generation in circuit. Therefore, thermal profile is needed to understand the behaviour of the system. Besides, it will also help the designers to figure out ways to improve the performance of the system using more efficient methods [1].

1.3 OBJECTIVES

1. To observe the thermal profile by implementing the numerical techniques in solving the governing differential equation.
2. To obtain the thermal profile of VLSI model using ANSYS simulator.
3. To analyze and compare the performance of the numerical results and simulation.

1.4 SCOPE OF STUDY

Numerical technique is applied in order to get the thermal profile of the VLSI system and is simulated using ANSYS software to validate the results. The Finite Difference Method (FDM) is used to discretize the governing heat equation based on law of conservation of energy and is then solved using two stationary iterative methods namely Gauss-Seidel (GS) and the Successive Over Relaxation (SOR).

Material properties used in this project is Silicon (Si) which is most commonly used in building VLSI circuits. Si is usually in the form of wafer with different number of dies in it. Figure 1.2 shows the structure of a silicon wafer and a close up of a silicon die.

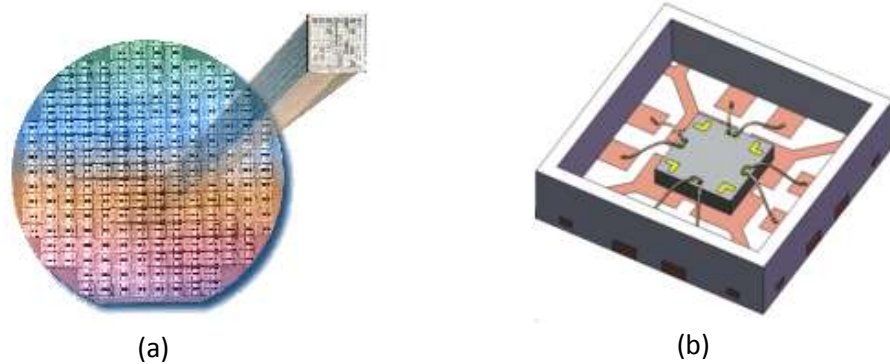


Figure 1.2 (a) Silicon wafer (b) Silicon die

Based on the size of the die, often one node at the top is set as the inward and one node at the bottom is set as the outward direction boundaries of the chip which allows the transfer of heat in and out of the VLSI system. The boundary condition at the tiny surface of the silicon is set to adiabatic meaning there is no heat transfer within the nodes and surroundings. Whereas the top and bottom boundaries are defined based on the surface of the VLSI system where heat is transferred through the soldered part causing the heat to flow vertically through the system. Also, the system is tested assuming that it is under steady state condition where there will be no switching within devices in the system.

CHAPTER 2

LITERATURE REVIEW

2.1 BACKGROUND

Back in the early 60's, instead of VLSI consisting billions of transistors in a chip, there was a time when only few bipolar transistors and resistors were fabricated into one IC known as Small Scale Integrated (SSI) system. In comparison, VLSI is simpler but more complex than SSI mainly because of the increasing number of the transistors and also the improvised functionality in VLSI [9]. Figure 2.1 shows the timeline from SSI to VLSI [10, 11].

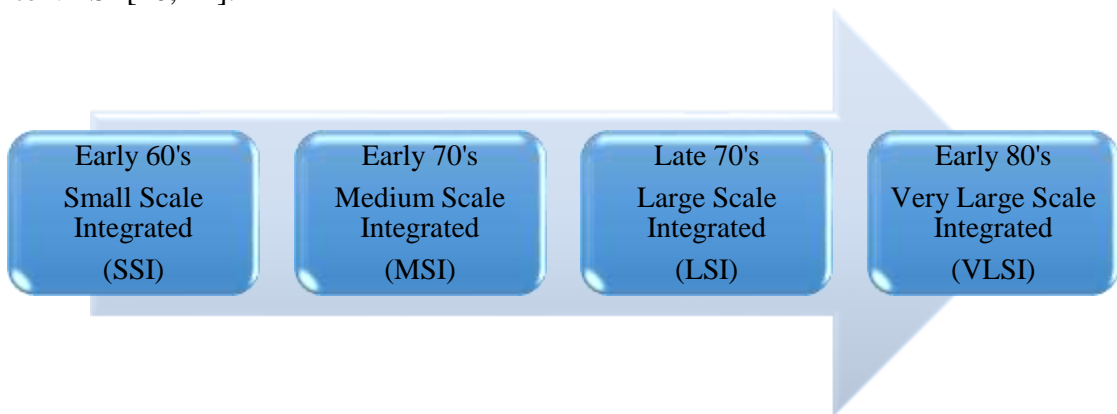


Figure 2.1 Scaling development of SSI to VLSI

The first bipolar transistors was invented in 1947 by Bell Labs, while the first IC made of Germanium (Ge) was invented by Jack Kilby from Texas Instrument Company in 1958. Later, Robert Noyce from Fairchild Semiconductor came up with the IC made of silicon that is use until now [12]. Figure 2.2 shows the first IC which is made of Germanium and later one which is made of Silicon. Silicon is chosen to be the most suitable material as it has wider bandgap compared to germanium which allows it to operate in high temperature. Besides, it is also inexpensive and well known as abundant element in nature.

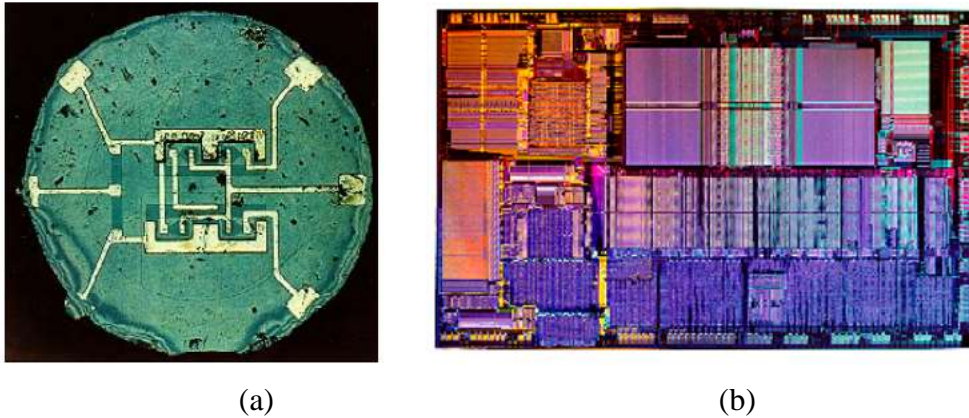


Figure 2.2 (a) IC made of Germanium (b) IC made of Silicon

2.1.1 Thermal Analysis

Pedram and Nazarian [13], mentioned that half of the IC failures are due to the thermal issues. They also described the importance of determining the thermal profile of the VLSI system before it is implement in the IC packages. Figure 2.3 shows the typical structure of IC package consisting all main components of IC. Thermal considerations are important because high temperature can cause problems such as changing the transistor and interconnect delay, other than increases the power densities and leakage which affects the reliability of the system. The chip might also burn out if the temperature keeps on changing because of the sensitivity of leakage power [14]. Basically, leakage power consumption depends on temperature. The higher the temperature, the higher the power of dissipation [13].

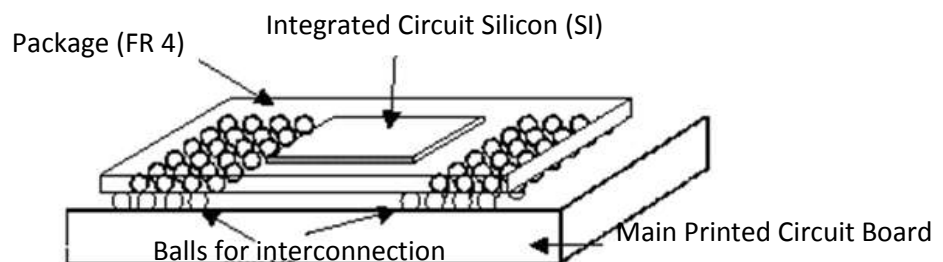


Figure 2.3 Typical structure of IC

Heat can transfer via three ways called radiation, conduction and convection. The conduction and radiation method can be implemented with complete passive heat transfer system but convection uses the active method that needs design overhead [13].

Heat dissipation whether at the circuit, package or on the board is governed by the heat differential equation as in (1) [13, 8, 15].

$$\rho C_{\rho} \frac{dT(\vec{r},t)}{dt} = \nabla \cdot (k(\vec{r},T) \nabla T(\vec{r},T)) + g(\vec{r},T) \quad (1)$$

subjected to general thermal boundary condition known as Robin's boundary condition which is as follows

$$k(\vec{r},T) \frac{dT(\vec{r},t)}{dn_i} + h_i T(\vec{r},T) = f_i(\vec{r},T) \quad (2)$$

Based on equation (1), T , ρ , C_{ρ} , k , and g represent temperature, density of material, mass heat capacity, thermal conductivity and heat energy generation. In equation (2), n_i is the outward direction normal to boundary condition, i . Meanwhile, h_i and $f_i(\vec{r},T)$ represents the coefficient of heat transfer and arbitrary function on the boundary surface [8, 15].

2.2 NUMERICAL TECHNIQUES

To achieve accurate temperature profile, a die is simulated along with its thermal mounts which require solving of the differential equation. Common numerical methods for full chip thermal analysis are Finite Difference Method (FDM) and Finite Element Method (FEM).

FDM is usually represented by truncating the Taylor series of expansion or balancing the equations. In [16], it is proved that FDM can be done by both difference equation and energy balancing. FDM is usually designed in the form of one or two dimensional along the Cartesian plane and there are two approaches to solve it which are by using the spherical type and geometrics type [16].

The structure of FDM scheme is usually in form of meshed rectangular cuboidal where the temperature region is assumed to be at the center of the cuboid [14]. FDM is used mainly to change the continuous derivatives with difference formula which consists of only discrete values that interconnects with the positions on the mesh [17]. This method is more stable than by using FEM due to the position of the mesh and its uniform grid. In fact, FEM consumes a lot of time and is not advisable for the design and run time of thermal analysis [1].

In order to solve the linear system equation obtained from the FDM, iterative method is used. Gauss Seidel (GS), Jacobi and Relaxation Methods are examples of iterative methods often used to solve any linear systems. Iterative methods construct series of solution approximation and improve the linear system solution involving large sparse system. However, it is not always applicable as there are criteria called the convergence criteria that need to be achieved before applying the concepts. Nevertheless, they are still ideal for FDM which involves solution of numerous sparse matrices.

2.3 SIMULATION

Thermal simulation is important in most of the design engineering application. There are few simulators that can perform this analysis but the often used are ANSYS and SOLIDWORKS simulator.

ANSYS is one of the software that can perform thermal analysis simulation. The result of the heat balanced equation obtained by the principle of conservation of energy is the source in performing the analysis. ANSYS will compute the nodal temperature based on the solution that has been done using the numerical methods [18].

The thermal analysis for ANSYS is able to handle the three important types of heat transfer which are convection, conduction and radiation. This project focused mainly on the heat conduction process. Therefore, the simulation will be done by designing and running a simple model based on the heat conduction process. In fact, ANSYS is also able to perform the steady state thermal analysis as well as the transient state thermal analysis.

Solidworks simulator can be used to determine the thermal analysis as well. For the thermal analysis, Solidworks is divided into three types of thermal analysis modules based on the level capability. They are Linear Static-Thermal Stress, Simulation Professional- Thermal Analysis and Thermal Analysis in Flow Simulation [19]. Also, this software is able to perform either steady state or transient temperature fields by initializing temperature, heat power input and output and also the thermal contact resistance within the components.

Both ANSYS and Solidworks do not require high cost prototype. Besides, these software helps to save time without redoing and delaying whatever issues related to thermal structural analysis [20].

2.4 APPLICATION

Using many sensors on the chip for thermal profiling has always been as a traditional way of determining the thermal profile of the VLSI systems. In fact, there are many ways to get the accurate performance and reliability analysis for the thermal profiling of the VLSI chips that have been published in the literatures. However, to get the accurate thermal profiles for large area of VLSI chips is not an easy task [21]. Therefore, by discretizing the governing heat equation (1), the temperature profiles can be obtained for the large area chip area at particular time, provided that the parameter values are given.

CHAPTER 3

METHODOLOGY

3.1 RESEARCH METHODOLOGY

Figure below shows the methodology flow for this project.

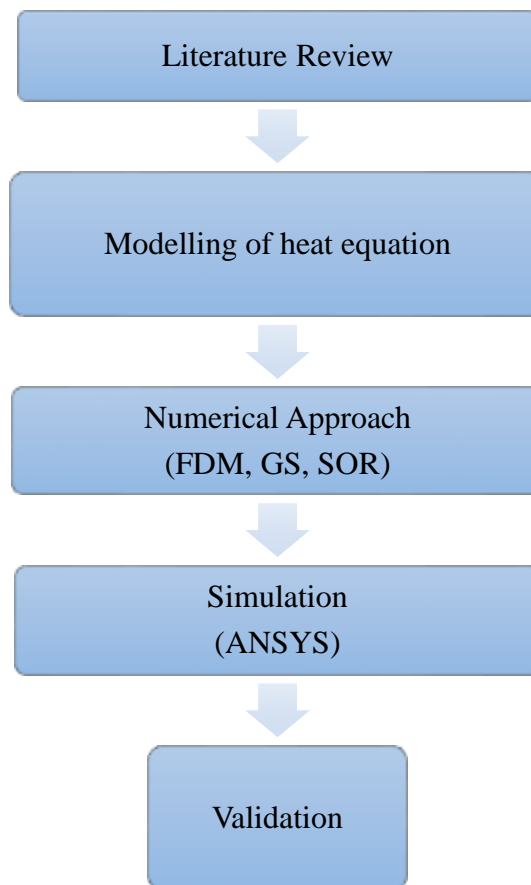


Figure 3.1 Methodology flow

3.2 MODELLING HEAT EQUATION

A typical VLSI model consists of basic components such as heat sink, heat spreader, Silicon bulk, the Thermal Interface Material (TIM) and Printed Circuit Board (PCB). Figure 3.2 (a) and (b) shows the two representation of packaged IC chip with basic components [22].

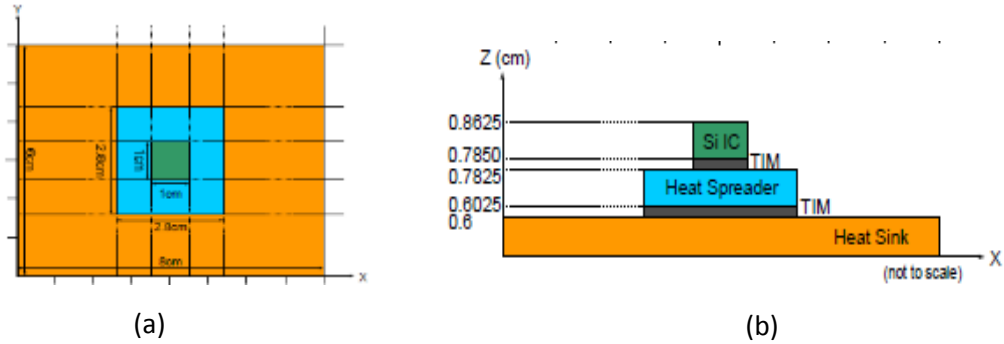


Figure 3.2 (a) 2D layout of packaged IC chip (b) packaged chip including heat spreader and TIM

In equation (1), the parameter thermal conductivity, $k(\vec{r}, T)$ is dependent on the position and temperature of the chip and the heat generation rate, g is induced by current flow or power consumption that were specified as body load. Power consumption in gates happened to be due to short circuit and leakage current in the circuit. However, power in ground or clock interconnects are basically due to self-generating which is expressed as $J_{ms}^2 \times R_\rho$. J_{ms}^2 is the current density of material and R_ρ is the temperature resistivity of material [7].

Setting the substrate temperature as zero allows the super positioning of solutions caused by the various current sources whereby the values for interconnect temperature should be added to the real substrate temperature later. For computational purpose, the two-dimensional (2D) model which is assumed in adiabatic boundary condition is used throughout this project. Also, the model is set to work under steady state condition whereby no time consideration will be taken into account.

3.3 NUMERICAL APPROACH

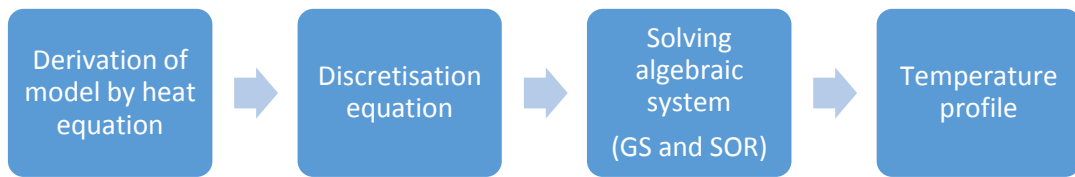


Figure 3.3 Numerical technique process

FDM is used in order to obtain an algebraic system. The main idea of this method is to change continuous derivatives with difference formula involving only discrete values with the positions on the mesh. FDM consists three ways to discretise the Partial Differential Equation (PDE) known as forward, backward and centered finite difference method. Among these three methods, the centered finite difference is usually the most accurate method as the centered difference would quarter the truncation error. Figure 3.4 shows the mesh on the x - y plane with T representing the temperature at each node [8].

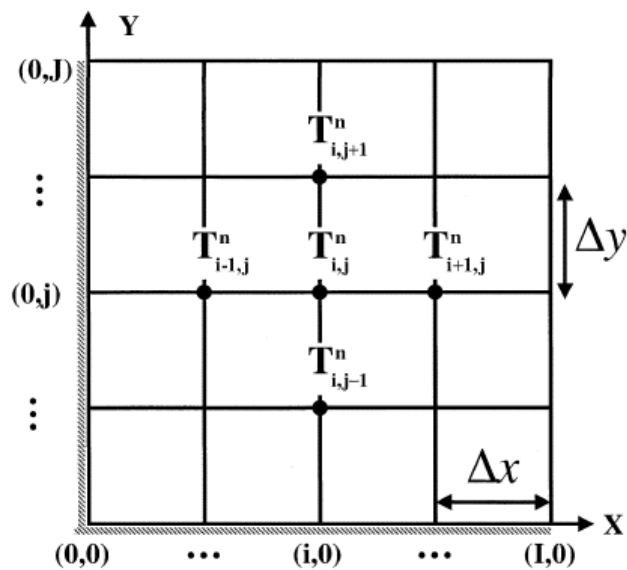


Figure 3.4 Meshes on the x - y plane where n is replaced with k throughout the calculation process

The first step using the numerical technique is to discretise equation (1) by using implicit FDM. The left and right sides of the equation (1) is replaced with backward and centered finite difference, respectively. The following equations represent the formula of the backward and centered finite difference

$$\frac{dT(x, y, t)}{dt} = \frac{T_{i,j}^{k+1} - T_{i,j}^k}{\Delta t}, \quad (3)$$

$$\frac{d^2T(x, y, t)}{dx^2} = \frac{T_{i+1,j}^{k+1} - 2T_{i,j}^{k+1} + T_{i-1,j}^{k+1}}{(\Delta x)^2} \quad (4)$$

and

$$\frac{d^2T(x, y, t)}{dy^2} = \frac{T_{i,j+1}^{k+1} - 2T_{i,j}^{k+1} + T_{i,j-1}^{k+1}}{(\Delta y)^2}. \quad (5)$$

By substituting all the equations from (3) to (5) into equation (1) the governing equation will be reduces to

$$\frac{T_{i,j}^{k+1} - T_{i,j}^k}{\Delta t} = \frac{k}{\rho C \rho} \left(\frac{T_{i+1,j}^{k+1} - 2T_{i,j}^{k+1} + T_{i-1,j}^{k+1}}{(\Delta x)^2} + \frac{T_{i,j+1}^{k+1} - 2T_{i,j}^{k+1} + T_{i,j-1}^{k+1}}{(\Delta y)^2} \right) + \frac{g(x, y, t)}{\rho C \rho}. \quad (6)$$

Now, let $(\Delta x)^2$ and $(\Delta y)^2$ as h^2 , the equation (6) can be rewrite as

$$\alpha T_{i,j}^{k+1} = T_{i,j}^k + \lambda (T_{i+1,j}^{k+1} + T_{i-1,j}^{k+1} + T_{i,j+1}^{k+1} + T_{i,j-1}^{k+1}) + \frac{\Delta t g_{i,j}^k}{\rho C \rho} \quad (7)$$

where $\alpha = 1 + \frac{4\Delta t k}{\rho C \rho h^2}$ and $\lambda = \frac{\Delta t k}{\rho C \rho h^2}$.

Generally, equation (7) can be represented in matrix form as

$$AT = b \quad (8)$$

Then, the resulting algebraic system is solved by using the GS and SOR methods. This method consists of two main characteristics, which are the serial form of computation and also the sequence of the new value in the equations that is examined. GS general formula in terms of matrices can be formed as in (9) which then can be expanded to form SOR general equation as in (10) [23]

$$T^{(k+1)} = (D - L)^{-1}(UT^{(k)} + b) \quad (9)$$

and

$$T^{(k+1)} = T^{(k)} + \omega(D - L)^{-1}(UT^{(k)} + b) \quad (10)$$

where D , $-L$, and $-U$ represent the diagonal, strictly lower triangular and strictly upper triangular parts of A , while ω in equation (10) indicates the acceleration parameter ($0 < \omega < 2$). When $\omega = 1$, the equation (10) will represent the GS method.

3.4 SIMULATION

For the comparison analysis, the model of the problem is designed by using ANSYS software. The parameter values are set and run under respective module. The model is assumed to be under steady state condition and also adiabatic. The simulation result obtained is then compared with the numerical techniques for validation.

CHAPTER 4

RESULTS AND DISCUSSION

All simulations are done using personal computer Intel (R) Pentium (R) CPU N3540 @ 2.16GHz, 2.16GHz and 4.00GB RAM. Simulation for the numerical technique is run using MATLAB R2013 and the maximum temperature (T_{\max}) in Kelvin (K), number of iterations (k) and computational time (t) in seconds were recorded. The simulation is done using different grid sizes which are 16×16 , 32×32 , 64×64 , 128×128 and 256×256 . The values of the parameters are based on the property of Silicon which is basically the material used in most VLSI systems. The 2D model length, L is set to 4.75m. Under adiabatic condition, the boundary condition is assigned to zero and initial temperature, T_{in} of the system is set under room temperature as $T_{in} = 293.15K$. Table 4.1 below shows the properties of silicon that has been used in this project.

Table 4.1: Properties of Silicon

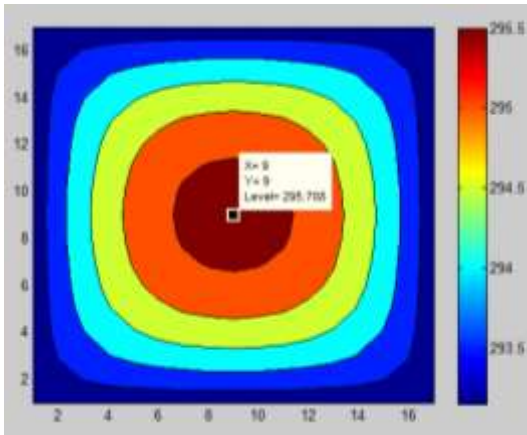
Material Properties (Silicon)	
Thermal Conductivity, $k(w/mK)$	149
Thermal Density, $\rho(kg/m^3)$	2330
Specific Heat Capacity, $C_p(j/kgK)$	703

4.1 NUMERICAL RESULTS

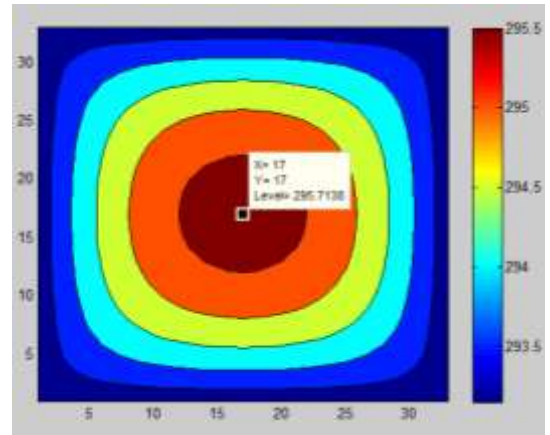
Table 4.2 shows the numerical results under steady state condition and is obtained using MATLAB R2013. Meanwhile, Figure 4.1 to 4.3 show the temperature profiles.

Table 4.2: Numerical results based on steady state condition

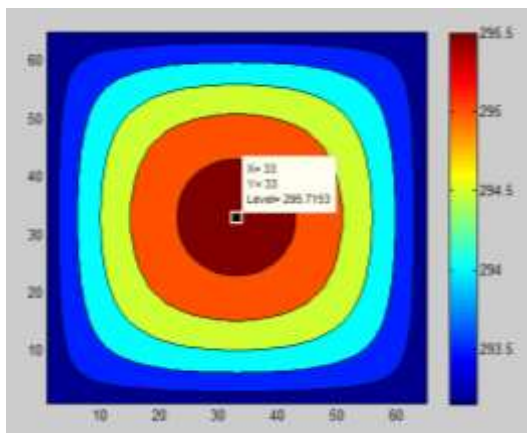
Size	Method	k	t	T_{\max}
16×16	GS	353	0.313	295.7080
	SOR ($\omega = 1.7$)	45	0.156	295.7080
	<i>pdepe</i>	-	-	295.6730
32×32	GS	1266	2.047	295.7138
	SOR ($\omega = 1.8$)	114	0.658	295.7138
	<i>pdepe</i>	-	-	295.6950
64×64	GS	4481	23.605	295.7153
	SOR ($\omega = 1.9$)	184	3.755	295.7153
	<i>pdepe</i>	-	-	295.7030
128×128	GS	15598	298.482	295.7155
	SOR ($\omega = 1.9$)	792	50.902	295.7155
	<i>pdepe</i>	-	-	295.7060
256×256	GS	53138	4893.471	295.7148
	SOR ($\omega = 1.9$)	2776	708.511	295.7148
	<i>pdepe</i>	-	-	295.7060



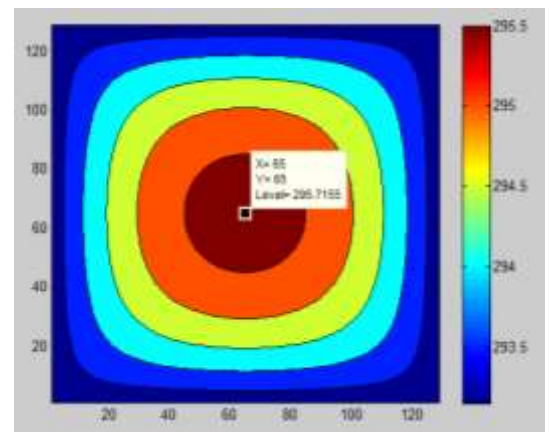
a) Mesh size 16x16



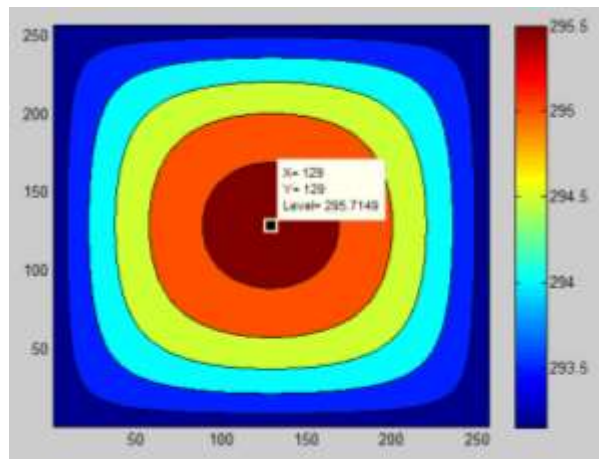
b) Mesh size 32x32



c) Mesh size 64x64

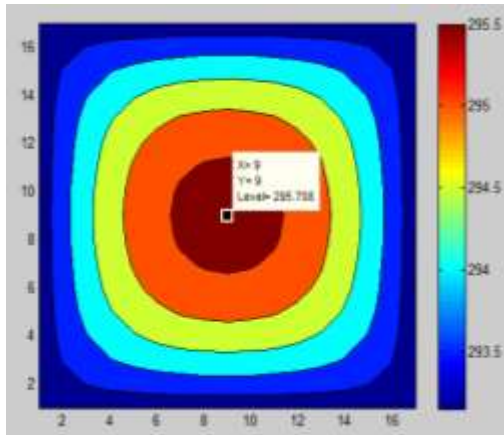


d) Mesh size 128x128

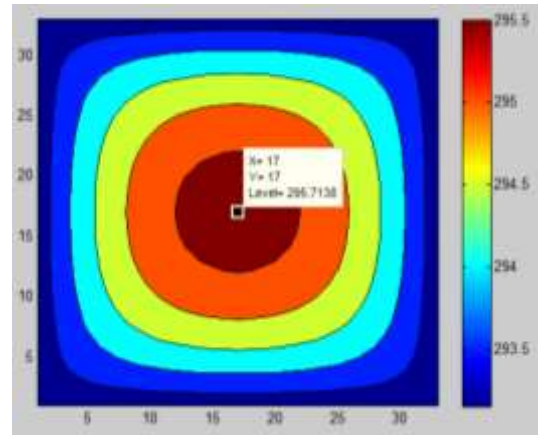


e) Mesh size 256x256

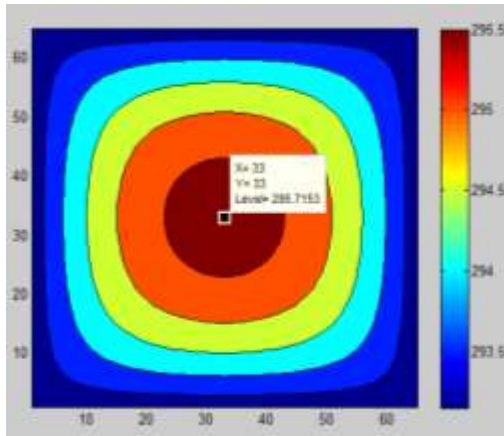
Figure 4.1 Temperature profile based on GS method



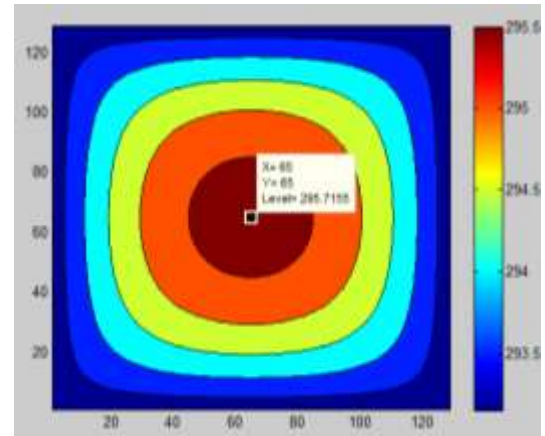
a) Mesh size 16x16



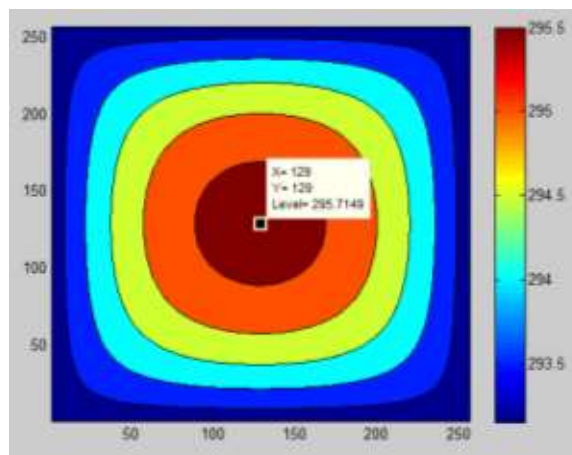
b) Mesh size 32x32



c) Mesh size 64x64

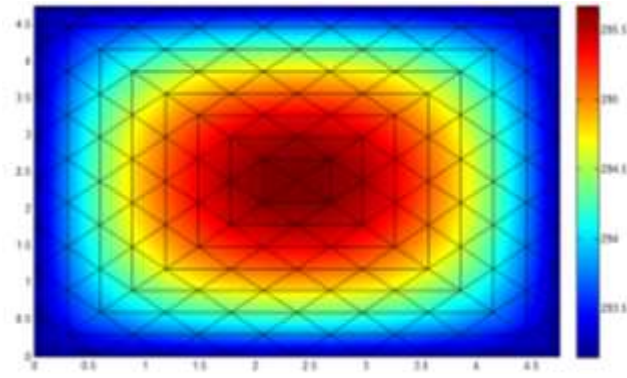


d) Mesh size 128x128

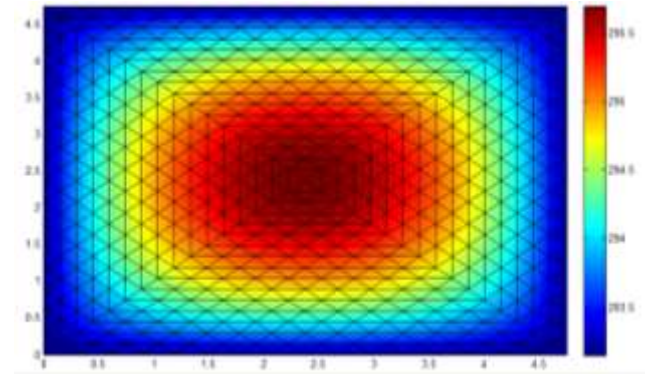


e) Mesh size 256x256

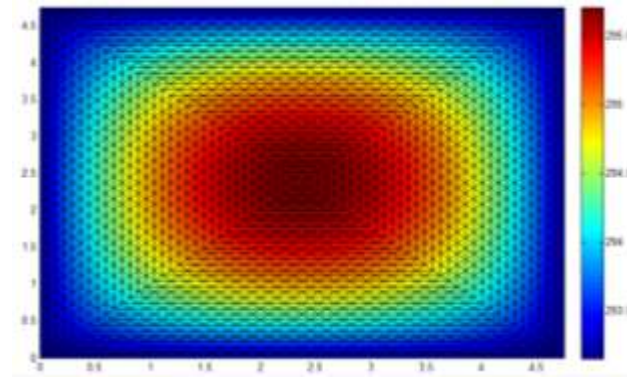
Figure 4.2 Temperature profile based on SOR method



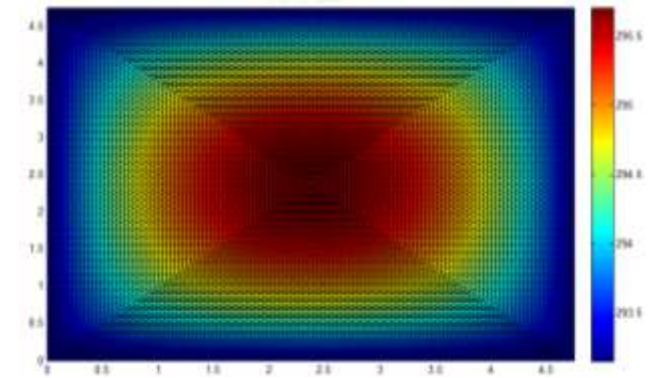
a) Mesh size 16x16



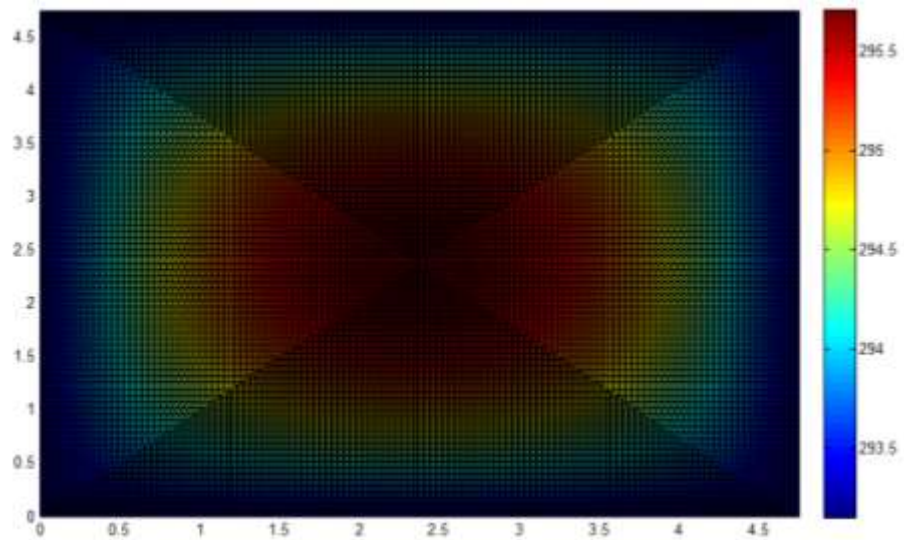
b) Mesh size 32x32



c) Mesh size 64x64



d) Mesh size 128x128



e) Mesh size 256x256

Figure 4.3 Temperature profile based on *pdepe* method

Results in Table 4.2 shows that SOR method reduces the number of iteration from 87.25% to 94.78% and also reduce the computational time from 50% to 85.52% compared to GS method. However the maximum temperature obtained by using GS, SOR and *pdepe* methods are comparable. Overall, the larger the mesh size, the higher the maximum temperature, number of iteration and computational time for each method.

4.2 SIMULATION RESULTS (ANSYS)

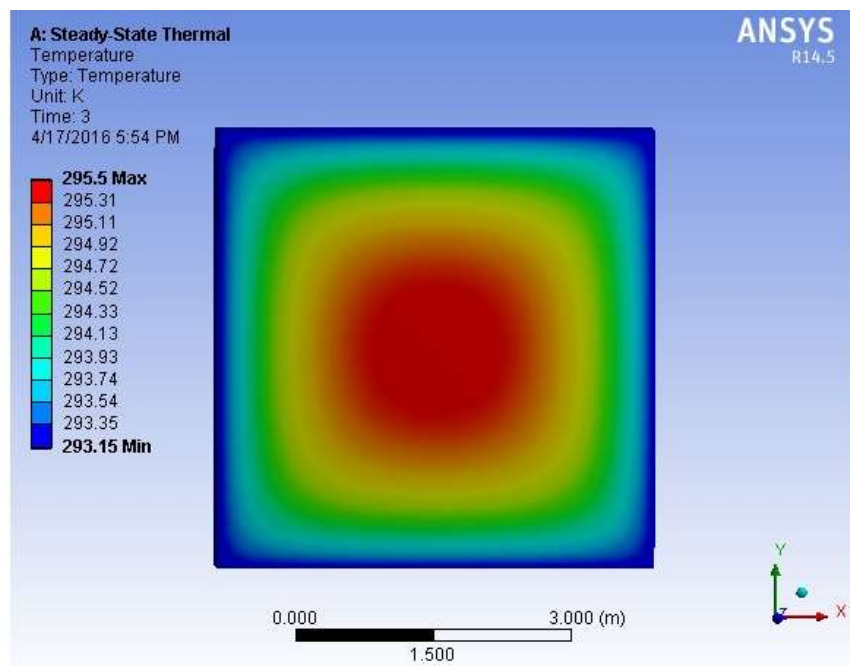


Figure 4.4 shows the temperature profile of a 2D model using the ANSYS software.

The condition for the model is set to a steady state thermal to synchronize with the results obtain using MATLAB R2013. The maximum temperature of the model is 295.5K which is slightly lower compared to the numerical results. However, the temperature is still comparable to the results in Table 4.2. The maximum temperature trend for the model appears to be the same with the results for numerical methods which is at the centre of the model. Based on both numerical and ANSYS results, it can be conclude that the maximum temperature increases around 8% from the initial temperature.

CHAPTER 5

CONCLUSION AND RECOMMENDATION

In conclusion, thermal profile of VLSI system can be obtained by discretizing the governing heat equation and solve using numerical techniques. An implementation of SOR method is able to reduce the number of iteration and computational time compared to GS method. Also, by using the properties of Si in the ANSYS simulator, the thermal profile for a 2D model is almost similar as the MATLAB R2013 results. Also, the results of maximum temperature obtained based on numerical and simulation techniques are comparable.

As for recommendations, the study can be extended into performing thermal analysis on a three-dimensional model. Besides that, considering the problem in an unsteady state condition also can be performed. The thermal profiling of the VLSI system also can be done using the parallel computing besides using different kinds of numerical technique such as Arithmetic Means (AM) [24] or Conjugate Gradient (CG) [25]. For more advanced study, developing monitoring tool or system also shall be able to perform based on the thermal profiling obtained.

REFERENCES

- [1] W. Huang, S. Ghosh, S. Velusamy, K. Sankaranarayanan, K. Skadron and M. R. Stan, "HotSpot: A compact thermal modeling methodology for early-stage VLSI design," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 14, (5), pp. 501-513, 2006.
- [2] K. Banerjee, M. Pedram, and A. H. Ajami, "Analysis and optimization of thermal issues in high-performance VLSI," in *Proceedings of the 2001 International Symposium on Physical Design*, 2001, pp. 230-237.
- [3] T. Kemper, Y. Zhang, Z. Bian, A. Shakouri, "Ultrafast temperature profile calculation in Ic chips" in *Dans Proceedings of 12th International Workshop on Thermal investigations of ICs*, 2006.
- [4] P. Y. Huang and Y. M. Lee, "Full-Chip thermal analysis for the early design stage via generalized integral transforms," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 17, (5), pp. 613-626, 2009.
- [5] A. Lakhssassi and M. Bougataya, "VLSI thermal analysis and monitoring," in *VLSI*, Rijeka: InTech, 2010, pp. 441-456.
- [6] H. Wang, "Compact modeling and analysis for electronic and thermal effects of nanometer integrated and packaged systems," PhD dissertation, Dept. Electrical Engineering, University of California, Riverside, 2012.
- [7] D. Chen, E. Li, E. Rosenbaum and S. M. Kang, "Interconnect thermal modeling for accurate simulation of circuit timing and reliability," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 19, (2), pp. 197-205, 2000.
- [8] T. Y. Wang and C. C. P. Chen, "Thermal-ADI: A linear-time chip-level dynamic thermal simulation algorithm based on alternating-direction-implicit (ADI) method," in *Proceedings of the 2001 International Symposium on Physical Design*, 2003, pp. 691-700.
- [9] Mary Bellis. (n.d.). *The History of the Integrated Circuit aka Microchip*. Aboutmoney [Online]. Available: http://inventors.about.com/od/istartinventions/a/intergrated_circuit.htm
- [10] N.Weste and Harris, D. (2004). Introduction to CMOS VLSI Design. Available: <http://web.ewu.edu/groups/technology/Claudio/ee430/Lectures/L1-print.pdf>

- [11] C. H. Roth and L. K. John, *Digital System Design using VHDL*, 2nd ed., Austin: CL Engineering, 2007.
- [12] J. D. Plummer, M. Deal, P. B. Griffin and P. D. Griffin, *Silicon VLSI Technology, Fundamentals, Practice and Modeling*, 2nd ed., New Jersey: Prentice Hall, 2000.
- [13] M. Pedram and S. Nazarian, "Thermal modeling, analysis, and management in VLSI circuits: Principles and methods," *Proceedings of the IEEE*, vol. 94, (8), pp. 1487-1501, 2006.
- [14] Y. Zhan, B. Goplen and S. S. Sapatnekar, "Electrothermal analysis and optimization techniques for nanoscale integrated circuits," in *Asia and South Pacific Conference on Design Automation*, 2006, pp. 1-4.
- [15] H. Wang, D. Li, S. X. D. Tan, M. Tirumala and A. X. Gupta, "Composable thermal modeling and characterization for fast temperature estimation," in *19th Topical Meeting on Electrical Performance of Electronic Packaging and Systems*, 2010, pp. 185-188.
- [16] B. A. Welt, A. A. Teixeira, K. V. Chau, M. O. Balaban and D. E. Hintenlang, "Explicit Finite Difference Methods for Heat Transfer Simulation and Thermal Process Design," *Journal of Food Science*, vol. 62, pp. 230–236, 1997.
- [17] Gerald W. Recktenwald. (2011). Finite-Difference Approximations to the Heat Equations. Available: <http://www.nada.kth.se/~jjalap/numme/FDheat.pdf>
- [18] *Thermal Analysis Guide*, SAS IP Inc, 2009. Available: http://orange.engr.ucdavis.edu/Documentation12.0/120/ans_the.pdf
- [19] Paul M. Kurowski. (2015). *Thermal Analysis with SOLIDWORKS Simulation 2015 and Flow Simulation 2015*, SDC Publications. Available: <http://files.solidworks.com/partners/pdfs/2015thermal.pdf>
- [20] *Thermal Structural Analysis*, DS Dassault Systemes, 2016. Available: <http://www.solidworks.com/sw/products/simulation/thermal-structural-analysis.htm>
- [21] K. Fukutani, S.M. Kang, J. H. Park, A. Shakouri and Y. Zhang, "Three-dimensional electro-thermal modeling of thin film micro- refrigerators for site-specific cooling of VLSI ICs," in *IMAPS 39th International Symposium on Microelectronics*, 2006, pp. 883-890.
- [22] J. H. Park, V. M. Heriz, A. Shakouri and S. M. Kang, "Ultra fast calculation of temperature profiles of VLSI ICs in thermal packages considering parameter variations," in *IMAPS 40th Int. Symp. Microelectronics*, 2007.
- [23] Black, Noel, Moore and Shirley. (2016). Gauss-Seidel Method, Wolfram Research Inc. Available: <http://mathworld.wolfram.com/Gauss-SeidelMethod.html>

- [24] M. S. Muthuvalu, V. S. Asirvadam and G. Mashadov, "Performance analysis of Arithmetic Mean method in determining peak junction temperature of semiconductor device," *Ain Shams Engineering Journal*, vol. 6, (4), pp. 1203-1210, 2015.
- [25] D. N. Hío, N. T. Thính and H. Sahli, "Splitting-based conjugate gradient method for a multi-dimensional linear inverse heat conduction problem," *Journal of Computational and Applied Mathematics*, vol. 232, (2), pp. 361-377, 2009.