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SWITCHING CONTROL MODEL FOR A FIVE-LEVEL H-BRIDGE/NEUTRAL POINT CLAMPED (H-NPC) INVERTER USING SINUSOIDAL PULSE WIDTH MODULATION (SPWM) TECHNIQUES

by

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# SWITCHING CONTROL MODEL FOR A FIVE-LEVEL H-BRIDGE/NEUTRAL POINT CLAMPED (H-NPC) INVERTER USING SINUSOIDAL PULSE WIDTH MODULATION (SPWM) TECHNIQUES

by

ISMAILA MAHMUD

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BANDAR SERI ISKANDAR,

PERAK

JUNE 2013

DECLARATION OF THESIS

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|---|---|
| Title of thesis | Switching Control Model for a Five-level H-bridge/Neutral Point Clamped (H-NPC) Inverter using Sinusoidal Pulse Width Modulation (SPWM) Techniques |

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hereby declare that the thesis is based on my original work except for quotations and citations which have been duly acknowledged. I also declare that it has not been previously or concurrently submitted for any other degree at UTP or other institutions.

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## DEDICATION

This thesis is dedicated to my lovely wife, Fatima Musa and son, Mahmud Ismail Mahmud for their love and support during my study.

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## ABSTRACT

High power demand give rise to emergence of multilevel inverters in large electric drives and utility application. The structure of multilevel inverters has the ability to reduce harmonics and improve power rating performance. The development of a good switching control is necessary for the operation of the multilevel inverter.

This thesis is aimed to provide a clear understanding with simulation proofs on the modulation scheme of five-level H-bridge / neutral point clamped (H-NPC) inverter. In the modulation scheme design, several sinusoidal pulse width modulations (SPWM) such as Alternate Phase Opposition Disposition (APOD), Phase Opposition Disposition (POD) and Phase Disposition (PD) were investigated, and verified by the existing In-Phase Disposition (IPD) done on five-level H-NPC inverter. Various aspects of switching technique on the five-level H-NPC inverter such as harmonic suppression, total harmonic distortion reduction, high voltage level attainment and effect in change of the modulation index were discussed. The simulation and research findings are provided in detail. Overall, the IPD has the best performance in term of high voltage attainment at low modulation index of 0.6 and harmonic suppression of having a $33^{rd}$ harmonic order as the lowest harmonic component.

PD has the best results in terms of Total Harmonic Distortion (THD) reduction with 17 % THD for the line-line voltage waveform at 0.9 amplitude modulation index. IPD and APOD have 28.60 % and 29 % respectively. POD has the highest with 30 % THD. A similar trend of decrease in the total harmonic distortion as the amplitude modulation index has been increased was observed in all the four SPWM techniques.

## ABSTRAK

Permintaan kuasa elektrik yang tinggi menimbulkan kemunculan penyongsang pelbagai peringkat dalam pemacu elektrik yang besar dan juga untuk aplikasi utiliti. Struktur penyongsang pelbagai peringkat mempunyai keupayaan untuk mengurangkan kesan harmonik dan juga meningkatkan prestasi penarafan kuasa. Pembangunan kawalan pertukaran yang baik adalah penting bagi operasi penyongsangan pelbagai peringkat ini.

Tujuan tesis ini adalah untuk memberikan kefahaman yang jelas, disertakan juga dengan bukti-bukti simulasi daripada skim modulasi H-jambatan lima peringkat / penyongsangan titik neutral diapit (H-NPC). Dalam skim modulasi reka bentuk, beberapa bacaan kelebaran dan ketinggian sinusoidal (SPWM) seperti alternatif fasa penyusunan pembangkang (APOD), fasa penyusunan pembangkang (POD), dan penyusunan fasa (PD) turut dikaji, dan telah disahkan oleh pelupusan yang sedia ada di dalam fasa yang telah dilakukan oleh H-NPC penyongsang lima peringkat. Pelbagai aspek daripada teknik beralih kepada H-NPC penyongsang lima peringkat seperti penindasan harmonik, jumlah pengurangan herotan harmonik, pencapaian tahap voltan tinggi dan juga kesan dalam perubahan indeks pemodulatan juga dibincangkan. Simulasi dan juga hasil peyelidikan juga disertakan dengan secara terperinci. Secara keseluruhannya, IPD memberikan prestasi yang terbaik dalam pencapaian voltan tinggi pada indeks pemodulatan rendah iaitu 0.6 manakala penggagalan harmonik terendah didapati pada turutan harmonik yang ke-33.

PD memberikan hasil yang ter baik dari segi jumlah keherotan harmonik (THD) dengan pengurangan sebanyak 17 % untuk gelombang voltan garis ke garis pada 0.9 amplitud. IPD dan APOD masing-masing memberikan peratusan sebanyak 28.60 % dan 29 % bagi jumlah keherotan harmonik (THD). Manakala, POD memberikan peratusan yang tertinggi antara semua dengan bacaan 30% THD. Trend penurunan

peratusan yang selaras didapati dalam jumlah keherotan harmonik (THD), sebaliknya indeks modulasi amplitude didapati meningkat dalam kesemua empat teknik SPWM.

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# NOMENCLATURE

| | |
|---|---|
| $A_c$ | Amplitude (peak value) of the carrier wave |
| $A_m$ | Amplitude (peak value) of the modulating wave |
| C | Capacitance of a capacitor |
| CMI | Cascaded H-bridge Multilevel Inverter |
| $f$ | frequency of the modulating wave |
| $f_c$ | frequency of the carrier wave |
| FC | Flying Capacitor Inverter |
| H-NPC | H-bridge / neutral point clamped Inverter |
| $m_a$ | Amplitude modulation index |
| $m_f$ | frequency modulation index |
| NPC | Neutral Point Clamped Inverter |
| PWM | Pulse Width Modulation |
| S | Switch |
| SHE | Selective Harmonics Elimination |
| SPWM | Sinusoidal Pulse Width Modulation |
| SVM | Space Vector Modulation |
| $V_{an}$ | phase output voltage |
| $V_{ab}$ | Line-line output voltage |
| $V_{ao}$ | phase output voltage with respect to negative dc rail |
| $V_{dc}$ | dc voltage |
| $V_{ref}$ | sinusoidal reference signal / modulating signal. |

# CHAPTER 1

# INTRODUCTION

The main purpose of this chapter is to introduce the work produced in this thesis about pulse width modulation on a five-level H-bridge Neutral Point Clamped (H-NPC) inverter. It synthesizes the main topics of the research which are elaborated in their designated chapters; such as the research background, motivation, objectives, and contributions. It concludes with an overview of the content of the thesis outline section.

## 1.1 Motivation

Many modulation techniques have been used to control the switching elements of a multilevel inverter such that a low harmonic content of the output waveform is produced. Among the techniques are; Sinusoidal Pulse Width Modulation (SPWM), Space Vector Modulation (SVM), and Selective Harmonic Elimination - Pulse Width Modulation (SHE-PWM) etc.

Among the most outstanding modulation scheme used in the switching of the inverter is the SPWM, where the gate signals of the inverter switches are generated from the comparison between sinusoidal modulating waveform and triangular carrier waveform [1]. Utilization of multi-triangular carrier in SPWM results in distortion reduction in multilevel inverters. The methods could be in the form of carrier disposition or phase-shifting of the carrier [2]-[3]. The carrier disposition is to arrange the carrier waveforms in a vertical disposition and define based on the relationship between the carriers. Alternative Phase Opposition Disposition (APOD), Phase Opposition Disposition (POD), and Phase Disposition (PD) are classified under vertical disposition. Phase-shifting (PS) SPWM technique is referred to as the horizontal arrangement. Flying capacitors and cascaded H-bridges perform very well

with PS-SPWM while neutral point clamped inverter perform better with PD-SPWM [4]-[9].

Space Vector Modulation (SVM) provides another method to control the switching of multilevel inverters. It uses the inverter's system control variable to control its switching. It identifies a switching pattern vector and presents it in a complex space (d, q). The major drawback of SVM method is the complication in sector identification and look-up table requirement to establish the switching intervals for all vectors. As the number of levels increases, redundant switching states and difficulty in selecting switching states increase significantly [4]-[5], [9]-[10].

The main feature in SHE-PWM is that, it chooses arbitrary harmonics (low order mostly) to eliminate through computing the appropriate switching angles of the inverter that will results in the elimination. Less commutation per cycle is one of the advantages of SHE-PWM which enable it to operate in air-cooling with high efficiency. In a variable speed operation, SHE-PWM has the disadvantage of computation of the switching angles being based on Fourier theorem which makes the harmonics to be partially eliminated. And could be amplified through closed-loop controller which will affect the overall performance and limited its usage to low dynamics performance drive applications [4]-[5], [11]-[12]. The SPWM technique involves the simple comparison of modulating signal and carrier signal to control the switching devices which endures it to be the most used modulation technique in the industries.

Research is growing in the part of voltage source inverter where newer topologies are discovered through the hybrid of the existing ones and so many developments had been achieved in that aspect of combining existing topology [4]-[5]. Some of the latest topologies that are ready found in practice are; Cascaded Matrix Converter (CMC), H–bridge/ Neutral Point Clamped (HNPC), Active Neutral Point Clamped (ANPC) and the Modular Multilevel Converter (MMC). Other topologies that are still under development are as follows; the transistor – clamped converter (TCC), the CHB fed with unequal DC source or asymmetric CHB, the cascaded NPC feeding open – end loads, the hybrid NPC – CHB and hybrid FC – CHB topologies and the stacked FC or stacked multi-cell etc [5].

The motivation of using the five-level H-NPC inverter is that a higher value of voltage could be produced and by controlling the modulation index, the speed of the motor could as well be control. Wu (2006) *et. al* [13], Shohel (2007) *et. al* [14] and Wanjekeche (2011) *et. al* [15] used In-Phase disposition (IPD) to achieved the output voltage of H-NPC inverter. Other SPWM techniques such as APOD, POD and PD have perform superbly in many topologies and could as well perform better in H-NPC inverter. So an important question arises to which among the SPWM technique could perform better and motivated us to carry out the research.

## 1.2 Background

The need to control torque and speed in motor is paramount. The use of modern Variable Speed Drive (VSD) ensures that speed of the driven machine is maintained within ± 0.1 %, independent of load against the 3 % from no load to full load speed variation for the speed regulation of a classical fixed speed induction motor [16]-[18]. With the control of speed and torque, the drive can control the variables of process, such as flow by controlling the speed of a pump. When conventional mechanical methods such as inlet dampers, throttling control and flow-control valves are used to drive fans or pump with a fixed-speed motor, they control the air or liquid flow which result to significant amount of energy loss [19].

Initially DC drives and motors were used because speed and torque could be controlled without the need for sophisticated electronics. However, high maintenance requirement of DC motor have led to a decrease in their popularity [16]. This also led to the emergence of AC drives, as AC motors are inexpensive and required little maintenance. The performance of AC drive is as good as DC drives. The use of AC drives like 5-level H-NPC will ensure that the environment is not polluted with high electromagnetic radiation, reduction in $CO_2$ emission and energy cost is also reduced. AC drives are categorized into direct and indirect topologies as shown in Figure 1.1. The direct topology connects the source directly to the load through semiconductor switches and appropriate control system. Cycloconverter and matrix inverter falls in the direct topology category, thus the former is the most used topology among the two

in high-power application while the latter reaching only up to 150 kVA makes it not to be in high-power ranges [19]. Cycloconverter with its excellent dynamic performance has the short limitation of non-constant power factor over range of speeds, large footprint compared to standard drive and limitation on the maximum output frequency [16].

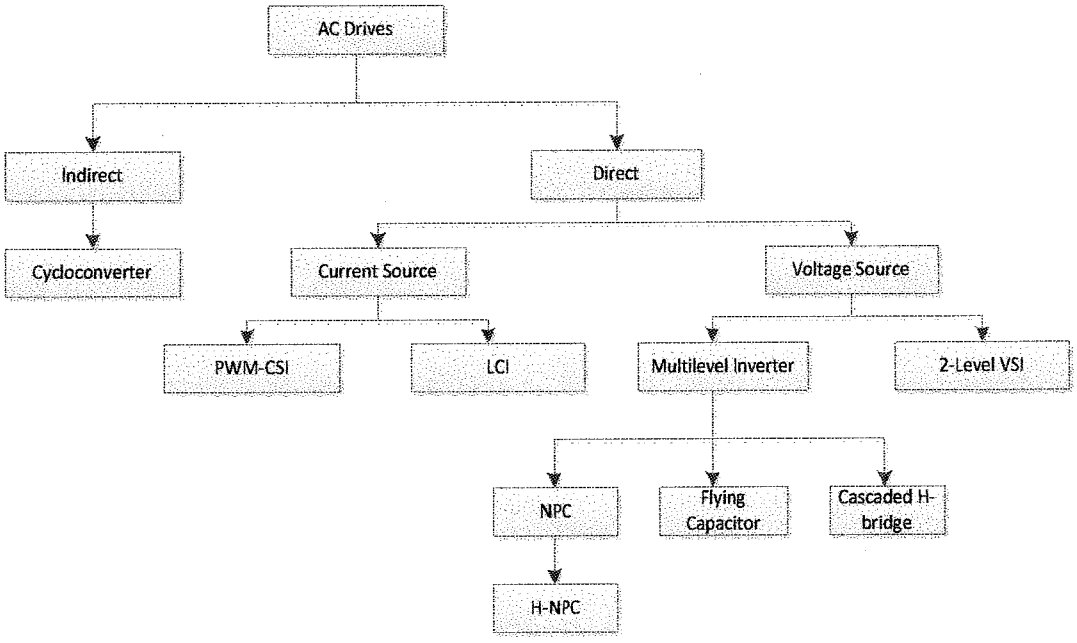



Figure 1.1: Classifications of AC Drives

The indirect topology has an energy-storage element (capacitor or inductor) in between rectification and inversion for the power transfer. It is classified into current-source (inductor as the energy-storage element) and voltage-source (capacitor as the energy-storage element) depending on the DC-link energy-storage element. Two current-source inverters have found industrial presence: Load-Commutated Inverter (LCI) and the Pulse Width Modulation – Current Source Inverter (PWM-CSI). The LCI had decades of operation as a simple converter topology but have the disadvantage of distorted input-current waveform and low-input power factor [19]. Voltage-source inverters have experienced much market penetration with the classical two-level inverter dominating the lower voltage market. Multilevel inverter topologies with their DC – link source and extra switches, are arranged in such a way to produce different output voltage levels in the form of a stepped waveform with less common-mode voltage, harmonic distortion and a reduction in the rate of change of voltage

[20].These characteristics provided them to be among the high-power medium voltage applications. The popular multilevel voltage-source inverters are; the Cascaded H-bridge (CHB) [21], Neutral Point Clamped (NPC) [22] and Flying Capacitor (FC) [23].

The three-level NPC inverter has wide acceptance due to its simple transformer rectifier circuit structure, with less number of capacitor and low device count [5]. Though higher number of levels could be achieved by extending the NPC structure, these are less attractive due to unbalance voltage of the DC-link capacitors and uneven distribution of losses in the inner and outer devices. H-bridge / Neutral Point Clamped (H-NPC) inverter retain the structure of NPC inverter in H-bridge form which allows it to generate five-level output voltage waveform and solves the problem of neutral balancing associated with higher number of levels in NPC. This thesis mainly looks at the sinusoidal pulse width modulation techniques on H-NPC using total harmonic distortion as the performance index.

### 1.3 Scope

The study is based on the investigation of four different SPWM techniques which make the hardware implementation costly for all the techniques to be implemented. Therefore, the scope of this thesis is limited to the simulation model of the four SPWM techniques; In-Phase disposition (IPD), Alternative Phase Opposition Disposition (APOD), Phase Opposition Disposition (POD), and Phase Disposition (PD).

### 1.4 Objectives

SPWM uses high frequency switching property of semiconductor devices to achieve the desired output. The modulation will be carried out by comparing the magnitude of the two signals (carrier and modulating). Amplitude modulation index can used to control the fundamental-frequency component $f$ in the inverter output voltage [13], [24] as given by Equation (1.1):

$$m = \frac{A_m}{A_c} \tag{1.1}$$

where $A_m$ and $A_c$ are the peak values of the modulating and carrier waves.

Based on this basic knowledge, following objectives are drawn in order to accomplish the project:

a) To design the simulation models for SPWM techniques that would be applied to five-level H-NPC inverter.
b) To simulate the performance of the inverter's output voltage.

## 1.5 Contribution of the Thesis

The main contribution of this thesis is the analytical investigation of Sinusoidal Pulse Width Modulation (SPWM) techniques applied to the five-level H-bridge / Neutral Point Clamped (H-NPC) inverter. A comprehensive comparison of the SPWM techniques based on the following performance indexes; voltage attainment, harmonic suppression and total harmonic distortion reduction was done. MATLAB / Simulink simulations were carried out and the results show that both techniques could be used in modulating the Five-level H-NPC inverter. The IPD-SPWM shows superiority in terms of harmonic suppression ($33^{rd}$ harmonic order being the least harmonic component) and voltage attainment (attaining both five levels and nine levels for the phase and line voltage respectively at 0.6 amplitude modulation index), while APOD that is close to it has $11^{th}$ harmonic order as the least harmonic component and attain five levels and nine levels for the phase and line voltage respectively at 0.7 amplitude modulation index. PD has the best performance in terms of total harmonic distortion reduction with 17 % for line-line voltage, whereas nearest to it is IPD with 28.60 %.

## 1.6 Thesis Organization

The complete organization of the study takes the form of seven chapters, including this opening chapter. Chapter 2 starts by setting out the theoretical aspects of the research, by looking at the conventional multilevel inverter topologies like flying capacitor, neutral point clamped and cascaded H-bridge inverter. Their operations, features, advantages and disadvantages were discussed. It also provides detailed review on the classical modulation techniques; Space Vector Modulation (SVM), Sinusoidal Pulse Width Modulation (SPWM) and Selective Harmonic Elimination – Pulse Width Modulation (SHE-PWM).

Chapter 3 describes the system operation and features of the five-level H-NPC inverter and related work were presented. The design detail of simulation model to the SPWM techniques; In-Phase Disposition (IPD), Alternate Phase Opposition Disposition (APOD), Phase Opposition Disposition (POD) and Phase Disposition (PD) were given. In chapter 4, comprehensive discussion on the results is provided for IPD, APOD, POD and PD. The performance of the modulation schemes at different amplitude and frequency modulation indices are also evaluated.

The last chapter presents the summary that shows the analytical investigation of SPWM techniques on five-level H-NPC inverter where its performance index are compared and a conclusion of this dissertation along with some recommendations for future work.

# CHAPTER 2

# LITERATURE REVIEW ON MULTILEVEL INVERTERS AND MODULATION SCHEMES

In this chapter an overview discussion on multilevel inverter topologies such as Flying Capacitor (FC) inverter, Neutral Point Clamped (NPC) inverter and Cascaded H-bridge Multilevel Inverter (CMI) and the conventional modulation techniques; sinusoidal pulse width modulation (SPWM), space vector modulation (SVM), selective harmonic elimination – pulse width modulation (SHE-PWM) and hysteresis current control are being presented.

## 2.1 Multilevel Inverter

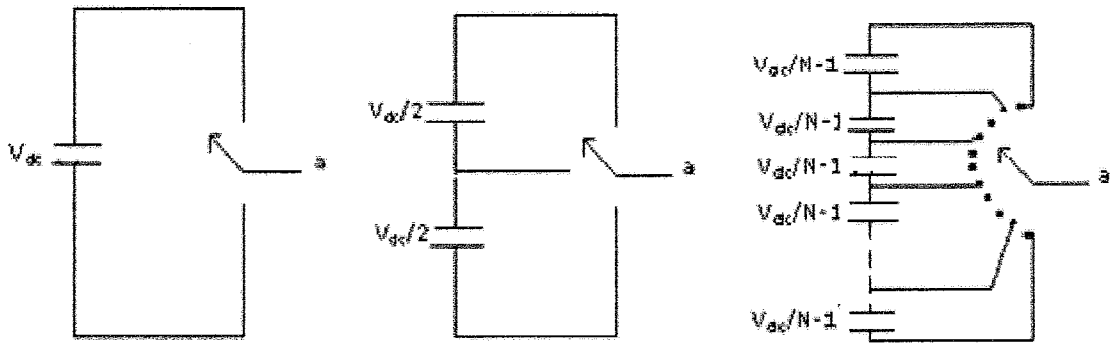
The two-level inverter as shown in Figure 2.1(a) produces output voltage of either zero or $\pm V_{dc}$. Operating at a high switching frequency along with PWM technique enabling it to produce a voltage or current output waveform that has appreciable harmonic contents. Semiconductor device rating constraints and switching losses make two-level inverter less acceptable in high power and high voltage applications. The topologies of multilevel inverter as shown in Figure 2.1(b) and (c) make it easy to attain higher voltage and power without much stress on the switching devices [25].

A multilevel inverter includes an array of power semiconductor switches and capacitor voltage sources as shown in Figure 2.1(b) and (c). A higher output is obtained from the addition of the capacitor voltage through the commutation of the switches as depicted in Figure 2.1(c) [20]. The series-connected capacitors form the input source of the inverter which also provide some nodes that the inverter can be connected to [25].

The voltage $V_c$ across each capacitor is the same and is given by Equation (2.1):

$$V_c = \frac{V_{dc}}{N-1} \tag{2.1}$$

where, N donates the number of the levels.

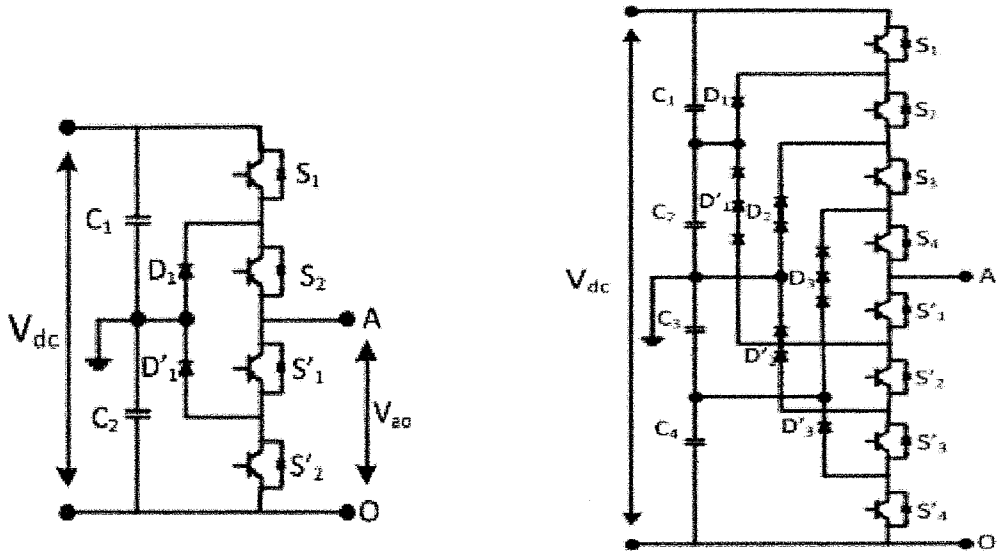



(a) Two-level (b) Three-level (c) N-level

Figure 2.1: Multilevel Inverter structures

### 2.1.1 Neutral Point Clamped (NPC) Inverter

Neutral point clamped inverter also called diode clamped inverter is one of the most used multilevel inverter topology, the major difference between the two-level inverter and the NPC inverter is the diode used in clamping the DC bus voltage in order to attain steps in the output voltage. The NPC inverter was proposed in 1981 by Nabae, Takahashi, and Akagi [22]. It consists of two pairs of switches ($S_1$, $S'_1$ and $S_2$, $S'_2$) and two clamping diodes $D_1$ and $D'_1$ as shown in Figure 2.2(a). The diodes enable the inverter to have access to the neutral point. As to avoid short-circuiting the system, each switch pair works in complimentary mode. The inverter produces three voltage levels in each phase, where a common DC bus is shared. Two capacitors $C_1$ and $C_2$ connected across the DC bus split it into three levels. In a three-level inverter, a set of two switches is on at any given time. Figure 2.2 shows the circuit for a neutral point clamp inverter for a three-level and five-level.




(a) Three-level (b) Five-level

Figure 2.2: Diode Clamped Inverter

Each capacitor has a voltage of $\boldsymbol{V_{dc}/(N-1)}$ at steady state for an N-level inverter. The quality of the output voltage waveform improve with an increase in the number of voltage levels and come close to a sinusoidal waveform [26]. However, capacitor voltage balancing will be of serious concern in high level inverters. The system becomes practically impossible to implement as the number of switching device and diode increase with an increase in the voltage level. Using PWM to switch the inverter brings the challenge to control the reverse recovery of the clamping diode in the design [20]. The operation of NPC inverter is straight forward even with its complex structure compare to two-level inverter.

*2.1.1.1 Operation of NPC Inverter*

Three-level neutral-point clamped inverter has its dc bus divided by two capacitors $C_1$ and $C_2$ as shown in Figure 2.2(a). The voltage across each capacitor will be $V_{dc}/2$ when the DC bus voltage is $V_{dc}$. The voltage stress that each device will be subjected is $V_{dc}/2$ of the capacitor voltage.Voltage staircase waveform of NPC inverter is synthesized through certain switch combination to produce a three-level voltage across point 'A' and 'O', $V_{ao}$:

a) Switching switch $S_1$ and $S_2$ ON, $V_{ao}$ is$V_{dc}/2$.

b) Switching switch $S_2$ and $S_1$' ON, $V_{ao}$ is 0.

c) Switching switch $S_1$' and $S_2$' ON, $V_{ao}$ is $-V_{dc}/2$.

In practical implementation, the complementary switches need some dead time incorporated in between their switching signals, implying a time transition delay between turning ON and OFF of the switches in the complementary pair to avoid the short circuiting the DC bus voltage of the inverter.

*2.1.1.2 Features of NPC Inverter*

(a) *Blocking diode voltage requirement* - The active switching devices are only needed to block a voltage level of $V_{dc}/(N-1)$ each in case of N-level inverter but the clamping diodes need to have different voltage ratings for reverse voltage blocking. In Figure 2.2(b), $D_1'$ (in the 5-level diode clamped inverter) has to block three capacitor voltages or $3V_{dc}/4$ when all lower devices, $S_1'$-$S_4'$ are turned on. Similarly, $D_2$ and $D_2'$ have to block $2V_{dc}/4$, and $D_3$ has to block $3V_{dc}/4$. The number of diodes required for each phase will be $(N-1)x(N-2)$ when the voltage rating of each blocking diode are assume to be equal to the voltage rating of active device. The expression shows that N is increased quadratically. When N is sufficiently high, the system becomes impractical to implement due to the number of diodes required [27]-[28]

(b) *Unequal device rating* - In Figure-2.2(b), switch $S_1$ conducts once when $V_{ao} = V_{dc}$ whereas switch $S_4$ conducts almost for the complete cycle apart from when $V_{ao} = 0$. The result of this uneven conduction duty is having various current ratings for the switching devices. When an average duty is used for all devices in the inverter design, there may be oversized and undersized in the outer switches and inner switches respectively. If the design is to match the critical case, then $2(N-2)$ oversized outer devices will in each phase.

*2.1.1.3 Advantages and Disadvantages of NPC Inverter*

The advantages are enunciated as follows;

a) The capacitance requirement of the converter is minimizes as all the phases share a common DC bus. This ensures that the inverter could be practically use in a back-to-back topology such as in an adjustable speed drive or high-voltage back-to-back inter-connection.
b) Efficiency of the fundamental frequency switching is high.
c) Possibility of pre-charging the capacitors as a group.
d) High number of levels give low harmonic content such that filter could be avoided

The disadvantages are given as follows;

a) In a single inverter, if a precise monitoring and control is not done on the intermediate DC level, real power flow will be difficult.
b) In a higher number of levels, the requirement number of clamping diodes is quadratic compared to the number of levels [27], which makes it to become cumbersome.

The diode-clamped inverter is among the most used multilevel inverter that has been use in providing multiple voltage levels through series connection of capacitors. Increasing the number of capacitors enable the inverter to be extended to any number of level. The three-level topology is the most popular descriptions of this topology where one additional level is introduce as a result of connecting the DC bus to two capacitors. The neutral point of the DC bus result in the additional level, thus this lead to the term neutral point clamped (NPC) inverter to be used. However, the neutral point is not accessible for an even number of voltage levels, and in this case Multiple Point Clamped (MPC) is used instead. The issue of balancing capacitor voltage limits the implementation of diode-clamped inverter to three-level. The maturity of the three-level inverter in industrial developments over the past several years, make it be used extensively in industrial application [28].

### 2.1.2 Flying Capacitors Inverter

Flying capacitor inverter also known as capacitor clamped inverter proposed in 1992 by Maynard and Foch [23]. Its structure is similar to that of the diode-clamped inverter with capacitor in the place of clamping diodes. Flying capacitor implores a ladder series connection of DC side capacitors clamping the switching devices in each leg. The magnitude of the steps in the output voltage waveform is as result of the increment between voltage of the two adjacent capacitor legs [29]. Figure 2.3 shows single-phase five-level Flying Capacitor (FC) inverters.

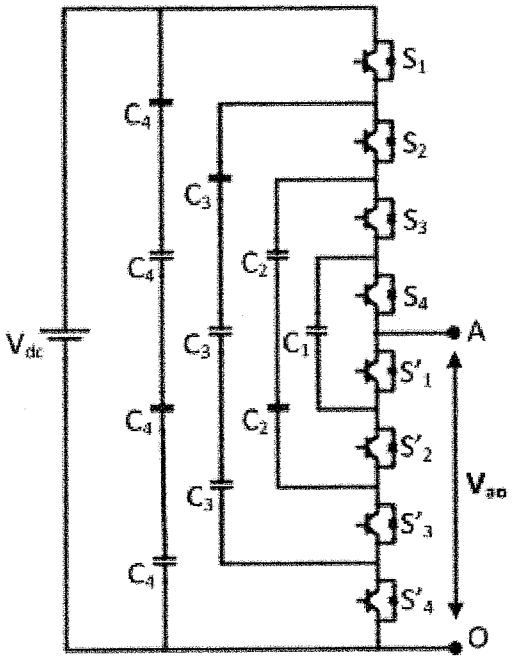



Figure 2.3:Five-level Flying Capacitor

#### *2.1.2.1 Operation of Flying Capacitors Inverter*

In the operation of five-level flying capacitor inverter, the DC bus is divided into five level over four DC capacitors which is shared by each of the three phase leg of the inverter as shown in Figure 2.3. The auxiliary (clamping) capacitors ($C_1$, $C_2$ and $C_3$) need to be pre-charge to $V_{dc}/4$, $V_{dc}/2$, $3V_{dc}/4$ voltage respectively. This enables the inverter to effectively generate multilevel voltage waveforms. The structure of each phase-leg is identical.

Enormous number of large capacitors is required similar to the clamping diode in NPC inverter for voltage clamping. In each phase, $(N-1)(N-2)/2$ clamping capacitors are required for an N-level inverter in addition to the *(N-1)* main DC bus capacitors provided that the same voltage rating used for each capacitor is the same as that of the main power switch.

Flying-capacitor inverter does not require all its switches to conduct in a consecutive series and with some redundancies in the phase, unlike the diode-clamped inverter that has redundancies only in line-line [27], [30]. These redundancies give the control system ability to balance voltages across various levels and the choice to charging/discharging specific capacitors.

The synthesis of voltage in a five-level flying capacitor inverter is more flexible than in neutral point clamped inverter. Using Figure 2.3, the phase output voltage of the five-level with respect to the negative DC rail, $V_{aro}$, can be obtained by the following switch combinations [20], [27].

a) For voltage level $V_{ao} = V_{dc}$, turn on all upper switches $S_1$, $S_2$, $S_3$ and $S_4$.

b) For voltage level $V_{ao} = 3V_{dc}/4$, has four combinations:
   a) $S_1, S_2, S_3, S'_4$
   b) $S_2, S_3, S_4, S'_1$
   c) $S_1, S_3, S_4, S'_2$
   d) $S_1, S_2, S_4, S'_3$.

c) For voltage level $V_{ao} = V_{dc}/2$, has six combinations:
   a) $S_1, S_2, S'_3, S'_4$
   b) $S_3, S_4, S'_1, S'_2$
   c) $S_1, S_4, S'_2, S'_3$
   d) $S_1, S_3, S'_4, S'_2$
   e) $S_2, S_4, S'_1, S'_3$
   f) $S_2, S_3, S'_1, S'_4$

d) For voltage level $V_{ao} = V_{dc}/4$, has four combinations:
   a) $S_1, S'_2, S'_3, S'_4$
   b) $S_4, S'_1, S'_2, S'_3$
   c) $S_3, S'_1, S'_2, S'_4$
   d) $S_2, S'_1, S'_3, S'_4$

e) For voltage level $V_{ao} = 0$, all lower switches are turn on; $S'_1$, $S'_2$, $S'_3$ and $S'_4$.

### *2.1.2.2 Features of Flying Capacitors Inverter*

The large number of storage capacitors required for this inverter is its major problem. In each phase, $(N-1)(N-2)/2$ clamping capacitors are required for an N-level inverter excluding the $(N-1)$ main DC bus capacitors as long as the same voltage value is being used for every capacitor is similar to that of the main power switch [20].

Two or more switch combinations of the middle voltage levels (i.e.,$3V_{dc}/4$, $V_{dc}/2$, $V_{dc}/4$) may be employ in order to balance the capacitor charge and discharge in one or several fundamental cycles. Real power conversions using flying capacitor multilevel inverter can be achieved by proper selection of switch combinations. However, the selection of a switch combination becomes very complex, when it involves real power conversions and the need to have the fundamental frequency less than the switching frequency [27].

### *2.1.2.3 Advantages and Disadvantages of Flying Capacitors Inverter*

The advantages are enunciated as follows;

a) No need for additional clamping diodes.
b) The flying capacitors can be balance using the switching redundancy within the phase, so a single DC source is required.
c) Due to the non-use of transformer to attain the required number of voltage levels, the cost of the inverter and power loss are reduced.
d) In the phase leg of flying capacitor inverter, the capacitors are being charged to separate voltage levels unlike the neutral point clamped topology where the series chain of capacitors share the similar voltage,.
e) It can control real and reactive power flow.

The disadvantages are given as follows;

a) The need for the capacitors to be set up with an initial charge as the required voltage level, before the inverter could be worth use in any modulation technique. This makes the modulation process to be very complex and becomes an obstacle to the smooth operation of the inverter.
b) The control for tracking the voltage levels for all of the capacitors is complicated.
c) Complexity in pre-charging all of the capacitors to a similar voltage level and startup.
d) The design of capacitors rating is challenging due the large portions of the DC bus voltage across them.
e) Poor switching operation and efficiency when use in real power transmission.
f) The capacitors are expensive and bulky compared to clamping diode in NPC inverter.
g) The inverter with higher number of levels has packaging difficulties.

### 2.1.3 Cascaded Multilevel Inverter

Another alternative for a multilevel inverter topology with less switching elements constraint compared to the earlier stated topologies is the series H-bridge inverter or cascaded H-bridge multilevel inverter (CMI). The cascaded H-bridge inverter structure is based on the series connection of H-bridges with separates DC sources as shown in Figure 2.4. The DC sources have to be isolated from each other due the series connection of the output terminals of the H-bridges. Owing to this property, CMI have been used in renewable energy like photovoltaic arrays or fuel cells in order to achieve higher levels. Three-phase transformer with isolated secondary windings could be used for diode rectifiers to produce the DC sources. With its modularity and flexibility, the CMI shows superiority in high-power applications, especially shunt and series connected FACTS controllers. The output of CMI is synthesized to nearly a sinusoidal voltage waveform by the combination of many isolated voltage levels. The phase of the inverter is made of series connection of single-phase full bridges. The three-phase CMI structure consists of three

indistinguishable phase legs of the series connection of H-bridge inverters, which produce different waveforms of output voltage and has the possibility of having balance-phase AC system. This feature could not be found in other voltage-source inverter structure having a common DC source. Easy to scale the voltage and power level since the topology consists of series power conversion cells.

### *2.1.3.1 Operation of Cascaded Multilevel Inverter*

The phase voltage of the CMI is form from adding the voltages produced by the different H-bridge cells. Different combinations of the four switching devices in each cell as shown in Figure 2.4 ($S_{a1}$, $S'_{a1}$, $S_{a2}$ and $S'_{a2}$ as in the case of the first cell) generates three voltage output levels $V_{dc}$, 0, $-V_{dc}$ [4]. The staircase waveform is virtually sinusoidal without even use filter. The CMI shown in Figure 2.4, each phase has two separate DC sources which generates a five levels output voltage. $V_{dc}$ is produced by turning switches $S_{a1}$ and $S'_{a2}$ on, while $-V_{dc}$ is produced by turning switches $S_{a2}$ and $S'_{a1}$ on. The output voltage will be 0 by turning on $S_{a1}$ and $S_{a2}$ switches or $S'_{a1}$ and $S'_{a2}$ switches. For the number of the output levels N, in each phase is given by Equation (2.1), when $n$ is the number of modules connected in series [26].

$$N = 2n + 1 \tag{2.1}$$

Either wye (Y) or delta (Δ) configurations could be connected to the output voltage of a three-phase cascaded multilevel inverter system. For example, Figure 2.4 shows a wye-configured 5-level CMI inverter with separated capacitors.

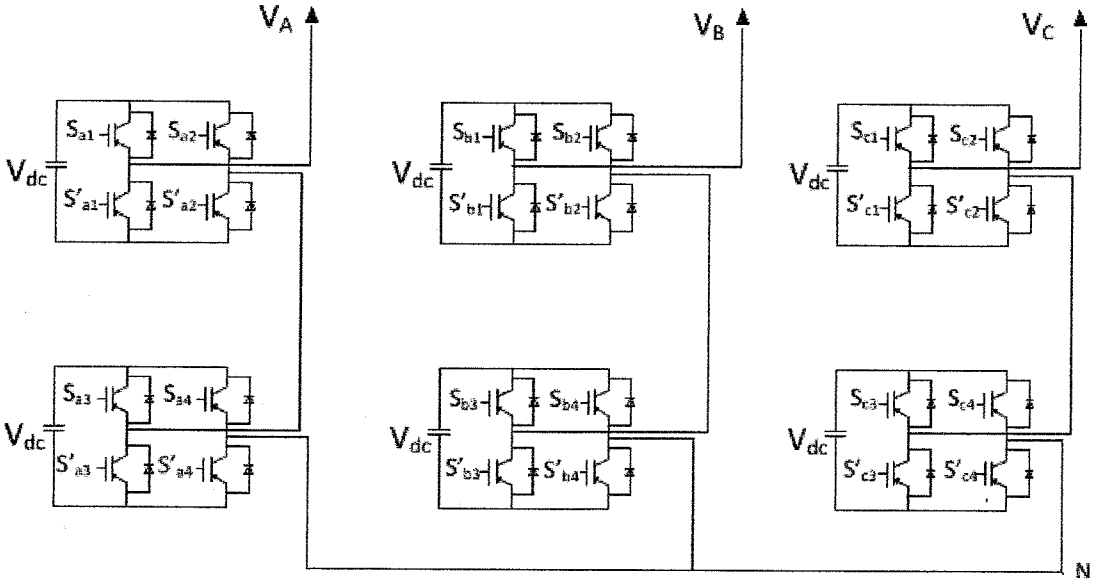



Figure 2.4: Five-level Cascaded H/bridge Multilevel Inverter topology

### *2.1.3.2 Features of Cascaded Multilevel Inverter*

Separate DC sources are needed for a real power conversions (AC to DC and DC to AC) when using the cascaded multilevel inverter. Various renewable energy sources such as biomass, photovoltaic, and fuel cell are well suited for the structure of separate DC sources [27]. The separated DC sources of the inverter makes it impossible to be in back-to-back form, as connecting two converters in a back-to-back fashion with separate DC sources will result in a short circuit when their switches are not synchronized.

*2.1.3.3 Advantages and Disadvantages of Cascaded Multilevel Inverter*

The advantages and disadvantages of the CMI are listed below [27].

The advantages are enunciated as follows;

a) The regulation of the DC buses is simple.
b) Modulating each full-bridge cell is possible due to separated DC source. Unlike the NPC and FC inverter where a central controller must be used to modulate each phase legs.
c) Has the minimum number of elements count between all multilevel inverters with the similar number of voltage levels.

The disadvantages are given as follows;

a) Synchronization of reference and the carrier waveforms of the full-bridge cells are only achieved when there is proper communication between cells.
b) Limited applications due to the need of independent DC sources for real power conversions.

## 2.2 Multilevel Modulation Techniques

Power electronic inverters mostly operate in the "switched mode", which means the inverter switches are always either in the turn-on state (saturated with only a small voltage drop across the switch) or turn-off state (no current flows). Modulation in power electronics inverters is simple the switching process of electronics devices (semiconductor switches) between the two states (i.e. on and off). When these switches alternate between these two states, it controls the flow of power in the inverter. High efficiency of power conversion is ensured when operating in switching mode. Pulse Width Modulation (PWM) is the technique mostly used in adjusting the AC output of power electronic inverters which changes the duty cycle of the inverter switches at a high switching frequency to attain the aim average low-frequency output current or voltage.

High switching frequency is referred in pulse width modulation process; so as to attenuate the undesired effect resulted from the discontinuous power flow at switching. Losses do occur as result of the transition between the two switching

states. Though at off-state the losses are zero, while relatively low during the on-state. Switching frequency has to be limited due to the switching losses. For GTO inverters, the ratio of switch frequency to fundamental frequency $f_c/f$ (the pulse number) may be as low as unity, which is known as square wave switching. Another application where the pulse number may be low is in converters which are better described as amplifiers [31], whose upper output fundamental frequency may be relatively high. These high power switch-mode amplifiers find application in active power filtering [32], test signal generation [33], servo [34] and audio amplifiers [35].

The low pulse numbers place the greatest demands on effective modulation to reduce the distortion as much as possible. In these circumstances, multilevel inverters can reduce the distortion substantially, by staggering the switching instants of the multiple switches and increasing the apparent pulse number of the overall inverter.

### 2.2.1 Pulse Width Modulation (PWM)

PWM schemes can operate based on the fundamental and high switching frequency. It could also be classified in terms of the method developed to control the inverter is open loop or closed loop concepts as shown in Figure 2.5. Among these are sinusoidal PWM, selective harmonic elimination, space vector modulation and hysteresis current control.

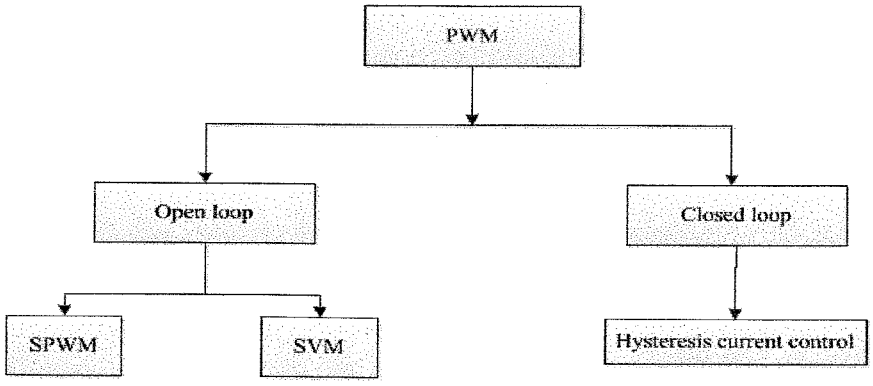



Figure 2.5: Control classification of PWM

*2.2.1.1 Sinusoidal Pulse Width Modulation (SPWM)*

The SPWM for three phase inverter shown in Figure 2.6 uses three reference sine wave and a triangular carrier wave as shown in Figure 2.7. The switching signals for the inverter switches are obtained by the intersection of the triangular carrier wave and the reference sine waves. The reference signals $V_{ref}$ of the phase voltages are sinusoidal (120° out of phase to each other) in the steady state, forming a symmetrical three-phase system. Figure 2.8(a) and (b) show the phase voltage $V_{oa}$ and line-line voltage $V_{ab}$ generated from the SPWM respectively [9].

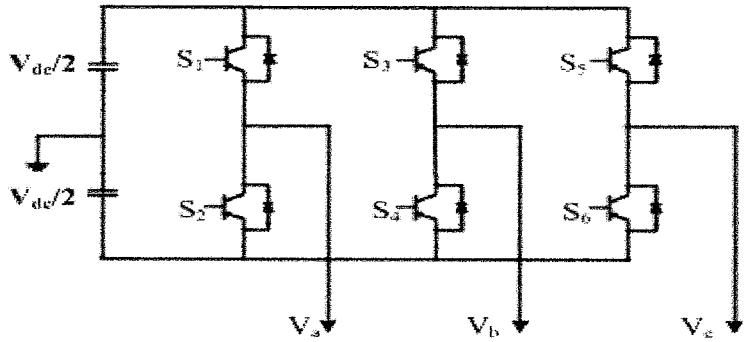



Figure 2.6:Three-phase power Inverter

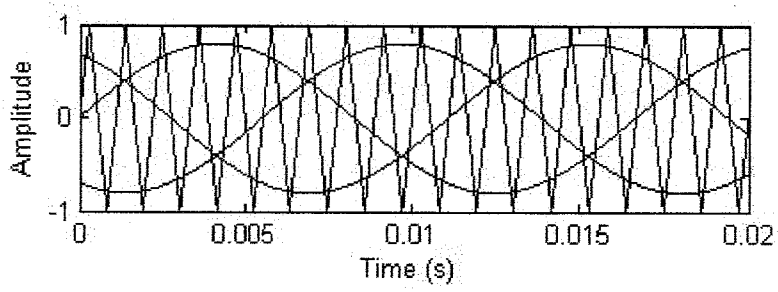
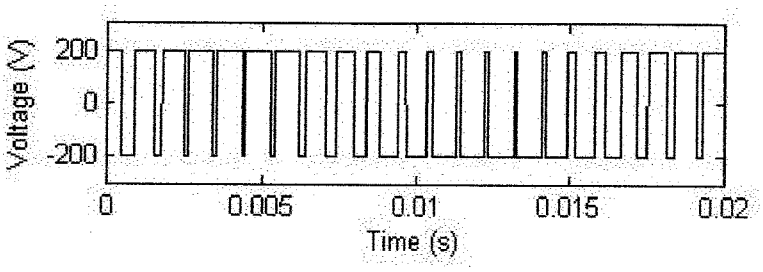
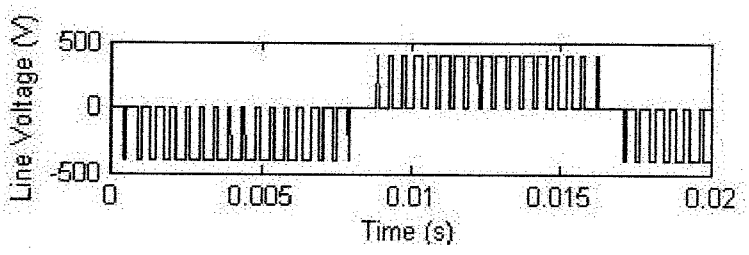



Figure 2.7:SPWM's modulating and carrier signal for a 3 phase inverter




(a) Phase Voltage of three phase Inverter




(b) Line-line Voltage of three phase Inverter

Figure 2.8: SPWM scheme for a 3 phase Inverter

*2.2.1.2 Space Vector Modulation (SVM)*

Space Vector Modulation (SVM) is one of the modulation techniques used in real time and digital control of a voltage source inverter. It is established on vector selection in the *q-d* stationary reference frame. The commanded voltage vector is defined by Equation (2.2) and Figure 2.9 shows the *d*, *q* component of the space vector plotted along with the vectors available by the inverter. Identifying the nearest three vectors is the first step in the SVM scheme. $V_d$ and $V_q$, are obtained from Equation (2.2).

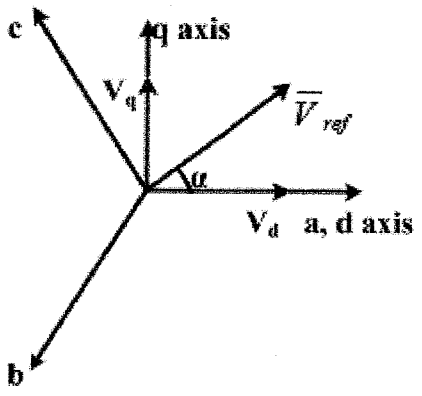



Figure 2.9: Voltage Space vector and its component in d, q.

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} \tag{2.2}$$

From Figure 2.9, $\overline{V}_{ref}$ and α can be obtained and are given in Equation (2.3) and (2.4) respectively.

$$\left|\overline{V}_{ref}\right| = \sqrt{V_d^{\,2} + V_q^{\,2}} \tag{2.3}$$

$$\alpha = \tan^{-1}\left(V_q / V_d\right) = \omega_s t = 2\pi f_s t \tag{2.4}$$

where $f_s$ is the fundamental frequency.

The time duration for the command vectors basically represents the off or on-states time (duty cycle time) of the selected switches during a sampling period $T_{pwm}$ of the modulation scheme [14] and are given in Equation (2.5) – (2.9).

$$T_0 = T_{pwm} - T_1 - T_2 \tag{2.5}$$

$$T_1 = T_{pwm} a \sin(\pi/3 - \alpha) \tag{2.6}$$

$$T_2 = T_s a \sin(\alpha) \tag{2.8}$$

$$a = \frac{\sqrt{3}}{V_{dc}} V_{ref} \tag{2.9}$$

There are eight possible switching combinations for the three phase two-level inverter shown in Figure 2.10. The switching mode for the lower transistor switches ($S_2$, $S_4$, $S_6$) are the exact opposite to the upper switches ($S_1$, $S_3$, $S_5$), so knowing one will give the other state [36]-[37]. The switching combinations and the phase and line-line output voltages in terms of DC supply voltage $V_{dc}$ are derive according to Equations (2.10) and (2.11) are summarized in Table 2.1.

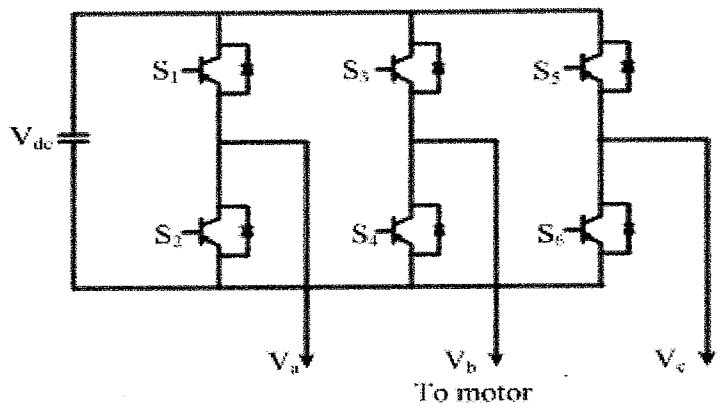



Figure 2.10: Three-phase power Inverter

When a, b or c is 1, it indicate that an upper transistor ($S_1$, $S_3$, $S_5$) is switched on, the corresponding lower transistors ($S_2$, $S_4$, $S_6$) are turn-off, that is the corresponding *a'*, *b'* or *c'* is 0.

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = V_{dc} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \tag{2.10}$$

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \frac{1}{3} V_{dc} \begin{bmatrix} 2 & -1 & 0 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \tag{2.11}$$

Table 2.1: Summary of the switching combination for a 3 phase Inverter in SVM

| Switching Vectors | | | Phase Voltage | | | Line-line Voltage | | |
|---|---|---|---|---|---|---|---|---|
| a | b | c | $V_a$ | $V_b$ | $V_c$ | $V_{ab}$ | $V_{bc}$ | $V_{ca}$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 2/3 | -1/3 | -1/3 | 1 | 0 | -1 |
| 1 | 1 | 0 | 1/3 | 1/3 | -2/3 | 0 | 1 | -1 |
| 0 | 1 | 0 | -1/3 | 2/3 | -1/3 | -1 | 1 | 0 |
| 0 | 1 | 1 | -2/3 | 1/3 | 1/3 | -1 | 0 | 1 |
| 0 | 0 | 1 | -1/3 | -1/3 | 2/3 | 0 | -1 | 1 |
| 1 | 0 | 1 | 1/3 | -2/3 | 1/3 | 1 | -1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

Changing the phase voltages to the corresponding eight combinations into the *d-q* plane by carrying out a *d-q* transformation which correspond to an orthogonal projection of $[a, b, c]^t$ onto the two dimensional (*d-q*) plane perpendicular to the vector $[1, 1, 1]^t$ as shown in Figure 2.9. This will results in two zero vectors and six non-zero vectors [38] and form hexagonal as shown in Figure 2.11.

The zero vectors are at the origin while two adjacent non-zero vector have an angle of 60° between them.

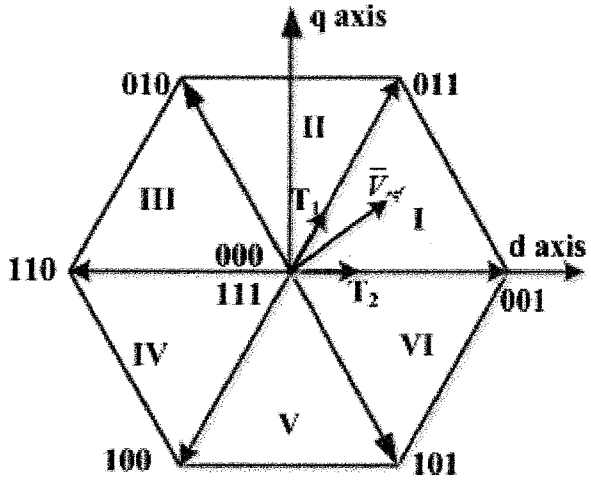



Figure 2.11: Space Vector diagram for a 3 phase Inverter

An optimum performance with a fixed switching frequency is obtained in SVM technique when each leg changes its state once in one switching period. To actualize this, two adjacent nonzero active state vectors and a zero state vector are applied in the first half period [39]-[40]. The mirror image of same sequence is applied to the next half of the switching period. The symmetrical SVM switching pattern is depicted in Figure 2.12.

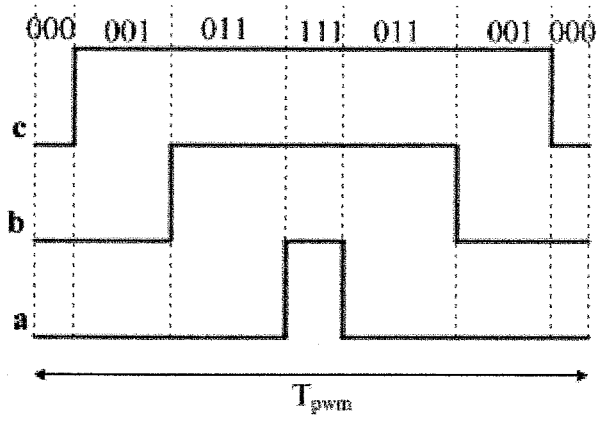



Figure 2.12: Duty cycle generation using SVM

*2.2.1.3 Selective Harmonic Elimination (SHE)*

The selective harmonics elimination techniques was proposed by Patel in 1974 based on fundamental switching theory and dependent on the elimination of defined harmonic content orders [4]. The main concept of this technique is to obtain the Fourier series expansion of the output voltage and define the switching angles of harmonic order to be eliminated. A $(2m + 1)$ –level inverter is used in producing a generalized quarter-wave symmetric stepped voltage waveform as shown in Figure 2.13, where $m$ is the number of switching angles.

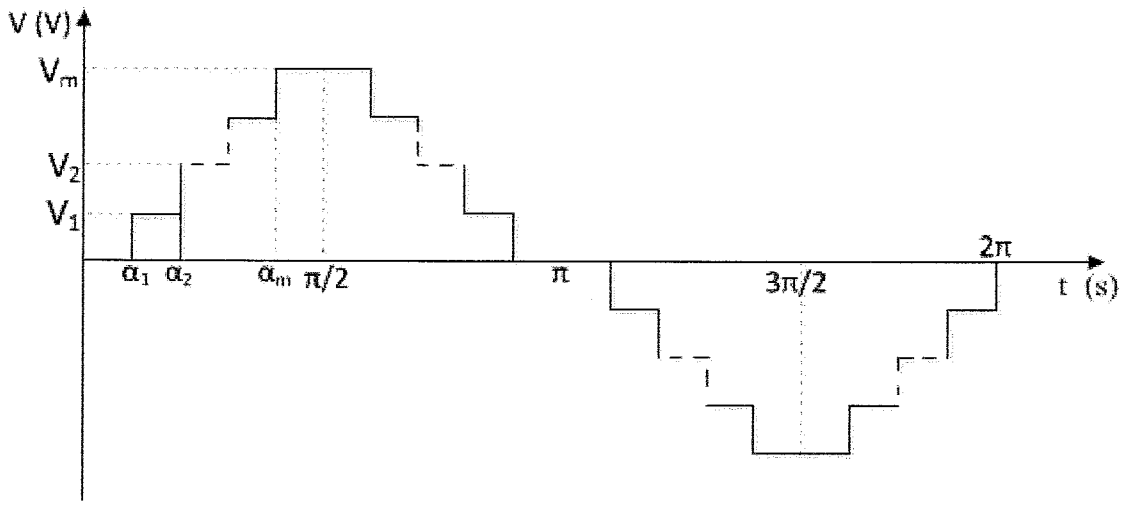



Figure 2.13: Generalized stepped Voltage waveform

Equation (2.12) gives the Fourier series analysis of the stepped waveform for the amplitude of any odd $n^{th}$ harmonic, while the amplitudes of all even harmonics are zero.

$$h_n = \frac{4}{n\pi}\sum_{k=1}^{m}\left[V_k \cos(n\alpha_k)\right] \tag{2.12}$$

where $V_k$ is the $k^{th}$ level of the dc voltage, $m$ is the number of switching angles, n is an odd harmonic order and $\alpha_k$ is the $k^{th}$ switching angle. From $\alpha_1$ to $\alpha_m$ must satisfy $\alpha_1 < \alpha_2 < \cdots < \pi/2$ according to Figure 3.8.

Proper selection of angles among different level leads to the elimination of low-frequency harmonics, while additional filter circuit can be used to remove high-

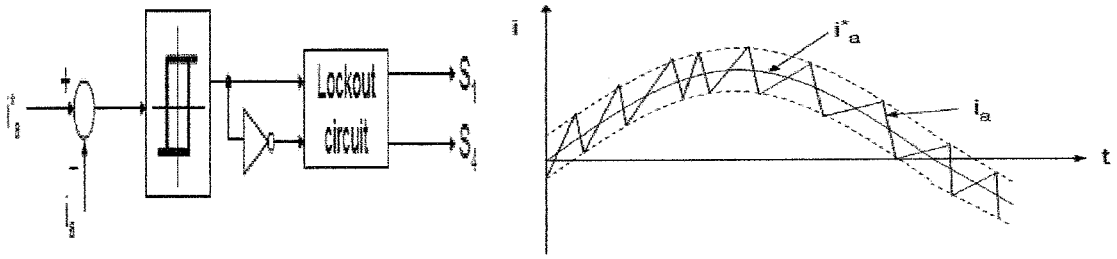
frequency harmonics [20]. The switching angles have to be below $\pi/2$, so that the number of eliminated harmonics are maintained at a constant level according to Equation (2.12), otherwise the modulation scheme no longer exist. As a result, a narrow range of modulation index is allowed when using this modulation strategy and perhaps its main drawback. For example, a modulation index of range 0.5 – 1.5 is only available for a seven-level equally stepped waveform. Applying this modulation technique with less than 0.5 modulation indexes, increases the total harmonic distortion (THD) and reducing the permissible harmonic components to be eliminated from 2 to 1.

#### *2.2.1.4 Hysteresis Current Control*

Figure 2.14(a) shows the controller that determines the error of the matching phase current which is kept within hysteresis bandwidth $\pm\Delta I$ as depicted in Figure 2.14(b). This hysteresis current control is applied in the switching state of a two-level inverter leg [41]-[42]. Defining a number of hysteresis bands used in a typical concept of two-level hysteresis current-control employed in drive systems extend it usage in multilevel systems. This type of controller involves *n-1* hysteresis bands evenly spaced on each side of the commanded current. When the measured current crosses a hysteresis band meaning it has deviated from the commanded value, then each time the voltage level increased by one. One important aspect of this control is that when the measured current overlaps the uppermost or lowermost hysteresis band then the voltage level will be at its lowest or highest value respectively. This regulates the current to be within the commanded value. The simplicity of the extension of two-level current control gives an acceptable voltage level switching and good regulation of the currents. Also, similar to the two-level hysteresis control response, the multi-level hysteresis control can handle steps change in the commanded current [43].

The use of a single hysteresis band and whenever the current touches the band, decreasing or increasing the voltage levels results in the reduction of the amount of analog circuitry. This method is coupled with voltage controlled oscillator and a timer

to push the current error to zero. To provide better dynamic performance, this method is extended to use two hysteresis bands and could be used for a large number of voltage levels with still little amount of analog circuitry. A different approach is to use the dual hysteresis band for multi-level inverter where current regulation is being achieved by the outer band and capacitor voltage balancing is achieve by the inner band [43].




(a) Logic circuit (b) Control waveform

Figure 2.14:Hysteresis current control and logic circuit

However, there are some inherent drawbacks [41]

a) No fixed PWM frequency: Involuntary lower sub-harmonics are produced by the hysteresis controller produces.
b) The current error is not strictly limited. The signal may leave the hysteresis band caused by the voltage of the other two phases.
c) Usually, there is no interaction between the three phases. No strategy to generate zero-voltage phasors.
d) Increased switching frequency (losses) especially at lower modulation or motor speed.
e) Phase lag of the fundamental current (increasing with the frequency).

## 2.3 Related Work

Al Mamum (2011) *et. al* [44], were able to developed a controller that uses the concept of fixed pulse pattern. However, the algorithm needs very high resources and control performance which will result to a complex control system and as well not cost effective. P. K. Chaturvedi (2011) *et. al* [6], they designed and implemented a

simple NPP regulator for a three phase three-level NPC based on the offset voltage addition to the reference voltages. They propose a method on how to calculate the offset voltage needed to realize the method. This is obtained without measuring the power factor angle and getting the difference between two DC link capacitor voltages for neutral point control implementation. The controlling of the discharging and charging of two capacitors is the basic idea behind this concept with suitable modification of the modulating signal in the SPWM technique.

C. M. Wu (1999) *et. al* [45], the authors were able to propose the five-level H-NPC inverter with its theoretical harmonic analysis. Their finding shows that the present of fourth order of the cross-modulated harmonics, though exhibiting an impressive harmonics suppression property. V. Guenneguez (2009) *et. al* [46], they introduce a SHE-PWM method and give the detail analysis on its loss and theoretical spectral analysis. The method used 180° symmetry SHE PWM to effectively obtained low voltage distortion on the motor. A study on losses in the H-NPC inverter shows that there is switching losses increase when using the 180° symmetry as compared to the 90° symmetry. From the above previous work, SPWM techniques exhibit a simple way of modulating the switching devices of any inverter by comparing two switching signals and with excellent output waveform characteristics. The previous work related to this research study is summarized in Table 4.1.

Table 2.2: Summary of previous work on PWM for Multilevel Inverter

| Reference | Approach | Description | Drawback |
|---|---|---|---|
| Z. Cheng (2007) *et. al* [47] | Space Vector Modulation (SVM) | SVM uses system control variable in a complex space (*d, q*) plane that are identified from each of the switching vector. The switching variable are computed off line and stored in a memory for the real time operation | Complexity in computing the space vector as the number of levels increases |
| V. Guenneguez (2009) *et. al* [46] | Selective Harmonic Elimination SHE-PWM | SHE-PWM is pre-calculated PWM method without carrier. It consists of calculating the switching angles, so as to take care of criteria like the inverter output waveform or the harmonic distortion on the motor | Increase in angles increase the switching loss and the computation of the switching angle becomes less accurate |
| P. K. Chaturvedi (2011) *et. al* [6] | Sinusoidal pulse width modulation (SPWM) | SPWM involves the comparing of carrier signal with reference signal to generate the switching signal | Fair harmonic mitigation |
| C. M. Wu (1999) *et. al* [45], Wu Bin (2006) *et. al* [13] | SPWM | Uses SPWM to generate 5 level output voltage and derived the analytical expression for the harmonics in the inverter | |
| Al Mamum (2011) *et. al* [44] | Fixed pulse pattern | The output voltage is obtained according to pulse pattern which are repeated every cycle. The pulse pattern is calculated off line, taking output voltage as parameter. | The frequency spectrum contains harmonic components in a wide frequency band |

## 2.4 Summary

In this chapter, an overview of classical multilevel inverter topologies such as; neutral point clamped, flying capacitors and cascaded multilevel inverter were presented with detail discussion on their operations, features, advantages and disadvantages. The conventional modulation schemes such as; sinusoidal pulse width modulation, space vector modulation, selective harmonic elimination and hysteresis current control were also presented with detail discussion on their operating features, merits and limitations. Previous works related to this research work were given.

# CHAPTER 3

# DEVELOPMENT OF THE SIMULATION MODELS

Five-level H-bridge / neutral point clamped inverter as a voltage source inverter has a primary function to produce a variable AC output voltage frequency and magnitude from a fixed DC source to the desired load.

## 3.1 Set up for the Simulation Models

This section discusses the modeling of five-level H-bridge / neutral point clamped inverter using sinusoidal pulse width modulation as the modulation scheme. The simulation involves building the MATLAB/Simulink blocks of the five-level H-bridge / neutral point clamped inverter circuit and each of sinusoidal pulse width modulation techniques. The blocks are shown in the Appendix A. Each SPWM technique is connected to the inverter and run to obtain the output voltage. The output voltage is analysis based the following performance index; harmonic suppression, total harmonic distortion, high voltage attainment and effect of amplitude modulation index variation. The sequence of the simulation procedure is illustrated in the flow chart as shown in Figure 3.1. In the following sections, the setting of five-level H-bridge / neutral point clamped inverter operation and the basic rules for the SPWM technique are discussed.

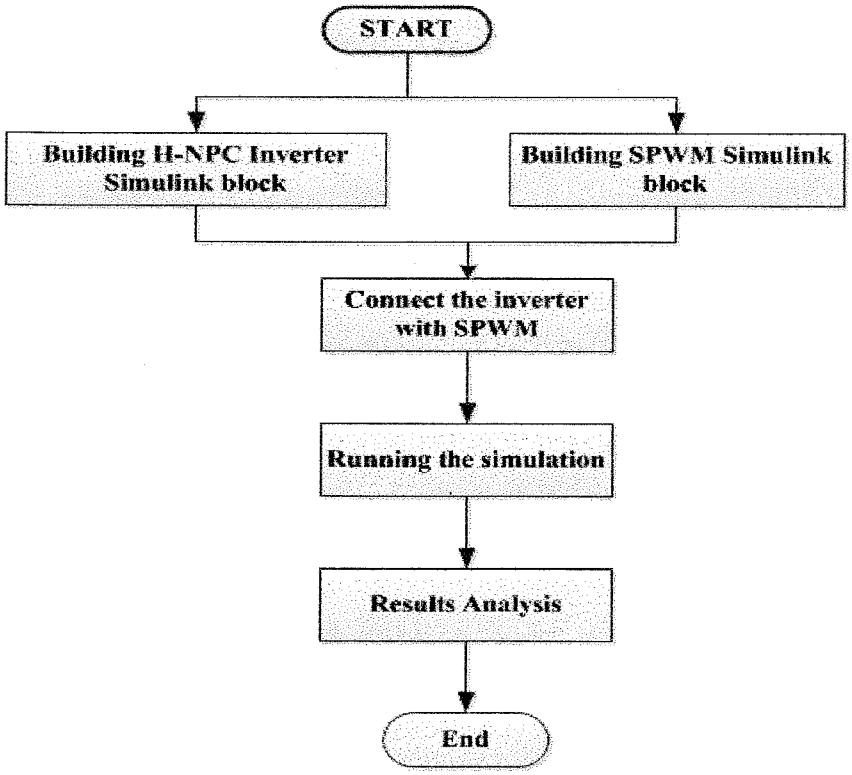



Figure 3.1: Flow chart of simulation procedure

### 3.2 Setting of H-NPC Inverter operation

Five-level H-NPC inverter consists of H-bridge connection of a two three-level NPC phase legs for each cell sharing a common DC bus as shown in Figure 3.2. Each leg has four switching devices with four freewheeling diodes and two clamping diodes to clamp the switches to the neutral are adopted. This topology has the advantage of producing five voltage levels in its phase voltages $V_{an}$, $V_{bn}$ and $V_{cn}$ as compared to the three levels for NPC inverter, resulting in a low Total Harmonic Distortion (THD) and $dv/dt$. Voltage stress on all the eight switching devices is half of DC bus voltage. The phase voltage of the inverter is the difference of the two legs voltage as given in Equation (3.1).

$$V_{an} = V_1 - V_2 \tag{3.1}$$

In each phase of the inverter, the eight switches constitute of four complementary switch pairs: $(S_{11}, S_{13})$, $(S_{12}, S_{14})$, $(S_{21}, S_{23})$ and $(S_{22}, S_{24})$ as in the case of phase 'a'

depicted in Figure 3.2. Therefore, four independent gate signals are required from the modulation scheme.

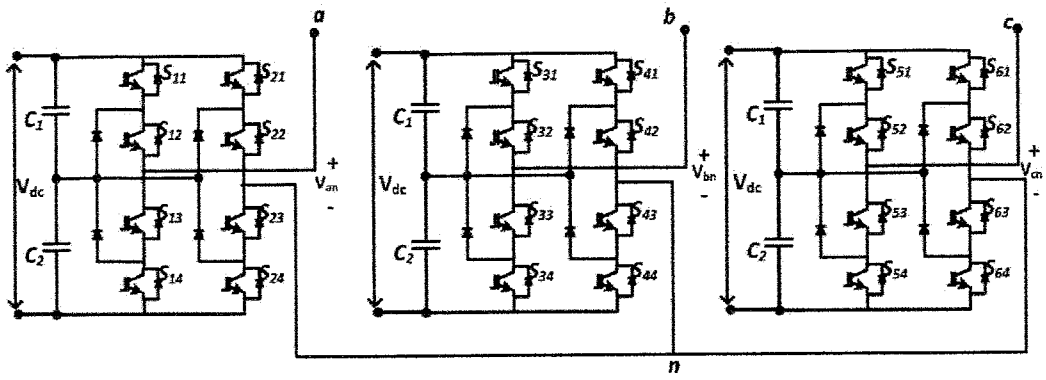



Figure 3.2: Five-level H-bridge/neutral point clamped (H-NPC) Inverter

### 3.2.1 Switching Mode of H-NPC Inverter

The switching operation of H-NPC inverter is based on that of phase leg of a three-level NPC inverter, where turning the upper switches ($S_{11}$ and $S_{12}$ in the case of phase 'a' in Figure 3.2) on in each leg produces $V_{dc}/2$. Switching the middle switches ($S_{12}$ and $S_{13}$) on produces zero voltage. Lower switches ($S_{13}$ and $S_{14}$) produces $-V_{dc}/2$ when switch on. The phase voltage of H-NPC inverter produces five voltage levels, $V_{dc}, V_{dc}/2$, 0, $-V_{dc}/2$ and $-V_{dc}$ when the dc bus voltage is $V_{dc}/2$. The inverter has eight valid operation modes that will result to the five levels of voltage taken Equation (3.1) into account as shown in Figure 3.3.

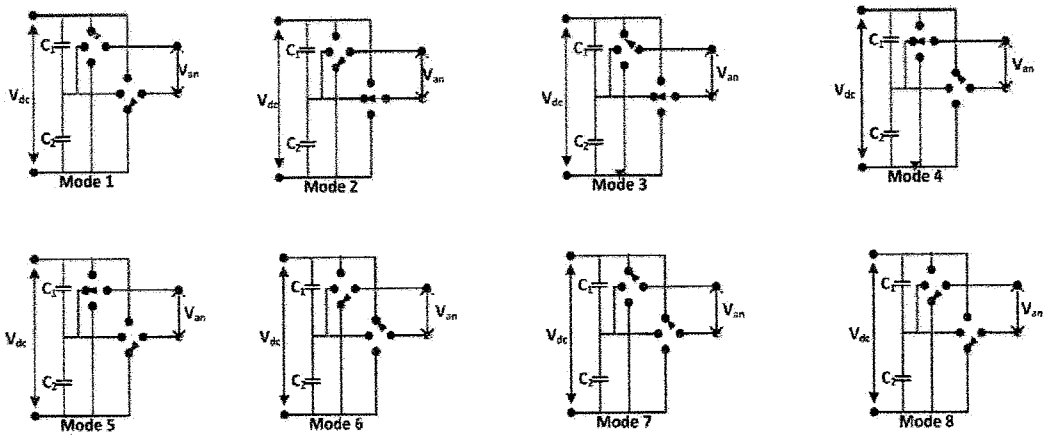



Figure 3.3: Switching modes of H-NPC Inverter

In Figure 3.3, mode 1 produces output voltage $V_{an} = V_{dc}$; in mode 2 the output voltage is $V_{an} = -V_{dc}/2$ in mode 3 the output voltage is $V_{an} = V_{dc}/2$; in mode 4 the output voltage is $V_{an} = -V_{dc}/2$; in mode 5 the output voltage is $V_{an} = V_{dc}/2$; in mode 6 the output voltage is $V_{an} = -V_{dc}$; and in mode 7 and 8, the output voltage is $V_{an} = 0$.

### 3.3 Sinusoidal Pulse Width Modulation Simulation

A sinusoidal pulse width modulation provides some advantages when use as the modulation scheme; in that an adjustment in the modulation index $m_a$ results in the change of the magnitude of the output voltage. Output frequency of the inverter could be change by adjusting the frequency of the modulating signal.

The traditional two-level sinusoidal pulse width modulation strategy has been extended to several levels for multilevel inverter. The multilevel voltage-source modulation scheme is the usual straightforward intersection of a triangle signals with modulating signal (duty cycle) [48]-[51]. There are four alternative SPWM techniques with different carrier arrangements:

a) In-Phase Disposition (IPD) – the two carrier signals are in phase, while the two reference signals are 180° out of phase to the other.
b) Alternate Phase Opposition Disposition (APOD) – it has its carrier signals, 180° out of phase with each other.
c) Phase Opposition Disposition (POD) – where the carriers below zero-axis are in phase and 180° out of phase with carriers above zero-axis which are also in phase within.
d) Phase Disposition (PD) – it has its carrier signals all in phase.

Several papers [13]-[15], use IPD to realize the desired output voltage of H-NPC inverter with a suppressed harmonic distortion. A MATLAB/Simulink model will be design according to the switching formation for each of the SPWM techniques on five-level H-NPC inverter and compare them to IPD.

### 3.3.1 In-Phase Disposition (IPD)

The in-phase disposition (IPD) is a modification of phase disposition (PD) where the triangle carrier waveforms are still in phase. In the five-level inverter IPD has two modulating waveforms instead of single modulating wave and two carrier waveforms instead of the four carrier waveforms in the conventional PD. The modulating waveforms are 180° out of phase to each other. Figure 3.4 shows the switching functions of IPD, while Figure 3.5 depicts the switching signals produced by IPD.

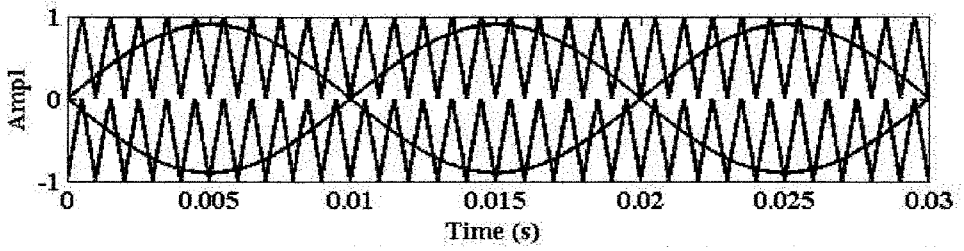



Figure 3.4: In-phase disposition (IPD)

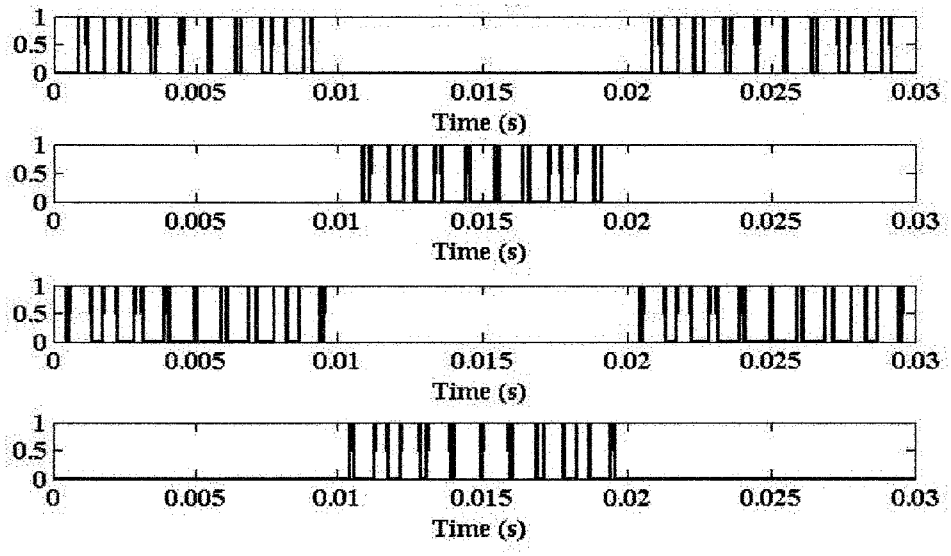



Figure 3.5: Switching signals generated by IPD

As shown in Figures 3.4 and 3.5, two gating signals are generated from the comprising of the modulating waveforms and carrier waveforms in the first half period. Another two gating signals are also produced in the second half period in a similar way to the first gating signals. These gating signals are used to drive the H-NPC inverter to achieve the desired output voltage with suppressed harmonic

contents. A MATLAB/Simulink model of IPD is developed to simulate the H-NPC inverter as shown in Figure A. 5.1 in the Appendix A.

### 3.3.2 Alternate Phase Opposition Disposition (APOD)

In the case of APOD modulation, the carrier signals are 180° out of phase with each neighboring carrier as shown in Figure 3.6. Considering a five-level inverter the APOD scheme is described below;

Taking $N = 5$ as the number of level, the rules for APOD method are,

a) The number of carrier signals should be $N - 1 = 4$, and are arranged to be 180° out of phase to each other.

b) The inverter produces $+V_{dc}/2$ when the reference signal is greater than all the carrier signals.

c) The inverter produces $+V_{dc}/4$ when the reference signal is less than the uppermost carrier signal and greater than all other carriers.

d) The inverter produces zero output voltage when the reference signal is less than the two uppermost carrier signals and greater than two lowermost carriers.

e) The inverter produces $-V_{dc}/4$ when the reference signal is greater than the lowermost carrier signal and lesser than all other carriers.

f) The inverter produces $-V_{dc}/2$ when the reference signal is lesser than all the carrier signals.

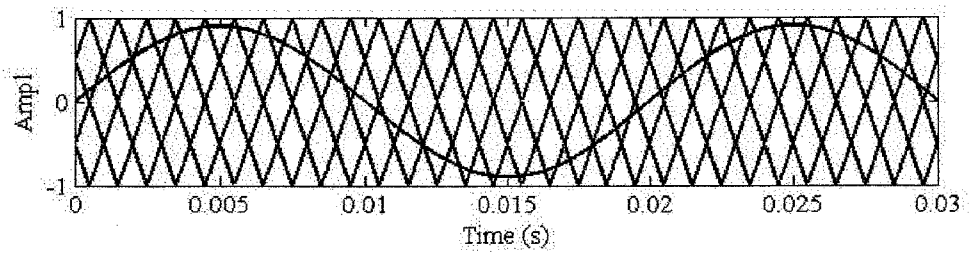



Figure 3.6: Alternative phase opposition disposition (APOD)

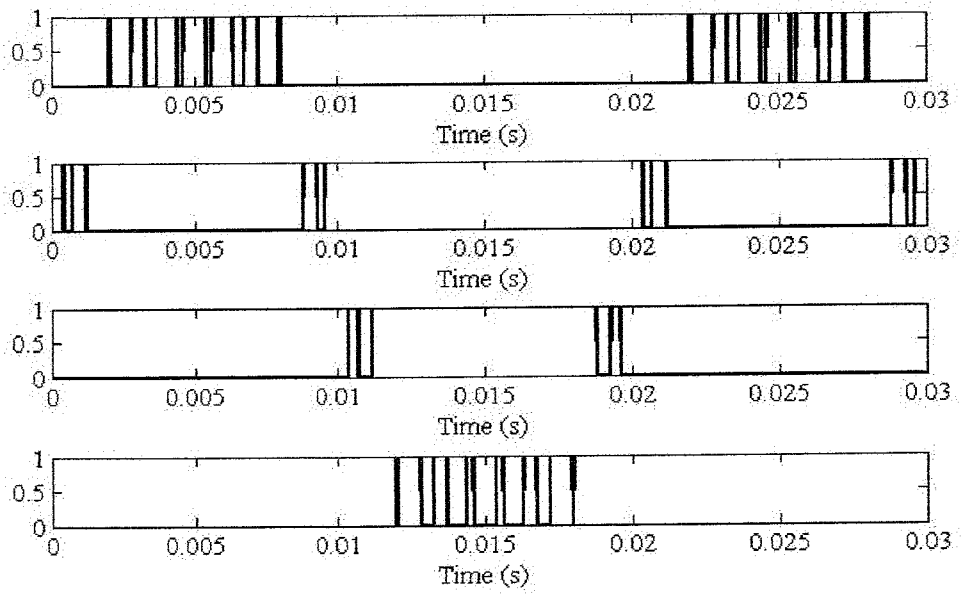



Figure 3.7: Switching signals generated by APOD

Figure 3.7 shows the switching signals generated from the intersection of reference signal and carrier signals of APOD. A model of APOD is developed to simulate the H-NPC inverter, as shown in Figure A.5.2 of the Appendix A.

### 3.3.3 Phase Opposition Disposition (POD)

All carrier signals below the zero-axis are in phase, in Phase Opposition Disposition (POD) modulation and are 180° out of phase with carrier signals above zero as shown in Figure 3.8.

Taking $N = 3$ as the number of level, the rules for the POD method are;

a) The number of carrier signals should be $N - 1 = 2$ carrier signals and are arranged so that all the carriers below zero-axis are in phase and180° out of phase with carriers above zero-axis.

b) The inverter produces $+V_{dc}/2$ when the reference signal is greater than carrier signals.

c) The inverter produces zero output voltage when the reference signal is greater than the lower carrier signal but less than the upper carrier signal.

d) The inverter produces $-V_{dc}/2$ when the reference signal is less than both carrier signals.

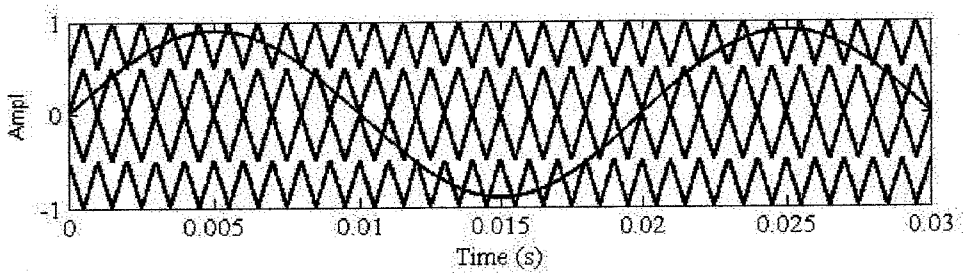



Figure 3.8: Phase opposition disposition (POD)

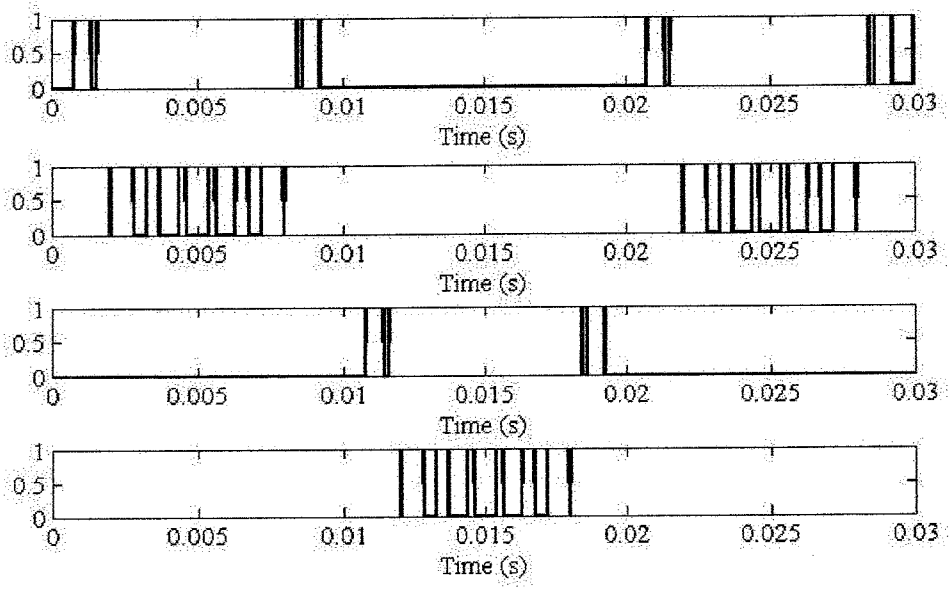



Figure 3.9: Switching signals generated by POD

Figure 3.9 shows how the switching signals are produced by POD -SPWM technique. In Figure 3.8 the POD - SPWM technique has four triangular signals. The upper triangles are occupying 0 to 1 magnitude, while the lower triangles occupied from -1 to 0 which are 180° out of phase with the upper triangular signals. A model of POD is developed to simulate the H-NPC inverter, as shown in Figure A.5.3 of the Appendix A.

### 3.3.4 Phase Disposition (PD)

PD has all its triangular carrier signals in phase with the neighboring carrier. Figure 3.10 shows the PD - SPWM technique for a five-level inverter. Therefore, four carrier (*N-1* in general) triangular signals are compared with the modulation reference signal.

Taking $N = 3$ as the number of level, the rules for the PD method are;

a) The number of carrier signals should be $N - 1 = 2$ carrier signals and are arrange in phase to each other.

b) The inverter produces $+V_{dc}/2$ when the reference signal is greater than carrier signals.

c) The inverter produces zero output voltage when the reference signal is greater than the lower carrier signal but less than the upper carrier signal.

d) The inverter produces $-V_{dc}/2$ when the reference signal is less than both carrier signals.

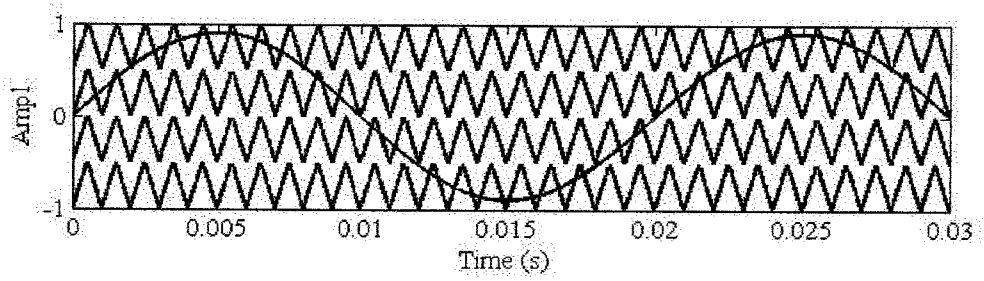



Figure 3.10: Phase disposition (PD)

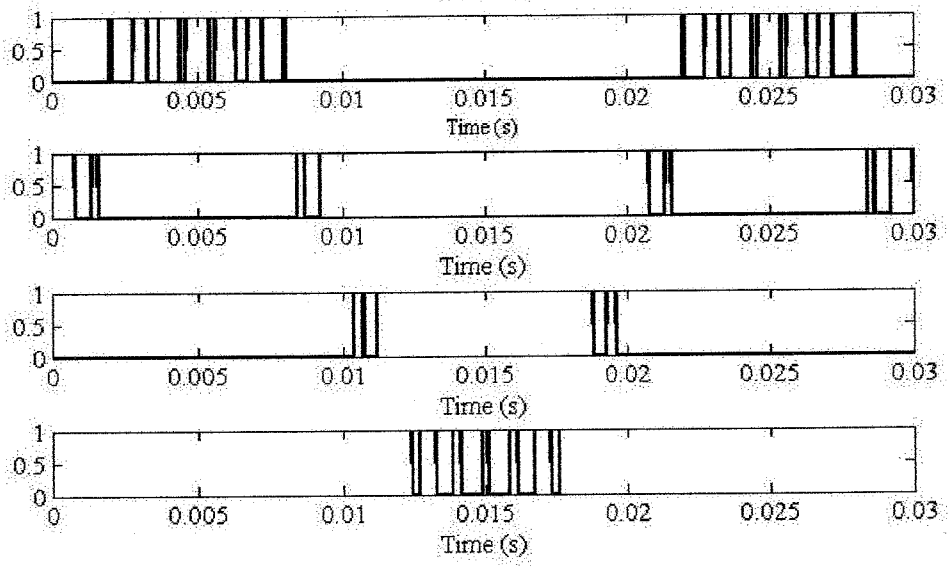



Figure 3.11: Switching signal generated by PD

In the PD technique, the reference signal is compared with the carrier at every instant of time and the switching signals are generated depending on which one is greater. Figure 3.11 shows how the switching patterns are produced by the PD - PWM technique. In the PD - PWM technique, there are four triangular carriers; the upper two triangles are occupying magnitude from 0 to 1while the lower two triangles range from -1 to 0. Similarly, for an N–level inverter, the number of carrier signals should be $N-1$ triangles and $2/(N-1)$ peak-to-peak value for each. A model of PD is developed to simulate the H-NPC inverter, as shown in Figure A.5.4 of the Appendix A.

### 3.4 Summary

This chapter has provided discussion on the simulation work for the modulating techniques such as the In-Phase Disposition (IPD), Alternate Phase Opposition Disposition (APOD), Phase Opposition Disposition (POD) and Phase Disposition (PD) on five-level H-bridge / neutral point clamped inverter. The finding and analysis of the simulation work would be presented in Chapter 4.

# CHAPTER 4

# RESULTS AND DISCUSSIONS

This chapter discusses the simulation results of five-level H-NPC inverter based on each of the SPWM techniques; IPD, APOD, POD and PD. The first section is the variation of amplitude modulation index and frequency modulation index for each of the SPWM techniques. The second section discusses the performance of five-level H-NPC inverter with comparison based on each result of the SPWM techniques.

## 4.1 In-Phase Disposition (IPD) Modulation Simulation

The H-NPC inverter is modeled based on the In-phase disposition (IPD) concept of Chapter 3. The modulation sub-system comprises of two modulating signals and two carrier signals as shown in Figure 4.1, to generate four gating signals for the switching devices of the H-NPC inverter phase cell. The gating signals of the remaining two phase cells are generated in a similar way with only changing the phase shifting of the modulating signal by 120° and 240° respectively in the cells.

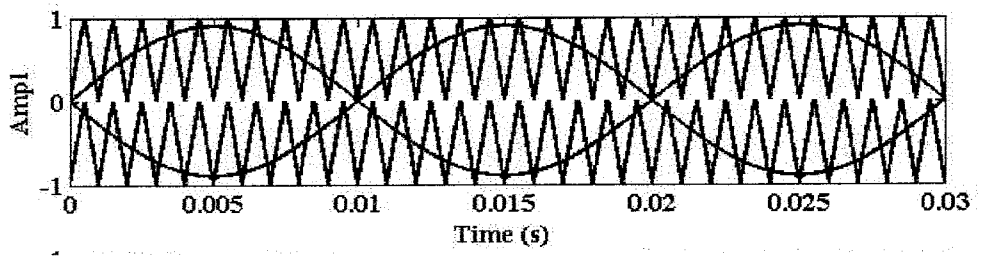



Figure 4.1: In-phase disposition (IPD)

### 4.1.1 Simulation results of IPD

The phase voltage waveform and its harmonic contents from IPD simulation of five-level H-bridge/neutral point clamped is shown in Figures 4.2 and 4.3 respectively. The inverter is simulated under the condition of amplitude modulation index

$m_a = 0.9$, frequency $f = 50\,Hz$, DC source voltage $V_{dc} = 100\,V$ and frequency modulation index $m_f = 20$.

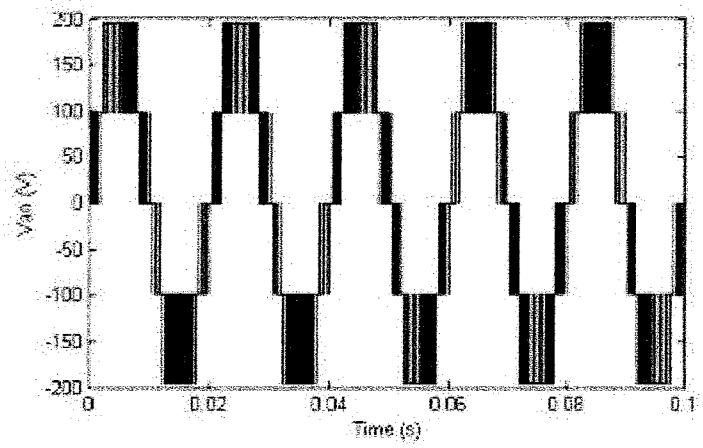



Figure 4.2: Phase voltage of H-NPC inverter using IPD

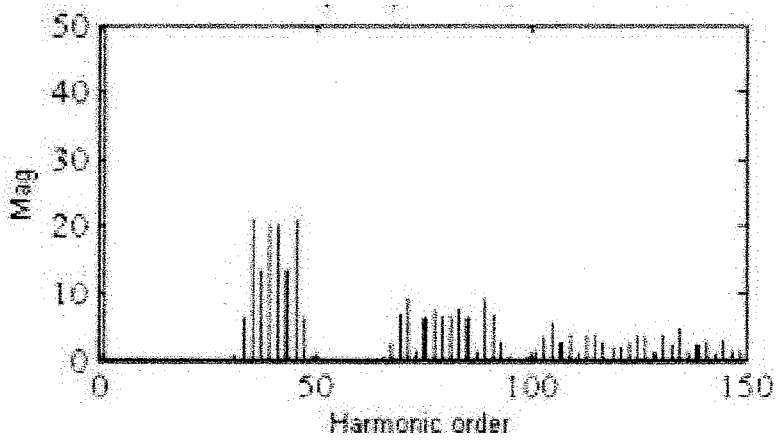



Figure 4.3: Harmonics content of the phase voltage with THD = 33.29 %

The phase voltage waveform consists of five levels and has total harmonic distortion at 33.29 %. The harmonics appear to be centered at $2m_f$ and its multiples $4m_f$ which are surrounded with sideband harmonics. The least harmonic content is the $33^{th}$ order and have triplen harmonic contents such as $(2m_f \pm 3)$ and $(4m_f \pm 3)$

Figures 4.4 and 4.5, shows the line-line voltage containing nine voltage levels and its harmonic content with THD of 27.18 %. The THD reduce as result of the cancellation of the triplen harmonics between the two phases due three phase balance system.

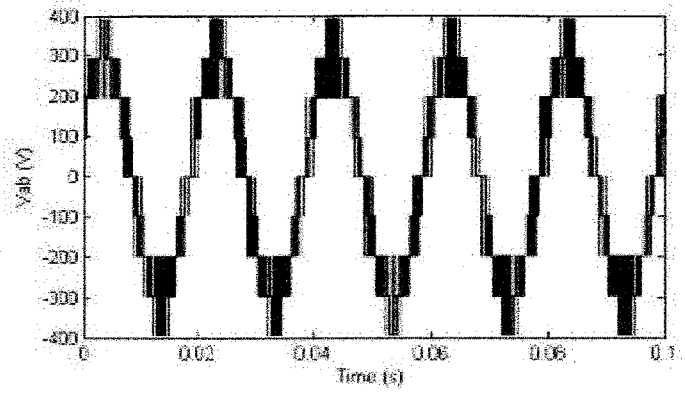



Figure 4.4: Line-line voltage of H-NPC inverter using IPD

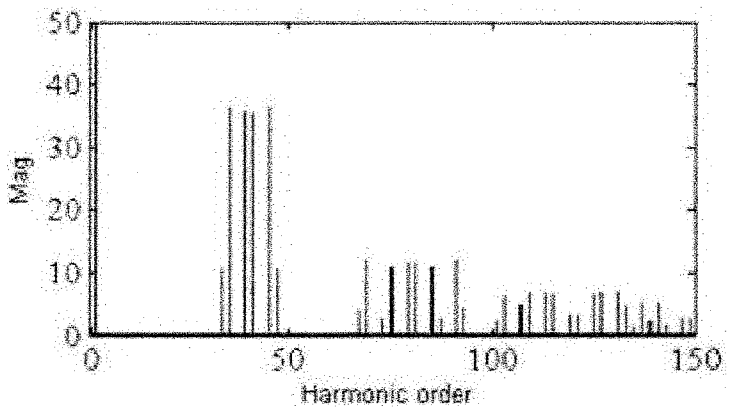


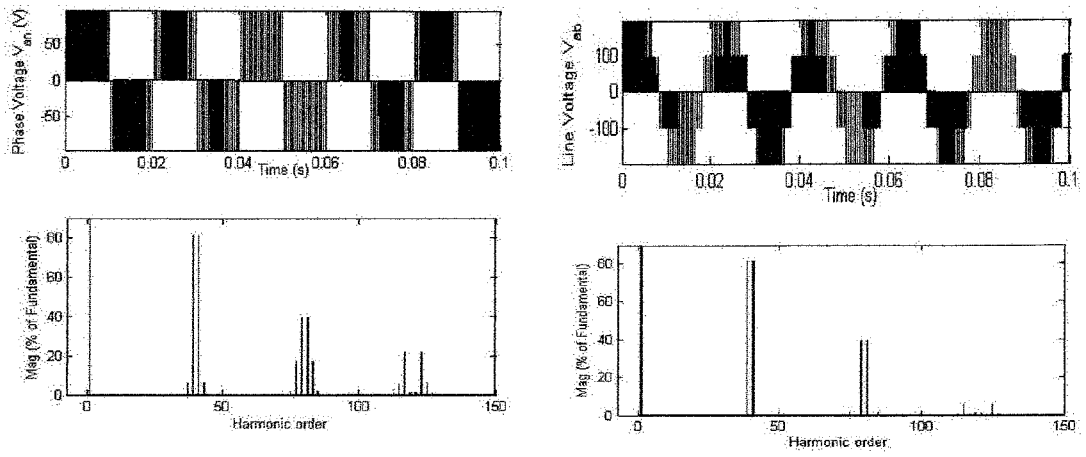

Figure 4.5: Harmonic contents of the line-line voltage with THD = 27.18 %

### 4.1.2 In-phase Disposition (IPD) with varying Amplitude Modulation Index

The amplitude modulation index $m_a$ is varied in the range of 0.2 – 1.0, while the inverter operates under the conditions; DC source voltage $V_{dc} = 100\ V$, frequency $f = 50\ Hz$, frequency modulation index $m_f = 20$.

Figure 4.6(a) shows the phase voltage waveform and its harmonic contents for $m_a = 0.2$. The line-line voltage waveform and its harmonic contents are depicted in Figure 4.6(b). The waveform of the phase voltage contains three voltage levels with Total Harmonic Distortion (THD) of 147.64 %. The harmonic contents to be centered at $2m_f$ and it multiplies; $4m_f$ with sideband harmonics surrounding them. The THD

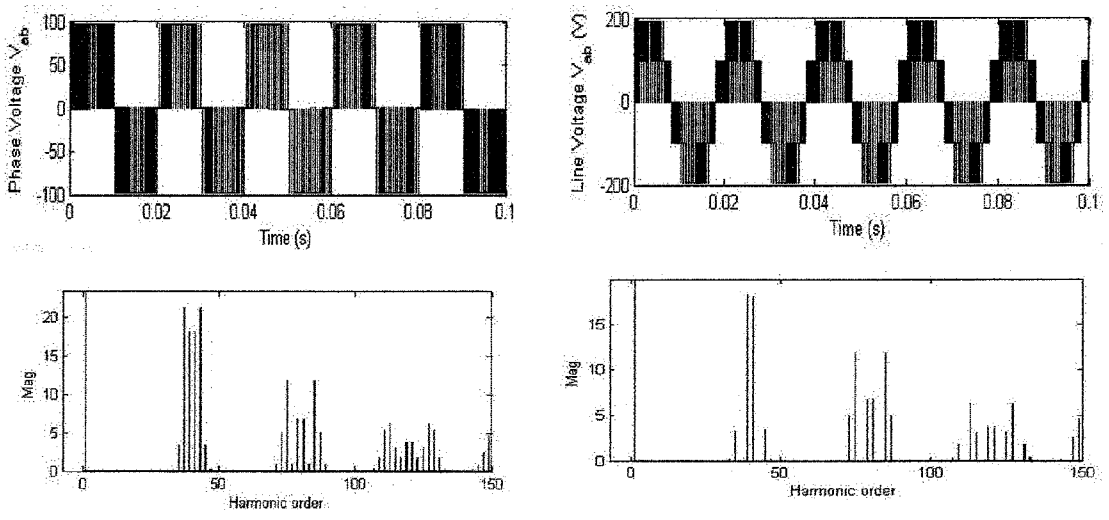
reduce in the line-line voltage due three phase balance system as the triplen harmonics cancel out between the phases.




(a) Phase Voltage (b) Line-line Voltage

Figure 4.6: Waveform and harmonic contents of H-NPC inverter for $m_a = 0.2$ (IPD)

The waveform and harmonic contents for $m_a = 0.5$ is similar to that of $m_a = 0.2$ in which it contains three voltage levels in phase waveform with 52.02 % as the THD as shown in Figure 4.7(a). The THD is reduced to 39.90 % in the line due to triplen harmonic cancellation between the phases because of three phase balance system as indicated in Figure 4.7(b).

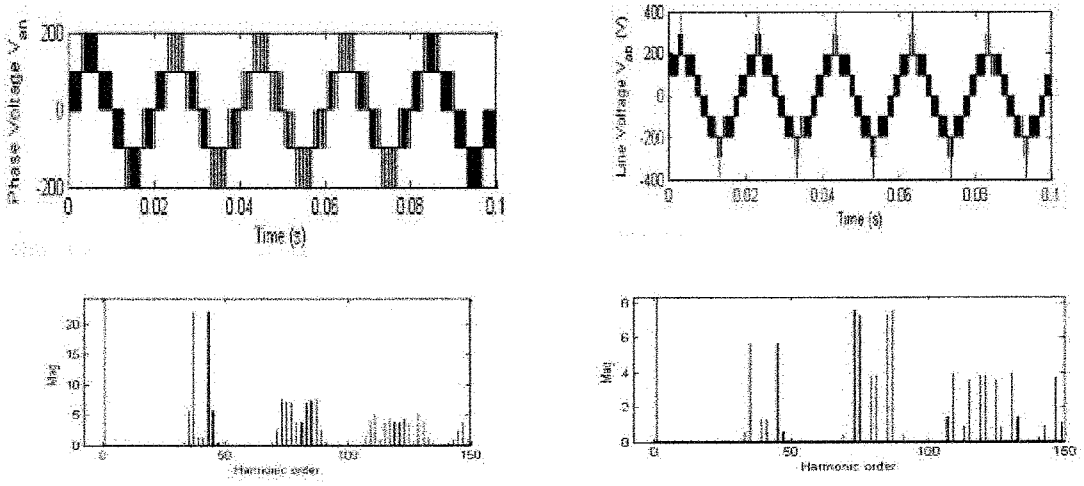



(a) Phase Voltage (b) Line-line Voltage

Figure 4.7: Waveform and harmonic contents of H-NPC inverter for $m_a = 0.5$ (IPD)

The waveform of the inverter begins to produces a five voltage levels at $m_a = 0.54$. Figure 4.8(a) shows the phase voltage waveform and harmonic contents

for$m_a$ = 0.6. The phase voltage is containing five voltage levels with total harmonic distortion (THD) of 44.32 %. The harmonics are centered around $2m_f$ and it multiplies $4m_f$ with sideband harmonics surrounding them. The least harmonic content is 33$^{th}$ order and have triplen harmonic such as $(2m_f \pm 3)$ and$(4m_f \pm 3)$. The triplen harmonics are eliminated in the line voltage as shown in Figure 4.8(b), which results to reduction of the THD to 25.64 %.




(a) Phase Voltage (b) Line-line Voltage

Figure 4.8: Waveform and harmonic contents of H-NPC inverter for $m_a$= 0.6 (IPD)

As shown in the Figures 4.6 and 4.7 that amplitude modulation index below 0.5 produces waveform that contains three voltage levels while above 0.5 produces five voltage levels as shown in Figure 4.8. The total harmonic distortion THD decreases as the amplitude modulation index increases as given in Table 4.1. Figure 4.9 shows the variation in THD as amplitude modulation index $m_a$ is varied from 0.2 to 1.0.

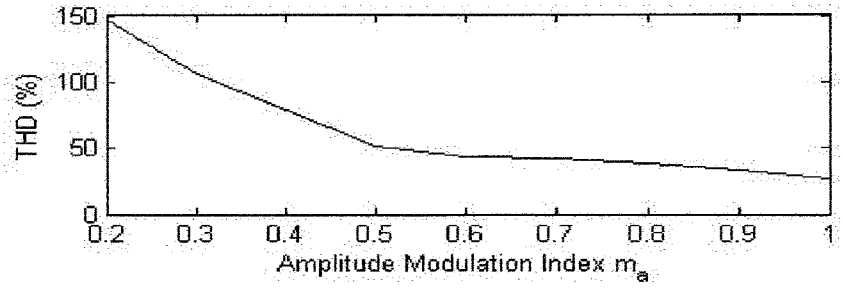



Figure 4.9: THD vs. Amplitude Modulation Index for IPD

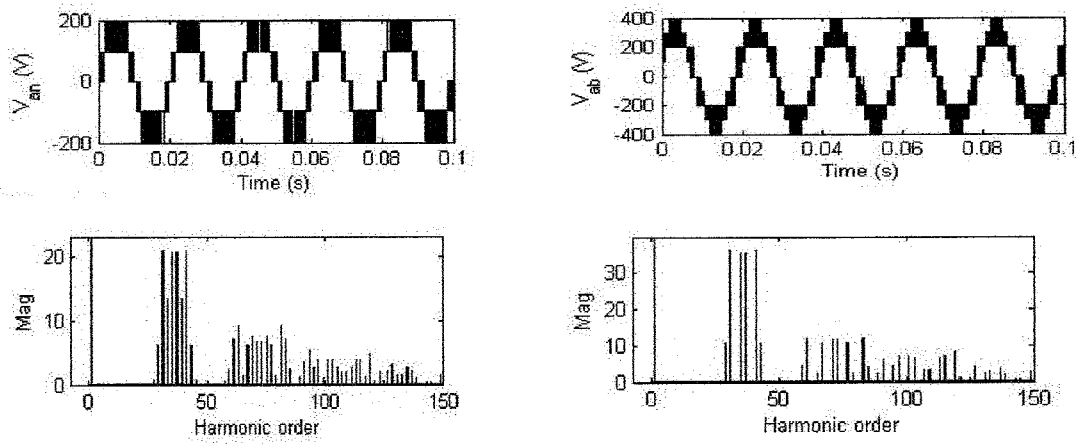
Table 4.1: Amplitude Modulation Index $m_a$ vs. THD for IPD

| Amplitude Modulation Index $m_a$ | Total Harmonic Distortion THD (%) |
|---|---|
| 0.2 | 147.64 |
| 0.3 | 105.73 |
| 0.4 | 78.42 |
| 0.5 | 52.02 |
| 0.6 | 44.32 |
| 0.7 | 41.78 |
| 0.8 | 38.15 |
| 0.9 | 33.29 |
| 1.0 | 26.63 |

### 4.1.3 In-phase Disposition (IPD) with varying Frequency Modulation Index

The simulation of H-NPC inverter for IPD with three different frequency modulation indices $m_f$; 18, 21 and 24 were carried out. The other parameters that inverter operates under are voltage DC source $V_{dc} = 100\,V$, amplitude modulation index $m_a = 0.9$ and frequency $f = 50\,Hz$.

The voltage waveform in the phase voltage consists of five voltage levels with 32.99 % as the total harmonic distortion as shown in Figure 4.10(a). The harmonic components are centered around $2m_f$ and it multiplies $4m_f$ with sideband harmonics surrounding them. The line-line voltage contains nine voltage levels and has 28.36 % THD as the triplen harmonics are absent due to three phase system balance as depicted in Figure 4.10(b).




(a) Phase Voltage (b) Line-line Voltage

Figure 4.10: Waveform and harmonic contents of H-NPC inverter for $m_f = 18$ (IPD)

The three different frequency modulation indices have the same harmonic characteristic as the harmonic are centered around $2m_f$ and it multiplies $4m_f$, $6m_f$ with sideband harmonics surrounding them. The total harmonic distortions (THDs) have small differences as indicated in Table 4.2.

Table 4.2: Frequency Modulation Index $m_f$ vs. THD for IPD

| Frequency Modulation Index $m_f$ | Total Harmonic Distortion THD (%) |
|---|---|
| 18 | 32.99 |
| 21 | 33.41 |
| 24 | 33.03 |

## 4.2 Alternate Phase Opposition Disposition (APOD) Simulations

The H-NPC inverter is modeled based on the alternate phase opposition disposition (APOD) concept of Chapter 3. The modulation sub-system comprises of modulating signal and four carrier signals as shown in Figure 4.11, to generate four gating signals for the switching devices of the H-NPC inverter phase cell. The gating signals of the remaining two phase cells are generated in a similar way with only

changing the phase shifting of the modulating signal by 120° and 240° respectively in the cells.

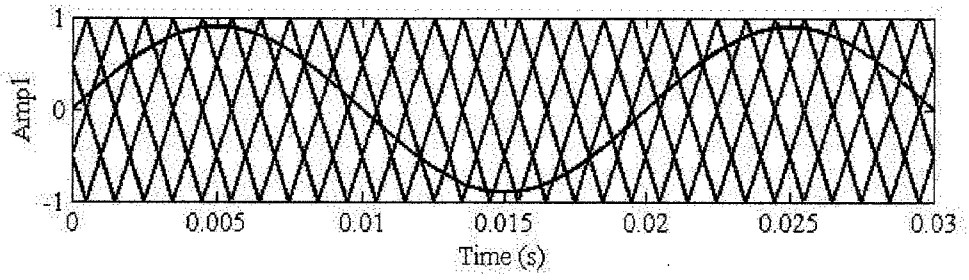



Figure 4.11: Alternate phase opposition disposition (APOD)

### 4.2.1 Simulation results of APOD

The phase voltage waveform and its harmonic contents from APOD simulation of five-level H-bridge/neutral point clamped is shown in Figures 4.12 and 4.13 respectively. The inverter is simulated under the condition of amplitude modulation index $m_a = 0.9$, frequency $f = 50\,Hz$, DC source voltage $V_{dc} = 100\,V$ and frequency modulation index$m_f = 20$. The phase voltage waveform consists of five levels and has total harmonic distortion at 33.46 %. The harmonics appear to be centered at $m_f$ and it multiples $2m_f$ which are surrounded with sideband harmonics. The least harmonic content is the $11^{th}$ order and have triplen harmonic contents such as $(m_f \pm 3)$ and $(2m_f \pm 3)$.

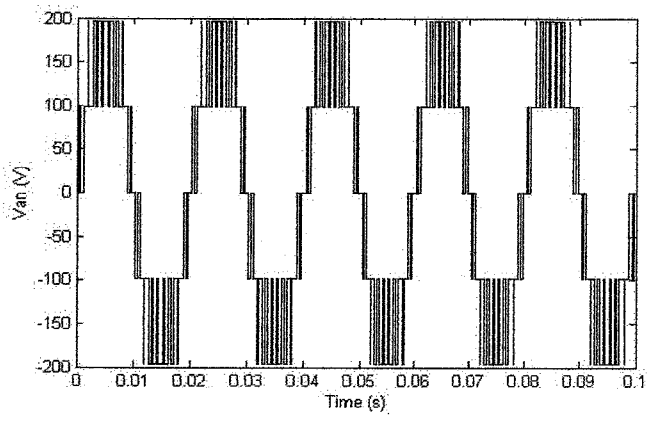



Figure 4.12: Phase voltage of H-NPC inverter using APOD

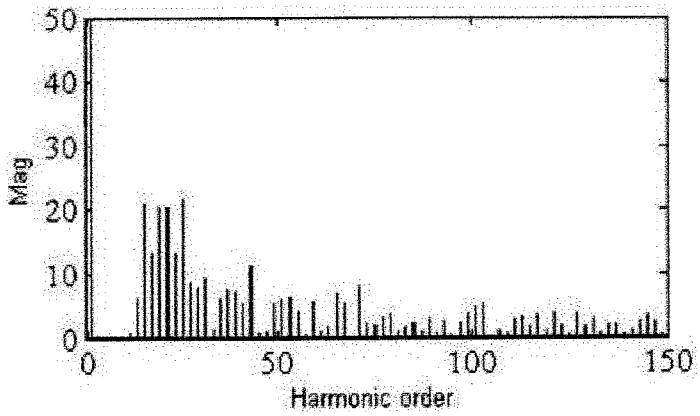



Figure 4.13: Harmonics content of the phase voltage with THD = 33.46 %

Figures 4.14 and 4.15, shows the line-line voltage containing nine voltage levels and its harmonic content with THD of 29.00 %. The THD reduce as result of the cancellation of the triplen harmonics between the two phases due three phase balance system.

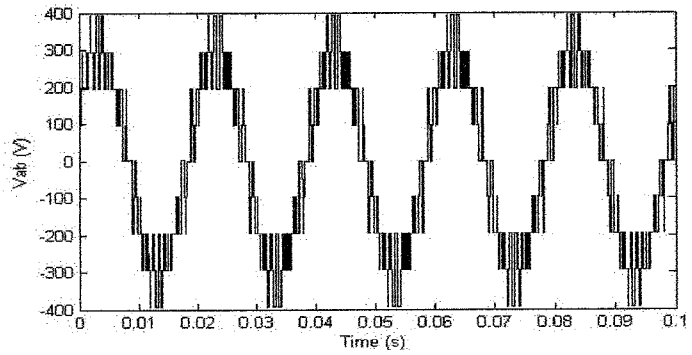



Figure 4.14: Line-line voltage of H-NPC inverter using APOD

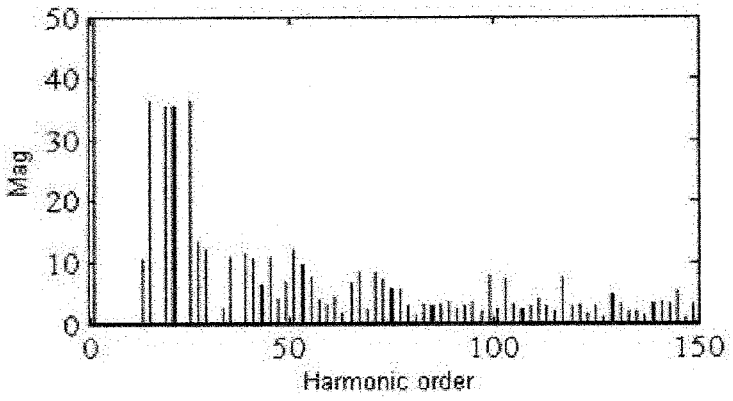
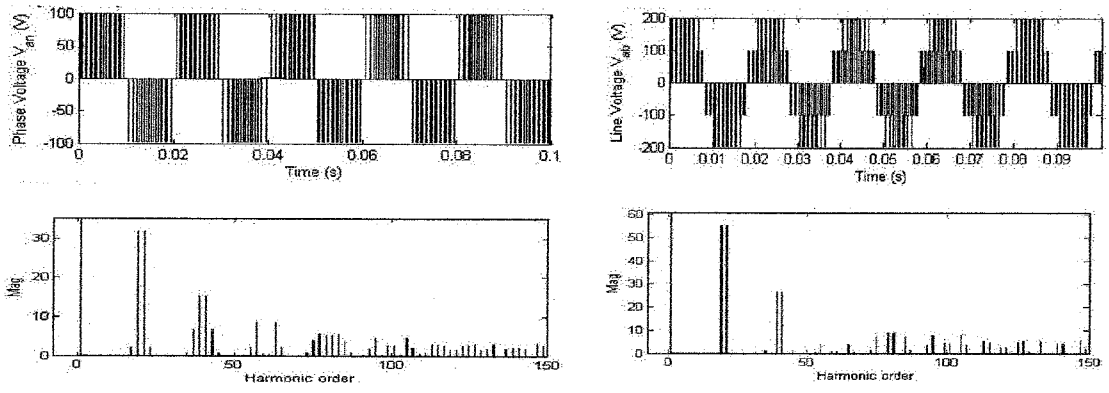



Figure 4.15: Harmonics content of the line-line voltage with THD = 29.00 %

### 4.2.2 Alternate Phase Opposition Disposition (APOD) with vary Amplitude Modulation Index

The amplitude modulation index $m_a$ is varied in the range of 0.2 – 1.0, while the inverter operates under the conditions; DC source voltage $V_{dc} = 100\,V$ frequency $f = 50\,Hz$ and frequency modulation index $m_f = 20$.

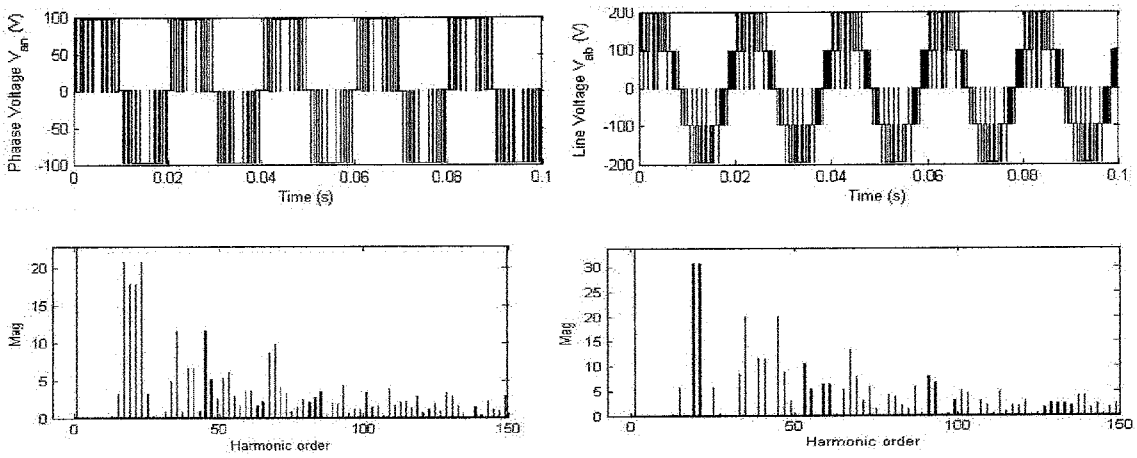
Figure 4.16(a) shows the phase voltage waveform and its harmonic contents for $m_a = 0.2$. The line-line voltage waveform and its harmonic contents are depicted in Figure 4.16(b). The waveform of the phase voltage contains three voltage levels with total harmonic distortion (THD) of 148.13 %. The harmonic contents to be centered at $m_f$ and it multiplies; $2m_f$ with sideband harmonics surrounding them. The THD reduce in the line-line voltage due three phase balance system as the triplen harmonics cancel out between the phases.




(a) Phase Voltage (b) Line-line Voltage

Figure 4.16: Waveform and harmonic contents of H-NPC inverter for $m_a = 0.2$ (APOD)

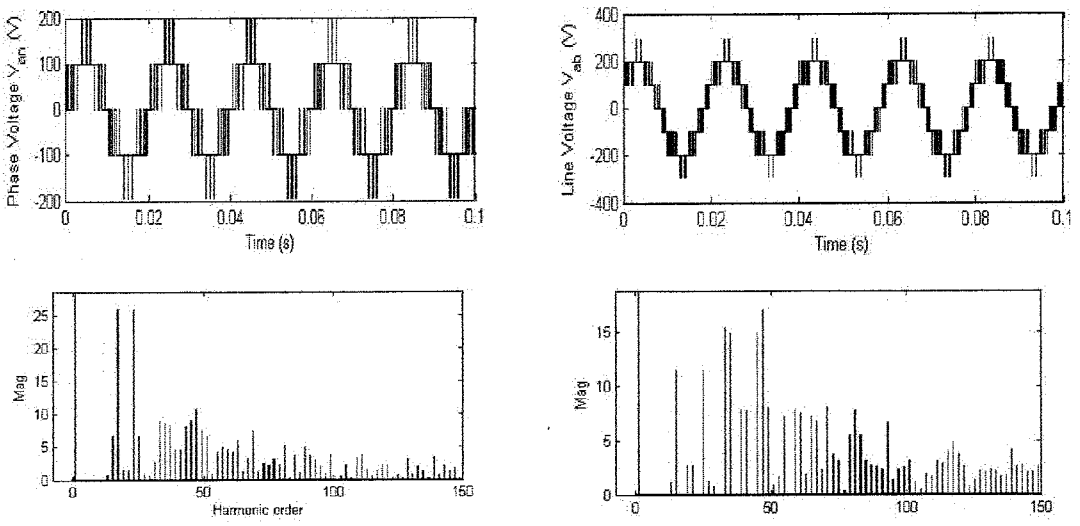
The waveform and harmonic contents for $m_a = 0.5$ is similar to that of $m_a = 0.2$ in which it contains three voltage levels in phase waveform with 52.79 % as the THD as shown in Figure 4.17(a). The THD is reduced to 39.93 % in the line-line voltage due to triplen harmonic cancellation between the phases because of three phase balance system as indicated in Figure 4.17(b).




(a) Phase Voltage (b) Line-line Voltage

Figure 4.17: Waveform and harmonic contents of H-NPC inverter for $m_a = 0.5$ (APOD)

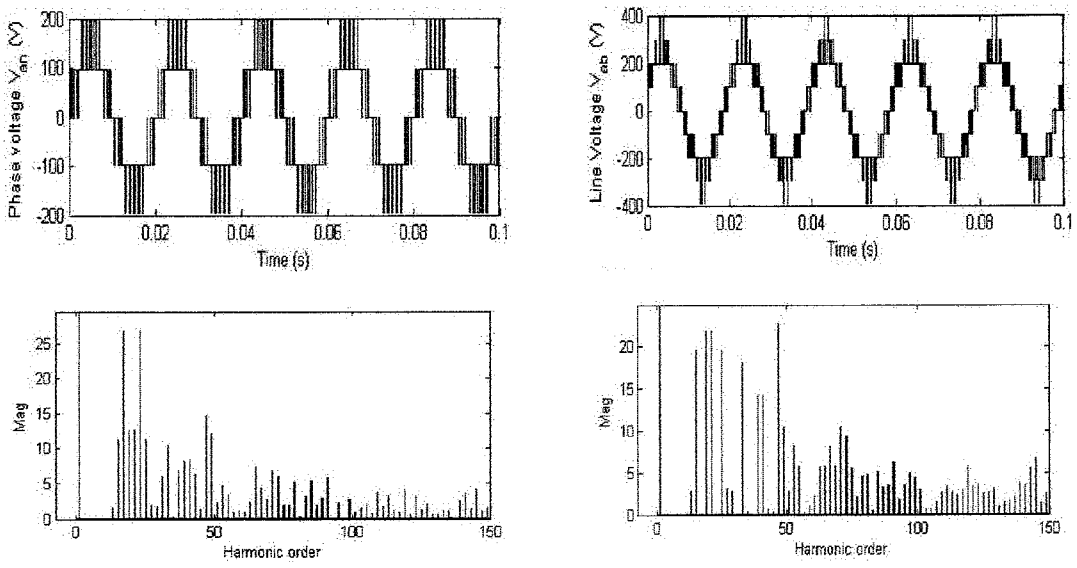
At $m_a = 0.6$, the phase voltage consists of five voltage levels with 44.67 % THD. The harmonics appear to be centered at $m_f$ and its multiples $2m_f$ which are surrounded with sideband harmonics. The least harmonic content is the 13$^{th}$ order, thus has some additional higher order harmonics than in $m_a = 0.5$ with minimal strength as shown in Figure 4.18(a). Triplen harmonic contents such as $(m_f \pm 3)$ and $(2m_f \pm 3)$ are present in the phase voltage. The line-line voltage contains seven voltage levels with 25.91 % THD.




(a) Phase Voltage (b) Line-line Voltage

Figure 4.18: Waveform and harmonic contents of H-NPC inverter for $m_a = 0.6$ (APOD)

At $m_a = 0.7$ the phase voltage consists of five voltage levels with 42.96 % THD. The harmonics appear to be centered at $m_f$ and it multiples $2m_f$ which are surrounded with sideband harmonics. The least harmonic content is the 13th order, thus has some additional higher order harmonics as in $m_a = 0.6$ with minimal strength as shown in Figure 4.19(a). Triplen harmonic contents such as $(m_f \pm 3)$ and $(2m_f \pm 3)$ are present in the phase voltage. The line-line voltage contains nine voltage levels with 25.91 % THD.




(a) Phase Voltage (b) Line-line Voltage

Figure 4.19: Waveform and harmonic contents of H-NPC inverter for $m_a = 0.7$ (APOD)

As shown in the Figure 4.16(a) and 4.17(a) that amplitude modulation index below 0.5 produces waveform that contains three voltage levels in the phase voltage while above 0.5 produces five voltage levels as shown in Figures 4.18a and 4.19a. Figure 4.18(b) shows that the line-line voltage consists of seven voltage levels for $\boldsymbol{m_a = 0.6}$ while Figure 4.19(b) shows that the line-line voltage consists of nine voltage levels for $\boldsymbol{m_a = 0.7}$. The total harmonic distortion THD decreases as the amplitude modulation index increases as given in Table 4.3. Figure 4.20 shows the variation in THDs as amplitude modulation index is varied from 0.2 to 1.0.

Table 4.3: Amplitude Modulation Index $m_a$ vs. THD for APOD

| Amplitude Modulation Index $m_a$ | Total Harmonic Distortion THD (%) |
|---|---|
| 0.2 | 148.13 |
| 0.3 | 106.34 |
| 0.4 | 77.36 |
| 0.5 | 52.79 |
| 0.6 | 44.67 |
| 0.7 | 42.96 |
| 0.8 | 38.45 |
| 0.9 | 33.46 |
| 1.0 | 28.10 |

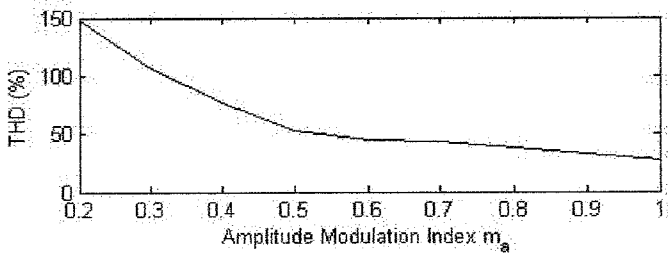


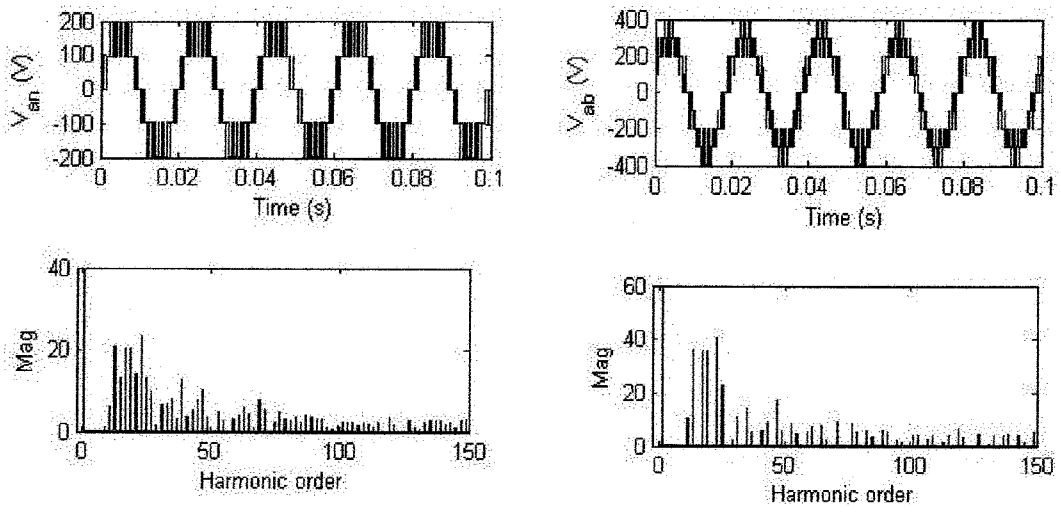

Figure 4.20: THD vs. Amplitude Modulation Index for APOD

### 4.2.3 Alternate Phase Opposition Disposition (APOD) with varying Frequency Modulation Index

The simulation of H-NPC inverter for APOD with three different frequency modulation indices$m_f$; 18, 21 and 24 were carried out. The other parameters that the inverter operates under are voltage DC source $V_{dc} = 100\,V$, amplitude modulation index $m_a = 0.9$ and frequency $f = 50\,Hz$.

The voltage waveform in the phase voltage consists of five voltage levels with 34.63 % as the total harmonic distortion for $m_f = 18$ as shown in Figure 4.21(a). The

harmonic components are centered around $m_f$ and it multiplies $2m_f$ with sideband harmonics surrounding them. The line-line voltage contains nine voltage levels and has 28.41 % THD as the triplen harmonics are absent due to three phase system balance.




(a) Phase Voltage (b) Line-line Voltage

Figure 4.21: Waveform and harmonic contents of H-NPC inverter for $m_f$= 18 (APOD)

The three different frequency modulation indices have the same harmonic characteristic as the harmonic are centered around $m_f$ and it multiplies $2m_f$, $3m_f$ with sideband harmonics surrounding them. The Total Harmonic Distortions (THDs) have small differences as indicated in Table 4.4.

Table 4.4: Frequency Modulation Index $m_f$ vs. THD for APOD

| Frequency Modulation Index $m_f$ | Total Harmonic Distortion THD (%) |
|---|---|
| 18 | 34.63 |
| 21 | 33.04 |
| 24 | 33.88 |

### 4.3 Phase Opposition Disposition (POD) Simulations

The H-NPC inverter is modeled based on the phase opposition disposition (POD) concept of Chapter 3. The modulation sub-system comprises of modulating signal and four carrier signals as shown in Figure 4.22, to generate four gating signals for the switching devices of the H-NPC inverter phase cell. The gating signals of the remaining two phase cells are generated in a similar way with only changing the phase shifting of the modulating signal by 120° and 240° respectively in the cells.

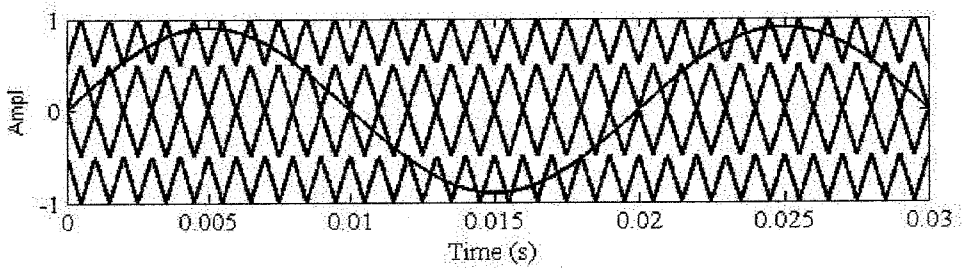



Figure 4.22: Phase opposition disposition (POD)

#### 4.3.1 Simulation results of POD

The phase voltage waveform and its harmonic contents from POD simulation of five-level H-bridge/neutral point clamped is shown in Figures 4.23 and 4.24 respectively. The inverter is simulated under the condition of amplitude modulation index $m_a = 0.9$, frequency $f = 50\,Hz$, DC source voltage $V_{dc} = 100\,V$ and frequency modulation index $m_f = 20$. The phase voltage waveform consists of five levels and has total harmonic distortion at 33.97 %. The harmonics appear to be centered at $m_f$ which is surrounded with sideband harmonics. The least harmonic content is the 3$^{rd}$ order and have triplen harmonic contents such as $(m_f \pm 3)$ and $(2m_f \pm 3)$.

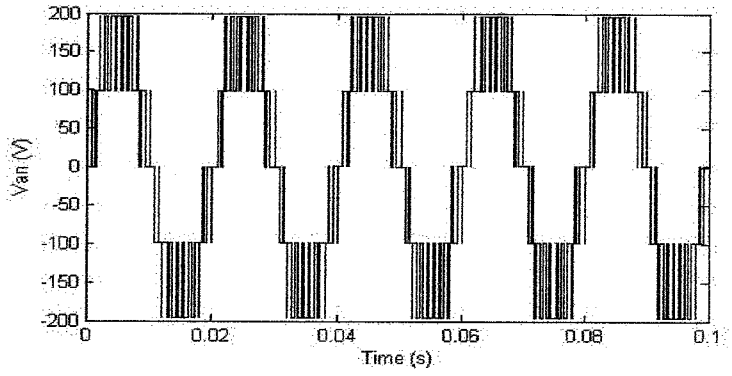



Figure 4.23: Phase voltage of H-NPC inverter using POD

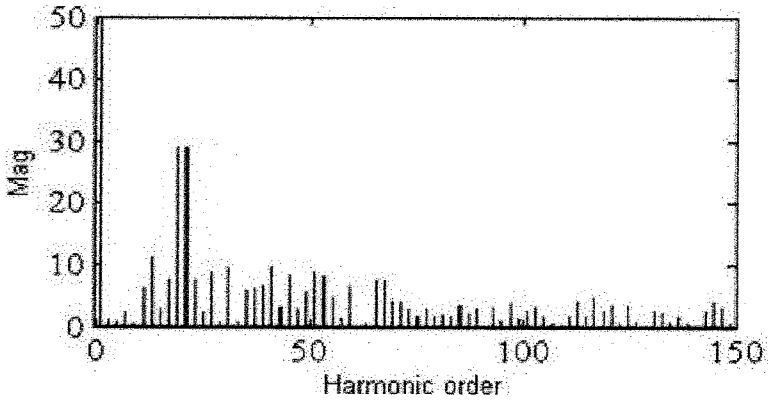



Figure 4.24: Harmonics content of the phase voltage with THD = 33.97 %

Figures 4.25 and 4.26, shows the line-line voltage containing nine voltage levels and its harmonic content with THD of 30.25 %. The THD reduce as result of the cancellation of the triplen harmonics between the two phases due three phase balance system.

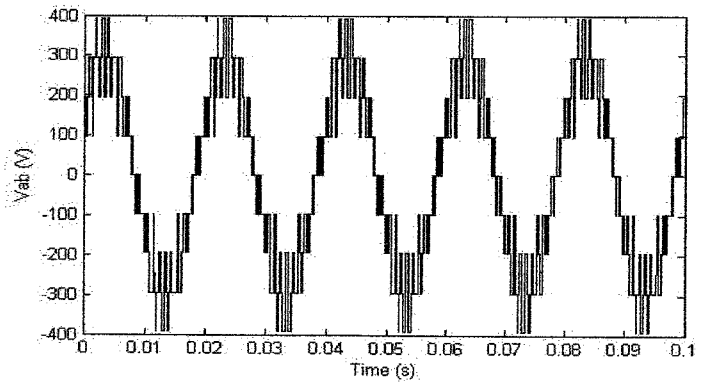



Figure 4.25: Line-line voltage of H-NPC inverter using POD

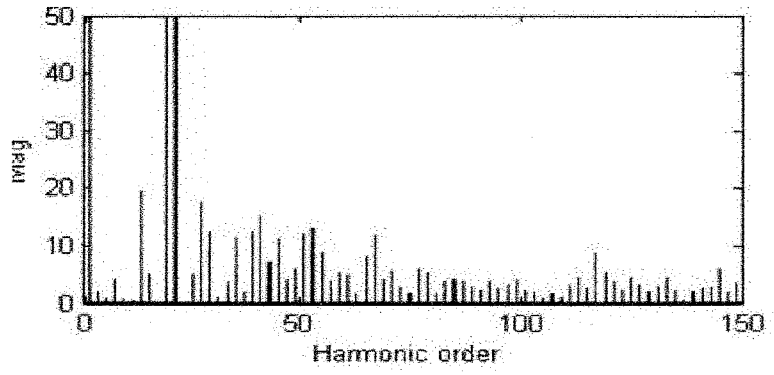
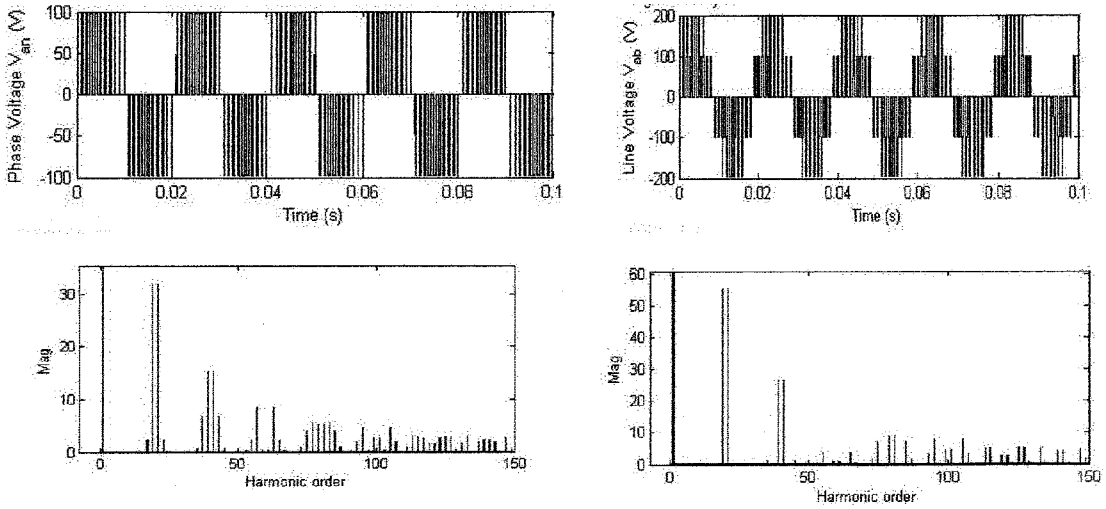



Figure 4.26: Harmonics content of the line-line voltage with THD = 30.25 %

### 4.3.2 Phase Opposition Disposition (POD) with varying Amplitude Modulation Index

The amplitude modulation index $m_a$ is varied in the range of 0.2 – 1.0, while the inverter operates under the conditions; DC source voltage $V_{dc} = 100\,V$, frequency $f = 50\,Hz$ and frequency modulation index $m_f = 20$.

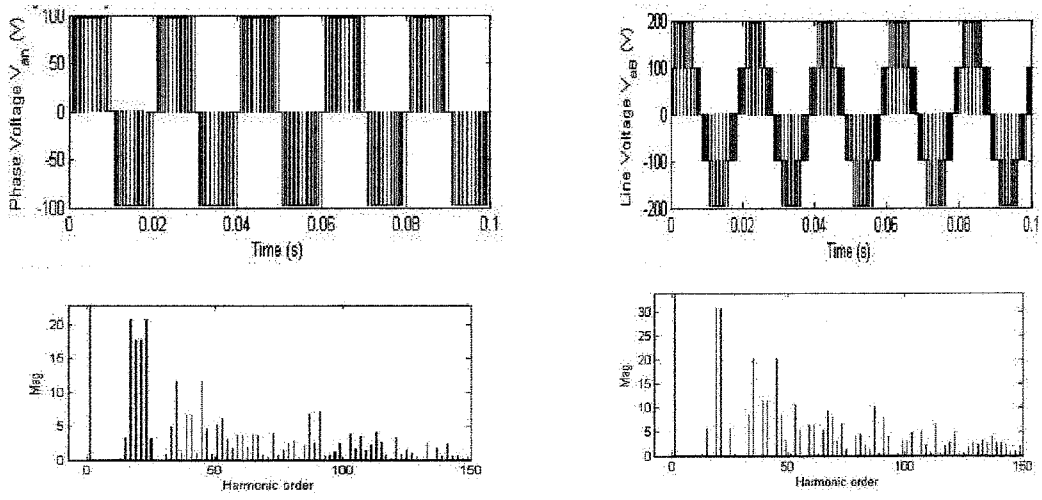
Figure 4.27(a) shows the phase voltage waveform and its harmonic contents for $m_a = 0.2$. The line-line voltage waveform and its harmonic contents are depicted in Figure 4.27b. The waveform of the phase voltage contains three voltage levels with total harmonic distortion (THD) of 146.86 %. The harmonic content to be centered at $m_f$ and it multiplies $2m_f$ with sideband harmonics surrounding them. The THD reduce in the line-line voltage due three phase balance system as the triplen harmonics cancel out between the phases.




(a) Phase Voltage (b) Line-line Voltage

Figure 4.27: Waveform and harmonic contents of H-NPC inverter for $m_a = 0.2$ (POD)

The waveform and harmonic contents for $m_a = 0.5$ is similar to that of $m_a = 0.2$ in which it contains three voltage levels in phase waveform with 52.79 % as the THD as shown in Figure 4.28(a). The THD is reduced to 39.93 % in the line-line voltage due to triplen harmonic cancellation between the phases because of three phase balance system as indicated in Figure 4.28(b).

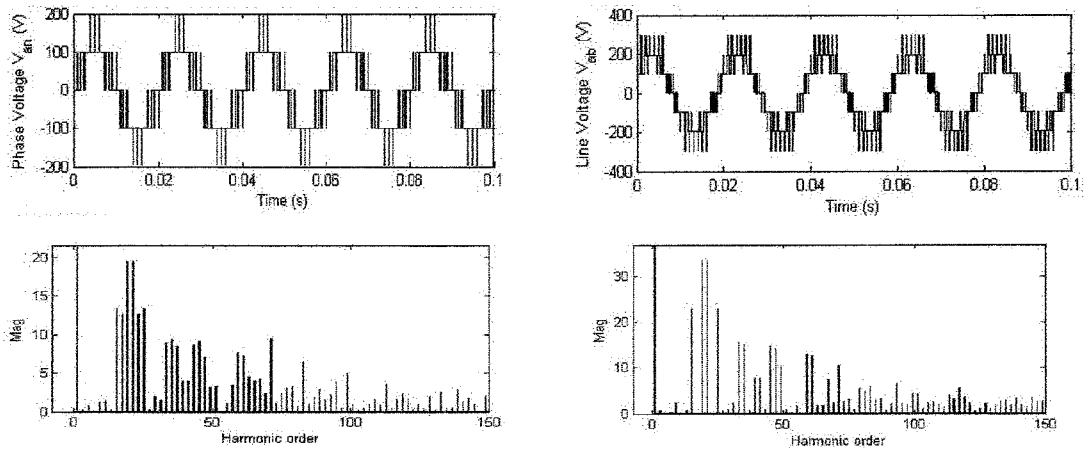



(a) Phase Voltage (b) Line-line Voltage

Figure 4.28: Waveform and harmonic contents of H-NPC inverter for $m_a = 0.5$ (POD)

At $m_a = 0.6$, the phase voltage consists of five voltage levels with 43.65 % THD. The harmonics appear to be centered at $m_f$ and its multiples $2m_f$ which are surrounded with sideband harmonics. The least harmonic content is the 9$^{th}$ order, thus

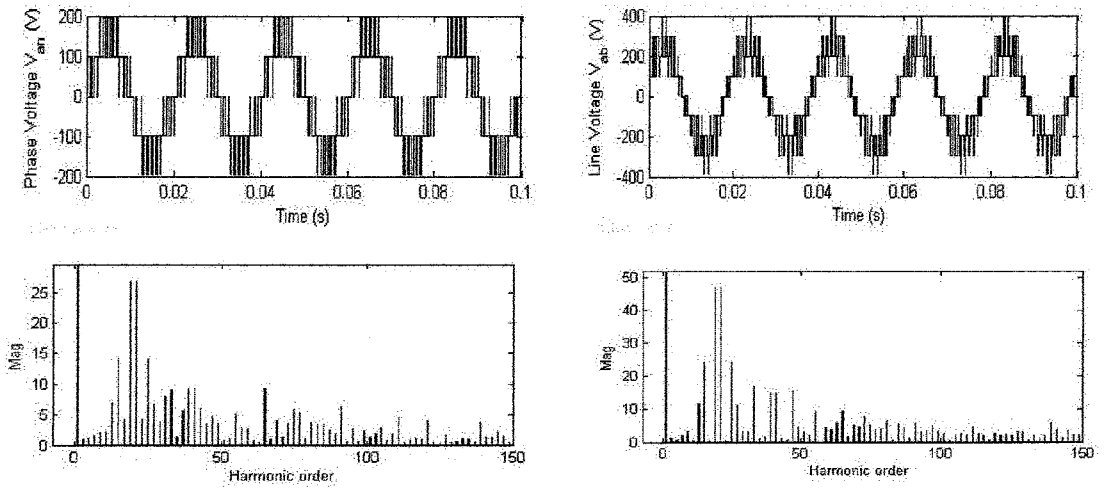
has some additional higher order harmonics than in $m_a = 0.5$ with minimal strength as shown in Figure 4.29(a). Triplen harmonic contents such as $(m_f \pm 3)$ and $(2m_f \pm 3)$ are present in the phase voltage. The line-line voltage contains seven voltage levels with 38.05 % THD.




(a) Phase Voltage (b) Line-line Voltage

Figure 4.29: Waveform and harmonic contents of H-NPC inverter for $m_a = 0.6$ (POD)

At $m_a = 0.7$, the phase voltage consists of five voltage levels with 40.42 % THD. The harmonics appear to be centered at $m_f$ which is surrounded with sideband harmonics. The least harmonic content is the 3rd order, thus has some additional higher order harmonics as in $m_a = 0.6$ with minimal strength as shown in Figure 4.30(a). Triplen harmonic contents such as $(m_f \pm 3)$ and $(2m_f \pm 3)$ are present in the phase voltage. The line-line voltage contains nine voltage levels with 38.05 % THD.




(a) Phase Voltage (b) Line-line Voltage

Figure 4.30: Waveform and harmonic contents of H-NPC inverter for $m_a = 0.7$ (POD)

As shown in the Figures 4.27(a) and 4.28(a), that amplitude modulation index below 0.5 produces waveform that contains three voltage levels in the phase voltage while above 0.5 produces five voltage levels as shown in Figure 4.29(a) and 4.30(a). Figure 4.29(b) shows that the line-line voltage consists of seven voltage levels for $m_a = 0.6$ while Figure 4.30(b) shows that the line-line voltage consists of nine voltage levels for $m_a = 0.7$. The total harmonic distortion THD decreases as the amplitude modulation index increases as given in Table 4.5. Figure 4.31 shows the variation in THDs as amplitude modulation index is varied from 0.2 to 1.0.

Table 4.5: Amplitude Modulation Index $m_a$ vs. THD for POD

| Amplitude Modulation Index $m_a$ | Total Harmonic Distortion THD (%) |
|---|---|
| 0.2 | 146.86 |
| 0.3 | 105.07 |
| 0.4 | 76.06 |
| 0.5 | 51.25 |
| 0.6 | 43.65 |
| 0.7 | 40.42 |
| 0.8 | 37.47 |
| 0.9 | 32.97 |
| 1.0 | 26.29 |

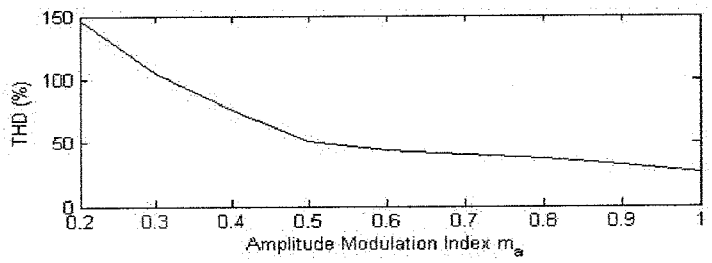
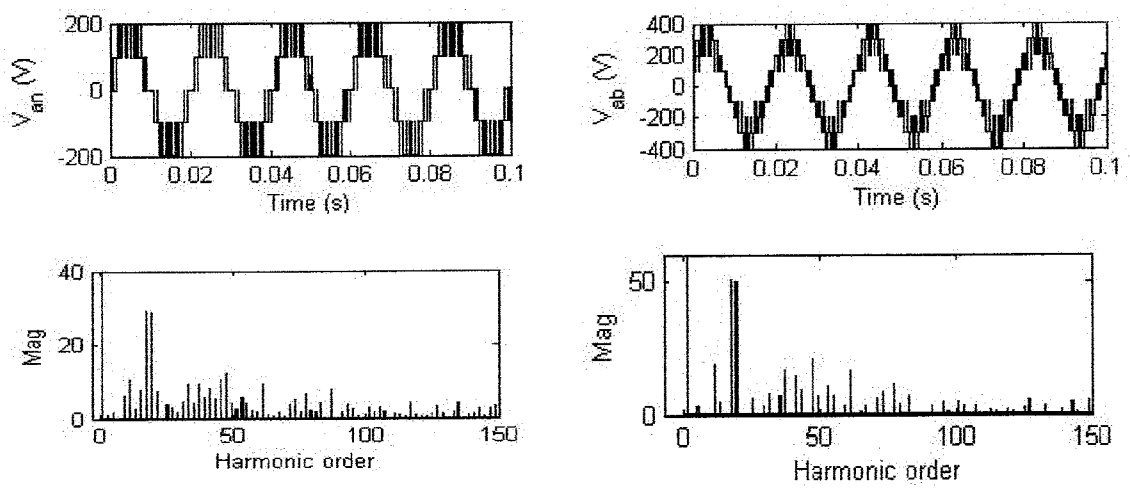



Figure 4.31: THD vs. Amplitude Modulation Index for POD

### 4.3.3 Phase Opposition Disposition (POD) with varying Frequency Modulation Index

The simulation of H-NPC inverter for POD with three different frequency modulation indices $m_f$; 18, 21 and 24 were carried out. The other parameters that the inverter operates under are voltage DC source $V_{dc} = 100\,V$ amplitude modulation index $m_a = 0.9$ and frequency $f = 50\,Hz$.

The voltage waveform in the phase voltage consists of five voltage levels with 32.73 % as the total harmonic distortion for $m_f = 18$ as shown in Figure 4.32(a). The harmonic components are centered on $m_f$ with sideband harmonics surrounding them. The line-line voltage contains nine voltage levels and has 29.48 % THD as the triplen harmonics are absent due to three phase system balance.




(a) Phase Voltage (b) Line-line Voltage

Figure 4.32: Waveform and harmonic contents of H-NPC inverter for $m_f$ = 18 (POD)

The three different frequency modulation indices have the same harmonic characteristic as the harmonic are centered on $m_f$ with sideband harmonics surrounding it. The total harmonic distortions (THDs) have small differences as indicated in Table 4.6.

Table 4.6: Frequency Modulation Index $m_f$ vs. THD for POD

| Frequency Modulation Index $m_f$ | Total Harmonic Distortion THD (%) |
|---|---|
| 18 | 34.63 |
| 21 | 33.04 |
| 24 | 33.88 |

### 4.4 Phase Disposition (PD) Simulations

The H-NPC inverter is modeled based on the phase disposition (PD) concept of Chapter 3. The modulation sub-system comprises of modulating signal and four carrier signals as shown in Figure 4.33, to generate four gating signals for the switching devices of the H-NPC inverter phase cell. The gating signals of the remaining two phase cells are generated in a similar way with only changing the phase shifting of the modulating signal by 120° and 240° respectively in the cells.

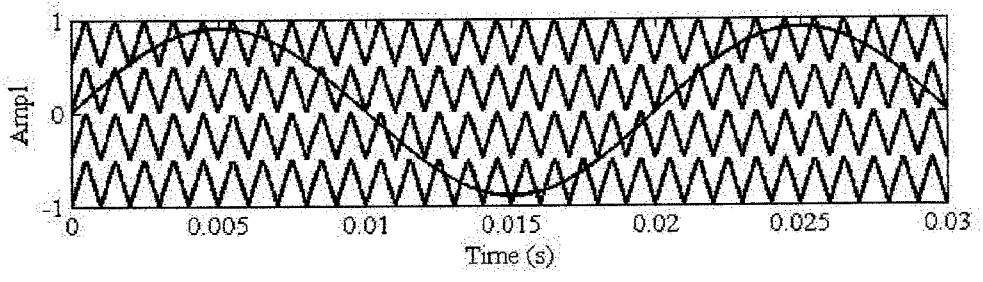



Figure 4.33: Phase disposition (PD)

### 4.4.1 Simulation results of PD

The phase voltage waveform and its harmonic contents from PD simulation of five-level H-bridge/neutral point clamped are shown in Figures 4.23 and 4.24 respectively. The inverter is simulated under the condition of amplitude modulation index $m_a = 0.9$, frequency $f = 50\,Hz$, DC source voltage $V_{dc} = 100\,V$ and frequency modulation index $m_f = 20$. The phase voltage waveform consists of five levels and has total harmonic distortion at 33.27 %. The first harmonics appear to be the most significant harmonic component. Harmonic energy is placed mostly into carrier component of phase cell.

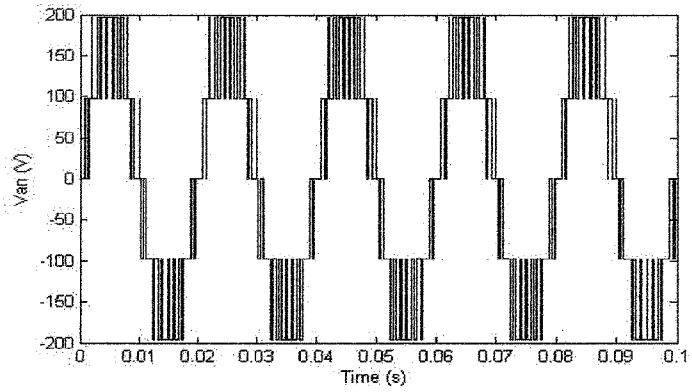



Figure 4.34: Phase voltage of H-NPC inverter using PD

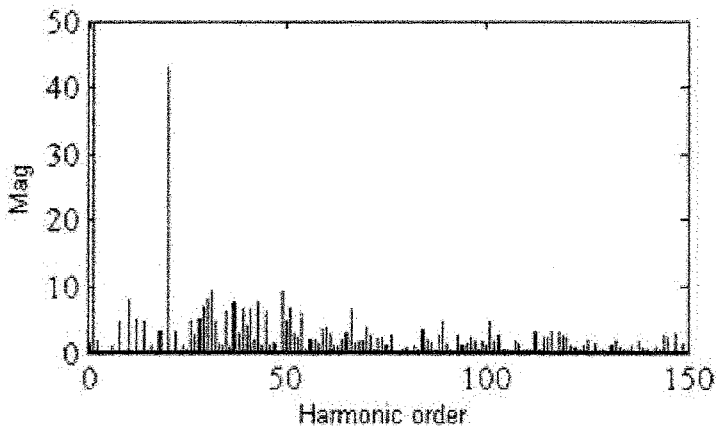



Figure 4.35: Harmonics content of the phase voltage with THD = 33.27 %

Figures 4.36 and 4.37, shows the line-line voltage containing nine voltage levels and its harmonic content with THD of 17.40 %. The THD reduce as result of the common-mode cancellation of the carrier harmonics between the two phases due three phase balance system.

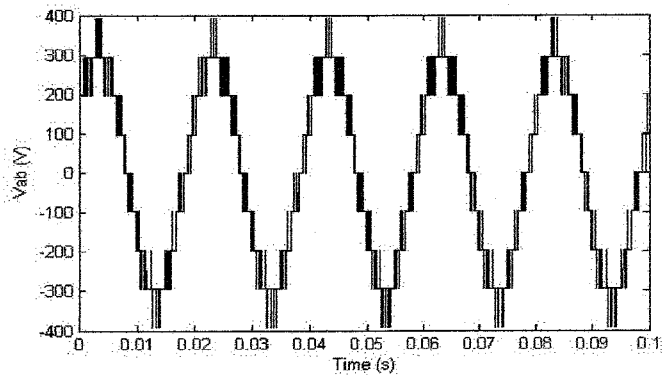



Figure 4.36: Line-line voltage of H-NPC inverter using PD

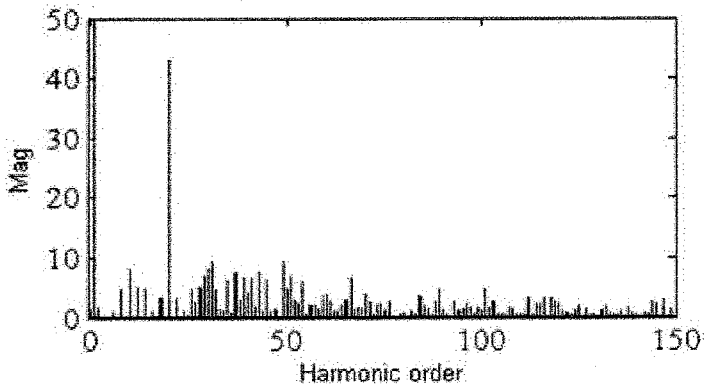


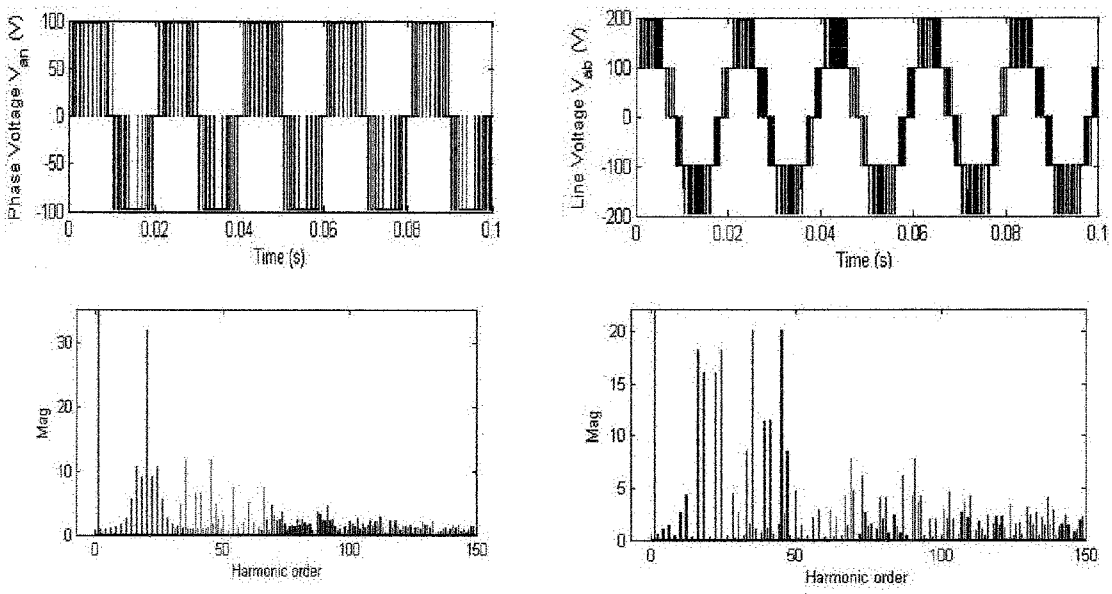

Figure 4.37: Harmonics content of the line-line voltage with THD = 17.40 %

### 4.4.2 Phase Disposition (PD) with varying Amplitude Modulation Index

The amplitude modulation index $m_a$ is varied in the range of 0.2 – 1.0, while the inverter operates under the conditions; DC source voltage $V_{dc} = 100\ V$, frequency $f = 50\ Hz$ frequency modulation index $m_f = 20$.

Figure 4.38(a) shows the phase voltage waveform and its harmonic contents for $m_a = 0.5$. The line-line voltage waveform and its harmonic contents are depicted

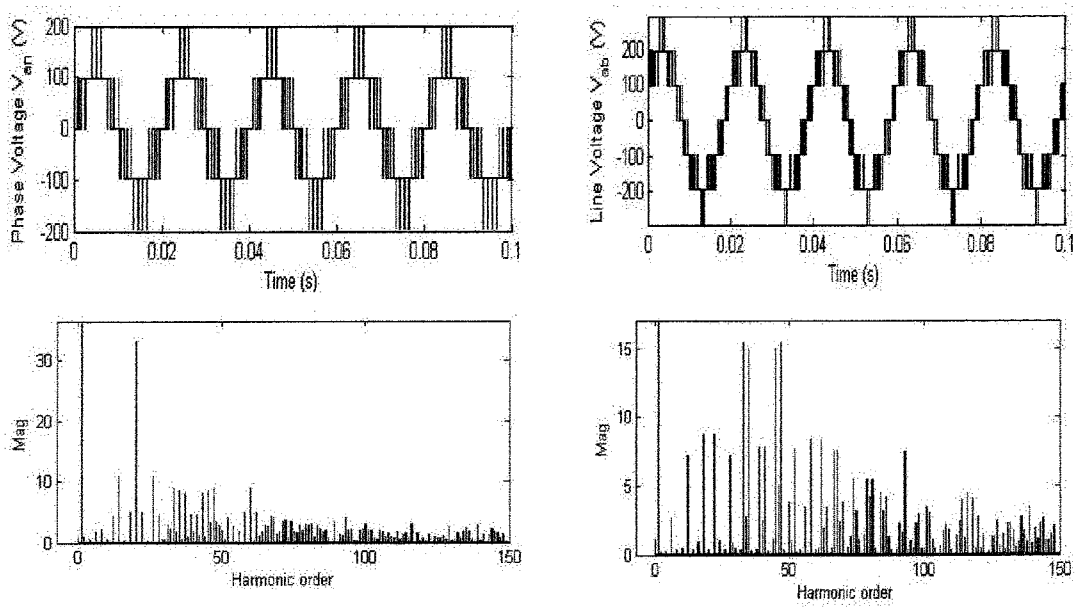
in Figure 4.38(b). The waveform of the phase voltage contains three voltage levels with total harmonic distortion (THD) of 147.50 %. The first harmonics appear to be the most significant harmonic component. Harmonic energy is placed mostly into carrier component of phase cell. The THD reduce as result of the common-mode cancellation of the carrier harmonics between the two phases due three phase balance system.




(a) Phase Voltage (b) Line-line Voltage

Figure 4.38: Waveform and harmonic contents of H-NPC inverter for $m_a$ = 0.5 (PD)

At $m_a$ = 0.6, the phase voltage consists of five voltage levels with 44.32 % THD. The first harmonics appear to be the most significant harmonic component. Harmonic energy is placed mostly into carrier component of phase cell as shown in Figure 4.39(a). The line-line voltage contains seven voltage levels with 25.48 % THD as shown in Figure 6.39(b).




(a) Phase Voltage (b) Line-line Voltage

Figure 4.39: Waveform and harmonic contents of H-NPC inverter for $m_a = 0.6$ (PD)

As shown in the Figure 4.38(a) that amplitude modulation index below 0.5 produces waveform that contains three voltage levels in the phase voltage while above 0.5 produces five voltage levels as shown in Figure 4.39(a). Figure 4.39(b) shows that the line-line voltage consists of seven voltage levels for $m_a = 0.6$ while Figure 4.36 shows that the line-line voltage consists of nine voltage levels for $m_a = 0.9$. The total harmonic distortion THD decreases as the amplitude modulation index increases as given in Table 4.7. Figure 4.40 shows the variation in THDs as amplitude modulation index is varied from 0.2 to 1.0.

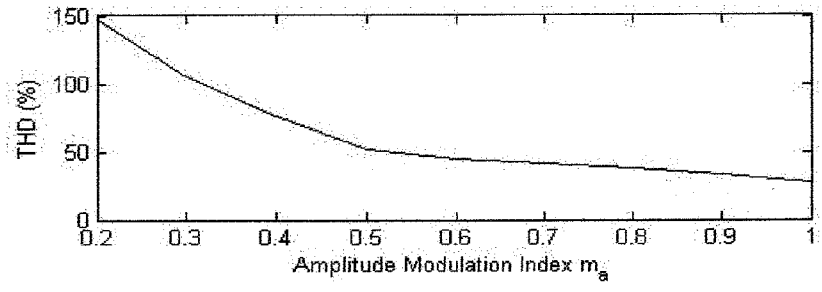



Figure 4.40: THD vs. Amplitude Modulation Index for PD

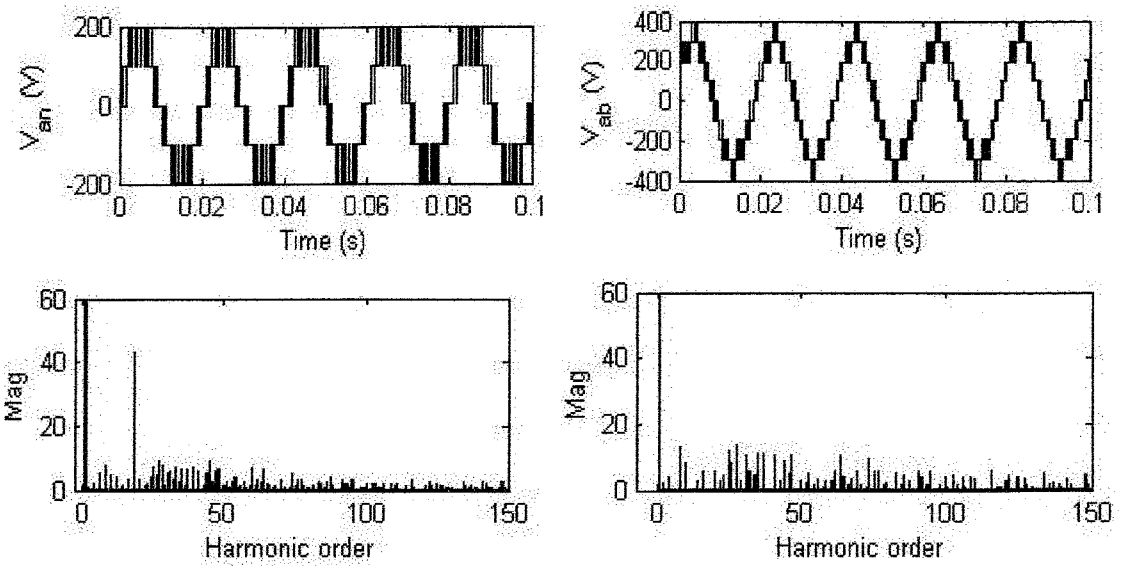
Table 4.7: Amplitude Modulation Index $m_a$ vs. THD for PD

| Amplitude Modulation Index $m_a$ | Total Harmonic Distortion THD (%) |
|---|---|
| 0.2 | 147.50 |
| 0.3 | 105.71 |
| 0.4 | 76.71 |
| 0.5 | 52.05 |
| 0.6 | 44.32 |
| 0.7 | 41.42 |
| 0.8 | 38.21 |
| 0.9 | 33.27 |
| 1.0 | 26.82 |

### 4.4.3 Phase Disposition (PD) with varying Frequency Modulation Index

The simulation of H-NPC inverter for PD with three different frequency modulation indices $m_f$; 18, 21 and 24 were carried out. The other parameters that the inverter operates under are voltage DC source $V_{dc} = 100\,V$ amplitude modulation index $m_a = 0.9$ and frequency $f = 50\,Hz$ .

The voltage waveform in the phase voltage consists of five voltage levels with 33.34 % as the total harmonic distortion for $m_f = 18$ as shown in Figure 4.41(a). The first harmonics appear to be the most significant harmonic component. The line-line voltage contains nine voltage levels and has 17.46 % THD.




(a) Phase Voltage (b) Line-line voltage

Figure 4.41: Waveform and harmonic contents of H-NPC inverter for $m_f$ = 18 (PD)

Table 4.8: Frequency Modulation Index $m_f$ vs. THD for PD

| Frequency Modulation Index $m_f$ | Total Harmonic Distortion THD (%) |
|---|---|
| 18 | 34.34 |
| 21 | 32.99 |
| 24 | 33.42 |

## 4.5 Comparisons of the SPWM Technique

The vertical shift-level SPWM techniques varied in orientation of their carrier signals. The four SPWM techniques are compared based on the following criteria; harmonic suppression, total harmonic distortion (THD) reduction, high voltage attainment and effect of variation in amplitude modulation index.

### 4.5.1 Harmonic Suppression

The IPD has the best harmonic suppression among the four SPWM techniques. In Figure 4.3, it can be seen that the least harmonic component for IPD is the $33^{rd}$ harmonic order against the $11^{th}$ harmonic order of the APOD as shown in Figure 4.12 and the $3^{rd}$ harmonic order of both POD and PD as shown in Figures 4.23 and 4.34 respectively under the same simulation conditions. In IPD, the harmonic are pushed to higher order where they are centered at $2m_f$ and it multiples $4m_f$ with sideband harmonic surrounding them. This spectrum pattern is retained for different modulation index.

### 4.5.2 Total Harmonic Distortion Reduction

The PD has the best THD reduction in the line-line voltage as shown in Figure 4.37 with 17.40 % THD. This is as the result of placing much energy in the carrier components of the phase cell which used common-mode to cancel out between the two phase voltages. The APOD and IPD have approximately the same results of 33.46 % and 33.29 % in the phase voltage respectively. The line-line voltage THD of APOD is 29.00 % and that of IPD is 28.69 %. APOD and IPD have better THD reduction than POD in the line-line voltage which had 30.25 %. This is as result of more energy is placed in the triplen harmonic order in APOD and IPD than in POD. The triplen harmonics are cancel out in the line-line voltage due to three phase balance system.

### 4.5.3 High Voltage Attainment

IPD attain both the five and nine voltages in the phase and line-line voltage respectively at $m_a$= 0.6 as shown in Figure 4.8. APOD and POD attain the five voltage levels at $m_a$= 0.6 but with seven voltage levels in the line-line voltage as depicted in Figure 4.18 and 4.29. The nine voltage levels is attained at $m_a$= 0.7 as shown in Figure 4.19 and 4.30. PD attained the nine voltage levels at $m_a$= 0.9 as depicted in Figure 4.36. This shows that the voltage level raises more in IPD with increase in the

amplitude modulation index $m_a$ than in APOD and POD. PD has the least in the raise of the voltage level compared to other three.

### 4.5.4 Effect of Amplitude Modulation Index Variation

The four SPWM techniques have almost similar phase voltage THD characteristics has the amplitude modulation index is varied from 0.2 – 1.0 as depicted in Figure 4.42 which is the compositions of the THD vs. amplitude modulation index of Figures 4.9, 4.20, 4.31 and 4.40.

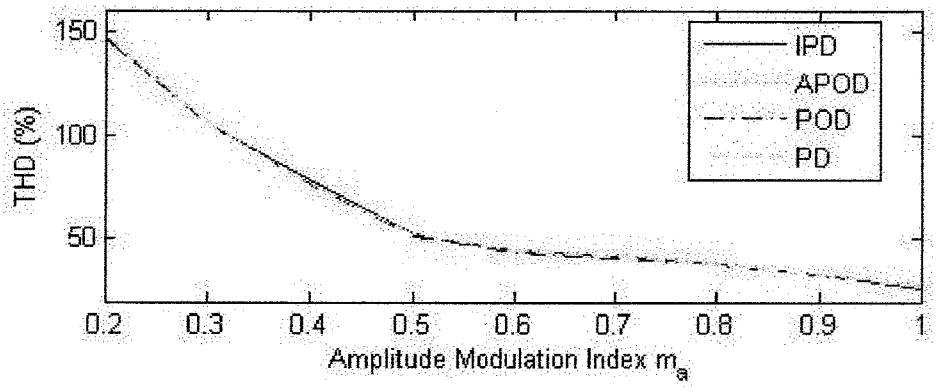



Figure 4.42: THD vs. Amplitude Modulation Index for All the SPWM techniques

## 4.6 Summary

This chapter has discussed the results of the SPWM techniques applied on five-level H-bridge/ neutral point clamped (H-NPC) inverter. In the first four sections, a section is dedicated to the simulation and analysis of each of the SPWM technique. The fifth section compares the simulation results of the SPWM techniques based on harmonic suppression, total harmonic distortion (THD) reduction, high voltage attainment and effect of variation in amplitude modulation index.

# CHAPTER 5

# CONCLUSIONS

In this final chapter, all the materials presented in the research work on sinusoidal pulse width modulation and multilevel inverter related to the H-bridge/neutral point clamped inverter is given. Analysis of the results obtained in this thesis based on the stated objectives is discussed by highlighting the achievement of the research work. This is followed by some suggestions for future work.

## 5.1 Evaluation of Achievement

This thesis addressed the issues of modeling effective sinusoidal pulse width modulation (SPWM) controllers for five-level H-bridge/neutral point clamped (H-NPC) inverter to achieve high voltage output with minimum harmonic distortion in output waveform.

To strengthen the research, a thorough literature review of the multilevel inverter topologies and different modulation techniques was presented in Chapter 2 where several aspect of multilevel inverter such as neutral point clamped (NPC) inverter, flying capacitors inverter, cascaded inverter, pulse width modulation, space vector were presented.

Chapter 3 gives the system operation of H-bridge / neutral point clamped inverter and modeling of sinusoidal pulse width modulation such as alternate phase opposition disposition (APOD), phase opposition disposition (POD) and in-phase disposition (IPD). This is followed by discussion on the simulation work in Chapter 4 using SPWM techniques. The performance of SPWM techniques on the five-level H-NPC inverter based on the Total Harmonic Distortion (THD), high voltage attainment as the amplitude modulation index is varied were discussed.

In this research work, the complete modeling of the four SPWM techniques has been derived. It could be concluded that IPD has the best performance in term of harmonic suppression and high voltage attainment at low amplitude modulation index. The lowest harmonic component is the $33^{rd}$ harmonic order for IPD against the $11^{th}$ of the APOD and the $3^{rd}$ harmonic order for both POD and PD. IPD attain both five voltage levels for the phase voltage and nine voltage levels for the line-line voltage at 0.6 amplitude modulation index, while APOD and POD attain the five voltage levels for the phase voltage and nine voltage levels for the line – line voltage at 0.7 amplitude modulation index. PD attain at 0.9 amplitude modulation index.

In term of total harmonic distortion reduction, PD has the best performance among SPWM technique with 17 % THD for the line-line voltage waveform at 0.9 amplitude modulation index against 28.69 % of IPD, 29.00 % of APOD and 30.25 % of the POD. The response of the four SPWM techniques over the amplitude modulation index range of 0.2 – 1.0 show similar trend in the decrease in the total harmonic distortion as the amplitude modulation index increases. The overall results demonstrate the effectiveness of the SPWM techniques.

## 5.2 Suggestions for Future Work

In this section, few suggestions for further research are given.

**a) Study of heat loss due to switching**

Further work could be explored by studying the effect of heat loss as result of the high frequency used in the SPWM techniques. Less loss in heat gives high efficiency.

**b) Prototype Development**

The SPWM techniques could be tested in a prototype. A digital circuit like FPGA or DSP could be used to implement the SPWM schemes, so that the results of the output waveform, harmonic reduction and suppression can be compared with the analysis of Chapter 4.

## LIST OF PUBLICATIONS


[1] I. Mahmud, I. Ismail and N. Z. Yahaya, "A Comparative Study of SPWM on A 5-Level H-NPC Inverter," *Res. J. App. Sci. Eng. Tech.*, to be published.

[2] I. Mahmud, I. Ismail and N. Z. Yahaya, "A Review on H-bridge/Neutral Point Clamped Inverter," submitted for publication.

[3] I. Mahmud, I. Ismail and N. Z. Yahaya, "Sinusoidal Pulse Width Modulation (SPWM) Technique: H-NPC Inverter," submitted for publication.

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# APPENDIX A:

# MATLAB/SIMULINK MODEL OF H-NPC INVERTER

1. Simulink model of In-phase Disposition (IPD)

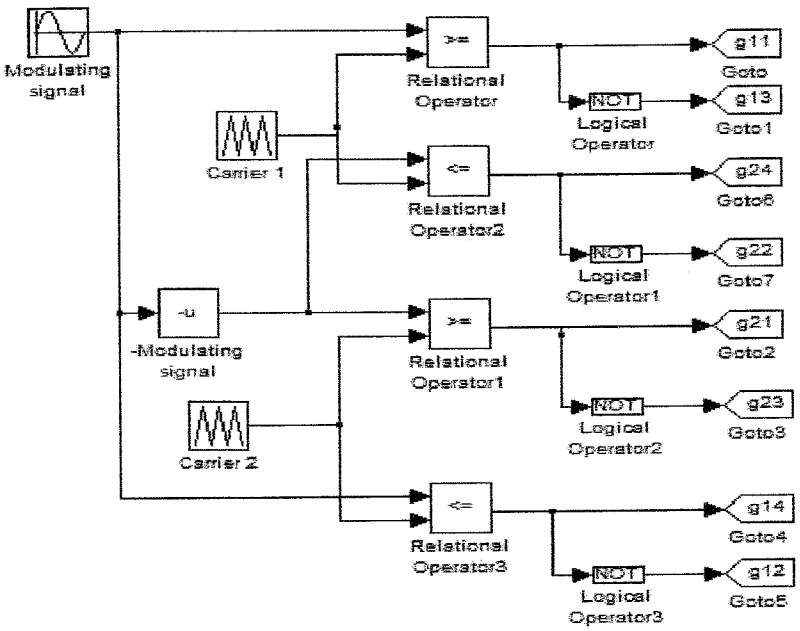


Figure A.5.1: Simulink model of In-phase Disposition (IPD)

2. Simulink model of Alternate Phase Opposition Disposition (APOD)

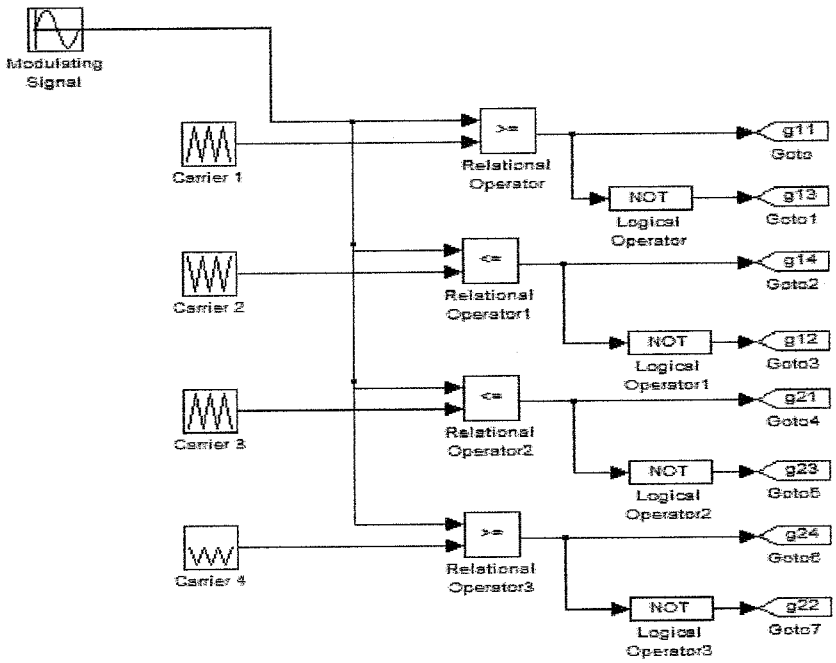


Figure A 5.2: Simulink model of Alternate Phase Opposition Disposition (APOD)

3. Simulink model of Phase Opposition Disposition (POD)

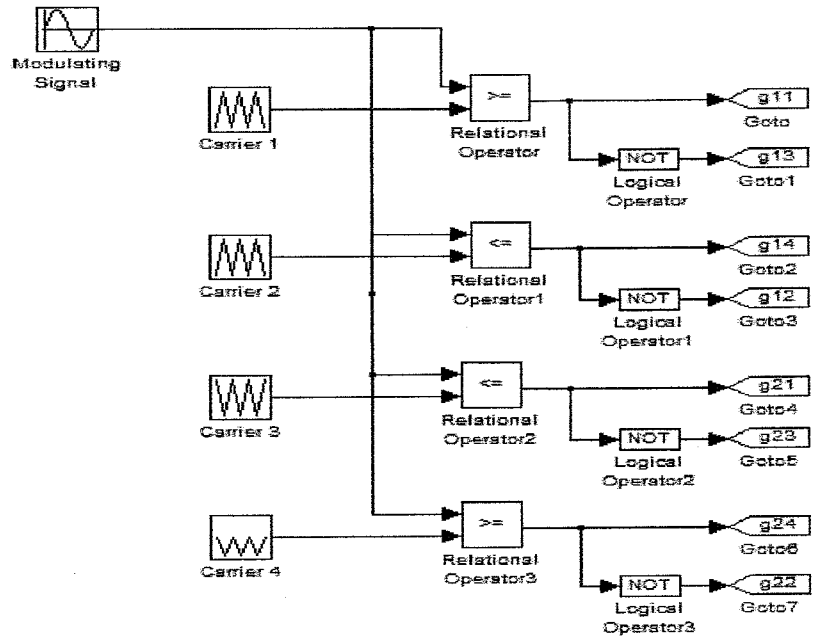


Figure A.5.3: Simulink model of Phase Opposition Disposition (POD)

4. Simulink model of Phase Disposition (PD)

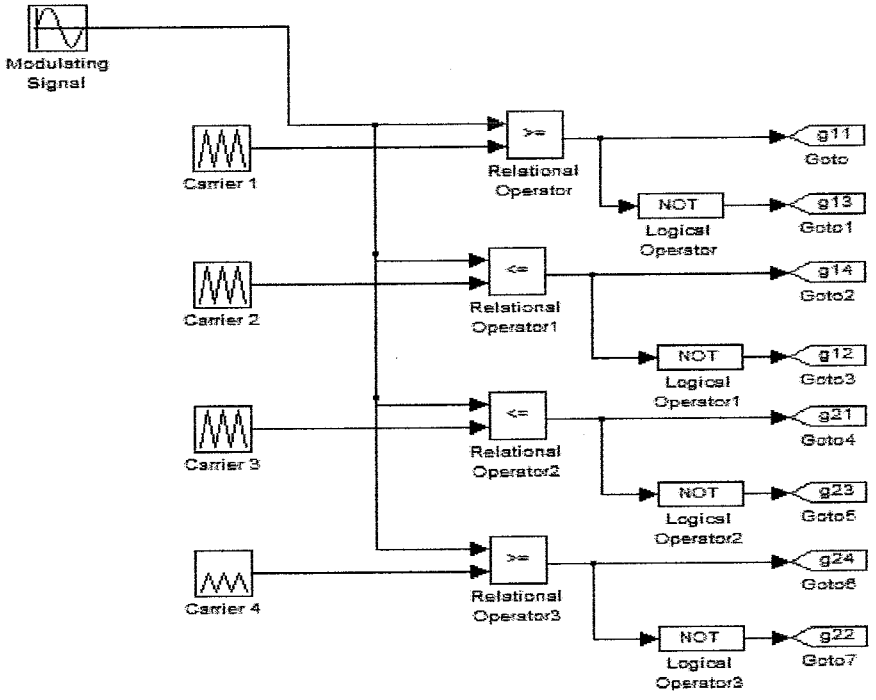


Figure A.5.4: Simulink model of Phase Disposition (PD)

5. Simulink model of a phase unit of H-NPC inverter

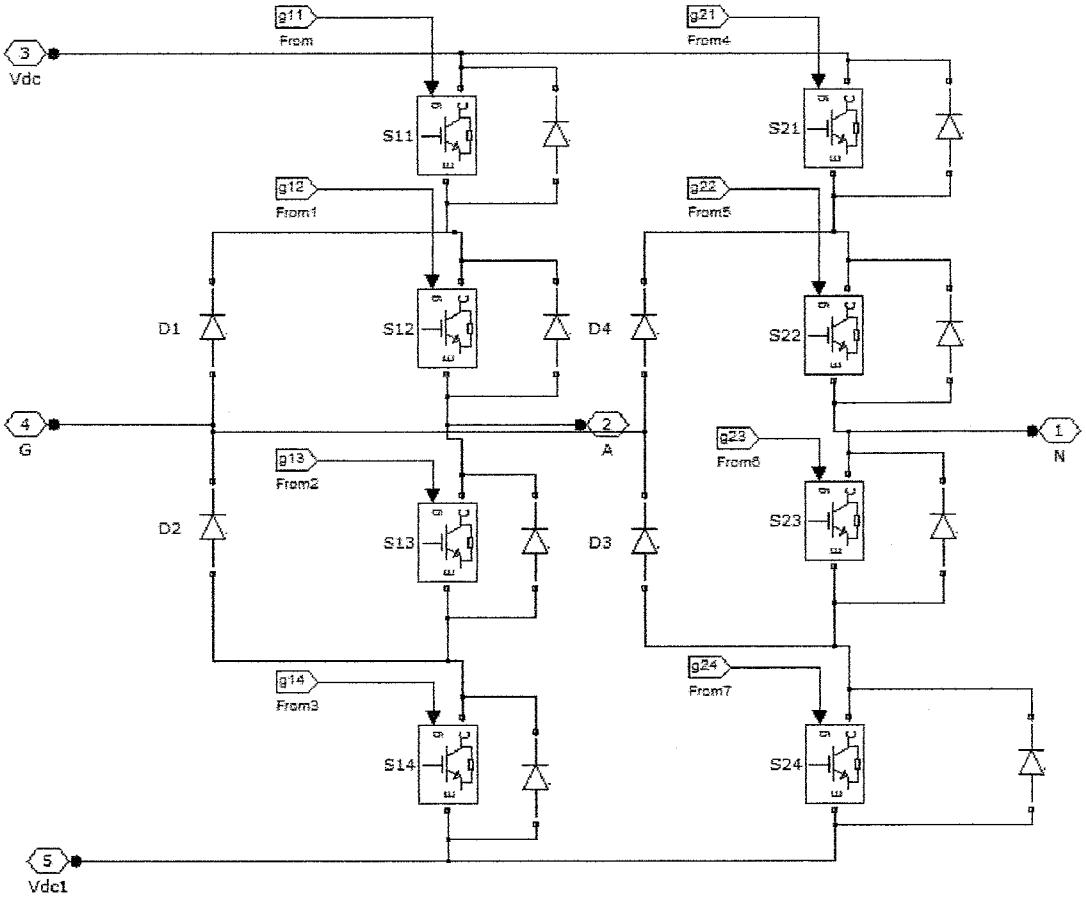


Figure A.5.5: Simulink model of a phase unit of H-NPC inverter

6. Simulink model of five-level H-NPC inverter

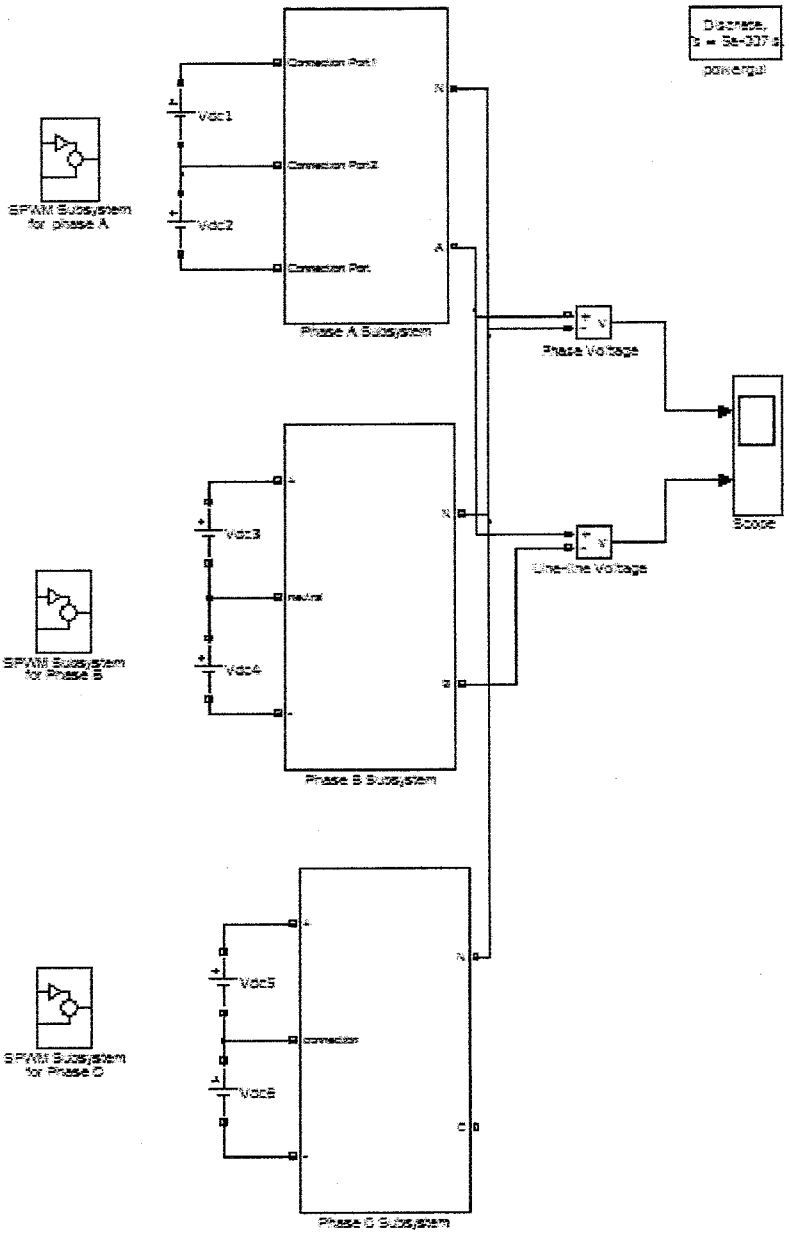


Figure A.5.6: Complete Simulink model of five-level H-NPC inverter