



UNIVERSITI
TEKNOLOGI
PETRONAS

FINAL EXAMINATION JANUARY 2023 SEMESTER

COURSE : TFB1053 - COMPUTER SYSTEMS
DATE : 12 APRIL 2023 (WEDNESDAY)
TIME : 9:00 AM - 12:00 NOON (3 HOURS)

INSTRUCTIONS TO CANDIDATES

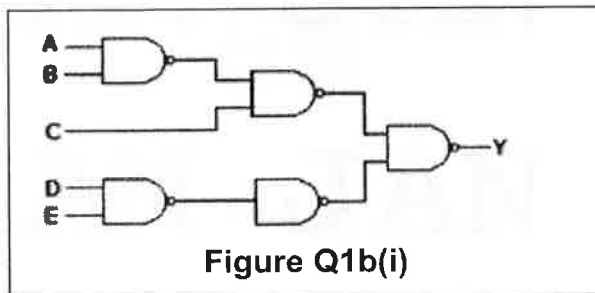
1. Answer **ALL** questions in the Answer Booklet.
2. Begin **EACH** answer on a new page in the Answer Booklet.
3. Indicate clearly answers that are cancelled, if any.
4. Where applicable, show clearly steps taken in arriving at the solutions and indicate **ALL** assumptions, if any.
5. **DO NOT** open this Question Booklet until instructed.

Note :

- i. There are **EIGHT (8)** pages in this Question Booklet including the cover page .
- ii. **DOUBLE-SIDED** Question Booklet.

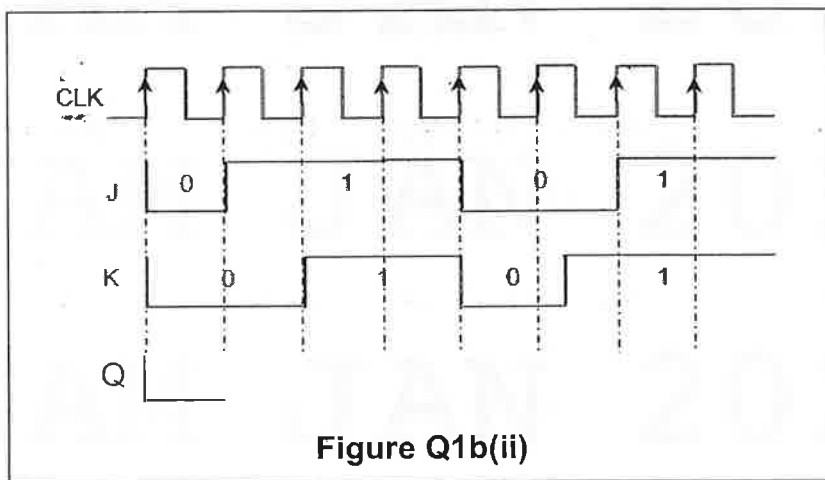
1. a. List **THREE (3)** main components in Central Processing Unit (CPU).
[3 marks]

- b. i. Given the logic circuit diagrams in **Figure Q1b(i)**. Derive the expression for Y in the simplest form. Show your work.



[3 marks]

- ii. Given the timing diagram for a JK Flip Flop in **Figure Q1b(ii)**. Draw the waveform for the output Q (Continue from the initial waveform given).



[3 marks]

- c. Draw the memory hierarchy diagram and describe the differences between various memory types in terms of size, speed, and cost.

[6 marks]

- d. Suppose we are considering an enhancement to the processor of a web server. The new Central Processing Unit (CPU) is 20 times faster on search queries than the old processor. The old processor is busy with search queries 70% of the time. Compute the speedup gained by integrating the enhanced CPU. Show your work.

[5 marks]

2. a. Convert the hexadecimal numbers in **Table Q2(a)** below into binary, octal, and decimal equivalent. Assume all are unsigned numbers.

Table Q2(a)

Hexadecimal number	Equivalent Binary number	Equivalent Octal number	Equivalent Decimal number
A10			
15.A8			

[6 marks]

- b. Convert the decimal numbers in **Table Q2(b)** below into 2's complement representation in binary and hexadecimal format.

Table Q2(b)

Decimal number	Binary equivalent	Hexadecimal equivalent
-138.625		
31.6875		

[4 marks]

- c. Assume 8-bit number system that uses 2's complement technique, compute the addition of two numbers given in **Table 2(c)** below. Indicate whether overflow occurs or not with Yes or No respectively.

Table Q2(c)

Number 1	Number 2	Overflow occur?	Result of Addition
01011100	01001110		
10100100	10110010		
01011100	10110010		

[6 marks]

- d. Determine the range of signed numbers that can be represented in 6 bits system using one's complement.

[4 marks]

3. a. Fill in the blanks in **FIGURE 3Q** to develop a program in Little Man Computer (LMC) Assembly Language for displaying the maximum number from a series of 0 or positive numbers entered by the user. Whenever a ZERO (0) is entered, the program will stop and display the maximum number. Assume negative numbers will not be entered.

	INP
	STA MAX
	BRZ STOP
LOOP	INP

	BRA LOOP
STOP	_____

MAX	DAT
NUM	DAT

Figure 3Q

[10 marks]

- b. List the **FIVE (5)** main steps performed by LMC for the ADD instruction in the Fetch and Execute phases. Use PC, MDR, IR, A for Accumulator register, etc. in describing the steps.

[5 marks]

- c. Describe the operations of Indirect Addressing Mode and Register Indirect Addressing Mode by drawing their Instruction formats and relationship with memory location or register content.

[5 marks]

4. Consider the memory map and events of processes in **FIGURE Q4** for a computer system that uses Dynamic Partitioning Memory Management.

P1		
<free> 30 K		
P2		
<free> 20 K		
P3		
<free> 50 K		
P4		

Step	Event	Required contiguous Memory size (K)
1	Process 5 arrives	16
2	Process 6 arrives	40
3	Process 7 arrives	20
4	Process 8 arrives	14
5	Process 5 leaves	-
6	Process 9 arrives	30

Figure Q4

- a. For each memory allocation techniques in First-fit, Best-fit, and Worst-fit, WITHOUT compaction, draw the memory map after event of step 4 has completed but before event of step 5 occurs.
- [6 marks]
- b. For each memory allocation techniques in First-fit, Best-fit, and Worst-fit, WITH compaction, draw the memory map after event of step 6 has completed (starting from step 1 again).
- [6 marks]
- c. Suppose the computer system uses the Paging Memory management with Associative registers.
- i. Explain how the logical addresses are translated to physical addresses.
- [4 marks]
- ii. Calculate the Effective memory access time if Associative register access time is 50 nanosec, memory access time is 250 nanosec, and hit ratio is 80%.
- [4 marks]

5. a. Based on **TABLE Q5(a)**, compute the average waiting time and average turnaround time for Round Robin with a time quantum of 4, and Shortest Remaining Time CPU Scheduling algorithms.

TABLE Q5(a)

Job Number	Arrival Time (ms)	CPU Cycle (ms)
1	0	10
2	1	2
3	2	3
4	3	1
5	4	5

[8 marks]

- b. Suppose a hard disk cylinder has five tracks, numbered 0 through 4 and each track contains five sectors also numbered 0 through 4. If it takes 5 msec to move the read/write head from one track to the next, 5 msec to rotate, and 1 msec to transfer data, calculate the seek time, search time, and transfer time for the Request List given in **Table Q5(b)**.

Table Q5(b)

Track	Sector
1	0
2	4
2	2
3	4
2	0
3	3
4	4
0	2

[6 marks]

c. Describe the advantages and disadvantages of the following File storage techniques:

i. Contiguous

[2 marks]

ii. Noncontiguous

[2 marks]

iii. Indexed

[2 marks]

– END OF PAPER –