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UNIVERSITI TEKNOLOGI PETRONAS

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UNIVERSITI TEKNOLOGI PETRONAS

IMPROVEMENT OF POWER QUALITY BY SHUNT ACTIVE POWER FILTER IN A THREE-PHASE FOUR-WIRE DISTRIBUTION SYSTEM

By

IZZELDIN IDRIS ABDALLA YAGOUBE

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I would like to dedicate my thesis to my beloved parents
who taught me that knowledge is the key to success.

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ABSTRACT

Power quality disturbances such as harmonics, power factor and neutral conductor current in a distribution network are the major concern as utilities are moving forward to a Smart Grid. Power quality for the digital economy in a Smart Grid distribution system is a priority with a variety of quality/price options. Meanwhile, the impact of renewal sources of energy like solar, wind, wave etc., which mainly use power electronic controllers and integrated into the Smart Grid cause increased power quality problems. The main source for high current harmonics, low power factor and excessive neutral current are high power mixed non-linear loads. International standards on power quality impose a maximum limit on Total Harmonic Distortion (THD) of 5 %. In addition the power factor is to be unity and the neutral conductor current is close to zero. In many applications the electrical power is distributed through three-phase four-wire system and as a result high neutral conductor current is produced in addition to the generation of current harmonics. The presence of harmonics in the distribution lines results in greater power losses, interference with communication lines and failure of operation of sensitive equipment. A reliable and cost-effective solution to power quality disturbances is active power filtering. This thesis addresses the above issues by using two-level, five-level and seven-level three-phase four-wire Shunt Active Power Filter (SAPF) in industrial distribution network to minimize the neutral current and to mitigate the current harmonics. The line-currents which have to be injected by SAPF are shaped by controlling the two-level and multilevel Voltage Source Inverter (VSI) based SAPF. In order to control the VSI, the reference signals are computed by using three proposed control schemes based on *p-q* theory, *d-q-0* theory and *a-b-c* theory. MATLAB/SIMULINK is used as a simulation tool to develop the power system models for dynamic simulation. The proposed control schemes for SAPF are analyzed and applied to three-phase four-wire system to compensate for harmonic source currents, correcting the power factor of the supply side near to unity and to improve the source current THD within the prescribed limit of 5 % as recommended by IEEE-519 standards.

ABSTRAK

Gangguan kualiti kuasa seperti harmonik, faktor kuasa dan arus pengalir neutral merupakan kebimbangan bagi utiliti kerana kebanyakan ke arah grid pintar. Kualiti kuasa untuk ekonomi digital dalam sistem pengagihan Grid Pintar adalah satu keutamaan dengan pelbagai pilihan kualiti / harga. Sementara itu, kesan daripada pembaharuan sumber tenaga seperti solar, angin, ombak dan lain-lain, yang kebanyakannya menggunakan alat kawalan kuasa elektronik dan bersepadu ke dalam Grid Pintar akan menambahkan masalah kualiti kuasa. Gangguan kualiti kuasa seperti harmonik, faktor kuasa dan arus neutral dalam rangkaian pengedaran adalah kebimbangan utama kepada utiliti dan pelanggan. Sumber utama terjadinya arus harmonik yang tinggi semasa, faktor kuasa yang rendah dan arus neutral yang berlebihan beban tinggi kuasa campuran bukan linear. Piawai antarabangsa mengenai kualiti kuasa mengenakan had maksimum Penyelewengan Jumlah Harmonik (THD) adalah 5 %. Tambahan pula, faktor kuasa sepatutnya adalah uniti dan arus konduktor neutral adalah menghampiri sifar. Kebanyakan penggunaan kuasa elektrik diedarkan melalui tiga fasa empat wayar sistem dan akibat arus pengalir neutral tinggi dihasilkan sebagai tambahan kepada generasi harmonik semasa. Kehadiran harmonik dalam talian agihan akan mengakibatkan kerugian kuasa yang lebih besar, gangguan dengan talian komunikasi dan kegagalan operasi peralatan sensitif. Satu penyelesaian yang boleh digunakan dan menjimatkan terhadap gangguan kualiti kuasa adalah penapisan kuasa aktif. Tesis ini memenangani isu-isu di atas dengan menggunakan dua peringkat, lima peringkat dan tujuh peringkat tiga fasa empat wayar Penapis Kuasa Aktif pirau (SAPF) dalam rangkaian pengagihan industri untuk mengurangkan arus neutral dan untuk mengurangkan arus harmonik. Arus talian yang telah disuntik oleh SAPF dibentuk dengan mengawal sumber voltan dua peringkat dan pelbagai peringkat Penyongsang (VSI) berdasarkan SAPF. Dalam usaha untuk mengawal VSI, isyarat rujukan diproses dengan menggunakan tiga kaedah kawalan yang dibentangkan di dalam tesis ini. Ianya adalah berdasarkan teori *p-q*, *dq-0* teori dan

teori *a-b-c*. MATLAB / SIMULINK digunakan sebagai alat simulasi bagi menghasilkan model sistem kuasa yang bersesuaian dengan simulasi dinamik. Kaedah kawalan bagi SAPF diperkenalkan di dalam tesis ini telah dianalisakan dan digunakan kepada sistem tiga fasa empat wayar untuk mengimbangi arus sumber harmonik, membetulkan faktor kuasa kepada menghampiri satu dan menambahbaik sumber arus THD ke jurang 5 % seperti dicadangkan oleh piawai IEEE-519.

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LIST OF ABBREVIATIONS

APF	Active power filter
APOD	Alternative phase opposite disposition
BJT	Bipolar junction transistor
CSI	Current source inverter
CHB-VSI	Cascaded H-bridge voltage source inverter
DS	Distribution system
EMI	Electromagnetic interference
FACTS	Flexible AC Transmission System
GTO	Gate turn-off thyristor
HAPF	Hybrid active power filter
IGBT	Insulated gate bipolar transistor
IPD	In-phase disposition
KCL	Kirchhoff's current law
KVL	Kirchhoff's voltage law
LS-SPWM	Level-shifted sinusoidal pulse width modulation
MLI	Multilevel inverter
MOS-FET	Metal oxide semiconductor field-effect transistor
PC	Personal computer
PCC	Point of common coupling
PDN	Power distribution network
POD	Phase opposite disposition
PPF	Passive power filter
PS-SPWM	Phase-shifted sinusoidal pulse width modulation

PWM	Pulse width modulation
RMS	Root mean square
SAPF	Shunt active power filter
THD	Total harmonic distortion
UAPF	Universal active power filter
VSI	Voltage source inverter

NOMENCLATURE

C	Capacitance
C_{dc}	Capacitor at the DC side of the SAPF
E	Energy stored in the DC capacitor
h	Current hysteresis band
i_{La}, i_{Lb}, i_{Lc}	Instantaneous phase currents of the load
i_{sa}, i_{sb}, i_{sc}	Instantaneous phase currents of the source
i_{sf}, i_{Lf}	Fundamental components of the source and load currents
i_{sH}, i_{LH}	Source and load harmonic current components
i_{sha}, i_{shb}, i_{shc}	Compensating phase currents injected by the SAPF
i_0, i_α, i_β	Currents of three-phase four-wire system in stationary frame
$i_{\alpha p}$	Instantaneous active current component on the α-axis
$i_{\alpha q}$	Instantaneous reactive current component on the α-axis
$i_{\beta q}$	Instantaneous reactive current component on the β-axis
$i_{\beta p}$	Instantaneous active current component on the β-axis
L	Inductance
M	Voltage source inverter level
n	Number of transient cycles
p	Instantaneous active power
$p_{\alpha p}$	Instantaneous active component of the real power on the α-axis
$p_{\alpha q}$	Instantaneous reactive component of the real power on the α-axis
$p_{\beta p}$	Instantaneous active component of the real power on the β-axis
$p_{\beta q}$	Instantaneous reactive component of the real power on the β-axis

q	Instantaneous reactive power
R_L, L_L	Resistance and inductance of the load
R_s, L_s	Source resistance and inductance (phase values) of the source
R_{sh}, L_{sh}	Resistance and inductance at AC side of SAPF
s	Instantaneous apparent power
T	period
v_{an}, v_{bn}, v_{cn}	Three-phase line-to-neutral voltages
v_{Ba}, v_{Bb}, v_{Bc}	Instantaneous phase voltages at the PCC
V_{dc}	Voltage at the DC side of the SAPF
v_{La}, v_{Lb}, v_{Lc}	Instantaneous phase voltages of the load
V_m, I_m	Maximum values of voltage and current
v_{lm}	Maximum line voltage
V_s, I_s	RMS values of voltage and current of the source
v_{sa}, v_{sb}, v_{sc}	Instantaneous phase voltages of the source
v_{sf}, v_{sH}	Fundamental and harmonic components of the source voltage
v_{sha}, v_{shb}, v_{shc}	Instantaneous phase voltages at the AC side of SAPF
v_0, v_α, v_β	Voltages of the three-phase four-wire system in stationary frame
v_1	Fundamental voltage
v_3	Third harmonic voltages
v_5	Fivth harmonic voltages
$\bar{p}_0$	Average part or DC component of zero-sequence power
$\tilde{p}_0$	Oscillating part of zero-sequence power
$\bar{p}$	Average part or DC component of the active power
$\tilde{p}$	Oscillating part of the active power
$\bar{q}$	Average part or DC component the reactive power

$\tilde{q}$	Oscillating part of the reactive power
ΔE	Rate of change in energy
Φ	Phase angle between input voltage and current
ω	Fundamental electrical angular frequency
3ω	Third harmonic electrical angular frequency
5ω	Fivth harmonic electrical angular frequency

CHAPTER 1

INTRODUCTION

A major concern within the electrical power industry is the power quality which has become an important and growing problem in power distribution networks (PDNs). Equipment based on static power electronic converters which are used to control and transfer of power injects significant amounts of harmonics into power system. Wide spread use of three-phase non-linear loads in power distribution system which include arc furnaces, adjustable speed drives, traction system, etc. create major power quality problems, mainly harmonics, on the modern distribution grid [1]-[3]. The concern about harmonics is growing because many equipment connected to the distribution systems (DS) are extremely sensitive. There are a few challenges on harmonic pollution that are to be addressed as utilities are moving forward to a Smart Grid. Power quality for the digital economy in a Smart Grid distribution system is a priority with a variety of quality/price options. Meanwhile, the impact of renewal sources of energy like solar, wind, wave etc., which mainly use power electronic controllers and integrated into the Smart Grid cause increased power quality problems. Against this backdrop, the importance of identifying new solutions for minimizing harmonic pollution has never been greater which will be a step forward to improve power quality. To improve overall system performance an accurate detection of harmonic disturbances is therefore extremely important and valuable for both power distributors and power consumers. Flexible AC Transmission System (FACTS) devices such as shunt active power filter (SAPF) are becoming controllable compensating equipment for power quality improvement. This thesis mainly focuses on developing two-level and multilevel voltage source inverters based SAPF for extracting harmonic disturbances in a three-phase, four-wire distribution system and to suppress the load

Harmonic currents and neutral conductor current. The three-phase non-linear loads based on solid-state devices draw harmonic currents in the form of primary lower-order positive-sequence harmonics (7^{th}, 13^{th}, 19^{th} etc.) at harmonic frequencies of 350 Hz, 650 Hz, 950 Hz etc., respectively, and primary lower-order negative-sequence harmonics (5^{th}, 11^{th}, 17^{th} etc.) at harmonic frequencies of 250 Hz, 550 Hz, 850 Hz etc., respectively [4]-6].

Harmonic currents create voltage drops across the system impedance and harmonic voltages at the corresponding harmonic frequencies. By using ohm's law the voltage distortion can be expressed as $V_H = (I_H \times Z)$, where Z is the impedance of an electrical load in the circuit, mostly is inductive. The harmonic voltage drop by each harmonic current will be at the same harmonic frequency. Because the system impedances are generally expected to be low, the magnitudes of the voltage harmonics are usually lower than those of the current harmonics. Therefore, the overall distortion of the voltage waveform is less than that of the current waveform. The existence of currents and voltages at these frequencies in PDNs are harmful for both power system operation and consumer products. Several undesirable phenomena in the operation of PDNs are caused by the current and harmonic voltages, such as: failure of operation of sensitive equipments, interface with communication lines, excessive amount of reactive power, increased power losses in the lines, low efficiency and poor power factor on the supply side [4], [7]-[9].

In several applications especially in low voltage industrial, commercial and residential distribution systems, the electrical power is distributed through three-phase four-wire system. Major single-phase non-linear loads in three-phase four-wire distribution system are personal computer (PC) power supplies, fax machines, photocopiers, fluorescent lighting, etc. which lead to additional challenge when connected besides three-phase non-linear loads. As a result the triplen or zero-sequence harmonics (3^{rd}, 9^{th}, 15^{th}, etc.) at harmonic frequencies of 150 Hz, 450 Hz, 750 Hz etc., respectively, are present which add up arithmetically at the neutral bus. The zero-sequence harmonics may cause overheating of motors and transformers, also reduce energy efficiency as well damage the neutral conductor as the neutral current sometimes reach magnitudes as high as 1.73 times the phase current [2],

[5]-[7], [9], [10]. Harmonics in power systems are defined as sinusoidal voltages and/or currents at frequencies, usually which are integer multiples of the system fundamental frequency. It is desirable to suppress harmonics in power systems by using power filtering devices such as passive power filters (PPFs) as conventional solution or active power filters (APFs) as a viable solution [2], [7], [11], [12] as each one of them has its own merits and demerits. Conventionally passive L-C filters and/or resistance are used to filter the harmonics and to compensate the reactive current due to non-linear loads. With the development of high power semi-conductor devices, APF technology attracted the attention of power system engineers to provide dynamic solutions to the power quality problems mainly to eliminate the voltage harmonics. In addition APFs are also used to regulate terminal voltage, to reduce voltage unbalance and to suppress voltage flicker in three-phase systems. In four-wire three-phase systems the problem of excessive neutral current is recognized in neutral wire which is produced when the single-phase non-linear loads are connected beside three-phase non-linear loads. APFs are capable of providing corrective measures to minimize the neutral current even with dynamically changing non-linear loads. A voltage source inverter (VSI) is the heart of APF. Various kinds of VSI classified according to their power converter types, operation modes, and phase numbers are presented in [13]-[16]. A capacitor DC storage element and insulated gate bipolar transistors (IGBTs) or other semi-conductor power switches are the main components of VSI, an isolation transformer and/or an interface inductor is mandatory when APFs are implemented on power networks. The VSI unlike the current source inverter (CSI), has many advantages such as minimal equipment impact, rapid control of active as well as reactive power, lower in cost, smaller in physical size, provides a high level of power quality, and ability to connect to weak ac networks, or even dead networks. Also VSI does not need an additional energy source in the DC side and it is the usual extended configuration [17]-[21]. Figs 1.1 and 1.2 show the converter type power circuit topologies of VSI and CSI, respectively.

In the first topology, the VSI has a capacitor connected on the DC side and it works as a voltage source, while in the second topology, the CSI has an inductor connected on the DC side and it works as a current source [19], [20], [22]-[24]. This chapter presents the background about active filtering, harmonics and their effect on

distribution network, neutral conductor current and methods used for its minimization, reactive power compensation followed by a brief introduction on control techniques used for generation of pulses for VSI, research motivation and objectives.

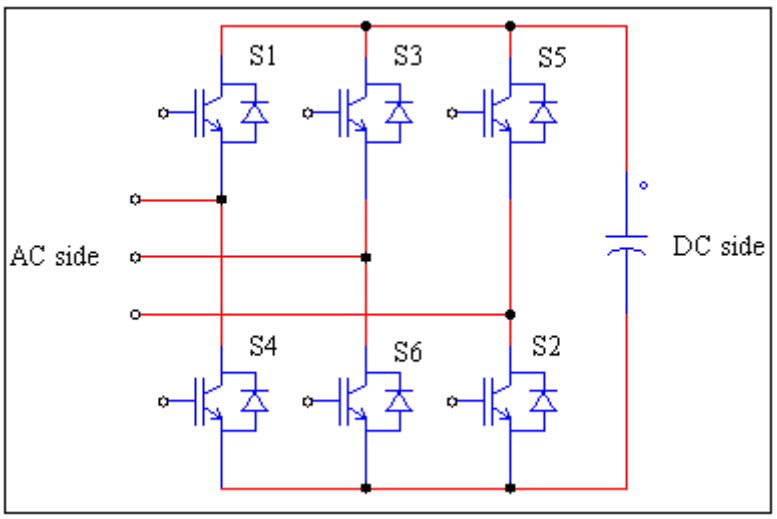


Fig 1.1: Power circuit of a VSI

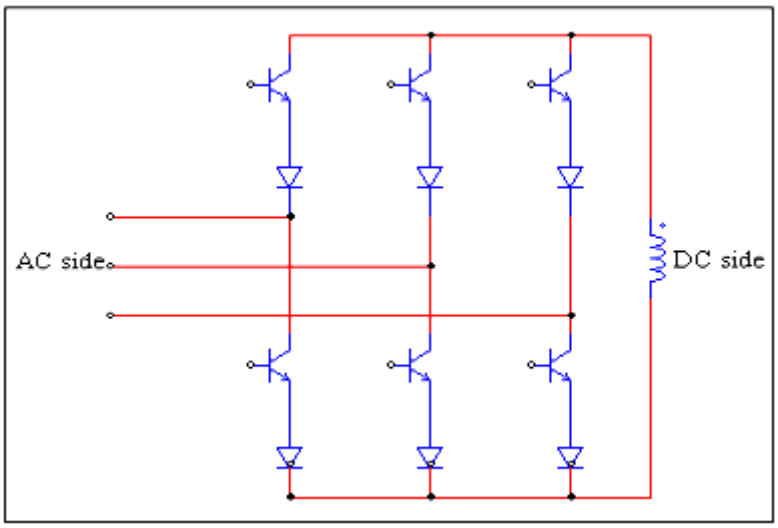


Fig 1.2: Power circuit of a CSI

1.1 Research motivation

As has been reported previously, power quality of distribution systems can be improved by active filtering of harmonics and by minimizing the neutral conductor current. In contrast to traditional passive filters which are used in three-phase, three-wire systems, active filtering by SAPF in three-phase four-wire systems

overcomes the inadequacies of passive filters. Passive filters have certain limitations such as compensation for a particular harmonic, resonance with load and utility impedance as well as the physical size. Recently VSI based SAPF is suggested as the most effective device for harmonic disturbances and investigations are carried out for improving the power quality in three-phase systems. A SAPF in a four-wire system mitigates harmonic pollution in the phase conductors and as well minimizes the neutral conductor current to zero.

1.2 Problem statement and solutions

1. Employing single-phase non-linear loads besides three-phase non-linear loads in a power system can cause excessive neutral current in addition to the harmonic distortion in supply lines which affect the four-wire distribution system in terms of power quality and efficiency.
2. As the three-phase three-wire SAPF is inadequate to improve the power quality this study proposes to solve the problem of suppression of current harmonics as well as neutral current minimization by implementing three-phase four-wire SAPF.
3. It is proposed to develop effective controllers in order to control the two-level, five-level and seven-level voltage source converters which will be used in SAPF.
4. Also it is proposed to provide solution for reactive power compensation, power factor and THD improvement on the supply side.

1.3 Objectives of study

The main objective of this study is to design and develop two-level as well as multi-level SAPF and to investigate its compensation performance in three-phase four-wire PDNs. The major objectives of the work reported in this thesis are:

1. To minimize the zero-sequence harmonic currents of the neutral conductor and harmonics currents in the supply lines of a three-phase four-wire PDN.

2. To design and simulate two-level, five-level and seven-level SAPF in a three-phase, four-wire distorted distribution system.
3. To develop several control strategies for the SAPF based on *p-q* theory, *d-q-0* theory and *a-b-c* theory.
4. To compensate the reactive power of the mixed nonlinear loads, to guarantee the supply side power factor close to unity and to reduce the THD of the source currents below 5 % by successfully eliminating the harmonic currents as well as reactive components of current.

1.4 Scope of Study

To fulfill the objectives of this thesis, before any modeling and simulation is applied on SAPF using MATLAB/SIMULINK; an extensive study on various types of VSI, control circuits and characteristics of the APF is essential. Also an understanding on the effect of non-linear loads on the distribution system to analyze the power quality problems is useful. Basically, the following work is carried out to meet the objectives of this thesis.

i. The power quality problem using active filtering in PDN as well as identifying and determine the type of APF which will be more suitable to be applied for this research was reported.
ii. Model a distribution system which is supplying mixed non-linear loads and compensated by a three-phase four-wire SAPF using MATLAB/SIMULINK software packages.
iii. Develop three different types of controllers based on *p-q* theory, *d-q-0* theory and *a-b-c* theory and propose several modulation techniques for five and seven-level VSI.
iv. Two-level, five-level and seven-level VSI based three-phase four-wire SAPF is proposed to suppress harmonic currents, to minimize the source neutral current to zero as well as to minimize THD of source current below 5 % and improve source power factor very close to unity.

1.5 Contribution of the study

The main contributions of this study are as follows:

- Design and development techniques of measurement and simulation blocks of three-phase four-wire distribution system using MATLAB/SIMULINK software.
- Proposed three control techniques based on *p-q* theory, *d-q-0* theory and *a-b-c* theory to control the three-phase four-wire two-level, five-level and seven-level SAPF.
- Five-level and seven-level CHB-VSI based three-phase four-wire SAPF have been proposed and simulated using several modulation techniques such as PS-SPWM as well as the three types of LS-SPWM (IPD, APOD and POD) which are simulated and compared using MATLAB/SIMULINK software.
- Improvement in peak transient current by using five-level and seven-level SAPF.

1.6 Organization of thesis

This thesis is organized into five chapters which are summarized as follows:

Chapter 1 presents the background about active filtering, harmonics and neutral conductor current and their effect on distribution network, research motivation, problem statement and objectives.
The rest of the thesis is organized as follows:

Chapter 2 presents types of APFs, connection of SAPF in a three-phase four-wire distribution system, a brief introduction on non-linear loads, models based on two-level, five-level and seven-level VSIs, followed by literature review on SAPF.

Chapter 3 introduces instantaneous power theory, estimation of reference currents for the control and operation of SAPF, proposed controllers and modulation techniques for two-level and multilevel SAPF. This chapter also presents simulation models for two-level and five/seven-level three-phase four-wire SAPF developed by MATLAB/SIMULINK.

Chapter 4 presents the simulation results and analysis on the compensating performance of two-level, five-level and seven-level VSI based SAPF using the proposed controllers and modulation techniques.

Chapter 5 reports the conclusions and summarizes the findings of the research. Also a brief report on contributions and recommendations for the future research is also presented.

CHAPTER 2

LITERATURE REVIEW AND SURVEY ON ACTIVE POWER FILTERS

2.1 Introduction

Active power filters have been around for a while and this chapter presents a brief introduction on the existing literature to provide the background information on VSI based active power filters (APFs) in general and SAPFs in particular. Basically APFs can be categorized based on the DC to AC converter types, the number of phases, the level and topology. Essentially, the PWM based VSI and CSI types are adopted in the development of APFs as presented in chapter one, Figs 1.1 and 1.2, respectively.

VSI is generally preferred as the power circuit of the APFs rather than a CSI, because the DC capacitor used as an energy storage element in VSI is more compact and less heavy than the DC inductor which is used as an energy storage element in CSI. Moreover, it is cheaper, highly efficient and expandable to multi-level to enhance the performance with lower switching frequencies. The second classification is based on the types of non-linear loads on the supply phases, such as single-phase, three-phase three-wire or four-wire system. The third classification is with respect to the level of the converter type, such as two-level or multi-level converter. The fourth classification is according to the topology, such as series, shunt and hybrid APF, as well as universal APF (UAPF). This chapter also presents a brief introduction on non-linear loads, two-level and multilevel inverters followed by an extensive discussion on literature review on modeling and applications of SAPF.

2.2 Active power filters (APFs)

Recently, electrical power quality issues have become significant for utilities, customers and the manufacturers of electrical equipments. A huge number of power electronic equipments employed to feed controlled electric power to electrical loads use semiconductor devices. The solid-state converters as non-linear loads are more sensitive to power quality variation than the equipments used in the past. Researchers and power system engineers are continuously searching for solutions to minimize harmonics, reactive power compensation and neutral current minimization as well as power factor improvement of the systems. Significant progress is also made on APF technology to overcome the above power quality problems. APF is a controllable current or voltage source which uses sold-state switches to inject harmonic current or voltage. Besides, APFs are the latest achievement of the power electronics filtering devices in the last four decades. The basic principle of APF is to utilize power electronics technologies to produce specific current or voltage components that cancel the harmonic currents or voltages caused by the non-linear loads [3], [11]. Typically APFs are composed of IGBT or MOS-FET or GTO based voltage source inverters with DC bus capacitor as an energy storage element. However, IGBT is the most commonly used device in VSI as it can operate at higher switching frequency as compared to other devices (about 25 kHz). Besides, its energy losses are also low.

APFs have compensation performance independent of power distribution system based on the precision of a model. Also, APF has many advantages over a passive filter. They provide effective harmonics extraction, reactive current compensation and do not cause harmful resonance with the power distribution system. The APF is characterized by not consuming any real power other than due to switching losses, smaller in size and more flexible in applications. But APFs also have some drawbacks with fast switching of high currents in their power circuits. This can result in high frequency noise which causes Electromagnetic Interference (EMI) in the distribution system [4], [14], [25], [26]. Basically, there are three main categories of APF with respect to their connection configurations in several power circuits namely, series APF, shunt APF (SAPF), and the third one is the combination of active and passive filters called as hybrid APF. Besides, a universal APF which uses a combination of

series and shunt APF is included as one of the custom power devices [11], [22].

2.2.1 Series active power filters

The series APFs are similar in construction as SAPFs, except that the interfacing inductor of shunt APFs is replaced with a matching transformer. The series APF is connected in series with the AC supply voltage at the point before the load through a matching transformer. A series APF control and operate like a voltage source and its principle of operation is based on injection voltage. A voltage is injected into the power system across the matching transformer which is added to the source voltage or subtracted from it to compensate any disturbance affecting the load voltage, such as voltage-flicker or voltage harmonics [14], [27]-[29]. Series APFs have been used as harmonic isolators and protective devices for sensitive loads when supply voltage drops to a low value. Also they are used to eliminate voltage harmonics, to minimize voltage unbalance and to improve regulation [11], [27]. However, it is less effective for harmonic currents and reactive power compensation.

2.2.2 Shunt Active Power Filters (SAPFs)

SAPFs are currently the most important and most widely used configuration of the APFs in active filtering applications. SAPF was established by Gyugi and Strycula in 1976 as reported in [20], [30]. The major components of a typical SAPF consist of IGBT based VSI, a DC capacitor as an energy storage element and an interface inductor. Actually, the power converter of SAPF is a boost-type converter which means that the DC bus voltage must be kept higher than the peak value of the AC bus voltage in order to guarantee the controllability of the PWM current control. Basically SAPF is connected in parallel with the harmonics generating loads without a transformer for low voltage network or with a transformer in case of high voltage network. This topology allows reducing the cost associated to SAPF design, and avoids the utilization of force-commutated semiconductors at high-voltage levels. Actually SAPF in power system network acts as a current source. The inductor, L_L installed at the AC side of the load plays a crucial role in stabilizing and providing

proper operating condition of the SAPF [14], [25], [29], [31]. The large interface inductor connected at the AC side of SAPF, L_{sh}, is used for protection from transient disturbances. Nevertheless, large L_{sh}, limits the ability of SAPF to tackle higher-order harmonics [11], [31]. The THD of the compensated currents is strongly dependent on the switching frequency of the IGBTs, and on the value of L_{sh}. The larger L_{sh}, the smaller the THD as reported in [32]. SAPF is considered as a feasible solution of power quality problems created by non-linear loads and also it is proper for current harmonics elimination by continuously tracking changes in its harmonic contents. There are several proposed control techniques for SAPFs to generate a suitable compensation current [11], [18], [26], [33]-[47]. The principle of operation of SAPF is based on the injecting compensating current with the same magnitude and contrary to the distorted current to achieve a purely sinusoidal current wave in-phase with the supply voltage. The compensation current, can be obtained by measuring the load current, and by subtracting it from a sinusoidal reference [15], [16], [43], [48]. It is possible to get sinusoidal and balanced compensated currents by the SAPF, based on a full compensation of the harmonic components as well as the components that differ from the fundamental positive-sequence components.

A major advantage of using SAPF is that it does not only carry the compensation current but also able to supply a small amount of active fundamental current to compensate for system losses which also contribute to compensate reactive power. After successful compensation by the SAPF, the compensated system should be satisfying simultaneously the following optimal compensation characteristics:

- The source current should be sinusoidal and in phase with the source voltage.
- Draw only fundamental current from the source.
- Draw only the DC component of instantaneous active power from the source.
- The three-phase four-wire system source neutral current is close to zero.

The features of SAPF can be summarized as [6], [49]-[51]:

- As SAPF is connected in parallel with the circuit; its failure would not disrupt the entire system.
- It is capable of compensating multiple harmonics, unlike a passive filter which

is tuned only for a particular harmonic. Also it can compensate selected number of harmonics. Table 2. 1 shows the harmonic order and their phase sequences.

- The compensation effect is unchangeable with the size of the load rate of change and always achieves satisfactory results.
- If necessary, it can be used to compensate displacement factor.
- There is no danger of overload as maximum current flows under the limit mode.

Table 2.1: Harmonic order versus phase sequence

NO	Harmonic order	Sequences
1	1, 4, 7, 10, 13, 16, 19	Positive-sequence
2	2, 5, 8, 11, 14, 17, 20	Negative-sequence
3	3, 6, 9, 12, 15, 18, 21	Zero-sequence

2.2.3 Hybrid active power filters (HAPFs)

The HAPFs are mainly realized by combining APFs and PPFs. HAPFs were proposed in 1988 and 1990 as reported in [14], [29]. A HAPF aims to compromise the high cost of APFs and resonances with the source impedance associated by the PPF. A HAPF can be built in four topologies as combinations of APFs and PPFs but not limited, as follows [13], [14], [27], [52]-[57]:

- Series APF and shunt passive power filter (SPPF).
- SAPF in series with SPPF.
- Series APF in series with SPPF.
- An integrated combination of SAPF and SPPF.

The harmonic current of the load flowing into the SPPF produces harmonic voltage at the load side, which is considered as one of the drawbacks of HAPF. From the HAPF topology, Series APF in series with SPPF, the series APF acts as variable impedance, thus the voltage and VA rating are reduced compared to other HAPF topologies.

The HAPFs will be considered as one of the development directions of APFs technology. The principle of operation of the HAPFs is based on the SPPFs which are used to cancel lower order harmonics of the load, and APFs tend to improve the performance of PPFs to cancel other harmonic components. The HAPFs are used for current harmonics suppression [14], [58], [59].

Nevertheless, HAPFs have a drawback associated with physical size of the PPFs, and also reactive power and resonance contributed by PPFs. Moreover, HAPF is exclusively devoted to harmonic filtering and does not have the capability to compensate reactive power.

2.2.4 Universal active power filter (UAPF)

The UAPF also called as unified power quality conditioner, is used to suppress voltage and current harmonics and to improve power quality at PCC. Basically UAPF circuit is a combination of SAPF and series APF with a common DC capacitor. UAPF has the capability to balance and regulate terminal voltage and eliminate negative sequence currents. However, it needs a complicated control system for large number of semiconductor switching devices used in the filter [27], [60], [61].

The principle of operation of UAPF is based on the series APF which is the most suitable one to handle voltage related problems. It tends to balance and isolate voltage harmonics and regulate the voltage level as well. Whereas the SAPF is the most promising filter to tackle the current related problem, as it tends to compensate harmonic and reactive currents, balance the unbalanced load currents and eliminate the source neutral current as well.

2.3 Distribution system with SAPF

The connection of a three-phase SAPF in a distribution system can be realized in four different ways as follows: [62], [63]

i. A three-phase three-wire SAPF, which consists of six IGBTs in bridge configuration and a DC capacitor as storage element.

ii. The SAPF which is an integrated combination of three single-phase SAPFs in a three-phase four-wire system.

iii. The third type of SAPF is the three-phase three-leg split-capacitor configuration in a three-phase four-wire system.

iv. The last topology is the three-phase four-leg SAPF.

2.3.1 Three-phase four-wire scheme

In several areas, power is distributed through three-phase four-wire system and traditional APF is inadequate for harmonics compensation and power factor correction. In many installations, the single-phase non-linear loads inject harmonic currents which flow into the neutral conductor. Thus there is an urgent need for neutral current compensation in addition to the number of power quality problems caused by the non-linear loads. To overcome this shortage, a three-phase four-wire SAPF has been introduced in the 1980s as reported by [38], [41], [48], [62]-[65].

The widespread use of single-phase non-linear loads, such as fluorescent lamps, AC/DC converters, photocopiers, computers, printers, etc., develop excessive current harmonics as well as excessive current in the neutral conductor. The excessive neutral current leads to overloading of the neutral conductor. This requires replacing the neutral conductor with oversized conductor to prevent the overheating of motors and overloading of the distribution transformer. One of the proposed solutions to reduce the neutral current is by using zigzag transformer as a traditional method but it is not a practicable method. The effective and practical solution is by using a three-phase four-wire SAPF in order to minimize the neutral current.

Actually, high neutral currents in three-phase four-wire systems usually result from the following situations [6], [66]-[69].

i. The presence of the single-phase non-linear loads in a balanced three-phase system.

ii. Heavy unbalanced load currents.

iii. The current harmonics distortion.

iv. A number of multiple power systems in the facility, especially multiple services drop.

The three topologies of three-phase four-wire SAPF are shown in Figs. 2. 1 to 2. 3. Fig 2. 1 show the possibility of using three single-phase inverters based SAPF as compensator for three-phase four-wire system supplying mixed non-linear loads. In this topology, a coupling transformer is essential to connect the SAPF to the system as there is no common neutral point.

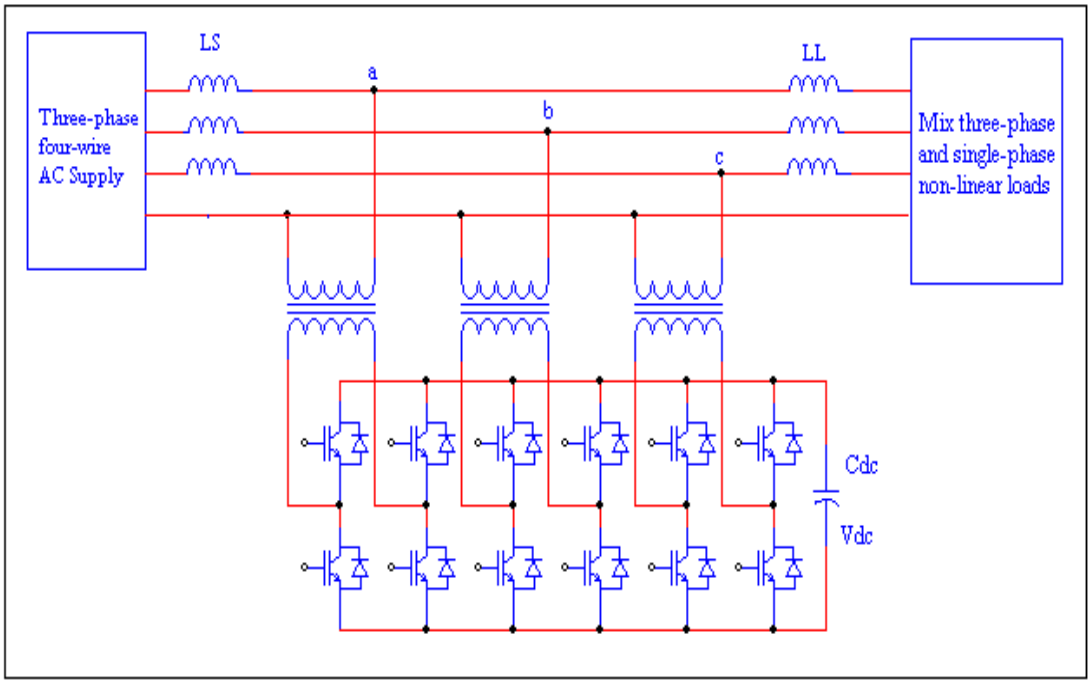


Fig 2.1: Three-phase four-wire system scheme with three single-phase inverters based SAPF

Basically, the three-phase four-wire SAPFs which are commonly used can be categorized into two main kinds depending on their connection to the neutral wire. In the first type the neutral wire is connected to the midpoint of supply by means of a capacitor divider as shown in Fig 2. 2. In the second type, the neutral wire is connected to the additional fourth leg as shown in Fig 2.11 [7], [36], [66], [70], [71]. The three-phase four-leg inverter topology is superior over three-wire type, in mode of operation of power switches, number of power switches and compensation performance. Also, some researchers point out that the four-leg converter topology is the best alternative to implement a three-phase four-wire APF. In this case, AC currents generated by the VSI have some high-order harmonics at the switching frequency, which can be easily filtered using a small passive filter [7], [64], [72].

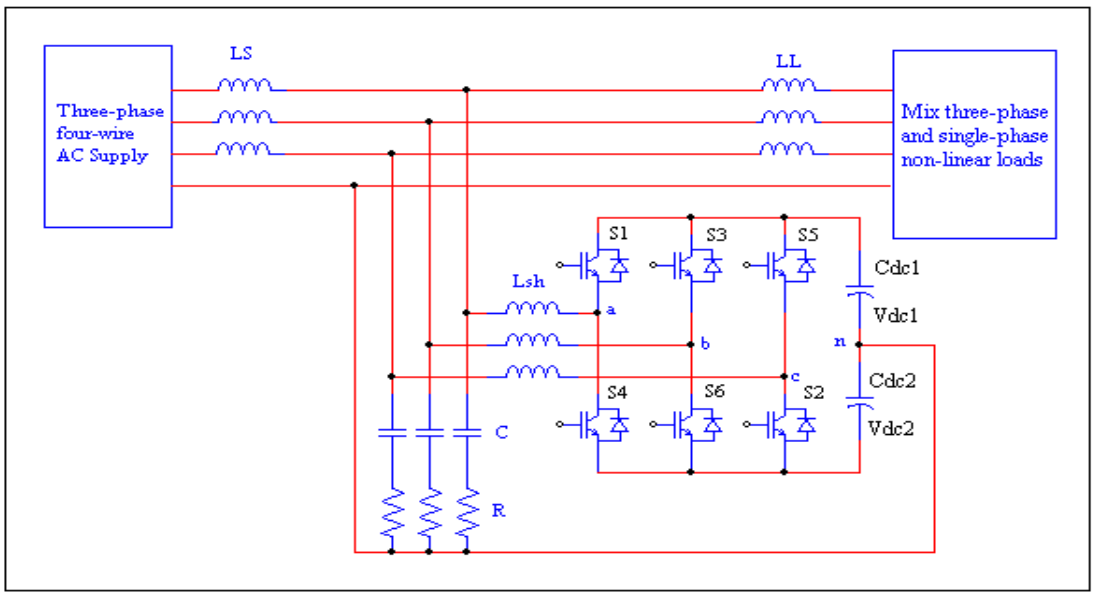


Fig 2.2: Three-phase four-wire system scheme with split-capacitor SAPF

For full compensation capability, a four-leg inverter connected as a SAPF as shown in Fig 2. 3 can be used. The compensated neutral current is provided through a fourth leg, called as neutral leg, allowing better controllability and dynamic stability than the three-leg with split-capacitor configuration as in Fig 2. 2. The main advantage of the four-leg configuration is its ability to suppress the neutral current from the source without any drawback in the filtering performance [33].

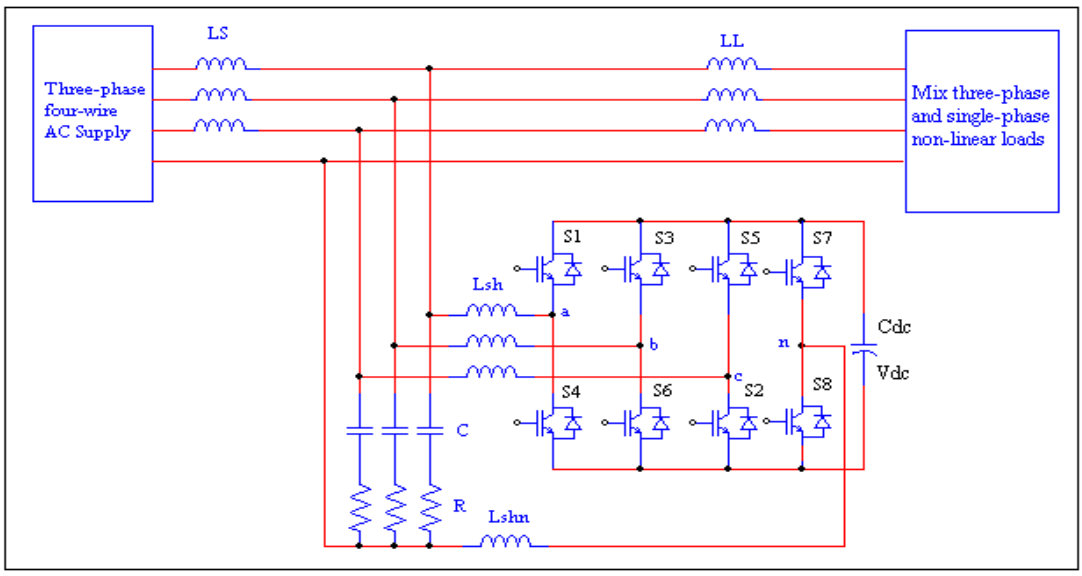


Fig 2.3: Three-phase four-wire system scheme with four-leg SAPF

2.3.2 Non-linear loads

Actually the loads connected to the PDNs can be categorized according to their behavior, either as linear or non-linear loads. The linear loads either resistive or inductive draw sinusoidal currents from three-phase sinusoidal voltages as shown in Appendix A by the simulation results and the THD is observed to be equal to zero. Typical linear loads in power system include heaters, motors etc.

A non-linear load with diodes or thyristors supplying a resistor or inductive load behaves as a harmonic source which has undesirable side effect of generating current harmonics on the PDNs. However, diode or thyristor rectifier with smoothing DC capacitor on the load side behaves like a harmonic voltage source. Non-linear loads such as diode or thyristor rectifiers draw distorted currents with very high THD from single-phase or three-phase sinusoidal voltages. Simulation studies on several typical controlled and uncontrolled rectifier loads are carried out as presented in Appendix A. Harmonic currents which flow through the power system impedance, cause voltage distortion. The voltage harmonics can be high or low according to the system impedance or current harmonics. Appendix A presents a detailed explanation on nonlinear loads and their effect on harmonic phase sequences. Only the odd-harmonics prevail in the PDNs because the even-harmonics swing equally in both positive and negative directions. The non-linear loads can be classified into two groups, as identified and un-identified harmonic-producing loads. The identified harmonic-producing loads are high power diode or thyristor rectifiers, cycloconverters, and arc furnaces. These loads are characterized because electric power utilities identify the individual non-linear loads installed by high-power consumers on PDNs in many cases. An unidentified harmonic producing load is a low-power diode rectifier used as a utility interface in an electric appliance [12], [14], [20], [51], [73], [74].

2.3.3 Discussion on types of inverters

A simple classification for converter topologies with respect to indirect (DC-link) inverter is given as in Fig. 2. 4. Indirect converters are classified into CSI and VSI topologies, depending on the DC storage element [23], [75].

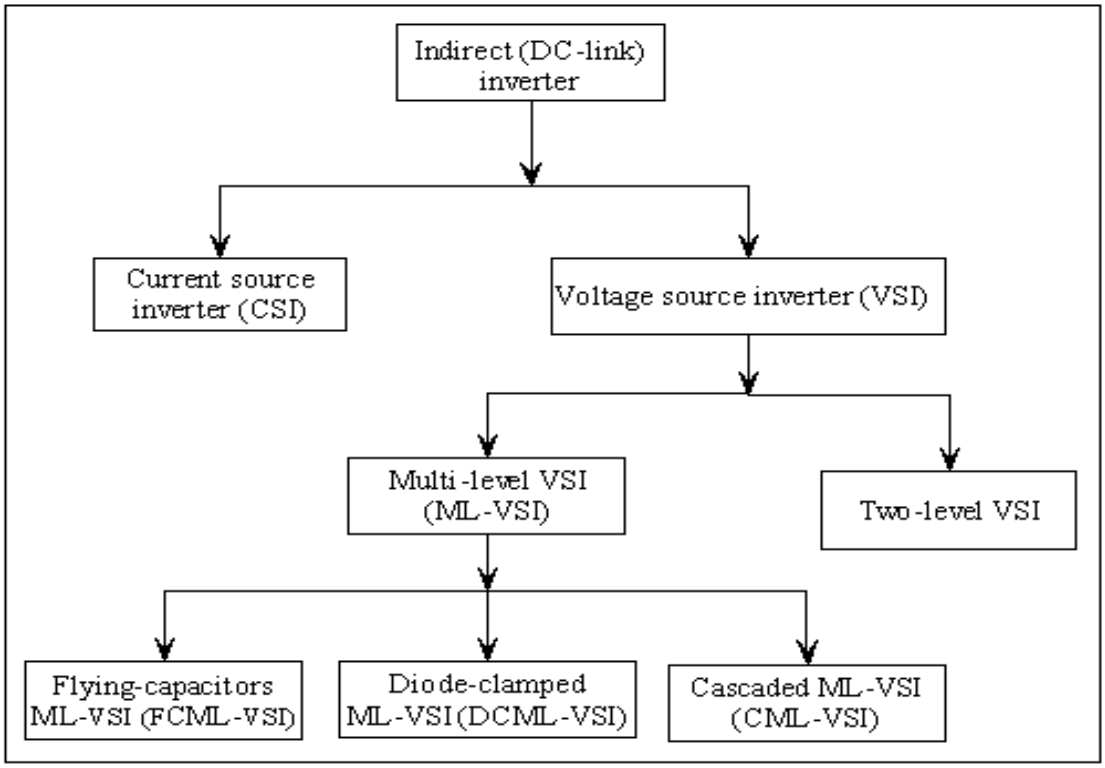


Fig 2.4: Classification of converters with respect to indirect (DC-link) inverter

2.3.3.1 Two-level VSI

The well-known two-level VSI using IGBTs is clearly the dominating converter topology in low or medium voltage power systems. With progress in IGBT voltage ratings of 3.3, 4.5, and 6.5 kV, two-level VSI can be applied to medium and high-power traction and industrial high-power drives. A two-level inverter generates an output voltage with two values (level) [23], [75].

2.3.3.2 Multilevel inverter topologies

Nowadays, there has been an increasing interest in using multilevel inverters for medium and high power energy conversion, especially for drives and reactive power compensation. A three-level inverter is an extension of two-level inverter which generates three voltage levels and the term multilevel starts here. As the number of levels in the inverter is increased the output voltages have more steps generating a staircase waveform with reduced harmonic distortion. Multilevel inverters were first introduced in 1981 by Akira Nabae as three-level neutral-point-clamped inverter.

Multilevel inverter (MLI) can be connected to the medium or high voltage networks without a coupling transformer. Moreover, high switching frequency is used only in the small voltage cell while the high voltage cells operate in low frequency. This makes a MLI is more suitable for higher power applications than two-level VSI implemented with common six-pulse converters although, it requires a minimum load current in order to make possible the voltage control [23], [76], [77]. The three-level neutral point clamped VSI is mostly applied in industrial medium voltage converters. The hard-switching transients of the power semiconductors at high commutation voltage cause high switching losses and a poor harmonic spectrum which produces additional losses on the load. Subsequently, problems are created by over-voltages in cables and machines due to the steep-switching transients [76], [78]. For these reasons, multilevel converters (MLCs) have been receiving more attention in the recent years and have been proposed as the best choice in a wide variety of medium and high voltage applications [79]. MLCs enable to reduce voltage distortion and improve harmonic spectrum without a series connection of devices, which can be considered the major merit of a multi-level structure. Other merits of these topologies are better output voltage quality and reduced EMI problems. The general concept of MLI involves producing an AC waveform from small voltage steps by utilizing a bank of series capacitors or separate DC source.

Several merits of the multilevel inverters are as follows:

i. Very low stress and distortion in the voltage output waveform.
ii. Simple in structure and consists of fewer components.
iii. An ability to reach high voltage and reduce harmonics by their own structures without transformers.
iv. The input current has minimum distortion.
v. Enable the utilization of low voltage devices in medium voltage application.
vi. Low switching frequency.
vii. The common voltages are very low.
viii. More suitable for medium and high voltage applications than the conventional two-level inverters.
ix. The initial and running costs and the EMI are less than the traditional PWM two-level inverter.

Now there are three major types of the multilevel inverters: diode-clamped, flying-capacitors and cascaded multilevel inverters [23], [75], [80]-[83].

A- Diode-Clamped Multilevel 1nverter

A diode-clamped multilevel inverter is introduced in 1980 as reported in [66] and its verification became more attractive after 1990s. The *M*-level diode-clamped converter typically consists of $(M-1)$ capacitors on the DC bus and produces *M* levels of the phase voltage. Fig. 2. 5 shows a seven-level diode-clamped converter

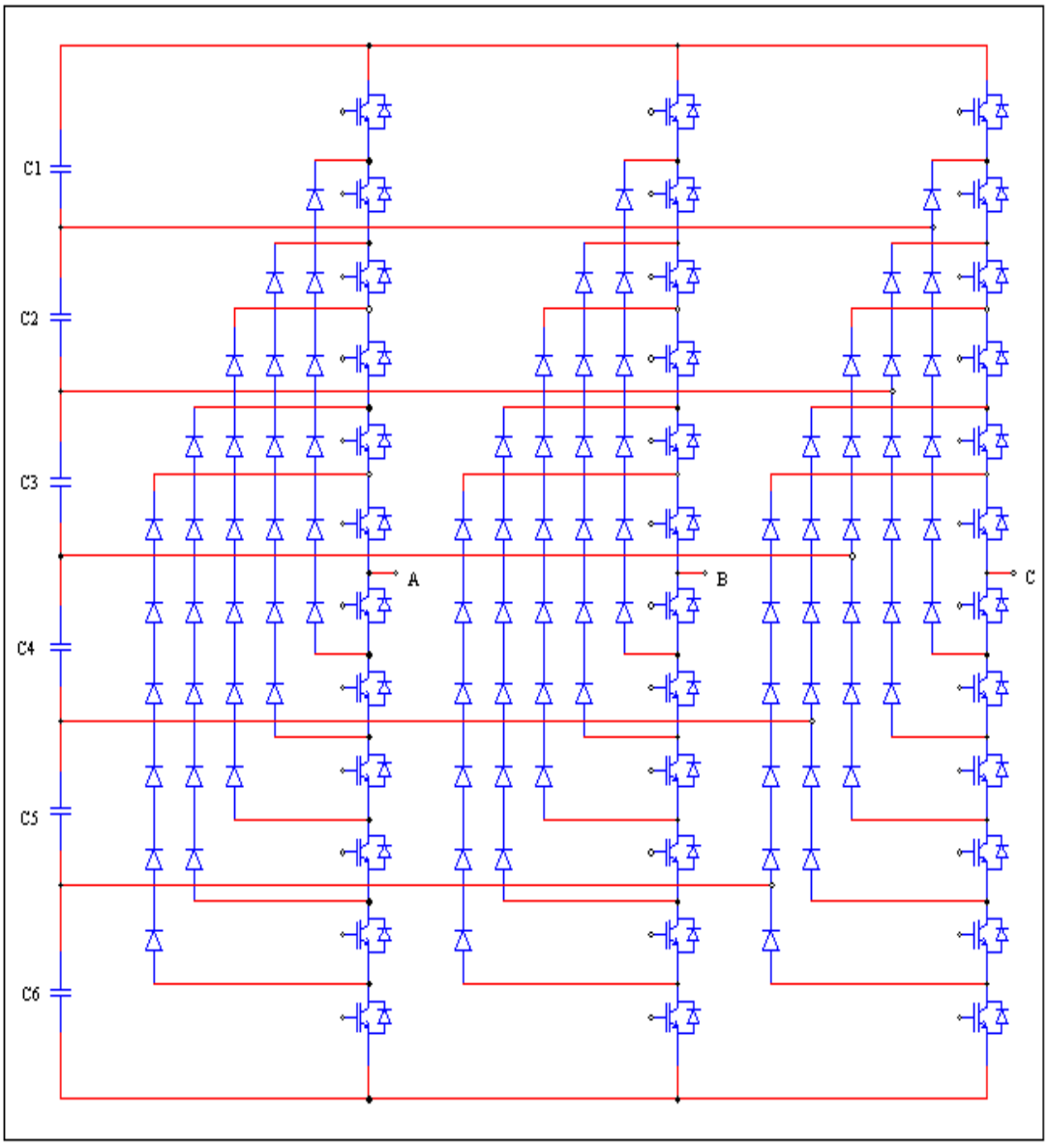


Fig 2.5: Three-phase seven-level diode-clamped VSI

in which the DC bus consists of six capacitors. For a DC bus voltage Vdc, the voltage across each capacitor is (V_{dc} / 6) [80].

The major merits and demerits of the diode-clamped multilevel inverter are summarized as follows:

Merits:

- When the number of levels is high enough, harmonic content will be low enough to avoid the need for AC filters.
- It has high efficiency because all devices are switched at the fundamental frequency.
- Imaginary power flow in the converter can be controlled.
- The control method is simple for a back-to-back inverter system.

Demerits:

- Excessive clamping diodes are required for building of higher levels.
- It is difficult to control the real power flow for the individual converter leg.

B- Flying-capacitor multilevel inverter

The fundamental building block of a flying-capacitors based 7-level converter is shown in Fig. 2. 6. Assuming that all capacitors have the same voltage rating, the series connections of capacitors indicate the voltage level between the clamping points. All phase legs share the same dc link capacitors C1 to C6. The voltage level defined in the flying-capacitors converter is similar to that of the diode-clamped type converter.

The phase voltage of an M-level converter has M levels including the reference level, and the line voltage has $(2*M-1)$ levels. Assuming that each capacitor has the same voltage rating as the switching device, the dc bus needs $(M-1)$ capacitors for an *M*-level converter. The voltage synthesis in a flying-capacitor converter has more flexibility than a diode-clamped converter [80].

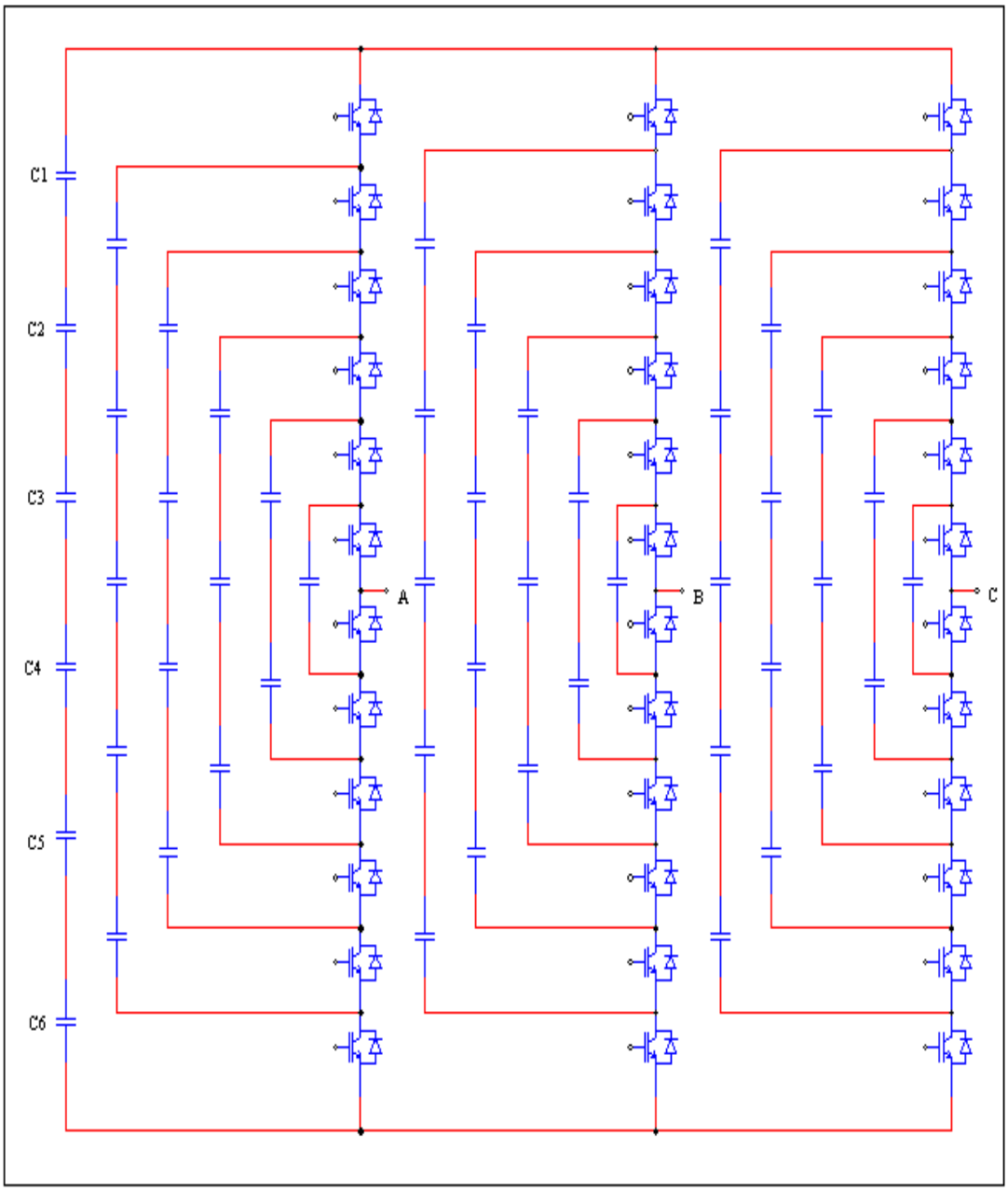


Fig 2.6: Three-phase seven-level flying-capacitors VSI

The major merits and demerits of the flying-capacitors multilevel inverter are summarized as follows:

Merits:

- Large amount of storage capacitors provides extra ride through capabilities during power outage.

- Provides switch combination redundancy for balancing different voltage levels.
- When the number of levels is high enough, harmonic content will be low enough to avoid the need for AC filters.
- Both real and imaginary power flow can be controlled, making the voltage source converter as a possible candidate for high voltage transmission.

Demerits:

- An excessive number of storage capacitors are required when the number of converter levels is high. High-level systems are more difficult to package and more expensive with the required bulky capacitors.
- The inverter control will be very complicated, and the switching frequency and switching losses will be high for real power transmission.

c- *Cascaded Multilevel Inverter*

The cascaded MLI is suitable for medium and high voltage systems. The inverter provides lower costs, higher performance, less EMI, and higher efficiency than the traditional PWM inverter. Because the switching frequency is the line frequency, switching losses and related EMI are negligible.

A cascaded MLI is quite different from the diode-clamped and flying-capacitor multilevel inverters. The cascaded MLI is structured by utilizing H-bridge units by cascading them together and each H-bridge has a separate DC source. The number of H-bridges can be calculated by using the following relation $(M-1)/2$, where M is the level number. Thus, the phase voltage would have $(2*N+1)$ levels, where N is the number of DC sources per phase. Fig. 2. 7 show the wye-connection of the seven-level cascaded multilevel inverter [80], [83].

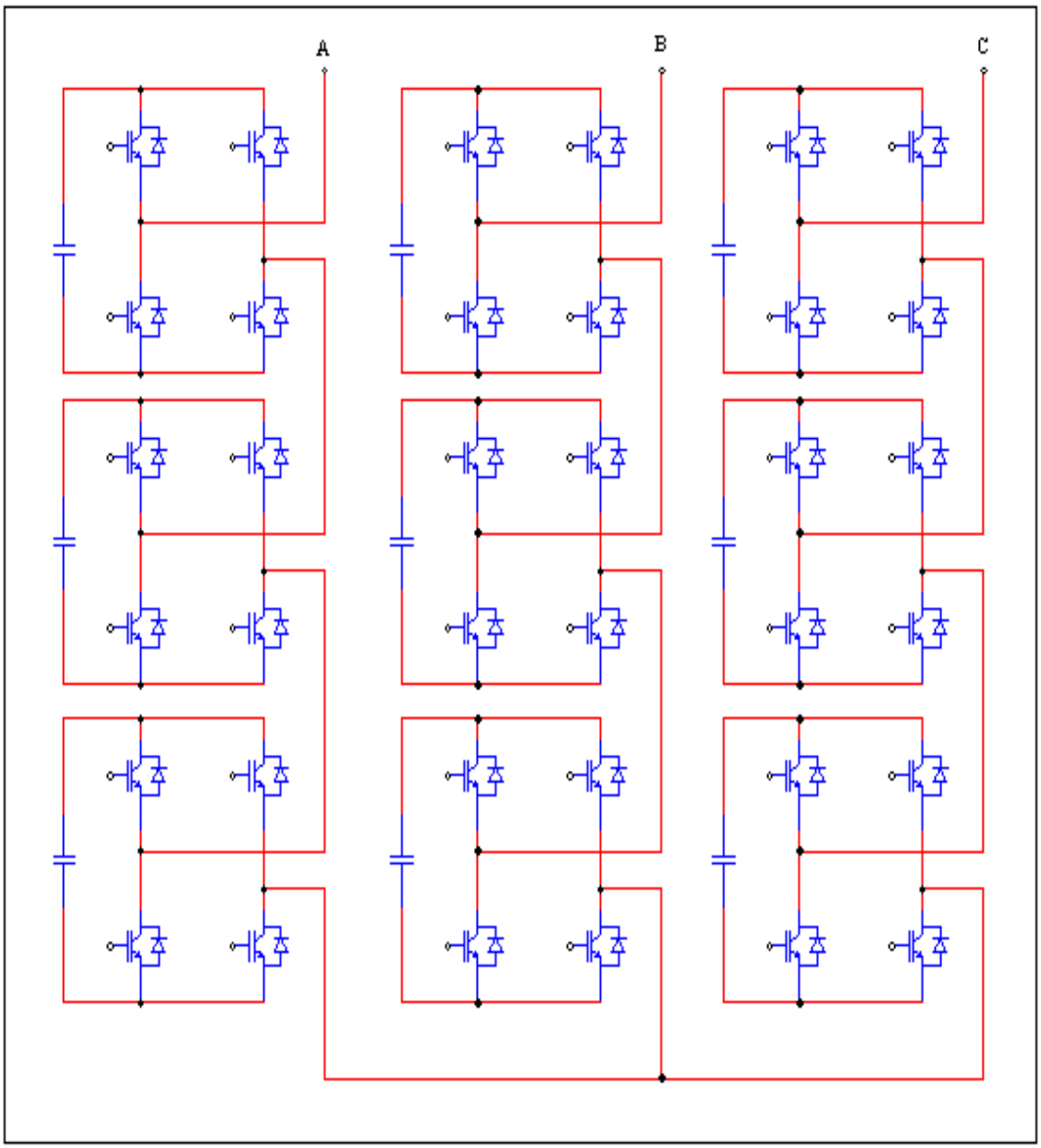


Fig 2.7: Three-phase seven-level cascaded VSI

The major merits and demerits of the cascaded multilevel VSI are summarized as follows:

Merits:

- Construction and maintenance of H-bridge is much easier and it has reasonable cost.
- Requires the least number of components among all multilevel converters to achieve the same number of voltage levels.

- The verification of the circuit is possible because each level has the same structure, and does not require extra clamping diodes or voltage balancing capacitors.

- Maximum output can be utilized from the DC sources, because it produces $(2*N-1)$ level phase voltage
- Soft-switching can be used in this structure to avoid bulky resistor-capacitor-diode Snubbers.

Demerits:

- It is very difficult to connect the inverters back-to-back because each H-bridge uses a separate DC capacitor.
- It requires separate DC sources for real power conversion, and thus its applications are somewhat limited.

2.3.3.3 Switches used in high voltage inverters

In power quality enhancement, inverter based custom power devices are used. The structure of these inverters requires power semiconductor devices that can turn on and off such as: MOS-FET, GTO and IGBT. The IGBT is a functional integration power device that combines the merits of both bipolar junction transistor (BJT) which has fixed forward voltage drop, high voltage and current ratings and low conduction losses and MOSFET which is fast switching voltage controlled device and needs low gate drive power. Thus, IGBT may be a good candidate as a power device to operate at high voltage and high power applications.

IGBT's major drawback is that it exhibits a relatively high current tail at turn-off which causes considerably high turn-off losses because the output stage of the IGBT is a BJT, a minority-carrier controlled device. In general, IGBT operates at lower frequency than MOSFET due to its slow switching characteristics. In order to operate IGBTs at a high switching frequency, soft switching techniques have to be used to reduce the device switching losses. Basically, Zero-voltage-switching eliminates the turn-on loss and reduces the turn-off loss by

slowing down the voltage rise and reducing the overlap between the switch voltage and current through [84]-[87].

2.3.3.4 Operation of the full-wave three-phase VSI

A VSI with six controllable switches is considered a multidisciplinary power electronic controller which can generate a sinusoidal voltage with several magnitudes, frequencies and phase angles. The following assumptions in analyzing the operation of the VSI for the circuits in Fig. 2. 9 are made:

- Two switches are always conducting, while the other four are blocking.
- One of the conducting switches is an odd numbered (S1 or S3 or S5) while the other is an even-numbered (S2 or S4 or S6).
- Each switch conducts for 120^0 or one third of a cycle (120^0 conduction mode).

Current follows out from the most positive source terminal, through an odd- numbered switch, through the load, through an even-numbered switch, and then back to the most negative source terminal, Table 2. 2 indicated the conducting periods of the switches [5], [88].

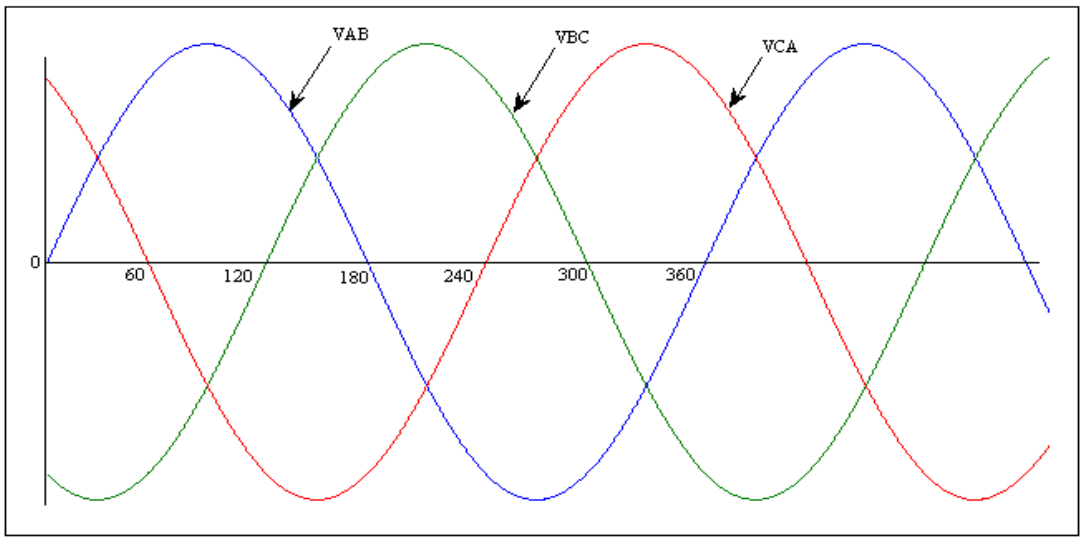
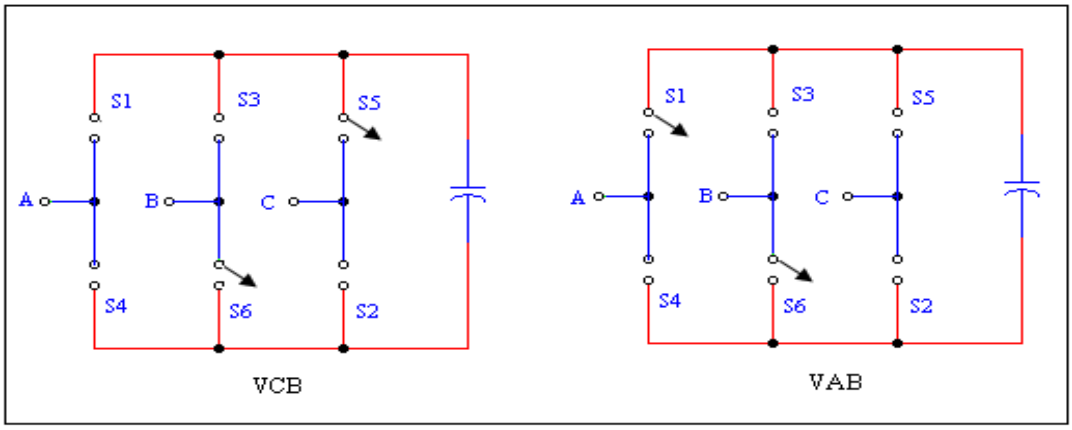


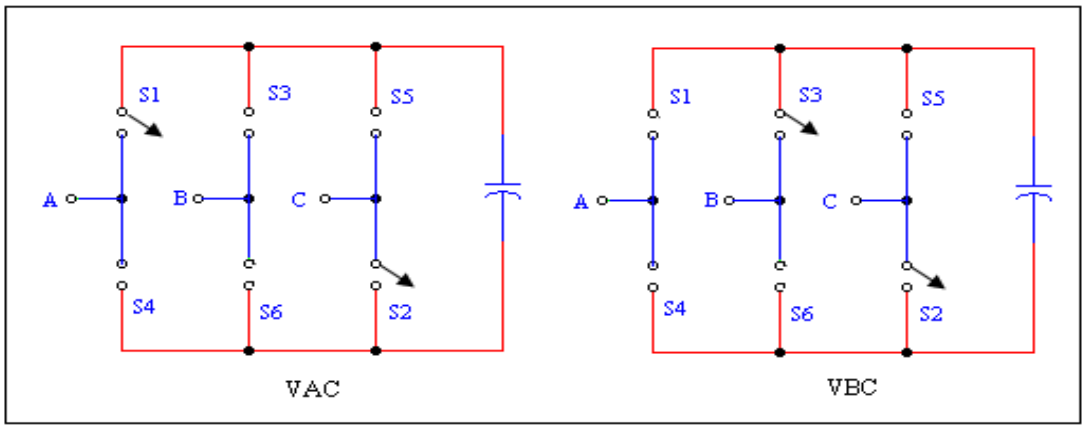
Fig 2.8: AC line-to-line voltage output waveform of the six-pulse VSI

Table 2.2: Conducting periods of the switches

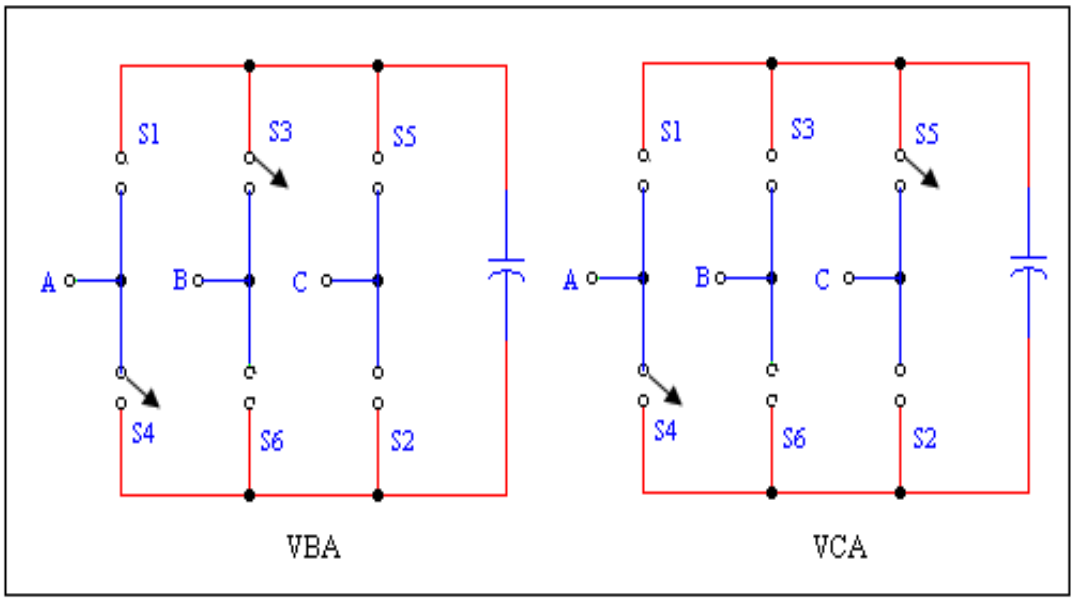
No	Period	High positive voltage	High negative voltage	On switches	
				Odd-numbered	Odd-numbered
1	0^0 to 60^0	C	B	S_5	S_6
2	60^0 to 120^0	A	B	S_1	S_6
3	120^0 to 180^0	A	C	S_1	S_2
4	180^0 to 240^0	B	C	S_3	S_2
5	240^0 to 300^0	B	A	S_3	S_4
6	300^0 to 360^0	C	A	S_5	S_4



(a) Equivalent circuits of line-to-line voltage of CB and AB, respectively



(b) Equivalent circuits of line-to-line voltage of AC and BC, respectively



(c) Equivalent circuits of line-to-line voltage of BA and CA respectively

Fig 2.9: (a) to (c) Equivalent circuits of six-pulse VSI

2.4 Power factor

Power factor is an indispensable issue in the discussion of power quality for many reasons. If the power factor of the system is low, it may cause sensitive devices to fail. In many instances, the low power factor of the utilities can result in a high cost and the utilities find it difficult to meet the resulting demands for electrical energy.

The non-sinusoidal source current due to a non-linear load implies high harmonic content and a low power factor and give rise to low-power transfer efficiency [49]. For sinusoidal signal the power factor is the relationship between the active power, *P,* and the apparent power *S*. If the harmonics are present, there will be an additional power called deforming power (*D*) which also is to be taken into consideration. Hence, the apparent power is composed of three parts the active power, *P*, the reactive power, *Q*, and deforming power, *D*. Figs 2. 10 shows the power in distorted AC network [49], [89].

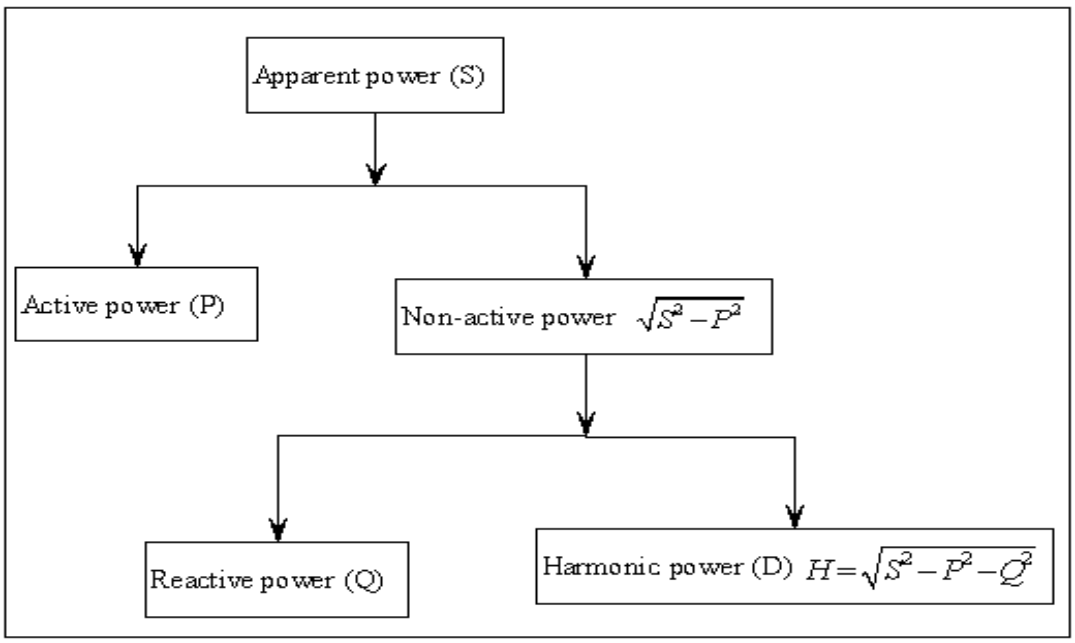


Fig 2.10: Components of power in distorted distribution network

In the case of non-linear loads, however the use of the reactive and the harmonic power is an actual necessity for accomplishing reactive power compensation and for harmonic filtering. The components of the electric apparent power of the system including harmonics is given by the expression (2.1)

$$S = \sqrt{P^2 + Q^2 + D^2} \tag{2.1}$$

The power factor is thus given by:

$$\text{Power factor} = \frac{P}{S} = \frac{P}{\sqrt{P^2 + Q^2 + D^2}} \tag{2.2a}$$

$$\text{or} \quad \text{Power factor} = \frac{V.I_{s1}\cos\varphi_1}{V.I_s} = \frac{I_{s1}}{I_s}\cos\varphi_1 \tag{2.2b}$$

If the SAPF should fully cover the reactive and harmonic powers together, then the total rated power of the SAPF is as in (2.3)

$$S_{APF} = \sqrt{Q^2 + D^2} \tag{2.3}$$

It is to be noted that the deforming power and the reactive power contribute to the degradation of the power factor [49], [50], [89], [90].

2.4.1 Merits of power factor correction

By correcting the low power factor the other benefits besides avoiding penalties imposed by the utilities include [49]:

- Minimization of voltage drop in the electrical system
- Minimization of heat in equipment
- Increased equipment life
- Reduction in cable size (especially in neutral conductor).
- Reduction in energy losses and operating costs
- Freeing up of available energy

2.5 Literature review and background study on application of SAPF

Since 1976, many researchers have approached the power quality problems using SAPFs and a number of designs have been realized both in laboratory and field installations. This part of chapter, gives state-of-the-art literature review of the SAPF. As SAPF is the most important topology among the various APF topologies it is most commonly controlled as a harmonic current source generator based on load current detection for harmonic compensation of identified non-linear loads. The load current harmonics are extracted by a suitable controller which will be discussed in the next chapter. The SAPF injects compensating currents to provide cancellation of load current harmonics. Thus, the supply currents are shaped into sinusoidal or close to sinusoidal waveform according to the harmonic compensation limits of SAPF. The performance and compensation capability of SAPF is not affected by the source inductance, L_S.

A. Terciyanli et. al. [91], presented the design of current-source converter (CSC) based three-wire SAPF to reduce the converter kilovolt-ampere rating. The design is based on the amplification of some selected harmonic current components of CSC by the AC-side filter. The proposed method is used for the elimination of 11^{th} and 13^{th} current harmonics of 12-pulse rectifier loads supplied from a medium-voltage underground cable. The method required a shunt capacitor bank at its AC terminals in order to prevent the power system from dangerous over voltages arising from high

current ripple caused by high-speed switching of power semiconductors. The main drawback is the physical size of CSC in SAPF.

M. Aredes et. al. [62], employed two control schemes to a conventional three-leg converter based three-phase four-wire SAPF. Both control strategies consider harmonics and zero sequence components. The first control strategy is based on the constant source instantaneous power theory strategy and the second one on the sinusoidal source current strategy. A dynamic hysteresis current control was developed to overcome the problems related with the dc voltage difference between DC capacitors. However, the capacitor voltage imbalance is a major problem for this topology as it degrades significantly the performance of the compensator.

J. Wang [92], developed a three-phase three-leg SAPF based on three-phase four-wire circuit instantaneous reactive power theory as a new type of power electronics controller which can filter harmonics as well as compensate reactive power and suppress neutral wire current. Also the system impedance does not influence the SAPF compensation characteristic, as mentioned by the same author. However, the imbalance problems of the DC bus voltage would be a considerable challenge.

N. Mendalek [33], presented modeling and sliding control of a three-phase four-leg split-capacitor SAPF topology, which is aimed to compensate harmonic phase currents, harmonic neutral current and reactive load currents in a four-wire distribution system. Also the DC-link capacitor voltages are regulated and equalized to eliminate the imbalance problem which is due to the presence of the DC component in the neutral wire current. For reliable control, a multivariable state space model of the APF is developed in the synchronous *d-q-0* frame. However, more components are required (additional leg and two capacitors) for this model and the proposed controller design which needs proper selection of sliding mode control parameters is a drawback

L. Chen and Z. JIA [93], have introduced the hardware and software design of a digital controller for SAPF based on double DSP chip of TMS320F2812 for the three-phase four-wire system. The main circuit of the SAPF selects a four-leg voltage

source inverter, and a dynamic hysteresis-band current control is used to track the current. The facility can compensate harmonic and reactive power completely for three-phase four-wire system. Nevertheless, three capacitors and three high pass filters at the DC and AC side of the SAPF, respectively, are used which increases the cost.

C. Madtharad and S. Premrudeepreechachacharn [69], applied neural networks to control three single-phase inverters as SAPF to improve the THD of the load current. However, the controller is very expensive as it involves twelve IGBTs. Moreover the result obtained for THD after compensation is twice the specified value of IEEE-519 standard.

D. Chen et. al. [65], presented a three-phase four-leg SAPF to minimize the neutral current in the Aircraft three-phase four-wire system using a current controller based on three dimensional space vector modulation (3DSVM) strategy suitable for three-phase four-wire system. Nevertheless, the waveforms of the neutral current before and after compensation as well as the THD are not reported.

A SAPF based on one-cycle control (OCC) for compensating unbalanced loads in a three-phase four-wire system is proposed in [68] by S. Hirve et. al. A comparison is made between the simulation results using a four-leg converter and a three-leg converter based APF. However, the results on THD are not reported and the neutral current is not fully compensated. Also unbalance of the dc bus voltage is a major drawback in the proposed method.

Indirect control theory has been proposed for a four-leg SAPF in [94] to compensate reactive power and to balance the load currents. The control for the fourth leg is made different by using the neutral current reference as zero. The proposed solution from the case study is simple and efficient with high utility, as reported by C. Balanuta et al. However, the injection current through SAPF, the neutral current and the THD are not recorded by the author.

A comparative analysis of four control strategies (p-q method, i_d, i_q method, unity power factor method and harmonic cancellation method) for the extraction of the

reference currents of a SAPF connected to a three-phase four-wire source with harmonic distortion and/or imbalance is reported by M. J. Ryan et. al. [47]. It is claimed that the perfect harmonic cancellation method is the only strategy which is capable of eliminating imbalances in the source currents. However the main drawback is unbalance of the dc bus voltage as three-leg split- capacitor SAPF is used

H. Li et.al. [95], proposed a novel current-detection algorithm based on time domain and realized by a DSPIC for three-phase SAPF. Several existing methods based current-detection algorithms are investigated and simulation results are presented. From simulation and experimental results, the author reported several advantages for the presented algorithms. However, all the proposed control algorithms are applicable only for three-phase three-wire SAPF.

A. Bhattacharya and C. Chakraborty [96], reported about an integration of predictive and adaptive properties of artificial neural networks (ANNs) used for fast estimation of the compensating current of a three-wire SAPF for fast convergence and reduced computations. The dynamics of the DC-link voltage of the SAPF is regulated by using an ANN-based PI controller. The system simulation results using MATLAB/SIMULINK and experimental prototype based on dSPACE1104 were claimed by the authors for three-phase three-wire system only.

D. Wu et. al. [48], proposed a design control strategy using a 3 kW SAPF prototype to provide a real-time detection method to separate the neutral wire current. However the authors failed to present the results on neutral current and THD of source currents.

Z. Juan et. al. [70], proposed a scheme using three dimensional SVPWM to control a four-leg SAPF with closed loop PI controller current adjustment to compensate harmonics and reactive power in a three-phase four-wire system. The authors claimed that the proposed approach can be applied to the control of other types of APFs. However, the SVPWM method needs complex calculations and the method fails to improve the power factor.

A seven-level cascaded type inverter is used as SAPF to exploit multilevel inverter

advantages with novel predictive current control as presented by A. M. Massoud et. at. [97]. The capacitor voltage control technique is used as a harmonic current extraction method. Besides, phase-shifted space vector modulation for the multilevel inverter is used as a PWM technique. Also a three-leg SAPF based on cascaded five-level converter with carrier phase shifted sinusoidal pulse width modulation (CPSSPWM) which directly output high voltage without transformers and achieve a high equivalent switching frequency effect at rather low device switching frequency is presented by [98]. The proposed method is limited to a three-wire system and does not consider harmonic suppression limitation and power factor improvement.

P. Xiao et. al. [99], proposed a SAPF configuration that uses tapped reactors for harmonic current sharing which reduces current stress of the switching devices by distributing the compensation current between two parallel legs of an H-bridge topology. It is claimed that the voltage stress across the switches is reduced by utilizing a conventional three-level flying capacitor topology which can produce seven voltage levels, which significantly reduces the switching current ripple and the size of passive components. Nevertheless, there is voltage unbalance associated with a flying capacitor topology and the proposed method is applied to a three-wire system only.

G. Escobar et. al. [100], presented a mathematical model of a cascaded H-bridge three-phase multilevel converter used as a SAPF for a three-wire system. It is claimed that the proposed controller compensate harmonic distortion and reactive power, guarantees regulation and balance all capacitor voltages. The work does not mention THD before and after compensation.

The cascaded H-bridge seven-level inverter with a proposed unipolar-multi carrier technique has been used to realize the three-wire SAPF, was presented by B. Geethalakshmi and K. Delhibabu [101]. The authors claimed that, the proposed unipolar-multi carrier technique gives the benefits of gain in fundamental voltage in over modulation region without loss of control unlike in conventional multi-carrier PWM technique. However only three-phase three-wire system is considered.

A SAPF for a high power system designed with an eleven-level cascaded H-bridge

inverter is presented by D. Mohan et. al. [102]. The compensation currents are extracted from the load using synchronous detection method under multi-carrier phase disposition PWM technique. However, the method deals with three-wire system only.

A seven-level cascaded H-bridge inverter based SAPF is designed to provide harmonic filtering multi-carrier PWM current control method by K. S. Rani and K. Porkumaran [59] which provides low ripple in filter current as claimed by the authors. The analysis and simulation is applicable only to three-wire system

From the literature study, it is observed that many researchers addressed the problems of harmonic suppression, source current THD, power factor correction, neutral current minimization but few rearch papers are published on three-phase four-leg two-level SAPF. The controllers developed are also complex which required more number of components. Moreover the THD of the source current obtained by some researches is above IEEE-519 Standards. Also the results obtained for source neutral current by two-level four-wire SAPF by some researchers is shown to be high. As there is not much published literature on three-phase four-wire multi-level SAPF, it is necessary to establish the compensating performance of five-level and seven-level SAPF by proposing new controlling techniques. Also it is necessary to improve the performance two-level SAPF by the proposed controllers.

2.6 Summary

This chapter has introduced active power filters (APFs), its objectives, benefits and types etc. A brief discussion on classification of VSIs according to their power circuit and their level is presented. An introduction to the three types of multilevel inverters, namely, diode-clamped, flying-capacitors and cascaded H-bridge inverters and their merits and demerits are also reported. As the VSI is the heart of SAPF, a detailed explanation on the principle of operation of the full-wave three-phase VSI is discussed. As power factor is one of the power quality issues the merits of its correction is also introduced. Finally, extensive literatue review and background study on the applications of VSI-based SAPF is reported in this chapter. In the next chapter the research methodology, modeling and simulation of SAPF and the proposed control techniques will be presented.

CHAPTER 3

RESEARCH METHODOLOGY

3.1 Introduction

Harmonics pollution is a major power quality issue which has huge economic impact within power industry and equally affects the consumer. There are several harmonic mitigation methods such as a conventional method by using PPFs which has been extensively used or modern methods by using APFs. In chapter 2, types of APFs, applications and the literature review on the work carried out on SAPF by previous researchers are outlined. In this chapter the system modeling and simulation of SAPF in a distribution network is introduced. The literature on instantaneous power theory for three-phase four-wire system to estimate the reference currents for the SAPF is reviewed. Also three different methods are presented for estimation of reference currents by the proposed controllers.

To minimize the load current harmonics and neutral conductor current, appropriate controllers are proposed for SAPF followed by a discussion on modulation techniques for two-level, five-level and seven-level VSI. Also to develop a model of VSI based SAPF, the design aspect of important parameters of VSI are outlined. Simulation models for two-level and five/seven-level SAPF developed by MATLAB/ SIMULINK are presented at the end of this chapter.

3.2 Research sequence

The steps involved in the implementation of this study are summarized by Fig 3.1 comprising three important phases which are mastering simulation tools, literature review and study on problems of supply side current.

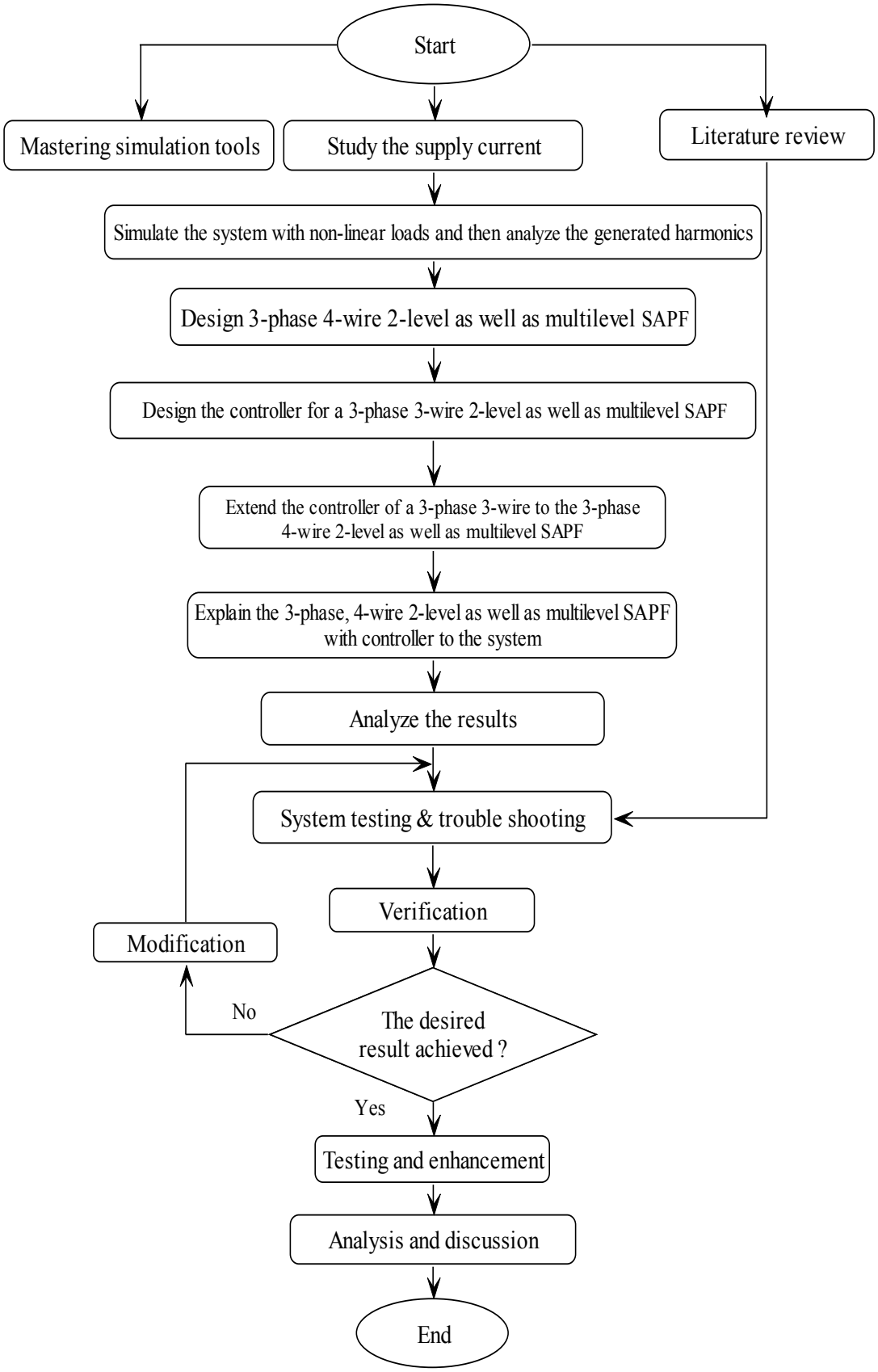


Fig 3.1: Research work flow

3.3 Distribution system with shunt active power filter

Fig 3. 2 shows a single line diagram of a distribution system with the three-phase AC source, source impedance, Zs, power system bus, and mixed non-linear loads consisting of one 6-pulse three-phase controlled rectifier and three single-phase uncontrolled rectifiers. A VSI based SAPF is connected to the network at PCC. A DC capacitor C_{dc} acts as an energy storage source. The capacitor provides the reactive power and harmonic power to the non-linear loads and a small amount of active power to meet the losses of VSI.

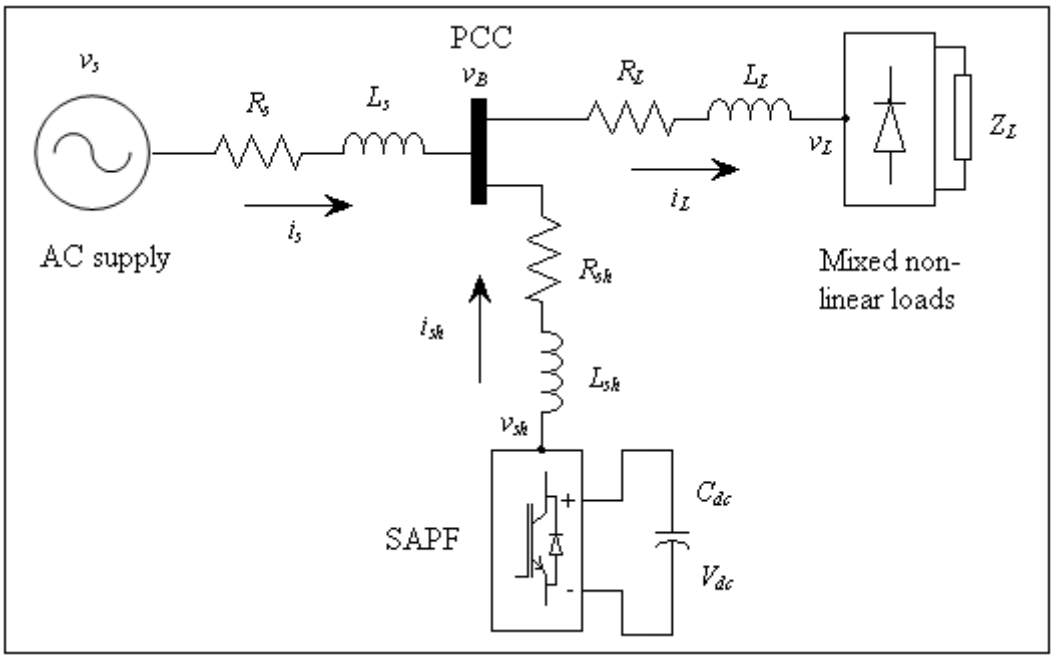


Fig 3.2: Single line diagram of the distribution system with SAPF

Referring to Fig 3. 2, the instantaneous voltages for balanced sinusoidal three-phase system are expressed as

$$v_{sa} = V_{sm}\sin(\omega t) \tag{3.1}$$

$$v_{sb} = V_{sm}\sin(\omega t - 2\pi/3) \tag{3.2}$$

$$v_{sc} = V_{sm}\sin(\omega t - 4\pi/3) \tag{3.3}$$

In a similar manner the instantaneous currents are expressed as in (3.4) to (3.6)

$$i_{sa} = I_{sm}\sin(\omega t - \phi) \tag{3.4}$$

$$i_{sb} = I_{sm} \sin(\omega t - \phi - 2\pi / 3) \tag{3.5}$$

$$i_{sc} = I_{sm} \sin(\omega t - \phi - 4\pi / 3) \tag{3.6}$$

The mixed non-linear loads draw fundamental and harmonic current components, i_{Lf}, i_{LH}, respectively, from the source. The harmonic part of load current is compensated by SAPF. Expressing the fundamental and harmonic components of voltage and current as,

$$v_s = v_{sf} + v_{sH} \tag{3.7}$$

$$i_s = i_{sf} + i_{sH} \tag{3.8}$$

$$i_L = i_{Lf} + i_{LH} \tag{3.9}$$

When the current harmonics are successfully eliminated, the reactive power is compensated and subsequently power factor obtained is close to unity. At that time the source only supply fundamental component of current, and can be expressed as,

$$i_s = i_{Lf} \tag{3.10}$$

Applying KCL at PCC of Fig 3.1,

$$i_{sa} = i_{La} - i_{sha} \tag{3.11}$$

$$i_{sb} = i_{Lb} - i_{shb} \tag{3.12}$$

$$i_{sc} = i_{Lc} - i_{shc} \tag{3.13}$$

By applying KVL, to the system shown in Fig 3. 2, the sum of instantaneous voltages of the AC supply, the load and the AC side of the SAPF are given by the following equations:

$$v_{sa} - v_{Ba} = R_s i_{sa} + L_s \frac{di_{sa}}{dt} \tag{3.14}$$

$$v_{sb} - v_{Bb} = R_s i_{sb} + L_s \frac{di_{sb}}{dt} \tag{3.15}$$

$$v_{sc} - v_{Bc} = R_s i_{sc} + L_s \frac{di_{sc}}{dt} \tag{3.16}$$

$$v_{Ba} - v_{La} = R_L i_{La} + L_L \frac{di_{La}}{dt}$$

(3.17)

$$v_{Bb} - v_{Lb} = R_L i_{Lb} + L_L \frac{di_{Lb}}{dt}$$

(3.18)

$$v_{Bc} - v_{Lc} = R_L i_{Lc} + L_L \frac{di_{Lc}}{dt} \tag{3.19}$$

$$v_{sha} - v_{Ba} = R_{sh} i_{sha} + L_{sh} \frac{di_{sha}}{dt} \tag{3.20}$$

$$v_{shb} - v_{Bb} = R_{sh} i_{shb} + L_{sh} \frac{di_{shb}}{dt} \tag{3.21}$$

$$v_{shc} - v_{Bc} = R_{sh} i_{shc} + L_{sh} \frac{di_{shc}}{dt} \tag{3.22}$$

Equations (3.14) to (3.16) are represented in matrix form as in (3.23) [15], [35], [38], [46], [103]-[105].

$$\frac{d}{dt}\begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} = \begin{bmatrix} -R_s / L_s & 0 & 0 \\ 0 & -R_s / L_s & 0 \\ 0 & 0 & -R_s / L_s \end{bmatrix}\begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} + \frac{1}{L_s} * \begin{bmatrix} v_{sa} - v_{Ba} \\ v_{sb} - v_{Bb} \\ v_{sc} - v_{Bc} \end{bmatrix} \tag{3.23}$$

3.4 Instantaneous power theory for three-phase, four-wire system

Conventional methods dealing with instantaneous power can be classified either as time-domain or frequency-domain. In this research the time-domain method is used to deal with instantaneous power which can be divided into two main groups. The first group provides the transformation of the three-phase instantaneous voltages and currents from *a-b-c* phases to three-orthogonal axes such as *α-β-0* coordinates (Clark Transformation), while the other group is based directly on the *a-b-c* phases. The compensation reference currents for generating control signals are obtained from the instantaneous real and reactive power components.

By using Clarke transformation, the three-phase instantaneous voltages, v_a, v_b, and v_c of the three-phase four-wire distribution system can be transformed into *α-β-0* quantities and vice versa as in (3.24) and (3.25), respectively.

$$\begin{bmatrix} v_0 \\ v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\tfrac{2}{3}} \begin{bmatrix} 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\ 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{3.24}$$

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \sqrt{\tfrac{2}{3}} \begin{bmatrix} 1/\sqrt{2} & 1 & 0 \\ 1/\sqrt{2} & -1/2 & \sqrt{3}/2 \\ 1/\sqrt{2} & -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} v_0 \\ v_\alpha \\ v_\beta \end{bmatrix} \tag{3.25}$$

In a similar manner the instantaneous currents, i_a, i_b, and i_c can be transformed into *α-β-0* quantities and vice versa as given in (3.26) and (3.27)

$$\begin{bmatrix} i_0 \\ i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\tfrac{2}{3}} \begin{bmatrix} 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\ 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{3.26}$$

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \sqrt{\tfrac{2}{3}} \begin{bmatrix} 1/\sqrt{2} & 1 & 0 \\ 1/\sqrt{2} & -1/2 & \sqrt{3}/2 \\ 1/\sqrt{2} & -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_0 \\ i_\alpha \\ i_\beta \end{bmatrix} \tag{3.27}$$

By using Park transformation, the three-phase instantaneous voltages and currents of the *a-b-c* coordinates can be transformed into synchronous direct axis (*d*), quadrature axis (*q*) and zero-sequence reference coordinates (phase quantities to synchronous reference). In this case first the three-phase voltages and currents are transformed from *a-b-c* coordinates into stationary coordinates by using Clarke transformation, as in (3.24) and (3.26), respectively, and then the inverse Clarke transformation can be applied as in (3.25) and (3.27), respectively. The quantities in stationary reference frame are transformed into synchronous rotating frame by utilizing Park transformation as in (3.28) and (3.29) for voltages and currents,

respectively, and then inverse Park transformation can be applied as in (3.30) and (3.31), respectively.

$$\begin{bmatrix} v_0 \\ v_d \\ v_q \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & \cos(\omega t) & \sin(\omega t) \\ 0 & -\sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} v_0 \\ v_\alpha \\ v_\beta \end{bmatrix} \tag{3.28}$$

$$\begin{bmatrix} i_0 \\ i_d \\ i_q \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & \cos(\omega t) & \sin(\omega t) \\ 0 & -\sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} i_0 \\ i_\alpha \\ i_\beta \end{bmatrix} \tag{3.29}$$

$$\begin{bmatrix} v_0 \\ v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & \cos(\omega t) & -\sin(\omega t) \\ 0 & \sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} v_0 \\ v_d \\ v_q \end{bmatrix} \tag{3.30}$$

$$\begin{bmatrix} i_0 \\ i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & \cos(\omega t) & -\sin(\omega t) \\ 0 & \sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} i_0 \\ i_d \\ i_q \end{bmatrix} \tag{3.31}$$

By substituting the voltages and currents of (3.24) and (3.26) in (3.28) and (3.29), respectively, the transformation from reference frame *a-b-c* coordinates to synchronous rotating frame *d-q-0* coordinates will be obtained as in (3.32) and (3.33), respectively.

$$\begin{bmatrix} v_0 \\ v_d \\ v_q \end{bmatrix} = \sqrt{\tfrac{2}{3}} \begin{bmatrix} 1 & 0 & 0 \\ 0 & \cos(\omega t) & \sin(\omega t) \\ 0 & -\sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\ 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{3.32}$$

$$\begin{bmatrix} i_0 \\ i_d \\ i_q \end{bmatrix} = \sqrt{\tfrac{2}{3}} \begin{bmatrix} 1 & 0 & 0 \\ 0 & \cos(\omega t) & \sin(\omega t) \\ 0 & -\sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\ 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{3.33}$$

Park inverse transformation, *d-q-0* coordinates to the *a-b-c* coordinates for voltages and currents are obtained as in (3.34) and (3.35), respectively, by substituting the voltages and currents of (3.24) and (3.26) in (3.30) and (3.31), respectively.

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \sqrt{\tfrac{2}{3}} \begin{bmatrix} 1 & 0 & 0 \\ 0 & \cos(\omega t) & -\sin(\omega t) \\ 0 & \sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} 1/\sqrt{2} & 1 & 0 \\ 1/\sqrt{2} & -1/2 & \sqrt{3}/2 \\ 1/\sqrt{2} & -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} v_0 \\ v_d \\ v_q \end{bmatrix} \tag{3.34}$$

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \sqrt{\tfrac{2}{3}} \begin{bmatrix} 1 & 0 & 0 \\ 0 & \cos(\omega t) & -\sin(\omega t) \\ 0 & \sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} 1/\sqrt{2} & 1 & 0 \\ 1/\sqrt{2} & -1/2 & \sqrt{3}/2 \\ 1/\sqrt{2} & -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_0 \\ i_d \\ i_q \end{bmatrix} \tag{3.35}$$

The complex instantaneous apparent power, s, is represented as

$$s = v^* i = p + jq \tag{3.36}$$

The instantaneous voltage and current in the *α-β* stationary frame are given as $v_\alpha + jv_\beta$ and $i_\alpha + ji_\beta$, respectively. Substituting these values of instantaneous voltage and current in equation (3.36), the complex instantaneous power in the *α-β* stationary frame is result as in (3.37)

$$s = (v_\alpha + jv_\beta)^*(i_\alpha + ji_\beta) = (v_\alpha - jv_\beta)(i_\alpha + ji_\beta) \tag{3.37a}$$

$$s = v_\alpha i_\alpha + v_\beta i_\beta + j(v_\alpha i_\beta - v_\beta i_\alpha) \tag{3.37b}$$

By separating the real and imaginary parts of the (3.37b), the active and reactive powers are obtained as in (3.38) and (3.39), respectively.

$$p = v_\alpha i_\alpha + v_\beta i_\beta \tag{3.38}$$

$$q = v_\alpha i_\beta - v_\beta i_\alpha \tag{3.39}$$

In three-phase four-wire system there is an additional instantaneous zero-sequence voltage, v_0 and current, i_0, respectively. The resultant power from is called zero-sequence instantaneous power, p_0, and is given as in (3.40)

$$p_0 = v_0 i_0 \tag{3.40}$$

The three independent quantities, zero-sequence, real and imaginary instantaneous powers from (3.38) to (3.40), can be expressed by the following matrix equation

$$\begin{bmatrix} p_0 \\ p \\ q \end{bmatrix} = \begin{bmatrix} v_0 & 0 & 0 \\ 0 & v_\alpha & v_\beta \\ 0 & -v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} i_0 \\ i_\alpha \\ i_\beta \end{bmatrix} \tag{3.41}$$

The three-phase instantaneous active power, $p_{3\Phi}$, in a three-phase system with or without neutral is calculated as the product of instantaneous phase voltages and instantaneous line currents as

$$p_{3\phi} = v_a(t)i_a(t) + v_b(t)i_b(t) + v_c(t)i_c(t) = v_a i_a + v_b i_b + v_c i_c \tag{3.42}$$

Also the three-phase instantaneous active power, $p_{3\Phi}$, can be expressed in terms of the *α-β-0* quantities as in (3.43) [13], [34], [106]-[110].

$$p_{3\phi} = v_\alpha i_\alpha + v_\beta i_\beta + v_0 i_0 = p + p_0 \tag{3.43}$$

3.4.1 Estimation of reference currents and components of power

The estimation of the reference current for the controller can be accomplished in two ways. In the first method the calculation is based on zero-sequence values from the beginning, and in the second method the calculation is first accomplished for the *α-β* quantities and then the zero-sequence values are included.

3.4.1.1 Method 1

For the first method equation (3.44) shows the inverse transformation of (3.41)

$$\begin{bmatrix} i_0 \\ i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} v_0 & 0 & 0 \\ 0 & v_\alpha & v_\beta \\ 0 & -v_\beta & v_\alpha \end{bmatrix}^{-1} \begin{bmatrix} p_0 \\ p \\ q \end{bmatrix} \tag{3.44}$$

separating zero-sequence, real and imaginary instantaneous powers equation (3.44) can be rewritten as in (3.45)

$$\begin{bmatrix} i_0 \\ i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} v_0 & 0 & 0 \\ 0 & v_\alpha & v_\beta \\ 0 & -v_\beta & v_\alpha \end{bmatrix}^{-1} \begin{bmatrix} p_0 \\ 0 \\ 0 \end{bmatrix} + \begin{bmatrix} v_0 & 0 & 0 \\ 0 & v_\alpha & v_\beta \\ 0 & -v_\beta & v_\alpha \end{bmatrix}^{-1} \begin{bmatrix} 0 \\ p \\ 0 \end{bmatrix} + \begin{bmatrix} v_0 & 0 & 0 \\ 0 & v_\alpha & v_\beta \\ 0 & -v_\beta & v_\alpha \end{bmatrix}^{-1} \begin{bmatrix} 0 \\ 0 \\ q \end{bmatrix} \tag{3.45}$$

The zero-sequence, active and reactive components of the current, can be expressed as in (3.46) by rewriting equation (3.41).

$$\begin{bmatrix} i_0 \\ i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} i_0 \\ 0 \\ 0 \end{bmatrix} + \begin{bmatrix} 0 \\ i_{\alpha p} \\ i_{\beta p} \end{bmatrix} + \begin{bmatrix} 0 \\ i_{\alpha q} \\ i_{\beta q} \end{bmatrix}$$

(3.46)

In a similar manner as in (3.46), the instantaneous currents of the *a*-*b*-*c* quantities of equation (3.27) can be expressed as follows:

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \sqrt{\tfrac{2}{3}} \begin{bmatrix} 1/\sqrt{2} & 1 & 0 \\ 1/\sqrt{2} & -1/2 & \sqrt{3}/2 \\ 1/\sqrt{2} & -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_0 \\ 0 \\ 0 \end{bmatrix} + \sqrt{\tfrac{2}{3}} \begin{bmatrix} 1/\sqrt{2} & 1 & 0 \\ 1/\sqrt{2} & -1/2 & \sqrt{3}/2 \\ 1/\sqrt{2} & -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} 0 \\ i_{\alpha p} \\ i_{\beta p} \end{bmatrix}$$
$$+ \sqrt{\tfrac{2}{3}} \begin{bmatrix} 1/\sqrt{2} & 1 & 0 \\ 1/\sqrt{2} & -1/2 & \sqrt{3}/2 \\ 1/\sqrt{2} & -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} 0 \\ i_{\alpha q} \\ i_{\beta q} \end{bmatrix} \tag{3.47}$$

Equation (3.47) can be simplified as in equation (3.48) which gives zero-sequence, active and reactive components of currents of '*a*', '*b*' and '*c*' phases.

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} i_{a0} \\ i_{b0} \\ i_{c0} \end{bmatrix} + \begin{bmatrix} i_{ap} \\ i_{bp} \\ i_{cp} \end{bmatrix} + \begin{bmatrix} i_{aq} \\ i_{bq} \\ i_{cq} \end{bmatrix} \tag{3.48}$$

The reference currents derived from equation (3.48) are i_{aq}, i_{bq} and i_{cq} for the phases '*a*', '*b*' and '*c*', respectively and can be renamed as i_{fa}^{*}, i_{fb}^{*} and i_{fc}^{*}. The reference current of neutral, i_{fn}^{*} is calculated as in equation (3.49).

$$i_{fn}^{*} = i_{fa}^{*} + i_{fb}^{*} + i_{fc}^{*} \tag{3.49}$$

By using equation (3.48), the instantaneous powers p_a, p_b and p_c of phases '*a*', '*b*' and '*c*', respectively, can be expressed as in (3.50)

$$\begin{bmatrix} p_a \\ p_b \\ p_c \end{bmatrix} = \begin{bmatrix} v_a i_{a0} \\ v_b i_{b0} \\ v_c i_{c0} \end{bmatrix} + \begin{bmatrix} v_a i_{ap} \\ v_b i_{bp} \\ v_c i_{cp} \end{bmatrix} + \begin{bmatrix} v_a i_{aq} \\ v_b i_{bq} \\ v_c i_{cq} \end{bmatrix} \tag{3.50}$$

Also equation (3.50) can be expressed as zero-sequence, active and reactive components of power as in (3.51)

$$\begin{bmatrix} p_a \\ p_b \\ p_c \end{bmatrix} = \begin{bmatrix} p_{a0} \\ p_{b0} \\ p_{c0} \end{bmatrix} + \begin{bmatrix} p_{ap} \\ p_{bp} \\ p_{cp} \end{bmatrix} + \begin{bmatrix} p_{aq} \\ p_{bq} \\ p_{cq} \end{bmatrix} \tag{3.51}$$

The instantaneous reactive components of the power p_{aq}, p_{bq} and p_{cq} from equation (5.51) make no contribution to instantaneous power flow in the three-phase system because the sum of instantaneous reactive components of power is always equal to zero as in equation (3.52).

$$p_{aq} + p_{bq} + p_{cq} = 0 \tag{3.52}$$

In terms *α-β-0* quantities the three-phase active power of the three-phase four-wire system can be expressed as:

$$p_{3\varphi}(t) = p_{\alpha} + p_{\beta} + p_{0} = p_{\alpha p} + p_{\alpha q} + p_{\beta p} + p_{\beta q} + p_{0} \tag{3.53}$$

When the reactive components of the power of α and β quantities are zero, then the three-phase active power of the three-phase four-wire system can be expressed as:

$$p_{3\varphi}(t) = p_{\alpha p} + p_{\beta p} + p_{0}$$

(3.54)

Method 2

For the estimation of reference currents by the second method, the powers of the *α-β* quantities only are expressed first as:

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{3.55}$$

From the equation (3.55) the determinant of the first matrix is determined as

$$\Delta = v_\alpha^2 + v_\beta^2 \tag{3.56}$$

By inverse transformation of equation (3.55), the *α-β* components of current can be expressed as in (3.57)

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{1}{\Delta} \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} p \\ q \end{bmatrix} \tag{3.57}$$

Equation (3.58) shows active and reactive components of current of the equation (3.57)

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{1}{\Delta} \begin{bmatrix} v_\alpha & -v_\beta \\ v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} p \\ 0 \end{bmatrix} + \frac{1}{\Delta} \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} 0 \\ q \end{bmatrix} \cong \begin{bmatrix} i_{\alpha p} \\ i_{\beta p} \end{bmatrix} + \begin{bmatrix} i_{\alpha q} \\ i_{\beta q} \end{bmatrix} \tag{3.58}$$

From equation (3.58), the instantaneous active and reactive components of current in terms of α-*β* components can be expressed as in (3.59) and (3.60), respectively.

$$i_{\alpha p} = v_\alpha p / \Delta, \quad i_{\beta p} = v_\beta p / \Delta \tag{3.59}$$

$$i_{\alpha q} = -v_\beta q / \Delta, \quad i_{\beta q} = v_\alpha q / \Delta \tag{3.60}$$

At this stage the zero-sequence current is included to estimate the reference currents based on α-*β*-*0* quantities as $-i_0$, $i_{\alpha q}$ and $i_{\beta q}$, and can be expressed in terms of *a-b-c* phase currents as i_{fa}^*, i_{fb}^* and i_{fc}^*. Similar to equation (3.37), these reference currents can be expressed as in equation (3.61)

$$\begin{bmatrix} i_{fa}^{*} \\ i_{fb}^{*} \\ i_{fc}^{*} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1/\sqrt{2} & 1 & 0 \\ 1/\sqrt{2} & -1/2 & \sqrt{3}/2 \\ 1/\sqrt{2} & -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} -i_0 \\ i_{\alpha q} \\ i_{\beta q} \end{bmatrix} \tag{3.61}$$

The reference current of the neutral i_{fn}^{*}, can be calculated in a similar manner as in (3.49), which is

$$i_{fn}^{*} = i_{fa}^{*} + i_{fb}^{*} + i_{fc}^{*} \tag{3.62}$$

Instantaneous active power in *α-β* reference frame is calculated by using the instantaneous voltages and currents and then can be separated into active and reactive components as in (3.63)

$$\begin{bmatrix} p_{\alpha} \\ p_{\beta} \end{bmatrix} = \begin{bmatrix} v_{\alpha} i_{\alpha} \\ v_{\beta} i_{\beta} \end{bmatrix} = \begin{bmatrix} v_{\alpha} i_{\alpha p} \\ v_{\beta} i_{\beta p} \end{bmatrix} + \begin{bmatrix} v_{\alpha} i_{\alpha q} \\ v_{\beta} i_{\beta q} \end{bmatrix} \cong \begin{bmatrix} p_{\alpha p} \\ p_{\beta p} \end{bmatrix} + \begin{bmatrix} p_{\alpha q} \\ p_{\beta q} \end{bmatrix} \tag{3.63}$$

By substituting the active and reactive components of current of equations (3.59) and (3.60) in (3.63), the active components of the real power of *α-β* quantities can be expressed as in (3.64) and (3.65), respectively.

$$p_{\alpha p} = v_{\alpha} i_{\alpha p} = v_{\alpha}^{2} p / \Delta \tag{3.64}$$

$$p_{\beta p} = v_{\beta} i_{\beta p} = v_{\beta}^{2} p / \Delta \tag{3.65}$$

In a similar manner, the reactive components of the real power of *α-β* quantities can be expressed as in (3.66) and (3.67), respectively.

$$p_{\alpha q} = v_{\alpha} i_{\alpha q} = -v_{\alpha} v_{\beta} q / \Delta \tag{3.66}$$

$$p_{\beta q} = v_{\beta} i_{\beta q} = v_{\alpha} v_{\beta} q / \Delta \tag{3.67}$$

3.4.2 DC and AC components of power

One of the major merits of using the *p-q* theory for controller design of SAPF is the possibility of independently selecting the portions of real, imaginary, and

zero-sequence compensating powers. Sometimes, it is convenient to separate these powers into their average and oscillating parts (DC and AC components) by using low or high-pass filters as in equations (3.68) to (3.70)

$$p_o = \overline{p}_o + \tilde{p}_o \tag{3.68}$$

$$p = \overline{p} + \tilde{p} \tag{3.69}$$

$$q = \overline{q} + \tilde{q} \tag{3.70}$$

To have a good system performance, it is important to compensate all undesirable power components generated by non-linear loads that can damage or make the power system overloaded or stressed by harmonic pollution. In this way, it would be desirable for a three-phase balanced power-generating system to supply only the average component of active power of the load. Meanwhile, all other power components required by the nonlinear load, i.e. average and oscillating parts of reactive and zero-sequence instantaneous powers as well as the oscillating part of active power, should be compensated by the SAPF [39], [30], [43], [111]. In this thesis, three methods are used to estimate the reference currents of the SAPF controller, which are: *p-q* theory, *d-q-0* theory and *a-b-c* theory methods.

3.5 Control strategy of SAPF

A number of control strategies can be used to estimate the reference currents for SAPF, such as, *p-q* theory, synchronous reference frame method (*d-q-0* theory), *a-b-c* theory, etc. The harmonic producing loads are assumed to be current sources and SAPF behaves as an ideal current source capable of injecting desired compensation currents. The SAPF can be used to control currents based on three major harmonic component detection methods [26]:

i. Load current detection: This method detects the load currents, which flow downstream of the PCC, and then extracts harmonic currents from the load currents.

ii. Source current detection: This method detects the source currents, which escapes upstream of the PCC, and then extracts harmonic currents from the source currents.

iii. Voltage detection: This method detects the bus voltages at the PCC, and then extracts harmonic voltages from the bus voltages.

The compensating current, i_{sh} in time domain for the above three detection methods is expressed as follows: [26]

Load current detection: $i_{sh} = i_{LH}$

Source current detection: $i_{sh} = K_s * i_{sH}$

Voltage detection: $i_{sh} = K_v * v_H$

where i_{LH} is the load harmonic current, i_{sH} is the source harmonic current and v_H is the voltage harmonic at PCC.

Here, K_s have no dimension while K_v has the dimension of (l/Ω). The SAPF itself, in each method, acts as the current source of i_{sh}. In case of voltage detection method, it behaves like a pure resistor of $1/K_v$ (Ω). Out of these three methods, the load current detection method requires less effort for computation and is also accurate because it extracts harmonic currents direct from non-linear load current.

3.6 Proposed controllers for SAPF

The SAPF controller estimates the reference currents and generates the control signals for the IGBTs of VSI. The hysteresis current control with fixed band is implemented here to generate the switching pattern for IGBTs in order to get precise and quick response. The hysteresis band current control technique has proven to be the most suitable for all applications of current control in a two-level VSI based SAPF. Furthermore the hysteresis band current controller which uses a relay controller is superior in terms of easy implementation and quick current controllability with minimum software and hardware [111].

The reference injection currents of the SAPF are referred to as i_f^* and the actual injection currents by the SAPF are referred to as i_{sh} as shown in Fig. 3. 3. The control of SAPF can be realized by the hysteresis control technique by forcing the SAPF compensation current, i_{sh} signal to follow its estimated reference signal, i_f^* within a certain tolerance band. The measured i_{sh} is compared with i_f^* and the resulting error is subjected to the relay controller in hysteresis block to determine the switching pattern of two-level SAPF, whereas in multilevel the resulting error is compared with the triangle carrier in order to generate the switching pattern [11], [111]-[113].

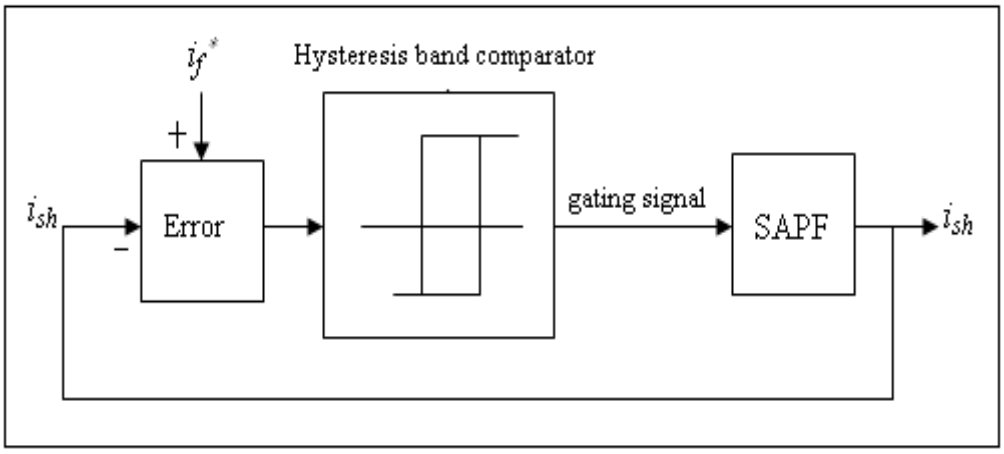


Fig 3.3: Hysteresis band current control technique of SAPF

3.6.1 Proposed controller based on *p-q* theory and hysteresis band current controller

A controller is developed by extending *p-q* theory introduced in [114] to control a three-phase four-leg SAPF as shown in Fig. 3. 4. The simulation model as shown in Fig. 3. 5 consist of a hysteresis current control block as shown in Appendix B and the *p-q* theory based reference current calculation block. The VSI based SAPF receives the gating signals from hysteresis current control block. The control circuit is implemented based on the instantaneous power theory discussed in section 3.3. Based on a number of simulation experiments a high-pass filter (cutoff frequency = 2000 Hz, damping factor, ζ = 0.707 and sampling time $1x10^{-8}s$) is designed to extract the DC component of the real power and then the AC component is used in order to estimate the reference currents.

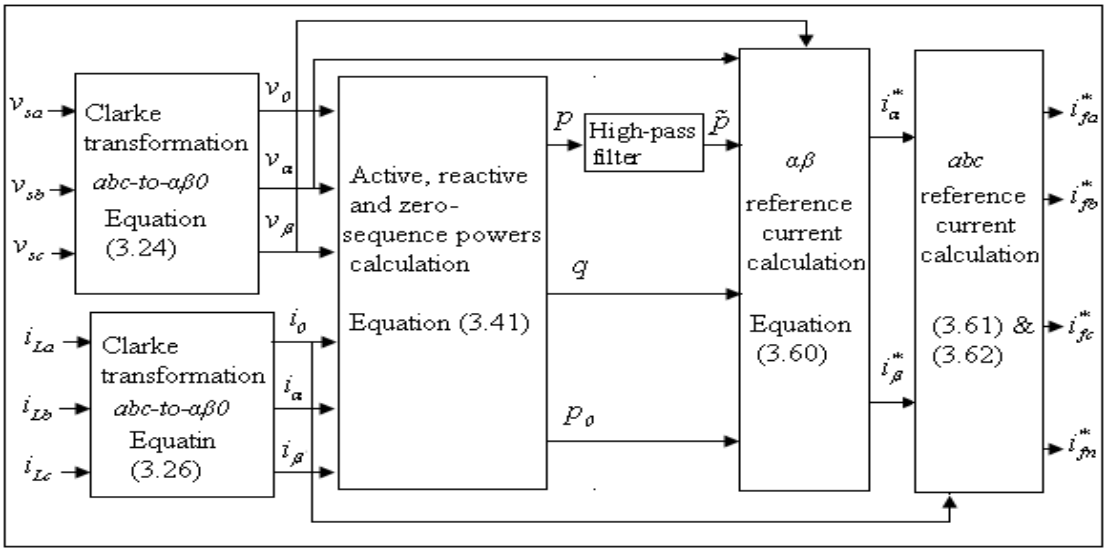


Fig 3.4: Proposed controller based on the *p–q* theory

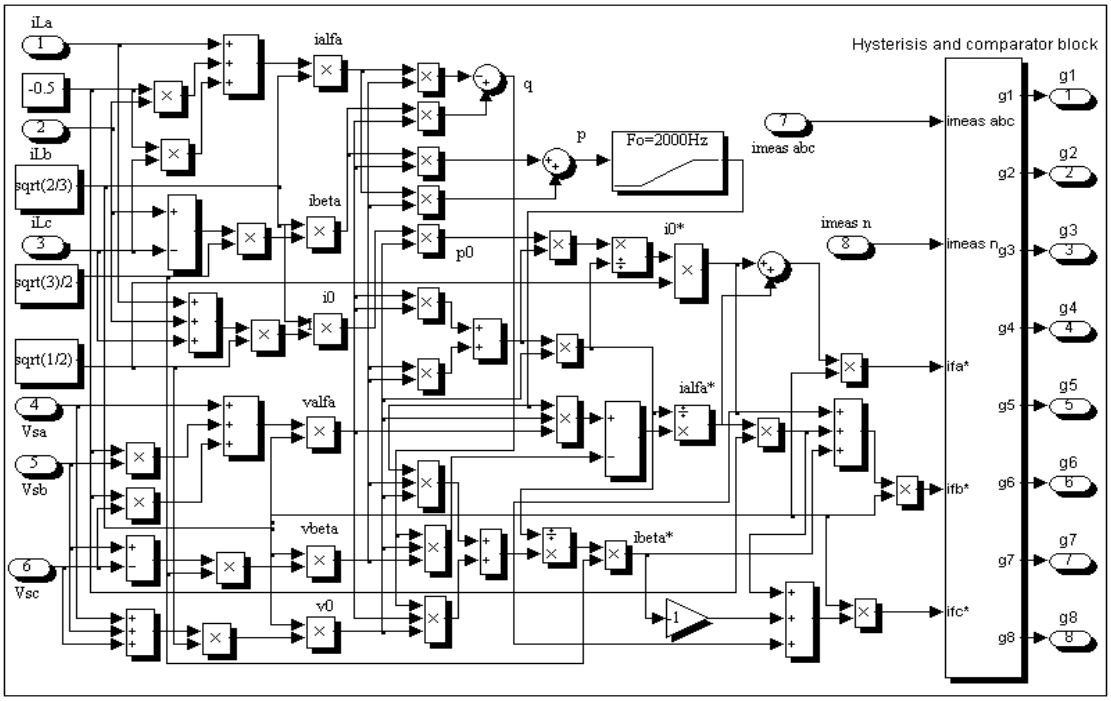


Fig 3.5: Simulation model of the proposed controller based on *p-q* theory

3.6.2 Proposed controller based on synchronous reference frame (*d-q-0* theory)

In *d-q-0* reference frame theory less effort is required and minimum equipment is needed to estimate the reference currents. First, the load current are sensed and

transformed from the *a-b-c* frame to the *d-q-0* synchronous reference frame using Park's transformation. The transformed i_d, i_q component currents are then passed through high-pass filters with the following specifications, based on numerous experiments it was found that (cutoff frequency = 100 Hz and damping factor, $\zeta = 0.2$), which will eliminate the fundamental components of the currents and leaves only the harmonic components. The filtered components i_d^* i_q^* together with i_0 represents the reference currents which will be compared with the actual SAPF currents. The resulting error will be subjected to a relay controller (hysteresis block) in order to generate the switching pattern of SAPF. Figs. 3. 6 and 3. 7 show the block diagram and the simulation model of the proposed controller for the three-phase four-leg SAPF which is developed based on *d-q-0* theory and hysteresis band current control.

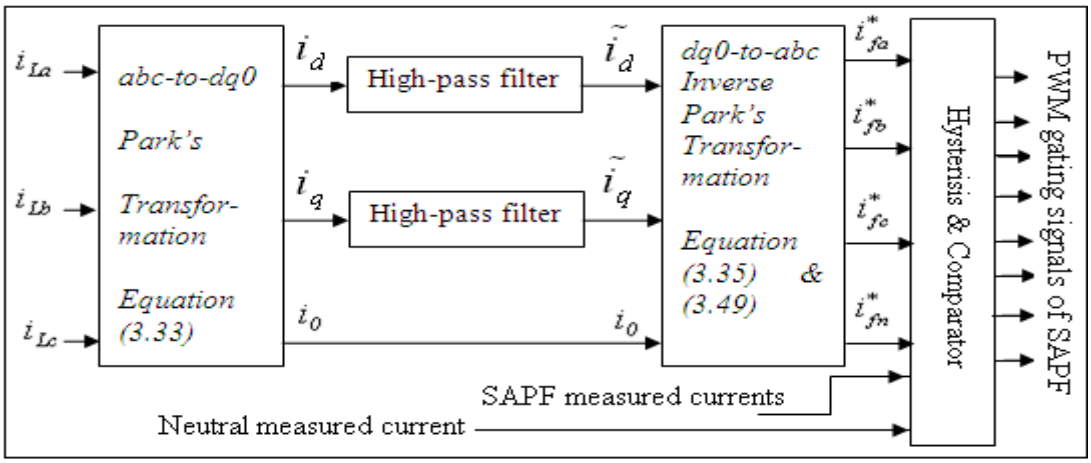


Fig 3.6: Proposed controller based on the *d–q-0* theory

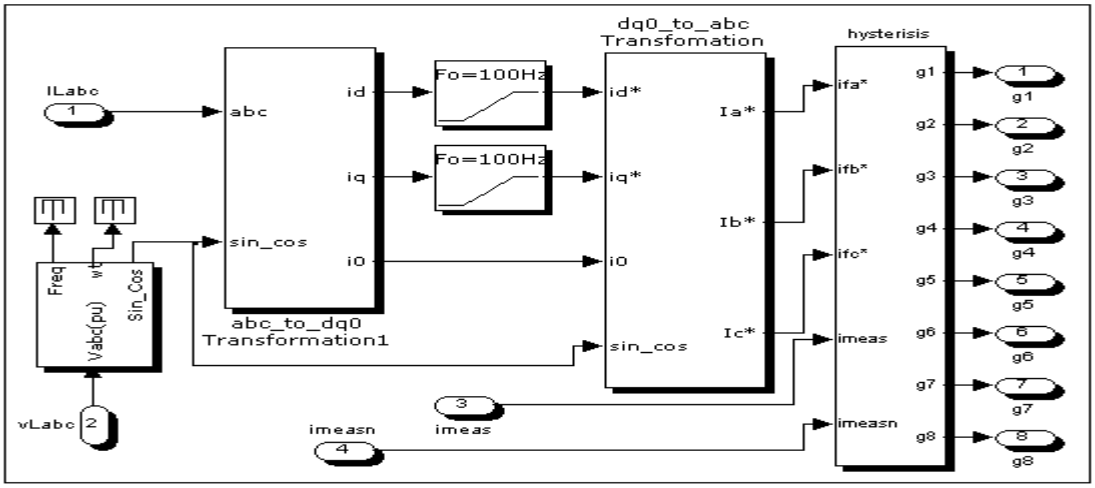


Fig 3.7: Simulation model of the proposed controller based on *d-q-0* theory

3.6.3 Proposed controller based on *a-b-c* theory

In this proposed control strategy, the load currents are detected by PLL to generate the reference currents of the phases '*a*', '*b*' and '*c*' based on *a-b-c* theory without axis transformation. The resulting reference currents are compared with the actual currents injecting by the SAPF and then the resulting error is subjected to a relay controller in order to determine the desired switching pattern of the SAPF. The SAPF aims to inject the compensation currents at the PCC in order to suppress the harmonics, to minimize the neutral current and to improve the power factor. The simulation model of the proposed current controller of a three-phase four-leg SAPF is shown in Fig. 3. 8. The circuit of the proposed controller consists of the hysteresis band current control block and the load current detection based reference current calculation, the subsystem blocks of PLL and RMS as presented in Appendix B. The SAPF receives the gating signals from the hysteresis current control blocks of the switching pattern generation which are shown in Fig. 3. 8.

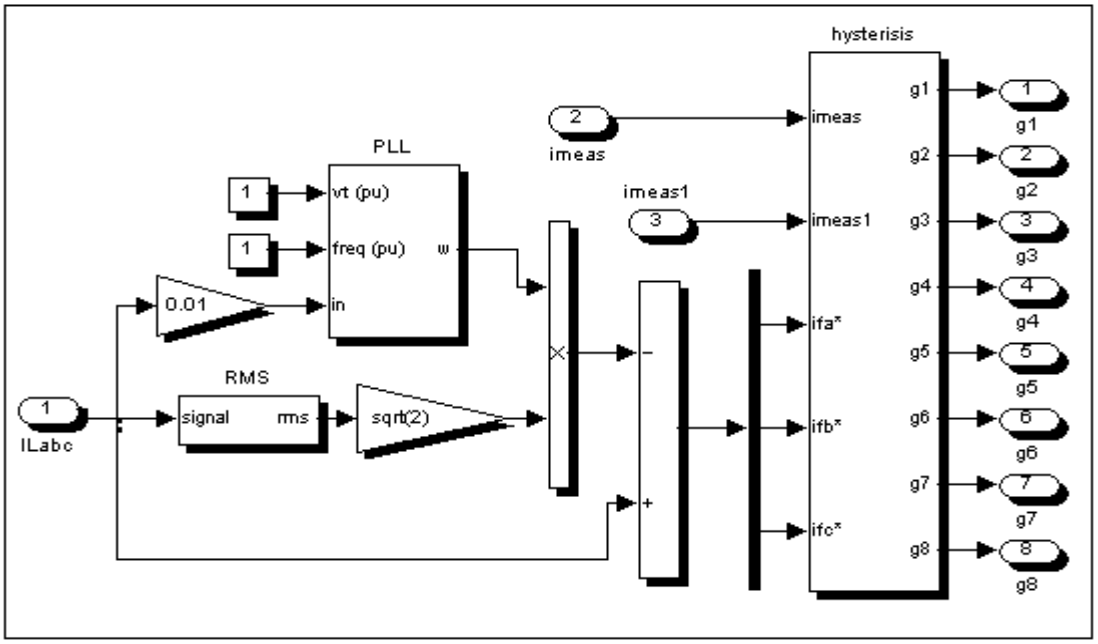


Fig 3.8: Simulation model of the proposed current control based on *a-b-c* theory

3.7 Modulation techniques

The PWM control is the most widely used method of controlling the modulation

depth of inverters for both the two-level and multilevel family. A significant amount of research has been published on various ways of implementing PWM control. The focus here is on carrier-based sinusoidal PWM schemes for controlling a cascaded multilevel inverter. The SPWM schemes are more flexible and simpler to implement to the multilevel inverters. The carrier-based modulation techniques for multilevel VSIs can be generally classified into phase-shifted and level-shifted modulations which are discussed in this thesis. Both modulation schemes can be employed to the cascaded H-bridge (CHB) VSI. The SPWM technique, when applied to multilevel inverters, uses a number of level-shifted carrier waves to compare with reference phase voltage or current signals.

3.7.1 SPWM modulation technique for two-level VSI

The basic principle of the SPWM used to control the current in two-level VSI is explained here. The control signals which are generally sinusoidal and 120^{o} out of phase are compared with the high frequency triangle wave (carrier signal) of constant amplitude as shown in Fig 3. 9. When the control signal is greater than the carrier signal, the PWM output will be high (+1), and the output will be low (-1) otherwise. In general, the modulation index, $m_a = (control\ \ signal)/(carrier\ \ signal)$ is defined as the ratio of the magnitude of the control signal to that of the magnitude of the carrier signal, where m can be greater than zero and equal or less than one [115].

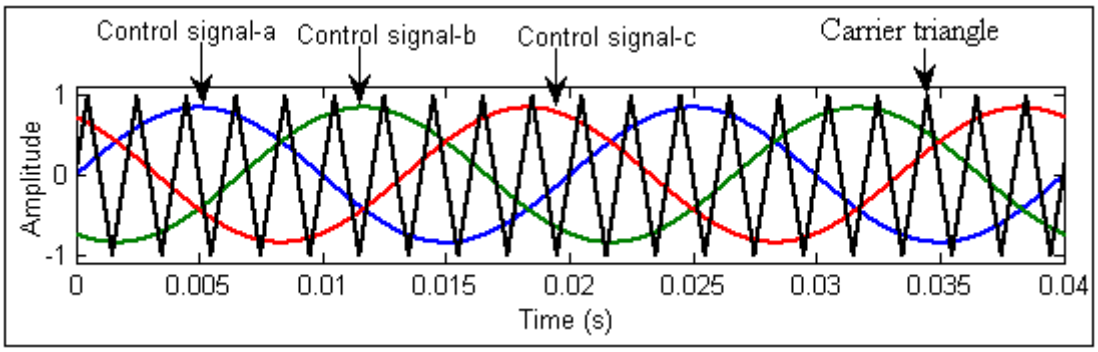


Fig 3.9: A generalized SPWM strategy of three-phase two-level VSI

The six PWM pulses generated by the scheme of Fig. 3. 9 are shown in Fig 3. 10 which are programmed to control six IGBTs of SAPF. The odd numbered pulse train

is used to trigger the upper side devices of the first, second, and third arms of VSI and the even numbered pulse train is used to trigger the lower side switches.

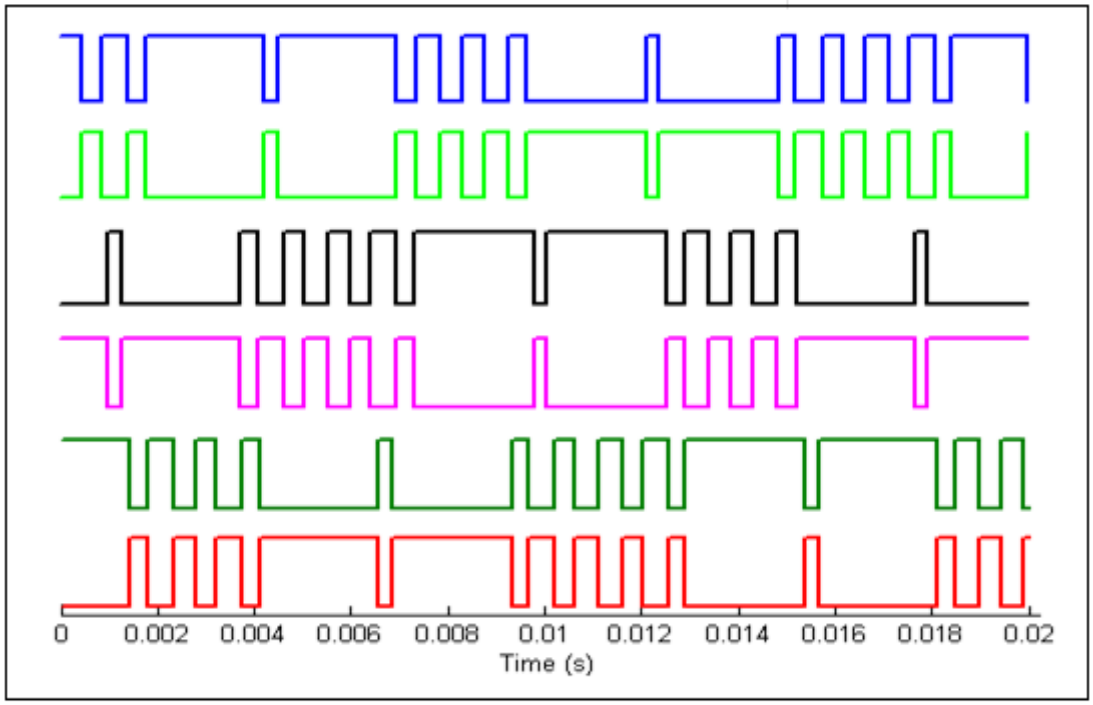


Fig 3.10: Six pulses generated by the SPWM to control a three-arm VSI.

3.7.2 Phase-shifted sinusoidal PWM (PS-SPWM) for multilevel VSI

The most common PWM method used for CHB-VSIs is the PS-SPWM which can maintain a good controllability. For an *M*-level CHB-VSI, the sinusoidal modulation signal is compared with *M-1* triangular carrier signals that are phase shifted by 360/(*M-1*) degrees. The generated PWM signals control the corresponding switches. In Fig. 3. 11, the four triangular carrier waveforms each with 360°/4 phase shift accompanied by sinusoidal modulation waveform are shown. Similarly Fig. 3. 12 shows, the six triangular carrier waveforms each with 360°/6 phase shift accompanied by sinusoidal modulation waveform. By comparing these carriers and the modulation waveform, the PWM signals for a five-level and seven-level CHB-VSI will be generated. The PWM gating signals, output line-to-line and phase voltages of the five-level CHB-VSI are shown as in Appendix C [116].

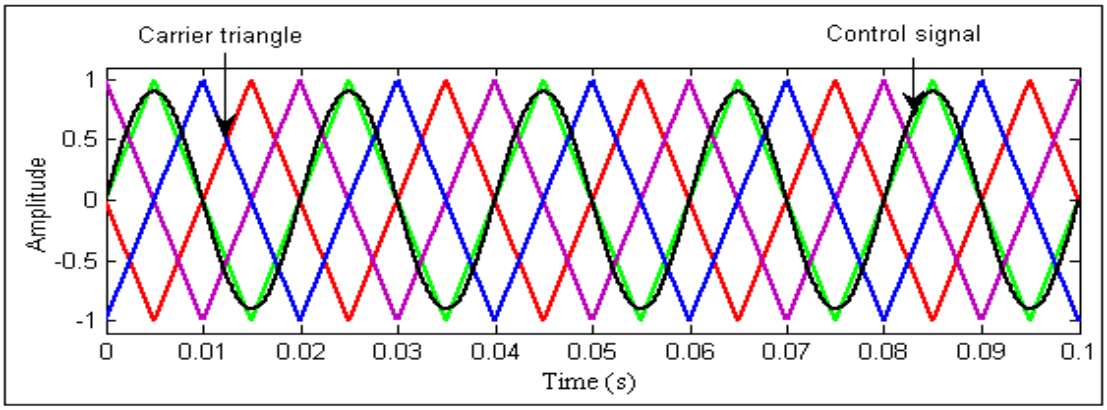


Fig 3.11: Phase-shifted PWM for five-level CHB-VSI

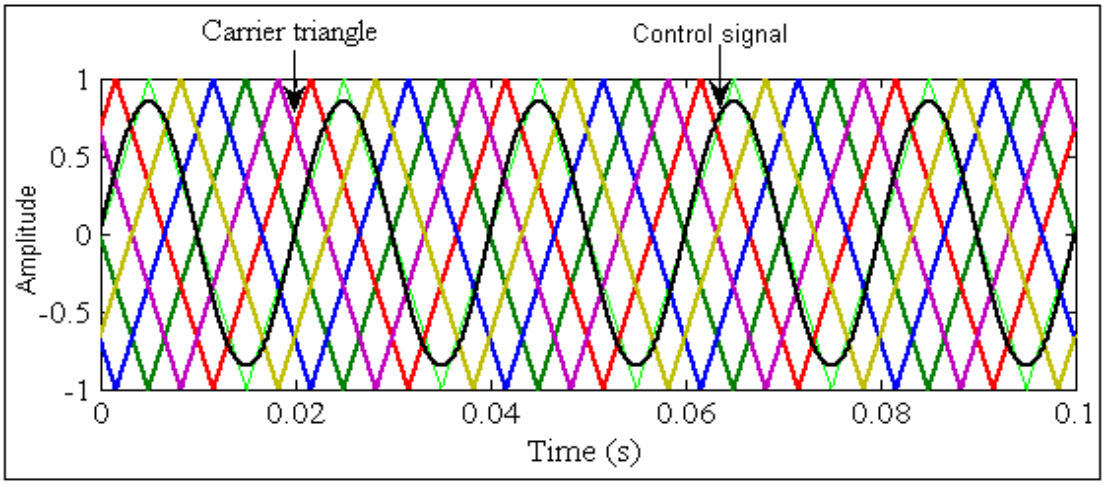


Fig 3.12: Phase-shifted PWM for seven-level CHB-VSI

3.7.3 Level-shifted SPWM (LS-SPWM) for multilevel VSI

LS-SPWM is the natural extension of a bipolar PWM for multilevel VSI. Bipolar PWM is a popular and easiest technique to implement. By generalizing the bipolar PWM idea for a multilevel inverter, several triangle carrier signals which are required can be determined by using *M-1* carriers and only one reference or modulation signal per phase. The carriers are arranged in vertical shifts instead of the phase-shift used in PS-SPWM. Each carrier is set between two voltage levels; hence the name level-shifted. Since each carrier is associated with two levels, the same principle of bipolar PWM can be applied. Actually, there are three main alternative LS-PWM strategies which are employed with the multilevel VSI in order to maintain the switching gate control. A brief discussion on these three strategies i.e. in-phase disposition, alternative phase opposite disposition and phase opposite disposition

[115], [116] is outlined here. The PWM gating signals, output line-to-line and phase voltages of five-level CHB-VSI are shown as in Appendix C.

3.7.3.1 In-phase disposition (IPD)

In-phase disposition (IPD) method use carriers of same frequency, amplitude and phases, but differ in DC offset to occupy contiguous bands as shown in Fig 3. 13

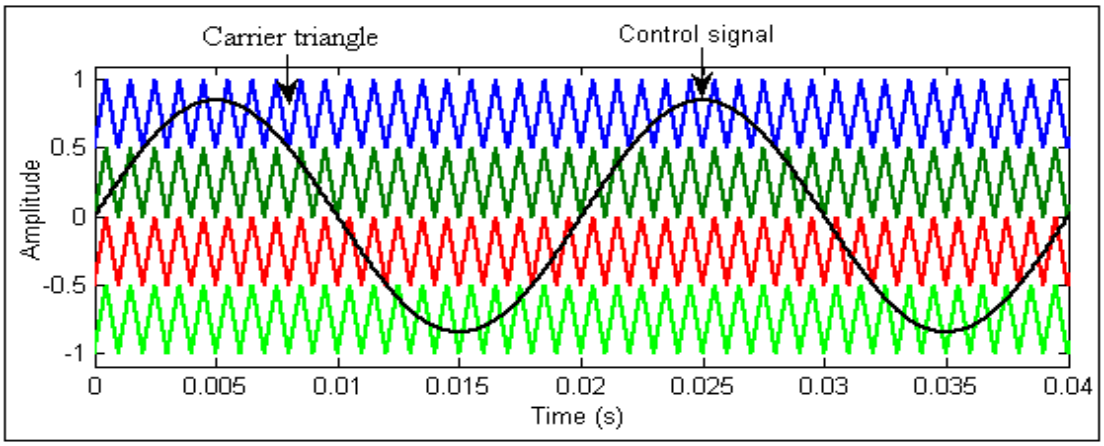


Fig 3.13: IPD modulation for five-level CHB-VSI

and 3. 14 for five-level and seven-level VSI, respectively. The carriers are in phase across all the bands. In this technique, four and six triangular carriers are selected for five-level and seven-level, respectively based on the formula $M-1$, i.e *5-1 = 4* and *7-1 = 6*, respectively [115], [116].

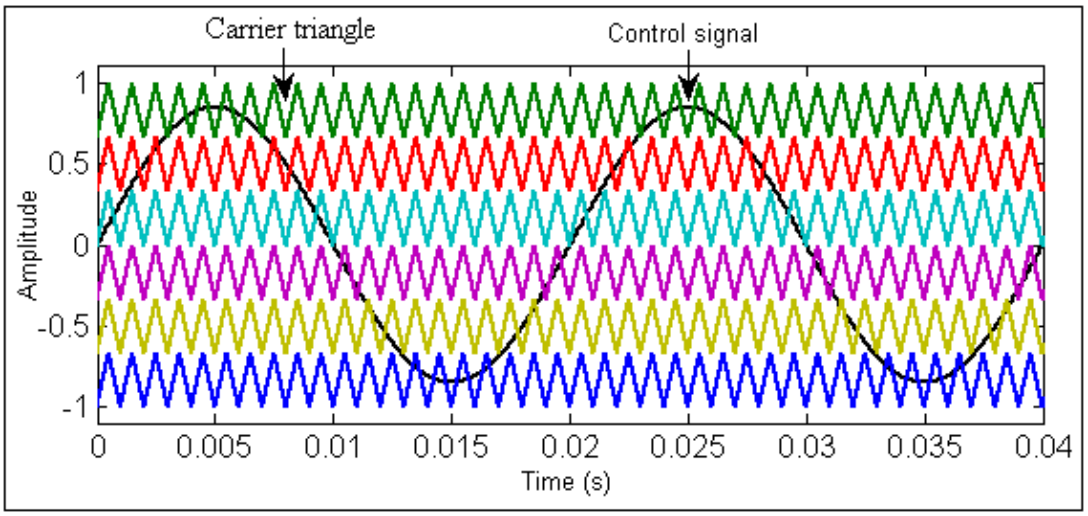


Fig 3.14: IPD modulation for seven-level CHB-VSI

3.7.3.2 Alternative phase opposite disposition (APOD)

Alternative phase opposite disposition (APOD) method use carriers of same frequency and same amplitude but differ in their DC offset and phases as shown in Figs. 3. 15 and 3. 16 for five-level and seven-level, respectively. In this method the

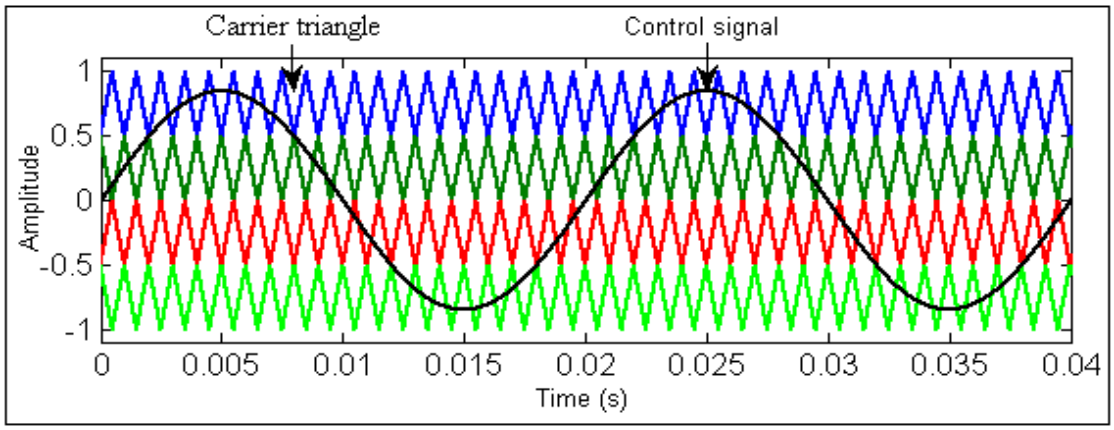


Fig 3.15: APOD modulation for five-level CHB-VSI

carriers are phase shifted by 180^{o} such that two degrees of freedom of carriers namely their DC-offset and phases are available. In APOD the carriers in adjacent bands are phase shifted by 180^{o} [115].

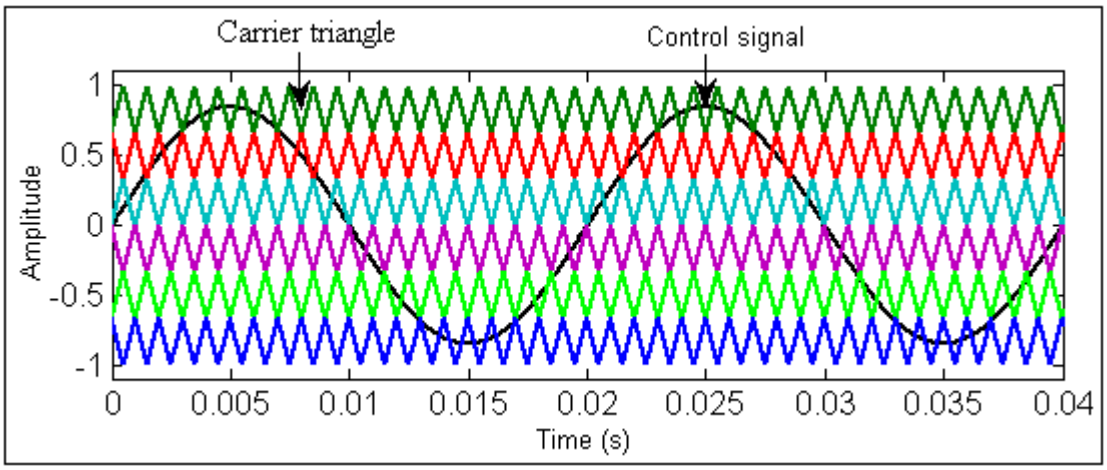


Fig 3.16: APOD modulation for seven-level CHB-VSI

3.7.3.3 Phase opposite disposition (POD)

In case of phase opposite disposition (POD) method the carriers are the same in

frequency and amplitude but they are again different in phase and DC offset as the case of APOD. In this technique the carriers above the zero reference are in phase, but shifted by 180^{o} from those carriers below the zero reference, Figs. 3. 17 and 3. 18 shows the modulation techniques for five-level and seven-level, respectively [115].

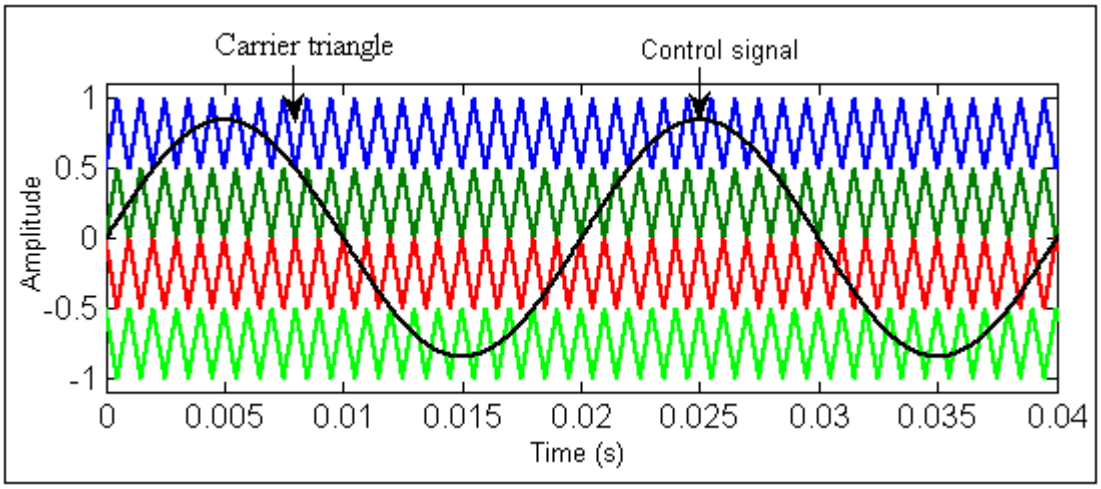


Fig 3.17: POD modulation for five-level CHB-VSI

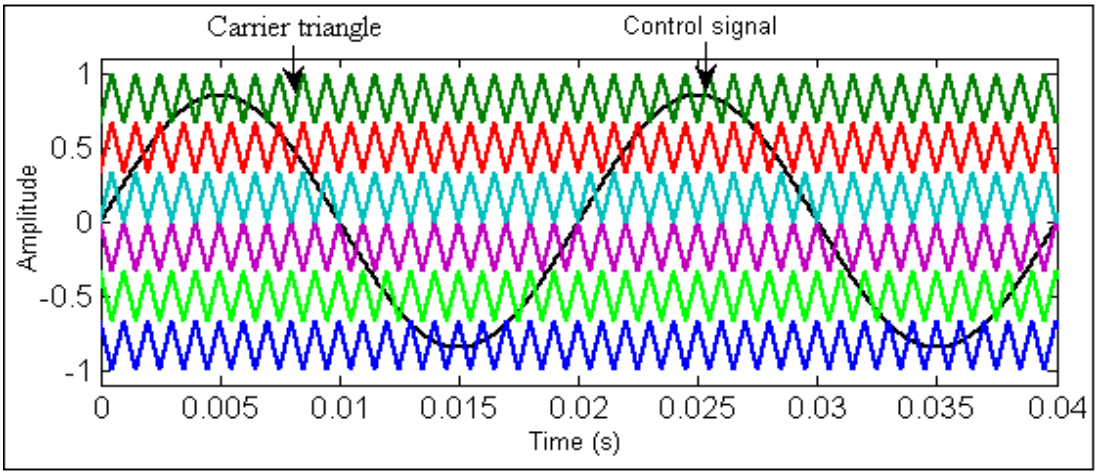


Fig 3.18: POD modulation for seven-level CHB-VSI

3.8 Parameters selection of VSI based SAPF

Apart from the IGBT switches of VSI, the other important parameters in the design of the SAPF are the DC-link voltage (V_{dc}), the value of DC storage capacitor (C_{dc}), the interface inductor (L_{sh}) and switching frequency (f_s). A proper selection of these parameters offers a satisfactory compensation performance for the SAPF.

3.8.1 Selection of DC-link voltage (V_{dc})

From several simulation and experimental studies which are carried out by a number of researchers, the value of V_{dc} is determined by an empirical rule applied to the three-phase VSIs with balanced loads. Subsequently for optimal SAPF compensation performance, the value of V_{dc} can be varied between 50 % to 100 % greater than the maximum line voltage v_{lm}, of the AC supply [18], [21], [117]. Thus V_{dc} can be expressed as in (3.71)

$$1.5v_{lm} \le V_{dc} \le 2v_{lm} \tag{3.71}$$

3.8.2 Selection of DC-capacitor (C_{dc})

The energy storage device, C_{dc} is a large capacitor connected at the input terminals of the SAPF, which is used to make the input V_{dc} constant. A capacitor can store electric energy and when disconnected from its charging circuit, it can be used like a temporary battery. Estimation of the value of C_{dc} is based on the following assumptions

i. The SAPF is connected to a system rated at X kVA.
ii. Under transient conditions for n cycles the SAPF can handle half and twice the capacity of the system.
iii. The capacitor can change its voltage, V_{dc} from $1.5v_{lm}$ to $2v_{lm}$, where v_{lm} is the maximum line voltage

Thus the change in energy that can be handled by C_{dc} is

$$\Delta E = (2X - 0.5X)nT \tag{3.72}$$

Initial energy, E stored by C_{dc}

$$E = 0.5C_{dc}(V_{dc})^2 \tag{3.73}$$

The change in energy should be supported by the energy stored by C_{dc} [18], [118], [119].

From equations (3.72) and (3.73),

$$0.5C_{dc}[(2v_{lm})^2 - (1.5v_{lm})^2] = (2X - 0.5X)nT \quad (3.74)$$

Hence,

$$C_{dc} = 2(2X - 0.5X)nT / [(2v_{lm})^2 - (1.5v_{lm})^2] \quad (3.75)$$

3.8.3 Selection of interface inductance

The interface inductor, L_{sh}, connected at the AC side of SAPF plays a very important role in the design of the SAPF which will limit the ability of SAPF to tackle harmonics. The THD of the compensated currents is strongly dependent on the switching frequency of the IGBTs, and on the value of L_{sh}. The value of L_{sh} is selected based on the equation (3.76) [18], [31].

$$L_{sh} = V_{dc} / (4hf_{s\max})$$

(3.76)

where h = hysteresis band and f_{smax} = maximum switching frequency

3.9 Three-phase four-wire PDN with SAPF

The basic operating principle of SAPF is outlined here. The three-phase non-linear load which consists of a six-pulse controlled thyristor rectifier draws a non-sinusoidal current with positive and negative sequence harmonics. The three single-phase uncontrolled diode rectifiers which are connected beside the six-pulse controlled rectifier act as single-phase non-linear loads and as a result the neutral current is present in PDN. The SAPF is connected to the PDN at PCC through a circuit breaker. The main objective of the SAPF is to prevent the current harmonics to circulate through AC mains impedance and hence avoid the distortion of the voltage at PCC. In addition the SAPF is to minimize the neutral current by mitigating the load harmonic currents. These objectives of the SAPF can be accomplished by controlling the active filter in order to generate harmonic currents which match in magnitude and phase with those existing in the load current.

3.9.1 Simulation model with two-level SAPF

Fig 3. 19 illustrates the MATLAB/SIMULINK simulation model of the three-phase four-leg two-level SAPF which is used to suppress the harmonic content propagated to the source from the mixed non-linear loads as well as to minimize the neutral current in a three-phase four-wire PDN. The model is developed by using a SAPF with IGBT inverter, a series inductor on the AC side and a capacitor as an energy storage element at DC side. The mixed non-linear loads consist of one three-phase six-pulse thyristor rectifier and three single-phase diode rectifiers. Fig 3. 20 shows some of the measurement blocks of a three-phase four-wire PDN including two-level SAPF connected at the PCC.

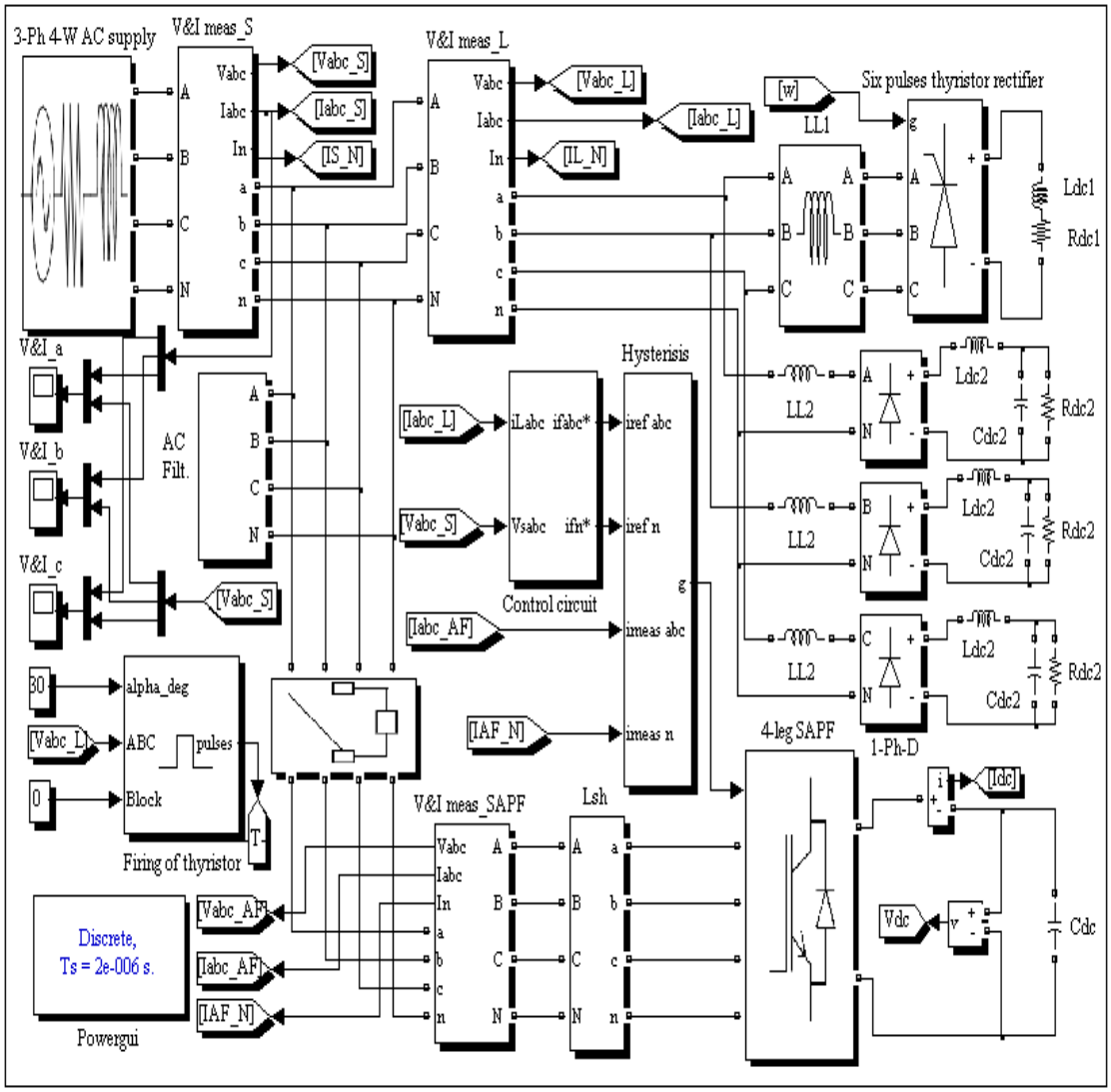


Fig 3.19: Simulation model with two-level SAPF

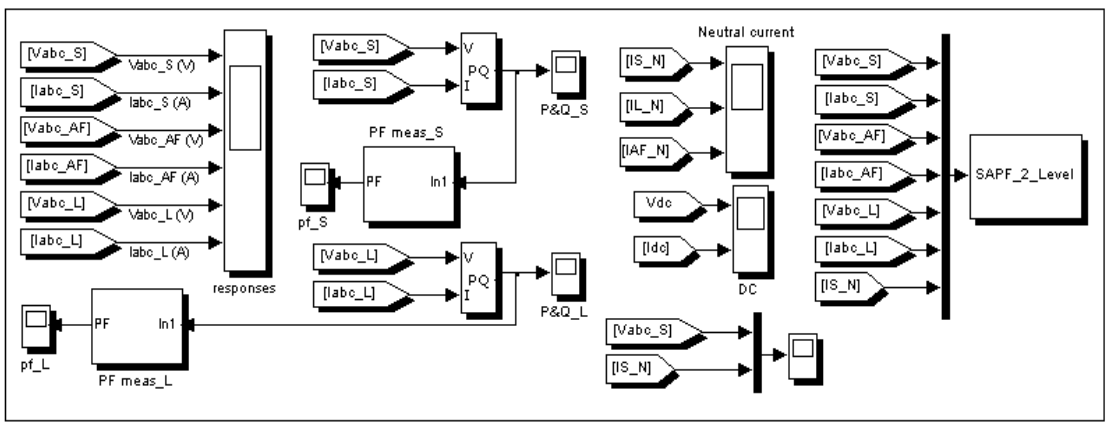


Fig 3.20: Measurement blocks of a three-phase four-wire PDN with two-level SAPF

3.9.2 Simulation model with five-level/seven-level SAPF

Fig 3. 21 illustrates the simulation model of the five/seven-level three-phase four-wire CHB-VSI based SAPF.

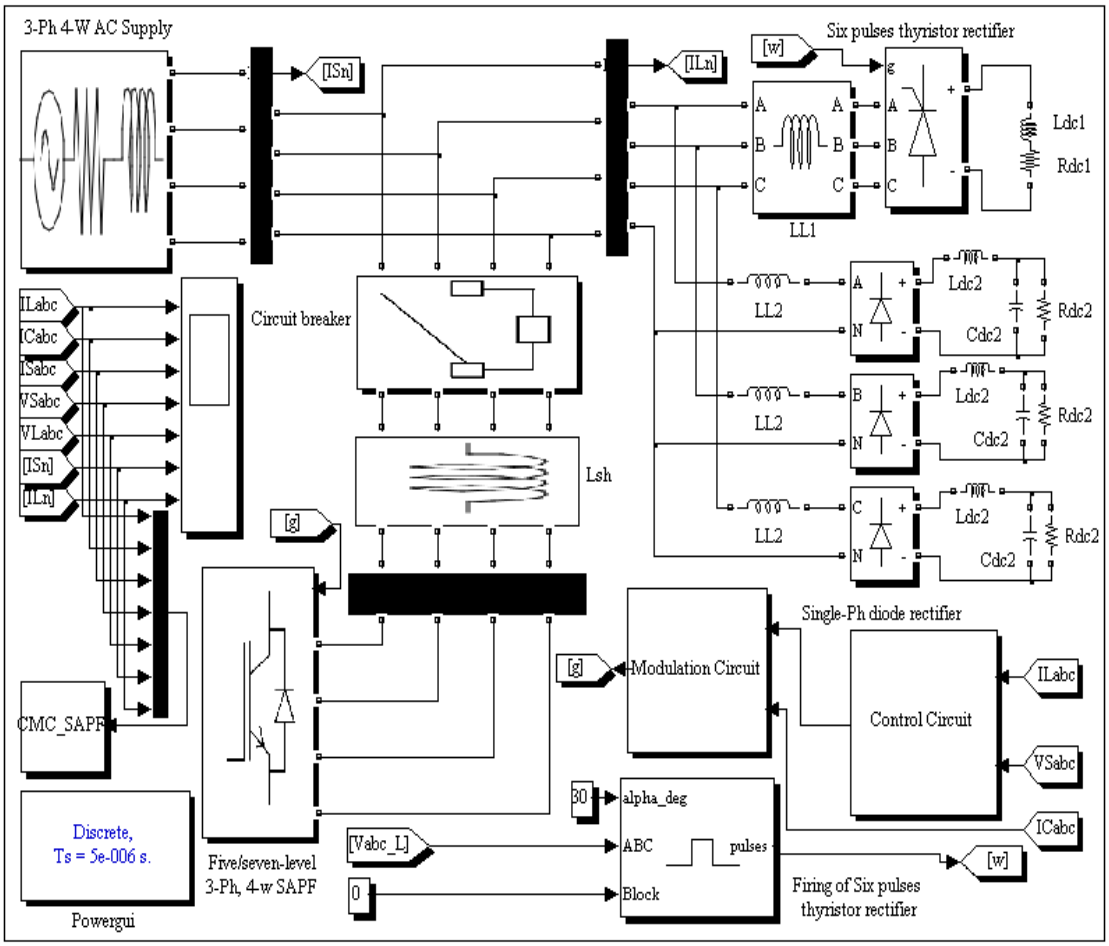


Fig 3.21: Simulation model with five/seven-level SAPF

Figs. 3. 22 and 3. 24 shows the simulation models of power circuit of the five-level and seven-level CHB-VSI based SAPF, respectively. Figs. 3. 23 and 3. 25 shows the simulation models of gate pulse generation for five-level and seven-level CHB-VSI based four-wire SAPF, respectively. The three-phase four-wire structure of the five-level CHB-VSI based SAPF can be maintained by the wye-connection as shown in Fig. 3. 22 which consists of twenty-four IGBTs with six capacitors as energy storage elements. Similarly the three-phase four-wire structure of the seven-level CHB-VSI based SAPF can be obtained, which consists of thirty-six IGBTs with nine capacitors, as in Fig. 3. 24. The three-phase four-wire five-level CHB-VSI consists of cascaded single-phase full-bridge VSI with separate DC-link capacitor. A five-level CHB-VSI requires two modules of the single-phase full-bridge VSI in each phase and a seven-level CHB-VSI needs three modules of the single-phase full-bridge VSI in

each phase. In general, the number of modules per phase for an M level CHB-VSI is equal to $(M-1)/2$ [105].

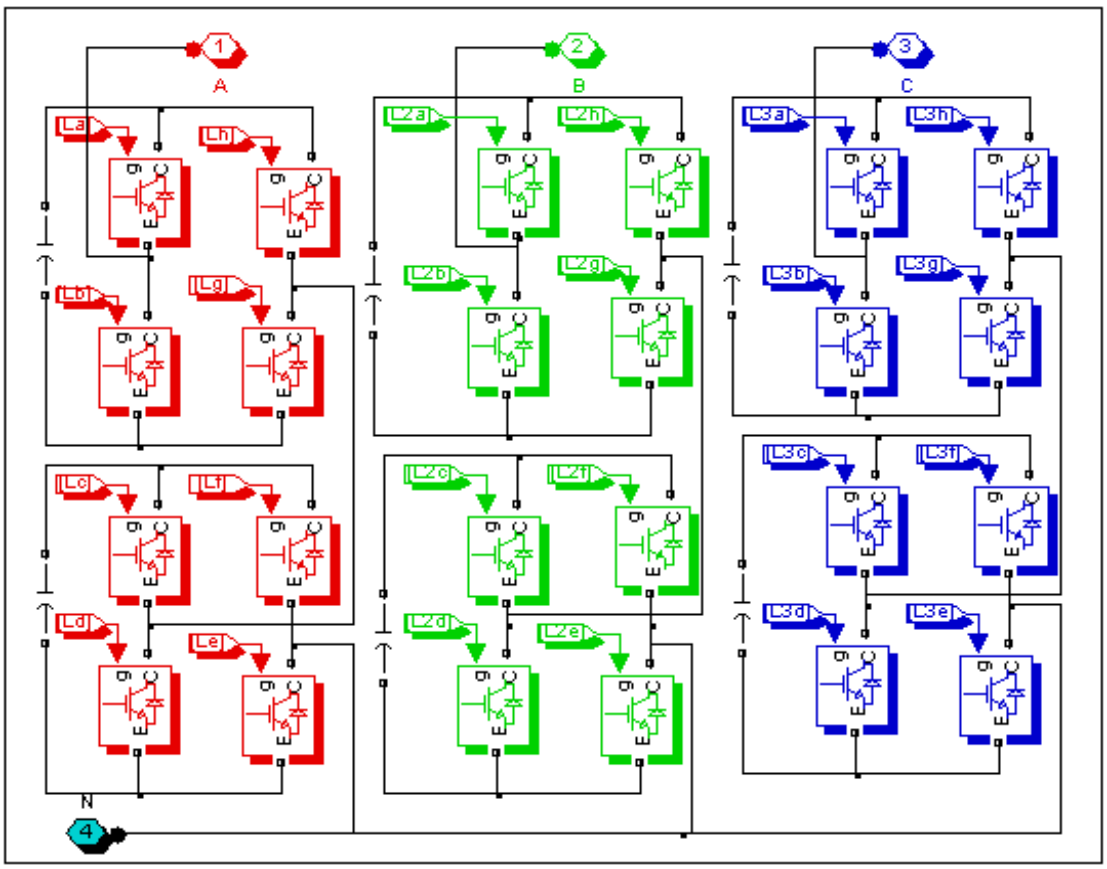


Fig 3.22: Power circuit of the five-level CHB-VSI based four-wire SAPF

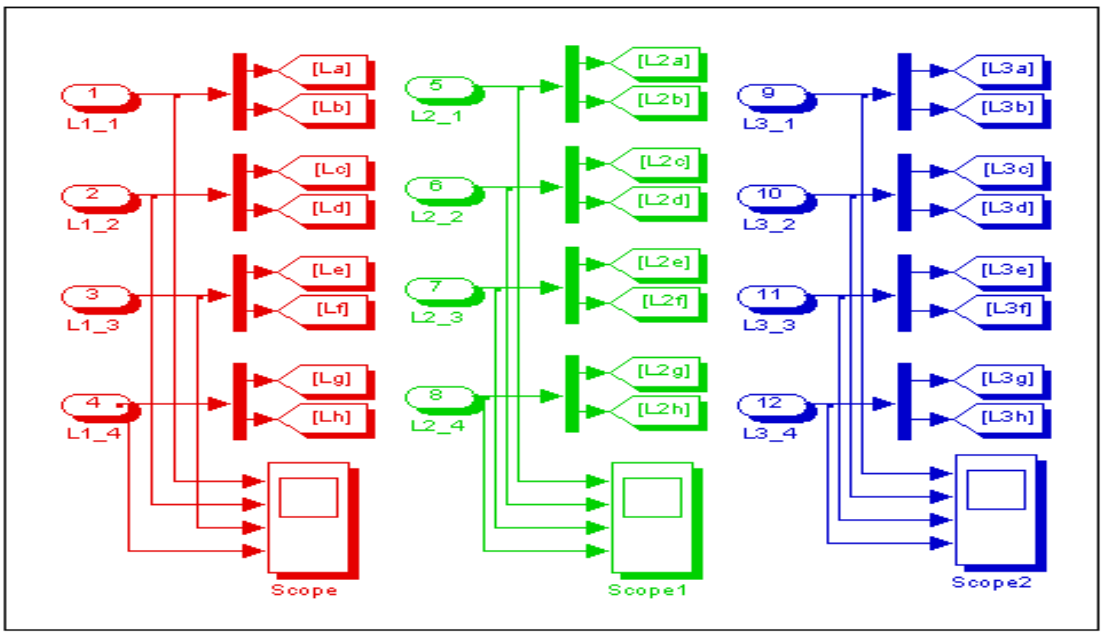


Fig 3.23: Switching pulses of the five-level CHB-VSI based four-wire SAPF

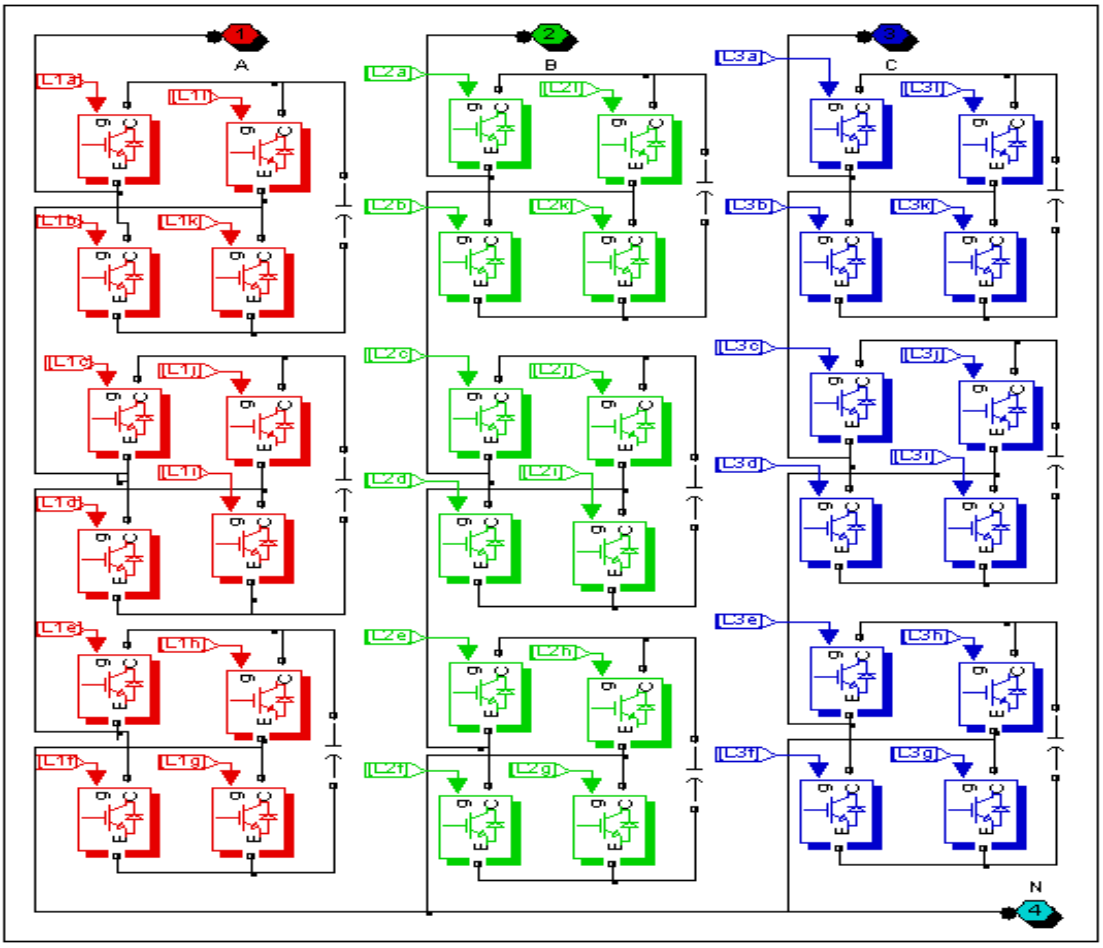


Fig 3.24: Power circuit of the seven-level CHB-VSI based four-wire SAPF

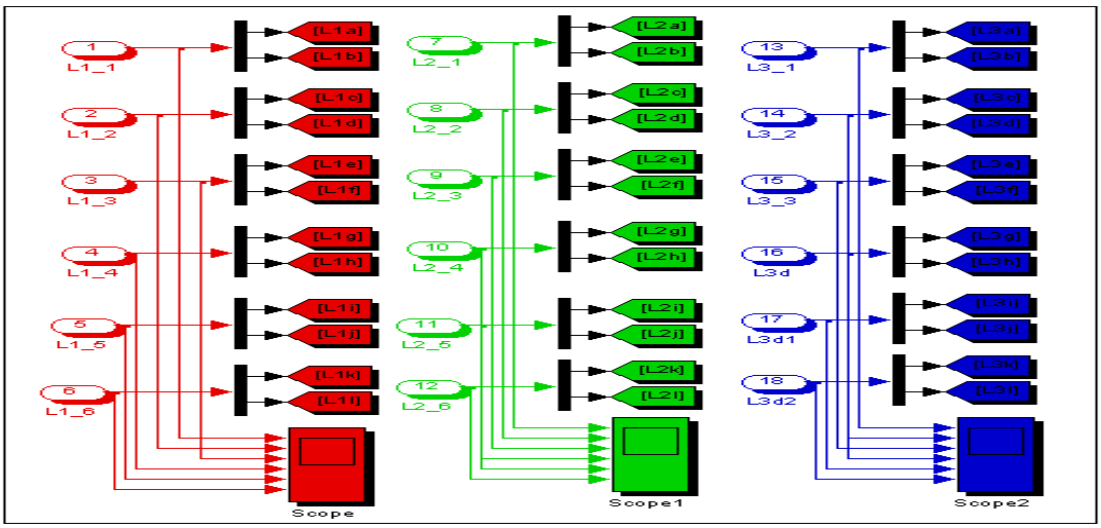


Fig 3.25: Switching pulses of the seven-level CHB-VSI based four-wire SAPF

3.10 Simulation settings

The proposed two-level, five-level and seven-level three-phase four-wire SAPF are simulated using MATLAB/SIMULINK. To achieve the research goals in an efficient manner, simulation parameters were adjusted. By changing the stopping time to 0.3 s instead of 10 s, maximum simulation step size was selected to be $2x\,10^{-6}$, and finally, the solver option was set as shown in Fig 3. 26. The design specifications and the parameters that are used in the proposed simulation system are indicated in Table 3. 1.

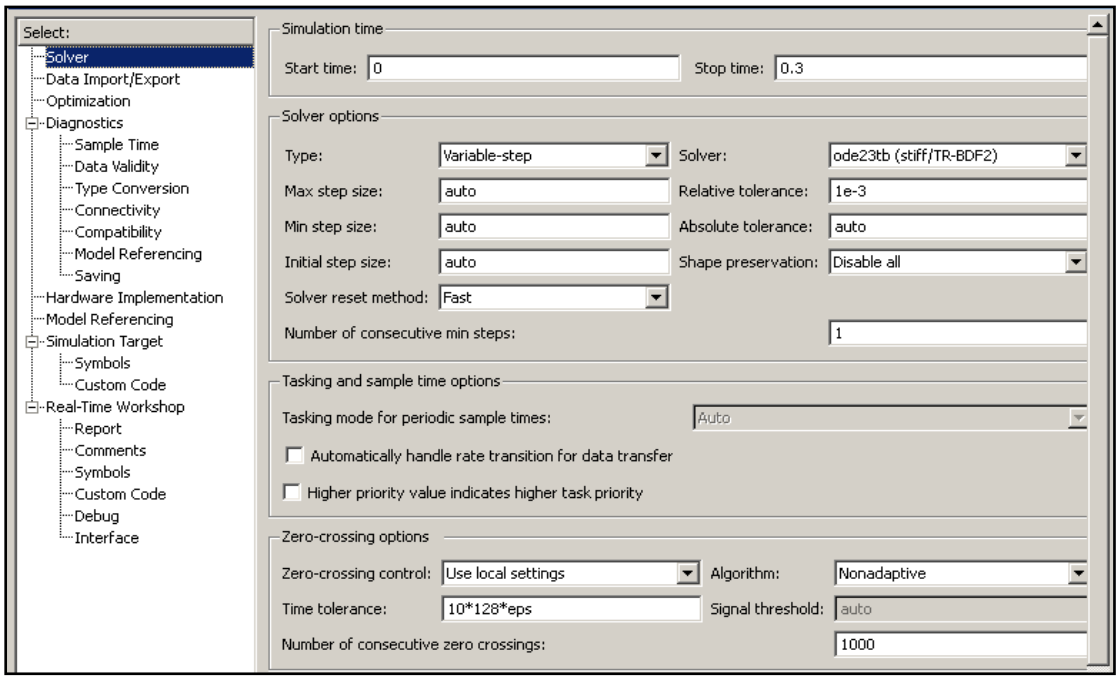


Fig 3.26: The solver option

Table 3.1: Important data for the simulation

No	Parameter	Value
1	3-Φ AC source voltage (RMS)	415 V
2	Source frequency (f)	50 Hz
3	Source resistance (R_s)	2 m Ω
4	Source inductance (L_s)	0.002 mH
5	3-Φ thyristor bridge rectifier AC side inductance (L_{L1})	6 mH
6	3-Φ thyristor bridge rectifier DC side impedance (R_{dc1}, L_{dc1})	12 Ω, 20 mH
7	3-Φ thyristor bridge rectifier firing angle (α)	30^o
8	1-Φ diode bridge rectifier AC side inductance (L_{L2})	3 mH
9	1-Φ diode bridge rectifier DC side resistance, inductance and capacitance (R_{dc2}, L_{dc2} & C_{dc2})	15 Ω, 1 mH, 470 μF
10	Snubber resistance and capacitance of bridge rectifiers	500 Ω, 1 μF
11	Simulation time step	2 μs
12	Snubber resistance of SAPF	0.1 M Ω
13	Snubber capacitance of SAPF	∞
14	Ron of SAPF, thyristor and diode bridge rectifiers	1 m Ω
15	Interface inductance at AC side of SAPF (L_{sh})	6 mH
16	DC storage capacitor of two-level SAPF (C_{dc})	1500 μF
17	AC R-C filter of two-level SAPF	2 Ω, 2 μF
18	Multilevel SAPF capacitor per cell	100 μF
19	Switching frequency of multilevel SAPF	50 Hz
20	Modulation index (m_a)	1.0

3.11 Summary

In this chapter the basic concepts of distribution system suppling mixed non-linear loads and employing SAPF to compensate power qualty disturbances are presented. The mathematical models governering SAPF operation are developed. A detailed explanation on instantaneous power theory for three-phase four-wire system is outlined i.e. estimation of reference currents and DC and AC components of power. Also the three proposed controllers for the estimation of reference currents for SAPF are presented. For the operation of multi-level SAPF, the modulation techniques, namely, PS-SPWM and LS-SPWM applied to the five-level and seven-level VSI are also discussed. An introduction to IPD, APOD and POD modulation techniques which are the three types of LS-SPWM is also reported. Subsequently, an overview of selection of important parameters in the design of the SAPF is discussed. The simulation models with two-level, five-level and seven-level SAPF are developed to achieve the objectives of the proposed study. The simulation settings and important data for the simulation are also presented. Finally, the flow chart of research sequence is presented at the end of this chapter. Simulation results based on the developed models in this chapter are analyzed in the next chapter.

CHAPTER 4

SIMULATION RESULTS AND DISCUSSIONS

4.1 Introduction

Based on the simulation models of the distribution system developed by using MATLAB/SIMULINK and SimPowerSystem Blockset which are introduced in chapter 3, the simulation results are presented in this chapter in order to demonstrate the application of SAPF employing the proposed control techniques. Moreover, the results are presented to support the theoretical analysis and derived equations in chapter 3. The VSI based SAPF is represented by IGBT switches, interface inductor and DC capacitor which are the main elements. Simulation is carried out using MATLAB/SIMULINK version 7.9.0 (R2009b) professional software and personal computer (PC) with the following specifications: (i) System: Microsoft Window XP; Professional; Version 2002; Service Pack 3 and (ii) Manufactured and supported by: DELL Optiplex 330; Intel[R] Core[TM]2 Duo CPU; E7300 @ 2.66GHz; 0.98 GB of RAM; Physical Address Extension.

The three-phase, four-wire distribution system for simulation under this study is a PDN loaded by one three-phase non-linear load, which is a thyristor bridge rectifier, and three single-phase non-linear loads, which are diode bridge rectifiers, as in Figs. 3.19 and 3.21 of Chapter 3. A preliminary study is carried out to understand the effect of non-linear loads on the power system and results are established. In order to compare the performance of SAPF using the proposed controllers based on *p-q* theory *d-q-0* theory and *a-b-c* theory, three case studies are considered and simulated. In case study 1, a two-level four-leg SAPF is used as a compensator to the PDN, while in case studies 2 and 3 a five-level and seven-level CHB-VSI based SAPF, respectively, are connected to the PDN.

The simulation is carried out on the test system by using the proposed controllers for reference currents estimation of the load currents. The hysteresis current control technique is used to generate the PWM gating signals of the two-level four-wire SAPF, while PS-SPWM and LS-SPWM techniques are used in five-level and seven-level SAPF to generate the PWM gating signals. At first, the simulation results by two-level four-wire SAPF using different proposed controllers are presented and analyzed. Simulation results on THD, active and reactive powers, power factor, and neutral conductor current are analyzed and compared to show the performance of SAPF. Next the performance of a five-level four-wire CHB-VSI based SAPF using different proposed controllers and different modulation techniques is studied, in order to have effective and efficient control strategy. Similarly simulation studies are carried out with the seven-level four-wire CHB-VSI based SAPF using different proposed controllers and different modulation techniques. Finally a comparative study is presented analyzing the simulation results.

4.2 Effect of non-linear loads on distribution system

To analyze the effect of mixed single-phase and three-phase non-linear loads on the distribution system when the SAPF is not introduced, the PDN as shown in Fig 3.19 is simulated considering the data of the system and non-linear loads as in Table 3.1. Figs. 4.1 to 4.9, represent the simulation results of voltage, current, THD, and active and reactive powers as well as power factor.

Fig. 4.1 shows the simulation waveform of phase ‘a’ source line-to-neutral voltage, which is observed to be pure sinusoidal with a peak value of 338.85 V. Similar results are obtained for the phases ‘b’ and ‘c’, but with a phase shift of 120^{o}, which are not shown in this thesis.

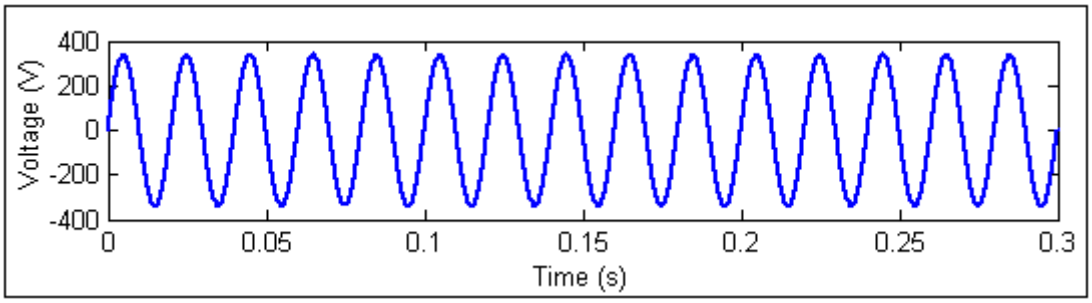


Fig 4.1: Phase ‘a’ source line-to-neutral voltage

It is observed that the voltage THD of the harmonic spectrum as in Fig. 4.2 is equal to 0.02 % which is less than the IEEE-519 standards. Similar result can be shown for phases ‘b’ and ‘c’ also which are not presented in this thesis.

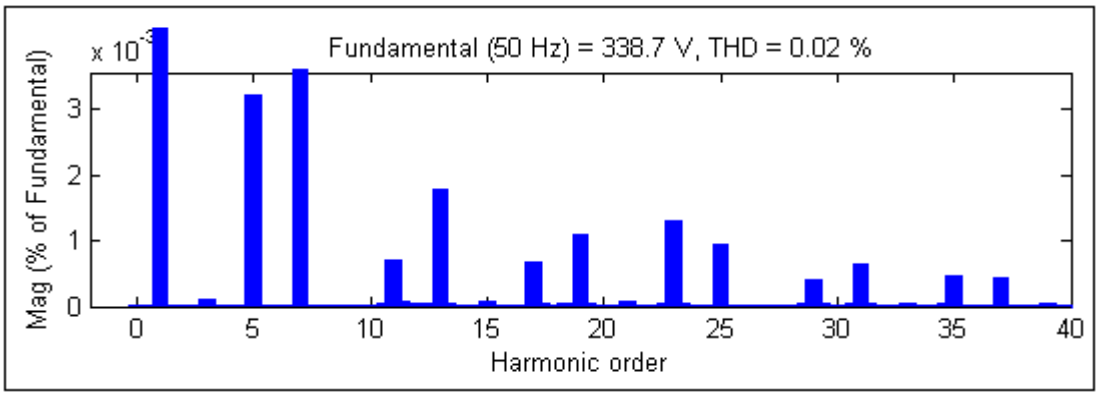


Fig 4.2: Harmonic spectrum and THD for phase ‘a’ source line-to-neutral voltage

However, the distorted source current due to the presence of the non-linear loads is clearly seen as in Fig. 4.3 for phase ‘a’, where the peak current reaches 105.2 A. Similar simulation results for current for the other two phases are obtained with a phase shift of 120^{o}.

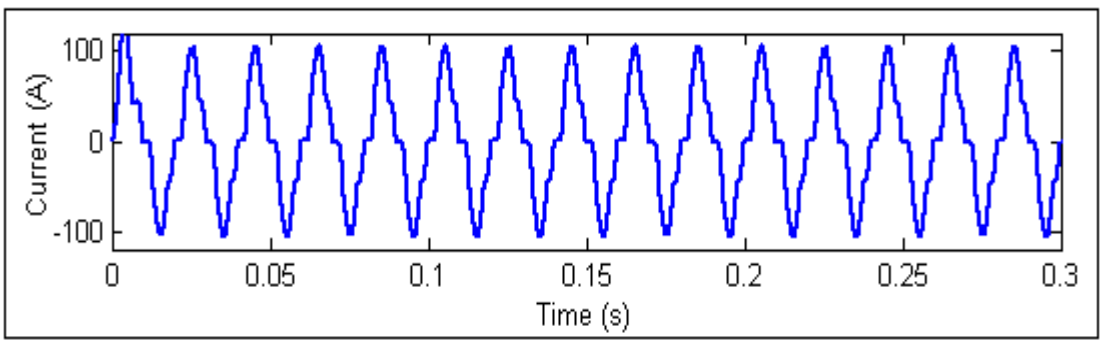


Fig 4.3: Phase ‘a’ source current without SAPF

The phase ‘a’ source current distortion leads to a very high current THD of 27.51 % which is illustrated in Fig. 4.4 by considering the first 40 harmonics. Similar measurements and results are obtained for the other two phases.

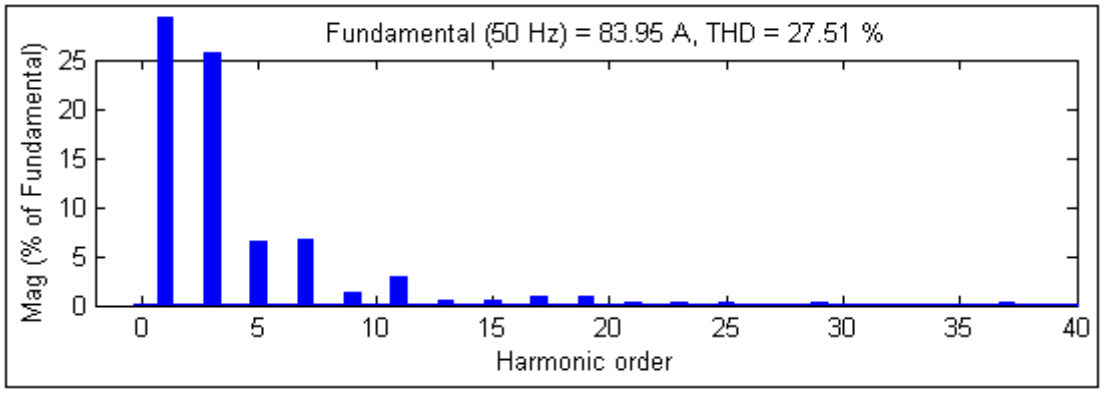


Fig 4.4: Harmonic spectrum and THD for phase ‘a’ source current without SAPF

The source neutral conductor current is also observed to be very high as shown in Fig. 4.5, where the peak current reaches 64.17 A. This causes serious problems to the PDNs if the neutral conductor current is not limited to a very small value.

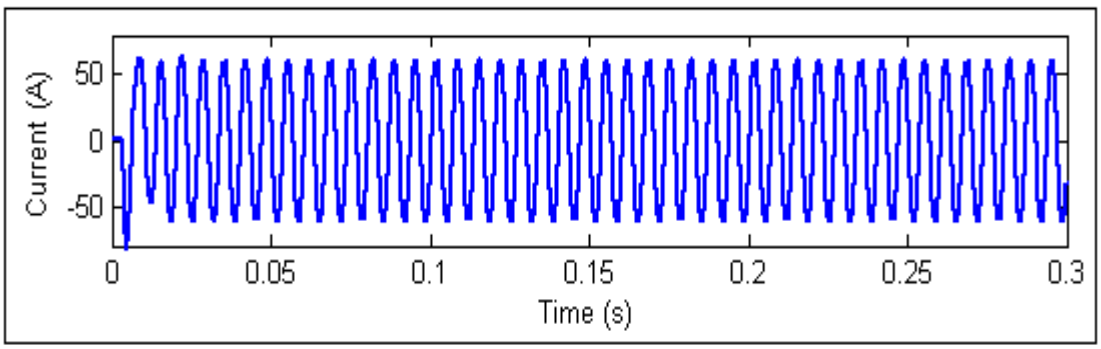


Fig 4.5: Source neutral current without SAPF

To illustrate the nature of source neutral current, the harmonic spectrum and THD of the first 40 harmonics is shown in Fig. 4.6, where the triplen harmonics such as 3rd, 9th, 15th, 21st, 27th, 33rd and 39th are present predominantly. The effect of these harmonics may cause overheating of the neutral conductor and also the equipment such as motors or transformers connected to the power system.

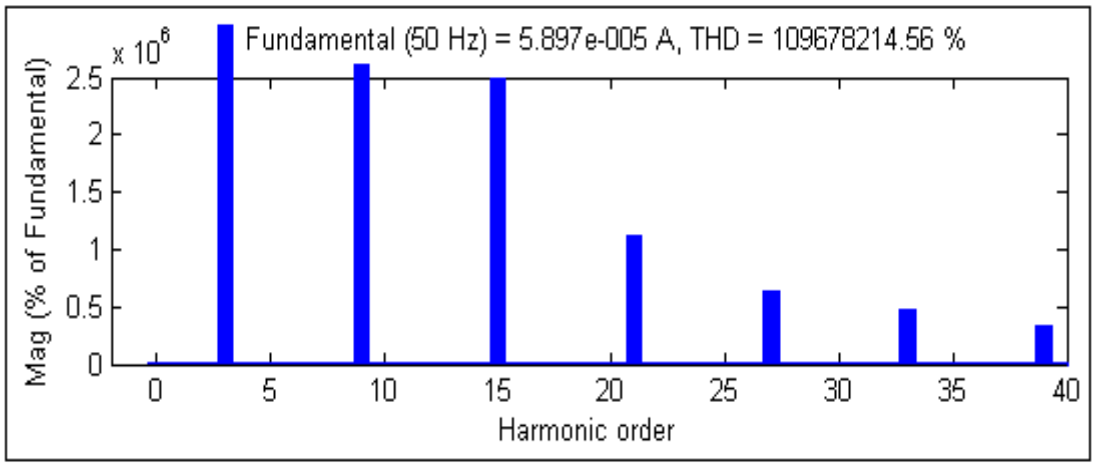


Fig 4.6: Harmonic spectrum and THD of source neutral current without SAPF

Fig. 4.7 shows phase 'a' source voltage and source current, where the current is non-sinusoidal and also is not in-phase with the source voltage. Also it is clear from Fig. 4.7 that the supply side power factor is low, because there is an additional power, known as deforming power, d, which will be included in the calaculation of power factor i.e. $power\ factor = p/s = p/\sqrt{p^2+q^2+d^2}$. Similar results are obtained for the phases 'b' and 'c'.

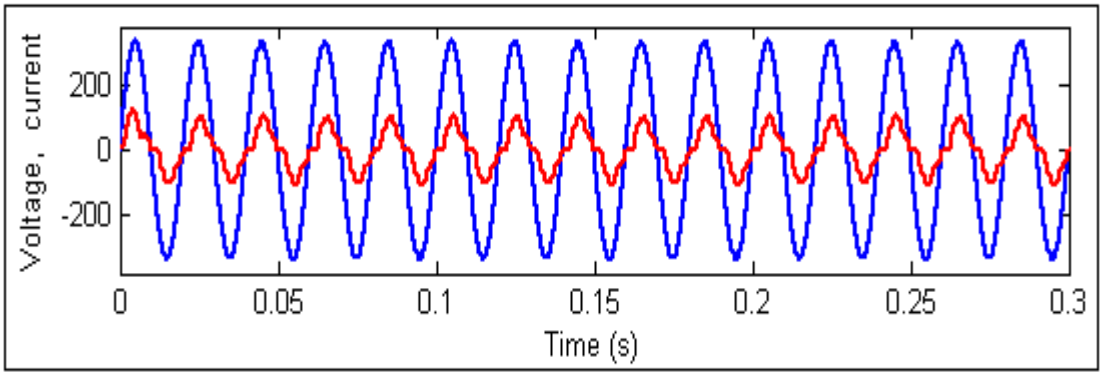


Fig 4.7: Phase 'a' source voltage and source current without SAPF

Fig. 4.8 shows the response of power system for active and reactive power flow when mixed non-linear loads are connected and the reactive power is observed to be as high as 14.59 kvar as the thyristor and diode bridge rectifiers draw large reactive power from the source. Consequently the power factor measured (simulation measurement block) at the source end drops to as low as 0.8056 as shown in Fig. 4.9.

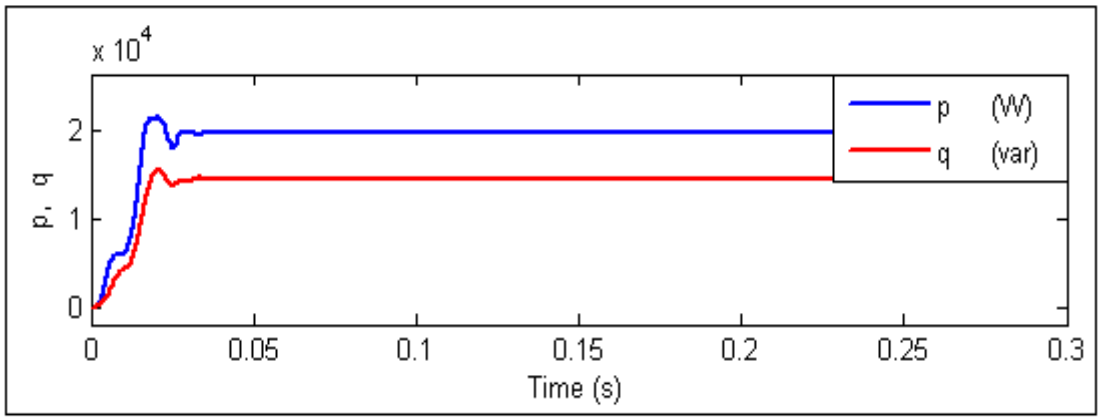


Fig 4.8: Active and reactive powers of the distribution system without SAPF

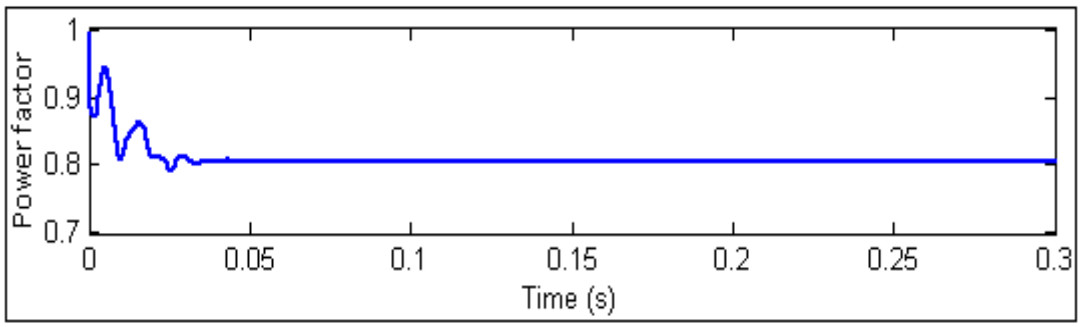


Fig 4.9: Power factor at source end without SAPF

4.3 Case study 1 – Performance of two-level SAPF

The distribution system model as in Fig. 3.19 using a two-level four-wire SAPF compensator with the proposed three control schemes (*p-q* theory, *d-q-0* theory and *a-b-c* theory) based hysteresis current control technique is considered for simulation. Simulation is carried out on the system model by using each proposed control topology independently. For all control schemes, the two-level four-wire SAPF compensates not only current harmonics, but also reactive current components, can be observed by minimizing the THD of current and improving the power factor at source end. To distinguish the simulation results with and without SAPF, a circuit breaker is used to provide connection of SAPF to the system at PCC. The circuit breaker closes at 0.08 s and opens at 0.22 s in all cases of simulation except in the case of simulation for active and reactive power flow, and power factor where the SAPF is connected continuously.

4.3.1 Simulation results with two-level SAPF using *p-q* theory based controller

The proposed controller based on *p-q* theory and hysteresis band controller is presented as in Figs. 3.4 and 3.5 of Chapter 3. The two-level SAPF which has four-leg generates the distorted injecting current in leg 'a' as shown in Fig. 4.10 by using the proposed *p-q* theory based controller in order to compensate the distorted current developed by the non-linear loads which is shown in Fig. 4.3. Similar currents but with 120^{o} phase shift are injected by legs 'b' and 'c' of the SAPF into phases 'b' and 'c' of the distribution system. The injected current reaches a peak value of 47.25 A as shown in Fig. 4.10.

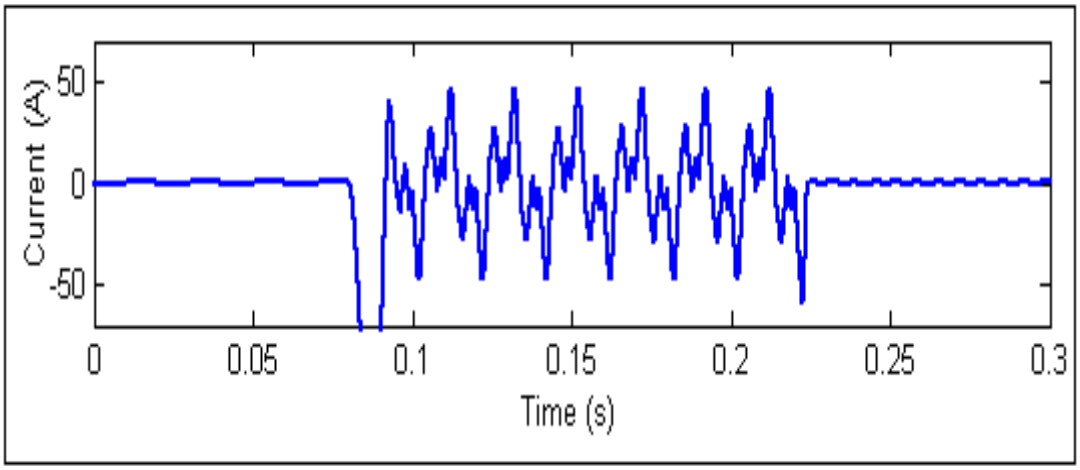


Fig 4.10: Current injected by two-level SAPF using *p-q* theory based controller

Fig. 4.11 shows phase 'a' source current with and without SAPF. It is found that the two-level four-wire SAPF using the proposed *p-q* theory based hysteresis current controller is able to compensate the source current when it is connected during the interval 0.08 s to 0.22 s. The resultant sinusoidal source current between 0.08 s and 0.22 s as in Fig. 4.11 reaches a peak value of 83.72 A which is less than the uncompensated peak current of 105.2 A. Similar simulation result and measured value is obtained for the phases 'b' and 'c'.

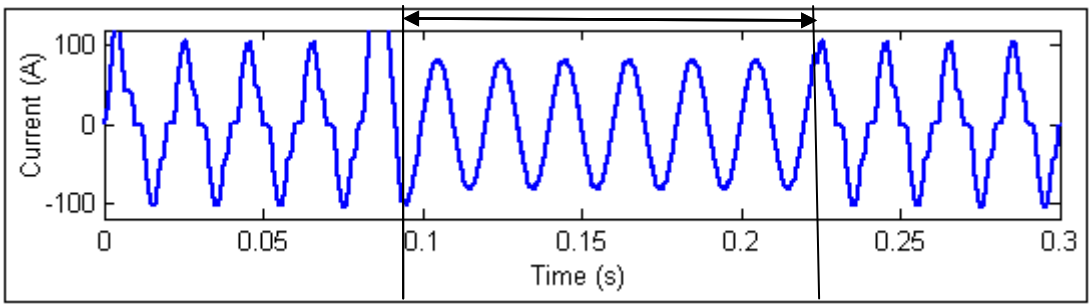
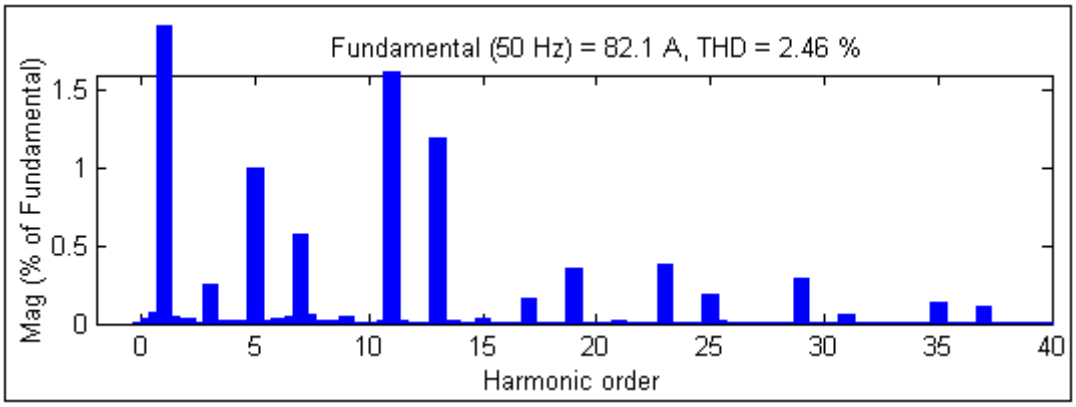
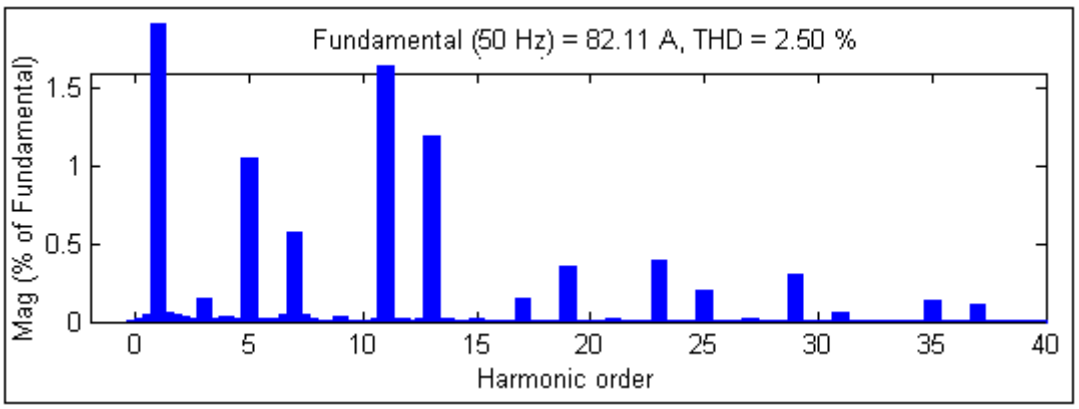


Fig 4.11: Source current with two-level SAPF using *p-q* theory based controller

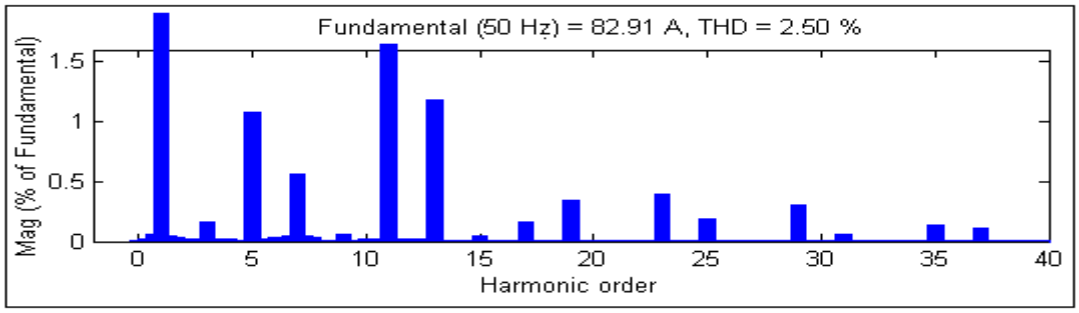
Figs. 4.12 (a) to (c) shows the harmonic spectrum and THD of source currents of phases 'a', 'b' and 'c', respectively. As observed the source current THD is successfully minimized to around 2.5 % as compared to the result before compensation which is 27.51 %. The THDs for the first 40 harmonics calculated for all phase currents is demonstrated to be less than the prescribed value by IEEE-519 Standards.



(a) Phase 'a' source current



(b) Phase 'b' source current



(c) Phase 'c' source current

Fig 4.12: (a) to (c) Harmonic spectrum and THD of source currents with two-level SAPF using *p-q* theory based controller

Fig. 4.13 shows the compensating injected current into the neutral conductor by two-level four-wire SAPF using the proposed *p-q* theory based hysteresis current controller in order to minimize the source neutral current to zero between the interval 0.08 s and 0.22 s.

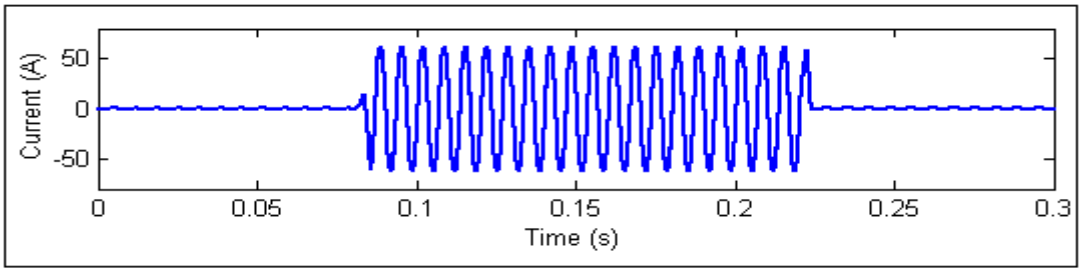


Fig 4.13: Current injected into the neutral conductor by two-level SAPF using *p-q* theory based controller

It is found that the two-level four-wire SAPF using the proposed *p-q* theory based hysteresis current controller is able to minimize the source neutral current to nearly zero when it is connected during the interval 0.08 s to 0.22 s as shown in Fig. 4.14.

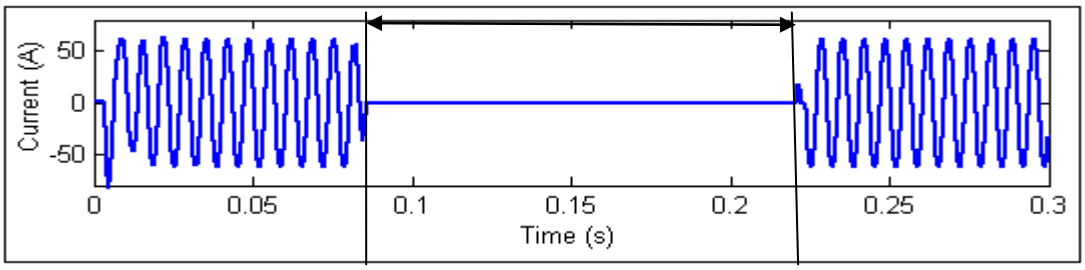


Fig 4.14: Simulated source neutral current with two-level SAPF using *p-q* theory based controller

Fig. 4.15 shows phase 'a' source voltage and source current, where the current is non-sinusoidal except during the interval between 0.08 s and 0.22 s when the SAPF has come into operation. During the interval between 0.08 s and 0.22 s the source current is sinusoidal and is in-phase with the source voltage. Thus, it can be concluded that the developed two-level four-wire SAPF using the proposed *p-q* theory based hysteresis current control has successfully compensated the harmonic load currents and improved the supply power factor to nearly unity. Similar results are obtained for the phases 'b' and 'c' also.

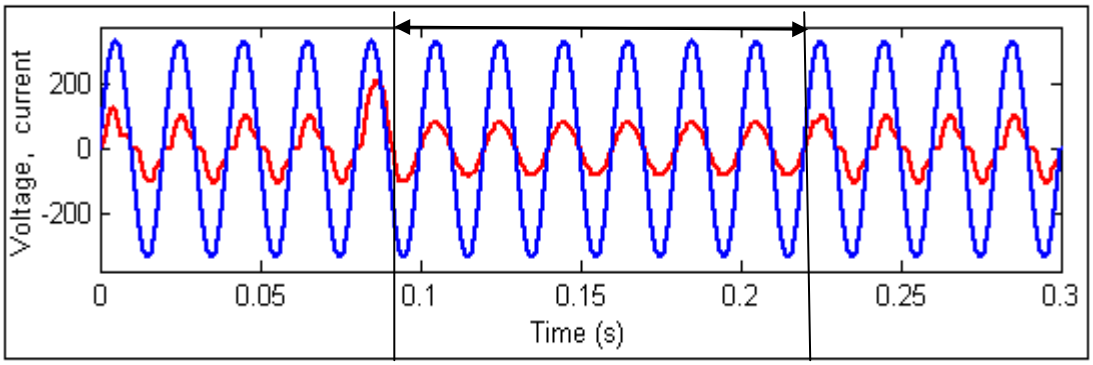


Fig 4.15: Source voltage and source current with two-level SAPF using *p-q* theory based controller

The dynamic response of the DC side voltage of a two-level SAPF using the proposed *p-q* theory based hysteresis current control is shown in Fig. 4.16

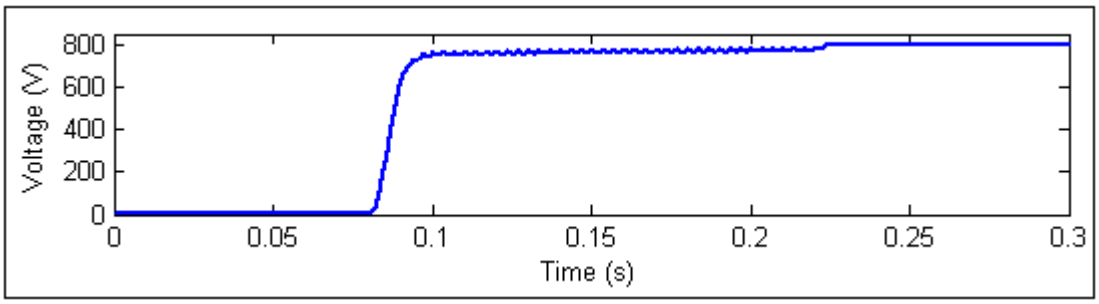


Fig 4.16: DC-link voltage of two-level SAPF using *p-q* theory based controller

Fig. 4.17 shows the active and reactive powers after compensation by a two-level four-wire SAPF using the proposed *p-q* theory based hysteresis current control. The reactive power before compensation which is equal to 14.59 kvar is successfully

compensated to a very low value. Consequently the power factor at the source end is improved to unity as shown in Fig. 4.18.

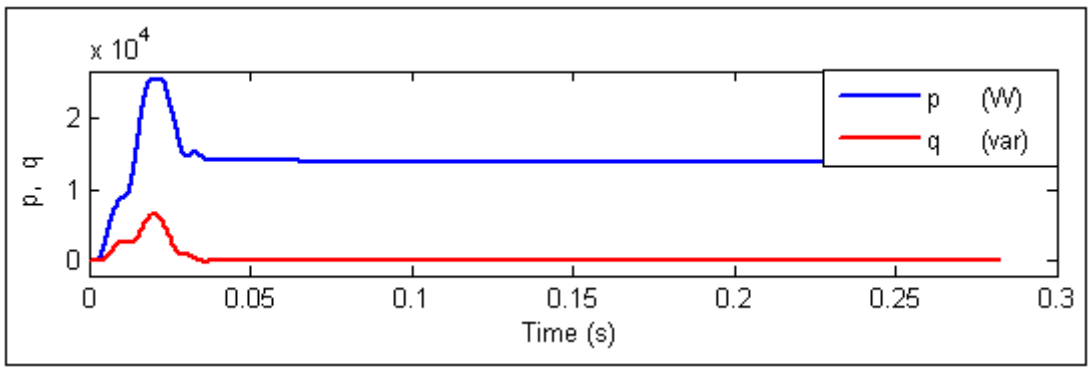


Fig 4.17: Active and reactive powers with two-level SAPF using *p-q* theory based controller

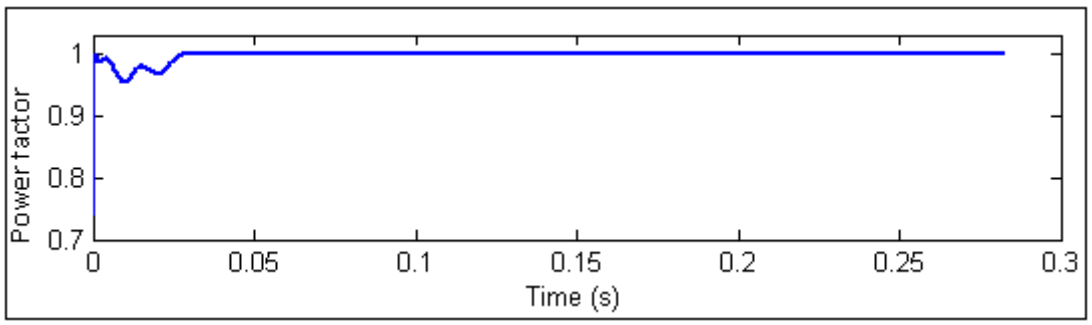


Fig 4.18: Power factor at source end with two-level SAPF using *p-q* theory based controller

4.3.2 Simulation results with two-level SAPF using *d-q-0* theory based controller

The proposed controller based on *d-q-0* theory and hysteresis band controller is presented as in Figs. 3.6 and 3.7 of Chapter 3. The two-level SAPF which has four-leg generates the distorted injecting current in leg 'a' as shown in Fig. 4.19 by using the proposed *d-q-0* theory based controller in order to compensate the distorted current developed by the non-linear loads which is shown in Fig. 4.3. Similar currents but with 120^{o} phase shift are injected by legs 'b' and 'c' of the SAPF into phases 'b' and 'c' of the distribution system. The injected current reaches a peak value of 32.14 A as shown in Fig. 4.19.

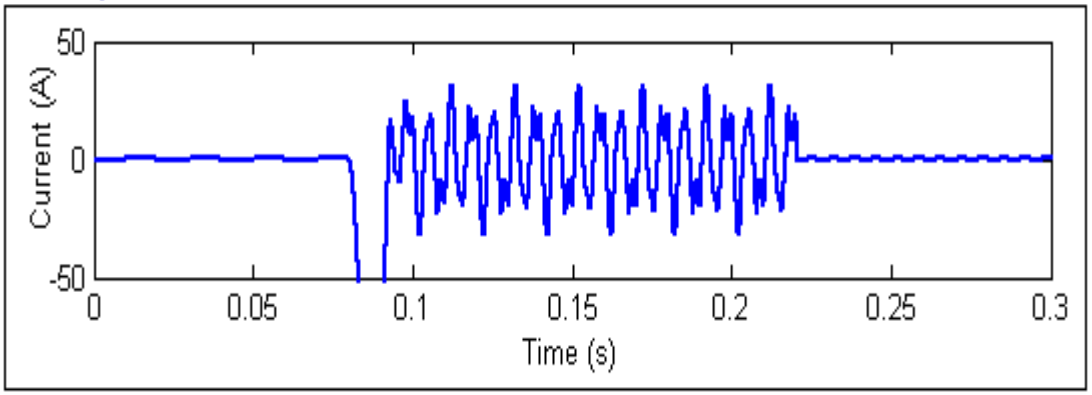


Fig 4.19: Current injected by two-level SAPF using *d-q-0* theory based controller

Fig. 4.20 shows phase 'a' source current with and without SAPF. It is found that the two-level four-wire SAPF using the proposed *d-q-0* theory based hysteresis current controller is able to compensate the source current when it is connected during the interval 0.08 s to 0.22 s. The resultant sinusoidal source current between 0.08 s and 0.22 s reaches a peak value of 87.44 A which is less than the uncompensated peak current of 105.2 A. Similar simulation result and measured value is obtained for phases 'b' and 'c'.

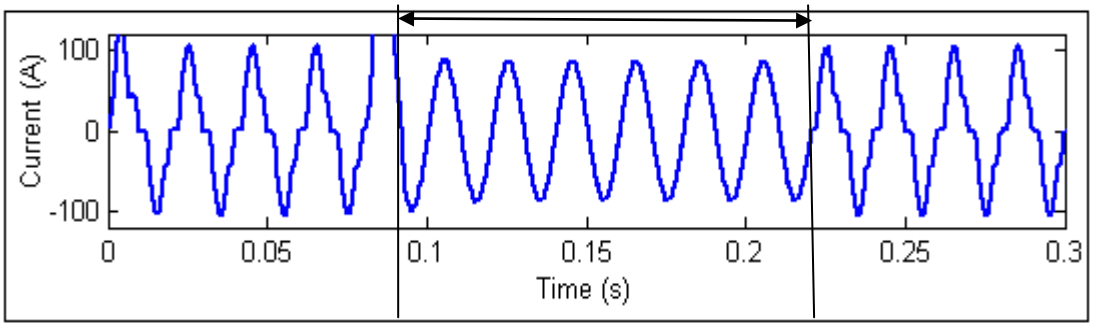
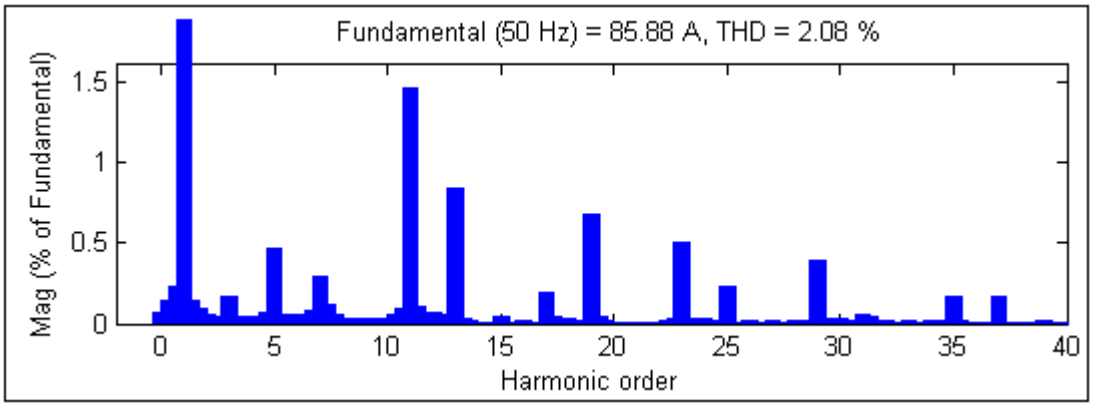
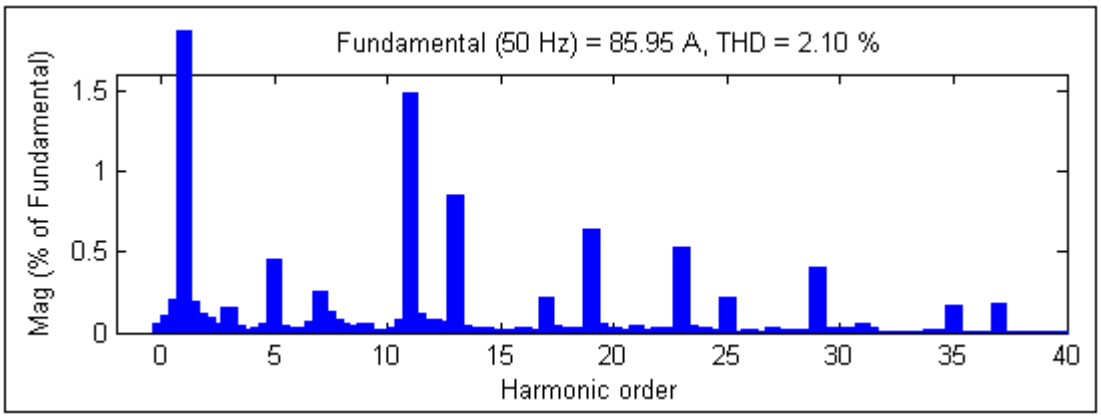


Fig 4.20: Source current with two-level SAPF using *d-q-0* theory based controller

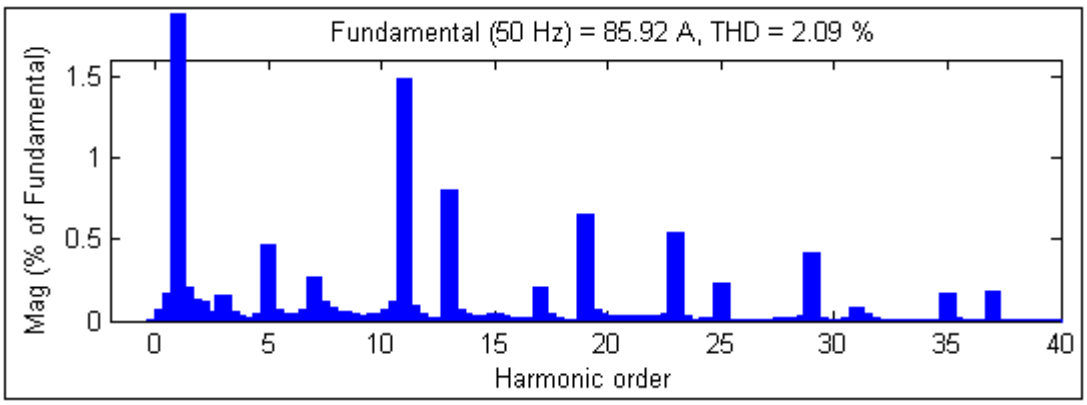
Figs. 4.21 (a) to (c) shows the harmonic spectrum and THD of source currents of phases 'a', 'b' and 'c', respectively. As observed the source current THD is successfully minimized to around 2.09 % as compared to the result before compensation which is 27.51 %. The THDs for the first 40 harmonics calculated for all phase currents is less than the prescribed value by IEEE-519 Standards.



(a) Phase 'a' source current



(b) Phase 'b' source current



(c) Phase 'c' source current

Fig 4.21: (a) to (c) Harmonic spectrum and THD of source currents with two-level SAPF using *d-q-0* theory based controller

Fig. 4.22 shows the compensating injected current into the neutral conductor by two-level four-wire SAPF using the proposed *d-q-0* theory based hysteresis current

controller in order to minimize the source neutral current to zero between the interval 0.08 s and 0.22 s.

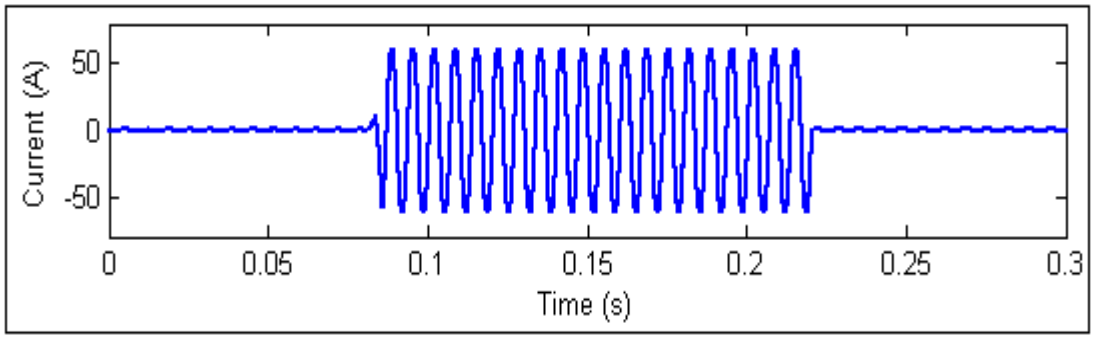


Fig 4.22: Current injected into the neutral conductor by two-level SAPF using *d-q-0* theory based controller

It is found that the two-level four-wire SAPF using the proposed *d-q-0* theory based hysteresis current controller is able to minimize the source neutral current to nearly zero when it is connected during the interval 0.08 s to 0.22 s as shown in Fig. 4.23.

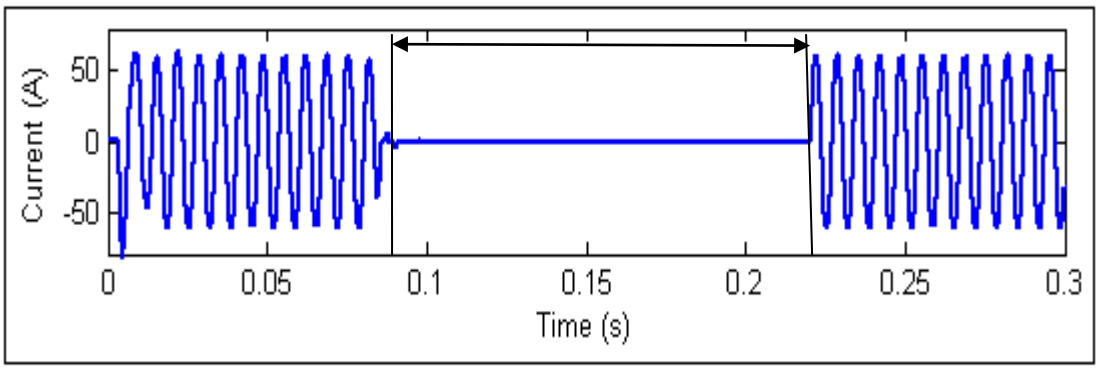


Fig 4.23: Simulated source neutral current with two-level SAPF using *d-q-0* theory based controller

Fig. 4.24 shows phase 'a' source voltage and source current, where the current is non-sinusoidal except during the interval between 0.08 s and 0.22 s when the SAPF has come into operation. During the interval between 0.08 s and 0.22 s the source current is sinusoidal and is in-phase with the source voltage as measured by the simulation block. Thus, it can be concluded that the developed two-level

four-wire SAPF using the proposed *d-q-0* theory based hysteresis current control has successfully compensated the harmonic load currents and improved the supply power factor to nearly unity. Similar results are obtained for the phases 'b' and 'c' also.

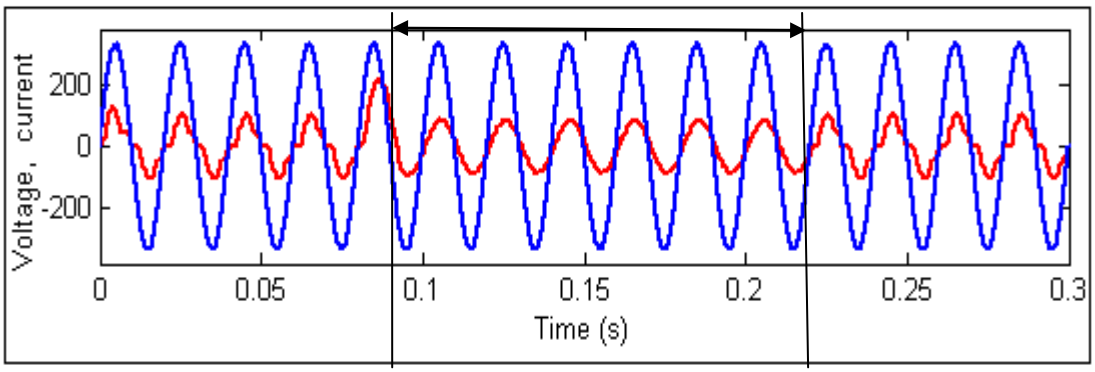


Fig 4.24: Source voltage and source current with two-level SAPF using *d-q-0* theory based controller

The dynamic response of the DC side voltage of a two-level four-wire SAPF using the proposed *d-q-0* theory based hysteresis current control is shown in Fig. 4.25.

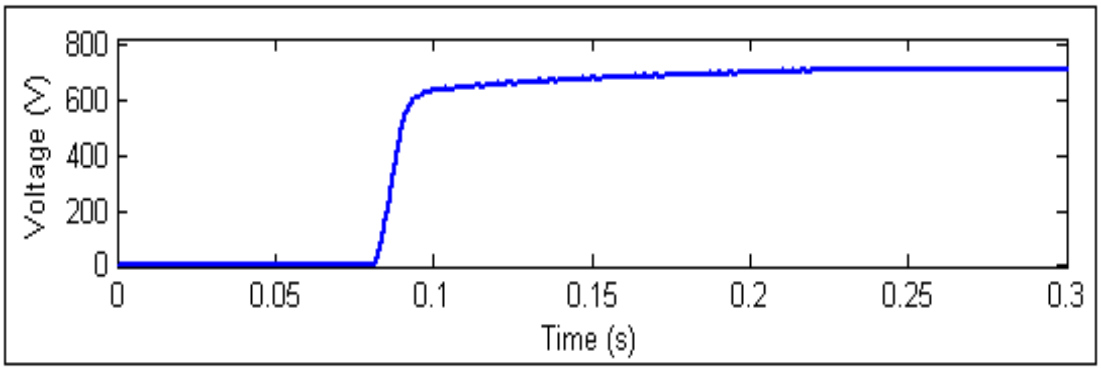


Fig 4.25: DC-link voltage of two-level SAPF using *d-q-0* theory based controller

Fig. 4.26 shows the active and reactive powers after compensation by a two-level four-wire SAPF using the proposed *d-q-0* theory based hysteresis current control. The reactive power before compensation which is equal 14.59 kvar is successfully compensated to a very low value. Consequently the power factor at the source end is improved to 0.985 as shown in Fig. 4.27.

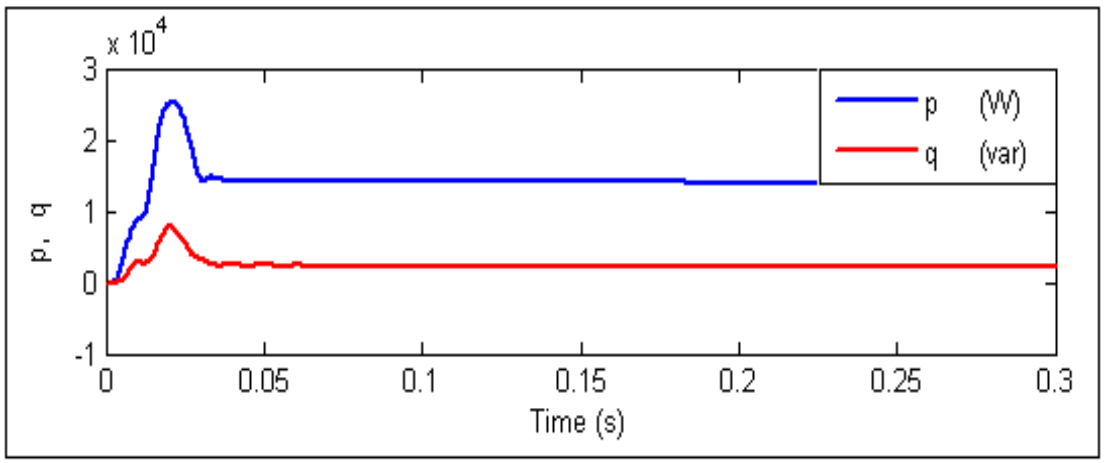


Fig 4.26: Active and reactive powers with two-level SAPF using *d-q-0* theory based controller

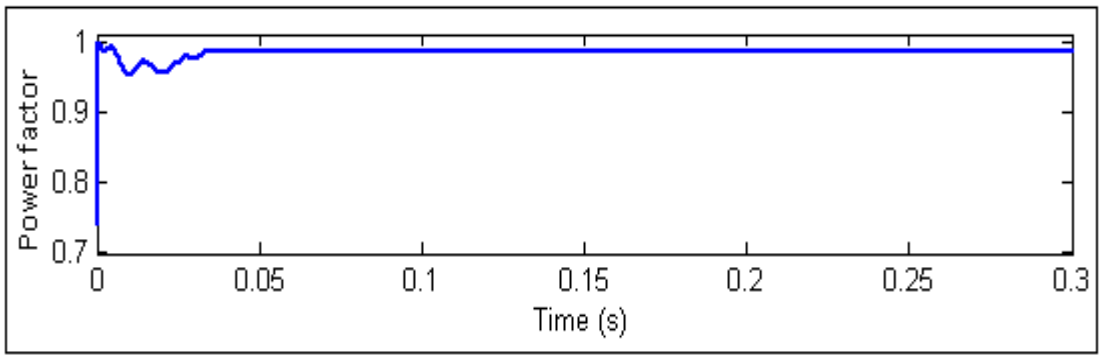


Fig 4.27: Power factor at source end with two-level SAPF using *d-q-0* theory based controller

4.3.3 Simulation results with two-level SAPF using *a-b-c* theory based controller

The proposed controller based on *a-b-c* theory and hysteresis band controller is presented as in Fig. 3.8 of Chapter 3. The two-level SAPF which has four-leg generates the distorted injecting current in leg 'a' as shown in Fig. 4.28 by using the proposed *a-b-c* theory based controller in order to compensate the distorted current developed by the non-linear loads which is shown in Fig. 4.3. Similar currents but with 120^{o} phase shift are injected by legs 'b' and 'c' of the SAPF into phases 'b' and 'c' of the distribution system. The injected current reaches a peak value of 34.74 A as shown in Fig. 4.28.

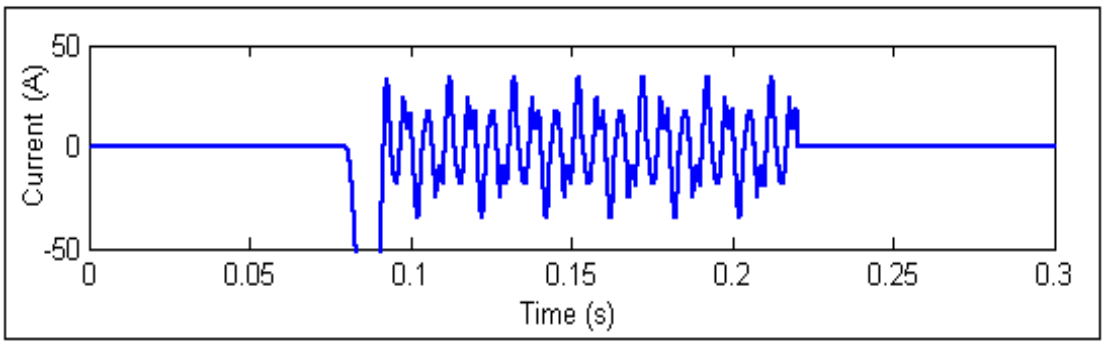


Fig 4.28: Current injected by two-level SAPF using *a-b-c* theory based controller

Fig. 4.29 shows phase 'a' source current with and without SAPF. It is found that the two-level four-wire SAPF using the proposed *a-b-c* theory based hysteresis current controller is able to compensate the source current when it is connected during the interval 0.08 s to 0.22 s. The resultant sinusoidal source current between 0.08 s and 0.22 s reaches a peak value of 87.47 A which is less than the uncompensated peak current of 105.2 A. Similar simulation result and measured value is obtained for the phases 'b' and 'c'.

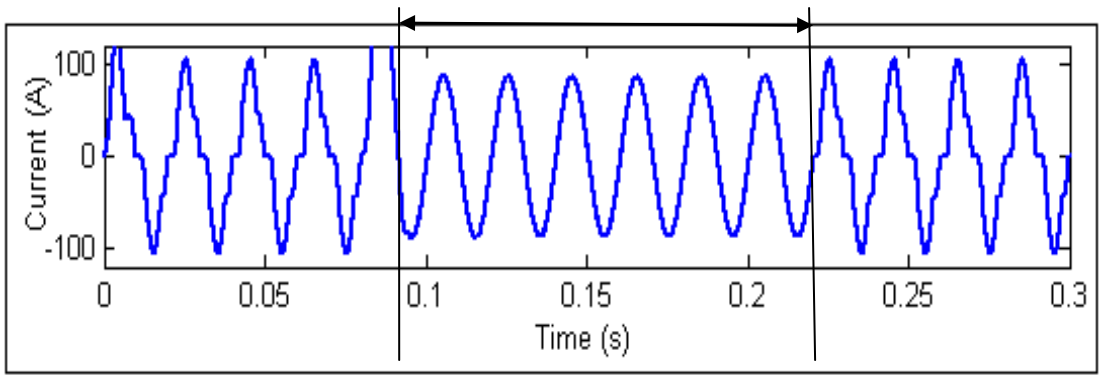
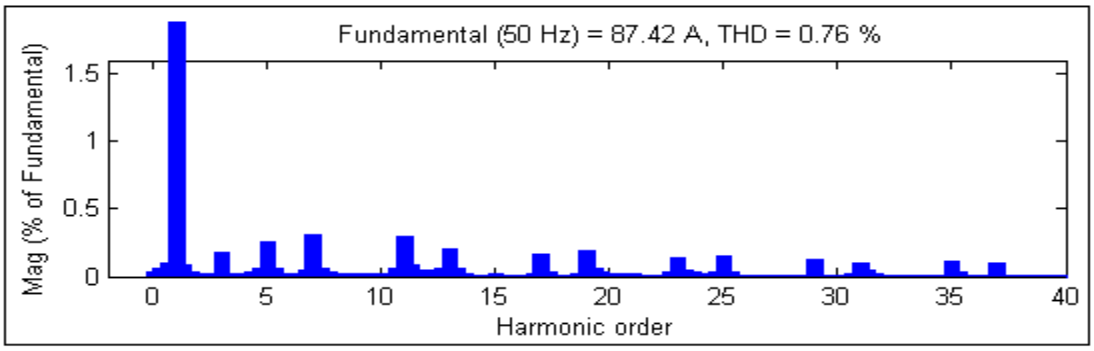
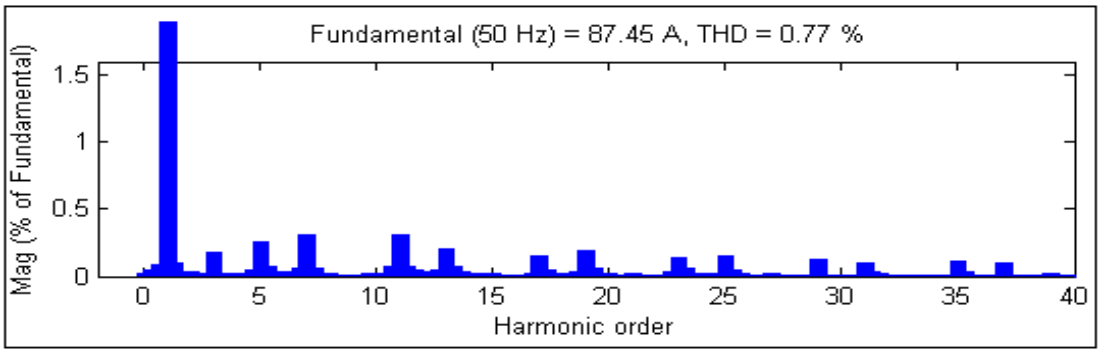


Fig 4.29: Source current with two-level SAPF using *a-b-c* theory based controller

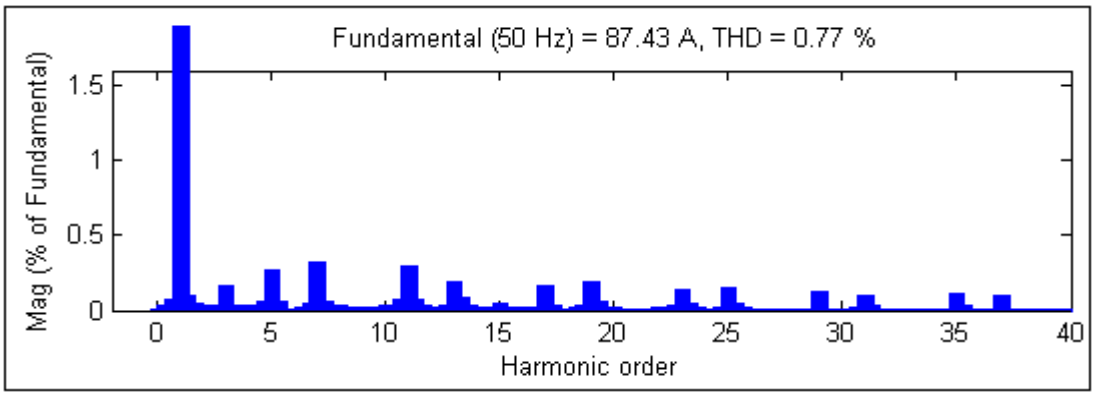
Figs. 4.30 (a) to (c) show the harmonic spectrum and THD of source currents of phases 'a', 'b' and 'c', respectively. As observed the source current THD is successfully minimized to around 0.77 % as compared to the result before compensation which is 27.51 %. The THDs for the first 40 harmonics calculated for all phase currents is demonstrated to be less than the prescribed value by IEEE-519 Standard.



(a) Phase 'a' source current



(b) Phase 'b' source current



(c) Phase 'c' source current

Fig 4.30: (a) to (c) Harmonic spectrum and THD of source currents with two-level SAPF using *a-b-c* theory based controller

Fig. 4.31 shows the compensating injected current into the neutral conductor by two-level four-wire SAPF using the proposed *a-b-c* theory based hysteresis current controller in order to minimize the source neutral current to zero between the interval 0.08 s and 0.22 s.

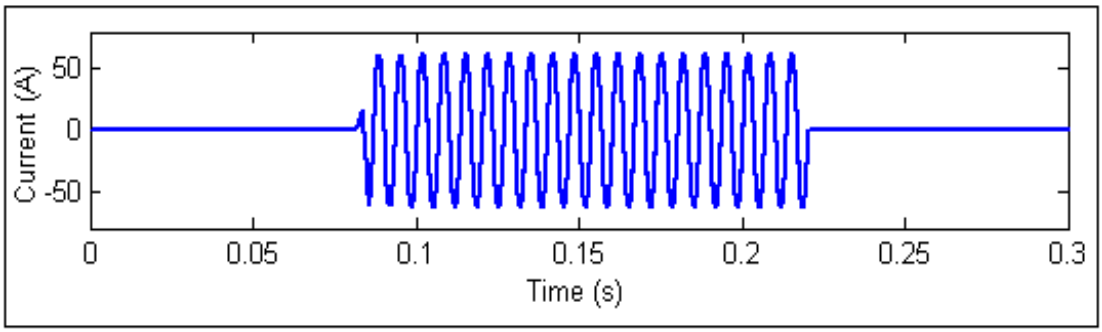


Fig 4.31: Current injected into the neutral conductor by two-level SAPF using *a-b-c* theory based controller

It is found that the two-level four-wire SAPF using the proposed *a-b-c* theory based hysteresis current controller is able to minimize the source neutral current to nearly zero when it is connected during the interval 0.08 s to 0.22 s as shown in Fig. 4.32.

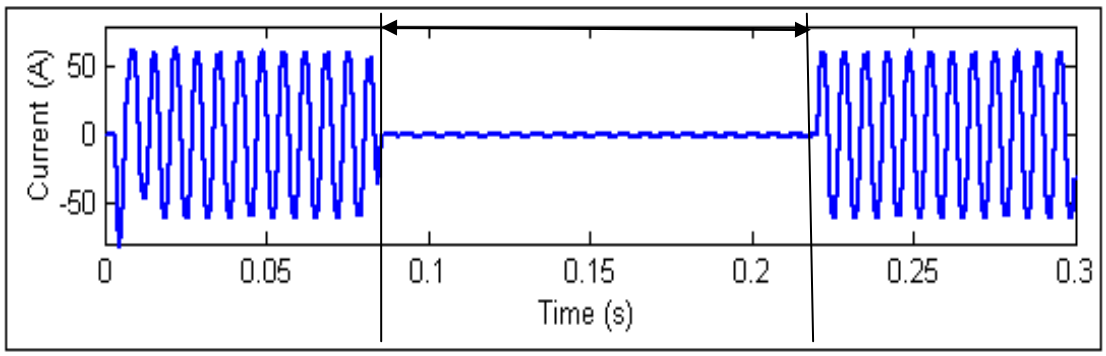


Fig 4.32: Simulated source neutral current with two-level SAPF using *a-b-c* theory based controller

Fig. 4.33 shows phase 'a' source voltage and source current, where the current is non-sinusoidal except during the interval between 0.08 s and 0.22 s when the SAPF has come into operation. During the interval between 0.08 s and 0.22 s the source current is sinusoidal and is in-phase with the source voltage. Thus, it can be concluded that the developed two-level four-wire SAPF using the proposed *a-b-c* theory based hysteresis current control has successfully compensated the harmonic load currents and improved the supply power factor to nearly unity. Similar results are obtained for the phases 'b' and 'c'.

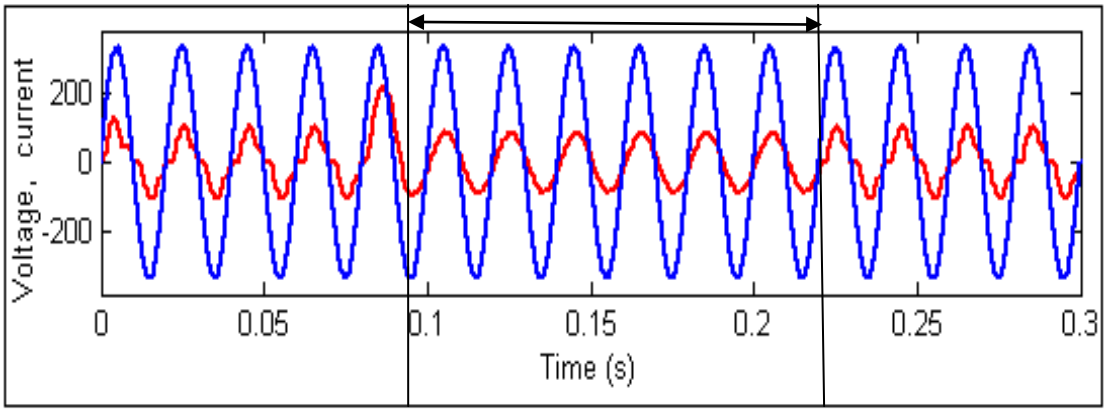


Fig 4.33: Source voltage and source current with two-level SAPF using *a-b-c* theory based controller

The dynamic response of the DC side voltage of a two-level four-wire SAPF using the proposed *a-b-c* theory based hysteresis current control is shown in Fig. 4.34.

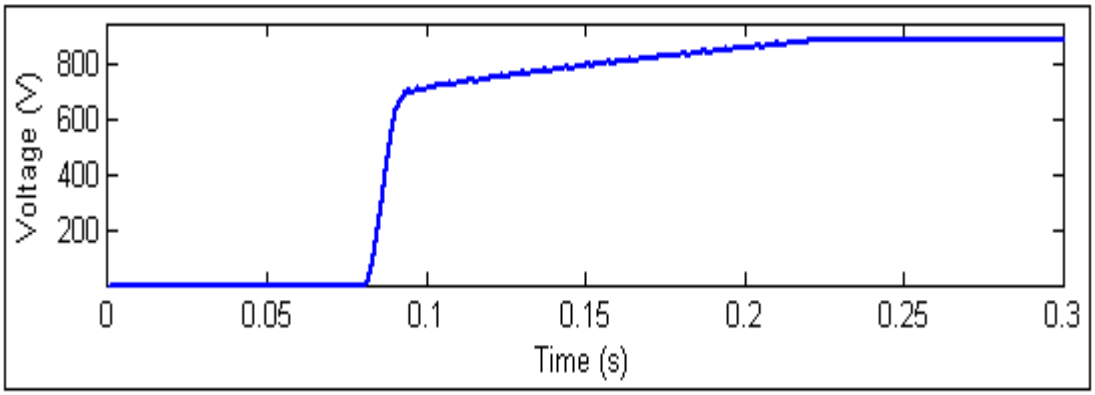


Fig 4.34: DC-link voltage of two-level SAPF using *a-b-c* theory based controller

Fig. 4.35 shows the active and reactive powers after compensation by a two-level four-wire SAPF using the proposed *a-b-c* theory based hysteresis current control. The reactive power before compensation which is equal 14.59 kvar is successfully compensated to a very low value. Consequently the power factor at the source end is improved to 0.987 as shown in Fig. 4.36.

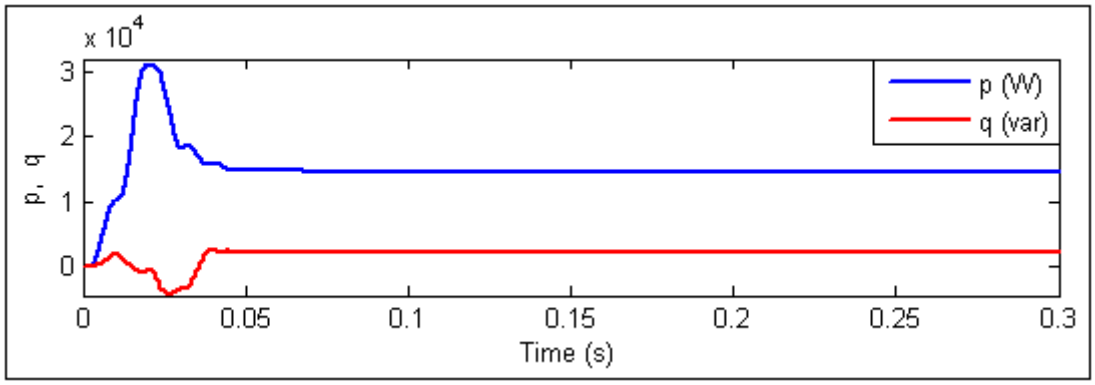


Fig 4.35: Active and reactive powers with two-level SAPF using *a-b-c* theory based controller

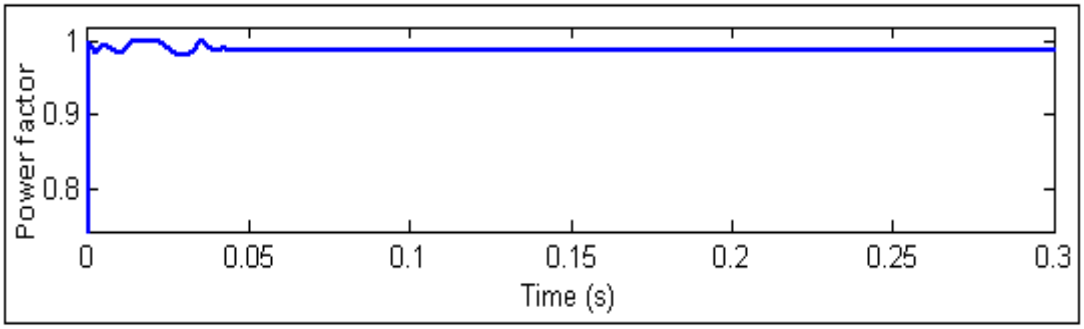


Fig 4.36: Power factor at source end with two-level SAPF using *a-b-c* theory based controller

To compare the performance of two-level four-wire SAPF by the proposed three types of controllers, the THDs of source currents are presented in Table 4.1. It can be observed that in all the three cases the THD is less than the prescribed limit of 5 % as recommended by IEEE-519 standards. However, the THD obtained by the proposed *a-b-c* theory based controller is far less than by the other two controllers as illustrated in Table 4.1.

Table 4.1: Source currents THD with two-level four-wire SAPF

Controller	THD *p-q* theory	THD *d-q-0* theory	THD *a-b-c* theory
Phase 'a'	2.46	2.08	0.76
Phase 'b'	2.50	2.10	0.77
Phase 'c'	2.50	2.09	0.77

Simulation results of compensated source neutral currents by two-level four-wire SAPF using the three types of proposed controllers are given in Table. 4.2. As observed these currents are far less than 64.17 A before compensation. However the controller based on *d-q-0* theory reduced the source neutral conductor current to a very small value of 0.49 A as shown in Table. 4.2.

Table 4.2: Source neutral current with two-level four-wire SAPF

Controller type	*p-q* theory	*d-q-0* theory	*a-b-c* theory
Peak neutral current	0.88 A	0.49 A	1.37 A

Simulation results for power factor at the source end with two-level four-wire SAPF using the three different proposed controllers is given in Table 4.3. It can be observed that the power factor is greatly improved as compared to the value before compensation which is 0.8056. However the controller based on *p-q* theory improved the source end power factor to unity as shown in Table 4.3 which makes the source current sinusoidal.

Table 4.3: Power factor at source end with two-level four-wire SAPF

Controller type	*p-q* theory	*d-q-0* theory	*a-b-c* theory
Supply Power factor	1.0	0.985	0.987

To observe the effect of switching in operation of the two-level SAPF, the recorded peak transient current at source is presented as in Table 4.4. It is observed that *d-q-0* theory based controller gives less peak current as compared to the other two controllers as shown in Table 4.4.

Table 4.4: Transient current with two-level four-wire SAPF

Controller type	*p-q* theory	*d-q-0* theory	*a-b-c* theory
Peak transient current	212.9 A	209.9 A	215.8 A

4.4 Case study 2 – Performance of five-level SAPF

The distribution system model as in Fig. 3.21 of Chapter 3 using a five-level four-wire SAPF compensator with the proposed three control schemes (*p-q* theory, *d-q-0* theory and *a-b-c* theory) based on PS-SPWM and LS-SPWM techniques is considered for simulation. Simulation is carried out on the system model by using each proposed control topology independently. For all control schemes, the five-level four-wire SAPF compensates not only current harmonics, but also reactive current components. To distinguish the simulation results with and without SAPF, a circuit breaker is used to provide connection of SAPF to the system at PCC. The circuit breaker closes at 0.08 s and opens at 0.22 s in all cases of simulation except in the case of simulation for active and reactive power flow, and power factor where the SAPF is connected continuously.

4.4.1 Simulation results with five-level four-wire SAPF using PS-SPWM

In the PS-SPWM technique the PWM signals are generated in order to control the five-level CHB-VSI based SAPF as shown in Appendix D. The sinusoidal modulation signal (reference current) is compared with four triangular carrier signals which are phase shifted by 360/4 degrees. By comparing these carrier signals and the reference currents, the PWM signals for a five-level CHB-VSI are developed.

4.4.1.1 Simulation results with five-level SAPF using proposed p-q theory based controller and PS-SPWM

The proposed controller based on *p-q* theory and PS-SPWM technique is presented as in Figs. 3.4 and 3.11 of Chapter 3. The five-level SAPF which has four wires generates the distorted injecting current in leg 'a' as shown in Fig. 4.37 by using the proposed *p-q* theory based controller and PS-SPWM technique in order to compensate the distorted current shown in Fig. 4.3. Similar currents but with 120^{o} phase shift are injected by legs 'b' and 'c' of the SAPF into phases 'b' and 'c' of the distribution system. The injecting current reaches a peak value of 49 A as shown in Fig. 4.37.

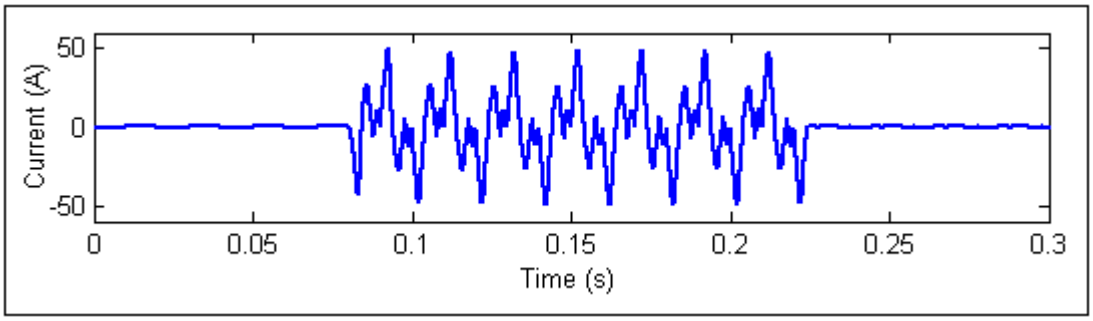


Fig 4.37: Current injected by five-level SAPF using *p-q* theory based controller and PS-SPWM

Fig. 4.38 shows phase 'a' source current with and without SAPF. It is found that the five-level four-wire SAPF using the proposed *p-q* theory based controller and PS-SPWM technique is able to compensate the source current when it is connected during the interval 0.08 s to 0.22 s. The resultant sinusoidal source current between 0.08 s and 0.22 s reaches a peak value of 85.07 A which is less than the uncompensated peak current of 105.2 A. Similar simulation result and measured value are obtained for the phases 'b' and 'c'.

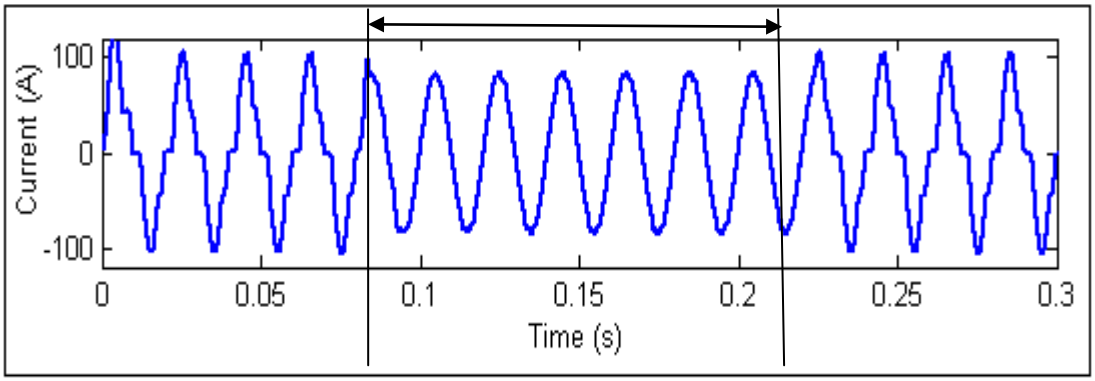
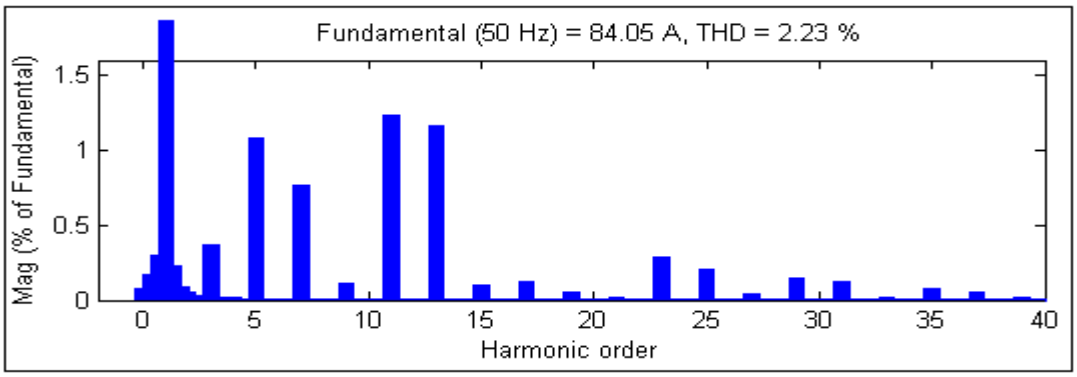
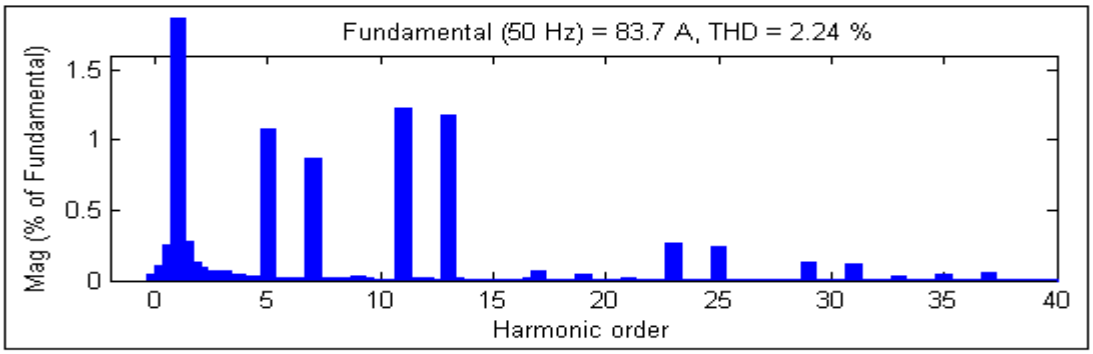


Fig 4.38: Source current with five-level SAPF using *p-q* theory based controller and PS-SPWM

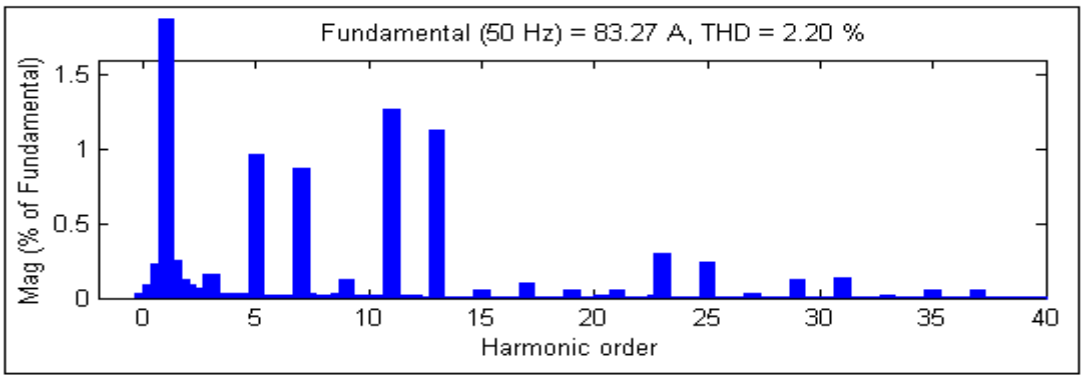
Figs. 4.39 (a) to (c) show the harmonic spectrum and THD of source currents of phases 'a', 'b' and 'c', respectively. As observed the source current THD is successfully minimized to around 2.23 % as compared to the result before compensation which is 27.51 %. The THDs for the first 40 harmonics calculated for all phase currents is demonstrated to be less than the prescribed value by IEEE-519 Standards.



(a) Phase 'a' source current



(b) Phase 'b' source current



(c) Phase 'c' source current

Fig 4.39: (a) to (c) Harmonic spectrum and THD of source currents with five-level SAPF using *p-q* theory based controller and PS-SPWM

Fig. 4.40 shows the compensating injected current into the neutral conductor by five-level four-wire SAPF using the proposed *p-q* theory based controller and PS-SPWM technique in order to minimize the source neutral current to zero between the interval 0.08 s and 0.22 s.

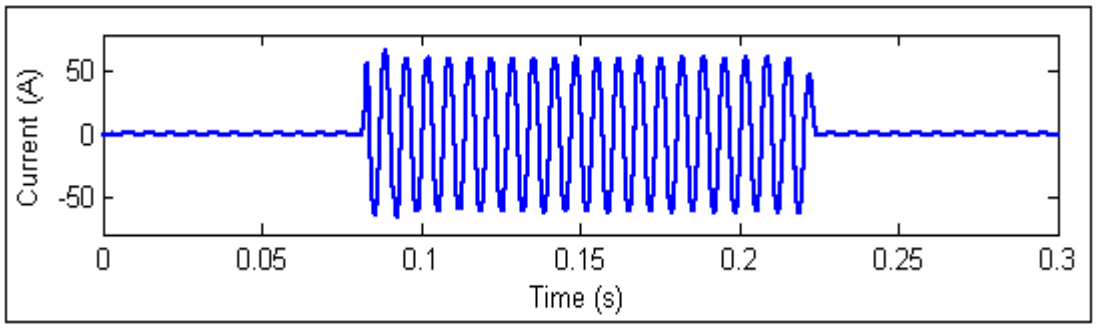


Fig 4.40: Current injected into the neutral conductor by five-level SAPF using *p-q* theory based controller and PS-SPWM

It is found that the five-level four-wire SAPF using the proposed *p-q* theory based controller and PS-SPWM technique is able to minimize the source neutral current to nearly zero when it is connected during the interval 0.08 s to 0.22 s as shown in Fig. 4.41.

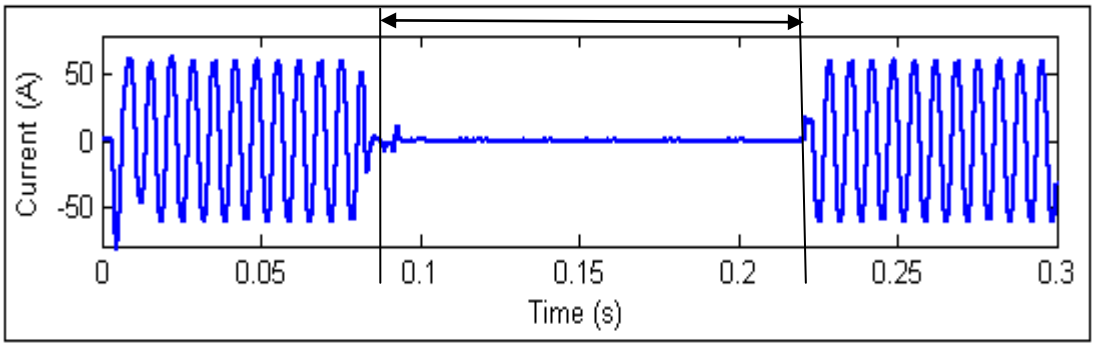


Fig 4.41: Simulated source neutral current with five-level SAPF using *p-q* theory based controller and PS-SPWM

Fig. 4.42 shows phase 'a' source voltage and source current, where the current is non-sinusoidal except during the interval between 0.08 s and 0.22 s when the SAPF has come into operation. During the interval between 0.08 s and 0.22 s the source current is sinusoidal and is in-phase with the source voltage. Thus, it can be concluded that the developed five-level four-wire SAPF using the proposed *p-q* theory based controller and PS-SPWM technique has successfully compensated the harmonic load currents and improved the supply power factor to nearly unity. Similar results are obtained for the phases 'b' and 'c' also.

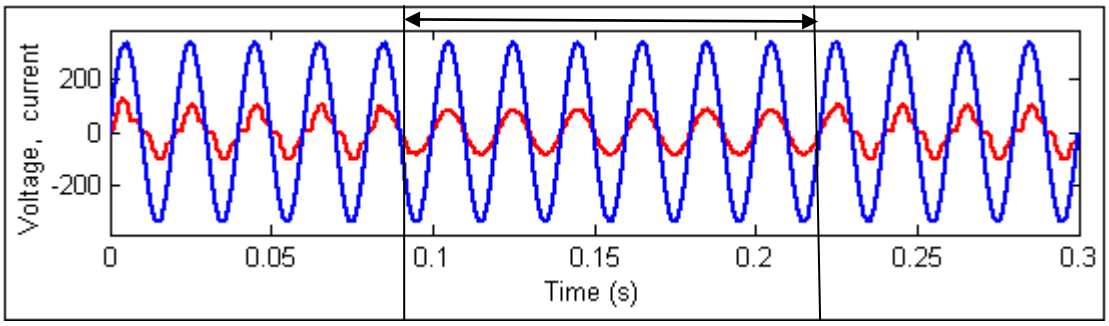


Fig 4.42: Source voltage and source current with five-level SAPF using *p-q* theory based controller and PS-SPWM

Fig. 4.43 shows the active and reactive powers after compensation by a five-level four-wire SAPF using the proposed *p-q* theory based controller and PS-SPWM technique. The reactive power before compensation which is equal 14.59 kvar is successfully compensated to a very low value. Consequently the power factor at the source end is improved to unity as shown in Fig. 4.44.

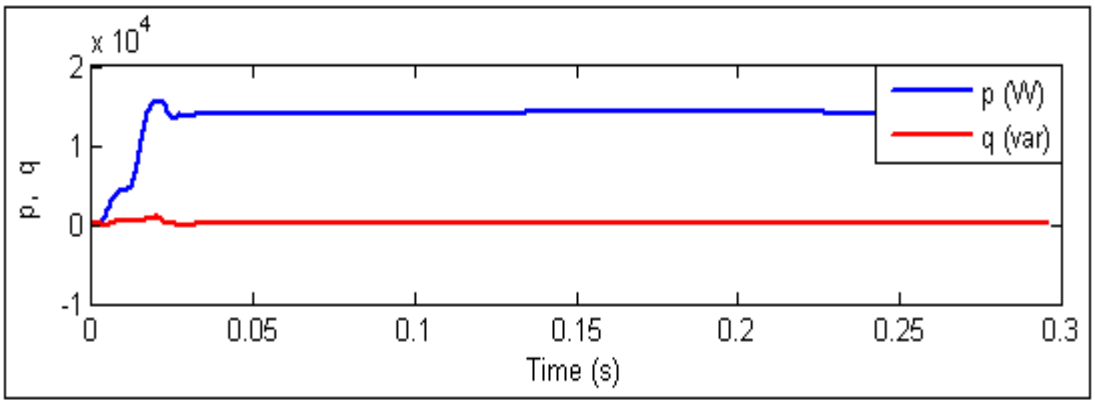


Fig 4.43: Active and reactive powers with five-level SAPF using *p-q* theory based controller and PS-SPWM

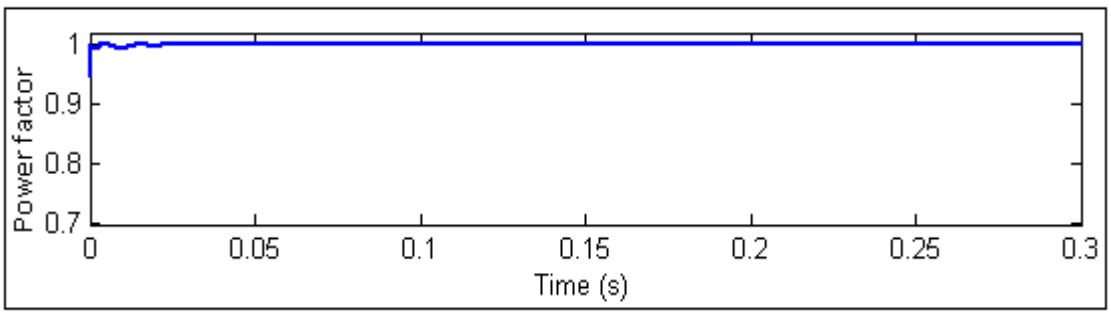


Fig 4.44: Power factor at source end with five-level SAPF using *p-q* theory based controller and PS-SPWM

4.4.1.2 Simulation results with five-level SAPF using proposed d-q-0 theory based controller and PS-SPWM

The proposed controller based on *d-q-0* theory and PS-SPWM technique is presented in Figs. 3.6 and 3.11. The five-level SAPF which has four wires generates the distorted injecting current in leg 'a' as shown in Fig. 4.49 by using the proposed *d-q-0* theory based controller and PS-SPWM technique in order to compensate the distorted current shown in Fig. 4.3. Similar currents but with 120^{o} phase shift are injected by legs 'b' and 'c' of the SAPF into phases 'b' and 'c' of the DS. The injecting current reaches a peak value of 31.83 A as shown in Fig. 4.49.

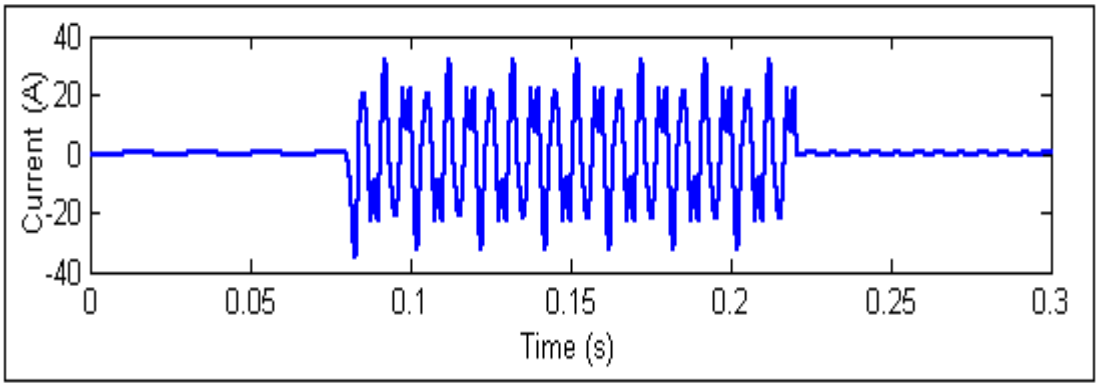


Fig 4.45: Current injected by five-level SAPF using *d-q-0* theory based controller and PS-SPWM

Fig. 4.50 shows phase 'a' source current with and without SAPF. It is found that the five-level four-wire SAPF using the proposed *d-q-0* theory based controller and PS-SPWM technique is able to compensate the source current when it is connected during the interval 0.08 s to 0.22 s. The resultant sinusoidal source current between 0.08 s and 0.22 s reaches a peak value of 83.95 A which is less than the uncompensated peak current of 105.2 A. Similar simulation result and measured value are obtained for the phases 'b' and 'c'.

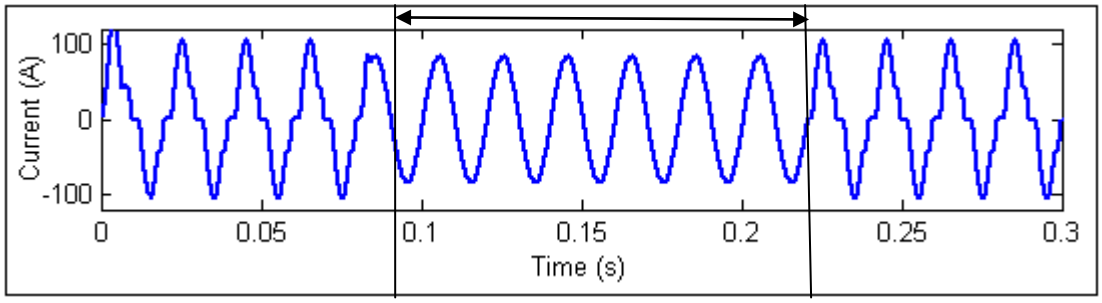
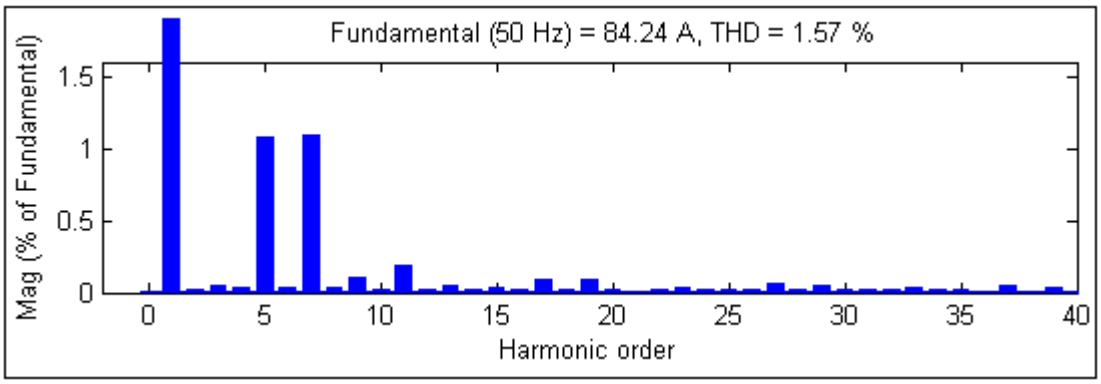
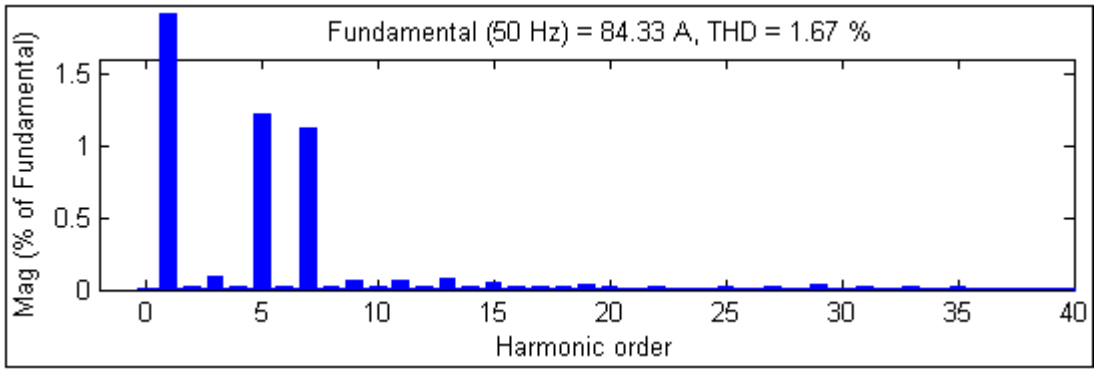


Fig 4.46: Source current with five-level SAPF using *d-q-0* theory based controller and PS-SPWM

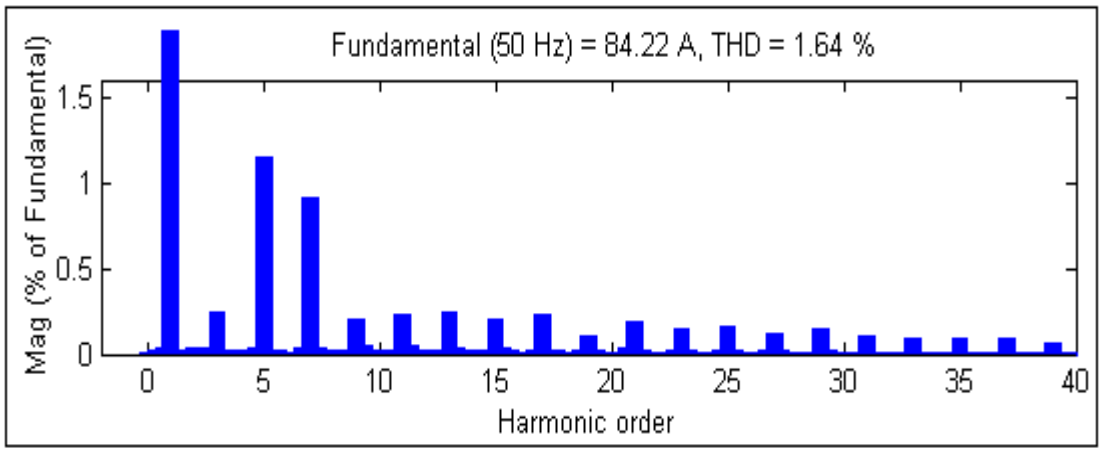
Figs. 4.47 (a) to (c) shows the harmonic spectrum and THD of source currents of phases 'a', 'b' and 'c', respectively. As observed the source current THD is successfully minimized to around 1.64 % as compared to the result before compensation which is 27.51 %. The THDs for the first 40 harmonics calculated for all phase currents is demonstrated to be less than the prescribed value by IEEE-519 Standards.



(a) Phase 'a' source current



(b) Phase 'b' source current



(c) Phase 'c' source current

Fig 4.47: (a) to (c) Harmonic spectrum and THD of source current with five-level SAPF using *d-q-0* theory based controller and PS-SPWM

Fig. 4.48 shows the compensating injected current into the neutral conductor by five-level four-wire SAPF using the proposed *d-q-0* theory based controller and PS-SPWM technique in order to minimize the source neutral current to zero between the interval 0.08 s and 0.22 s.

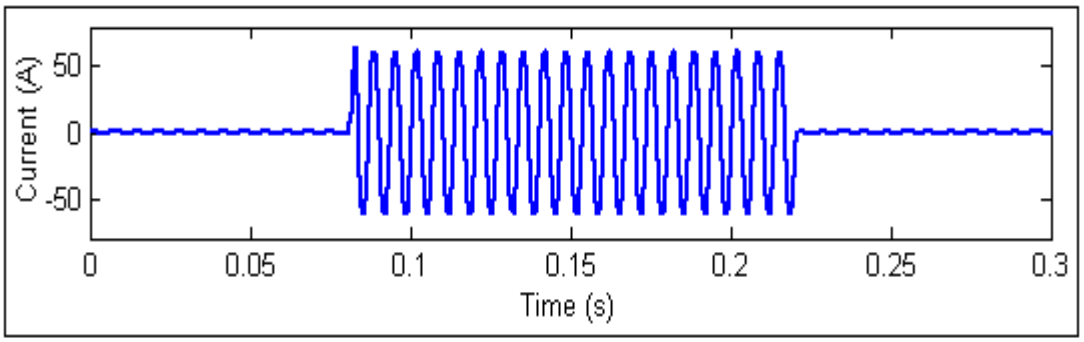


Fig 4.48: Current injected into the neutral conductor by five-level SAPF using *d-q-0* theory based controller and PS-SPWM

It is found that the five-level four-wire SAPF using the proposed *d-q-0* theory based controller and PS-SPWM technique is able to minimize the source neutral current to nearly zero when it is connected during the interval 0.08 s to 0.22 s as shown in Fig. 4.49.

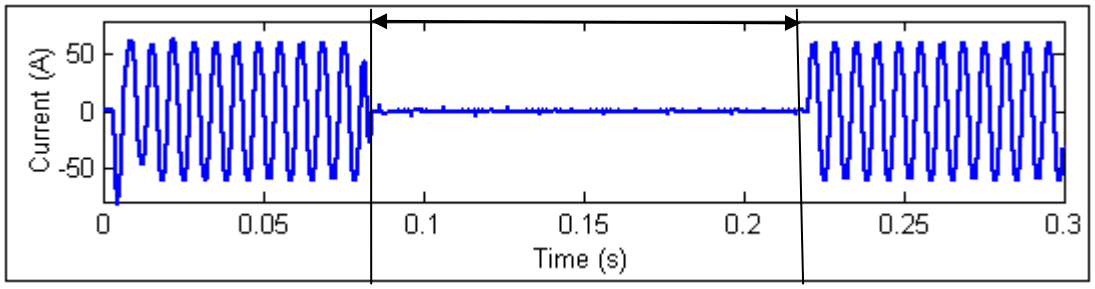


Fig 4.49: Simulated source neutral current with five-level SAPF using *d-q-0* theory based controller and PS-SPWM

Fig. 4.50 shows phase 'a' source voltage and source current, where the current is non-sinusoidal except during the interval between 0.08 s and 0.22 s when the SAPF has come into operation. During the interval between 0.08 s and 0.22 s the source current is sinusoidal and is in-phase with the source voltage. Thus, it can be concluded that the developed five-level four-wire SAPF using the proposed *d-q-0* theory based controller and PS-SPWM technique has successfully compensated the harmonic load currents and improved the supply power factor to nearly unity. Similar results are obtained for the phases 'b' and 'c' also.

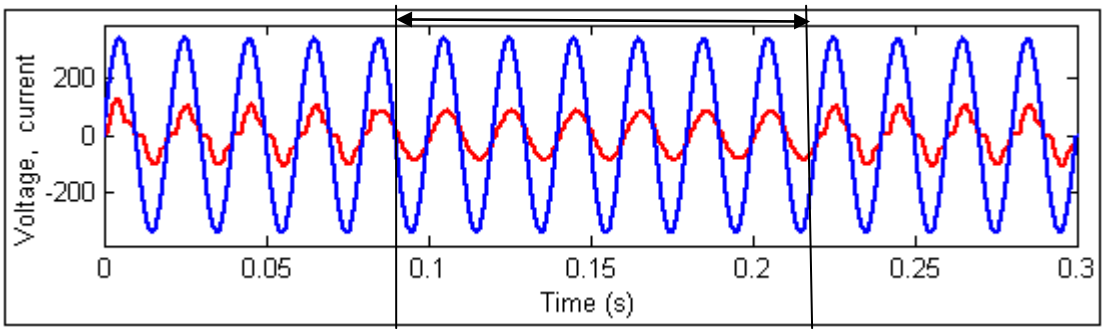


Fig 4.50: Source voltage and source current with five-level SAPF using *d-q-0* theory based controller and PS-SPWM

Fig. 4.51 shows the active and reactive powers after compensation by a five-level four-wire SAPF using proposed *d-q-0* theory based controller and PS-SPWM technique. The reactive power before compensation which is equal 14.59 kvar is successfully compensated to a very low value. Consequently the power factor at the source end is improved to 0.986 as shown in Fig. 4.52.

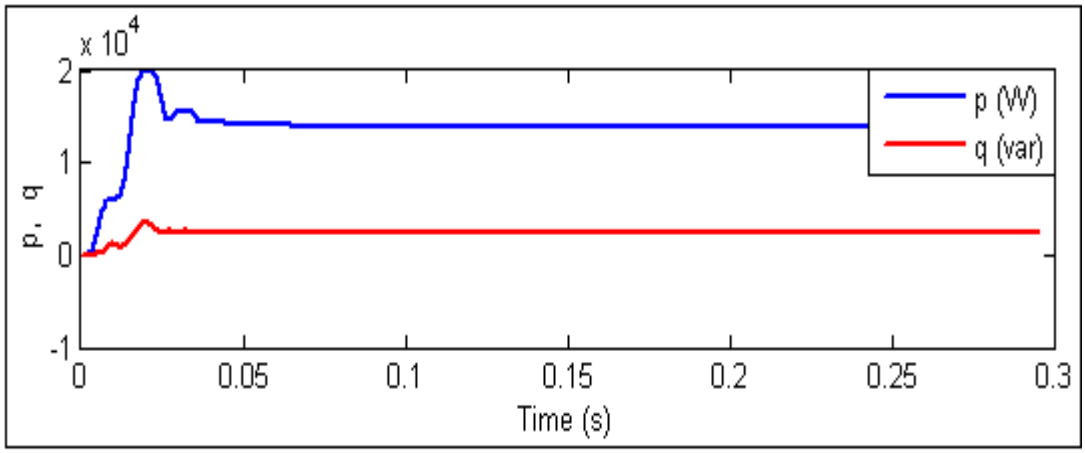


Fig 4.51: Active and reactive powers with five-level SAPF using *d-q-0* theory based controller and PS-SPWM

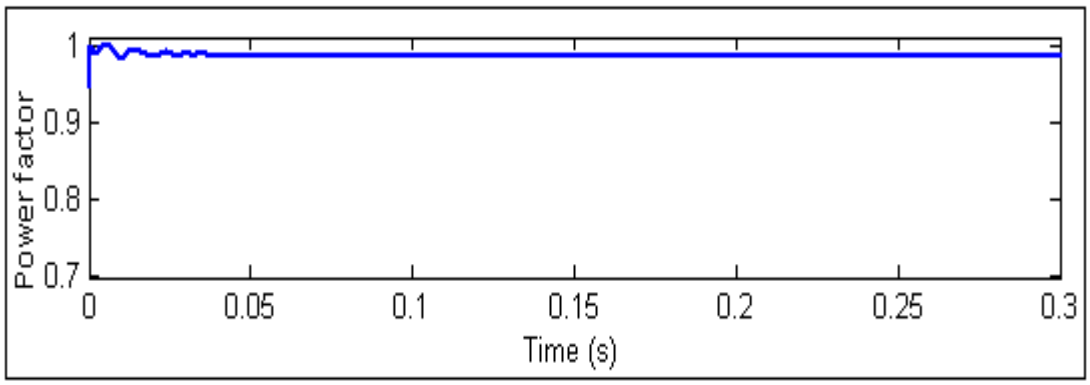


Fig 4.52: Power factor at source end with five-level SAPF using *d-q-0* theory based controller and PS-SPWM

4.4.1.3 Simulation results with five-level SAPF using proposed a-b-c theory based controller and PS-SPWM

The proposed controller based on *a-b-c* theory and PS-SPWM technique is presented as in Figs. 3.8 and 3.11. The five-level SAPF which has four wires generates the distorted injecting current in leg 'a' as shown in Fig. 4.53 by using the proposed *a-b-c* theory based controller and PS-SPWM technique in order to compensate the distorted current shown in Fig. 4.3. Similar currents but with 120^{o} phase shift are injected by legs 'b' and 'c' of the SAPF into phases 'b' and 'c' of the distribution system. The injected current reaches a peak value of 34.90 A as shown in Fig. 4.53.

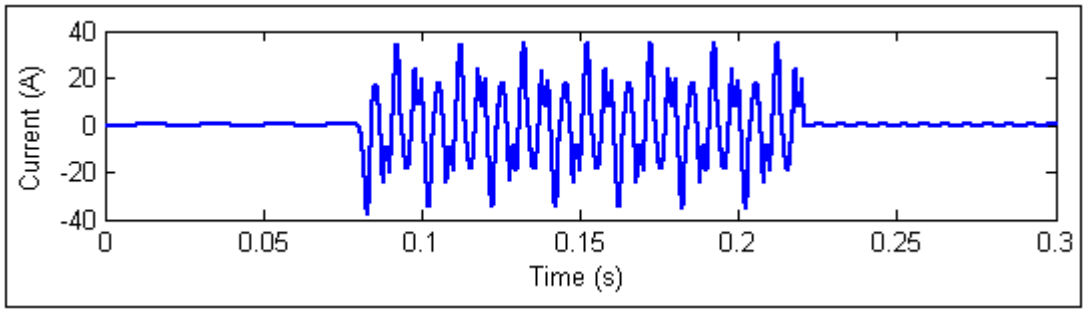


Fig 4.53: Current injected by five-level SAPF using *a-b-c* theory based controller and PS-SPWM

Fig. 4.58 shows phase 'a' source current with and without SAPF. It is found that the five-level four-wire SAPF using the proposed *a-b-c* theory based controller and PS-SPWM technique is able to compensate the source current when it is connected during the interval 0.08 s to 0.22 s. The resultant sinusoidal source current between 0.08 s and 0.22 s reaches a peak value of 87.01 A which is less than the uncompensated peak current of 105.2 A. Similar simulation result and measured value are obtained for the phases 'b' and 'c'.

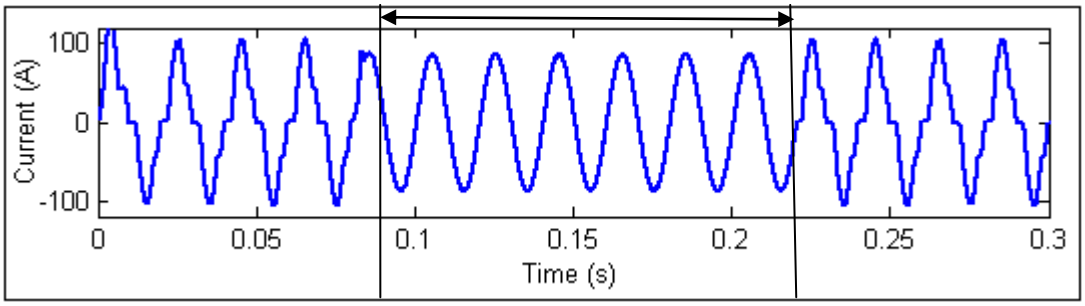
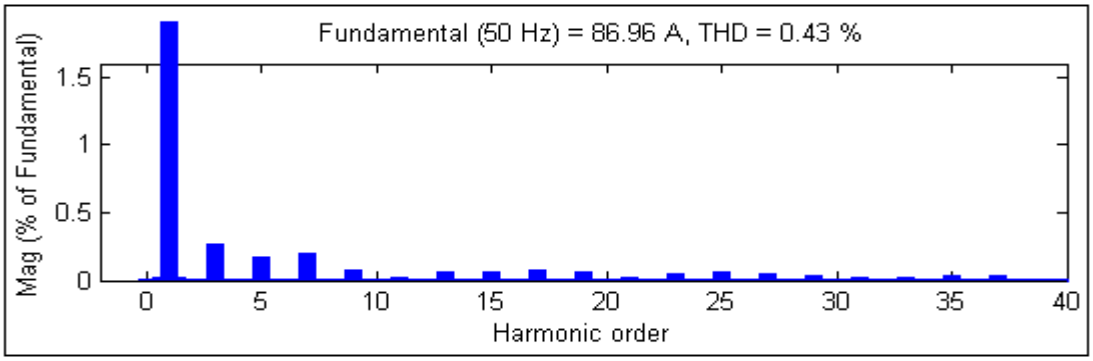
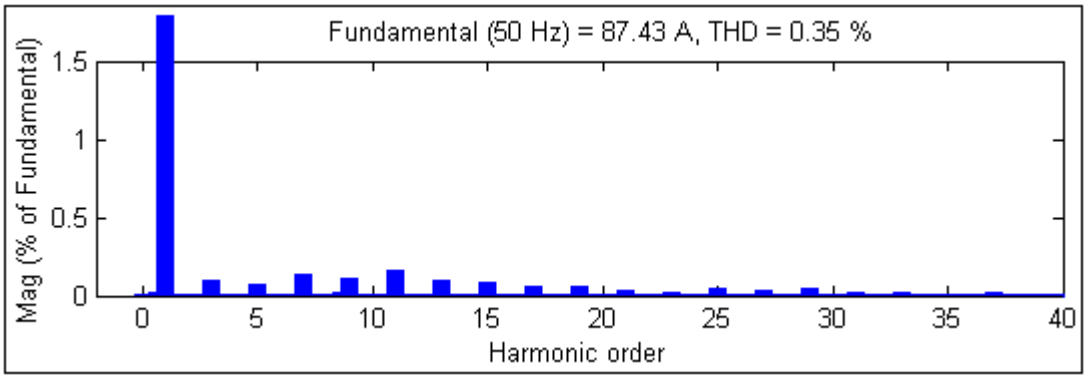


Fig 4.54: Source current with five-level SAPF using *a-b-c* theory based controller and PS-SPWM

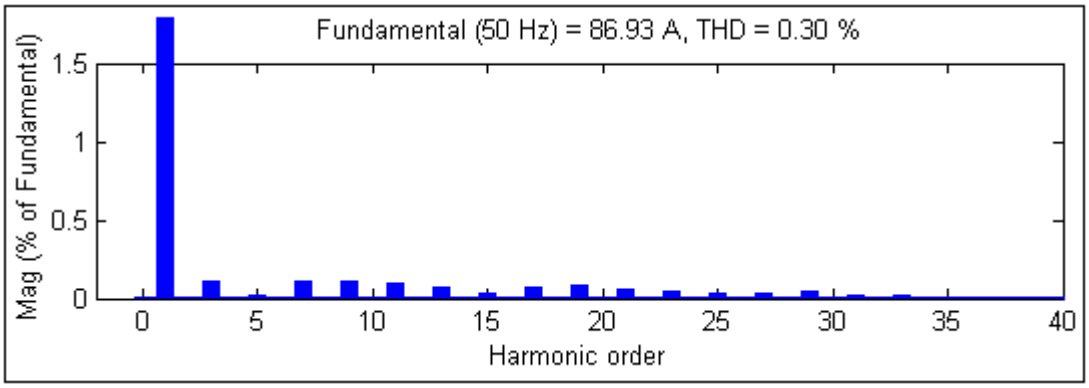
Figs. 4.55 (a) to (c) shows the harmonic spectrum and THD of source currents of phases 'a', 'b' and 'c', respectively. As observed the source current THD is successfully minimized to 0.43 %, 0.35 % and 0.30 % for the phases 'a', 'b' and 'c', respectively, as compared to the result before compensation which is 27.51 %. The THDs for the first 40 harmonics calculated for all phase currents is demonstrated to be less than the prescribed value by IEEE-519 Standards.



(a) Phase 'a' source current



(b) Phase 'b' source current



(c) Phase 'c' source current

Fig 4.55: (a) to (c) Harmonic spectrum and THD of source currents with five-level SAPF using *a-b-c* theory based controller and PS-SPWM

Fig. 4.56 shows the compensating injected current into the neutral conductor by five-level four-wire SAPF using the proposed *a-b-c* theory based controller and PS-SPWM technique in order to minimize the source neutral current to zero between the interval 0.08 s and 0.22 s.

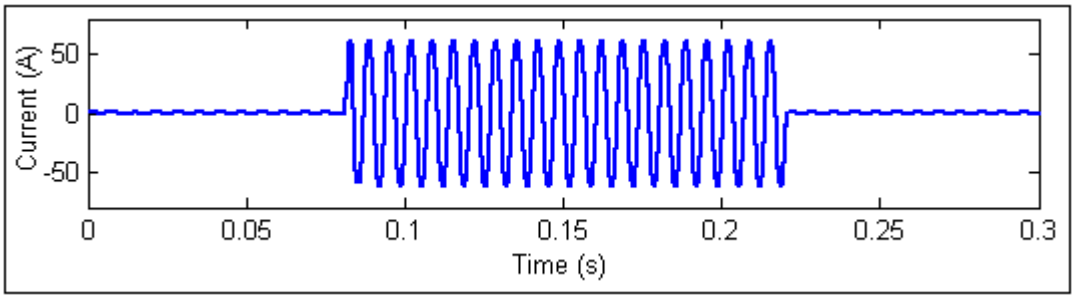


Fig 4.56: Current injected into the neutral conductor by five-level SAPF using *a-b-c* theory based controller and PS-SPWM

It is found that the five-level four-wire SAPF using the proposed *a-b-c* theory based controller and PS-SPWM technique is able to minimize the source neutral current to nearly zero when it is connected during the interval 0.08 s to 0.22 s as shown in Fig. 4.57.

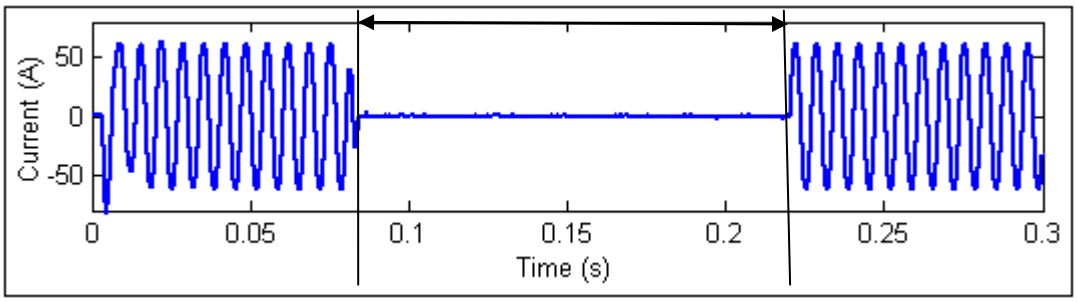


Fig 4.57: Simulated source neutral current with five-level SAPF using *a-b-c* theory based controller and PS-SPWM

Fig. 4.58 shows phase 'a' source voltage and source current, where the current is non-sinusoidal except during the interval between 0.08 s and 0.22 s when the SAPF has come into operation. During the interval between 0.08 s and 0.22 s the source current is sinusoidal and is in-phase with the source voltage. Thus, it can be concluded that the developed five-level four-wire SAPF using the proposed *a-b-c* theory based controller and PS-SPWM technique has successfully compensated the harmonic load currents and improved the supply power factor to nearly unity. Similar results are obtained for the phases 'b' and 'c' also.

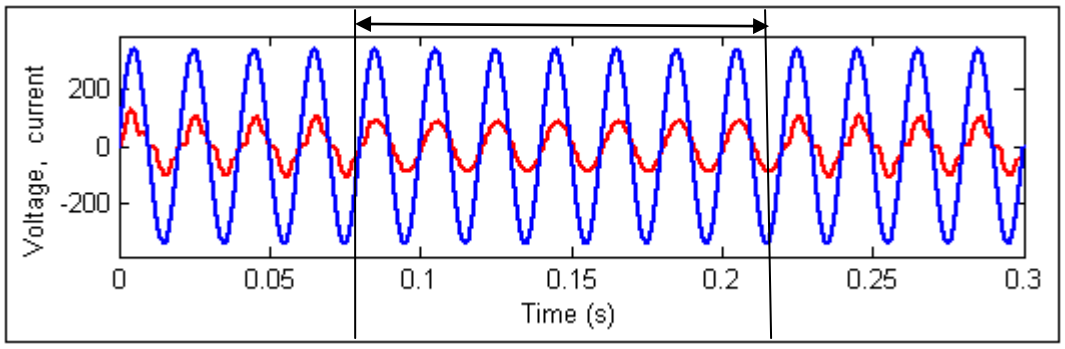


Fig 4.58: Source voltage and source current with five-level SAPF using *a-b-c* theory based controller and PS-SPWM

Fig. 4.59 shows the active and reactive powers after compensation by a five-level four-wire SAPF using proposed *a-b-c* theory based controller and PS-SPWM technique. The reactive power before compensation which is equal 14.59 kvar is successfully compensated to a very low value. Consequently the power factor at the source end is improved to 0.989 as shown in Fig. 4.60.

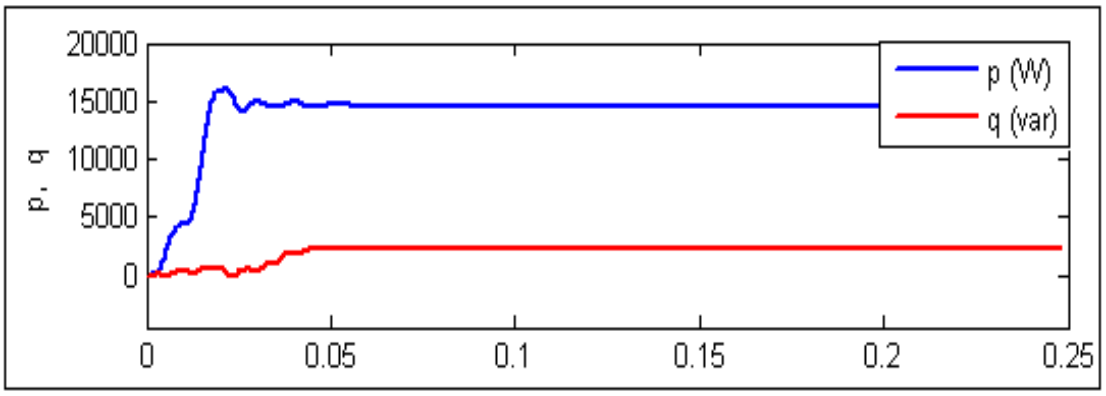


Fig 4.59: Active and reactive powers with five-level SAPF using *a-b-c* theory based controller and PS-SPWM

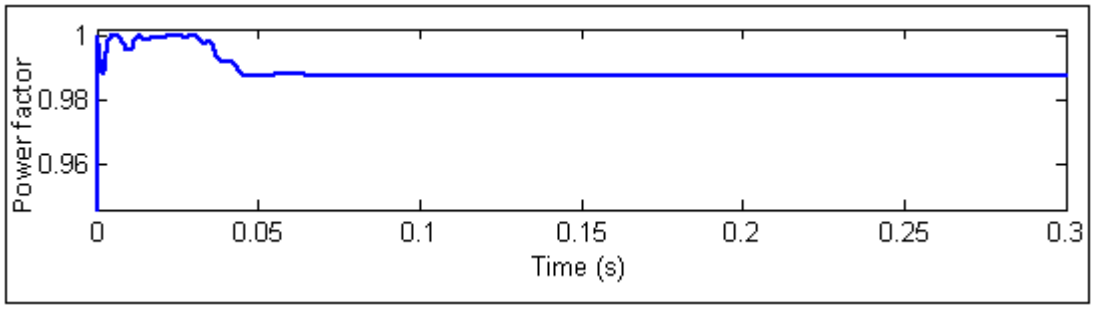


Fig 4.60: Power factor at source end with five-level SAPF using *a-b-c* theory based controller and PS-SPWM

To compare the performance of five-level four-wire SAPF by the proposed three types of controllers and PS-SPWM technique, the THDs of source currents are presented as in Table 4.5. It can be observed that in all the three cases the THD is less than the prescribed limit of 5 % as recommended by IEEE-519 standards. However, the THD obtained by the proposed *a-b-c* theory based controller is far less than by the other two controllers as illustrated in Table 4.5.

Table 4.5: Source currents THD with five-level SAPF using PS-SPWM

Controller	THD *p-q* theory	THD *d-q-0* theory	THD *a-b-c* theory
Phase 'a'	2.23	1.57	0.43
Phase 'b'	2.24	1.67	0.35
Phase 'c'	2.20	1.64	0.30

Simulation results of compensated source neutral currents by five-level four-wire SAPF using the three types of proposed controllers and PS-SPWM technique are given as in Table. 4.6. As observed these currents are far less than the value of 64.17 A before compensation. However the controller based on *d-q-0* theory reduced the source neutral conductor current to a very small value of 0.70 A as shown in Table. 4.6.

Table 4.6: Source neutral current with five-level SAPF using PS-SPWM

Controller type	*p-q* theory	*d-q-0* theory	*a-b-c* theory
Peak neutral current	0.95 A	0.70 A	1.20 A

Simulation results for power factor at the source end with five-level four-wire SAPF using the three different proposed controllers and PS-SPWM technique is given in Table 4.7. It can be observed that the power factor is greatly improved as compared to the value before compensation which is 0.8056. However the controller based on *p-q* theory improved the source end power factor to unity as shown in Table 4.7 which makes the source current sinusoidal.

Table 4.7: Power factor at source end with five-level SAPF using PS-SPWM

Controller type	*p-q* theory	*d-q-0* theory	*a-b-c* theory
Supply Power factor	1.0	0.986	0.989

To observe the effect of switching in operation of the five-level SAPF, the recorded peak transient current at source is presented as in Table 4.8. It is observed that *d-q-0* theory based controller with PS-SPWM technique gives less peak current as compared to the other two controllers as shown in Table 4.8.

Table 4.8: Transient current with five-level SAPF using PS-SPWM

Controller type	*p-q* theory	*d-q-0* theory	*a-b-c* theory
Peak transient current	98.92 A	86.27 A	87.91 A

4.4.2 Simulation results with five-level SAPF using LS-SPWM

The LS-SPWM technique which is introduced in section 3.6.3 of Chapter 3 is used to generate the PWM signals in order to control the five-level CHB-VSI based SAPF as shown in Appendix D. The sinusoidal modulation signal (reference current) is compared with four triangular carrier signals using three types of LS-SPWM such as IPD, APOD and POD modulation techniques. Simulation results are presented in each case.

4.4.2.1 Simulation results with five-level SAPF using p-q theory based controller and IPD

The proposed controller based on *p-q* theory and IPD modulation technique is presented as in Figs. 3.4 and 3.13. The five-level SAPF which has four wires generates the distorted injecting current in leg ‘a’ as shown in Fig. 4.69 by using the proposed *p-q* theory based controller and IPD modulation technique in order to compensate the distorted current as shown in Fig. 4.3. Similar currents but with 120^{o} phase shift are injected by legs ‘b’ and ‘c’ of the SAPF into phases ‘b’ and ‘c’ of the distribution system. The injected current reaches a peak value of 49.22 A as shown in Fig. 4.61.

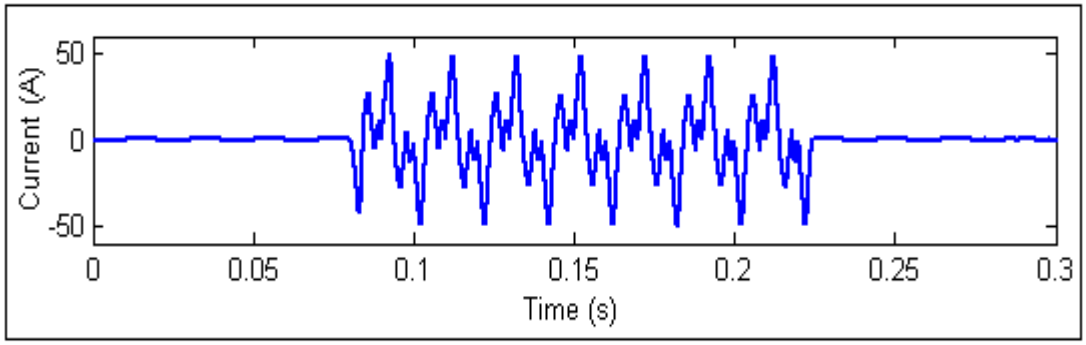


Fig 4.61: Current injected by five-level SAPF using *p-q* theory based controller and IPD

Fig. 4.62 shows phase 'a' source current with and without SAPF. It is found that the five-level four-wire SAPF using the proposed *p-q* theory based controller and IPD modulation technique is able to compensate the source current when it is connected during the interval 0.08 s to 0.22 s. The resultant sinusoidal source current between 0.08 s and 0.22 s reaches a peak value of 84.55 A which is less than the uncompensated peak current of 105.2 A. Similar simulation result and measured value are obtained for the phases 'b' and 'c'.

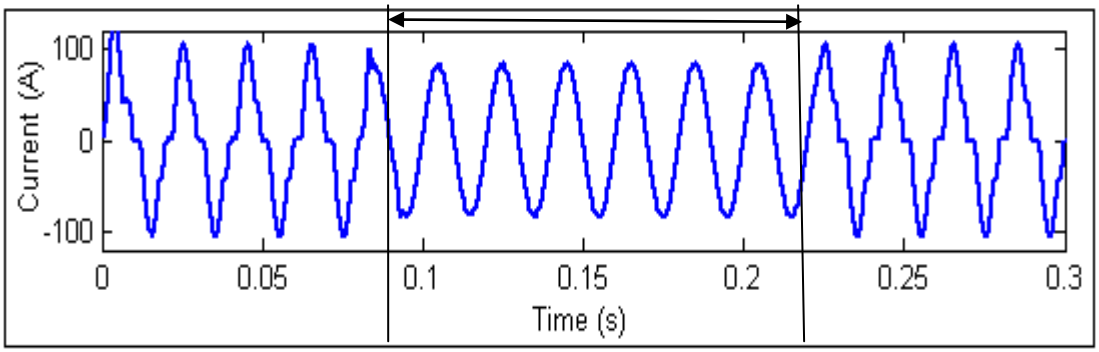
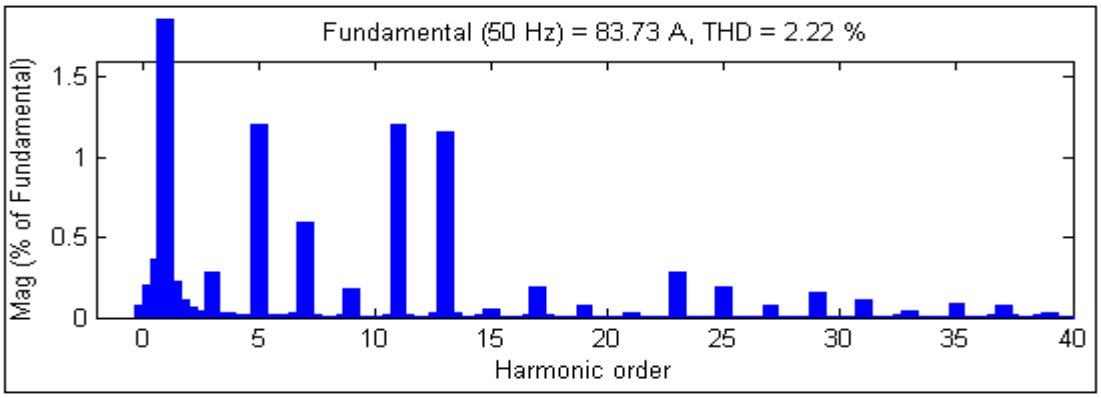
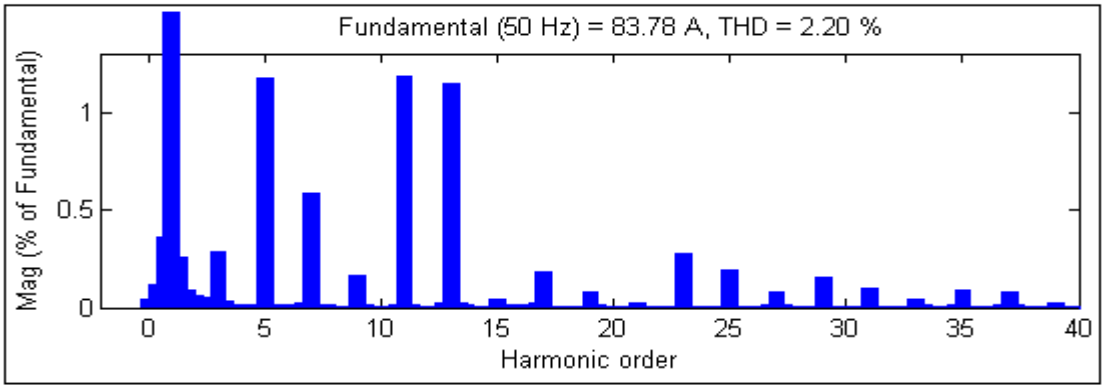


Fig 4.62: Source current with five-level SAPF using *p-q* theory based controller and IPD

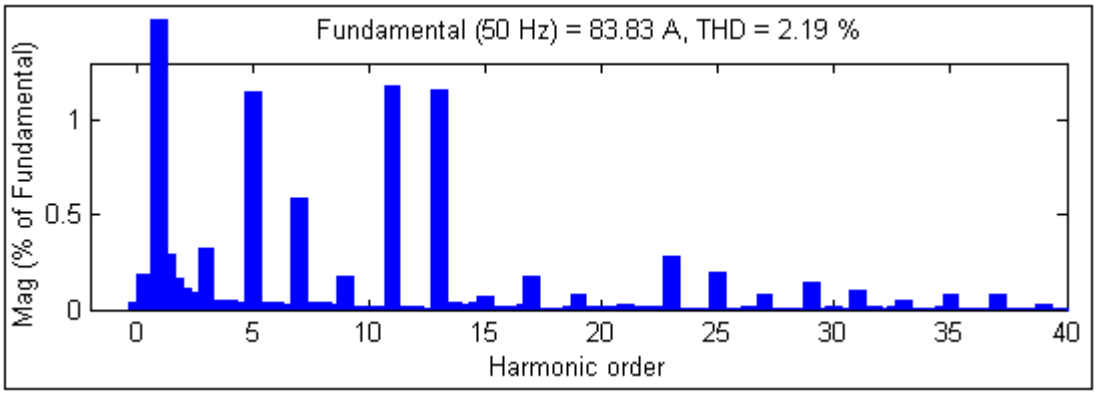
Figs. 4.63 (a) to (c) shows the harmonic spectrum and THD of source currents of phases 'a', 'b' and 'c', respectively. As observed the source current THD is successfully minimized to around 2.20 % as compared to the result before compensation which is 27.51 %. The THDs for the first 40 harmonics calculated for all phase currents is demonstrated to be less than the prescribed value by IEEE-519 Standards.



(a) Phase 'a' source current



(b) Phase 'b' source current



(c) Phase 'c' source current

Fig 4.63: (a) to (c) Harmonic spectrum and THD of source currents with five-level SAPF using *p-q* theory based controller and IPD

Fig. 4.64 shows the compensating injected current into the neutral conductor by five-level four-wire SAPF using the proposed *p-q* theory based controller and IPD modulation technique in order to minimize the source neutral current to zero between the interval 0.08 s and 0.22 s.

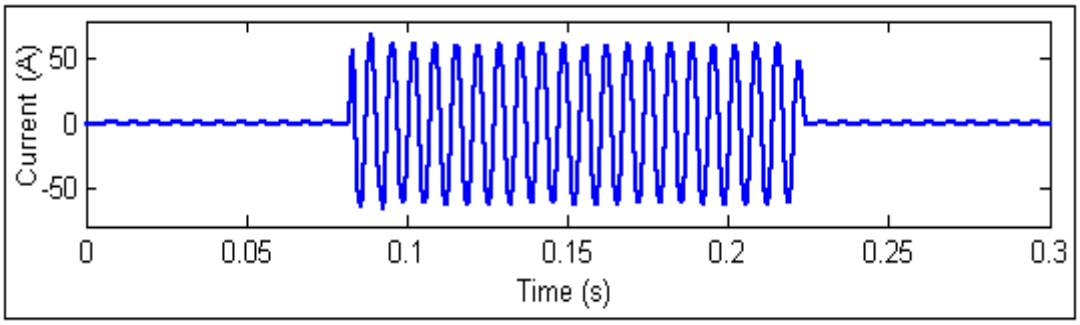


Fig 4.64: Current injected into the neutral conductor by five-level SAPF using *p-q* theory based controller and IPD

It is found that the five-level four-wire SAPF using the proposed *p-q* theory based controller and IPD modulation technique is able to minimize the source neutral current to nearly zero when it is connected during the interval 0.08 s to 0.22 s as shown in Fig. 4.65.

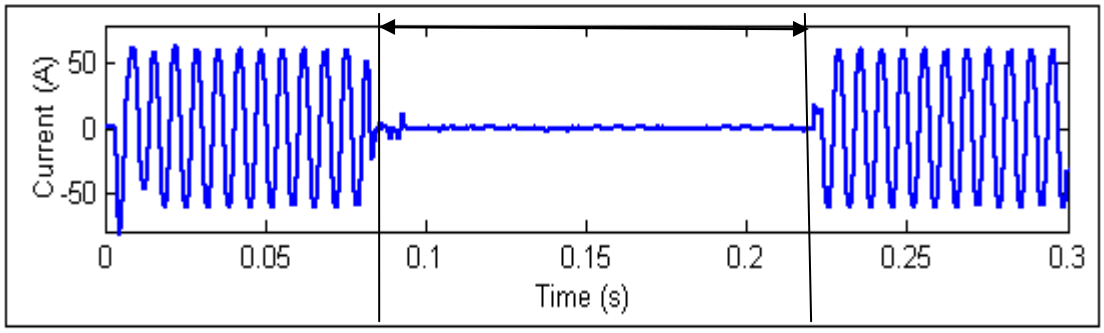


Fig 4.65: Simulated source neutral current with five-level SAPF using *p-q* theory based controller and IPD

Fig. 4.66 shows phase 'a' source voltage and source current, where the current is non-sinusoidal except during the interval between 0.08 s and 0.22 s when the SAPF has come into operation. During the interval between 0.08 s and 0.22 s the source current is sinusoidal and is in phase with the source voltage. Thus, it can be concluded that the developed five-level four-wire SAPF using the proposed *p-q* theory based controller and IPD modulation technique has successfully compensated the harmonic load currents and improved the supply power factor to nearly unity. Similar results are obtained for the phases 'b' and 'c' also.

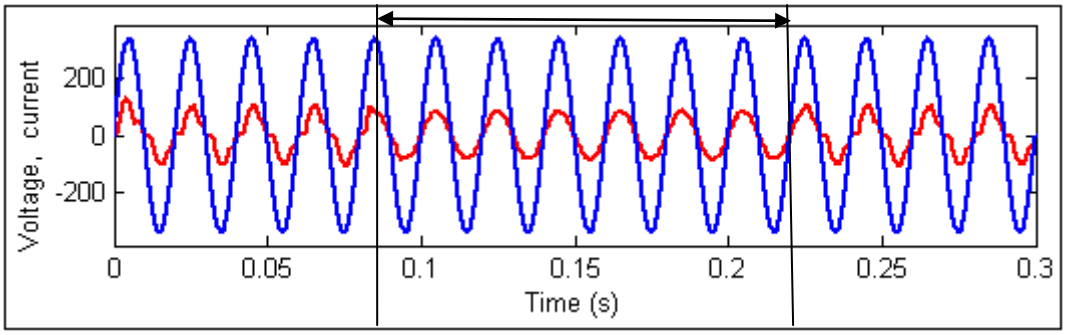


Fig 4.66: Source voltage and source current with five-level SAPF *p-q* theory based controller and IPD

Fig. 4.67 shows the active and reactive powers after compensation by a five-level four-wire SAPF using the proposed *p-q* theory based controller and IPD modulation technique. The reactive power before compensation which is equal 14.59 kvar is successfully compensated to a very low value. Consequently the power factor at the source end is improved to unity as shown in Fig. 4.68.

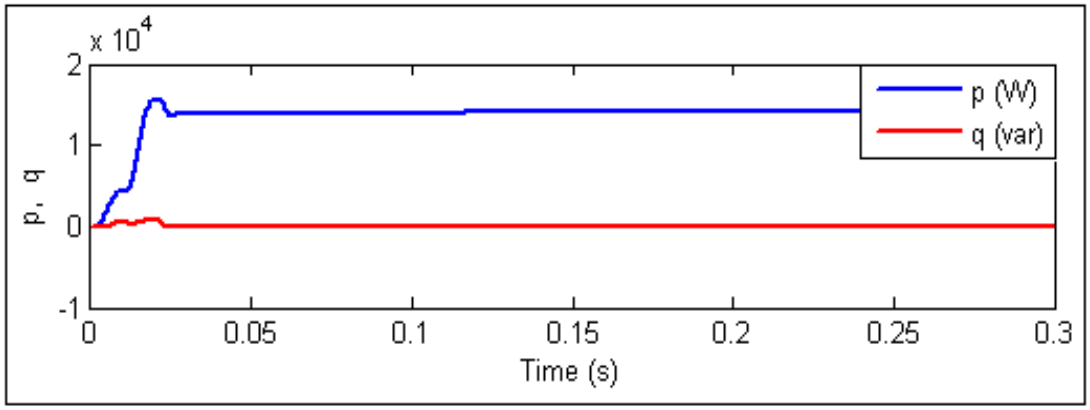


Fig 4.67: Active and reactive powers with five-level SAPF using *p-q* theory based controller and IPD

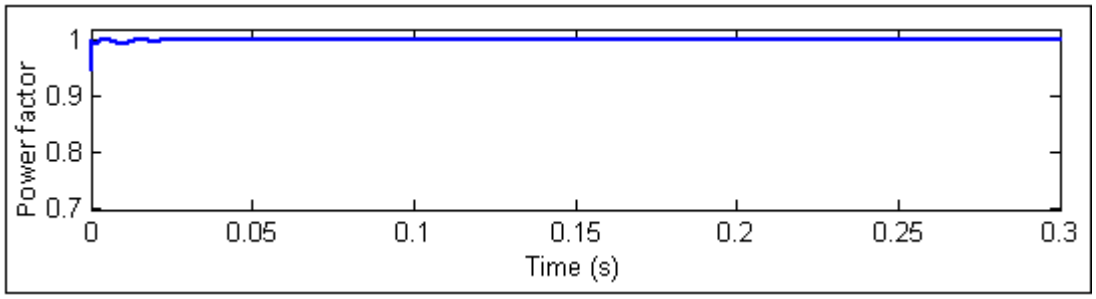


Fig 4.68: Power factor at source end with five-level SAPF using *p-q* theory based controller and IPD

4.4.2.2 *Simulation results with five-level SAPF using proposed d-q-0 theory based controller and IPD*

The proposed controller based on *d-q-0* theory and IPD modulation technique is presented as in Figs. 3.6 and 3.13. The five-level SAPF which has four wires generates the distorted injecting current in leg 'a' as shown in Fig. 4.69 by using the proposed *d-q-0* theory based controller and IPD modulation technique in order to compensate the distorted current shown in Fig. 4.3. Similar currents but with 120^{o} phase shift are injected by legs 'b' and 'c' of the SAPF into phases 'b' and 'c' of the distribution system. The injected current reaches a peak value of 32.70 A as shown in Fig. 4.69.

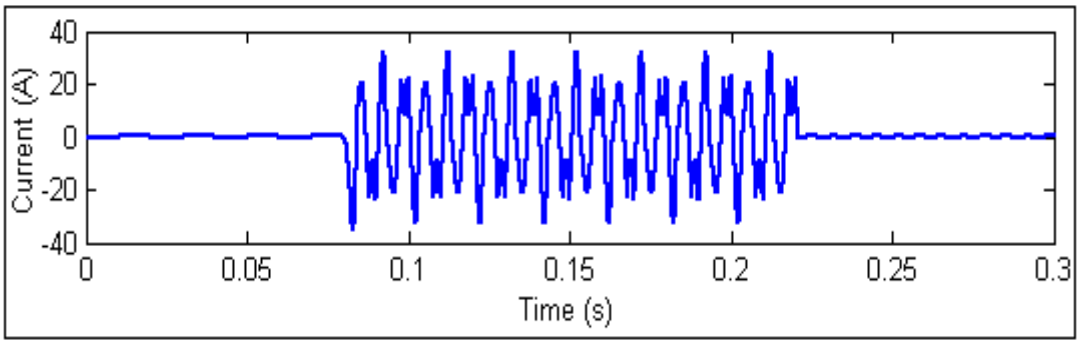


Fig 4.69: Current injected by five-level SAPF using *d-q-0* theory based controller and IPD

Fig. 4.70 shows phase 'a' source current with and without SAPF. It is found that the five-level four-wire SAPF using the proposed *d-q-0* theory based controller and IPD modulation technique is able to compensate the source current when it is connected during the interval 0.08 s to 0.22 s. The resultant sinusoidal source current between 0.08 s and 0.22 s reaches a peak value of 84.97 A which is less than the uncompensated peak current of 105.2 A. Similar simulation result and measured value are obtained for the phases 'b' and 'c'.

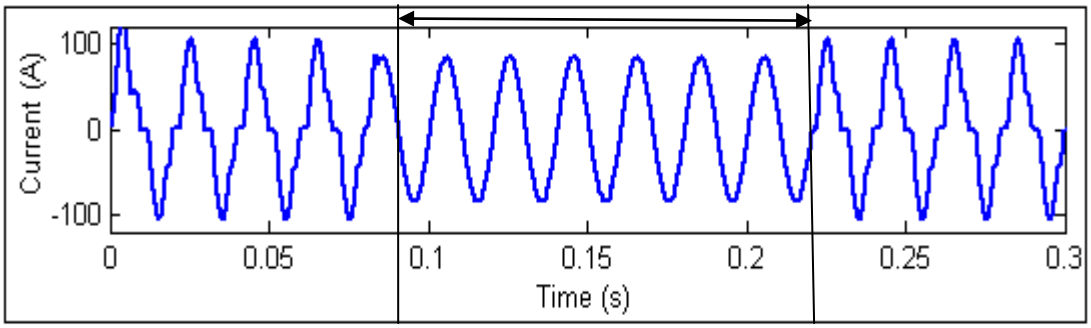
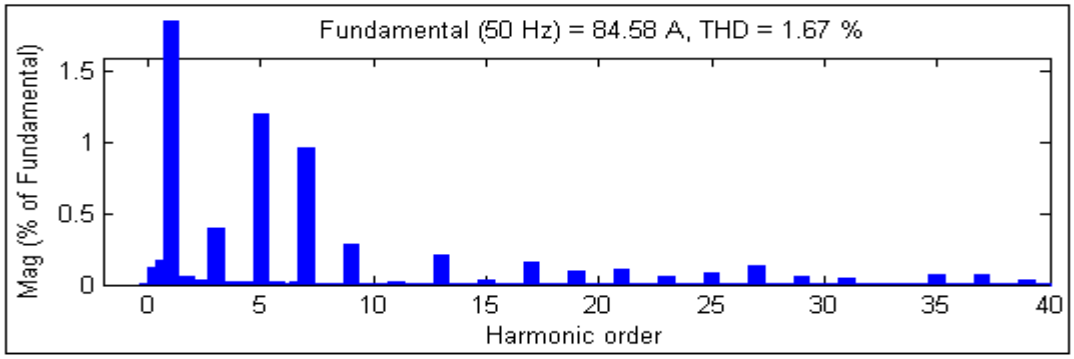
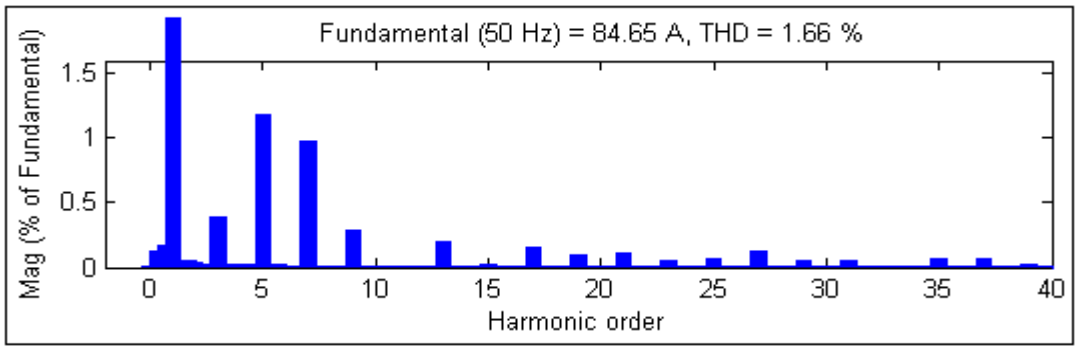


Fig 4.70: Source current with five-level SAPF using *d-q-0* theory based controller and IPD

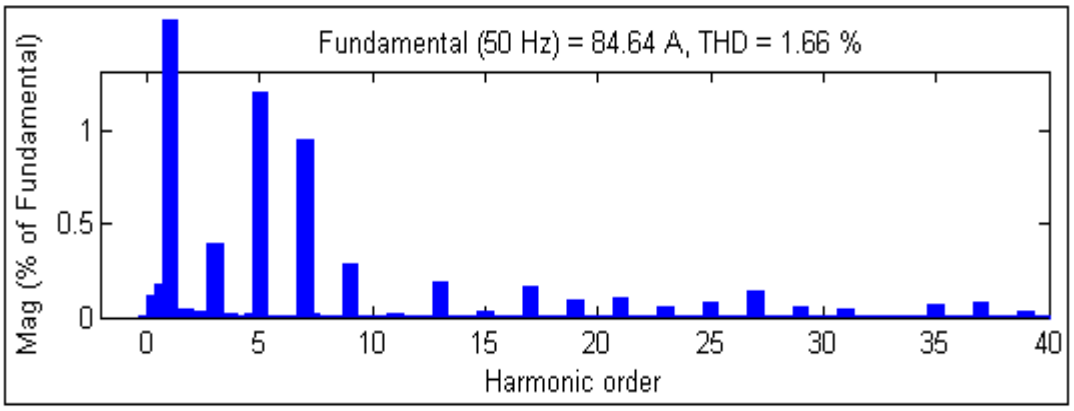
Figs. 4.71 (a) to (c) shows the harmonic spectrum and THD of source currents of phases 'a', 'b' and 'c', respectively. As observed the source current THD is successfully minimized to around 1.66 % as compared to the result before compensation which is 27.51 %. The THDs for the first 40 harmonics calculated for all phase currents is demonstrated to be less than the prescribed value by IEEE-519 Standards.



(a) Phase 'a' source current



(b) Phase 'b' source current



(c) Phase 'c' source current

Fig 4.71: (a) to (c) Harmonic spectrum and THD of source currents with five-level SAPF using *d-q-0* theory based controller and IPD

Fig. 4.72 shows the compensating injected current into the neutral conductor by five-level four-wire SAPF using the proposed *d-q-0* theory based controller and IPD modulation technique in order to minimize the source neutral current to zero between the interval 0.08 s and 0.22 s.

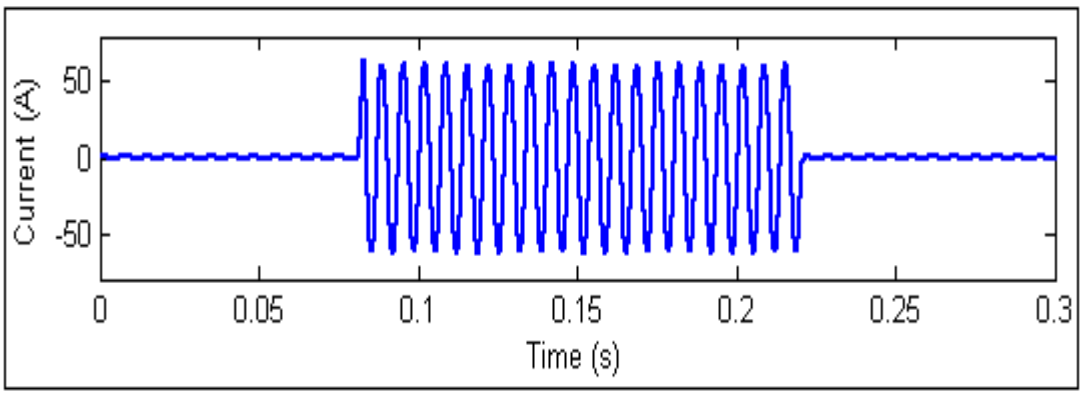


Fig 4.72: Current injected into the neutral conductor by five-level SAPF using *d-q-0* theory based controller and IPD

It is found that the five-level four-wire SAPF using the proposed *d-q-0* theory based controller and IPD modulation technique is able to minimize the source neutral current to nearly zero when it is connected during the interval 0.08 s to 0.22 s as shown in Fig. 4.73.

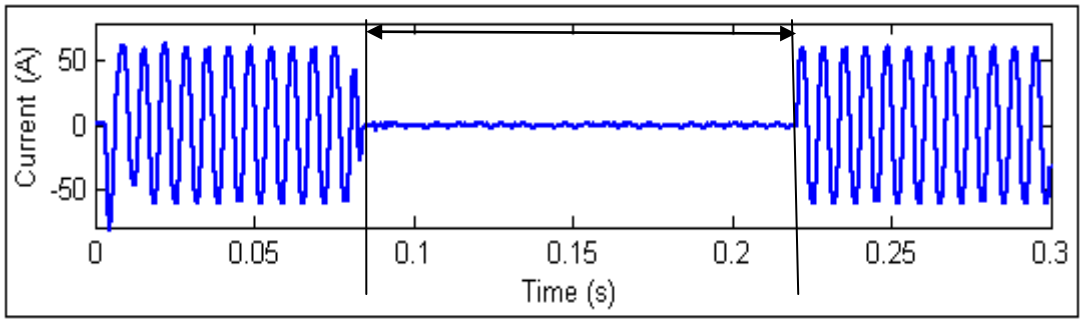


Fig 4.73: Simulated source neutral current with five-level SAPF using *d-q-0* theory based controller and IPD

Fig. 4.74 shows phase 'a' source voltage and source current, where the current is non-sinusoidal except during the interval between 0.08 s and 0.22 s when the SAPF has come into operation. During the interval between 0.08 s and 0.22 s the source current is sinusoidal and is in phase with the source voltage. Thus, it can be concluded that the developed five-level four-wire SAPF using the proposed *d-q-0* theory based controller and IPD modulation technique has successfully compensated the harmonic load currents and improved the supply power factor to nearly unity. Similar results are obtained for the phases 'b' and 'c' also.

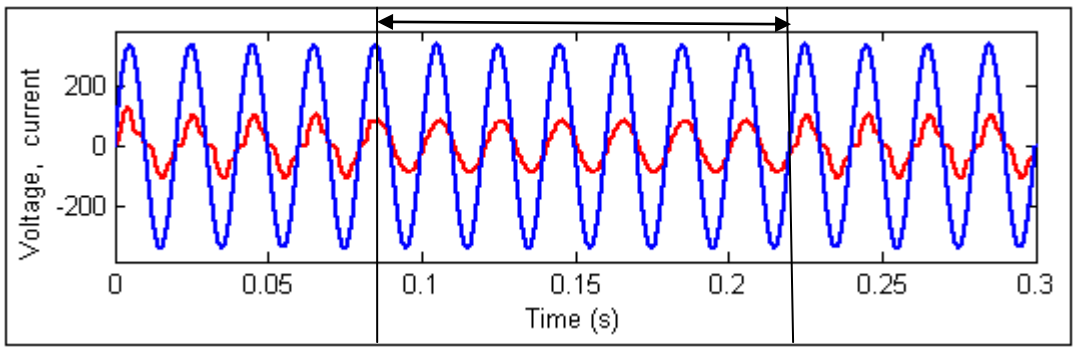


Fig 4.74: Source voltage and source current with five-level SAPF using *d-q-0* theory based controller and IPD

Fig. 4.75 shows the active and reactive powers after compensation by a five-level four-wire SAPF using proposed *d-q-0* theory based controller and IPD modulation technique. The reactive power before compensation which is equal 14.59 kvar is successfully compensated to a very low value. Consequently the power factor at the source end is improved to 0.986 as shown in Fig. 4.76.

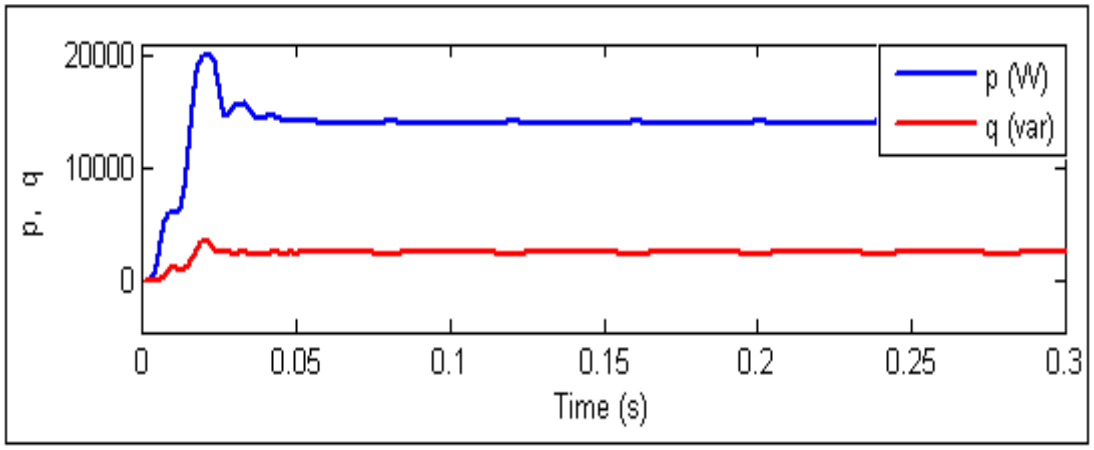


Fig 4.75: Active and reactive powers with five-level SAPF using *d-q-0* theory based controller and IPD

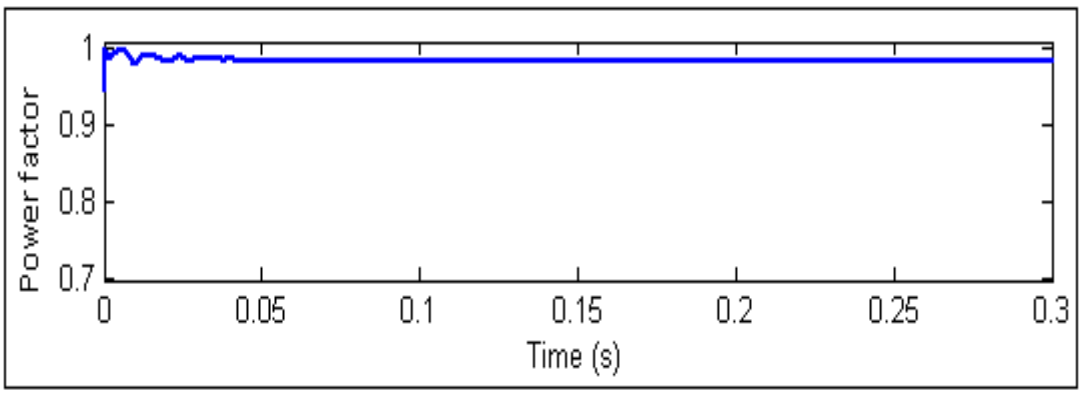


Fig 4.76: Power factor at source end with five-level SAPF using *d-q-0* theory based controller and IPD

4.4.2.3 Simulation results with five-level SAPF using proposed a-b-c theory based controller and IPD

The proposed controller based on *a-b-c* theory and IPD modulation technique is presented as in Figs. 3.8 and 3.13. The five-level SAPF which has four wires generates the distorted injecting current in leg 'a' as shown in Fig. 4.77 by using the proposed *a-b-c* theory based controller and IPD modulation technique in order to compensate the distorted current shown in Fig. 4.3. Similar currents but with 120^{o} phase shift are injected by legs 'b' and 'c' of the SAPF into phases 'b' and 'c' of the distribution system. The injected current reaches a peak value of 34.70 A as shown in Fig. 4.77.

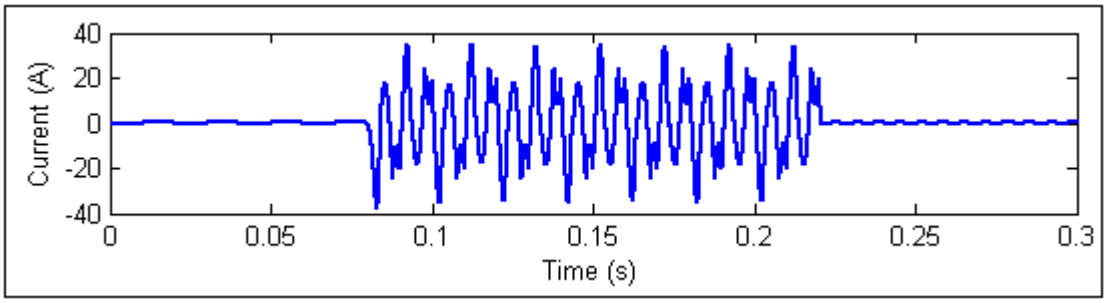


Fig 4.77: Injected current by five-level SAPF using *a-b-c* theory based controller and IPD

Fig. 4.78 shows phase 'a' source current with and without SAPF. It is found that the five-level four-wire SAPF using the proposed *a-b-c* theory based controller and IPD modulation technique is able to compensate the source current when it is connected during the interval 0.08 s to 0.22 s. The resultant sinusoidal source current between 0.08 s and 0.22 s reaches a peak value of 87.42 A which is less than the uncompensated peak current of 105.2 A. Similar simulation result and measured value is obtained for the phases 'b' and 'c'.

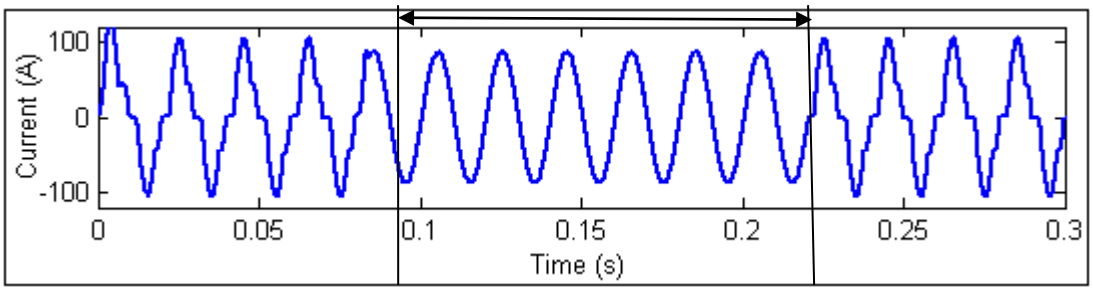
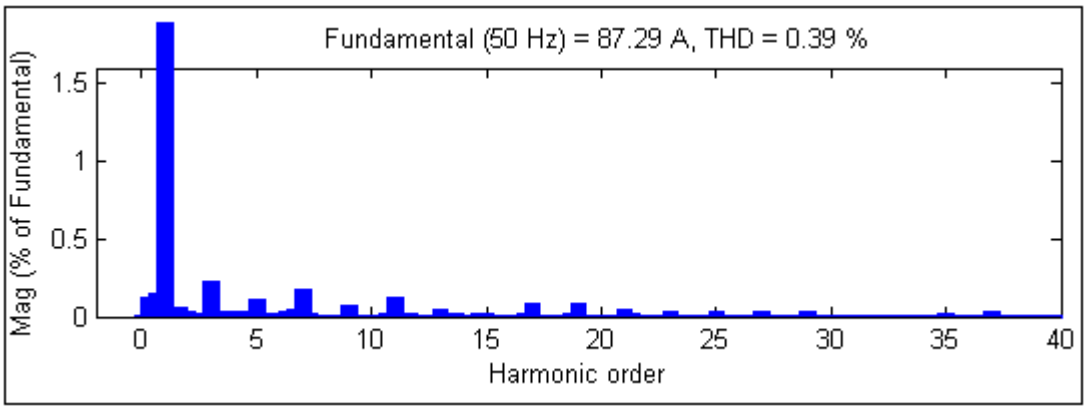
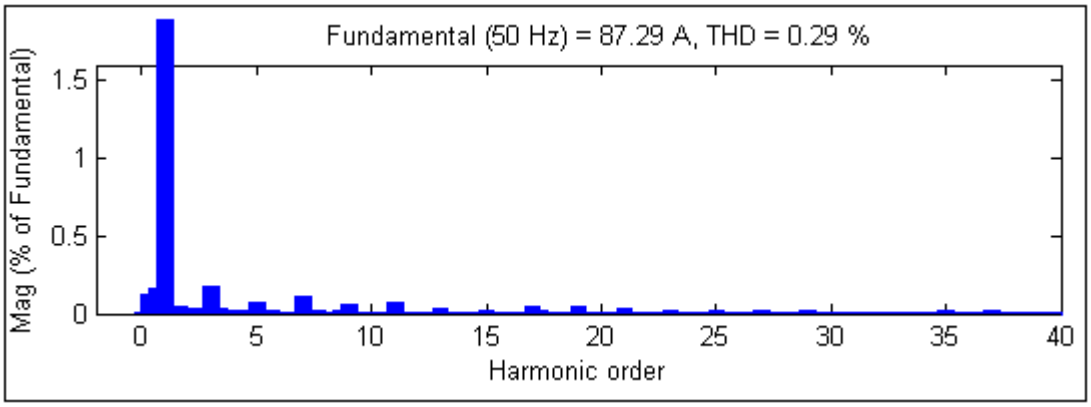


Fig 4.78: Source current with five-level SAPF using *a-b-c* theory based controller and IPD

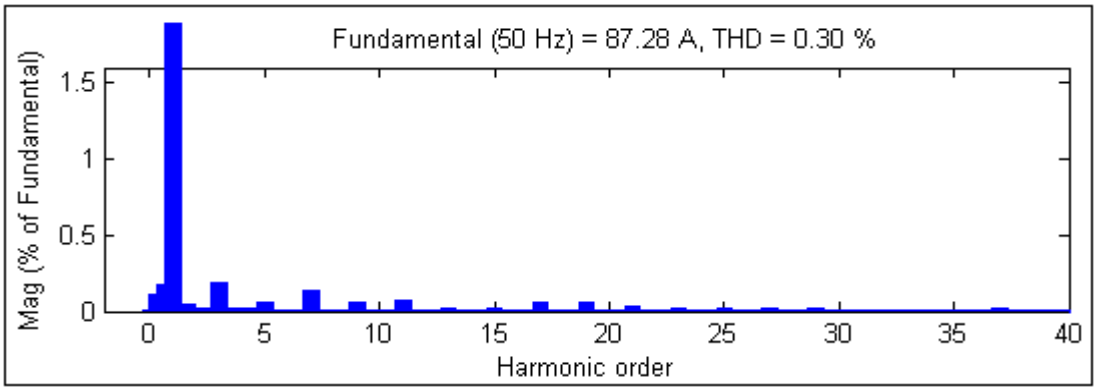
Figs. 4.79 (a) to (c) shows the harmonic spectrum and THD of source currents of phases 'a', 'b' and 'c', respectively. As observed the source current THD is successfully minimized to 0.39 %, 0.29 % and 0.30 % for the phases 'a', 'b' and 'c', respectively as compared to the result before compensation which is 27.51 %. The THDs for the first 40 harmonics calculated for all phase currents is demonstrated to be less than the prescribed value by IEEE-519 Standards.



(a) Phase 'a' source current



(b) Phase 'b' source current



(c) Phase 'c' source current

Fig 4.79: (a) to (c) Harmonic spectrum and THD of source currents with five-level SAPF using *a-b-c* theory based controller and IPD

Fig. 4.80 shows the compensating injected current into the neutral conductor by five-level four-wire SAPF using the proposed *a-b-c* theory based controller and IPD modulation technique in order to minimize the source neutral current to zero between the interval 0.08 s and 0.22 s.

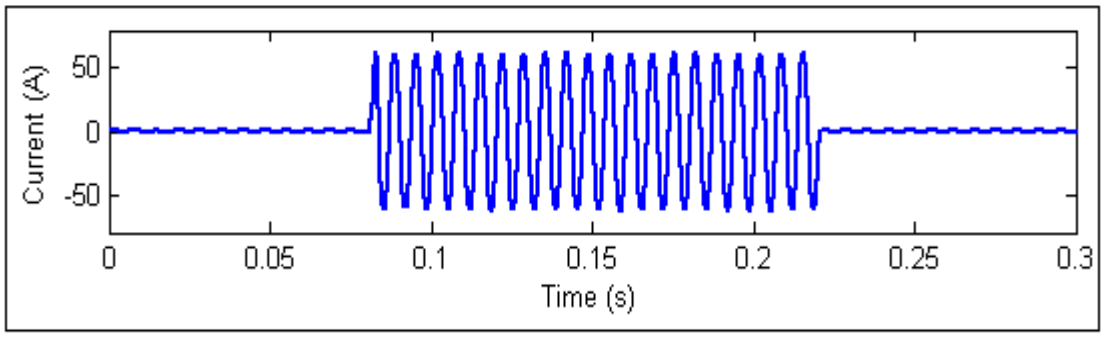


Fig 4.80: Current injected into the neutral conductor by five-level SAPF using *a-b-c* theory based controller and IPD

It is found that the five-level four-wire SAPF using the proposed *a-b-c* theory based controller and IPD modulation technique is able to minimize the source neutral current to nearly zero when it is connected during the interval 0.08 s to 0.22 s as shown in Fig. 4.81.

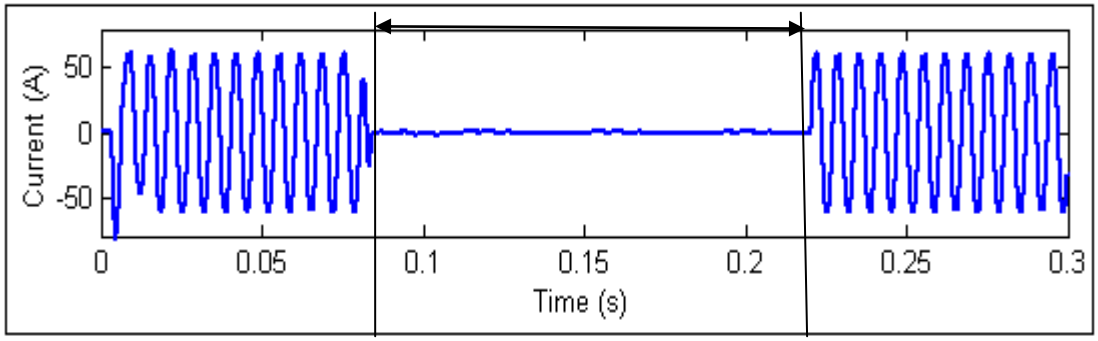


Fig 4.81: Simulated source neutral current with five-level SAPF using *a-b-c* theory based controller and IPD

Fig. 4.82 shows phase 'a' source voltage and source current, where the current is non-sinusoidal except during the interval between 0.08 s and 0.22 s when the SAPF has come into operation. During the interval between 0.08 s and 0.22 s the source current is sinusoidal and is in-phase with the source voltage. Thus, it can be concluded that the developed five-level four-wire SAPF using the proposed *a-b-c* theory based controller and IPD modulation technique has successfully compensated the harmonic load currents and improved the supply power factor to nearly unity. Similar results are obtained for the phases 'b' and 'c' also.

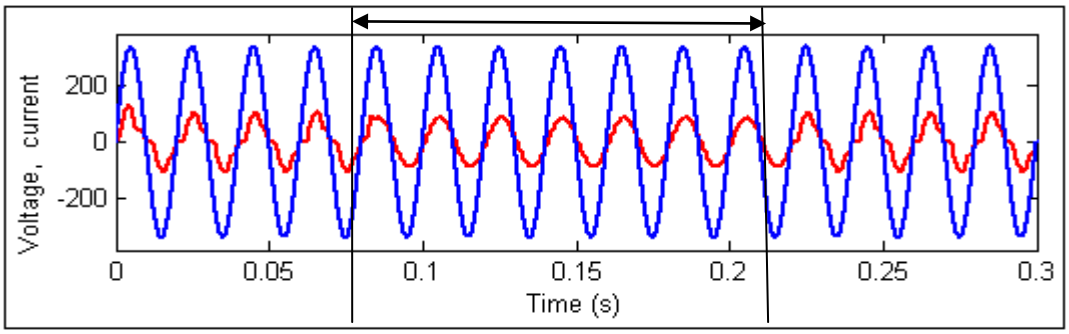


Fig 4.82: Source voltage and source current with five-level SAPF using *a-b-c* theory based controller and IPD

Fig. 4.83 shows the active and reactive powers after compensation by a five-level four-wire SAPF using proposed *a-b-c* theory based controller and IPD modulation technique. The reactive power before compensation which is equal 14.59 kvar is successfully compensated to a very low value. Consequently the power factor at the source end is improved to 0.988 as shown in Fig. 4.84.

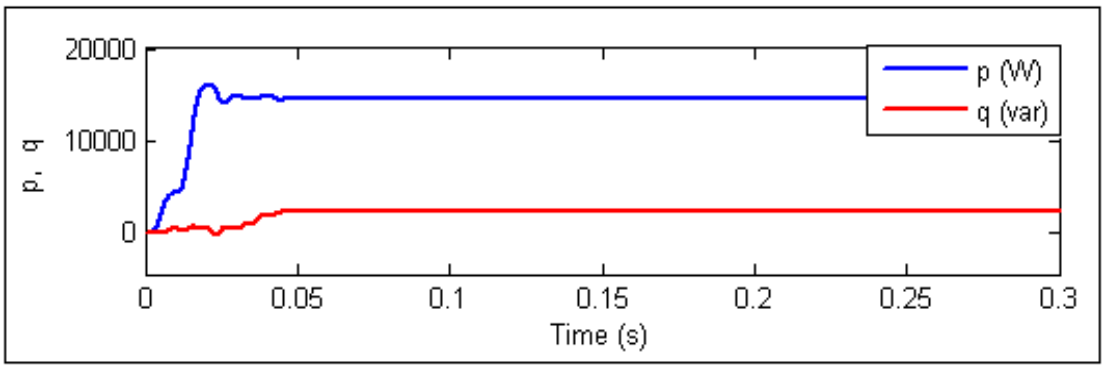


Fig 4.83: Active and reactive powers with five-level SAPF using *a-b-c* theory based controller and IPD

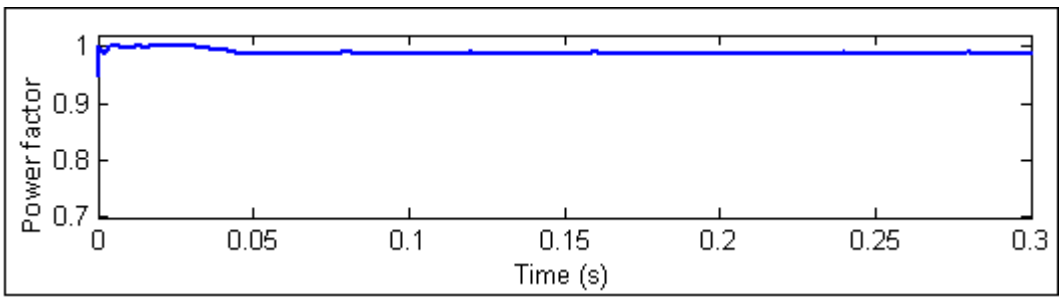


Fig 4.84: Power factor at source end with five-level SAPF using *a-b-c* theory based controller and IPD

To compare the performance of five-level four-wire SAPF by the proposed three types of controllers and IPD modulation technique, the THDs of source currents are presented in Table 4.9. It can be observed that in all the three cases the THD is less than the prescribed limit of 5 % as recommended by IEEE-519 standards. However, the THD obtained by the proposed *a-b-c* theory based controller is far less than by the other two controllers as illustrated in Table 4.9.

Table 4.9: Source currents THD with five-level SAPF using IPD

Controller	THD *p-q* theory	THD *d-q-0* theory	THD *a-b-c* theory
Phase 'a'	2.22	1.67	0.39
Phase 'b'	2.20	1.66	0.29
Phase 'c'	2.19	1.66	0.30

Simulation results of compensated source neutral currents by five-level four-wire SAPF using the three types of proposed controllers and IPD modulation technique are given in Table. 4.10. As observed these currents are far less than the value of 64.17 A before compensation. However the controller based on *d-q-0* theory reduced the source neutral conductor current to a very small value of 0.60 A as shown in Table. 4.10.

Table 4.10: Source neutral current with five-level SAPF using IPD

Controller type	*p-q* theory	*d-q-0* theory	*a-b-c* theory
Peak neutral current (A)	0.90	0.60	1.21

Simulation results for power factor at the source end with five-level four-wire SAPF using the three different proposed controllers and IPD modulation technique is given as in Table 4.11. It can be observed that the power factor is greatly improved as compared to the value before compensation which is 0.8056. However the controller based on *p-q* theory improved the source end power factor to unity as shown in Table 4.11which makes the source current sinusoidal.

Table 4.11: Power factor at source end with five-level SAPF using IPD

Controller type	*p-q* theory	*d-q-0* theory	*a-b-c* theory
Supply Power factor	1.0	0.986	0.988

To observe the effect of switching in operation of the five-level SAPF, the recorded peak transient current at source is presented in Table 4.12. It is observed that *d-q-0* theory based controller with IPD modulation technique gives less peak current as compared to the other two controllers as shown in Table 4.12.

Table 4.12: Transient current with five-level SAPF using IPD

Controller type	*p-q* theory	*d-q-0* theory	*a-b-c* theory
Peak transient current	94.49 A	83.64 A	84.69 A

4.4.2.4 Simulation results with five-level SAPF using p-q theory based controller and APOD

The proposed controller based on *p-q* theory and APOD modulation technique is presented as in Figs. 3.4 and 3.15. The five-level SAPF which has four wires generates the distorted injecting current in leg 'a' as shown in Fig. 4.85 by using the proposed *p-q* theory based controller and APOD modulation technique in order to compensate the distorted current shown in Fig. 4.3. Similar currents but with 120^{o} phase shift are injected by legs 'b' and 'c' of the SAPF into phases 'b' and 'c' of the distribution system. The injecting current reaches a peak value of 49.31 A as shown in Fig. 4.85.

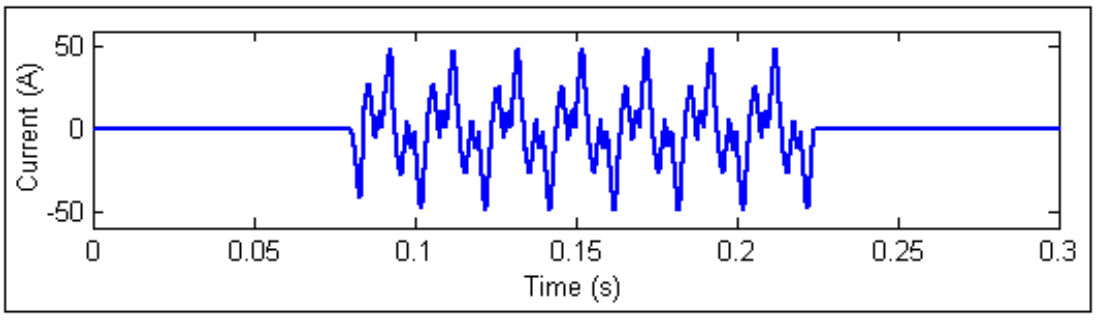


Fig 4.85: Current injected by five-level SAPF using *p-q* theory based controller and APOD

Fig. 4.86 shows phase ‘a’ source current with and without SAPF. It is found that the five-level four-wire SAPF using the proposed *p-q* theory based controller and APOD modulation technique is able to compensate the source current when it is connected during the interval 0.08 s to 0.22 s. The resultant sinusoidal source current between 0.08 s and 0.22 s reaches a peak value of 84.44 A which is less than the uncompensated peak current of 105.2 A. Similar simulation result and measured value is obtained for the phases ‘b’ and ‘c’.

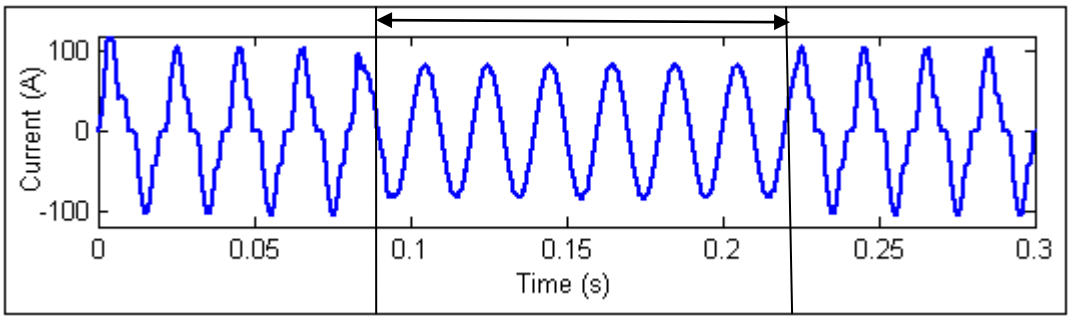
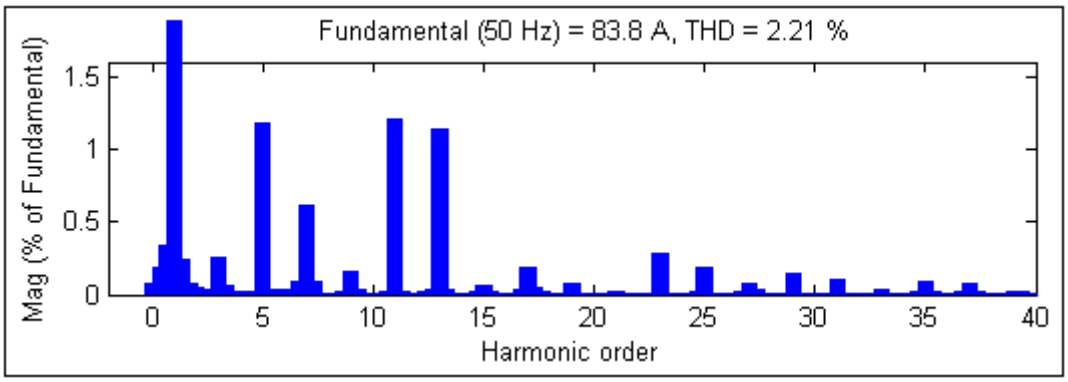
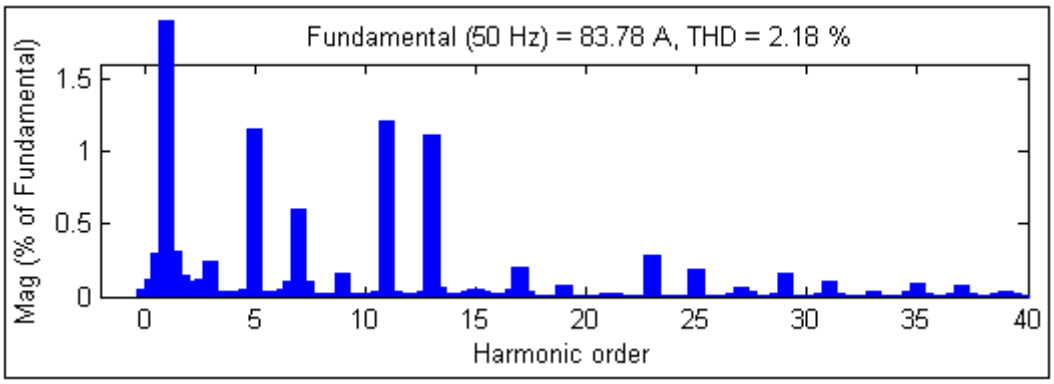


Fig 4.86: Source current with five-level SAPF using *p-q* theory based controller and APOD

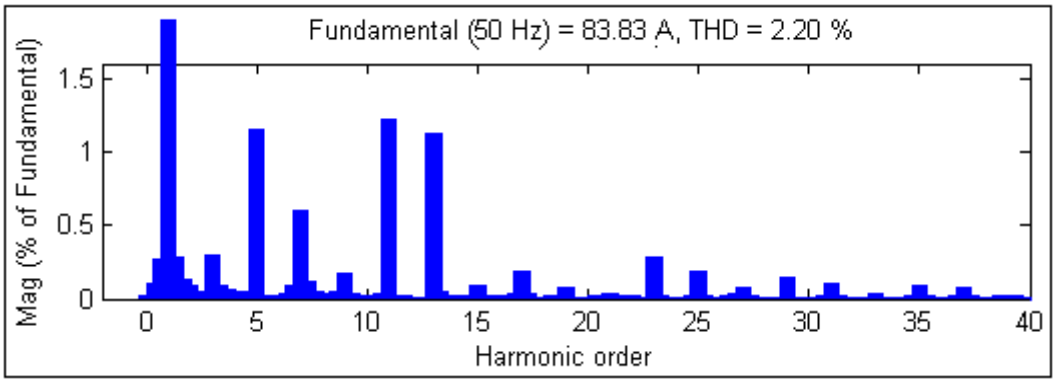
Figs. 4.87 (a) to (c) shows the harmonic spectrum and THD of source currents of phases ‘a’, ‘b’ and ‘c’, respectively. As observed the source current THD is successfully minimized to around 2.20 % as compared to the result before compensation which is 27.51 %. The THDs for the first 40 harmonics calculated for all phase currents is demonstrated to be less than the prescribed value by IEEE-519 Standards.



(a) Phase ‘a’ source current



(b) Phase 'b' source current



(c) Phase 'c' source current

Fig 4.87: (a) to (c) Harmonic spectrum and THD of source currents with five-level SAPF using *p-q* theory based controller and APOD

Fig. 4.88 shows the compensating injected current into the neutral conductor by five-level four-wire SAPF using the proposed *p-q* theory based controller and APOD modulation technique in order to minimize the source neutral current to zero between the interval 0.08 s and 0.22 s.

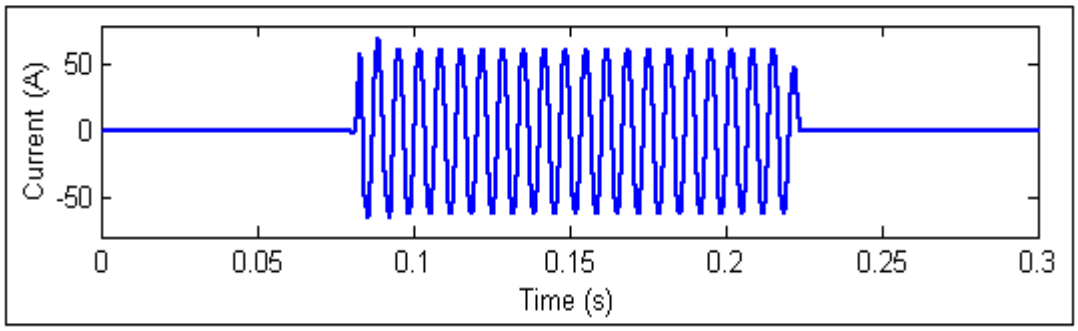


Fig 4.88: Current injected into the neutral conductor by five-level SAPF using *p-q* theory based controller and APOD

It is found that the five-level four-wire SAPF using the proposed *p-q* theory based controller and APOD modulation technique is able to minimize the source neutral current to nearly zero when it is connected during the interval 0.08 s to 0.22 s as shown in Fig. 4.89.

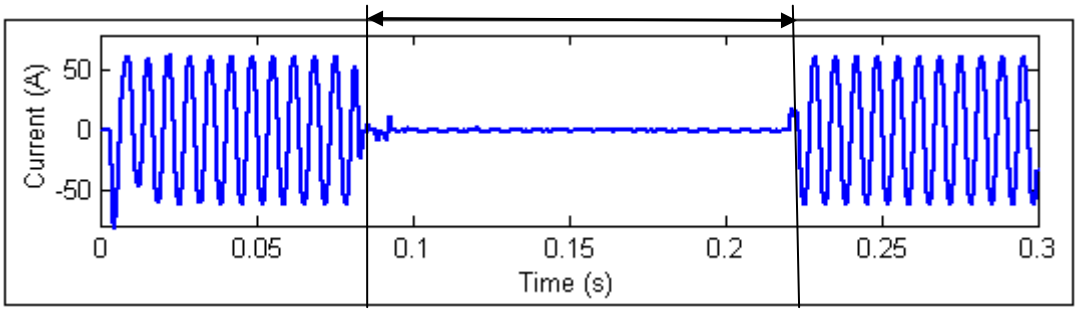


Fig 4.89: Simulated source neutral current with five-level SAPF using *p-q* theory based controller and APOD

Fig. 4.90 shows phase 'a' source voltage and source current, where the current is non-sinusoidal except during the interval between 0.08 s and 0.22 s when the SAPF has come into operation. During the interval between 0.08 s and 0.22 s the source current is sinusoidal and is in phase with the source voltage. Thus, it can be concluded that the developed five-level four-wire SAPF using the proposed *p-q* theory based controller and APOD modulation technique has successfully compensated the harmonic load currents and improved the supply power factor to nearly unity. Similar results are obtained for the phases 'b' and 'c' also.

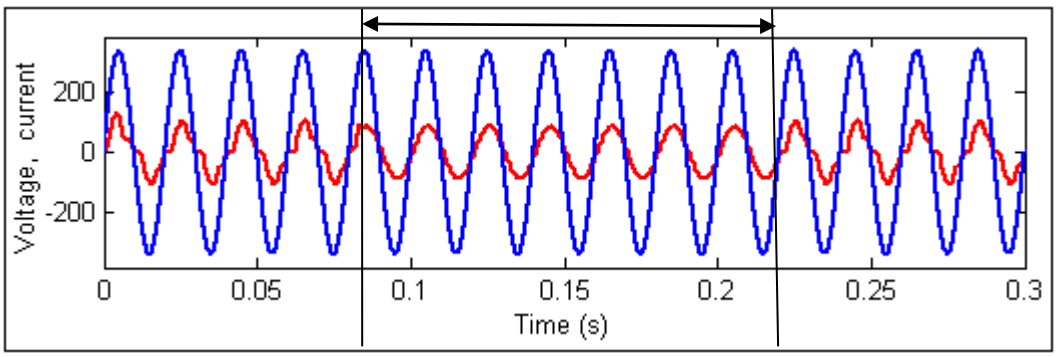


Fig 4.90: Source voltage and source current with five-level SAPF using *p-q* theory based controller and APOD

Fig. 4.91 shows the active and reactive powers after compensation by a five-level four-wire SAPF using the proposed *p-q* theory based controller and APOD modulation technique. The reactive power before compensation which is equal 14.59 kvar is successfully compensated to a very low value. Consequently the power factor at the source end is improved to unity as shown in Fig. 4.92.

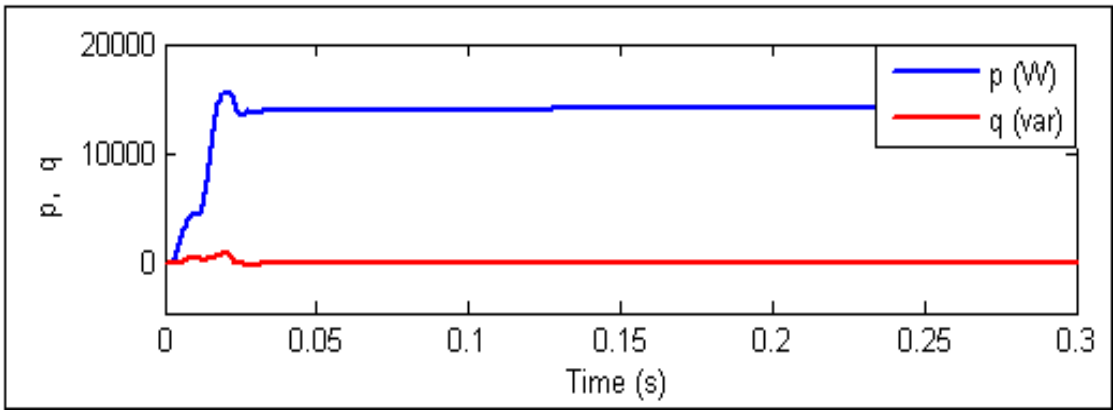


Fig 4.91: Active and reactive powers with five-level SAPF using *p-q* theory based controller and APOD

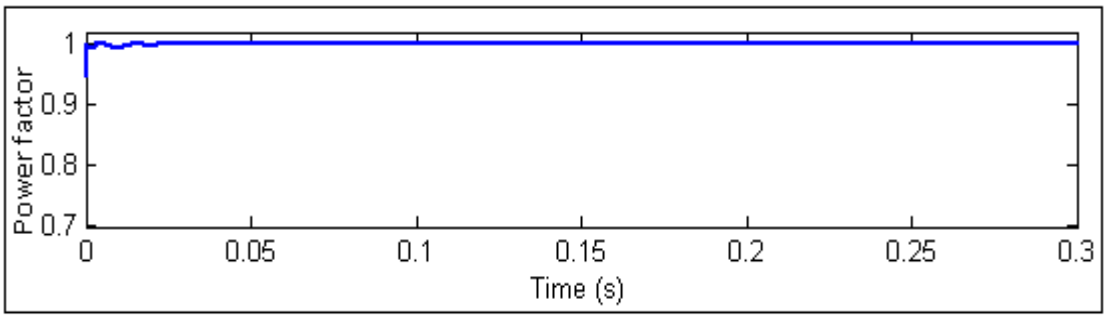


Fig 4.92: Power factor at source end with five-level SAPF using *p-q* theory based controller and APOD

4.4.2.5 Simulation results with five-level SAPF using d-q-0 theory based controller and APOD

The proposed controller based on *d-q-0* theory and APOD modulation technique is presented as in Figs. 3.6 and 3.15. The five-level SAPF which has four wires generates the distorted injecting current in leg 'a' as shown in Fig. 4.93 by using the proposed *d-q-0* theory based controller and APOD modulation technique in order to

compensate the distorted current shown in Fig. 4.3. Similar currents but with 120^{o} phase shift are injected by legs ‘b’ and ‘c’ of the SAPF into phases ‘b’ and ‘c’ of the distribution system. The injecting current reaches a peak value of 32.80 A as shown in Fig. 4.93.

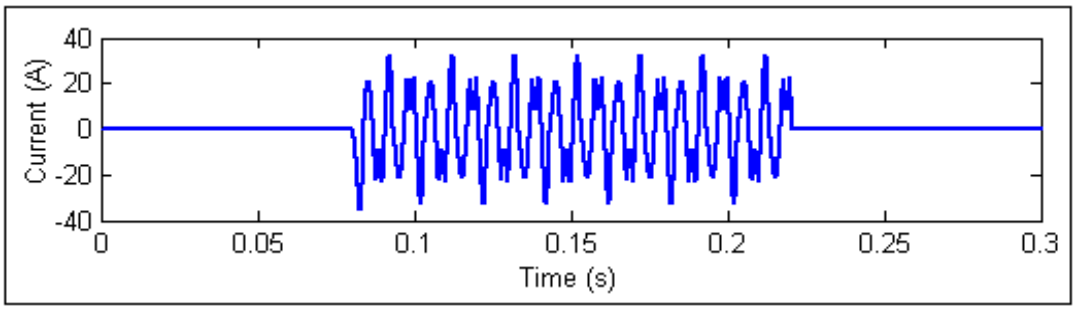


Fig 4.93: Current injected by five-level SAPF using *d-q-0* theory based controller and APOD

Fig. 4.94 shows phase ‘a’ source current with and without SAPF. It is found that the five-level four-wire SAPF using the proposed *d-q-0* theory based controller and APOD modulation technique is able to compensate the source current when it is connected during the interval 0.08 s to 0.22 s. The resultant sinusoidal source current between 0.08 s and 0.22 s reaches a peak value of 84.69 A which is less than the uncompensated peak current of 105.2 A. Similar simulation result and measured value is obtained for the phases ‘b’ and ‘c’.

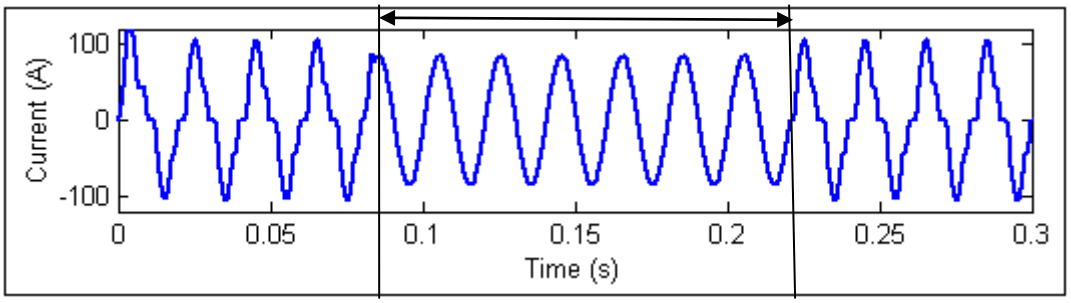
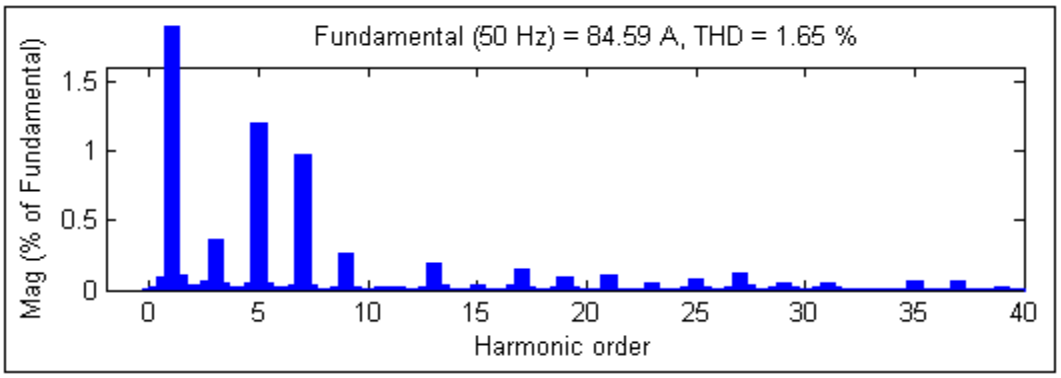


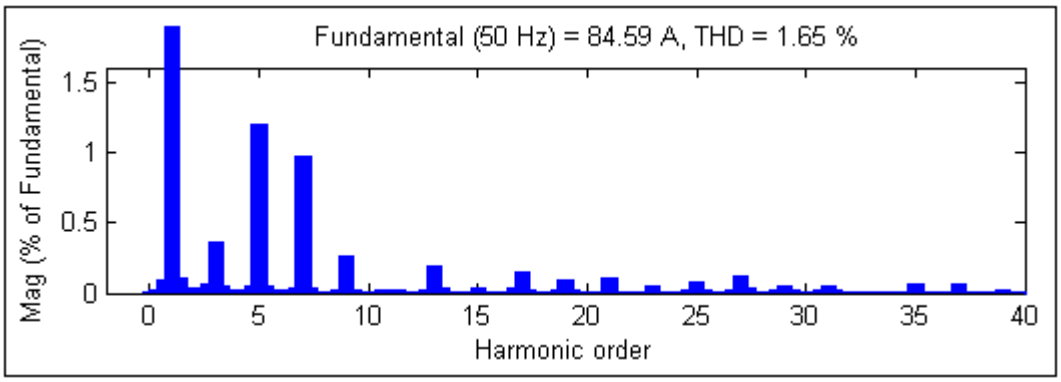
Fig 4.94: Source current with five-level SAPF using *d-q-0* theory based controller and APOD

Figs. 4.95 (a) to (c) shows the harmonic spectrum and THD of source currents of phases ‘a’, ‘b’ and ‘c’, respectively. As observed the source current THD is

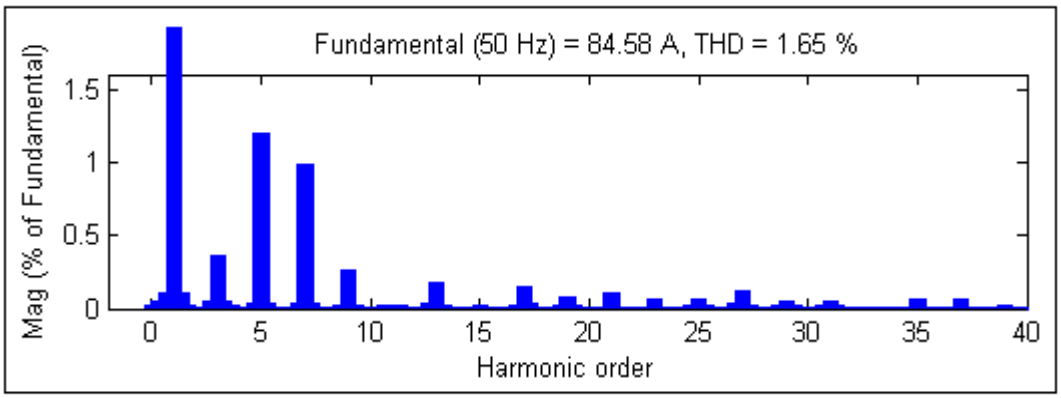
successfully minimized to around 1.65 % as compared to the result before compensation which is 27.51 %. The THDs for the first 40 harmonics calculated for all phase currents is demonstrated to be less than the prescribed value by IEEE-519 Standards.



(a) Phase 'a' source current



(b) Phase 'b' source current



(c) Phase 'c' source current

Fig 4.95: (a) to (c) Harmonic spectrum and THD of source currents with five-level SAPF using *d-q-0* theory based controller and APOD

Fig. 96 shows the compensating injected current into the neutral conductor by five-level four-wire SAPF using the proposed *d-q-0* theory based controller and APOD modulation technique in order to minimize the source neutral current to zero between the interval 0.08 s and 0.22 s.

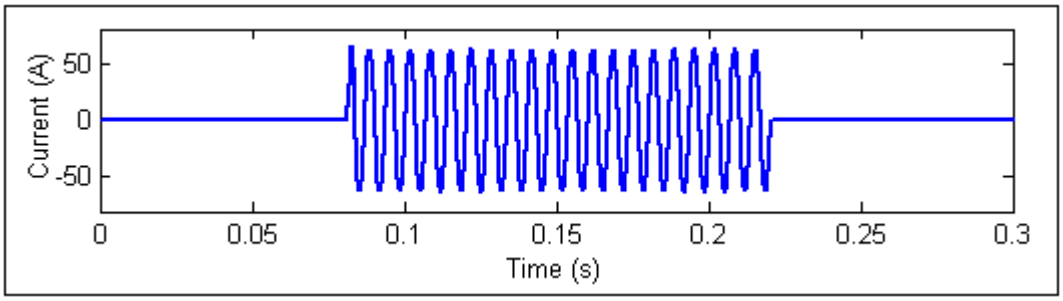


Fig 4.96: Current injected into the neutral conductor by five-level SAPF using *d-q-0* theory based controller and APOD

It is found that the five-level four-wire SAPF using the proposed *d-q-0* theory based controller and APOD modulation technique is able to minimize the source neutral current to nearly zero when it is connected during the interval 0.08 s to 0.22 s as shown in Fig. 4.97.

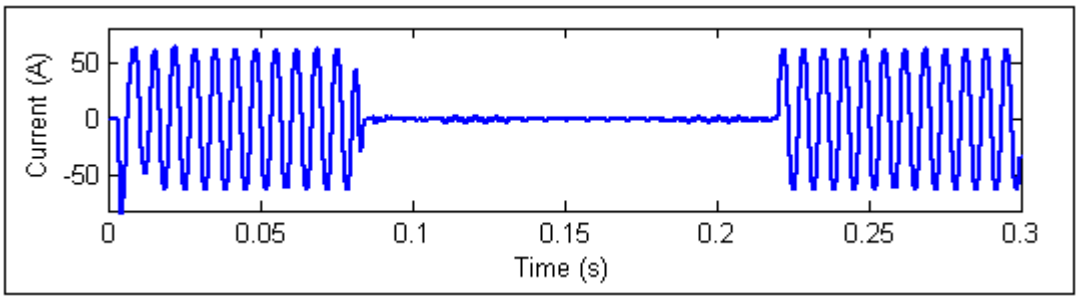


Fig 4.97: Simulated source neutral current with five-level SAPF using *d-q-0* theory based controller and APOD

Fig. 4.98 shows phase 'a' source voltage and source current, where the current is non-sinusoidal except during the interval between 0.08 s and 0.22 s when the SAPF has come into operation. During the interval between 0.08 s and 0.22 s the source current is sinusoidal and is in phase with the source voltage. Thus, it can be concluded that the developed five-level four-wire SAPF using the proposed *d-q-0* theory based controller and APOD modulation technique has successfully compensated the

harmonic load currents and improved the supply power factor to nearly unity. Similar results are obtained for the phases ‘b’ and ‘c’ also.

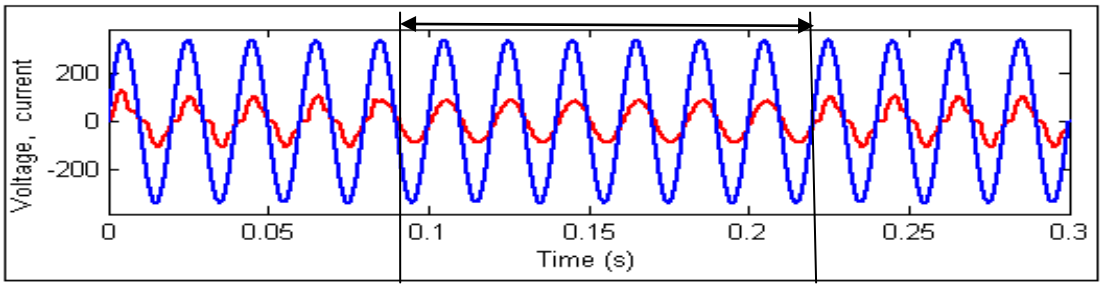


Fig 4.98: Source voltage and source current with five-level SAPF using *d-q-0* theory based controller and APOD

Fig. 4.99 shows the active and reactive powers after compensation by a five-level four-wire SAPF using proposed *d-q-0* theory based controller and APOD modulation technique. The reactive power before compensation which is equal 14.59 kvar is successfully compensated to a very low value. Consequently the power factor at the source end is improved to 0.985 as shown in Fig. 4.100.

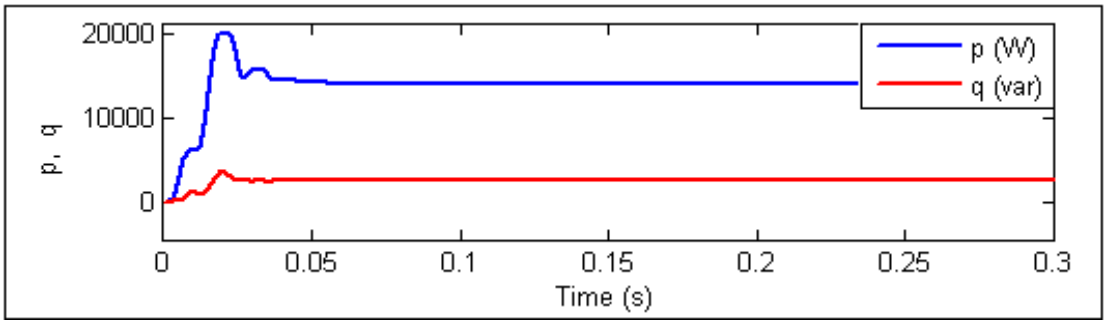


Fig 4.99: Active and reactive powers with five-level SAPF using *d-q-0* theory based controller and APOD

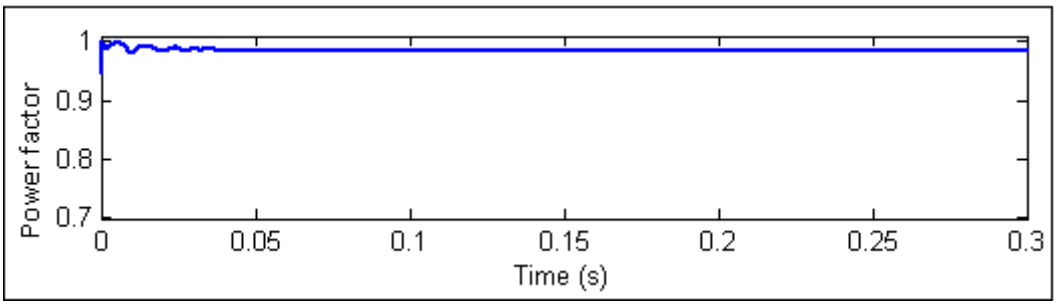


Fig 4.100: Power factor at source end with five-level SAPF using *d-q-0* theory based controller and APOD

4.4.2.6 *Simulation results with five-level SAPF using a-b-c theory based controller and APOD*

The proposed controller based on *a-b-c* theory and APOD modulation technique is presented as in Figs. 3.8 and 3.15. The five-level SAPF which has four wires generates the distorted injecting current in leg 'a' as shown in Fig. 4.101 by using the proposed *a-b-c* theory based controller and APOD modulation technique in order to compensate the distorted current shown in Fig. 4.3. Similar currents but with 120^{o} phase shift are injected by legs 'b' and 'c' of the SAPF into phases 'b' and 'c' of the distribution system. The injected current reaches a peak value of 34.80 A as shown in Fig. 4.101.

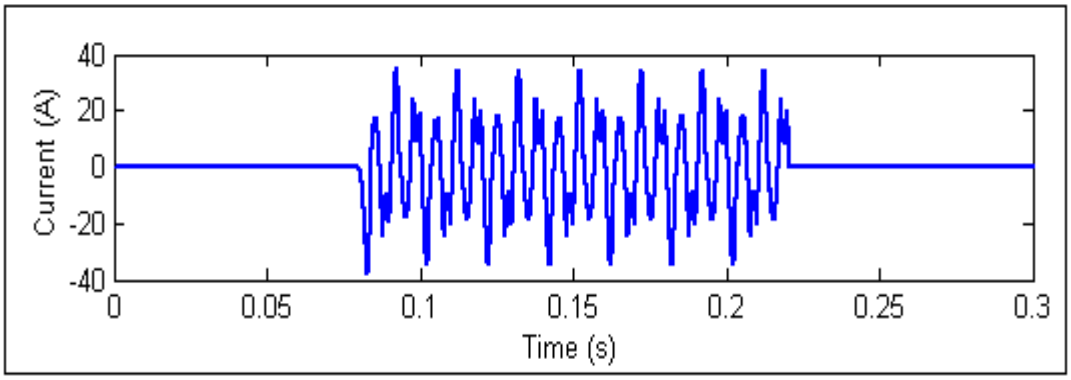


Fig 4.101: Current injected by five-level SAPF using *a-b-c* theory based controller and APOD

Fig. 4.102 shows phase 'a' source current before and after connecting the SAPF to the system. It is found that the five-level four-wire SAPF using the proposed *a-b-c* theory based controller and APOD modulation technique is able to compensate the source current when it is connected during the interval 0.08 s to 0.22 s. The resultant sinusoidal source current between 0.08 s and 0.22 s reaches a peak value of 87.46 A which is less than the uncompensated peak current of 105.2 A. Similar simulation result and measured value is obtained for the phases 'b' and 'c'.

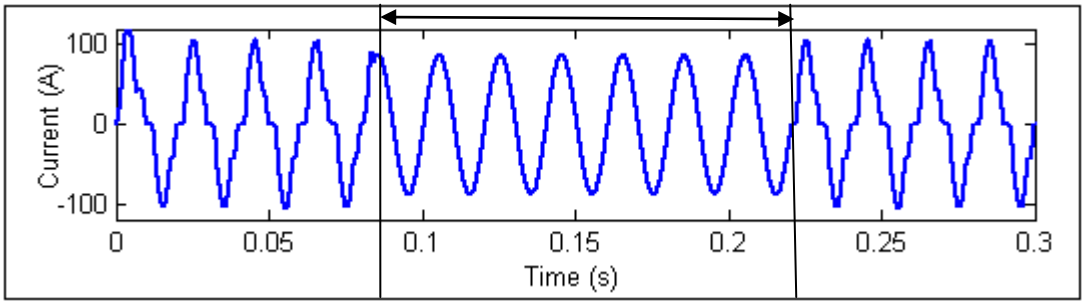
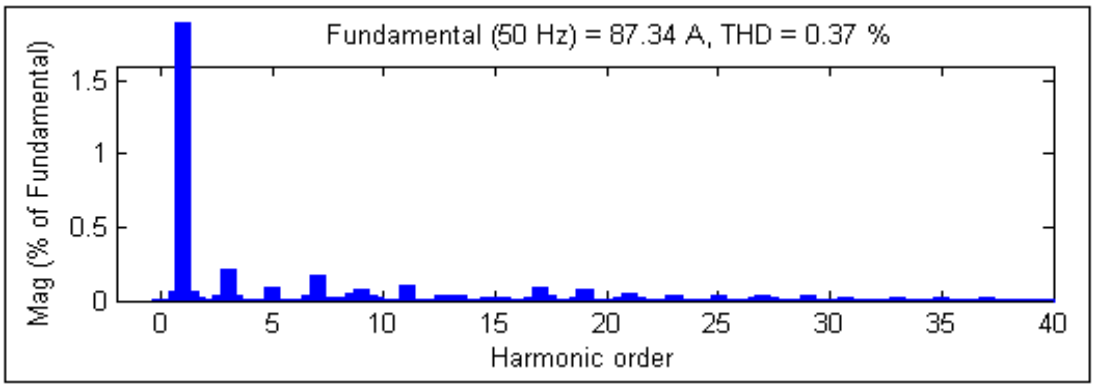
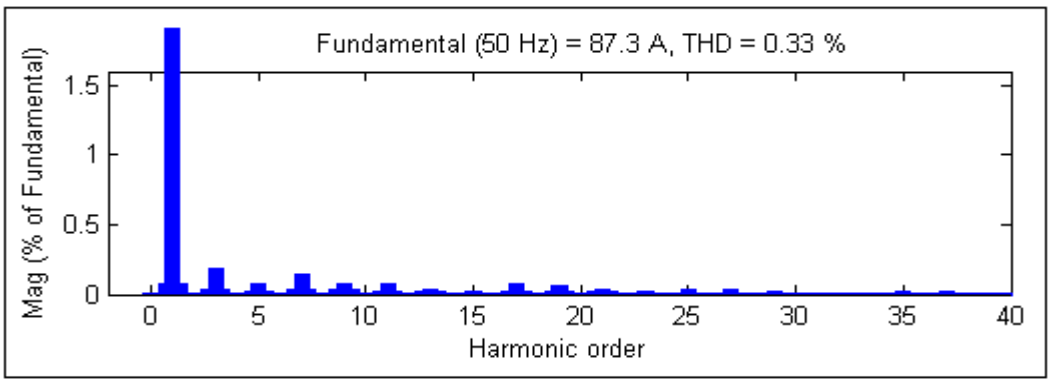


Fig 4.102: Source current with five-level SAPF using *a-b-c* theory based controller and APOD

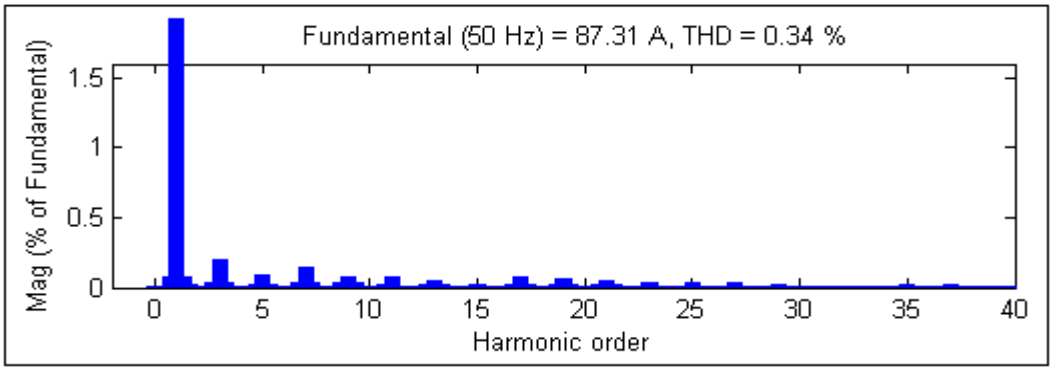
Figs. 4.103 (a) to (c) shows the harmonic spectrum and THD of source currents of phases 'a', 'b' and 'c', respectively. As observed the source current THD is successfully minimized to 0.37 %, 0.33 % and 0.34 % for the phases 'a', 'b' and 'c', respectively as compared to the result before compensation which is 27.51 %. The THDs for the first 40 harmonics calculated for all phase currents is demonstrated to be less than the prescribed value by IEEE-519 Standards.



(a) Phase 'a' source current



(b) Phase 'b' source current



(c) Phase 'c' source current

Fig 4.103: (a) to (c) Harmonic spectrum and THD of source currents with five-level SAPF using *a-b-c* theory based controller and APOD

Fig. 4.104 shows the compensating injected current into the neutral conductor by five-level four-wire SAPF using the proposed *a-b-c* theory based controller and APOD modulation technique in order to minimize the source neutral current to zero between the interval 0.08 s and 0.22 s.

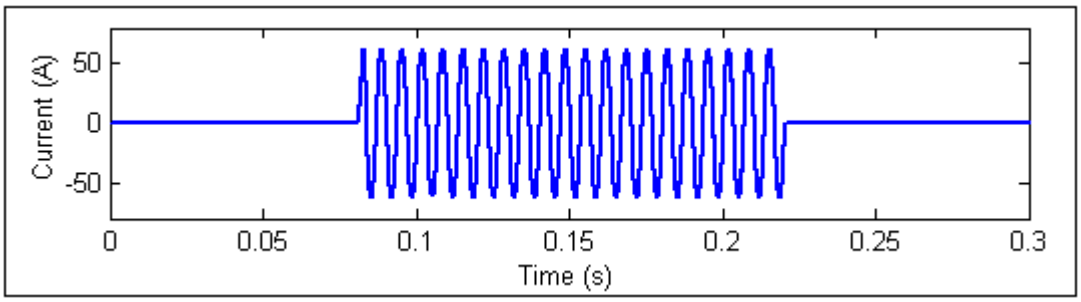


Fig 4.104: Current injected into the neutral conductor by five-level SAPF using *a-b-c* theory based controller and APOD

It is found that the five-level four-wire SAPF using the proposed *a-b-c* theory based controller and APOD modulation technique is able to minimize the source neutral current to nearly zero when it is connected during the interval 0.08 s to 0.22 s as shown in Fig. 4.105.

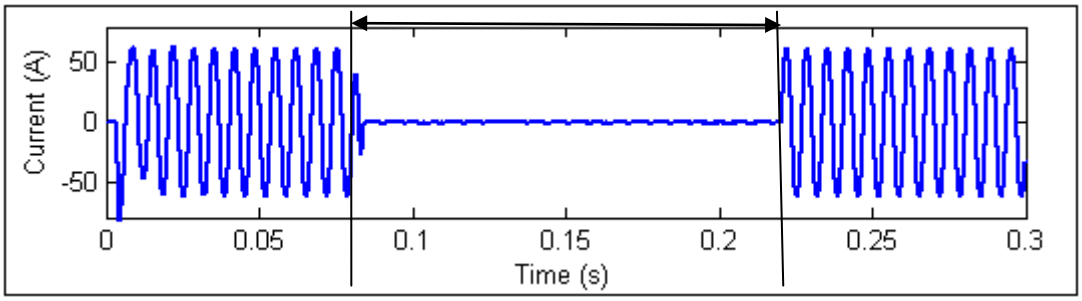


Fig 4.105: Simulated source neutral current with five-level SAPF using *a-b-c* theory based controller and APOD

Fig. 4.106 shows phase 'a' source voltage and source current, where the current is non-sinusoidal except during the interval between 0.08 s and 0.22 s when the SAPF has come into operation. During the interval between 0.08 s and 0.22 s the source current is sinusoidal and is in-phase with the source voltage. Thus, it can be concluded that the developed five-level four-wire SAPF using the proposed *a-b-c* theory based controller and APOD modulation technique has successfully compensated the harmonic load currents and improved the supply power factor to nearly unity. Similar results are obtained for the phases 'b' and 'c' also.

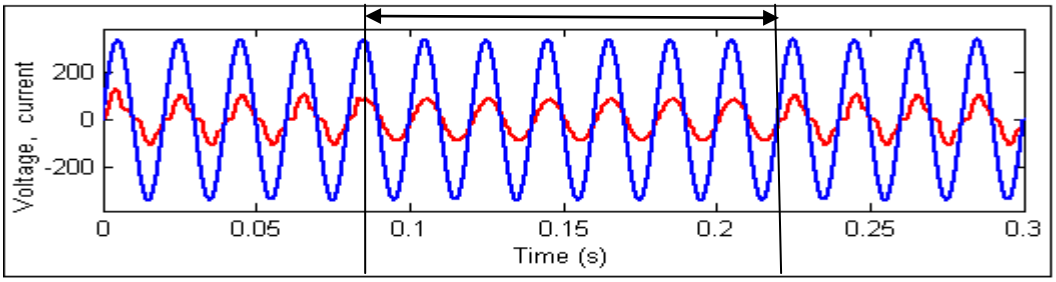


Fig 4.106: Source voltage and source current with five-level SAPF using *a-b-c* theory based controller and APOD

Fig. 4.107 shows the active and reactive powers after compensation by a five-level four-wire SAPF using proposed *a-b-c* theory based controller and APOD modulation technique. The reactive power before compensation which is equal 14.59 kvar is successfully compensated to a very low value. Consequently the power factor at the source end is improved to 0.988 which is very close to unity as shown in Fig. 4.108.

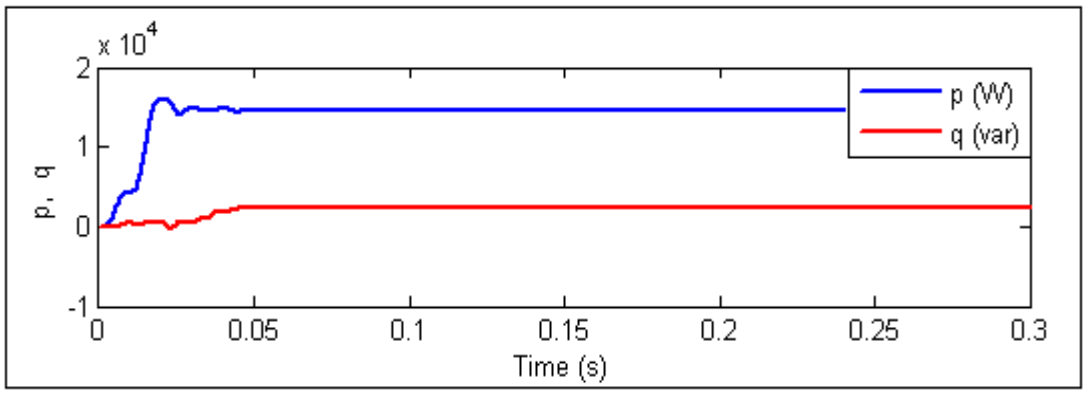


Fig 4.107: Active and reactive powers with five-level SAPF using *a-b-c* theory based controller and APOD

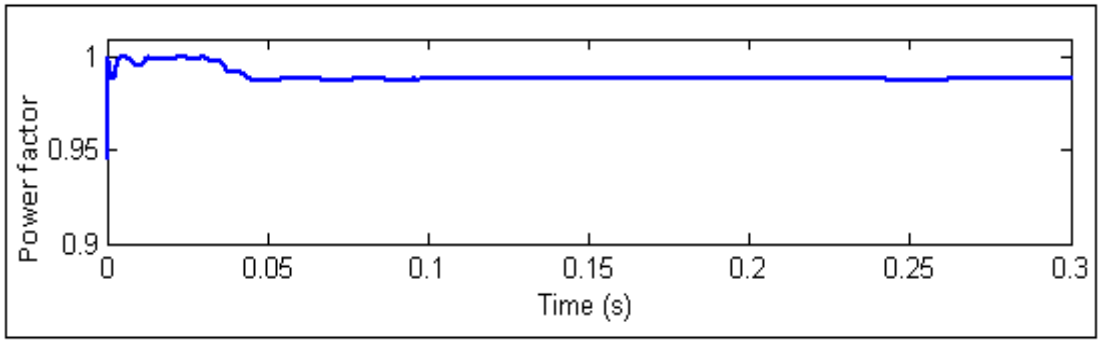


Fig 4.108: Power factor at source end with five-level SAPF using *a-b-c* theory based controller and APOD

To compare the performance of five-level four-wire SAPF by the proposed three types of controllers and APOD modulation technique, the THDs of source currents are presented in Table 4.13. It can be observed that in all the three cases the THD is less than the prescribed limit of 5 % as recommended by IEEE-519 standards. However, the THD obtained by the proposed *a-b-c* theory based controller is far less than by the other two controllers as illustrated in Table 4.13.

Table 4.13: Source currents THD with five-level SAPF using APOD

Controller	THD *p-q* theory	THD *d-q-0* theory	THD *a-b-c* theory
Phase 'a'	2.21	1.65	0.37
Phase 'b'	2.21	1.65	0.33
Phase 'c'	2.20	1.65	0.34

Simulation results of compensated source neutral currents by five-level four-wire SAPF using the three types of proposed controllers and APOD modulation technique are given in Table. 4.14. As observed these currents are far less than the value of 64.17 A before compensation. However the controller based on *d-q-0* theory reduced the source neutral conductor current to a very small value of 0.63 A as shown in Table. 4.14.

Table 4.14: Source neutral current with five-level SAPF using APOD

Controller type	*p-q* theory	*d-q-0* theory	*a-b-c* theory
Peak neutral current	0.92 A	0.63 A	1.13 A

Simulation results for power factor at the source end with five-level four-wire SAPF using the three different proposed controllers is given as in Table 4.15. It can be observed that the power factor is greatly improved as compared to the value before compensation which is 0.8056. However the controller based on *p-q* theory improved the source end power factor to unity as shown in Table 4.15 which makes the source current sinusoidal.

Table 4.15: Power factor at source end with five-level SAPF using APOD

Controller type	*p-q* theory	*d-q-0* theory	*a-b-c* theory
Supply Power factor	1.0	0.985	0.988

To observe the effect of switching in operation of the five-level SAPF, the recorded peak transient current at source is presented in Table 4.16. It is observed that *d-q-0* theory based controller with APOD modulation technique gives less peak current as compared to the other two controllers as shown in Table 4.16.

Table 4.16: Transient current with five-level SAPF using APOD

Controller type	*p-q* theory	*d-q-0* theory	*a-b-c* theory
Peak transient current	90.37 A	82.99 A	87.62 A

4.4.2.7 Simulation results with five-level SAPF using p-q theory based controller and POD

The proposed controller based on *p-q* theory and POD modulation technique is presented as in Figs. 3.4 and 3.17 of Chapter 3. The five-level SAPF which has four wires generates the distorted injecting current in leg 'a' as shown in Fig. 4.109 by using the proposed *p-q* theory based controller and POD modulation technique in order to compensate the distorted current shown in Fig. 4.3. Similar currents but with 120^{o} phase shift are injected by legs 'b' and 'c' of the SAPF into phases 'b' and 'c' of the distribution system. The injected current reaches a peak value of 49.35 A as shown in Fig. 4.109.

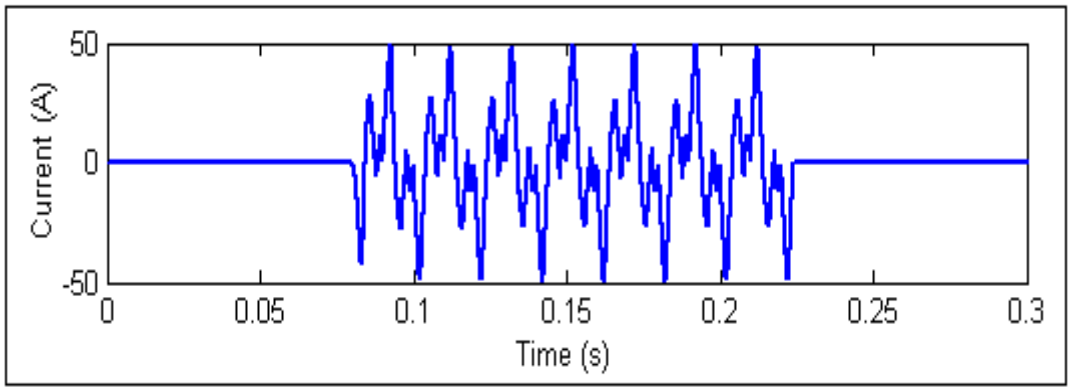


Fig 4.109: Current injected by five-level four-wire SAPF using *p-q* theory based controller and POD

Fig. 4.110 shows phase 'a' source current with and without SAPF. It is found that the five-level four-wire SAPF using the proposed *p-q* theory based controller and POD modulation technique is able to compensate the source current when it is connected during the interval 0.08 s to 0.22 s. The resultant sinusoidal source current between 0.08 s and 0.22 s reaches a peak value of 84.50 A which is less than the uncompensated peak current of 105.2 A. Similar simulation result and measured value is obtained for the phases 'b' and 'c'.

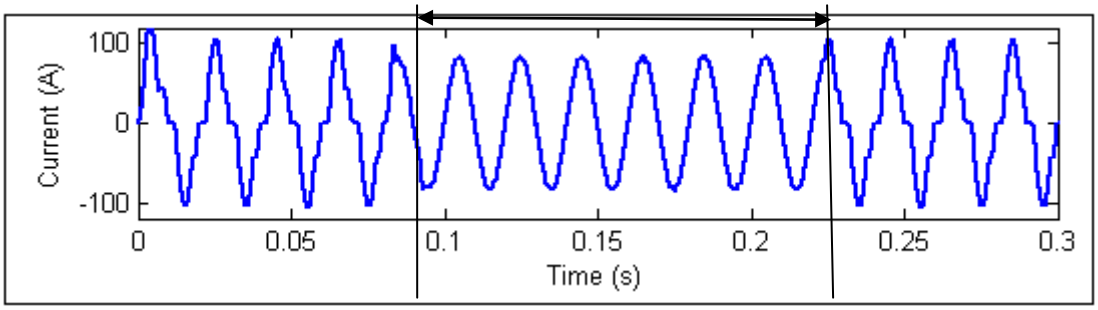
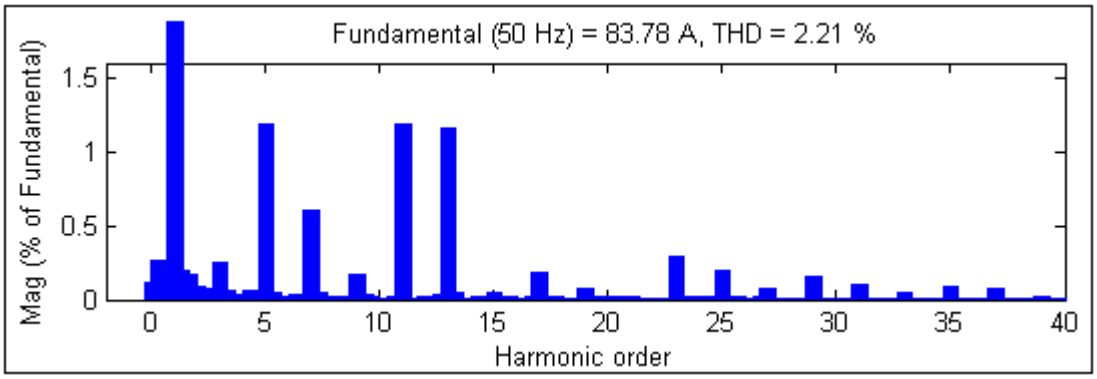
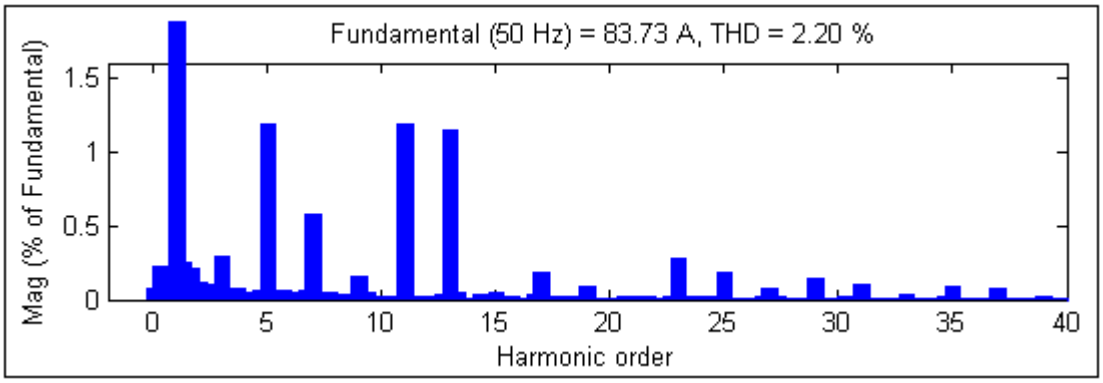


Fig 4.110: Source current with five-level SAPF using *p-q* theory based controller and POD

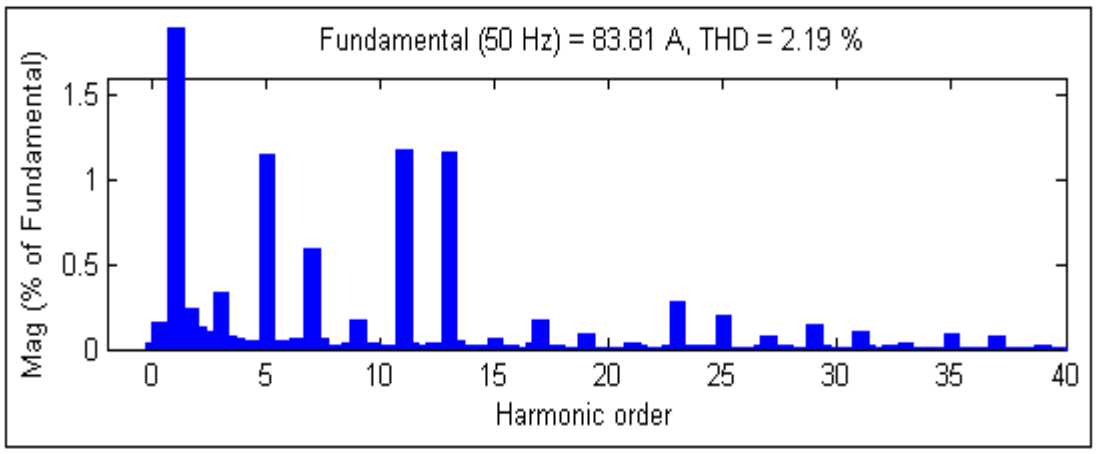
Figs. 4.111 (a) to (c) shows the harmonic spectrum and THD of source currents of phases 'a', 'b' and 'c', respectively. As observed the source current THD is successfully minimized to around 2.20 % as compared to the result before compensation which is 27.51 %. The THDs for the first 40 harmonics calculated for all phase currents is demonstrated to be less than the prescribed value by IEEE-519 Standards.



(a) Phase 'a' source current



(b) Phase 'b' source current



(c) Phase 'c' source current

Fig 4.111: (a) to (c) Harmonic spectrum and THD of source currents with five-level SAPF using *p-q* theory based controller and POD

Fig. 4.112 shows the compensating injected current into the neutral conductor by five-level four-wire SAPF using the proposed *p-q* theory based controller and POD modulation technique in order to minimize the source neutral current to zero between the interval 0.08 s and 0.22 s.

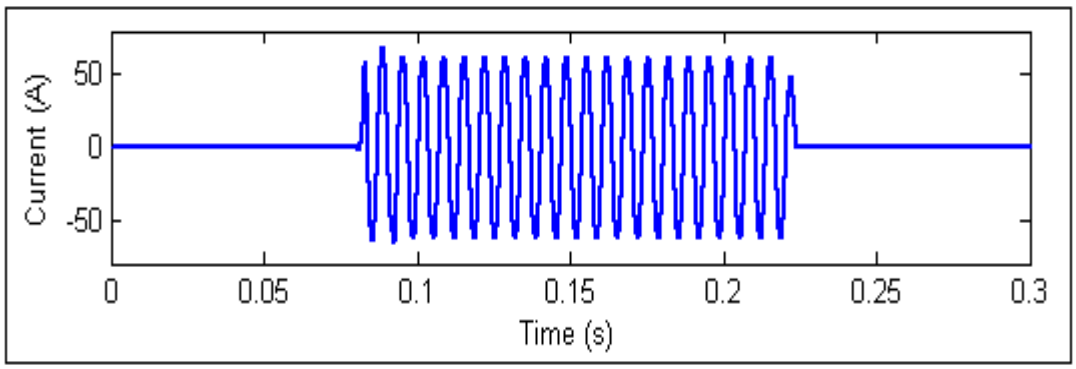


Fig 4.112: Current injected into the neutral conductor by five-level SAPF using *p-q* theory based controller and POD

It is found that the five-level four-wire SAPF using the proposed *p-q* theory based controller and POD modulation technique is able to minimize the source neutral current to nearly zero when it is connected during the interval 0.08 s to 0.22 s as shown in Fig. 4.113.

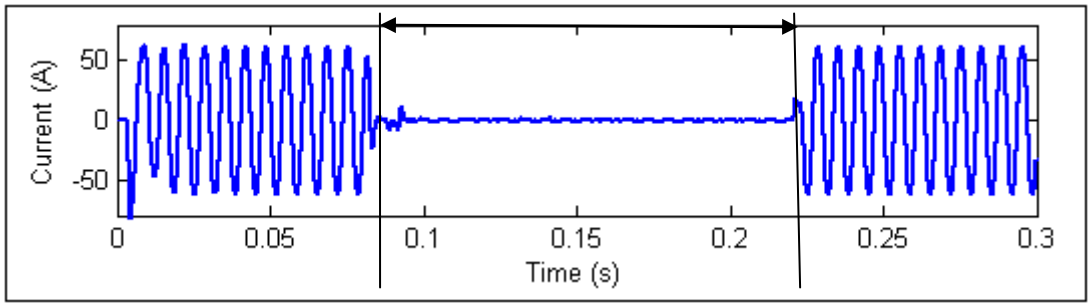


Fig 4.113: Simulated source neutral current with five-level SAPF using *p-q* theory based controller and POD

Fig. 4.114 shows phase 'a' source voltage and source current, where the current is non-sinusoidal except during the interval between 0.08 s and 0.22 s when the SAPF has come into operation. During the interval between 0.08 s and 0.22 s the source current is sinusoidal and is in phase with the source voltage. Thus, it can be concluded that the developed five-level four-wire SAPF using the proposed *p-q* theory based controller and POD modulation technique has successfully compensated the harmonic load currents and improved the supply power factor to nearly unity. Similar results are obtained for the phases 'b' and 'c' also.

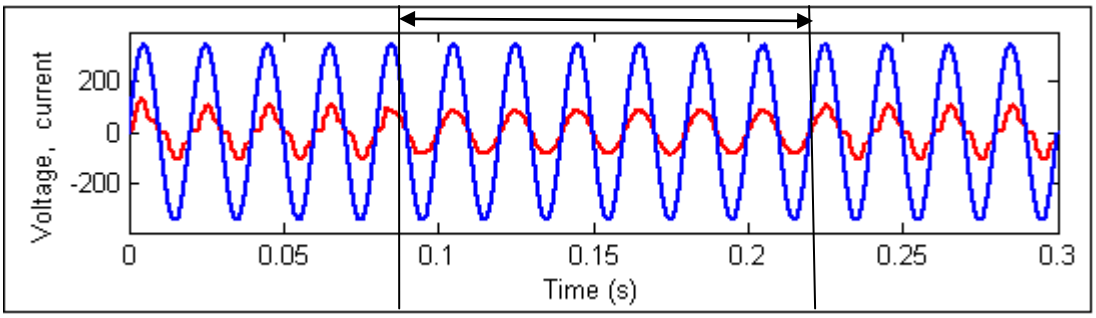


Fig 4.114: Source voltage and source current with five-level SAPF using *p-q* theory based controller and POD

Fig. 4.115 shows the active and reactive powers after compensation by a five-level four-wire SAPF using the proposed *p-q* theory based controller and POD modulation technique. The reactive power before compensation which is equal 14.59 kvar is successfully compensated to a very low value. Consequently the power factor at the source end is improved to unity which is very close to unity as shown in Fig. 4.116.

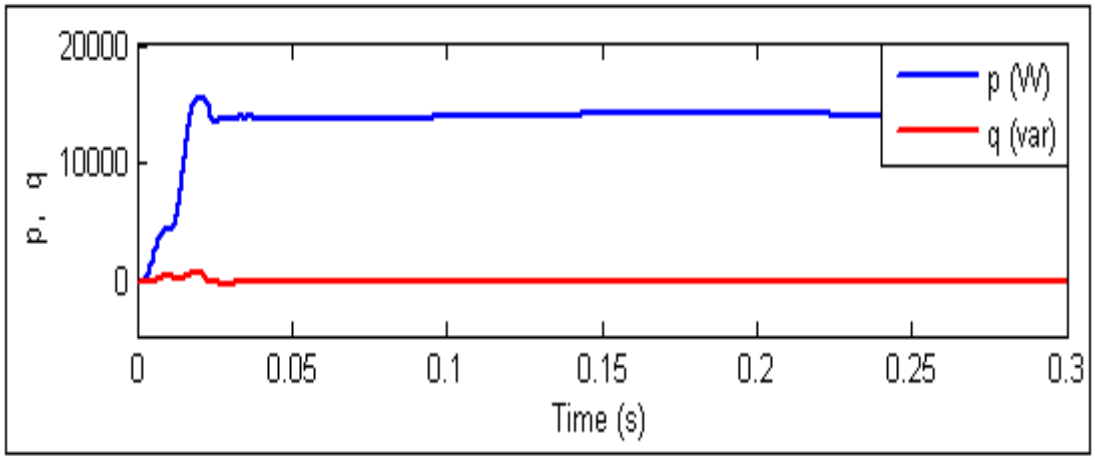


Fig 4.115: Active and reactive powers with five-level SAPF using *p-q* theory based controller and POD

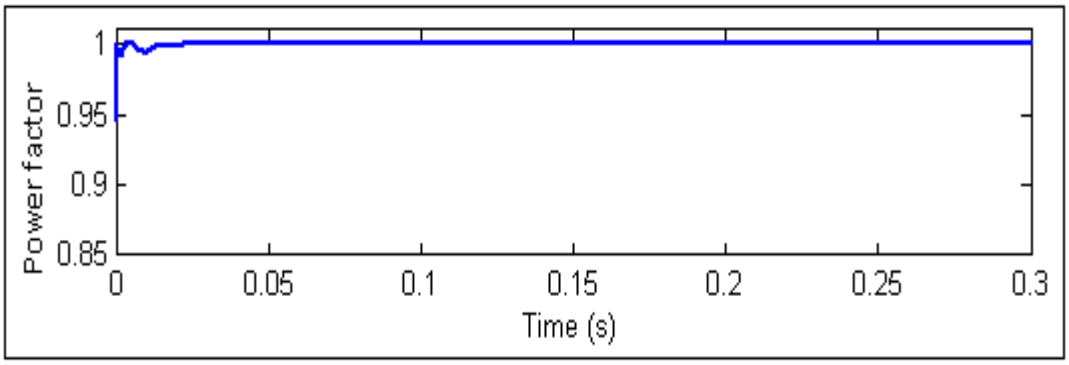


Fig 4.116: Power factor at source end with five-level SAPF using *p-q* theory based controller and POD

4.4.2.8 Simulation results with five-level SAPF using d-q-0 theory based controller and POD

The proposed controller based on *d-q-0* theory and POD modulation technique is presented as in Figs. 3.6 and 3.17. The five-level SAPF which has four wires generates the distorted injecting current in leg 'a' as shown in Fig. 4.117 by using the proposed *d-q-0* theory based controller and POD modulation technique in order to compensate the distorted current shown in Fig. 4.3. Similar currents but with 120^{o} phase shift are injected by legs 'b' and 'c' of the SAPF into phases 'b' and 'c' of the distribution system. The injecting current reaches a peak value of 32.71 A as shown in Fig. 4.117.

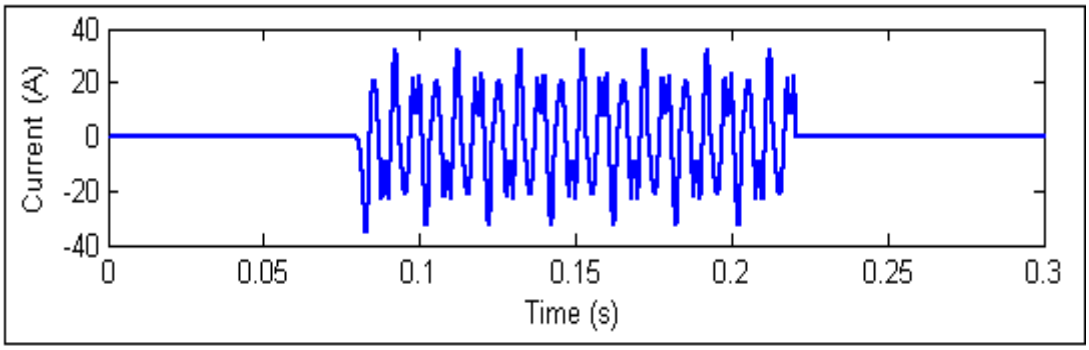


Fig 4.117: Current injected by five-level SAPF using *d-q-0* theory based controller and POD

Fig. 4.118 shows phase 'a' source current with and without SAPF. It is found that the five-level four-wire SAPF using the proposed *d-q-0* theory based controller and POD modulation technique is able to compensate the source current when it is connected during the interval 0.08 s to 0.22 s. The resultant sinusoidal source current between 0.08 s and 0.22 s reaches a peak value of 84.24 A which is less than the uncompensated peak current of 105.2 A. Similar simulation result and measured value is obtained for the phases 'b' and 'c'.

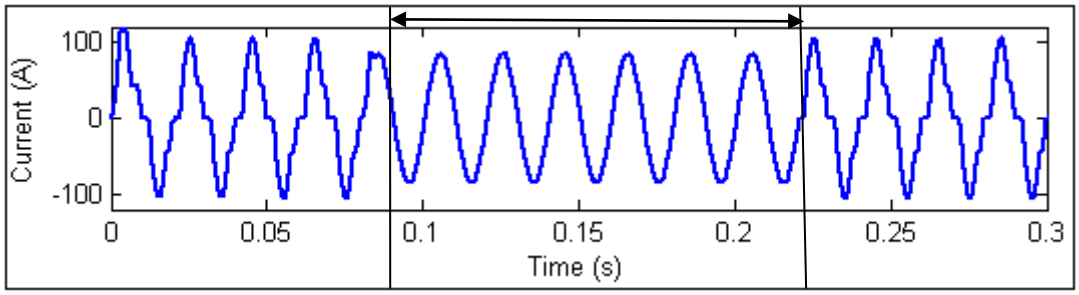
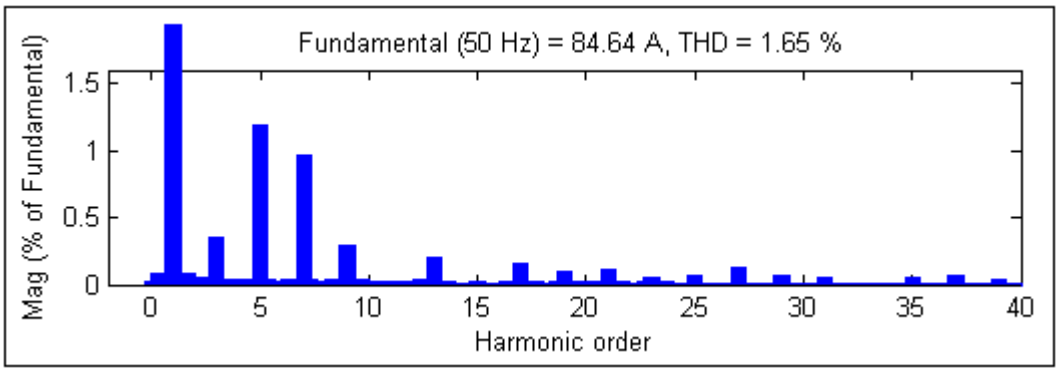
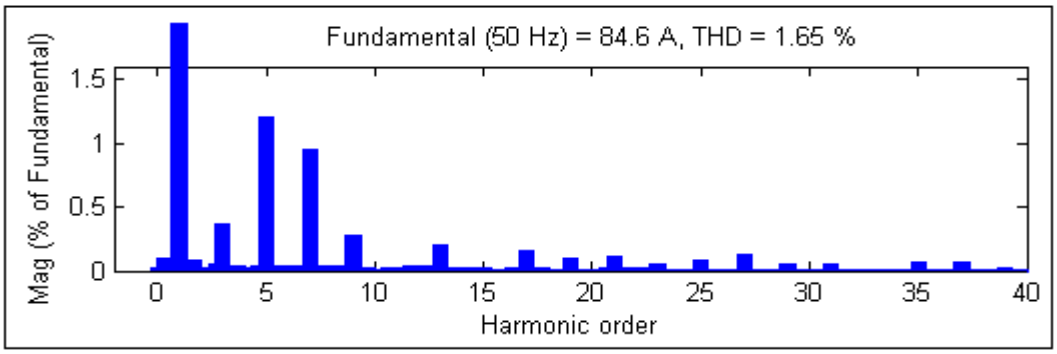


Fig 4.118: Source current with five-level SAPF using *d-q-0* theory based controller and POD

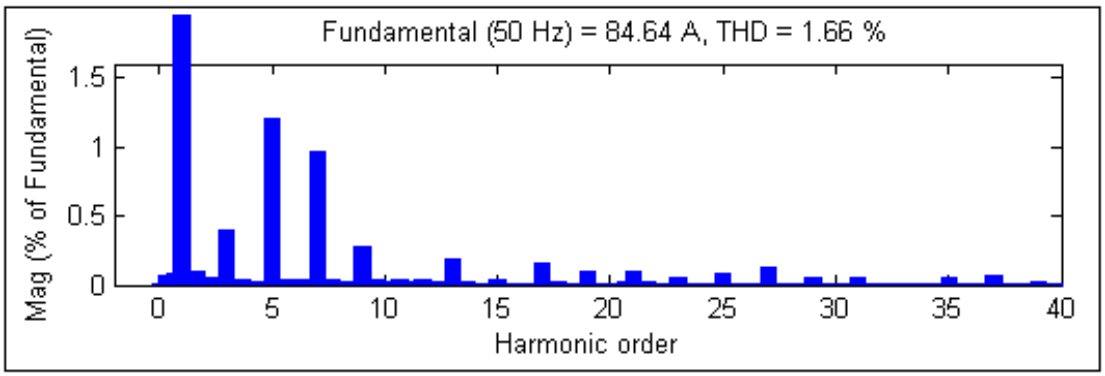
Figs. 4.119 (a) to (c) shows the harmonic spectrum and THD of source currents of phases 'a', 'b' and 'c', respectively. As observed the source current THD is successfully minimized to around 1.65 % as compared to the result before compensation which is 27.51 %. The THDs for the first 40 harmonics calculated for all phase currents is demonstrated to be less than the prescribed value by IEEE-519 Standards.



(a) Phase 'a' source current



(b) Phase 'b' source current



(c) Phase 'c' source current

Fig 4.119: (a) to (c) Harmonic spectrum and THD of source currents with five-level SAPF using *d-q-0* theory based controller and POD

Fig. 120 shows the compensating injected current into the neutral conductor by five-level four-wire SAPF using the proposed *d-q-0* theory based controller and POD modulation technique in order to minimize the source neutral current to zero between the interval 0.08 s and 0.22 s.

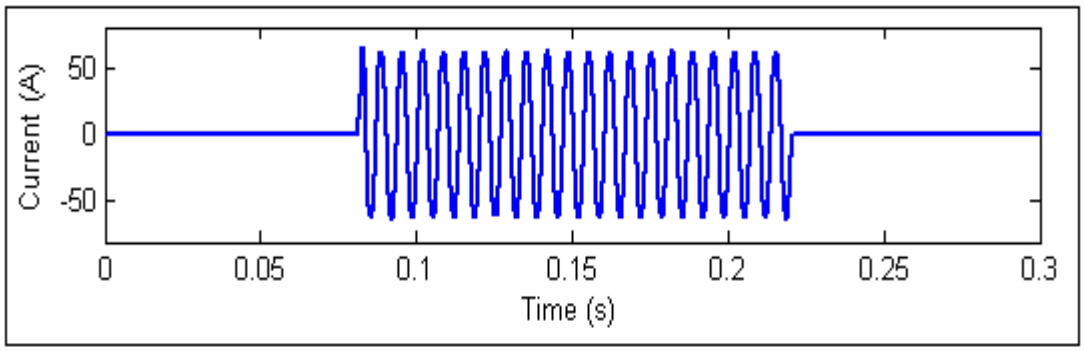


Fig 4.120: Current injected into the neutral conductor by five-level SAPF using *d-q-0* theory based controller and POD

It is found that the five-level four-wire SAPF using the proposed *d-q-0* theory based controller and POD modulation technique is able to minimize the source neutral current to nearly zero when it is connected during the interval 0.08 s to 0.22 s as shown in Fig. 4.121.

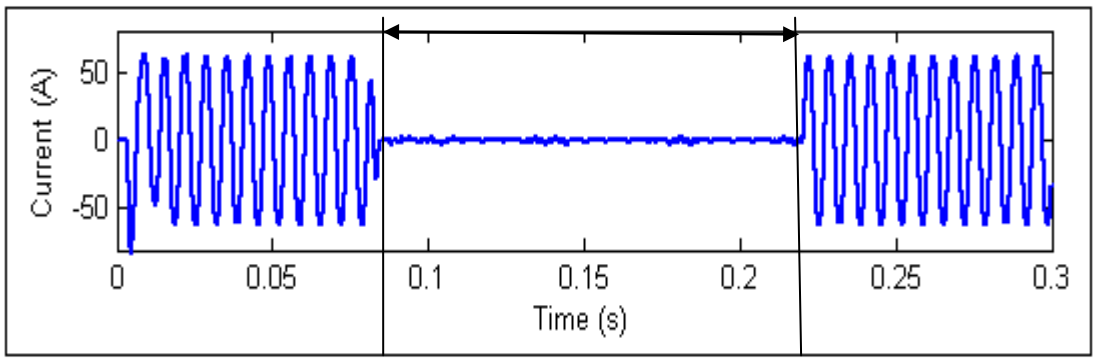


Fig 4.121: Simulated source neutral current with five-level SAPF using *d-q-0* theory based controller and POD

Fig. 4.122 shows phase 'a' source voltage and source current, where the current is non-sinusoidal except during the interval between 0.08 s and 0.22 s when the SAPF has come into operation. During the interval between 0.08 s and 0.22 s the source current is sinusoidal and is in-phase with the source voltage. Thus, it can be concluded that the developed five-level four-wire SAPF using the proposed *d-q-0* theory based controller and POD modulation technique has successfully compensated the harmonic load currents and improved the supply power factor to nearly unity. Similar results are obtained for the phases 'b' and 'c' also.

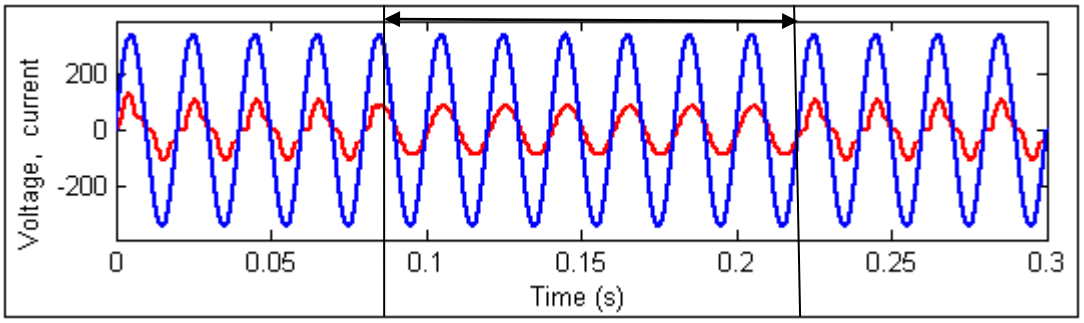


Fig 4.122: Source voltage and source current with five-level SAPF using *d-q-0* theory based controller and POD

4.123 shows the active and reactive powers after compensation by a five-level four-wire SAPF using proposed *d-q-0* theory based controller and POD modulation technique. The reactive power before compensation which is equal 14.59 kvar is successfully compensated to a very low value. Consequently the power factor at the source end is improved to 0.985 which is very close to unity as shown in Fig. 4.124.

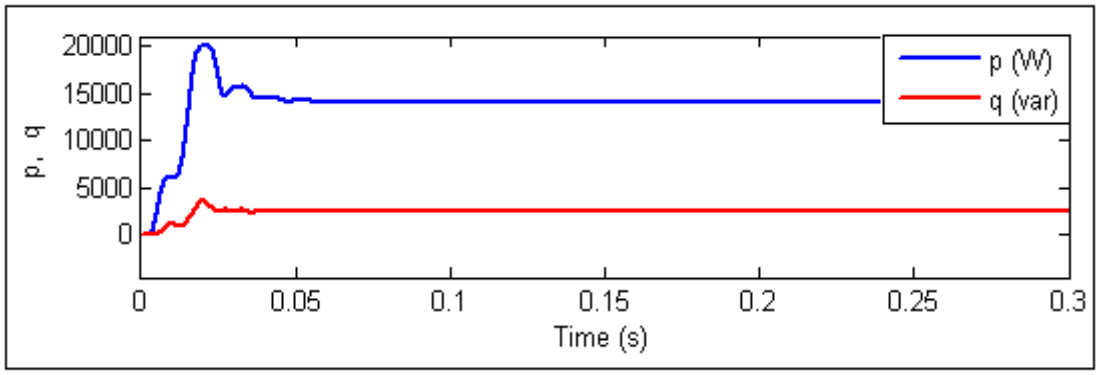


Fig 4.123: Active and reactive powers with five-level SAPF using *d-q-0* theory based controller and POD

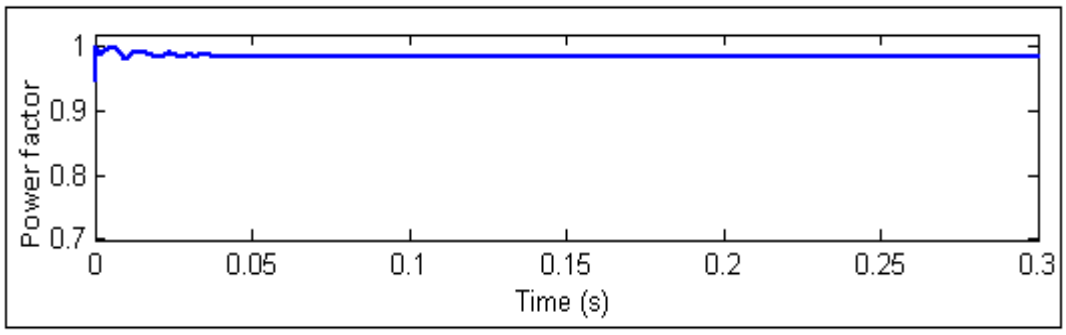


Fig 4.124: Power factor at source end with five-level SAPF using *d-q-0* theory based controller and POD

4.4.2.9 Simulation results with five-level SAPF using a-b-c theory based controller and POD

The proposed controller based on *a-b-c* theory and POD modulation technique is presented as in Figs. 3.8 and 3.17. The five-level SAPF which has four wires generates the distorted injecting current in leg 'a' as shown in Fig. 4.125 by using the proposed *a-b-c* theory based controller and POD modulation technique in order to compensate the distorted current shown in Fig. 4.3. Similar currents but with 120^{o} phase shift are injected by legs 'b' and 'c' of the SAPF into phases 'b' and 'c' of the distribution system. The injected current reaches a peak value of 34.80 A as shown in Fig. 4.125.

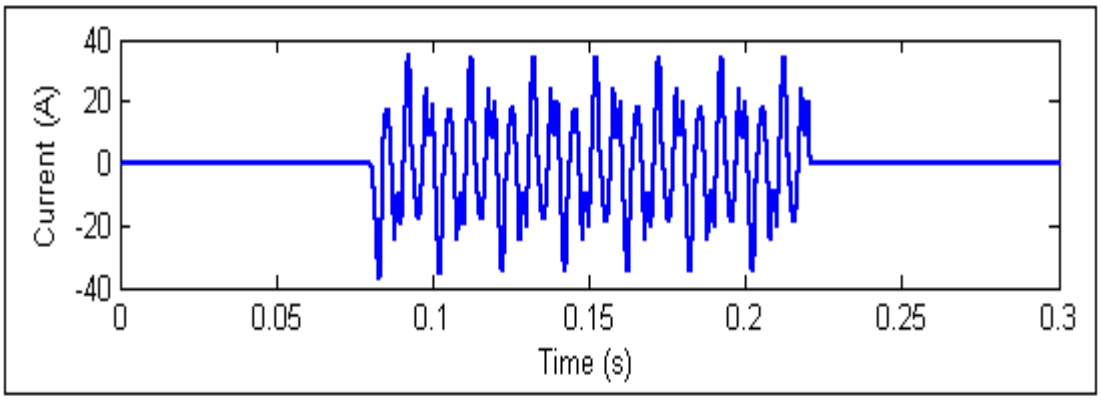


Fig 4.125: Current injected by five-level SAPF using *a-b-c* theory based controller and POD

Fig. 4.126 shows phase 'a' source current with and without SAPF. It is found that the five-level four-wire SAPF using the proposed *a-b-c* theory based controller and POD modulation technique is able to compensate the source current when it is connected during the interval 0.08 s to 0.22 s. The resultant sinusoidal source current between 0.08 s and 0.22 s reaches a peak value of 87.29 A which is less than the uncompensated peak current of 105.2 A. Similar simulation result and measured value is obtained for the phases 'b' and 'c'.

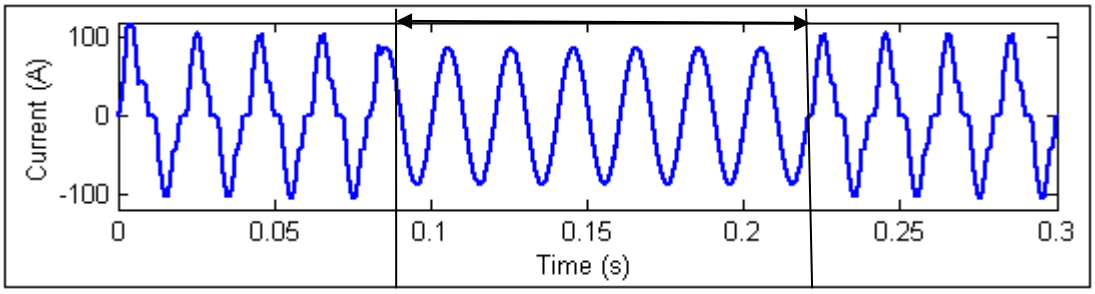
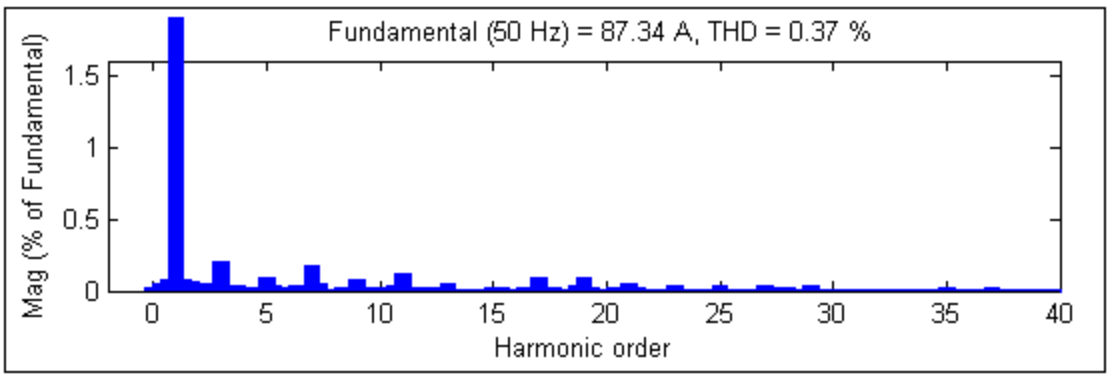
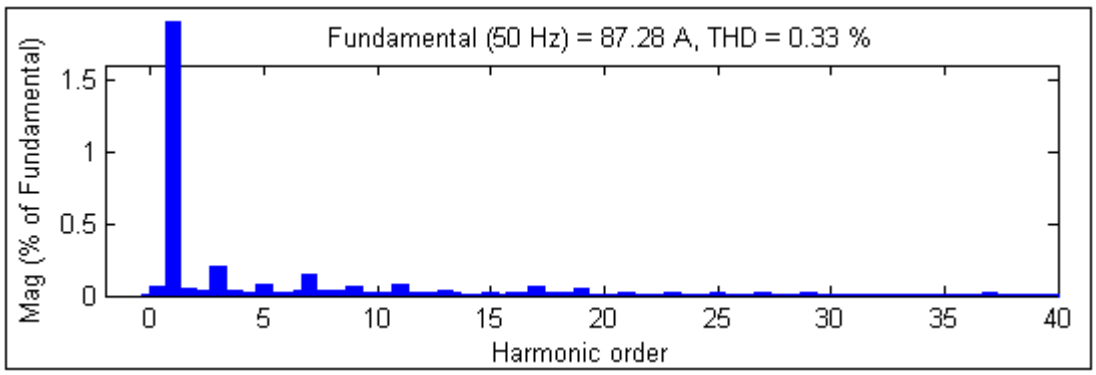


Fig 4.126: Source current with five-level SAPF using *a-b-c* theory based controller and POD

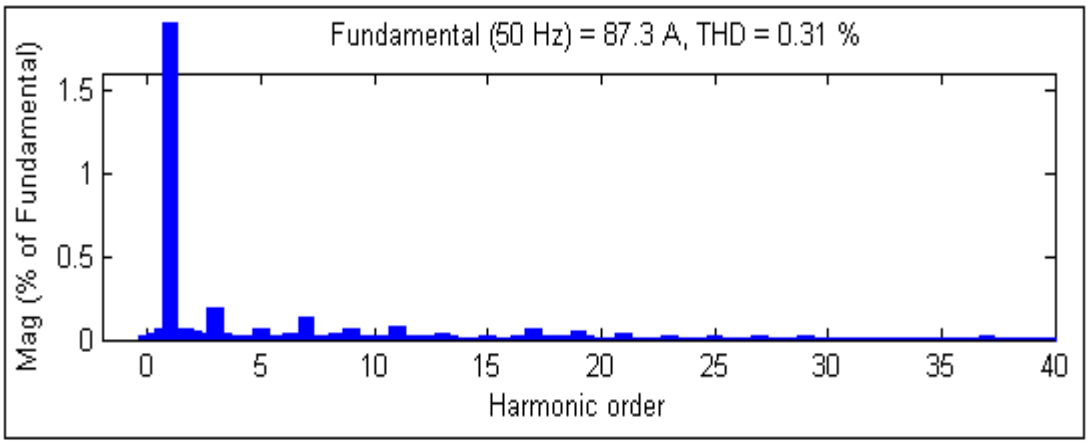
Figs. 4.127 (a) to (c) shows the Harmonic spectrum and THD of source currents of phases 'a', 'b' and 'c', respectively. As observed the source current THD is successfully minimized to 0.37 %, 0.33 % and 0.31 % for the phases 'a', 'b' and 'c', respectively as compared to the result before compensation which is 27.51 %. The THDs for the first 40 harmonics calculated for all phase currents is demonstrated to be less than the prescribed value by IEEE-519 Standards.



(a) Phase 'a' source current



(b) Phase 'b' source current



(c) Phase 'c' source current

Fig 4.127: (a) to (c) Harmonic spectrum and THD of source currents with five-level SAPF using *a-b-c* theory based controller and POD

Fig. 4.128 shows the compensating injected current into the neutral conductor by five-level four-wire SAPF using the proposed *a-b-c* theory based controller and POD modulation technique in order to minimize the source neutral current to zero between the interval 0.08 s and 0.22 s.

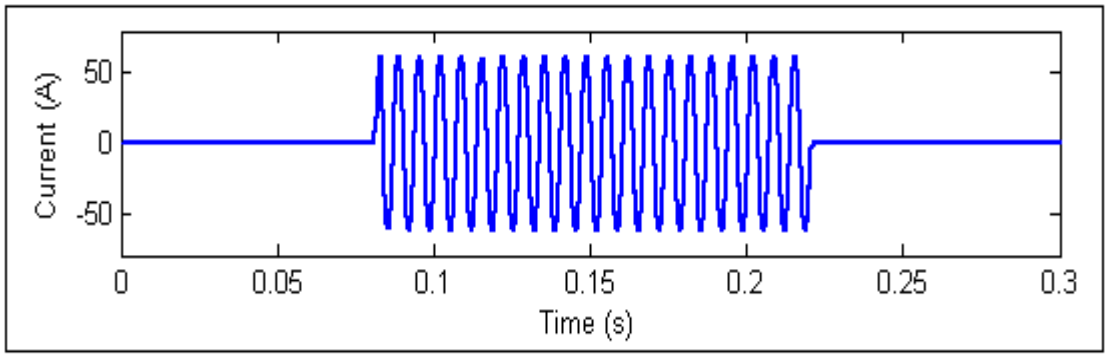


Fig 4.128: Current injected into the neutral conductor by five-level SAPF using *a-b-c* theory based controller and POD

It is found that the five-level four-wire SAPF using the proposed *a-b-c* theory based controller and POD modulation technique is able to minimize the source neutral current to nearly zero when it is connected during the interval 0.08 s to 0.22 s as shown in Fig. 4.129.

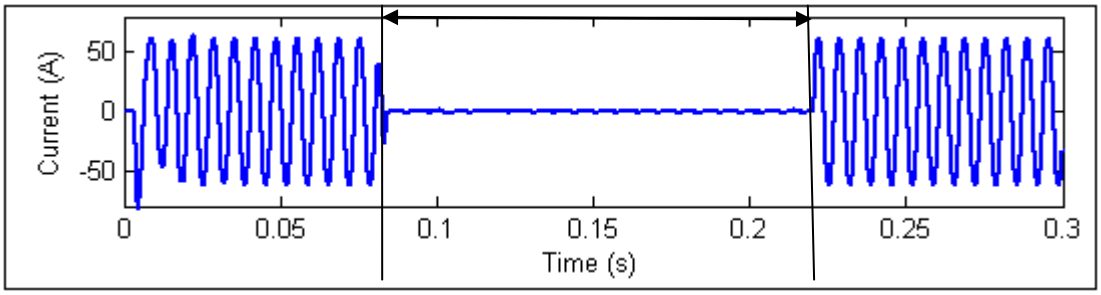


Fig 4.129: Simulated source neutral current with five-level SAPF using *a-b-c* theory based controller and POD

Fig. 4.130 shows phase 'a' source voltage and source current, where the current is non-sinusoidal except during the interval between 0.08 s and 0.22 s when the SAPF has come into operation. During the interval between 0.08 s and 0.22 s the source current is sinusoidal and is in phase with the source voltage. Thus, it can be concluded that the developed five-level four-wire SAPF using the proposed *a-b-c* theory based controller and POD modulation technique has successfully compensated the harmonic load currents and improved the supply power factor to nearly unity. Similar results are obtained for the phases 'b' and 'c' also.

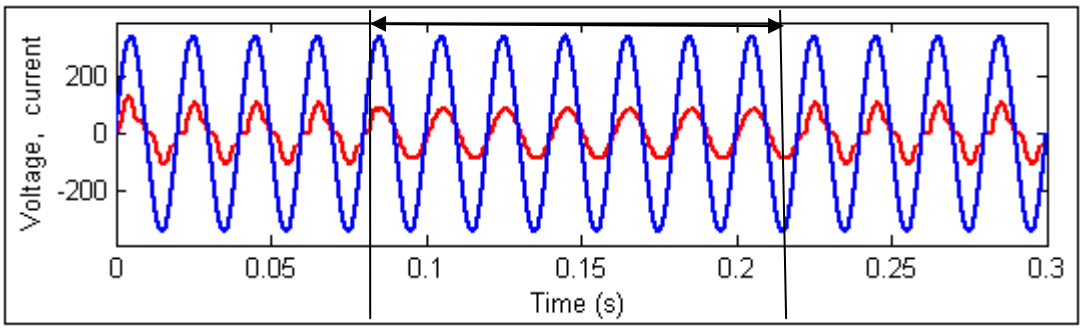


Fig 4.130: Source voltage and source current with five-level SAPF using *a-b-c* theory based controller and POD

Fig. 4.131 shows the active and reactive powers after compensation by a five-level four-wire SAPF using proposed *a-b-c* theory based controller and POD modulation technique. The reactive power before compensation which is equal 14.59 kvar is successfully compensated to a very low value. Consequently the power factor at the source end is improved to 0.986 which is very close to unity as shown in Fig. 4.132.

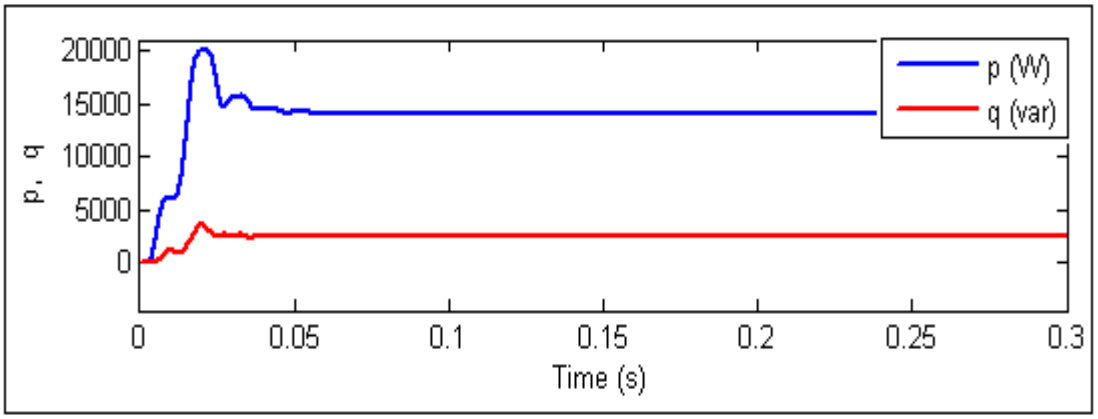


Fig 4.131: Active and reactive powers with five-level SAPF using *a-b-c* theory based controller and POD

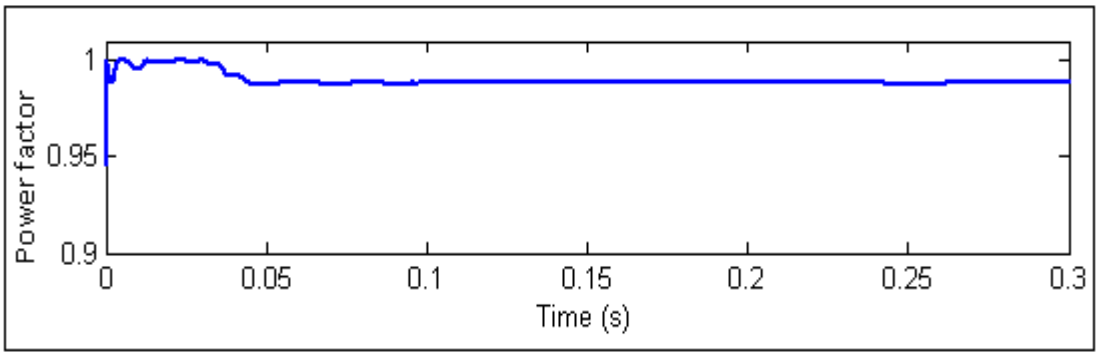


Fig 4.132: Power factor at source end with five-level SAPF using *a-b-c* theory based controller and POD

To compare the performance of five-level four-wire SAPF by the proposed three types of controllers and POD modulation technique, the THDs of source currents are presented in Table 4.17. It can be observed that in all the three cases the THD is less than the prescribed limit of 5 % as recommended by IEEE-519 standards. However, the THD obtained by the proposed *a-b-c* theory based controller is far less than by the other two controllers as illustrated in Table 4.17.

Table 4.17: Source currents THD with five-level SAPF using POD

Controller	THD *p-q* theory	THD *d-q-0* theory	THD *a-b-c* theory
Phase 'a'	2.21	1.65	0.37
Phase 'b'	2.20	1.65	0.33
Phase 'c'	2.19	1.66	0.31

Simulation results of compensated source neutral currents by five-level four-wire SAPF using the three types of proposed controllers and APOD modulation technique are given in Table. 4.18. As observed these currents are far less than the value of 64.17 A before compensation. However the controller based on *d-q-0* theory reduced the source neutral conductor current to a very small value of 0.74 A as shown in Table. 4.18.

Table 4.18: Source neutral current with five-level SAPF using POD

Controller type	*p-q* theory	*d-q-0* theory	*a-b-c* theory
Peak neutral current	0.99 A	0.74 A	1.12 A

Simulation results for power factor at the source end with five-level four-wire SAPF using the three different proposed controllers and POD modulation technique is given in Table 4.19. It can be observed that the power factor is greatly improved as compared to the value before compensation which is 0.8056. However the controller based on *p-q* theory improved the source end power factor to unity as shown in Table 4.19 which makes the source current sinusoidal.

Table 4.19: Power factor at source end with five-level SAPF using POD

Controller type	*p-q* theory	*d-q-0* theory	*a-b-c* theory
Supply Power factor	1.0	0.985	0.986

To observe the effect of switching in operation of the five-level SAPF, the recorded peak transient current at source is presented in Table 4.20. It is observed that *d-q-0* theory based controller with POD modulation technique gives less peak current as compared to the other two controllers as shown in Fig. Table 4.20.

Table 4.20: Transient current with five-level SAPF using POD

Controller type	*p-q* theory	*d-q-0* theory	*a-b-c* theory
Peak transient current	85.43 A	83.52 A	87.72 A

4.5 Case study 3 – Performance of seven-level four-wire SAPF

The distribution system model as in Fig. 3.21 of Chapter 3 using a seven-level four-wire SAPF compensator with the proposed three control schemes (*p-q* theory, *d-q-0* theory and *a-b-c* theory) based on PS-SPWM and LS-SPWM techniques is considered for simulation. Simulation is carried out on the system model by using each proposed control topology independently. For all control schemes, the seven-level four-wire SAPF compensates not only harmonic currents, but also reactive current components. To distinguish the simulation results with and without SAPF, a circuit breaker is used to provide connection of SAPF to the system at PCC. The circuit breaker closes at 0.08 s and opens at 0.22 s in all cases of simulation except in the case of simulation for active and reactive power flow, and power factor where the SAPF is connected continuously.

4.5.1 Simulation results with seven-level four-wire SAPF using proposed controllers and PS-SPWM

In the PS-SPWM technique the PWM signals are generated in order to control the seven-level CHB-VSI based SAPF as shown in Appendix D. The reference current is compared with six triangular carrier signals that are phase shifted by 360/6 degrees. By comparing these carriers and the reference current, the PWM signals for a seven-level CHB-VSI are developed.

The proposed controller based on *p-q* theory and PS-SPWM technique is presented as in Figs. 3.4 and 3.12 of Chapter 3. The seven-level SAPF which has four wires generates the distorted injecting current in leg ‘a’ as shown in Fig. 4.133 by using the proposed *p-q* theory based controller and PS-SPWM technique in order to compensate the distorted current shown in Fig. 4.3. Similar currents but with 120^{o} phase shift are injected by legs ‘b’ and ‘c’ of the SAPF into phases ‘b’ and ‘c’ of the distribution system. The injectd current reaches a peak value of 49.40 A as shown in Fig. 4.133.

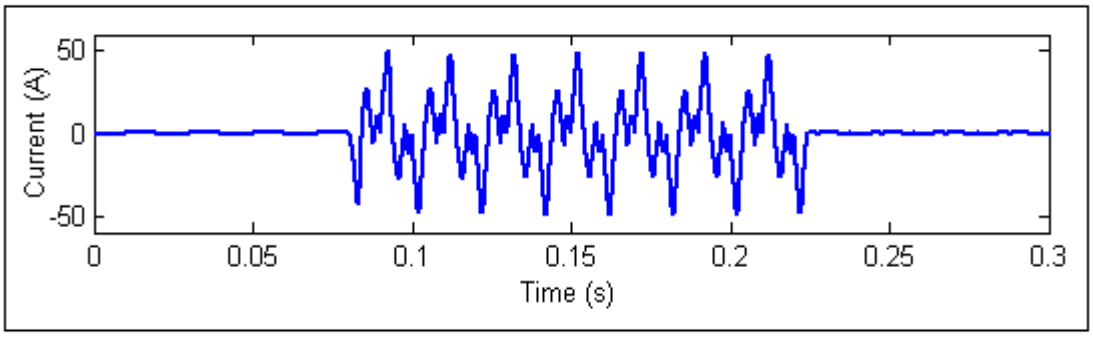


Fig 4.133: Current injected by seven-level SAPF using *p-q* theory based controller and PS-SPWM

Fig. 4.134 shows phase 'a' source current with and without SAPF. It is found that the seven-level four-wire SAPF using the proposed *p-q* theory based controller and PS-SPWM technique is able to compensate the source current when it is connected during the interval 0.08 s to 0.22 s. The resultant sinusoidal source current between 0.08 s and 0.22 s reaches a peak value of 85.82 A which is less than the uncompensated peak current of 105.2 A. Similar simulation result and measured value is obtained for the phases 'b' and 'c'.

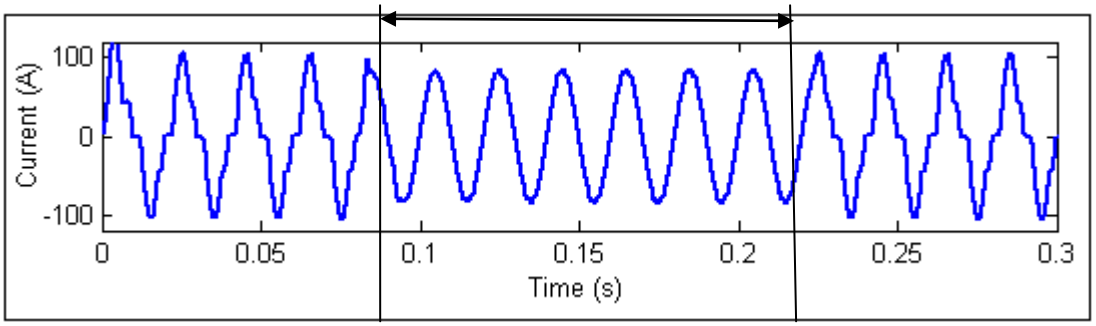


Fig 4.134: Source current with seven-level SAPF using *p-q* theory

The magnitudes of peak injected current by the seven-level SAPF and the peak source current after compensation is presented in Table 4.22.

Table 4.21: Injected and source currents with seven-level SAPF using PS-SPWM

Controller	*p-q* theory	*d-q-0* theory	*a-b-c* theory
Peak injected current	49.40 A	32.01 A	35.11 A
Peak source current	85.82 A	84.03 A	87.91 A

To compare the performance of seven-level four-wire SAPF by the proposed three types of controllers and PS-SPWM technique, the THDs of source currents are presented in Table 4.23. It can be observed that in all the three cases the THD is less than the prescribed limit of 5 % as recommended by IEEE-519 standards. However, the THD obtained by the proposed *a-b-c* theory based controller is far less than by the other two controllers as illustrated in Table 4.23.

Table 4.22: Source currents % THD with seven-level SAPF using PS-SPWM

Controller	*p-q* theory	*d-q-0* theory	*a-b-c* theory
Phase 'a'	2.01	1.45	0.30
Phase 'b'	2.03	1.43	0.28
Phase 'c'	1.99	1.43	0.27

Simulation results of compensated source neutral currents by seven-level four-wire SAPF using the three types of proposed controllers and PS-SPWM technique are given in Table. 4.24. As observed these currents are far less than the value of 64.17 A before compensation. However the controller based on *d-q-0* theory reduced the source neutral conductor current to a very small value of 0.54 A as shown in Table. 4.24.

Table 4.23: Source neutral current with seven-level SAPF using PS-SPWM

Controller type	*p-q* theory	*d-q-0* theory	*a-b-c* theory
Peak neutral current	0.77 A	0.54 A	0.89 A

Simulation results for power factor at the source end with seven-level four-wire SAPF using the three different proposed controllers and PS-SPWM technique is given in Table 4.25. It can be observed that the power factor is greatly improved as compared to the value before compensation which is 0.8056. However the controller based on *p-q* theory improved the source end power factor to unity as shown in Table 4.25 which makes the source current sinusoidal.

Table 4.24: Power factor at source end with seven-level SAPF using PS-SPWM

Controller type	*p-q* theory	*d-q-0* theory	*a-b-c* theory
Supply Power factor	1.0	0.988	0.991

To observe the effect of switching in operation of the seven-level SAPF, the recorded peak transient current at source is presented in Table 4.26. It is observed that *d-q-0* theory based controller with PS-SPWM technique gives less peak current as compared to the other two controllers as shown in Table 4.26.

Table 4.25: Transient current with seven-level SAPF using PS-SPWM

Controller type	*p-q* theory	*d-q-0* theory	*a-b-c* theory
Peak transient current	85.33 A	83.41 A	87.61 A

4.5.2 Simulation results with seven-level SAPF using LS-SPWM

The LS-SPWM technique which is introduced in section 3.6.3 of Chapter 3 is used to generate the PWM signals in order to control the seven-level CHB-VSI based SAPF as shown in Appendix D. The reference current is compared with six triangular carrier signals using three types of LS-SPWM such as IPD, APOD and POD modulation techniques. Simulation results are presented in each case.

4.5.2.1 Simulation results with seven-level SAPF using the proposed controllers and IPD

The magnitudes of peak injected current by the seven-level SAPF and the peak source current after compensation is presented in Table 4.27.

Table 4.26: Injected and source currents with seven-level SAPF using IPD

Controller	*p-q* theory	*d-q-0* theory	*a-b-c* theory
Peak injected current	49.43 A	32.90 A	34.91 A
Peak source current	85.03 A	85.06 A	87.50 A

To compare the performance of seven-level four-wire SAPF by the proposed three types of controllers and IPD modulation technique, the THDs of source currents are presented in Table 4.28. It can be observed that in all the three cases the THD is less than the prescribed limit of 5 % as recommended by IEEE-519 standards. However, the THD obtained by the proposed *a-b-c* theory based controller is far less than by the other two controllers as illustrated in Table 4.28.

Table 4.27: Source currents % THD with seven-level SAPF using IPD

Controller	*p-q* theory	*d-q-0* theory	*a-b-c* theory
Phase 'a'	2.09	1.55	0.27
Phase 'b'	2.07	1.54	0.27
Phase 'c'	2.03	1.54	0.28

Simulation results of compensated source neutral currents by seven-level four-wire SAPF using the three types of proposed controllers and IPD modulation technique are given in Table. 4.29. As observed these currents are far less than the value of 64.17 A before compensation. However the controller based on *d-q-0* theory reduced the source neutral conductor current to a very small value of 0.54 A as shown in Table. 4.29.

Table 4.28: Source neutral current with seven-level SAPF using IPD

Controller type	*p-q* theory	*d-q-0* theory	*a-b-c* theory
Peak neutral current	0.79 A	0.54 A	0.92 A

Simulation results for power factor at the source end with seven-level four-wire SAPF using the three different proposed controllers and IPD modulation technique is given in Table 4.30. It can be observed that the power factor is greatly improved as compared to the value before compensation which is 0.8056. However the controller based on *p-q* theory improved the source end power factor to unity as shown in Table 4.30 which makes the source current sinusoidal.

Table 4.29: Power factor at source end with seven-level SAPF using IPD

Controller type	*p-q* theory	*d-q-0* theory	*a-b-c* theory
Supply Power factor	1.0	0.988	0.990

To observe the effect of switching in operation of the seven-level SAPF, the recorded peak transient current at source is presented in Table 4.31. It is observed that *d-q-0* theory based controller with IPD modulation technique gives less peak current as compared to the other two controllers as shown in Table 4.31.

Table 4.30: Transient current with seven-level SAPF using IPD

Controller type	*p-q* theory	*d-q-0* theory	*a-b-c* theory
Peak transient current	85.35 A	83.41 A	87.61 A

4.5.2.2 Simulation results with seven-level SAPF using the proposed controllers and APOD

The magnitudes of peak injected current by the seven-level SAPF and the peak source current after compensation is presented in Table 4.32.

Table 4.31: Injected and source currents with seven-level SAPF using APOD

Controller	*p-q* theory	*d-q-0* theory	*a-b-c* theory
Peak injected current	49.51 A	33.00 A	35.00 A
Peak source current	84.52 A	84.78 A	87.55 A

To compare the performance of seven-level four-wire SAPF by the proposed three types of controllers and APOD modulation technique, the THDs of source currents are presented in Table 4.33. It can be observed that in all the three cases the THD is less than the prescribed limit of 5 % as recommended by IEEE-519 standards. However, the THD obtained by the proposed *a-b-c* theory based controller is far less than by the other two controllers as illustrated in Table 4.33.

Table 4.32: Source currents THD with seven-level SAPF using APOD

Controller	THD *p-q* theory	THD *d-q-0* theory	THD *a-b-c* theory
Phase 'a'	2.08	1.53	0.25
Phase 'b'	2.06	1.53	0.23
Phase 'c'	2.07	1.53	0.22

Simulation results of compensated source neutral currents by seven-level four-wire SAPF using the three types of proposed controllers and APOD modulation technique are given in Table. 4.34. As observed these currents are far less than the value of 64.17 A before compensation. However the controller based on *d-q-0* theory reduced the source neutral conductor current to a very small value of 0.55 A as shown in Table. 4.34.

Table 4.33: Source neutral current with seven-level SAPF using APOD

Controller type	*p-q* theory	*d-q-0* theory	*a-b-c* theory
Peak neutral current	0.80 A	0.55 A	0.93 A

Simulation results for power factor at the source end with seven-level four-wire SAPF using the three different proposed controllers and APOD modulation technique is given in Table 4.35. It can be observed that the power factor is greatly improved as compared to the value before compensation which is 0.8056. However the controller based on *p-q* theory improved the source end power factor to unity as shown in Table 4.35 which makes the source current sinusoidal.

Table 4.34: Power factor at source end with seven-level SAPF using APOD

Controller type	*p-q* theory	*d-q-0* theory	*a-b-c* theory
Supply Power factor	1.0	0.987	0.989

To observe the effect of switching in operation of the seven-level SAPF, the recorded peak transient current at source is presented in Table 4.36. It is observed that *d-q-0* theory based controller with APOD modulation technique gives less peak current as compared to the other two controllers as shown in Table 4.36.

Table 4.35: Transient current with seven-level SAPF using APOD

Controller type	*p-q* theory	*d-q-0* theory	*a-b-c* theory
Peak transient current	85.34 A	83.43 A	87.64 A

4.5.2.3 Simulation results with seven-level SAPF using the proposed controllers and POD

The magnitudes of peak injected current by the seven-level SAPF and the peak source current after compensation is presented in Table 4.37.

Table 4.36: Injected and source currents with seven-level SAPF using POD

Controller	*p-q* theory	*d-q-0* theory	*a-b-c* theory
Peak injected current	49.56 A	32.11 A	34.91 A
Peak source current	84.60 A	84.32 A	87.38 A

To compare the performance of seven-level four-wire SAPF by the proposed three types of controllers and POD modulation technique, the THDs of source currents are presented in Table 4.38. It can be observed that in all the three cases the THD is less than the prescribed limit of 5 % as recommended by IEEE-519 standards. However, the THD obtained by the proposed *a-b-c* theory based controller is far less than by the other two controllers as illustrated in Table 4.38.

Table 4.37: Source currents THD with seven-level SAPF using POD

Controller	THD *p-q* theory	THD *d-q-0* theory	THD *a-b-c* theory
Phase ‘a’	2.08	1.52	0.25
Phase ‘b’	2.07	1.53	0.21
Phase ‘c’	2.05	1.52	0.20

Simulation results of compensated source neutral currents by seven-level four-wire SAPF using the three types of proposed controllers and POD modulation technique are given in Table. 4.39. As observed these currents are far less than the value of 64.17 A before compensation. However the controller based on *d-q-0* theory

reduced the source neutral conductor current to a very small value of 0.54 A as shown in Table. 4.39.

Table 4.38: Source neutral current with seven-level SAPF using POD

Controller type	*p-q* theory	*d-q-0* theory	*a-b-c* theory
Peak neutral current	0.78 A	0.54 A	0.94 A

Simulation results for power factor at the source end with seven-level four-wire SAPF using the three different proposed controllers and POD modulation technique is given in Table 4.40. It can be observed that the power factor is greatly improved as compared to the value before compensation which is 0.8056. However the controller based on *p-q* theory improved the source end power factor to unity as shown in Table 4.40 which makes the source current sinusoidal.

Table 4.39: Power factor at source end with seven-level SAPF using POD

Controller type	*p-q* theory	*d-q-0* theory	*a-b-c* theory
Supply Power factor	1.0	0.988	0.989

To observe the effect of switching in operation of the seven-level SAPF, the recorded peak transient current at source is presented in Table 4.41. It is observed that *d-q-0* theory based controller with POD modulation technique gives less peak current as compared to the other two controllers as shown in Table 4.41.

Table 4.40: Transient current with seven-level SAPF using POD

Controller type	*p-q* theory	*d-q-0* theory	*a-b-c* theory
Peak transient current	85.35 A	83.42 A	87.63 A

Table 4. 43 shows the performance results from the three different proposed control techniques which are obtained by two-level, five-level and seven-level SAPF.

Table 4.41: Performance results by two-level, five-level and seven-level SAPF

Modulation Technique	Controllers	Source current THD			Peak neutral current (A)			Power Factor		
		Two- Level	Five- Level	Seven- Level	Two- Level	Five- Level	Seven- Level	Two- Level	Five- Level	Seven-Level
Hysteresis	*p-q*	2.46			0.88			1.0		
	d-q-0	2.08			0.49			0.985		
	a-b-c	0.76			1.37			0.987		
PS-SPWM	*p-q*		2.20	1.99		0.95	0.77		1.00	1.00
	d-q-0		1.57	1.43		0.70	0.54		0.986	0.988
	a-b-c		0.30	0.27		1.20	0.89		0.989	0.991
IPD	*p-q*		2.19	2.03		0.90	0.79		1.00	1.00
	d-q-0		1.66	1.54		0.60	0.54		0.986	0.988
	a-b-c		0.29	0.27		1.21	0.92		0.988	0.990
APOD	*p-q*		2.20	2.06		0.92	0.80		1.00	1.00
	d-q-0		1.65	1.53		0.63	0.55		0.985	0.987
	a-b-c		0.33	0.22		1.13	0.93		0.988	0.989
POD	*p-q*		2.19	2.05		0.99	0.78		1.00	1.00
	d-q-0		1.65	1.52		0.74	0.54		0.985	0.988
	a-b-c		0.31	0.21		1.12	0.94		0.986	0.989

Table 4. 44 shows the effect of switching in operation of the two-level, five-level and seven-level SAPF, from the record of peak transient current it is found that five-level and seven-level SAPF under the different modulation techniques gives less peak transient current as compared to the two-level SAPF.

Table 4.42: peak transient current by two-level, five-level and seven-level SAPF

Case	Peak transient current (A)
Two-level SAPF	209.9
Five-level SAPF	82.99
Seven-level SAPF	83.41

4.6 Summary

In this chapter, simulation results and discussion on the compensation performance of SAPF for three-phase four-wire distribution system are presented in order to achieve the objective of the proposed study. Initially, the distribution system model is simulated without SAPF and then simulation is carried out with the two-level, five-level and seven-level three-phase four-wire SAPF using three different proposed controllers based on *p-q* theory, *d-q-0* theory and *a-b-c* theory, respectively. These SAPFs with the proposed controllers are applied to suppress the current harmonics, to minimize the source neutral current as well as the THD of source current below 5 % and to improve the power factor at the supply end very close to unity. From the simulation results, it is observed that, the minimum value of source neutral current obtained by *d-q-0* theory based controller is less compared to the *p-q* theory and *a-b-c* theory based controllers for both the two-level and multilevel three-phase four-wire SAPF. Also, it is observed that unity power factor is achieved at the source end by *p-q* theory based controller whereas minimum source current THD is achieved by *a-b-c* based controller. The compensation with five-level and seven-level three-phase four-wire SAPF caused an improvement in the minimization of source transient current. Moreover, it is observed from overall comparison, the compensating performance results obtained by five-level, seven-level VSI based three-phase four-wire SAPF is supperior over the results obtained by the two-level VSI based three-phase four-wire SAPF. The next chapter reports the conclusions.

CHAPTER 5

CONCLUSIONS AND RECOMMENDATIONS

5.1 Conclusions

The main focus in this thesis is minimization of current harmonics, improvement of power factor and elimination of neutral conductor current at the supply end of a three-phase four-wire distribution system. To investigate these power quality disturbances using two-level, five-level and seven-level VSI based SAPF, efficient control strategies and modeling of controllers are developed. Using MATLAB/SIMULINK software as a simulation tool, first a SIMULINK model of three-phase four-wire distribution system supplying mixed non-linear loads i.e. a three-phase thyristor bridge rectifier and three single-phase diode bridge rectifiers is developed. Initially the effect of mixed non-linear loads which create the power quality disturbances at the supply end of the three-phase four-wire distribution system is established. It is shown by simulation results that the source current as non-sinusoidal with a high current THD of 27.51 %, the source power factor as 0.8056 and the source neutral conductor current as 67.17 A for a standard distribution system.

For the two-level VSI based SAPF using three independent proposed control strategies based on *p-q* theory, *d-q-0* theory and *a-b-c* theory SIMULINK models are developed. Simulation results have clearly shown the improvement in power quality disturbances at the supply end of the distribution system. When the SAPF is connected to the distribution system the source current is shown to be sinusoidal with a low current THD as 0.76 % by *a-b-c* theory based controller, the supply end power factor as unity by *p-q* theory based controller and the source neutral conductor current as 0.49 A by *d-q-0* theory based controller. It is found that in all the case studies the

source current THD by the SAPF using the three proposed controllers is below the prescribed limit of 5 % by IEEE-519 standards, which clearly shows the effectiveness of two-level VSI based SAPF. As the switching frequency for IGBT switches of two-level VSI based SAPF is 2 kHz which is very high, five-level and seven-level VSI based SAPF are proposed where the switching frequency is limited to the normal supply frequency for efficient operation of VSI.

As the cascaded H-bridge multilevel inverter has many advantages over the diode-clamped and flying-capacitor multilevel inverters, further research is carried out on five-level and seven-level CHB-VSI based SAPF.

The PS-SPWM and LS-SPWM techniques are used to generate the PWM signals in order to control the five-level CHB-VSI based SAPF. In the case of LS-SPWM technique three different types of modulation techniques are used, namely, IPD, APOD and POD techniques.

SIMULINK models are developed for five-level VSI based SAPF by using these modulation techniques for the control strategies (*p-q* theory, *d-q-0* theory and *a-b-c* theory). Simulation results presented in each case study clearly show the improvement in power quality disturbances at the supply end of the distribution system.

When the SAPF is modulated by PS-SPWM technique and connected to the distribution system the source current is shown to be sinusoidal with a low current THD as 0.3 % by *a-b-c* theory based controller, the supply end power factor as unity by *p-q* theory based controller and the source neutral conductor current as 0.70 A by *d-q-0* theory based controller. It is found that in all the case studies the source current THD by the SAPF using the three proposed controllers is below the prescribed limit of 5 % by IEEE-519 standards, which clearly shows the effectiveness of five-level VSI based SAPF. Similar results are obtained with seven-level VSI based SAPF also.

When the SAPF is modulated by LS-SPWM technique and connected to the distribution system the source current is shown to be sinusoidal with a low current THD as 0.29 % by *a-b-c* theory based controller (IPD), the supply end power factor as unity by *p-q* theory based controller (IPD, APOD and POD) and the source neutral conductor current as 0.60 A by *d-q-0* theory based controller (IPD). It is found that in all the case studies the source current THD by the SAPF using the three proposed

controllers is below the prescribed limit of 5 % by IEEE-519 standards, which clearly shows the effectiveness of five-level VSI based SAPF. Similar results are also obtained with seven-level VSI based SAPF.

From the simulation results based on the five-level and seven-level SAPF it is observed that the model developed by the proposed controllers yielded reduced source current THD, high power factor at the source end, a very low source neutral conductor current and low source peak transient current as compared to two-level SAPF. However the seven-level VSI based SAPF is proved to be more efficient as compared to five-level VSI based SAPF.

It is clearly shown by the simulation results that the source current is nearly sinusoidal after compensation by using the two-level, five-level and seven-level three-phase four-wire SAPF with the three different proposed controllers. Subsequently the compensated source current is in-phase with the source voltage, thus reducing the reactive power requirement as the source end power factor is very close to unity.

The effectiveness and compensation performance of the SAPF is clearly demonstrated by these case studies and simulation results. The proposed control strategies and modulation techniques ensured efficient operation of two-level, five-level and seven-level VSI based SAPF for power quality improvement of three-phase four-wire distribution systems.

In summary, the capability of the two-level, five-level and seven-level three-phase four-wire SAPF with the proposed current controllers provides a flexible solution for power quality problems caused by the non-linear loads. The proposed controllers are proved to be simple, robust and possesses reliable characteristics which have shown satisfactory compensating performance by minimizing harmonic currents, improving the current THD and power factor at source end, and also by minimizing the source neutral current very close to zero.

5.2 Contributions

The main contributions of this thesis are as follows:

1) Design and development techniques of measurement and simulation blocks of

three-phase four-wire distribution system using MATLAB/SIMULINK software.

2) Proposed three control techniques based on *p-q* theory, *d-q-0* theory and *a-b-c* theory to control the three-phase four-wire two-level, five-level and seven-level SAPF.
3) Five-level and seven-level CHB-VSI based three-phase four-wire SAPF have been proposed and simulated using several modulation techniques such as PS-SPWM as well as the three types of LS-SPWM (IPD, APOD and POD) which are simulated by using MATLAB/SIMULINK software and the simulation results are compared.
4) Improvement in source peak transient current by using five-level and seven-level SAPF.

5.3 Future works and recommendations

Based on the work accomplished in this thesis, the following tasks are recommended for future work:

- Hardware implementation of the two-level, five-level and seven-level three-phase four-wire SAPF as an extension to the verification of simulation results.
- Higher levels of the SAPF such as nine-level, eleven-level etc. can be considered for higher voltage applications
- The proposed three-phase five-level and seven-level SAPF can be considered for medium-level and high-level voltage networks without a coupling transformer.

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[3] Izzeldin Idris Abdalla, K. S. Rama Rao, N. Perumal "A comparative study of shunt active power filter performance in distribution systems," *IEEE, The 5th International Power Engineering and Optimization Conference, (PEOCO 2011), Shah Alam, Selangor, Malaysia*, 6-7 June 2011.

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[5] <Accepted> Izzeldin Idris Abdalla, K. S. Rama Rao, N. Perumal "Seven-level cascaded inverter based shunt active power filter in a four-wire distribution system" *IEEE, The 9th International Conference on Power Electronics and Drive Systems (PEDS 2011), Singapore on* 5 – 8 December 2011.

[6] <Accepted> Izzeldin Idris Abdalla**,** K. S. Rama Rao, N. Perumal "Five-level Cascaded Inverter Based Shunt Active Power Filter in Four-wire Distribution System" *2011 2nd International Conference on Advances in Energy Engineering (ICAEE 2011),* Bangkok, Thailand *on* 27-28, December 2011.

[7] <Book Chapter accepted> Izzeldin Idris Abdalla, K. S. Rama Rao ''Simulation studies on a three-phase voltage source inverter (VSI) based shunt active power filter (SAPF) by MATLAB/SIMULINK" *Intech Open Access Publisher, SIMULINK, University Campus STeP Ri, Slavka Krautzeka* 83/A, 51000 Rijeka, Croati, 2011.

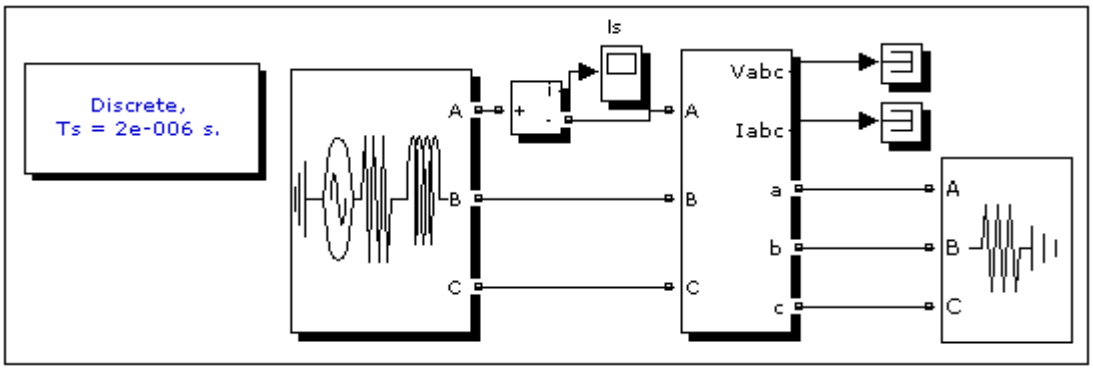
Appendix A

Linear and non-linear loads

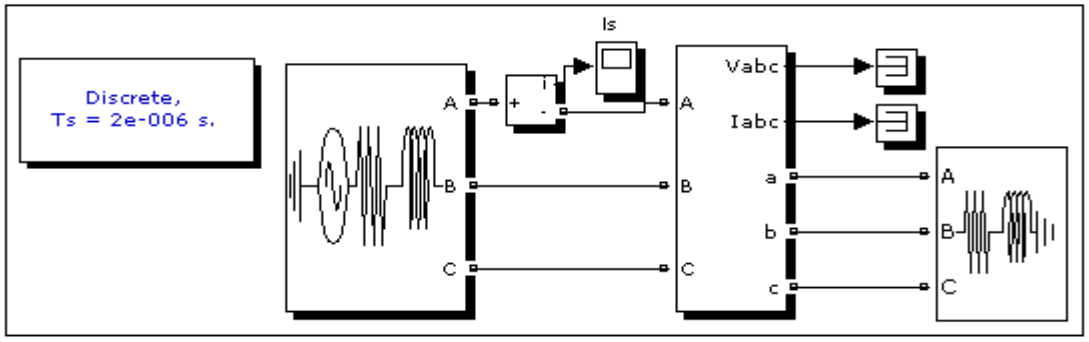
As mentioned in section 2.3.3 of chapter 2 the effect of linear and non-linear loads on the distribution system are demonstrated by the following simulation results:

A.1 Linear loads

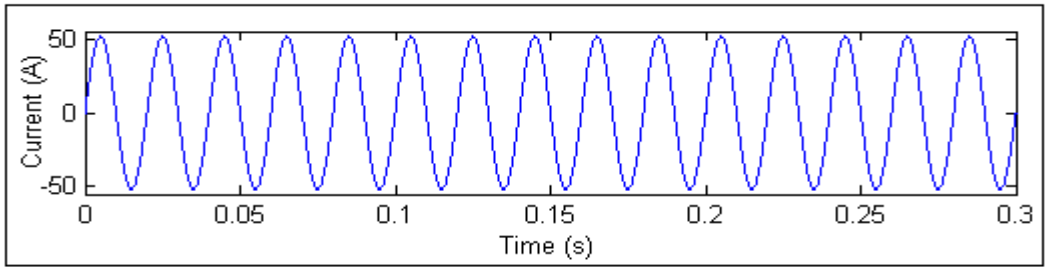
Similar simulation results, waveform and 0 % THD were obtained for both resistive and resistive/inductive loads as shown in Fig A1 (c) and (d).



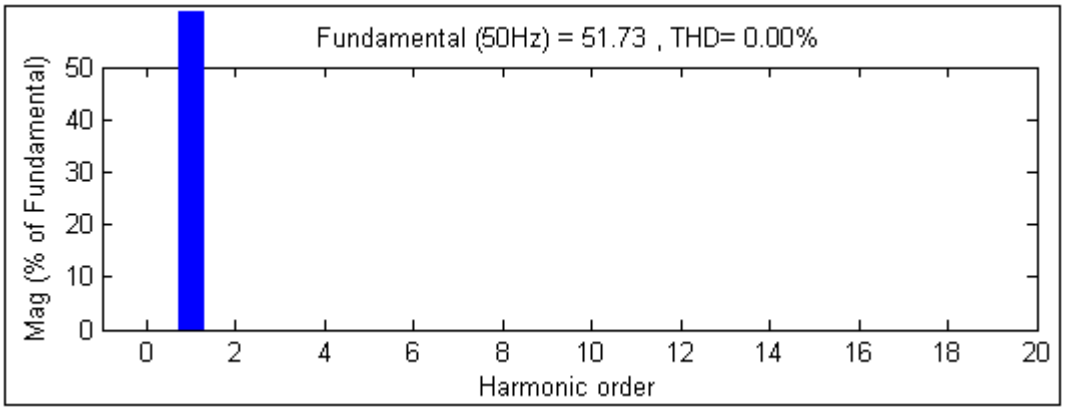
(a)



(b)



(c)



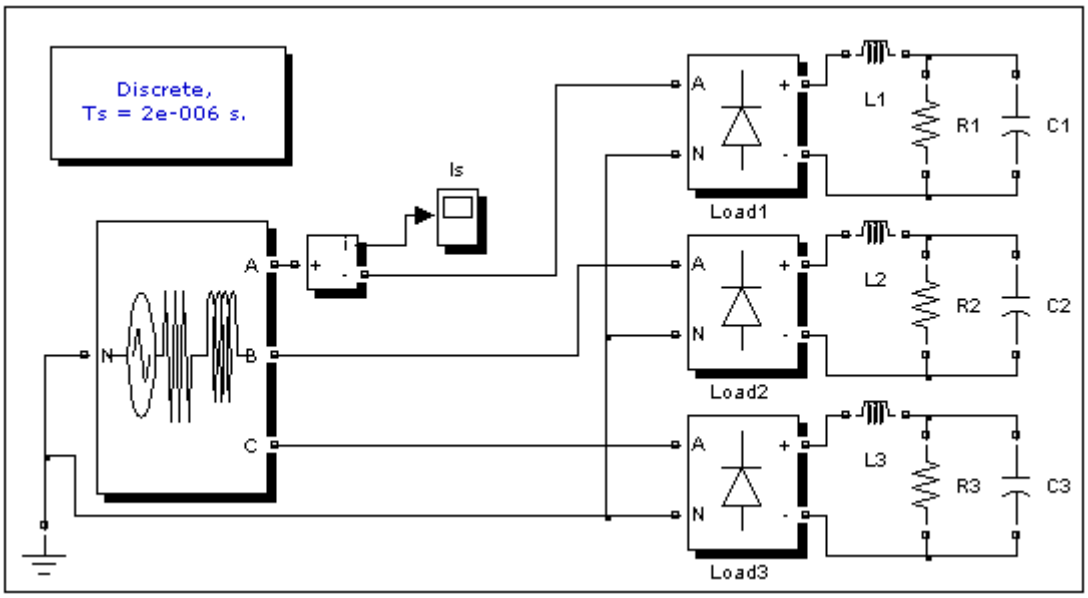
(d)

Fig A.1: Linear load connected to a three-phase system

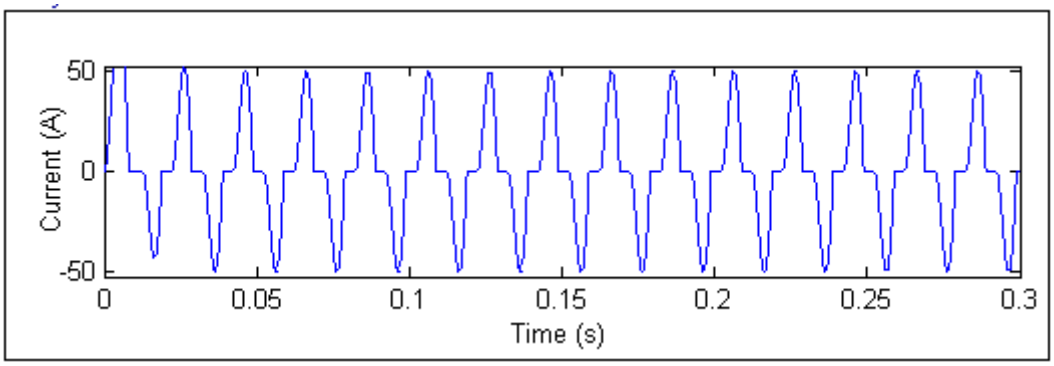
(a) Power circuit with a resistive load; (b) Power circuit with a resistive/inductive load; (c) phase current; (d) Harmonic spectrum of the phase current

A.2 Three single-phase non-linear loads connected to a three-phase four-wire system

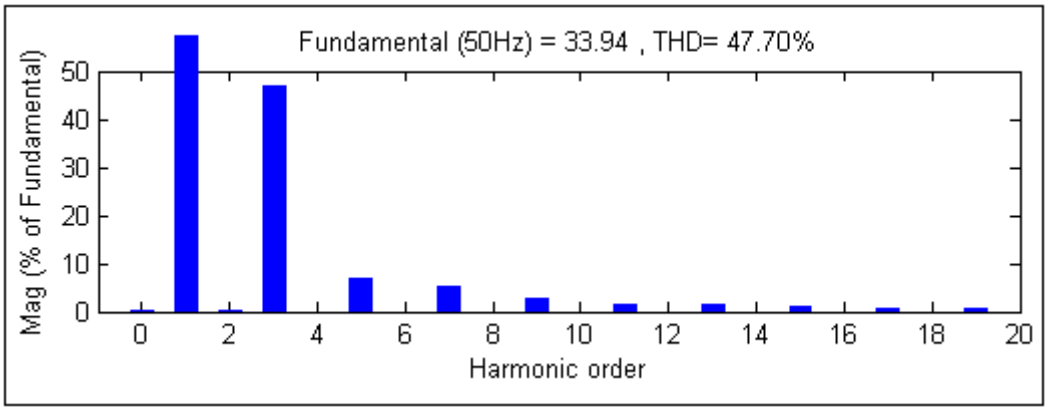
The power stage of three identical single-phase diode bridge rectifiers is shown in Fig. A.2. From the simulation results, it can be seen that the phase current THD about 47.7 % and the presence of large third order harmonic currents in the neutral conductor.



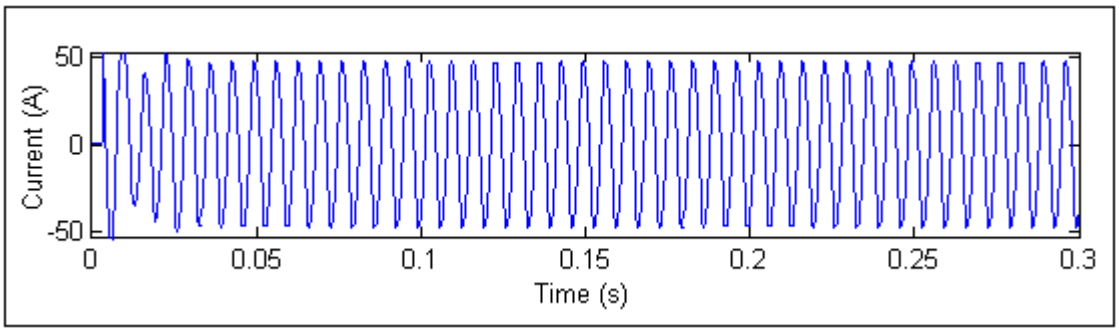
(a)


Current (A)
50
0
-50
0
0.05
0.1
0.15
0.2
0.25
0.3
Time (s)

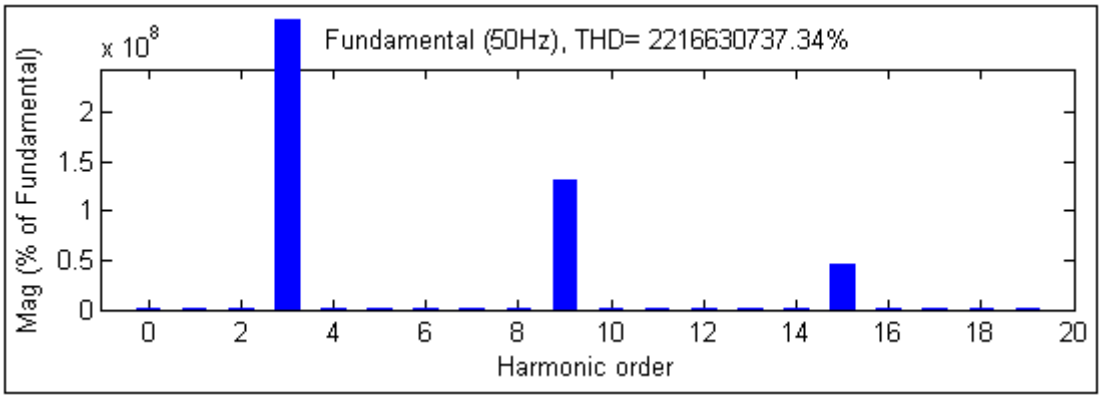
(b)


Fundamental (50Hz) = 33.94 , THD= 47.70%
Mag (% of Fundamental)
50
40
30
20
10
0
0
2
4
6
8
10
12
14
16
18
20
Harmonic order

(c)


Current (A)
50
0
-50
0
0.05
0.1
0.15
0.2
0.25
0.3
Time (s)

(d)


x 10^8
Fundamental (50Hz), THD= 2216630737.34%
Mag (% of Fundamental)
2
1.5
1
0.5
0
0
2
4
6
8
10
12
14
16
18
20
Harmonic order

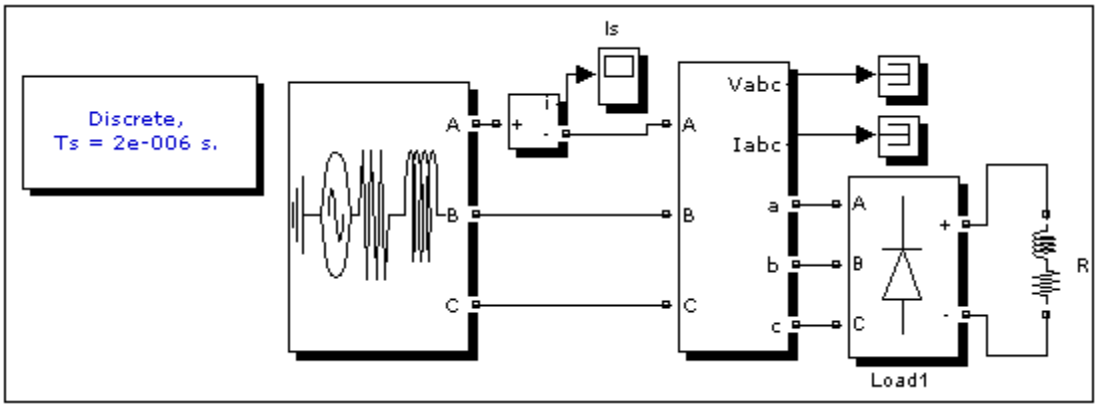
(e)

Fig A.2: Three single-phase diode bridge rectifiers with resistive loads and smoothing inductor/capacitor

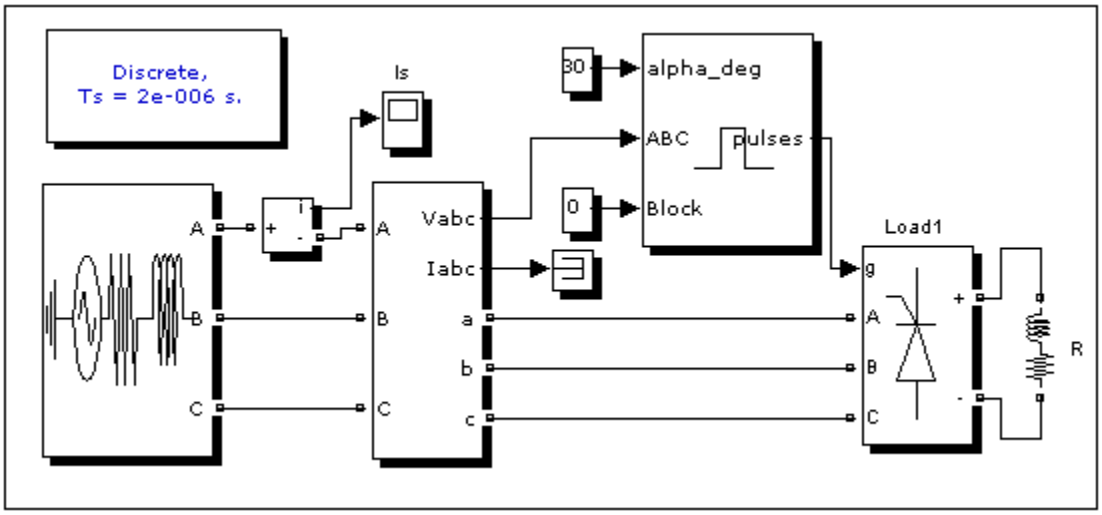
(a) Power circuit; (b) Phase 'a' current; (c) Harmonic spectrum of phase 'a' current; (d) Neutral conductor current (e) Harmonic spectrum of the neutral conductor current

A.3. Three-phase non-linear loads connected to a three-phase three-wire system

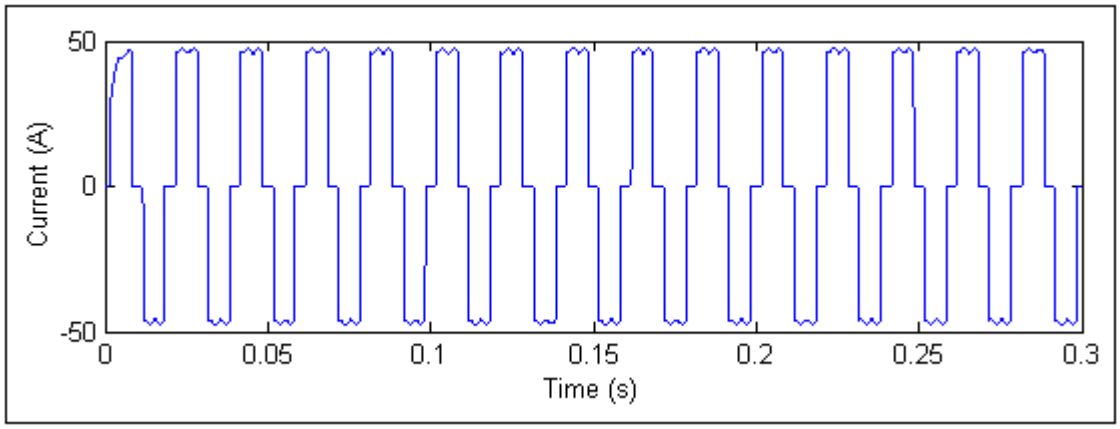
A three-phase diode and thyristor rectifier with a resistive and inductive loads is shown in Fig A. 3. The the phase current THD is 30.63 % as plotted in Fig A. 3 (d), the same results obtained for diode as well as thyristor rectifier.



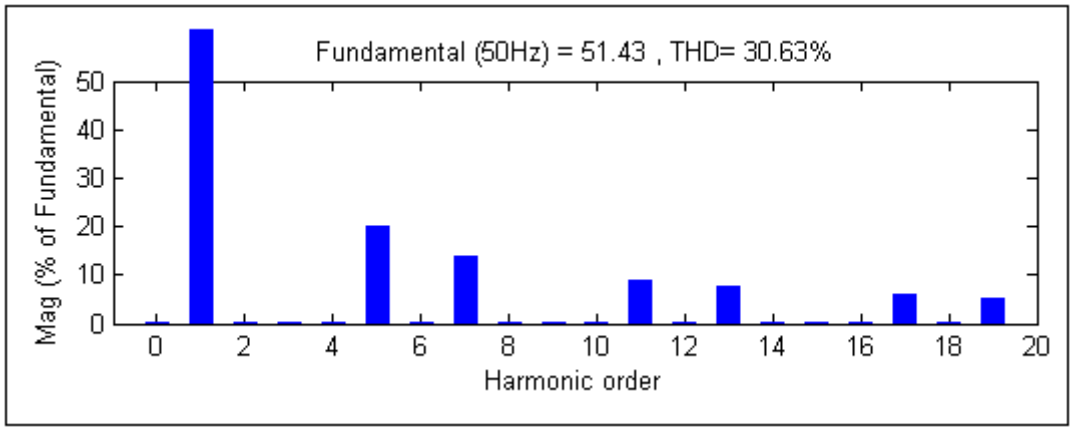
(a)



(b)



(c)



(d)

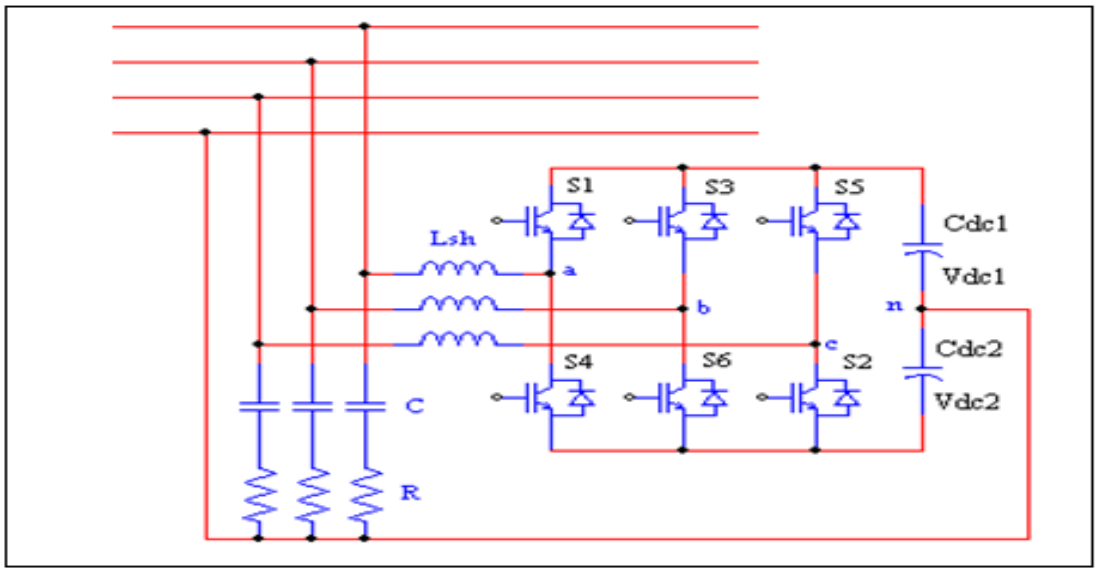
Fig A.3: Three-phase diode and thyristor bridge rectifiers with resistive load and smoothing inductor

(a) Power circuit with diode bridge rectifier; (b) Power circuit with thyristor bridge rectifier; (c) phase 'a' current; (d) Harmonic spectrum of current of phase 'a'

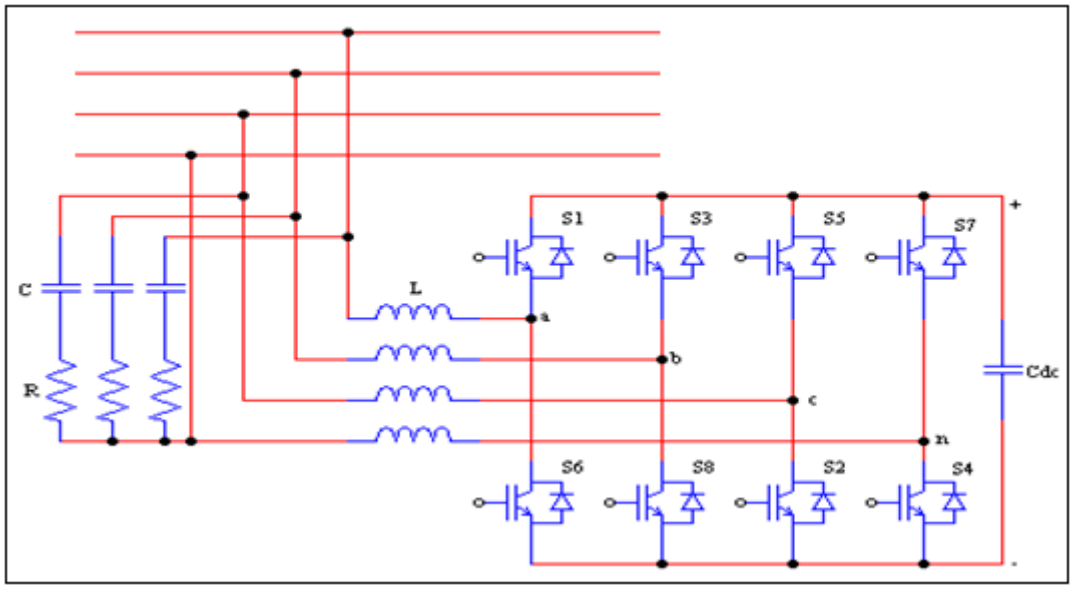
A.4. Study bakground and review

As non-linear loads are widely employed in PDNs which cause unbalance and draw excessive neutral current, conventional inductance-capacitance and/or resistance PPFs have been used to reduce the harmonics and to improve the power factor at the supply end. These PPFs are economical, simple and efficient filtering devices but they are bulky, load dependent, inflexible and also may cause resonance to power system networks [1], [11], [25], [33] [34], [92], [120]. The shortcomings of PPFs and remarkable progress in power electronics had spurred the interest in APFs to provide

better filtering performance. Three-phase three-wire APFs were established in around 1970s, but they could not be used in real power system networks because of unavailability of high-power high-speed switching devices [120]. In recent years the development in high power semi-conductor switches spurred the manufactures to put APFs in the market. A major factor in advancing the APF technology is the use of some of the improved self-commutating fast switching semi-conductor power devices such as IGBTs, metal oxide semiconductor field-effect transistors (MOS-FETs) and gate turn-off thyristors (GTOs) [14], [58]. Some of the possible multiple functions of APFs are harmonic filtering, reactive power compensation, power factor correction, voltage regulation, loads balancing, voltage-flicker mitigation etc. Besides, APFs are superior in filtering performance, smaller in physical size, and more flexible in application as compared to traditional PPFs [14], [92], [120]. In three-phase four-wire systems, the traditional three-phase three-wire APFs are inadequate to overcome harmonics pollution, to compensate reactive power and to improve the power factor, as well as to minimize the neutral current. To overcome the above disadvantages three-phase four-wire APFs are introduced in around 1980s [64]. APFs according to their connection to the power system networks are mainly divided into three kinds as shunt APFs (SAPFs), series APFs and hybrid APFs (HAPFs) [11]. In this thesis, a SAPF is adopted and its performance is analyzed in three-phase four-wire distribution networks. Basically, three-phase four-wire VSI based SAPF has two main types depending on the connection of neutral wire. In the first type the neutral wire is connected to the midpoint of the DC bus capacitor by means of a capacitor divider, while in the second type the neutral wire is connected to the additional fourth leg provided by the power semi-conductor devices [35], [66], [67], [70]-[72] [121], [122]. Figs A.4. (a) and (b) shows the two topologies of three-phase four-wire VSI based SAPF. A three-phase four-wire SAPF is adoptable to compensate reactive power, to mitigate positive, negative and zero-sequence harmonics as well as possible improvement of the power factor on the supply side.



(a)



(b)

Fig A.4: (a) VSI based three-phase, four-wire SAPF using three-leg split capacitor; (b) VSI based three-phase, four-wire SAPF using four-leg

A.5. Harmonics

The main target of any electric power system is to supply reliable power with high quality at minimum possible cost. The growing use of non-linear devices in power system causes distortion of the current and consequently the voltage waveforms. These current and voltage distortions induced one of the most significant static power

quality problems known as harmonics. Harmonics result in degradation of the power quality of other electrical equipments connected to the same power supply. It is well known that continuous operation with excessive harmonic current leads to increased voltage stress and excessive temperature rises, resulting in a much reduced power plant equipments useful life. For instance, a 10 % increase in voltage stress will result in 7 % increase in temperature, reducing the life expectancy to 30 % [10], [123], [124]. The current harmonics are defined as undesirable currents with frequencies that are an integral multiple of the fundamental frequency of the system. The harmonic pollution caused by static power converters is a serious problem in power systems [125]. Harmonics in power systems are not new, but recently the effects of harmonics have gained concern awareness. Due to deteriorating power quality, some electrical and electronic equipments are affected by the harmonics causing malfunction and failure. [121], [126]. A detailed study on the problem of harmonics in power system is based on:

i. Generation of harmonics.
ii. Power quality degradation due to the harmonics.
iii. Propagation, modelling, and analysis of harmonics.
iv. Suppression of harmonics using PPFs and APFs.
v. Measurement of harmonics.

In a balanced three-phase system, the fundamentals and $(3H \pm 1)^{th}$ harmonics, where H is the order of harmonic, all produce voltages displaced by 120^{o} mutually. The positive sequence harmonics have order (3H+1) and the negative sequence harmonics have order (3H-1). The third, ninth, $3n^{th}$ harmonics are called as zero sequence harmonics which have voltages in three phases that are co phased in time [4]. The converter type and control method will play a crucial role in the order and magnitude of harmonics. For example in single-phase voltage-source inverters, the output voltage waveform typically consists only of odd harmonics. The harmonic spectrum depends on the switching frequency and the control method. Several instruments are used to measure harmonic spectrum, where the signals are usually transformed from time domain to frequency domain by means of discrete Fourier transform algorithm to evaluate distortion contents of different spectral components [117].

A.5.1 Phase sequence of harmonics in balanced distribution network

The voltages of phases ‘a’, ‘b’ and ‘c’ with respect to their harmonic sequences can be expressed as in (A.1) to (A.3).

$$v_{an} = V_1 \cos(\omega t) + V_3 \cos(3\omega t) + V_5 \cos(5\omega t) + ... + V_n \cos(n\omega t) \quad \text{(A.1)}$$

$$v_{bn} = V_1 \cos(\omega t - 2\pi/3) + V_3 \cos 3(\omega t - 2\pi/3) + V_5 \cos 5(\omega t - 2\pi/3) + ... + V_n \cos n(\omega t - 2\pi/3) \quad \text{(A.2)}$$

$$v_{cn} = V_1 \cos(\omega t + 2\pi/3) + V_3 \cos 3(\omega t + 2\pi/3) + V_5 \cos 5(\omega t + 2\pi/3) + ... + V_n \cos n(\omega t + 2\pi/3) \quad \text{(A.3)}$$

simplifying (A.1) to (A.3) as in (A.4) to (A.6),

$$v_{an} = V_1 \cos(\omega t) + V_3 \cos(3\omega t) + V_5 \cos(5\omega t) + ... + V_n \cos(n\omega t) \quad \text{(A.4)}$$

$$v_{bn} = V_1 \cos(\omega t - 2\pi/3) + V_3 \cos(3\omega t) + V_5 \cos(5\omega t + 2\pi/3) + ... + V_n \cos n(\omega t - 2\pi/3) \quad \text{(A.5)}$$

$$v_{cn} = V_1 \cos(\omega t + 2\pi/3) + V_3 \cos(3\omega t) + V_5 \cos(5\omega t - 2\pi/3) + ... + V_n \cos n(\omega t + 2\pi/3) \quad \text{(A.6)}$$

The three fundamental components form a balanced three-phase set of phasors rotate at the fundamental electrical angular velocity ω rad/s with positive sequence *a-b-c*. Also the fifth harmonic phasors form a balanced set rotate at 5 ω rad/s, but with negative sequence a-b-c. The third harmonic components rotate at 3 ω rad/s and all them are in phase to have zero phase sequence. The phasors sequences are shown in Fig A.5.1.

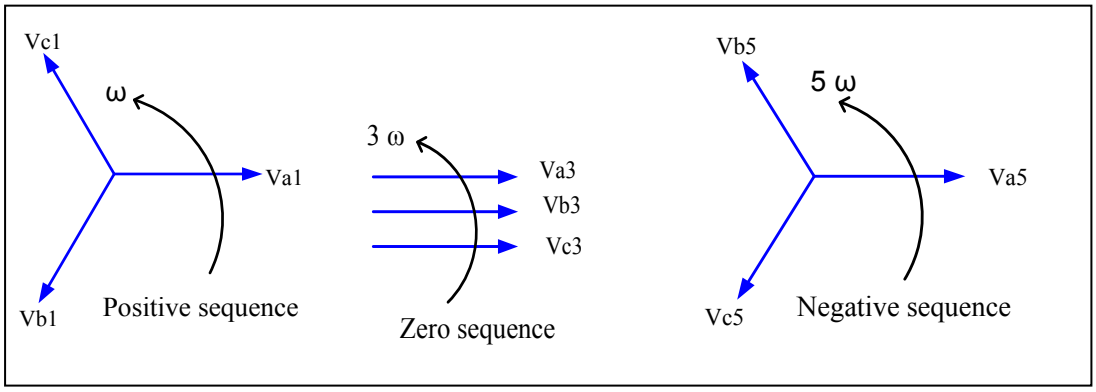


Fig A.5.1: Harmonic phasors

The positive, negative and zero sequence harmonics can be analyzed as follows:

$$V_{a1} + V_{b1} + V_{c1} = 0 \tag{A.7}$$

$$V_{a3} + V_{b3} + V_{c3} = 3V_{a3} \neq 0 \tag{A.8}$$

$$V_{a5} + V_{b5} + V_{c5} = 0 \tag{A.9}$$

From equations (A.7) to (A.9) it can be concluded that, the sum of positive and negative sequence harmonics in a balanced three-phase system is equal to zero, but the sum of zero sequence harmonics is not equal zero but exist in the system [127].

A.5.2 Balanced network harmonic components

In a wye-connection, the actual instantaneous line-to-line voltage will satisfy the following equation

$$v_{ab} = v_{an} - v_{bn} \tag{A.10}$$

Similarly the fundamental component of voltage

$$v_{ab1} = v_{an1} - v_{bn1} \tag{A.11}$$

However, the third harmonic component is given by (A.12)

$$v_{ab3} = v_{an3} - v_{bn3} = 0 \tag{A.12}$$

It is found that the third harmonic component of the voltage will not appear between two lines in a balanced system.

In the balanced three-phase network without a neutral conductor the line currents satisfy the equation as in (A.13)

$$i_a + i_b + i_c = 0 \tag{A.13}$$

As $i_{a3} = i_{b3} = i_{c3}$, it can be concluded that in a three-wire balanced system, no third harmonic currents can flow in the lines. This is valid for both wye-connection and delta connection of the loads. However, the third harmonic components in delta connected load now circulate a triplen current in the closed delta without appearing in the lines.

If a neutral wire connection is provided (four-wire system), the neutral current is given by the following equation

$$i_n = i_a + i_b + i_c = +3(i_3 + i_9 + ...) \quad \text{(A.14)}$$

One of benefits of a three-phase four-wire system is to prevent oscillation of the neutral voltage [128].

A.6. Total harmonic distortion (THD)

To study the impact and damage caused by harmonics pollution in power systems various harmonic standards were established. The percentage harmonic distortion standards can be categorized into two groups. The first group gives the harmonic limitation in an electric power supply or at PCC (system side standard, IEEE standard), and the second group of standard restricts the harmonic components coming out of the equipment (load-side standard, IEC-555) [129]. One of the most commonly used indexes in harmonic analysis is the THD.

Any distorted periodic signal can be represented by a sum of sinusoids of discrete frequencies. Actually the frequencies are multiple of the fundamental frequency. The current drawn by a non-linear load based on Fourier series can be expressed as follows:

$$i_L = I_0 + I_1 \sin(\omega t + \phi_1) + I_2 \sin(2\omega t + \phi_2) + I_3 \sin(3\omega t + \phi_3) + ... + I_h \sin(h\omega t + \phi_h) \quad \text{(A.15)}$$

Equation (1.15) can be rewritten as:

$$i_L(\omega t) = I_0 + \sum_{n=1}^{\infty} I_n \sin(n\omega t + \phi_n)$$

(A.16)

Equation (A.16) can be subdivided into fundamental and harmonic components as in (A.17), considering only the odd harmonics and neglecting zero sequence component (i_0)

$$i_L(\omega t) = I_{1max} \sin(\omega t + \phi_1) + \sum_{H=3,5,7}^{\infty} I_{Hmax} \sin(H\omega t + \phi_H) \quad \text{(A.17)}$$

where

I_{1max} = maximum value of fundamental component of the load current

I_{Hmax} = maximum value of individual harmonic components of the load current

The THD with respect to the current can be expressed as:

$$THD_i = \sqrt{\frac{\sum_{H=2}^{\infty} I_H^2}{I_1^2}} * 100\% \tag{A.18}$$

where I_1 and I_H are fundamental and harmonic currents, respectively. Actually THD is used to measure the deviation of a periodic waveform containing harmonics from a perfect sine wave. The THD for a fully sinusoidal waveform at a fundamental frequency will be equal to zero. Moreover THD can be used in low, medium and high voltage systems to measure the distortion of the line currents. For proper operation of the power system the THD should be not more than 5 % as recommended by the IEEE-519 power quality standards. [4], [130].

A.7. Zero-sequence components through the neutral conductor

The zero-sequence triplen harmonics, the 3rd and its odd multiples, add together creating a primary source of excessive neutral current in a three-phase four-wire system. A distribution system which provides neutral wire connection has become more important in recent years. Gamow and Teller in 1937, first suggested neutral current interaction but the real discovery of the neutral current interaction was in 1973 based on some conducted experiments as reported in [131].

Under balanced sinusoidal conditions, the neutral current will be equal to zero. If there is some phase current unbalance, the neutral current will exist but with small values that might not cause significant problems to the distribution system [10].

A.7.1 The main application requiring a neutral terminal connection

The main applications requiring a neutral terminal connection are follows:

i. Distributed generation (DG) systems connected to the AC utility grid power generators, usually based on renewable energy sources, such as wind power, photovoltaic and fuel-cells.

ii. Uninterruptible Power Supplies (UPS) to provide high quality AC currents to the users.
iii. Active power filtering of harmonics [66].

A.7.2 Neutral current contribution by single-phase non-linear loads

A number of single-phase non-linear loads (PC, fluorescent lamps, fax machines, AC/DC converters, etc.) used in industrial installions inject harmonic currents, which flow into the neutral wire. In balanced three-phase systems only the third-order harmonic currents flow into the neutral conductor and are three times as high as the corresponding harmonics in phase currents. System unbalances, such as supply-voltage unbalance and load unbalance, cause the loss of positive and negative-sequence symmetry in the positive and negative-sequence harmonics. Consequently, the sum of these harmonics in the neutral conductor is not equal to zero which can increase the root-mean-square (RMS) value of the neutral conductor current. In order to conduct studies on this harmonic problem, converter models are necessary to calculate the harmonic currents [6], [132]-[137].

A.7.3 Main drawbacks of high neutral current

When the neutral current is excessive significant problems are associated with the system such as

i. Neutral conductor damage due to improper sizing.
ii. Excessive neutral-to-earth voltage (NEV) due to the voltage drop caused by the neutral current.
iii. Increased levels of electromagnetic forces.
iv. Overheating of transformers that may result in insulation failure.
v. Increased short-circuit level at site and consequently damage to circuit breaker due to raise in resultant total current [10].

A.7.4 Methods used to minimize neutral current

In general two corrective measures of the neutral current are used with active filtering.

i. Using a three-phase three-wire inverter with a special transformer connection (delta/Yg, isolation transformer). Since the isolation transformer is bulky, heavy, and costly, it is not implemented in many applications, especially in mobile generation.
ii. Using a four-wire inverter based SAPF without isolation transformer. A four-wire transformerless inverter is more preferable than transformer type considering the cost of active filter.

There are two types of four-wire transformerless inverter topologies applicable to SAPF: a three-leg inverter with split dc bus and a four-leg inverter. A three-phase three-leg inverter with split DC-bus is one topology to implement three-phase four-wire system with a neutral point seen by the load. Compared to a three-phase three-wire system, it does not have the isolation transformer and provides three-dimensional control. Compared to a three-phase four-leg topology, it saves two power switches and reduces control complexity. Nevertheless, it has DC-bus voltage unbalance problem. The second configuration is known as four-leg or four-pole switch type where the fourth pole is used to stabilize the neutral of the SAPF [10], [36], [48], [138].

A.8. Reactive power compensation

SAPF is considered as a viable solution for the compensation of reactive power drawn by the non-linear loads. The inductive reactive power generally results from inductive loads such as welder or induction furnace, power transformer, induction motor and lighting ballasts. The existence of inductive reactive power in power system leads to very poor power factor and the system has the following disadvantages:

i. Increase in the capacity of transmission, substation, and distribution systems.
ii. Poor voltage regulation.
iii. Increase of electricity bills.
iv. Extra losses in feeder cables.
v. Decrease of effective capacity of cables and degrading the efficiency of distribution power.

The existence of inductive reactive power in PDNs is not included in the electric bill as consumption of reactive power, but results as an incremental charge of electricity bill by causing losses in the form of dissipation power at the load side [37], [124], [139]. The compensation of reactive power is accomplished by generating or absorbing the same amount by using SAPF connected at the PCC between the utility and the loads. However, in real applications, complete mitigation of the reactive power with the SAPF is not simple because the reactive power may be much higher than the harmonic power, and thus the SAPF loses its initial purpose, again with the same consequence of an increased cost. It is possible to achieve the reactive power mitigation without increasing the size of the DC-capacitor of the SAPF. Furthermore, by reducing the reactive power together with reduction in harmonics results in better power factor, which consequently lowers the electricity bill [140].

A.9. Methods of elimination of harmonics

The presence of non-linear loads in the PDNs is the main cause for current harmonics which in turn produce voltage harmonics [140]. The percent distortion of waveforms of the current and voltage absolutely depend upon the size of the non-linear loads of the system, the type of equipment, and the source impedance. When the non-linear loads on the system increase, consequently the voltage distortion increase. The existence of voltage harmonics are not desirable in PDNs as they cause additional losses and leads to malfunction of sensitive equipments [3].

The traditional solutions proposed to eliminate harmonic currents are by using over dimensioned electrical equipment, three-phase transformer special connections to eliminate the triplen and its proportional harmonics, and the connection of passive elements but they have more disadvantages than advantages [141]. Conventionally passive elements based L-C type PPF is widely used to limit harmonic propagation, improve power quality, reduce harmonic distortion, and provide reactive power compensation simultaneously. Also there are several techniques which have been developed to mitigate current harmonics as reported in [27], [142], [143]. A better

approach is effective active filtering, generally, incorporated with the harmonic mitigation equipment which can reduce the harmonic generation at source. Unlike

PPF, SAPF represents a remarkable trend for successful current harmonics suppression in PDNs, and it is accomplished in two ways. One method as a local solution by connecting SAPF directly at the load end and the other as a global solution by connecting it at the PCC as illustrated in Fig A.9 [36], [140], [144].

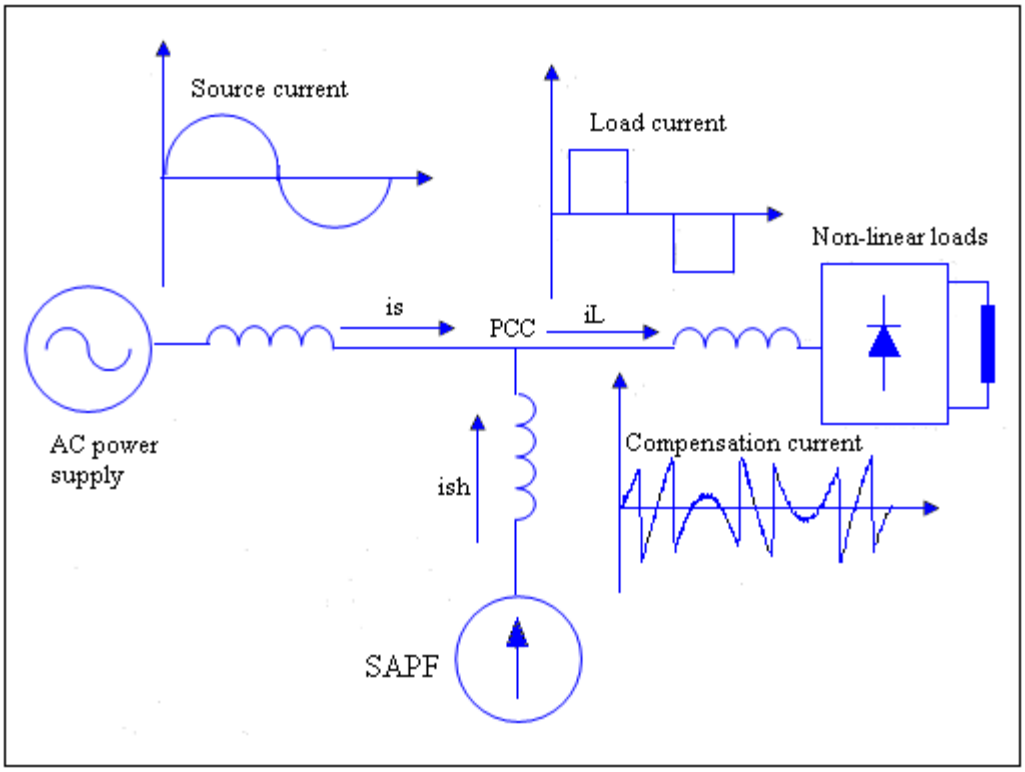


Fig A.9: Compensation characteristics of SAPF connecting at the PCC

Basically SAPF can suppress the current harmonics by generating a harmonic spectrum which has the same magnitude and opposite in phase of the current harmonics drawn by the non-linear loads and injects it at the PCC, thereby forcing the source current to become nearly sinusoidal [39] and source end power factor close to unity. Actually the PWM switching frequency for VSI is chosen to be high and the switching frequency harmonics in the compensation currents are suppressed by a small L-C low-pass filter [4]. The control strategy applied to the SAPF to calculate the reference currents plays a very important role in the characteristics and efficiency of harmonics compensation and its effectiveness [39].

A.10. Pulse width modulation (PWM) patten generation techniques

The pulse Width Modulation, PWM is a method of providing generated switching pulses of varying widths to an inverter in order to synthesize, on average, a desired voltage or current waveform (mostly a sine wave) at its output terminals. PWM can control the amount of power transferred to a certain load by simply controlling the width of the pulses. One of the reasons for using PWM technique is to reduce the total power delivered to a load without resulting in loss, which normally occurs when a power source is limited by a resistive element. The PWM control is considered as a key technology for SAPF. The widely used PWM modulation techniques for following current reference template can be grouped into three schemes as hysteresis band technique, triangular carrier technique and periodical sampling technique [61], [70].

A.10.1 Hysteresis control technique

The hysteresis current control technique with fixed band is based on deriving the switching signals of the inverter from the comparison of the current error within the hysteresis band. Appropriate stability, fast response, high accuracy, simple operation, inherent current peak limitation and load parameters variation independency make the hysteresis current control as one of the best current control schemes of VSIs. In this approach the current error (difference between the inverter reference current and inverter feedback current), is operated by the hysteresis current controller to generate the gating pulses which activate the inverter power switches in a manner that reduces the current error [40].

The hysteresis-rule-based carrierless PWM current controller shown in Fig A.10.1 is used to generate the PWM gating signals for the IGBTs of the compensator. The error signals from the three-phase reference currents (i_{fa}^{*}, i_{fb}^{*} and i_{fc}^{*}) and sensed currents (i_{sha}, i_{shb} and i_{shc}) of the inverter as shown in Fig. A.10.1 are sent to a hysteresis band comparator (relay) to generate the PWM gating signals. The compensator injects the desired compensation currents to the system to meet the requirement of the reactive power of the load and to suppress the harmonic currents of

the three phases of the AC source. Consequently balanced three-phase sinusoidal source currents appear in the PDN at all operating conditions improving the power factor to unity [28], [124].

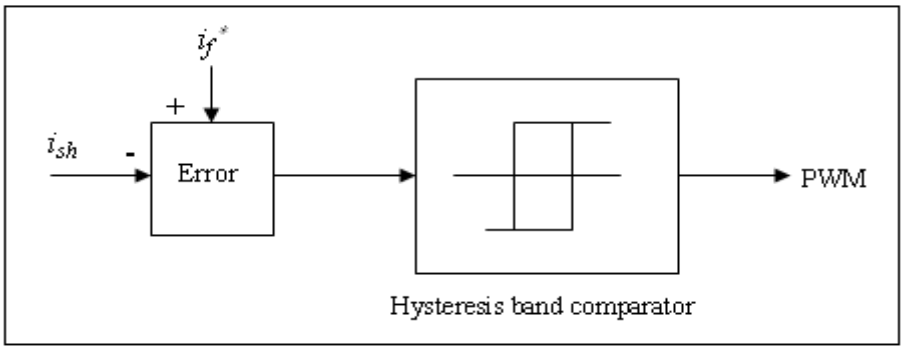


Fig A.10.1: Hysteresis band technique for PWM pattern generation

For hysteresis control the phase output current of the compensator is fed back to compare with the reference current. Whenever the phase current exceeds the upper band, the upper switch of the VSC leg will be turned ON while the lower switch will be turned OFF. If phase current falls below it is vice-versa. This method is indeed the easiest to be implemented as compared to other methods discussed in the next sections.

A.10.2 Triangular carrier (TC) technique

Fig A.10.2 shows the triangular carrier (TC) technique which compares the error between the i_{sh} and i_f^* with a fixed frequency, fixed amplitude triangular carrier wave. A proportional integral regulator (PI) provides the static and dynamic properties to the feedback loop. This method is more attractive than the other two methods in its implementation since the gains of the PI controller can be selected properly [129], [130].

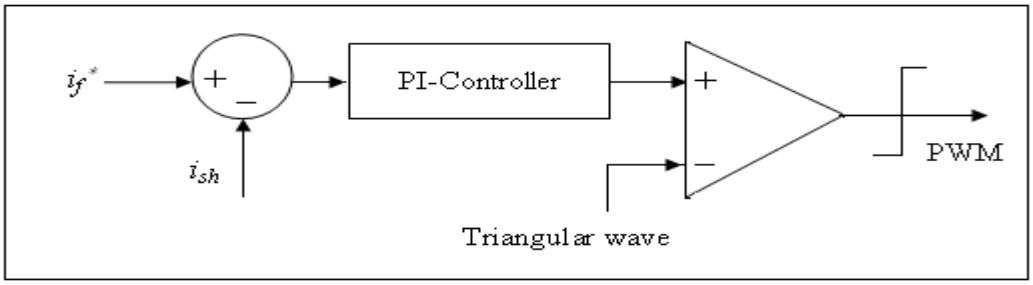


Fig A.10.2: Triangular carrier wave technique for PWM pattern generation

A.10.3 Periodical sampling (PS) technique

This method employs a clock of fixed frequency to control the power switches of the VSI. An error signal, generated from a measurement of the line and reference currents, is used to modulate the clock frequency and generate the PWM pattern using a comparator and D flip-flop, as shown in Fig A.10.3. The minimum time between switching is limited by the clock frequency [129], [130], [27].

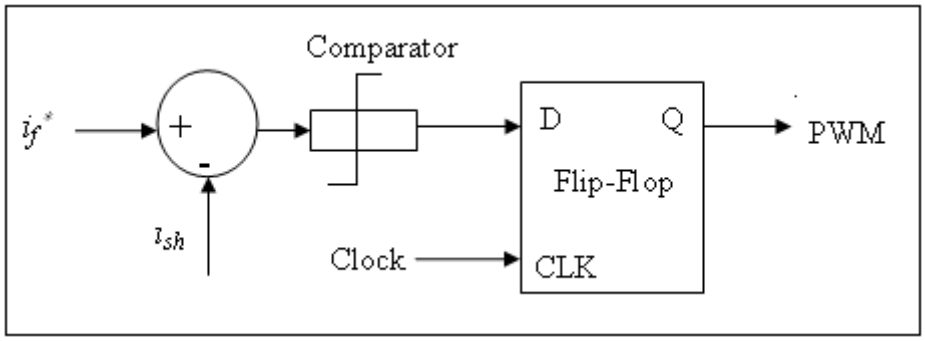


Fig A.10.3: Periodic sampling technique for PWM pattern generation

Appendix B

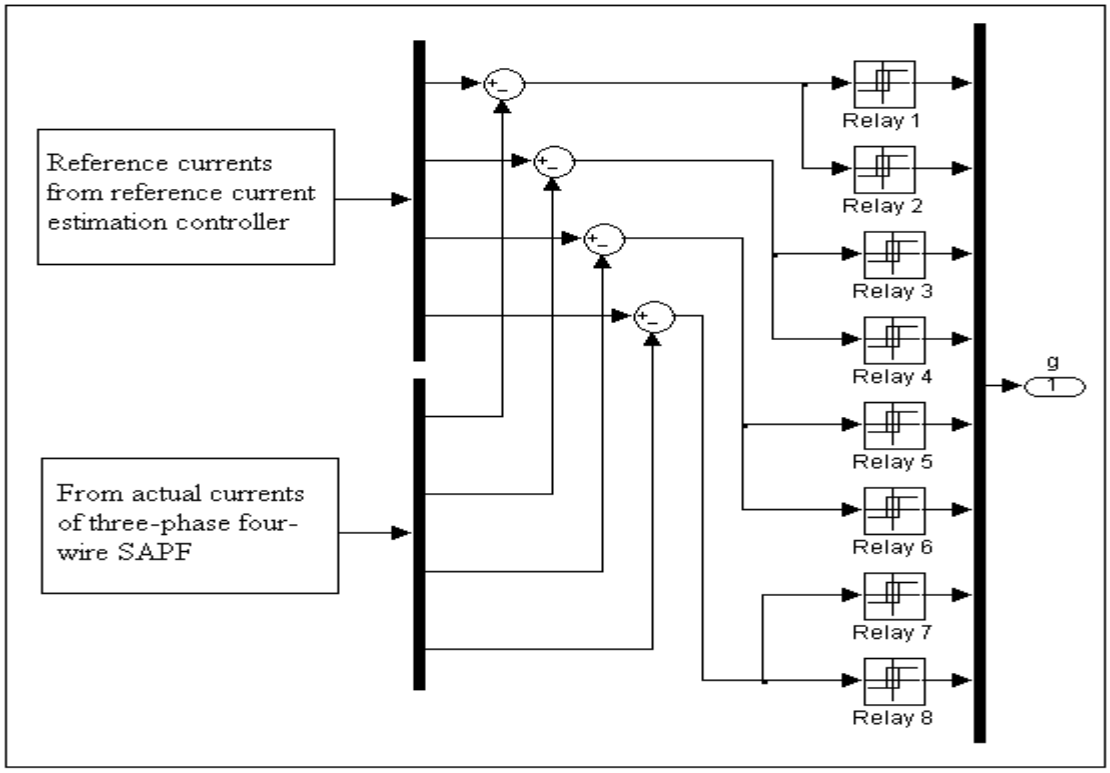


Fig. B.1: SIMULINK model of hystersis band current controller

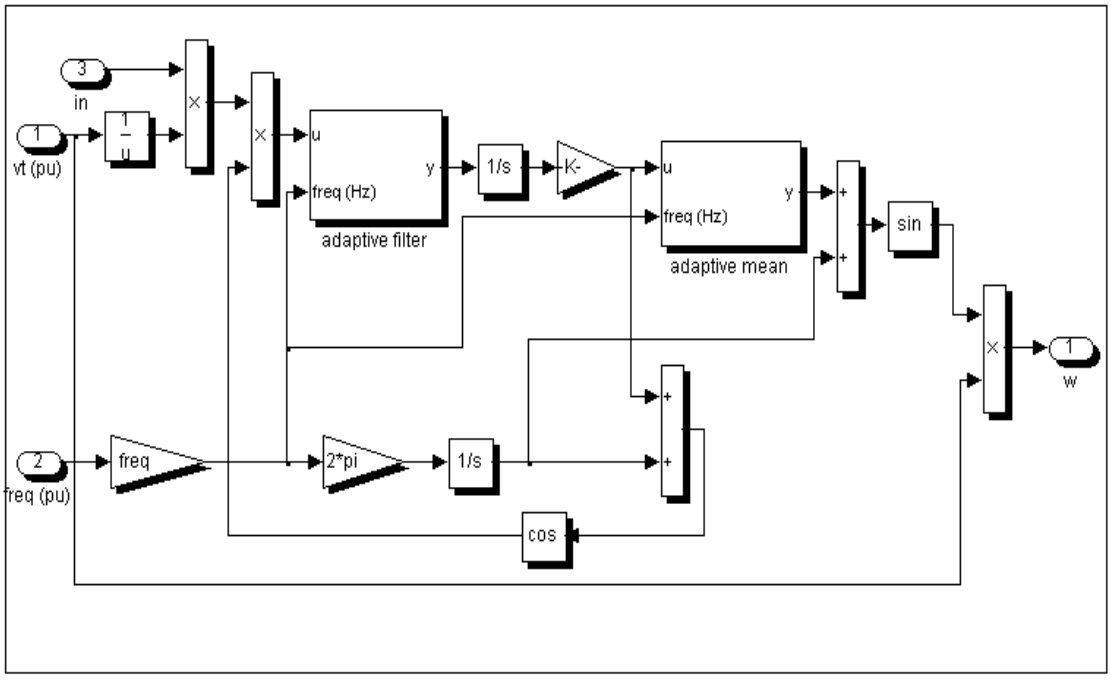


Fig. B.2: SIMULINK model of PLL of the *a-b-c* theory based controller

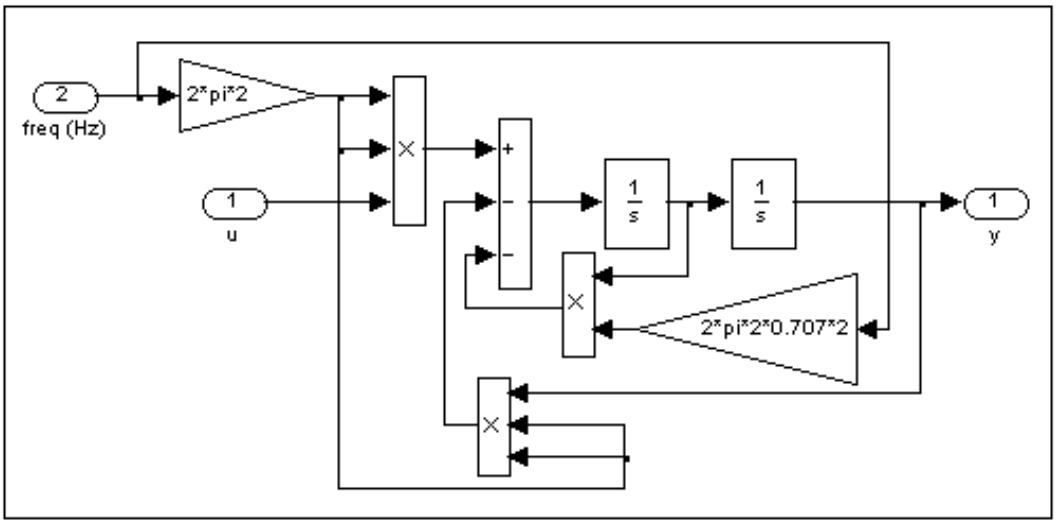


Fig. B.3: SIMULINK model of adaptive filter of PLL

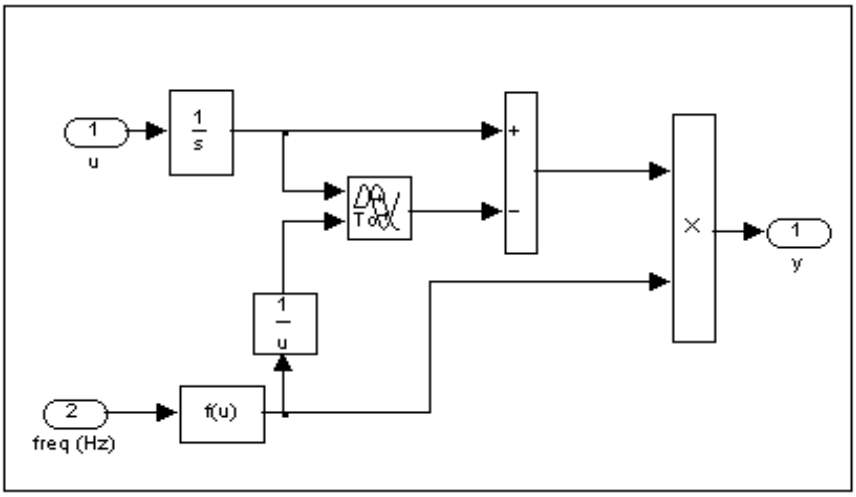


Fig. B.4: SIMULINK model of adaptive mean of PLL

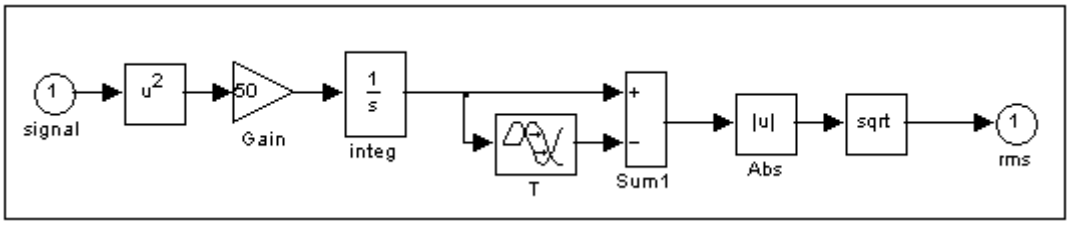
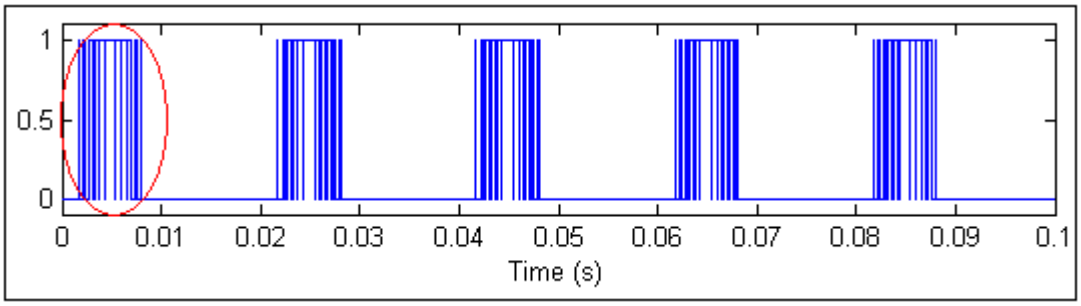


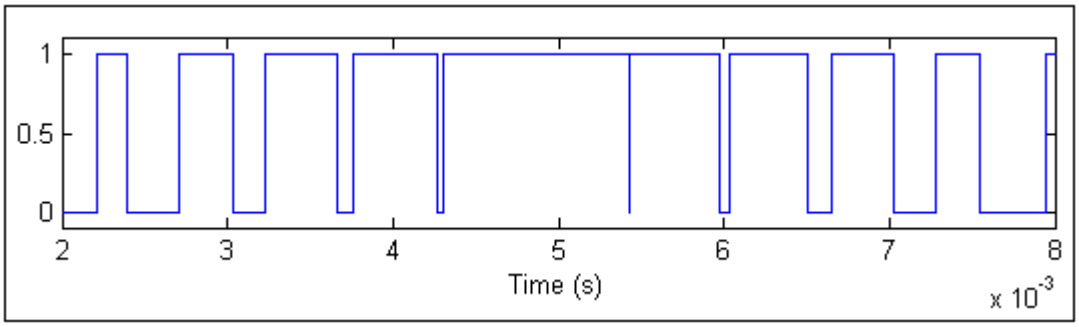
Fig. B.5: SIMULINK model of RMS block of the *a-b-c* theory based controller

Appendix C

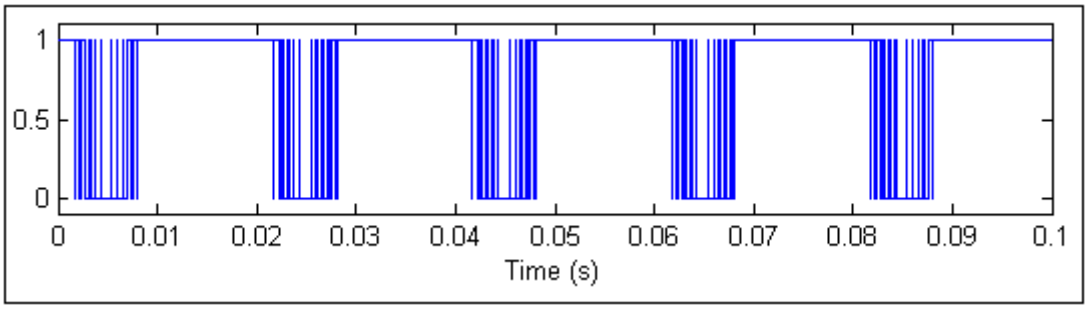
Gating signals and output voltages of five-level CHB-VSI

The PWM gating signals of the five-level CHB-VSI for phase 'a' are shown in Fig C.1: (a) to (h). These gating signals are controlled by comparing four carrier signals with the sinusoidal modulation signal. The gating signals are produced by the relational operator. The output signal from the relational operator is used to change the switching status (ON or OFF) of IGBTs. Figs C.2 to C.9 show the simulated line-to-line and phase voltage waveforms of the five-level CHB-VSI operating under the condition of (m_f = 70, ma = 0.8, f = 50 Hz, and f_c = 3500 Hz) and by using both PS-SPWM and LS-SPWM (IPD, APOD and POD) modulation techniques.

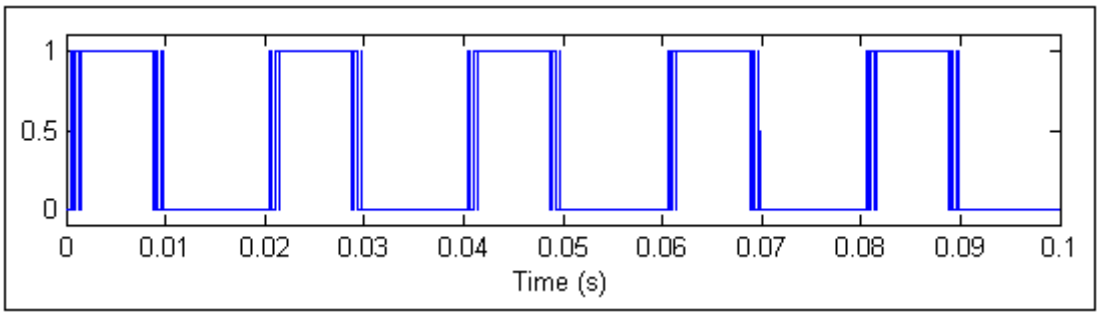




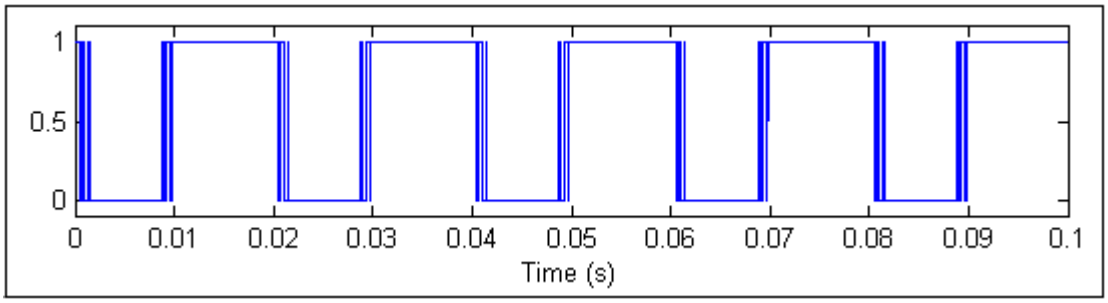
(a)



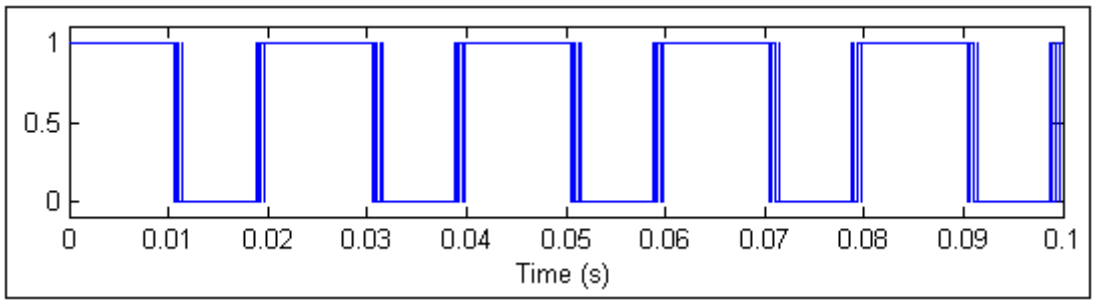
(b)


1
0.5
0
0
0.01
0.02
0.03
0.04
0.05
0.06
0.07
0.08
0.09
0.1
Time (s)

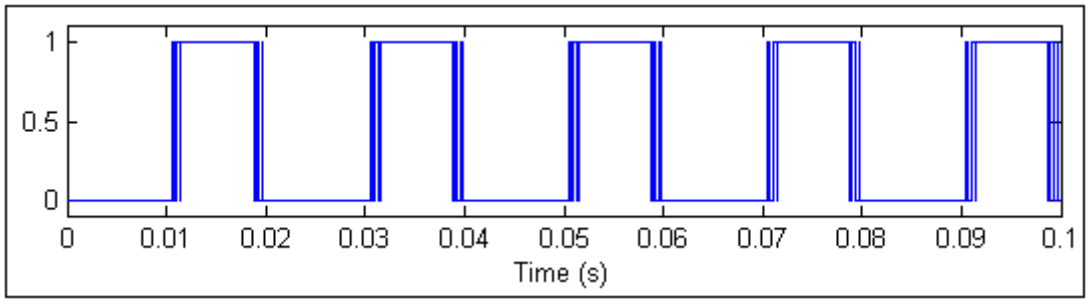
(c)


1
0.5
0
0
0.01
0.02
0.03
0.04
0.05
0.06
0.07
0.08
0.09
0.1
Time (s)

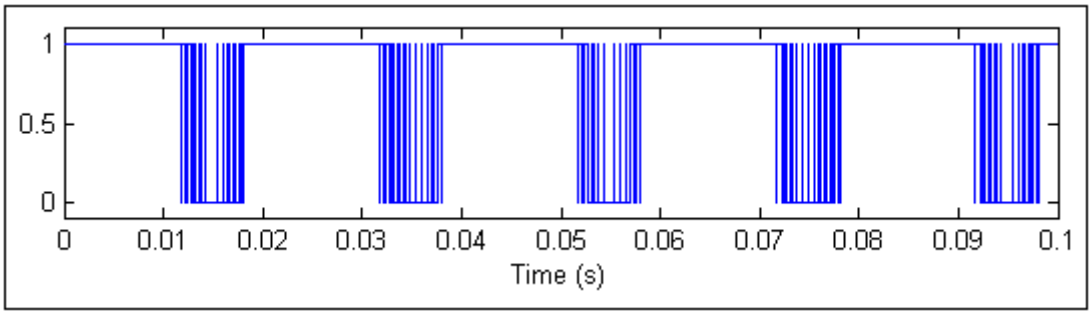
(d)


1
0.5
0
0
0.01
0.02
0.03
0.04
0.05
0.06
0.07
0.08
0.09
0.1
Time (s)

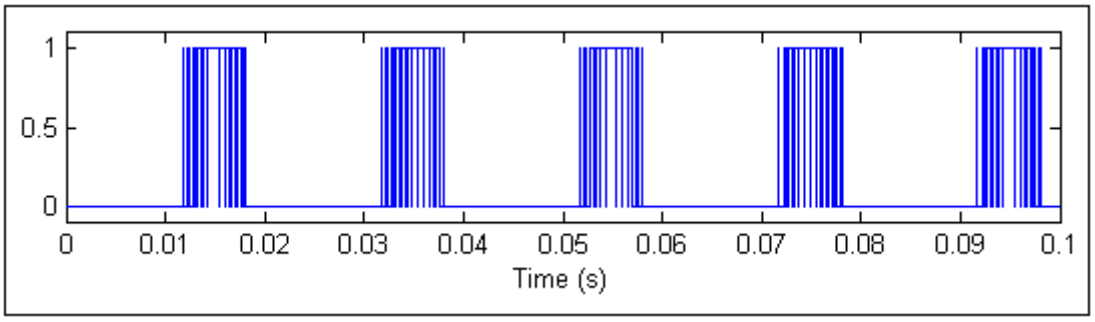
(e)


1
0.5
0
0
0.01
0.02
0.03
0.04
0.05
0.06
0.07
0.08
0.09
0.1
Time (s)

(f)



(g)



(h)

Fig C.1: (a) to (h) PWM gating signals of five-level CHB-VSI based SAPF

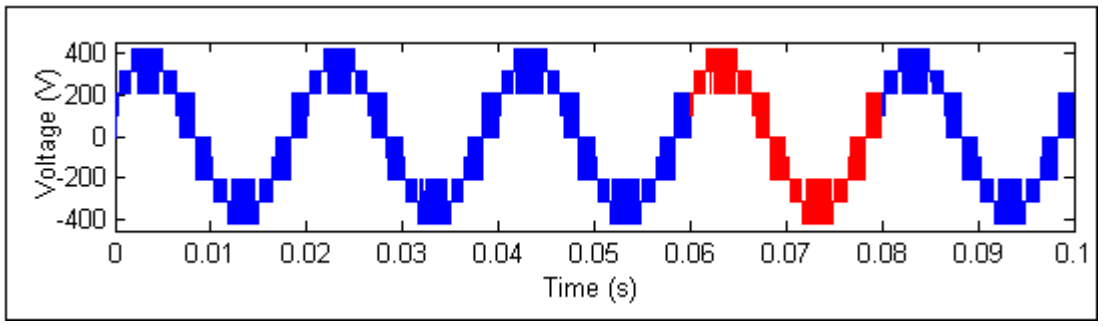


Fig C.2: Output line-to-line voltage of five-level CHB-VSI using PS-PWM

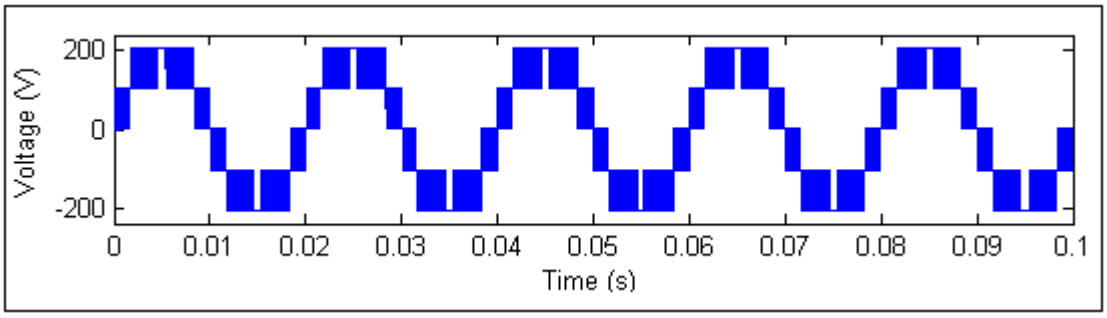


Fig C.3: Output phase voltage of five-level CHB-VSI using PSPWM

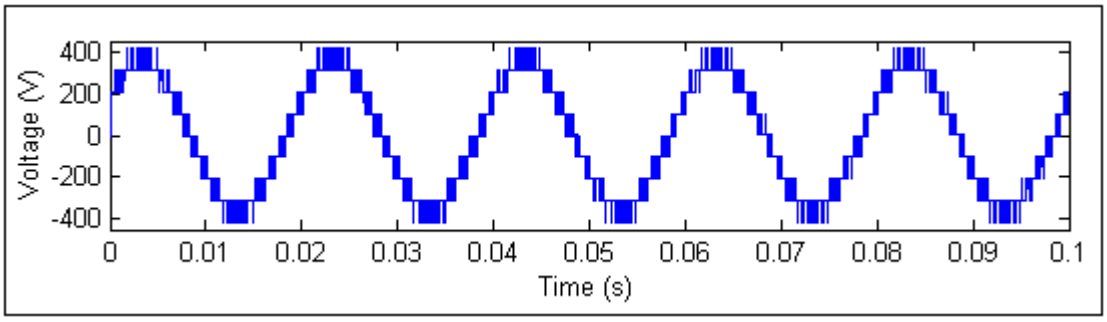


Fig C. 4: output line-to-line voltage of five-level CHB-VSI using IPD

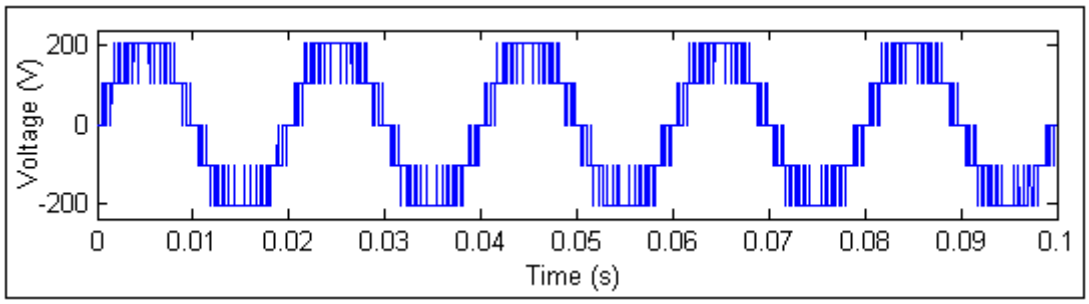


Fig C.5: output phase voltages of five-level CHB-VSI using IPD

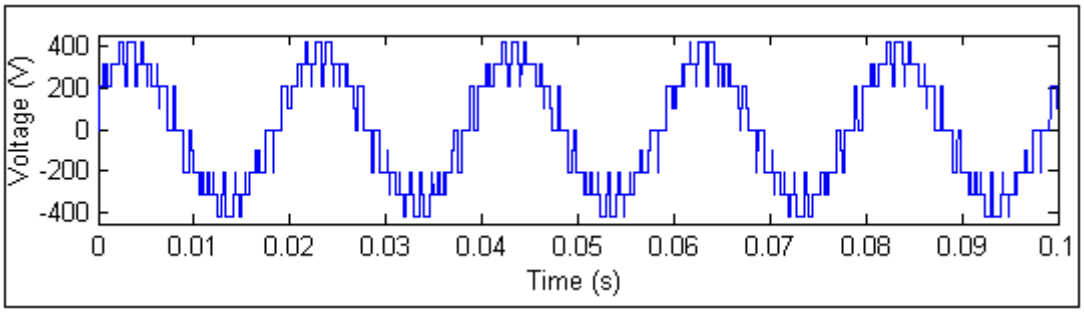


Fig C.6: Output line-to-line voltage of five-level CHB-VSI using APOD

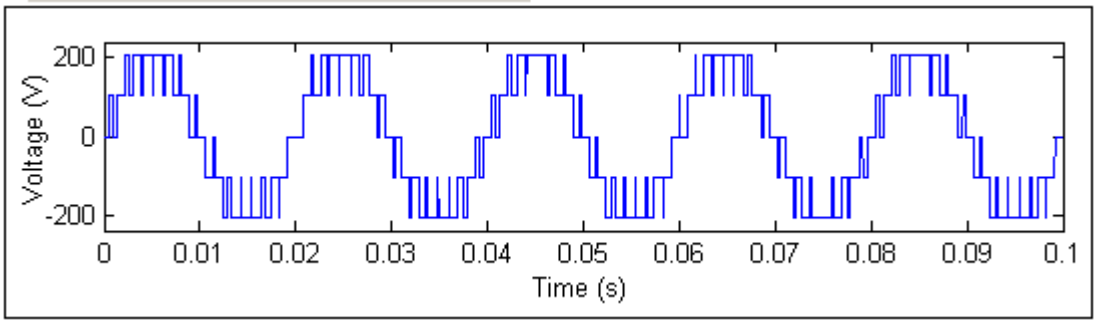


Fig C.7: Output phase voltage of five-level CHB-VSI using APOD

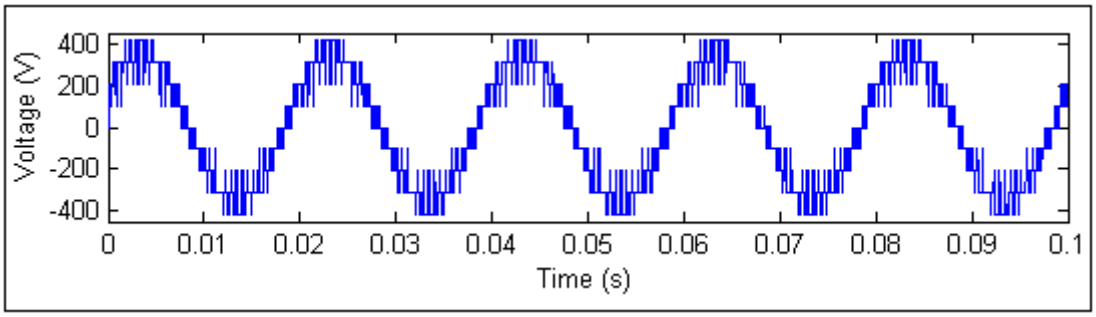


Fig C.8: Output line-to-line voltage of five-level CHB-VSI using POD

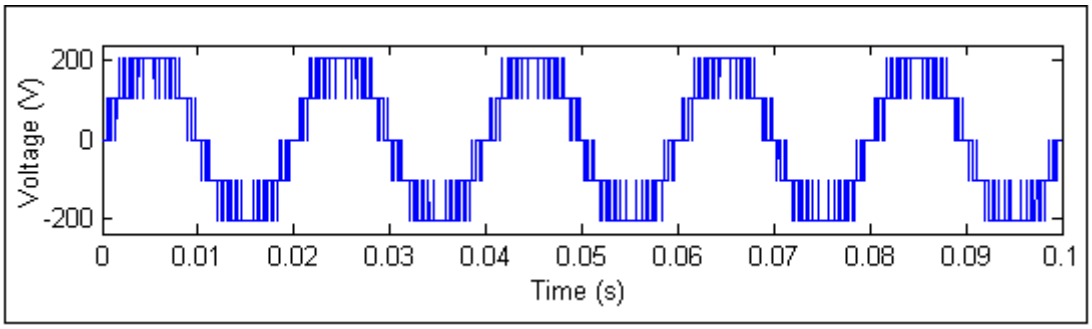


Fig C.9: Output phase voltage of five-level CHB-VSI using POD

Appendix D

Five-level CHB-VSI PS-SPWM

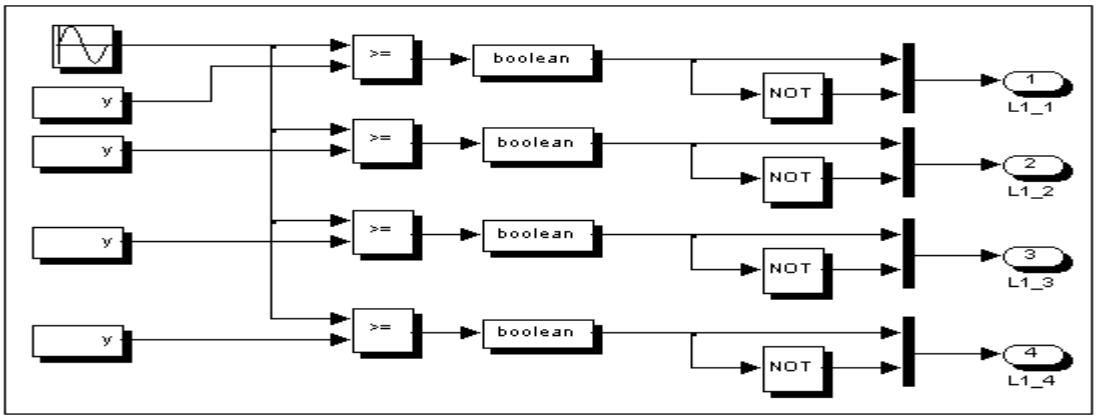


Fig D.1: SIMULINK model of five-level CHB-VSI gating signals generation using PS-SPWM

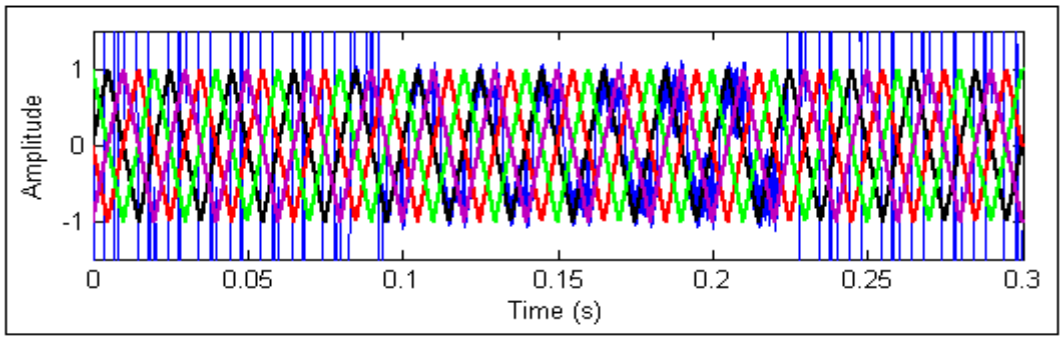


Fig D.2: PS-SPWM for five-level CHB-VSI

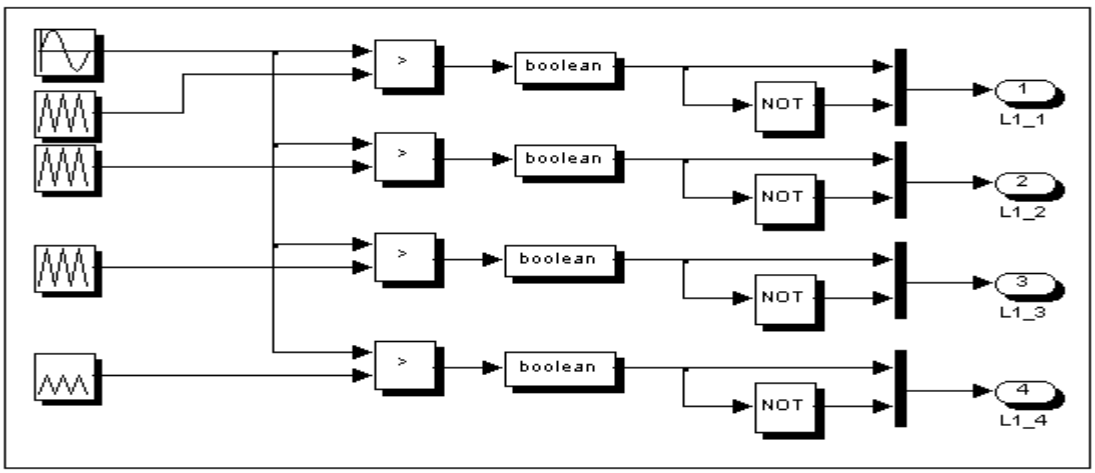


Fig D.3: SIMULINK model of five-level CHB-VSI gating signals generation using IPD

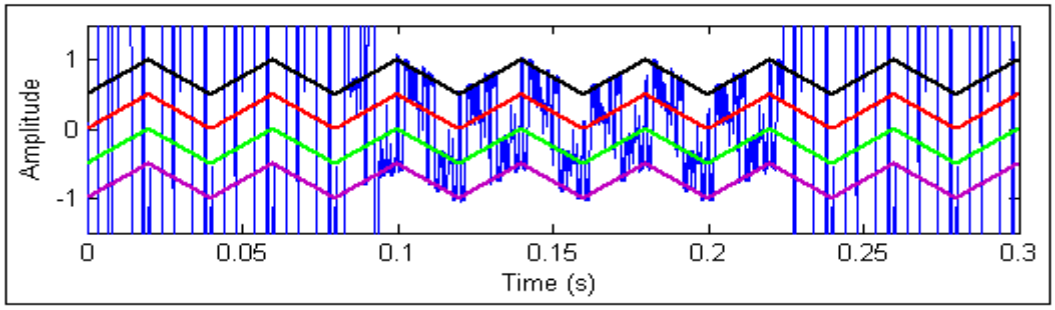


Fig D.4: IPD modulation technique using for five-level CHB-VSI

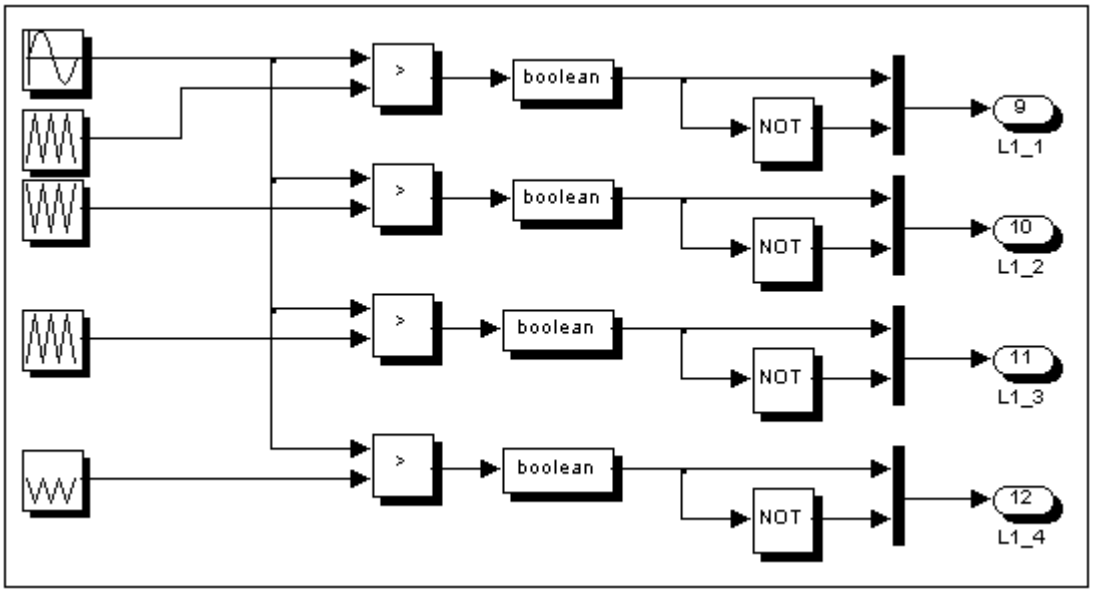


Fig D.5: SIMULINK model of five-level CHB-VSI gating signals generation using APOD

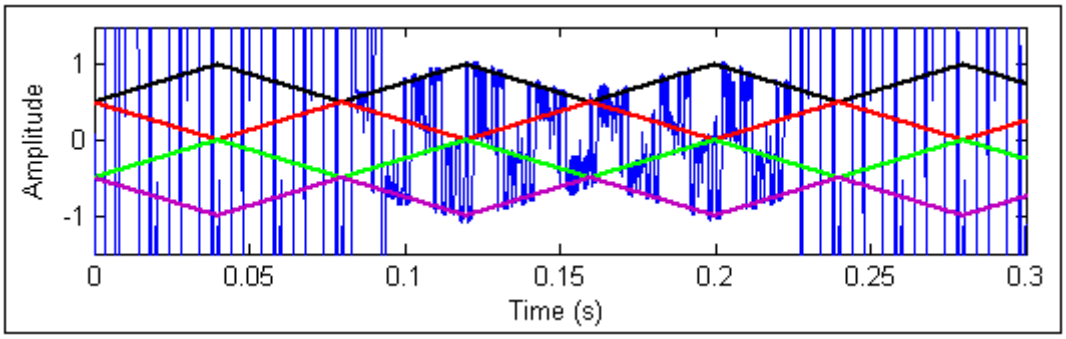


Fig D.6: APOD modulation technique using for five-level CHB-VSI

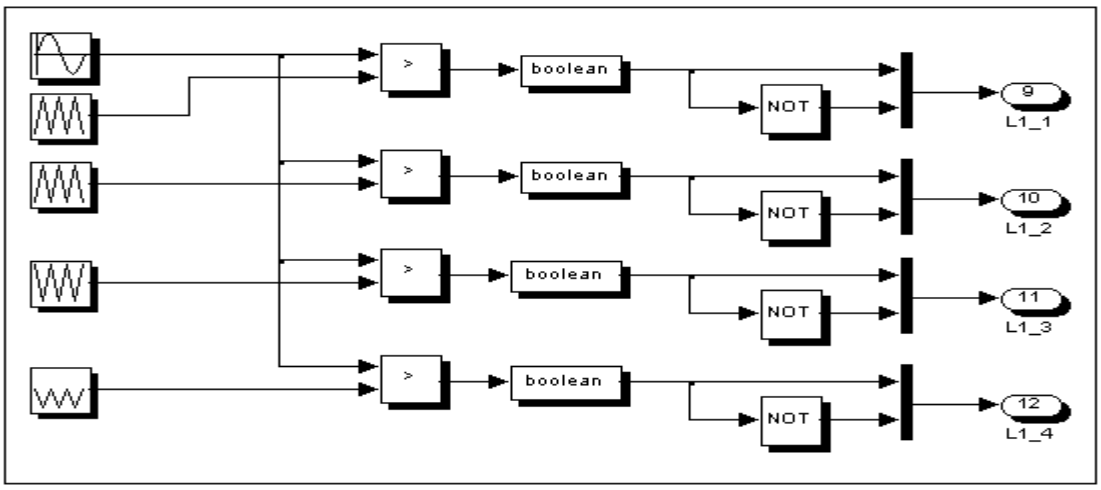


Fig D.7: SIMULINK model of five-level CHB-VSI gating signals generation using POD

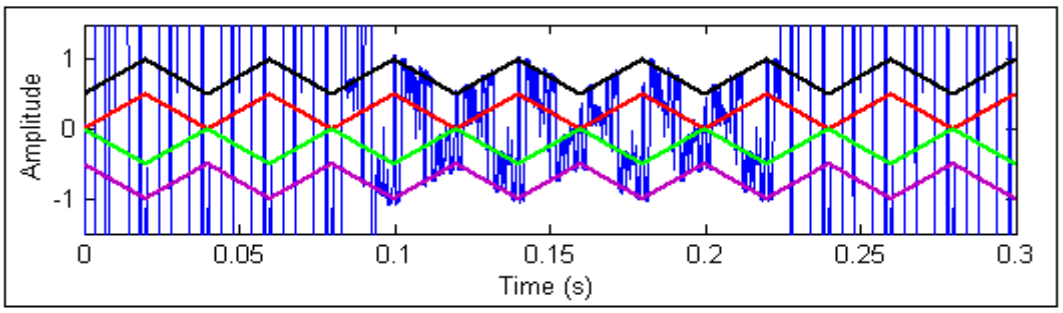


Fig D.8: POD modulation technique using for five-level CHB-VSI

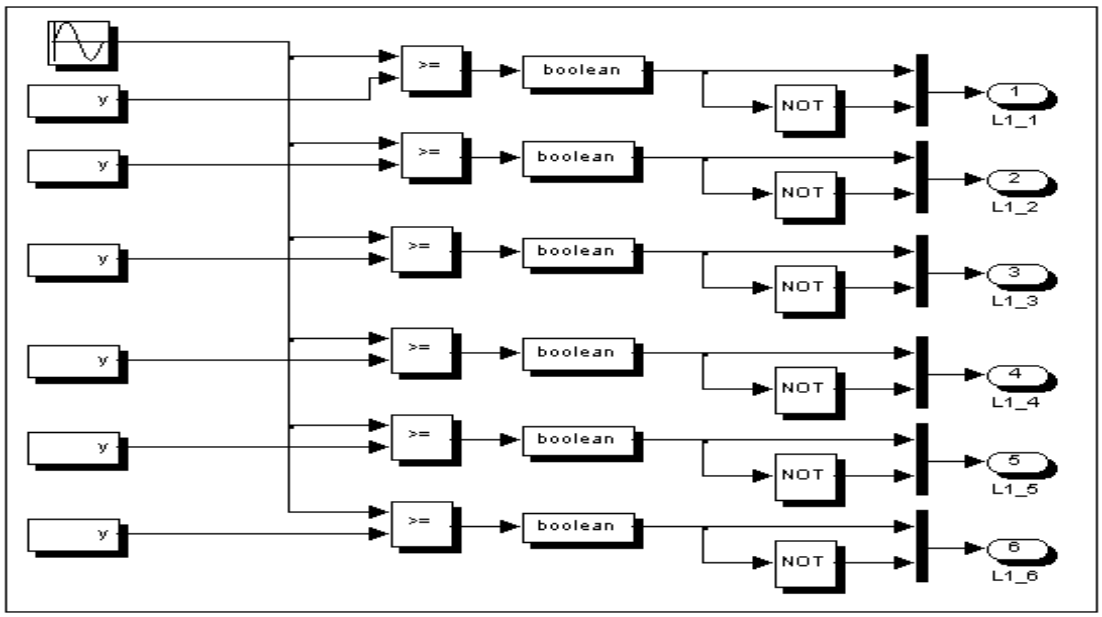


Fig D.9: SIMULINK model of seven-level CHB-VSI gating signals generation using PS-SPWM

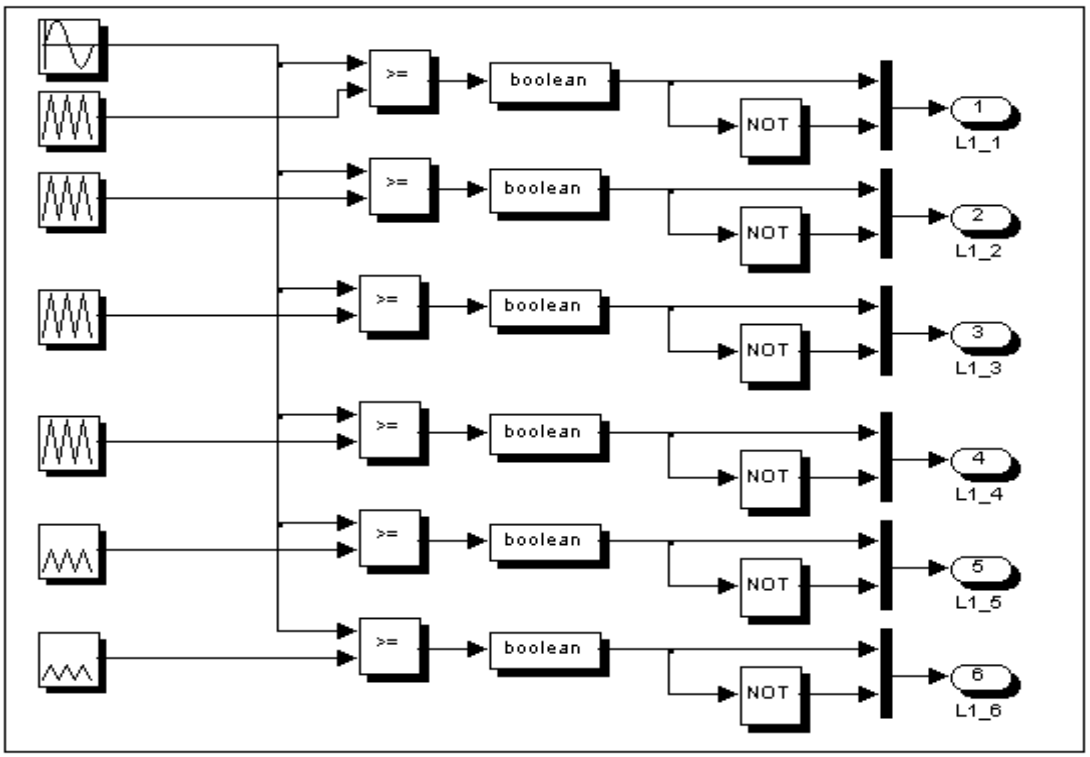


Fig D.10: SIMULINK model of seven-level CHB-VSI gating signals generation using IPD

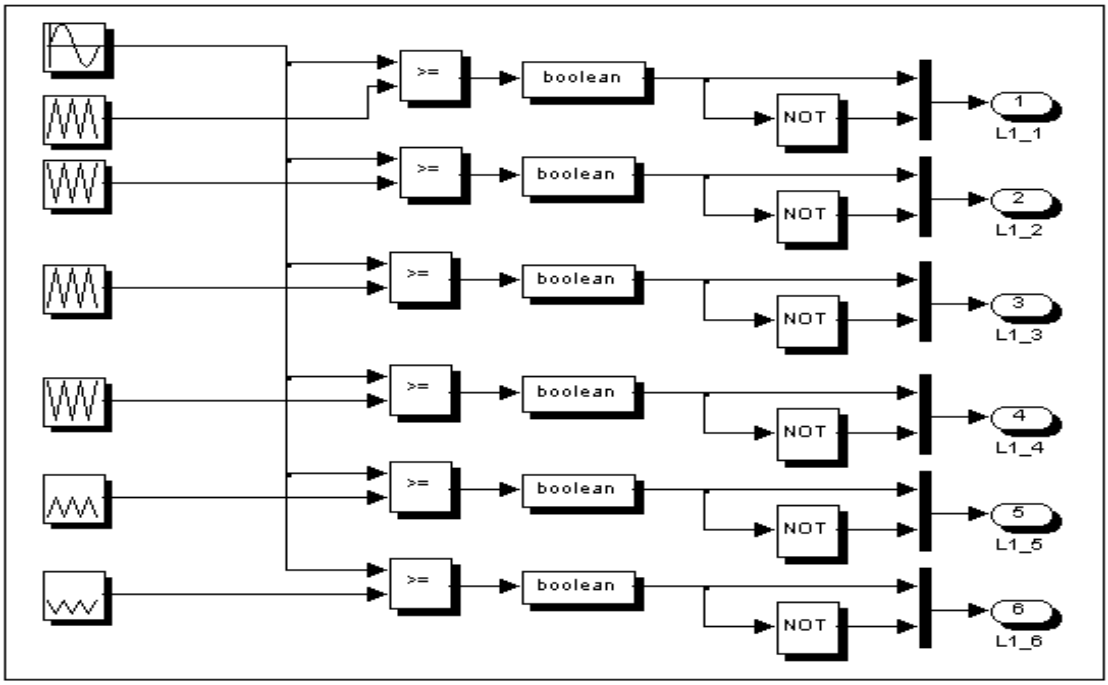


Fig D.11: SIMULINK model of seven-level CHB-VSI gating signals generation using APOD

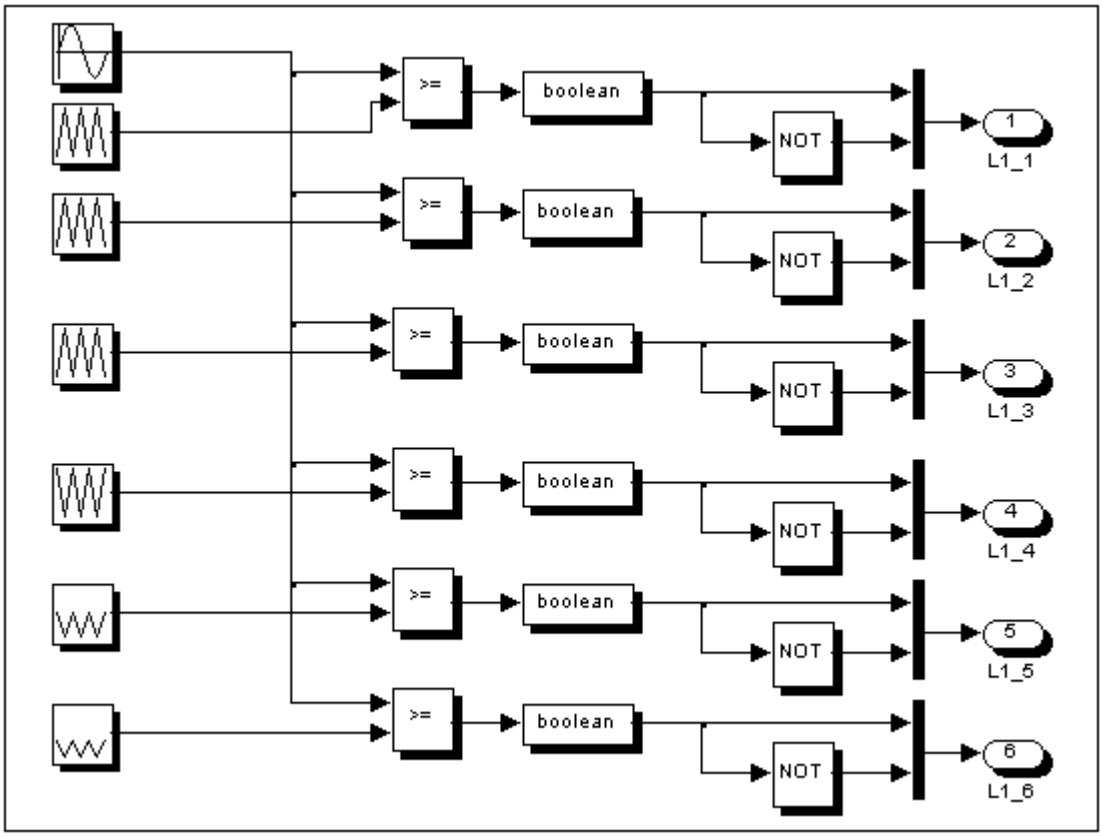


Fig D.12: SIMULINK model of seven-level CHB-VSI gating signals generation using POD