

RELIABILITY-EVALUATION OF NANOSCALE CIRCUIT DESIGN USING  
BAYESIAN NETWORKS

By

USMAN KHALID

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## ABSTRACT

As transistors are scaled down to nanometer dimension, their performances and behaviors become less predictable. Designing reliable circuit or systems using these nano-transistors (nano-circuits or systems) post new challenges and require paradigm shift in design techniques, process and flow. Reliability must be designed into the nano-circuit or systems. Inter-stage and intra-stage (priors) reliability of a designed circuit must be measured during design process so that design could be changed to increase the overall reliability of the nano-circuit or system. Existing reliability evaluation schemes such as Probabilistic Gate Model (PGM), Boolean Difference Error-based Calculator (BDEC), Probabilistic Transfer Matrix (PTM) and Bayesian Network (BN) evaluate the overall or cumulative reliability of a given circuits however only BN has the features to be used to evaluate the priors stage reliability which has never been explored before. Hence, this thesis presents the work that exploit BN capability to measure priors reliability of few standard circuits such as Full Adders and Decoders. Using BN with prior analysis, it was found that priors with large number of gates to have low reliability which subsequently contributed to the low overall reliability of the test circuit. In this research work the inputs of nanoscale circuits have also been modelled as probabilistic digital inputs (PDIs). The Monte Carlo simulation is applied to model PDIs in nanoscale circuits using BN. The results show that the lower values of PDIs gave low reliability values for the test circuits which means low logic input values are more sensitive and error prone to the reliability of the circuit.