DIGITAL CONTROL OF SWITCHING POWER CONVERTERS

By

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FINAL PROJECT REPORT

Submitted to the Electrical & Electronics Engineering Programme
in Partial Fulfillment of the Requirements
for the Degree
Bachelor of Engineering (Hons)
(Electrical & Electronics Engineering)

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CERTIFICATION OF APPROVAL

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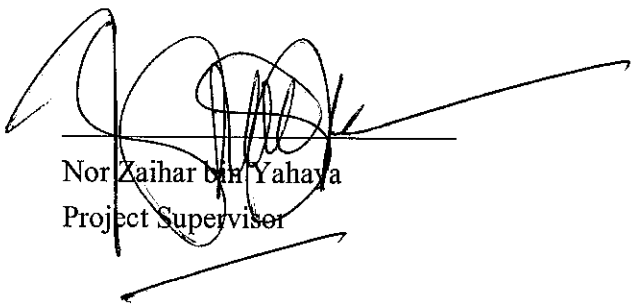
Approved:



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TRONOH, PERAK

December 2006

CERTIFICATION OF ORIGINALITY

This is to certify that I am responsible for the work submitted in this project, that the original work is my own except as specified in the references and acknowledgements, and that the original work contained herein have not been undertaken or done by unspecified sources or persons.

Rubiah binti Hassan

ABSTRACT

This report describes the design of a digital controller that capable to control the switching action of Buck converter. It focuses on how to generate the DPWM signal in order to vary the ON/OFF condition of the low power Buck converter switch. The main objective of this project is to have a controller that capable to produce a stable and high resolution of output voltage with high switching frequency response. Two (2) types of computer simulation have been carried out in this project which are the PSpice and MATLAB simulation. The PSpice simulation has been used to verify that the calculated parameters confirm the Buck converter operating in continuous conduction mode. The simulation results obtained in the PSpice simulation have been verified that the calculated parameters such resistor, inductor and capacitor value can be used for Buck converter circuit operating in continuous conduction mode. All the results obtained, except for the output current ripple are within ±10 % acceptable limit of percentage differences with its design requirements. The MATLAB simulation has been used to design the Buck converter system together with its digital controller part. The simulation results in MATLAB do not achieve the desired objectives because of the problem in setting the PID compensator coefficient which leads to a few simulation errors.

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LIST OF ABBREVIATIONS

AC	Alternating Current
ADC	Analog to Digital Converter
ASIC	Application Specific IC
CCM	Continuous Conduction Mode
CPU	Central Processing Unit
DC	Direct Current
dc	Direct Current
DC-DC	DC to DC
DPWM	Digital Pulse Width Modulation
EMI	Electro-magnetic Interference
FPGA	Field Programmable Gate Array
IC	Integrated Circuit
PCB	Printed Circuit Board
PID	Proportional Integral Derivative
VRM	Voltage Regulation Modules

CHAPTER 1
INTRODUCTION

1.1 Background Study

A switching power converter is a power electronics system which converts one level of electrical energy into another level of electrical energy at the load by the switching action [1], [2], [3]. As illustrated in Figure 1, there are various types of power converters that recently available such as direct current (DC) to DC power converter, DC to alternating current (AC) power converter, AC to DC power converter and AC to AC power converter.

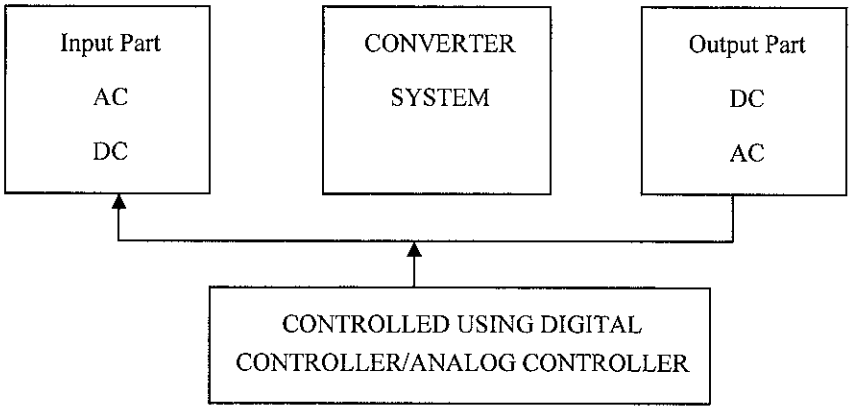
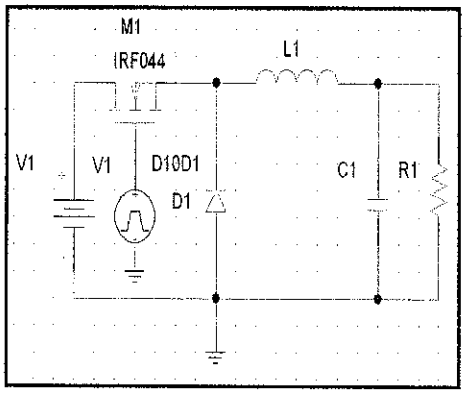


Figure 1 : The Architecture of Power Converter System

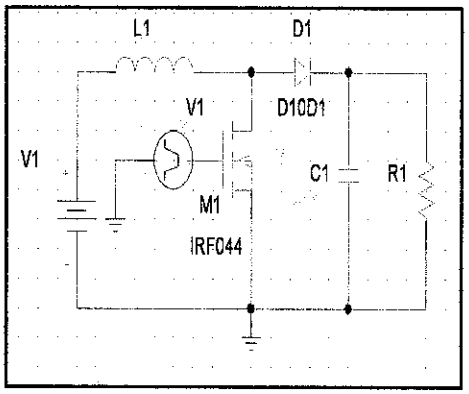
In order to make the conversion process happen, the analog or digital controller is used to control the switching devices of power converter circuit. The analog or digital controller will generate the switching pulse that has capability to turn on the switching devices in an appropriate switching time. Once the switching device has been turned ON, the current from the supply will flow through the circuit and then the conversion process starts.

The requirement for this project is to have a digital controller that has capability to control the switching action of the power converter. It does not mention in the project title what type of power converter can be used or must be used in completing this project. However, from the literature review done, it is known that the digital controller has been widely used to control the switching action of DC-DC power converter. Thus, in order to fulfill the project title requirement, the behavior of low power DC-DC power converter with the digital controller has been studied in details and its existing weaknesses will be improved.

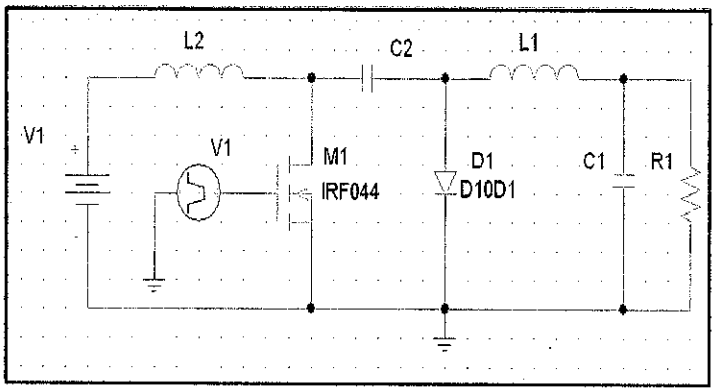
There are many topologies of DC-DC power converter available such as Buck converter (Figure 2.a), Boost converter (Figure 2.b) and Cuk converter (Figure 2.c) [4]. This project only focuses on the study of Buck converter that is controlled by the digital controller.



(a) – Buck converter



(b) – Boost Converter



(c) – Cuk converter

Figure 2 : The types of DC-DC power converters

Buck converter is a step down DC-DC power converter. It means that the dc input voltage at the supply will be converted into another level of dc output voltage at the load. The Buck converter is widely used in nowadays electronics equipments circuitry to step down the dc input voltage from the power cord to a regulated output voltage. This regulated output voltage is used as voltage supply for the overall circuit operation. Example of the electronic circuit that used Buck converter is Central Processing Unit (CPU), Full Programmable Gate Array (FPGA) and Application Specific Integrated Circuit (ASIC) [5].

Besides functioning as the controller for the conversion process, the switch of the power converter circuit is also necessary for the converter efficiency. A low-efficiency power system indicates large amounts of power are being dissipated in the form of heat. Thus, the efficiency of switching power converter is very important or else will contribute to problems as listed below.

1. The cost of energy increases due the increasing of consumption
2. Additional design complications might be imposed, especially regarding the design of device heat sinks.
3. Additional components such as heat sinks increase the cost, size and weight of the system and these will result low power density.
4. High power dissipation forces the switch to operate at low switching frequency, resulting limited bandwidth and slow response system.
5. Component and device reliability is reduced.

1.2 Problem Statement

In the past years, the analog controllers have been dominating in control of switching power converter because of its simplicity and low cost [6]. It is very simple to design analog controller because the output voltage of power converter circuit is already in the analog signal. This analog output voltage can be fed straightforward to the controller circuit without any signal conversion. Vice versa, when using digital controller, it must be converted into digital representation first, before it can be used in the digital controller circuit. The conversion process from analog signal to digital signal will add some complexity in design stages and it also contributes to the limit cycles problem. The detail explanation about limit cycles problem and a few other

problems encountered when designing DC-DC power converter that drives via digital controller is stated in Section 2.3 of literature review section.

1.2.1 Comparison between Analog and Digital Controller

The analog controller although simpler and cheaper than digital controller, but it also has several weaknesses. The analog controller is not the best method in regulating the output voltage of the power converter due to the complicated behavior of power converters. The power converter is a nonlinear system due to the time varying nature of the switches, variation of parameters and fluctuations of input voltage and load current. Whereas, the analog controllers are usually designed using the linear models. Therefore, it is difficult to design the control algorithms with high performance when using the analog controller.

Besides that, the analog controller also has others drawbacks such as low flexibility, large part count, low reliability and sensitive to the environmental influence such as thermal, aging and tolerance [7], [8], [9]. The digital control of switching power converter approach gives better solution than the analog controller and it also offers a number of advantages such as high programmability, high flexibility, fewer components and provides advance control algorithms[10], [11].

1.3 Objectives and Scopes of Work

1.3.1 Objectives of Work

There are five (5) objectives to achieve in this project. The first objective is to perform study on how to digitally control the switching action of low power Buck converter. Second objective is to perform study on the operation and the behavior of Buck converter circuit. Third objective is to design a digital control of switching Buck converter system in PSpice or MATLAB software. Fourth objective is the digital controller part must have capability to generate switching pulse width with high switching frequency. The last objective is that the designed system must able to produce stable output voltage at its load.

1.3.2 Scopes of Work

This project focuses on how to control the switching action of Buck converter by using the digital pulse width modulation (DPWM) technique. The DPWM signal that is generated by the digital controller will be used to control the switching device operation in the Buck converter circuit. In this project, the type of switching device used is MOSFET (IRF044). The MOSFET has been selected because it is the fastest power switching device which can adapt with switching frequency of more than 1 MHz. Thus, it is suitable to be used in this project as it has fast switching response. Besides that, this study also focuses on the design of low power 2W Buck converter.

CHAPTER 2
LITERATURE REVIEW

2.1 Overview on Digital Control of Switching Power Converters

Currently, most of the digital control of switching power converters are implemented using analog to digital converter (ADC) and microprocessors [12], [13]. A few names of digital signal processing microprocessors board have been known throughout this study such as ADMC – 401 [14], TMS320 [15] and so on. A typical block diagram of Buck converter with digital controller is as shown in Figure 3.

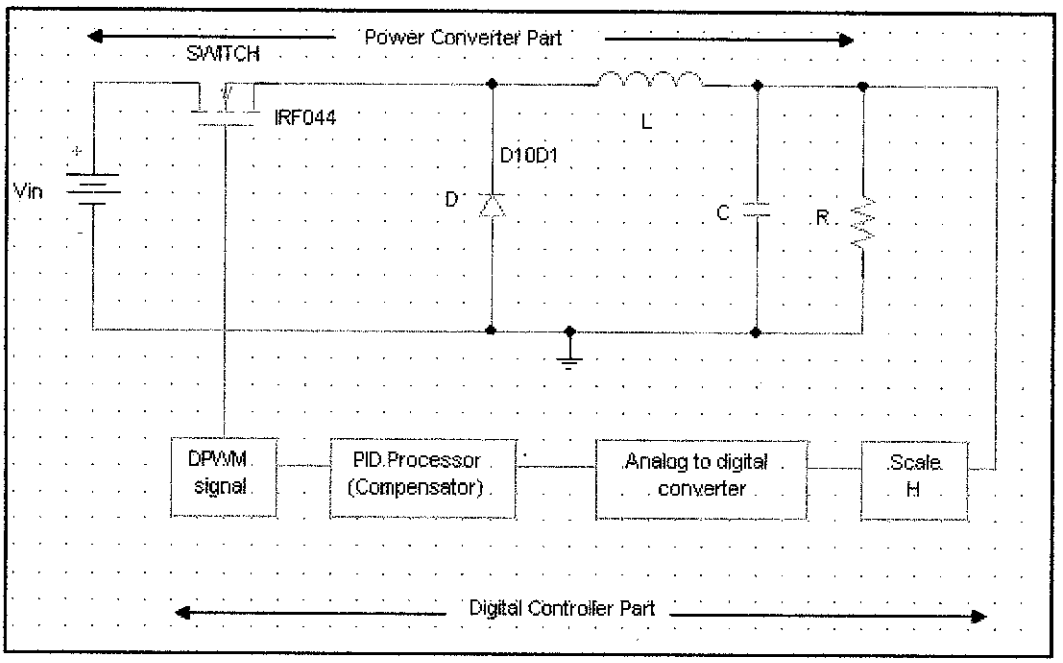


Figure 3 : Digital Controller of Buck Converter

The upper part of Figure 3 shows the Buck converter circuit where voltage conversion process occurred. The feedback loop shows the digital controller part which comprises of a few block diagrams used to generate the DPWM signal. The

DPWM signal generated by the digital controller part will be used to trigger the switching operation of the switch (IRF044). The efficiency and the stability of power converter conversion process depends on how good the digital controller can create the DPWM signal.

As shown in the Figure 3, the digital controller part consists of an ADC, a discrete-time proportional-integral-derivative (PID) processor and a DPWM generator. Every block diagram shown in Figure 3 has its own task, such as the ADC is used to digitize the regulated quantity of the analog output voltage. The PID subsystem on the other hand, is used to perform the job in translating the discrete representation of output voltage into the duty-cycle information used by DPWM generator. The DPWM generator is used to generate duty cycle signal by calculating and then timing the desired duration of ON and OFF periods of its output signal [16].

2.2 Buck Converter Topology

When Buck converter is in operation, it alternates between connecting the inductor to source voltage to store energy in the inductor and discharging that energy to the load. There are two operation modes for Buck converter which are continuous conduction mode (CCM) and discontinuous conduction mode (DCM) [17].

2.2.1 Continuous Conduction Mode

A Buck converter operates in CCM if the current passed through the inductor never falls to zero during the commutation cycle. The operating principle for this mode is described by the chronogram in Figure 4.

When the switch is turned on, the voltage across the inductor is equal to input voltage less output voltage ($V_L = V_{in} - V_o$). The inductor flows through the inductor rises linearly. As the diode is reverse-biased by the voltage source (V_{in}), no current flows through it. When the switch is turned off, the diode is forward biased. The voltage across the inductor is $V_L = -V_o$ (neglecting the diode drop). The inductor current I_L will decrease. During the CCM, the inductor value is greater than inductor critical value ($L > L_{CRIT}$).

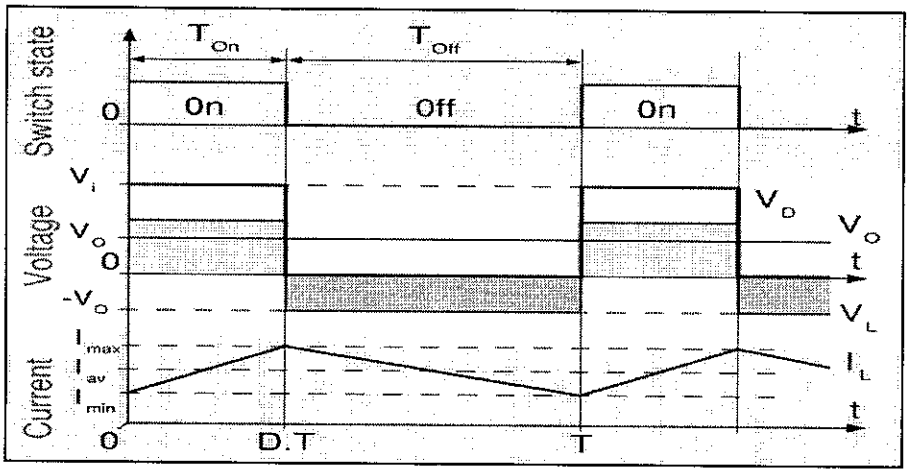


Figure 4 : The operating principles of an ideal CCM Buck converter [17]

2.2.2 Discontinuous Conduction Mode

In some cases, the amount of energy required by the load is small enough to be transferred in a time lower than the whole commutation period. In this case, the current through the inductor falls to zero during part of the period. The difference between CCM is the inductor is completely discharged at the end of commutation cycle. During the DCM, the inductor value is lower than the inductor critical value ($L < L_{CRIT}$). Figure 5 shows the switching waveform, output voltage waveform and inductor current waveform during DCM.

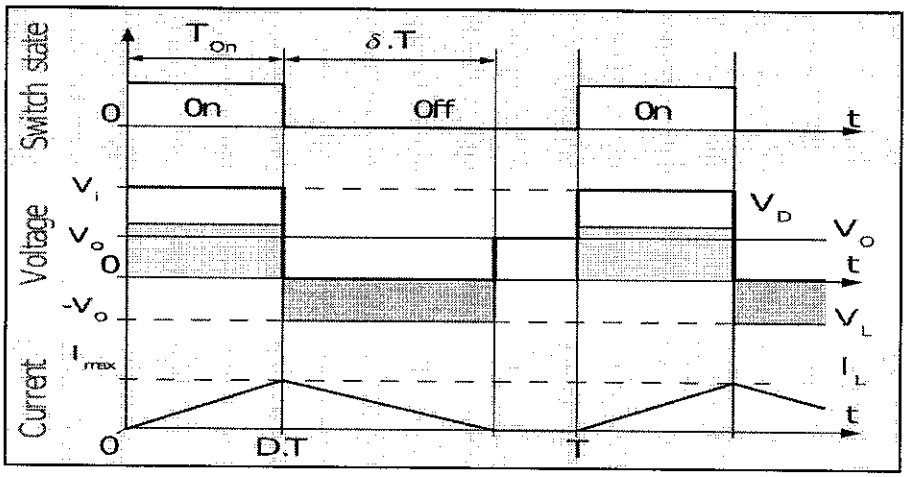


Figure 5 : The operating principles of an ideal DCM Buck converter [17]

2.3 Digital Controller Topology

In the digital controller, the sampled output voltage from power converter load is compared to a reference value then their difference forms an error signal. This error signal will be digitized to a digital representation in ADC subsystem. The resolution and the gain of error signal in the ADC subsystem are determined using the formulas below:

$$N_{ADC} = \text{int}(\log_2(V_{out} / \Delta V_{out}) \tag{1}$$

$$K_{ADC}(s) = \frac{1-2^{-N_{ADC}}}{V_{\max_{ADC}}} \tag{2}$$

For simplification, the ADC gain has been found using the formulas states in equation (3)

$$K_{ADC} = \frac{1}{\Delta V_{OUT}} \tag{3}$$

Where N_{ADC} represents the resolution of error signal in ADC subsystem, while V_{out} and ΔV_{out} are the value of output voltage and output voltage ripple respectively. $K_{A/D}$ is the gain of ADC subsystem and $V_{\max_{A/D}}$ is the maximum voltage range of ADC.

A compensator that implements a control law processes the quantized error signal obtained from the ADC subsystem. The control law can be represented in the following form [18]:

$$d[n] = \alpha_1 d[n-1] + \alpha_2 d[n-2] + .. + \beta_0 e[n] + \beta_1 e[n-1] + \beta_2 e[n-2] + ... \tag{4}$$

Where $d[n]$ and $e[n]$ are the current values of the duty ratio and the current value of the error signal, while $d[n-i]$ and $e[n-i]$ are the values of the duty ratio and the error signal i cycles before the current cycle. The coefficients α_i and β_i determine the compensator characteristics.

From equation (4), it can be seen that the compensator part requires several multiplications and additions. Digital multipliers are relatively large or slow components. If Figure 3 operates with proper feedback system, the difference between the measured output voltage and the reference voltage is relatively small. This opens the possibility to implement the compensator part using a relatively small look-up tables instead multipliers. A block diagram of the PID compensator based on look-up table structure is as shown in Figure 6. The compensator performs the following discrete-time PID control law [18].

$$d[n] = d[n-1] + \alpha e[n] + be[n-1] + ce[n-2] \tag{5}$$

Outputs of the look-up tables are pre-stored value of their inputs multiplied by the controller coefficients. The current and previous values of the error signal are used as address generators for the tables. New value of the duty ratio is formed as a sum of its previous value and the values at the look up tables' outputs. The PID control law given by Equation (5) results in zero steady-state error. Furthermore, there is no further important because the duty ratio has large variations and the result of multiplication by a controller coefficient cannot be stored in a small look-up table.

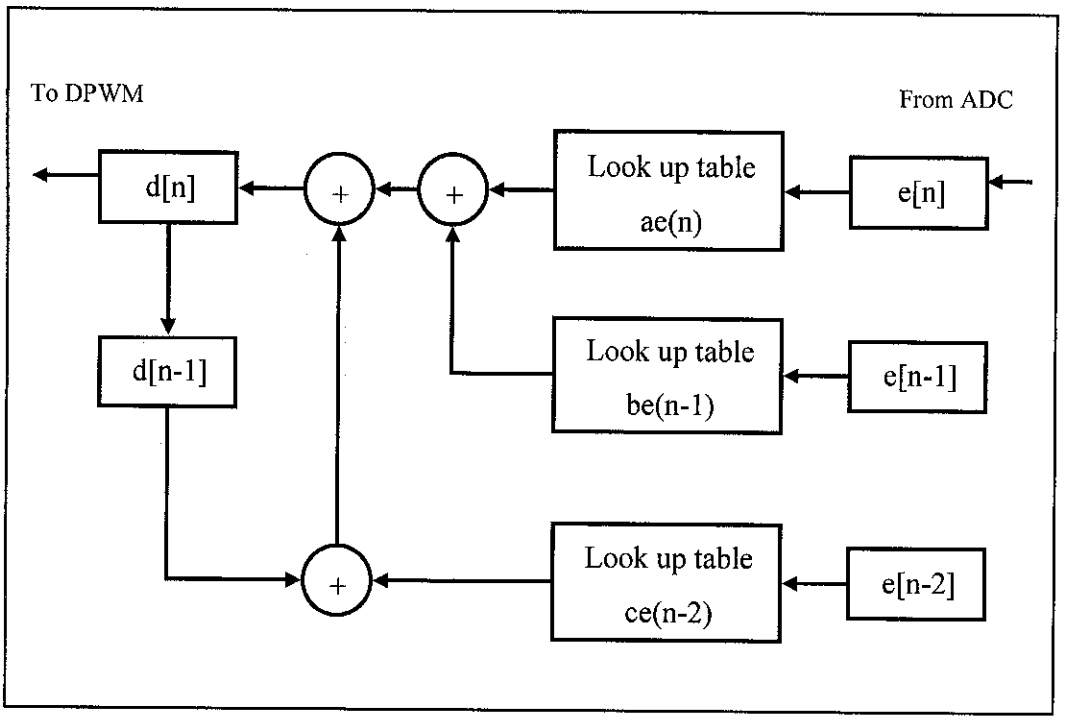


Figure 6 : PID compensator based on look-up tables

The output of PID controller is sent to DPWM generator to create switching waveform in order to trigger the switching operation of the MOSFET (IRF044). The resolution and the gain of DPWM signal are determined using the equation (6), (7) and (8) respectively.

$$N_{DPWM} \geq \text{int}\left[N_{ADC}+\log_2\left(\frac{V_{ref}}{V_{\max_{ADC}}.D}\right)\right] \tag{6}$$

$$N_{DPWM} \geq N_{ADC}+1 \tag{7}$$

$$K_{DPWM} = \frac{1}{2^{N_{DPWM}}-1} \tag{8}$$

Where N_{DPWM} represent the resolution of DPWM signals, N_{ADC} represents the resolution of ADC signal, V_{ref} represents the reference voltage, $V_{\max_{ADC}}$ is the maximum range of voltage for ADC circuit, K_{DPWM} represents the DPWM gain.

2.4 Limit Cycle Oscillation

One of the problems that usually encountered when designing the DC-DC power converter driven by the digital controller is the occurring of limit cycle oscillation. The limit cycle oscillation is the steady state oscillations of output voltage and other system variables at frequencies lower than the converter switching frequency. Steady-state limit cycling is undesirable if it leads to large amplitude output voltage variation. It also difficult to analyze and compensate the resulting output voltage noise and the electro-magnetic interference (EMI) if the output voltage has limit cycle oscillation. The limit cycle phenomenon can be avoided if the designed system satisfies the conditions state below [19]:

i. The DPWM resolution must be higher than the resolution of ADC
ii. The integral gain must be greater than 0 but less than 1 ($0 < K_i \leq 1$)
iii. The system need to satisfy nyquist theorem ($1 + N(A)L(j\omega) \neq 0$)
iv. Clock frequency of the digital circuit must greater than the switching frequency

However, it is not easy to satisfy all the conditions state above because they are interdependent to each other. As an example, in order to operate the power converter system at 1 MHz of switching frequency with 10 bits of DPWM resolution, the clock frequency of digital circuit will be, f_{clk} = 1/977picoseconds = 1.024 GHz. The 977 picoseconds of clock time correspond to switching time (1 μsec) divided by 2^{10}. The 1.024 GHz clock frequency is too high for DC-DC power converter application. This phenomenon will increase the cost of integrated circuit (IC) in the design stages. High clock frequency of digital circuit also requires more driving power that exceeds practical values for DC-DC power converter products.

Most of today electronics applications, such as Voltage Regulation Modules (VRM) are demanding very small output voltage ripple, as lower as 10 mV [20]. Lower output voltage ripple of the system can be achieved by using large bits numbers of ADC circuits. However, using too large bits numbers will contribute to high clock frequency of digital circuit. It is found that for a VRM system with 10 mV of output voltage ripple, it requires 10 bits of ADC resolution. This means the converter needs at least 11 bits of DPWM resolution in order to avoid limit cycle oscillation. To operate Buck converter for this VRM system with 1 MHz of switching frequency, such resolution requires 2 GHz clock frequency in counter-comparator implementation of DPWM generator. In the ring oscillator implementation of DPWM generator, it requires 2048 stages (2^{11} = 2048) stages of ring oscillator. This condition will result high power dissipation or large area. Thus it is beneficial to find ways to achieve the desired high output voltage resolution with the usage of low-resolution of the DPWM modules and acceptable range of clock frequency for the digital circuit.

CHAPTER 3
METHODOLOGY/PROJECT WORK

3.1 Project Flow Chart

In the first semester, the literature review has been done in order to get an understanding on the project requirement, concept and theory of the project. The PSpice simulations based on IEEE articles and other references also have been carried out in order to illustrate the outcomes of the study. A brief outline of the framework for the first semester is shown in Figure 7 below.

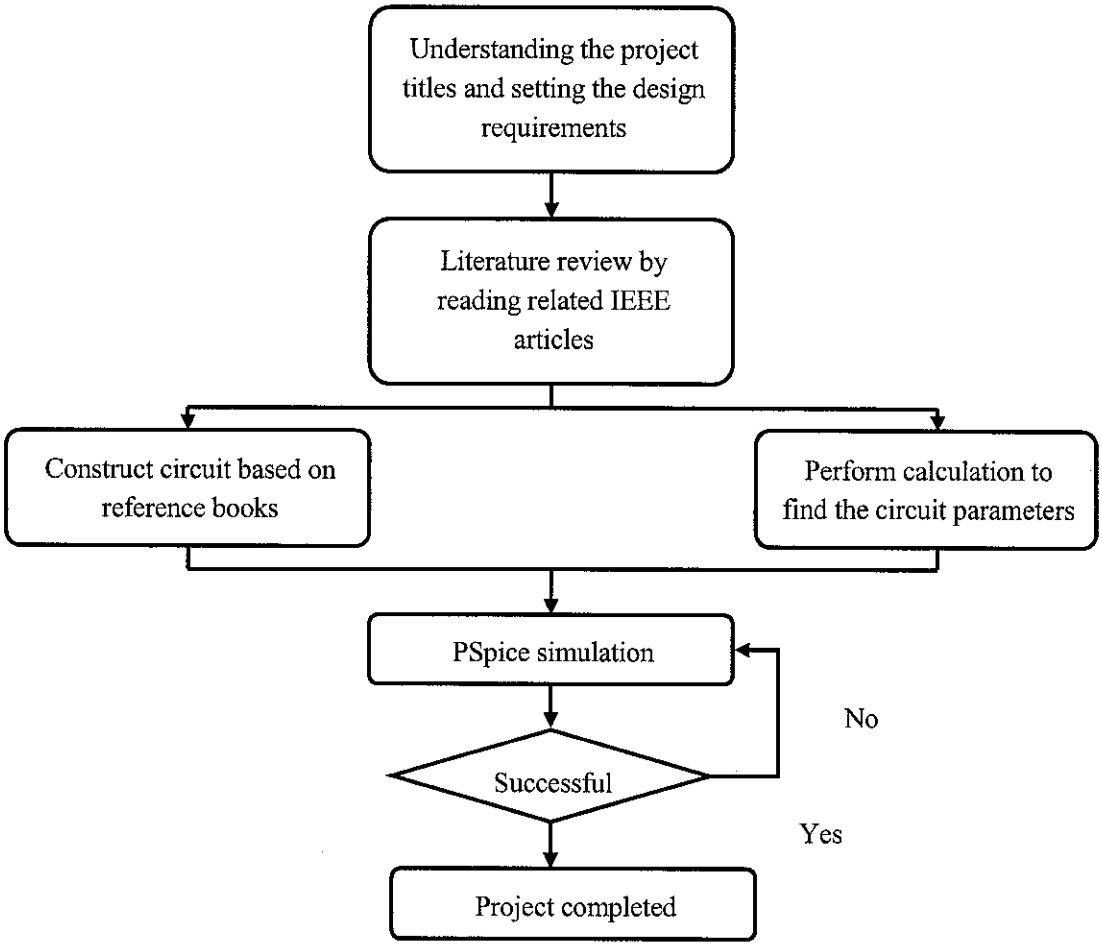


Figure 7 : Semester 1 project flow

In the second semester, this project continued by simulating the overall circuit diagram using PSpice and MATLAB software. The simulation results are compared with the output waveform found in the IEEE journals. This project can be considered successful if the simulation results of the designed circuit provide better performance than the results obtained from IEEE journal. A brief outline of the framework for second semester is shown in Figure 8 below.

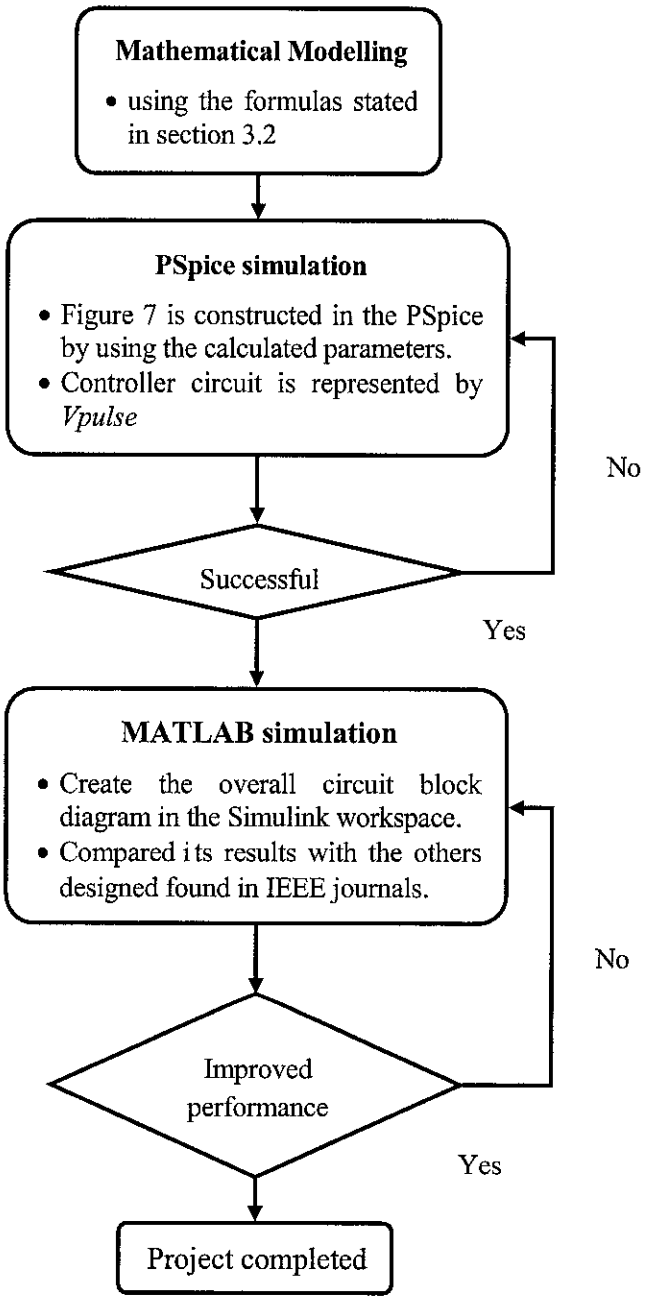


Figure 8 : Semester 2 project flow

3.2 Setting the Design Requirements

In the initial stage of project implementation, there are several parameter values to be set up as shown in the Table 1 below. The main targets during this stage are to meet the requirements for low power Buck converter operation and high switching frequency power converter. The parameter values are referred to the existing characteristics of micro power DC-DC converter from Linear Technology [21].

Table 1 : The parameter values

Design requirement	Value
Input voltage, V_{in}	12 V
Output voltage, V_{out}	5 V
Switching frequency, f_s	100 kHz
Maximum ripple current, ΔI	21 mA
Maximum output ripple voltage, ΔV_{out}	20 mV
Output power, P_o	2 W
Load current, I_L	415 mA

3.3 Mathematical Modelling

In the mathematical modeling stage, few formulas have been used in order to find the parameter values needed in simulation stages. The mathematical modeling stage has been divided into two parts which are the power converter part and the controller part.

3.3.1 Mathematical Modelling for Power Converter Part

Before constructing the Buck converter circuit, its parameters such as duty cycle, inductor, capacitor and resistor value are determined through calculations. The calculations are based on Buck converter formulas found in [4]. All the formulas used for power converter part are listed in this section.

- To calculate the duty cycle

$$D = \frac{Vout}{Vin} \tag{5}$$

Where:

V_{out} = Output voltage of power converter

V_{in} = Input Voltage of power converter

- To calculate the load resistor value

$$R = \frac{V_{out}}{I_{LOAD}} \tag{6}$$

Where:

V_{out} = Output voltage of power converter

I_{LOAD} = Load current

- To calculate the inductor value

$$L = \frac{DV_{in}(1-D)}{f_s \Delta I} \tag{7}$$

Where:

D = duty cycle

V_{in} = Input voltage

f_s = switching frequency

ΔI = Output current ripple

- To calculate capacitor value

$$C = \frac{V_{in}D(1-D)}{8Lf_s^2 \Delta V_{out}} \tag{8}$$

Where:

D = duty cycle

V_{in} = Input voltage

f_s = switching frequency

ΔV= Output voltage ripple

- To calculate L_{CRIT} value

$$L_{CRIT} = \frac{(1-D)}{2} TR \tag{9}$$

Where:

D = duty cycle

T = time

R = Load resistance

- To calculate minimum and maximum inductor current value

$$I_{LMIN} = DV_{IN}\left(\frac{1}{R_{LOAD}} - \frac{(1-D)T}{2L}\right) \tag{10}$$

$$I_{LMAX} = DV_{IN}\left(\frac{1}{R_{LOAD}} + \frac{(1-D)T}{2L}\right) \tag{11}$$

Where:

D = duty cycle

Vin = Input voltage

T = time

R = Load resistance

- To calculate output voltage ripple

$$\frac{\Delta V_{out}}{V_{out}} = \frac{\Delta V_{out}}{DV_{in}} = \frac{1-D}{8LCf_s^2} \tag{12}$$

Where:

D = duty cycle

f_s = switching frequency

R = Load resistance

3.3.2 Mathematical Modelling for Controller Part

Before constructing the overall digital control of switching Buck converter system in the Simulink workspace, the parameters such as number of bits for ADC signal, number of bits for DPWM signal, ADC gain and DPWM gain are determined through calculations. The calculations are based on the formulas listed below:

- To calculate number of bits for ADC signal

$$N_{ADC} = \text{int}(\log_2(V_{out} / \Delta V_{out}) \quad (13)$$

Where:

N_{ADC} = number of bits of ADC signal

V_{out} = output voltage

ΔV_{out} = ripple output voltage value

- To calculate the number of bits for DPWM signal

$$N_{DPWM} \geq \text{int}\left[N_{ADC} + \log_2\left(\frac{V_{ref}}{V_{\max_{ADC}} . D}\right)\right] \quad (14)$$

Where:

N_{DPWM} = number of bits of DPWM signal

V_{ref} = reference voltage

$V_{\max_{ADC}}$ = maximum allowable range of ADC voltage

D = duty cycle

- To calculate the ADC gain

$$K_{ADC}(s) = \frac{1 - 2^{-N_{ADC}}}{V_{\max_{ADC}}} \quad (15)$$

Where:

K_{ADC} = ADC gain

$V_{\max_{ADC}}$ = maximum allowable range of ADC voltage

N_{ADC} = number of bits of ADC signal

- To calculate DPWM gain

$$K_{DPWM} = \frac{1}{2^{N_{DPWM}} - 1} \tag{16}$$

Where:

K_{DPWM} = DPWM gain

N_{DPWM} = number of bits of DPWM signal

- To calculate a,b and c coefficients of PID compensator

$$d[n] = d[n-1] + \alpha e[n] + be[n-1] + ce[n-2] \tag{17}$$

Where:

$d[n]$ = current values of duty ratio

$e[n]$ = current value of error signal

$d[n-i]$ = the duty ratio i cycles before the current cycle

$e[n-i]$ = the error signal i cycles before the current cycle

a,b & c = the PID compensator coefficients

3.4 PSpice Simulation

The Buck converter circuit (See Figure 9) is simulated in the PSpice software. There are voltage and the current markers located in the circuit to indicate the location of output waveforms that need to be observed.

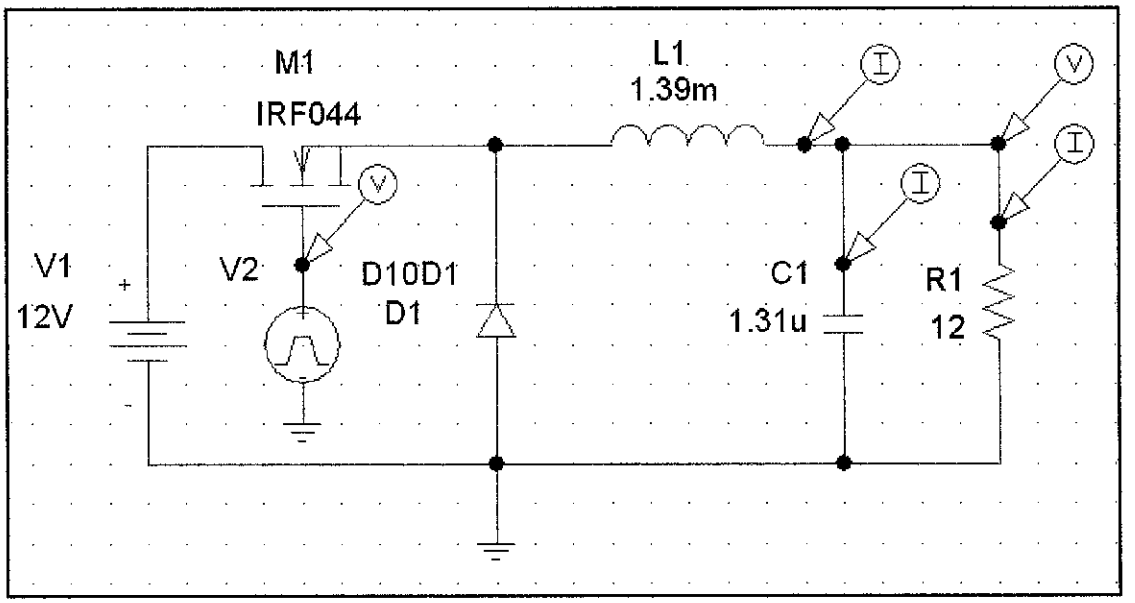


Figure 9 : The Buck converter circuit

The detail information about the PSpice components that used to construct the Buck converter circuit in Figure 9 is summarized in Table 2 below.

Table 2 : List of PSpice components

Component Name	Type / Label	Function	Value
Dc voltage source	*V1*	To supply dc input voltage to the power converter circuit.	12 V
Pulse width	V_{pulse} / *V2*	To generate switching pulse width for the Buck converter	Detail V_{pulse} setting is as listed in the Table 3.
MOSFET	*IRF044*	Functions as a switch to control the Buck converter	-

		operation	
Diode	*D10D1*	Act as free wheeling diode to ensure that the inductor current maintain its continuous mode.	-
Inductor	*L1*	Act as a filter of the power converter circuit	1.39 mH
Capacitor	*C1*	Act as a filter of the power converter circuit	1.31 μH
Resistor	*R1*	Act as the load	12 Ω

The switching operation (ON/OFF condition) of the power converter circuit is controlled by a switching pulse width generated by the digital controller. For simplification, the digital controller part that comprises ADC subsystem, PID compensator subsystem and DPWM generator subsystem are represented by the V_{pulse} (See Figure 10). The V_{pulse} component which functions as pulse width generator is available in the PSpice library. The actual ADC subsystem, PID compensator subsystem and DPWM generator subsystem is designed in the MATLAB/Simulink software. This is because the microprocessor function that represents the PID compensator subsystem is not available in the PSpice library.

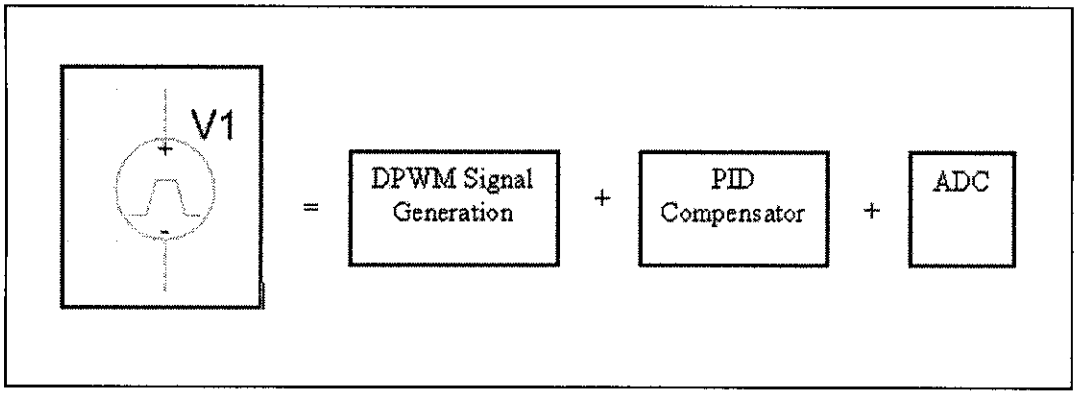


Figure 10 : V_{pulse} representing the digital controller part

In order to get a stable and an efficient power converter system, the correct setting of V_{pulse} / *V2* is very important. The Buck converter circuit in Figure 9 is simulated using the V_{pulse} setting shown in Table 3 below. There are six types of output waveforms observed in PSpice simulation and these outputs waveforms are stated in Section 4.2. As these six waveforms have been verified the behavior of Buck converter operating in CCM, the PSpice simulation completed.

Table 3 : The V_{pulse} / *V2* setting

Parameters	Value
DC	10 V
AC	1 V
V1	0 V
V2	40 V
TD (delay time)	0.01 µs
TR (rise time)	0.01 µs
TF (fall time)	0.01 µs
PW (t_{sw} x *D*)	4 µs
PER (t_{sw})	10 µs

3.5 MATLAB/Simulink Simulation

The overall digital control of switching power converter system which comprises Buck converter circuit and its digital controller part are designed in the MATLAB/Simulink software. This system consists four major parts (see Figure 11), which are power converter part, ADC subsystem, PID compensator and DPWM generator. The overall block diagram in Figure 11 is designed by referring to [12], [14], [18] and [22].

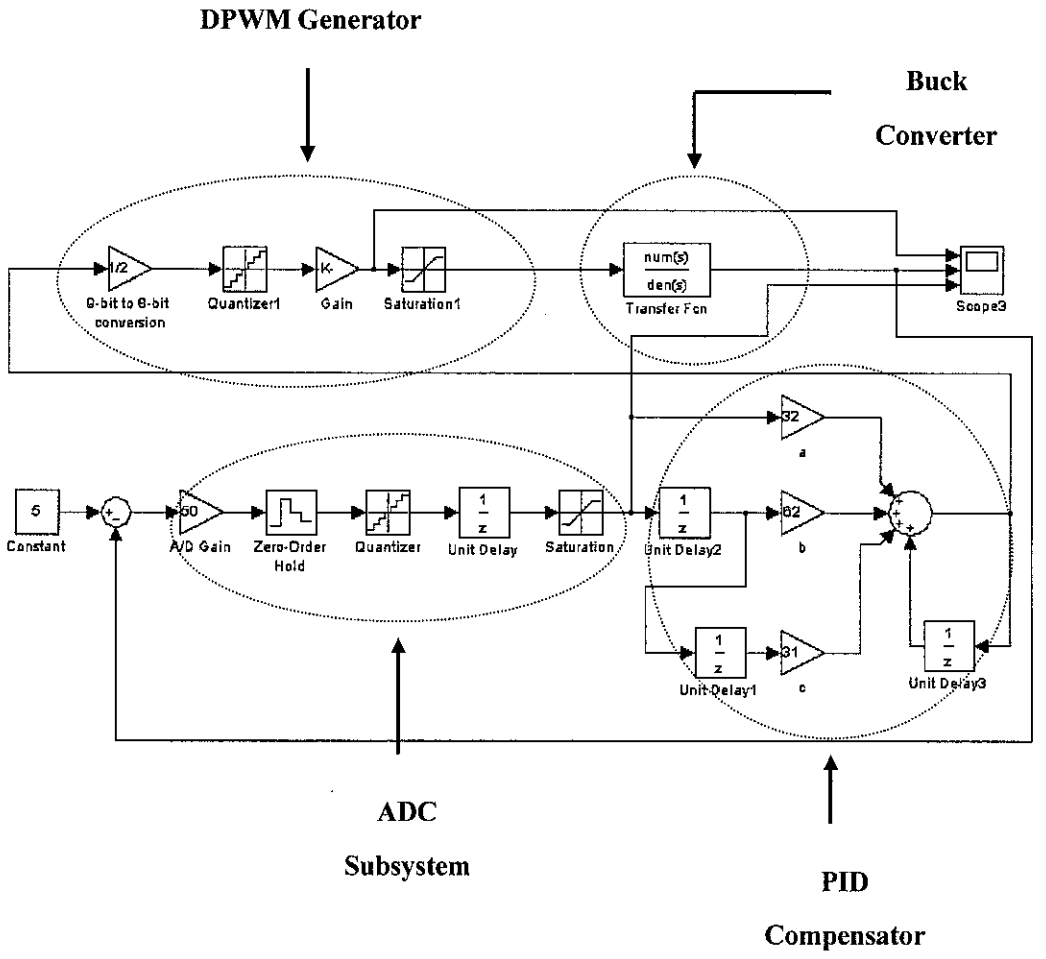


Figure 11 : The overall digital control of switching Buck converter system

3.5.1 Power Converter Subsystem

The exact electrical devices such as resistor, capacitor and inductor are not available in the MATLAB library. Thus, a transfer function is used as an approximation to represent the Buck converter circuit. The transfer function in Equation (18) is the discrete-time control-to-output transfer function which adapted from IEEE journal [12].

$$G_{vd}(z) = \frac{\left(\frac{T_s^2}{LC}\right)V_{in}}{z^2 - \left(2 - \frac{T_s}{RC}\right)z + \left(1 + \frac{T_s^2}{LC} - \frac{T_s}{RC}\right)} \tag{18}$$

Where:

$G_{vd}(z)$ = Control-to-output transfer function

R = Load Resistor

L = Inductor

C = Capacitor

T_s = Switching time

By substituting T_s = 1 μsec, R = 12 Ω , L = 1.39 mH and C = 1.31 μF into equation (18), the transfer function of Buck converter is:

$$G_{vd}(z) = \frac{0.659}{z^2 - 1.36387z + 1.02287} \tag{19}$$

As the Buck converter system is in continuous-time representation, Equation (19) is converted into continuous signal by using *d2c* (digital to continuous) command that available in MATLAB. The continuous-time control–to–output transfer function of Buck converter circuit is stated in Equation (20):

$$G_{vd}(s) = \frac{-3.651s + 69.04}{s^2 - 0.2264s + 69.04} \tag{20}$$

3.5.2 Stability Analysis of Buck Converter Transfer Function

The stability of the Buck converter transfer function is analyzed by using the SISO Design Tool that available in the MATLAB. As the PID compensator is in the discrete-time representation, the discrete-time control-to-output transfer function in equation (19) is used for the stability analysis.

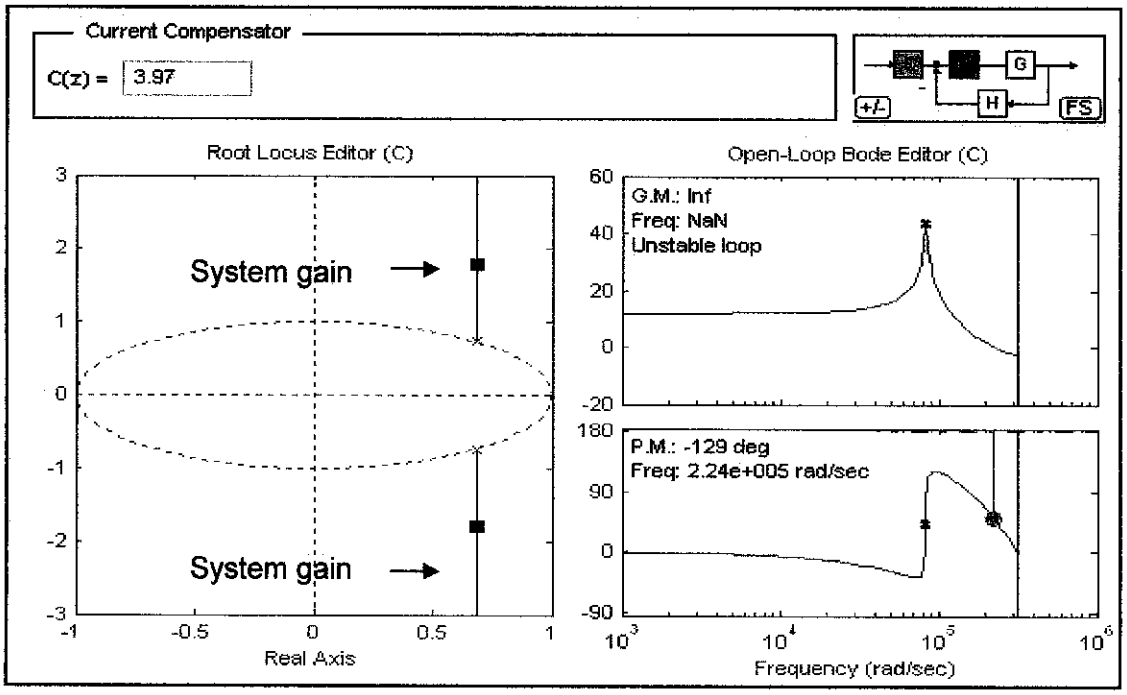


Figure 12 : Stability analysis for discrete-time control-to-output transfer function of Buck converter

The stability of Equation (19) can be analyzed from the graphs shown in Figure 12. By analyzing these three graphs, it is known that this system is unstable. In a stable digital control system, the gain of the system should be inside the unit circle (dotted circle). However, it can be seen from the root locus plot that the gain of the system (red square) is outside the unit circle. On the other hand, it clearly stated in the open-loop bode plot that the loop is unstable. As this unstable system cannot be used for the simulation purpose, it has been stabilized by adding one real zero to right hand plane of the root-locus plot (z = 0.1). Thus, the transfer function in equation (19) is changed to:

$$G_{vd}(z) = \frac{0.659(z-0.1)}{z^2 - 1.36387z + 1.02287} \qquad (21)$$

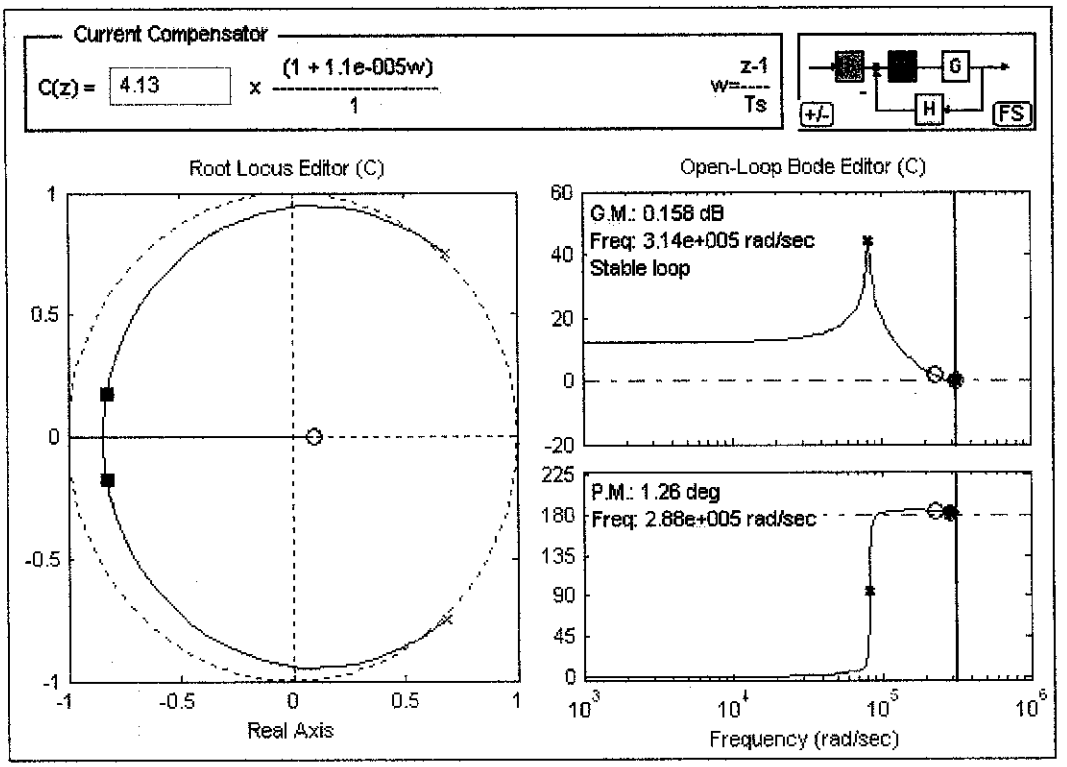


Figure 13 : System stabilization by adding real zero to the system

The stability of the stabilized transfer function (Equation (21)) is analyzed by using SISO Design Tool. From Figure 13, it is known that this system is stable because the gain of the system from root-locus plot is inside the unit circle. On the other hand, the open loop bode plot also stated that the system is stable. The range of gain ($C(z)$) for a stable system are determined by moving the red square along the blue circle of the root locus plot. Table 4 below shows the range of gain and its stability analysis observed when the red square is moved along the circle.

Table 4 : The range of gain used in the stability analysis

Gain ($C(z)$)	Stability analysis
0.31	Unstable system
0.32	Stable system
4.19	Stable system
4.20	Stable system
4.21	Stable system

As the value of gain ($C(z)$) choose in this project is 4.13, thus discrete-time transfer function of Buck converter become:

$$G_{vd}(z) = 4.13\frac{0.659(z-0.1)}{z^2 - 1.36387z + 1.02287} \tag{22}$$

The continuous-time representation of Equation (22) is determined using *d2c* command available in MATLAB and it is stated below:

$$G_{vd}(s) = \frac{4.045s + 62.14}{s^2 - 0.2261s + 69.04} \tag{23}$$

3.5.3 ADC Subsystem

The function of ADC subsystem is to convert the analog representation of error signal into the digital representation. The analog representation of error signal is obtained by comparing the output voltage from Buck converter circuit with the desired output voltage. In this project, the desired output voltage is 5 V. As shown in Figure 14, the error signal then will be amplified with ADC gain of 50. This error signal will be converted into digital representation after it passed through zero-order-hold block.

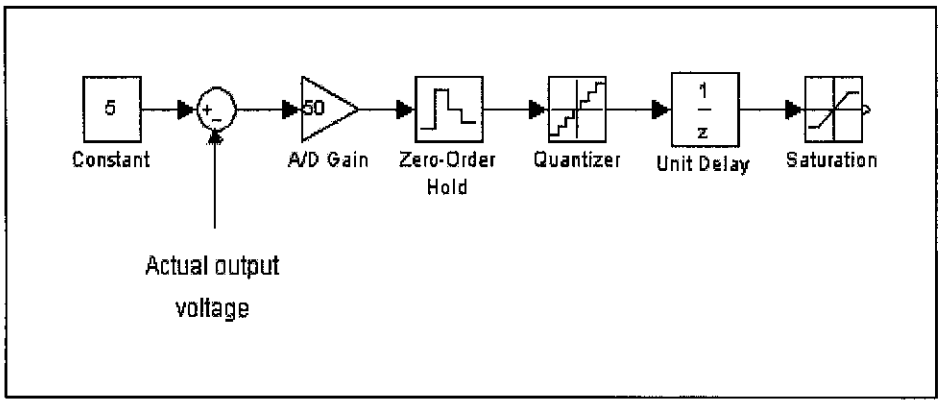


Figure 14 : The ADC subsystem

After that, the quantizer block will quantize the digital representation of error signal in 1.25μs as the clock frequency of the ADC circuit is 800 kHz. The saturation block will limit the upper and lower limit of quantization to 256 quantization levels. The

256 quantization levels is corresponds to 8 number of bits used for ADC circuit. In order to reduce the clock frequency from 2560 kHz to 800 kHz, only 9 possible quantization levels from -4 to 4 has been taken into account. Thus, the upper and lower limit of saturation block of Figure 14 is set up to 4 and -4 respectively. Then, the output signal generated in ADC subsystem is sent to PID compensator subsystem.

3.5.4 PID Compensator Subsystem

The duty cycle generated by PID compensator subsystem consists of current error signal ($e[n]$), error signal before the current value (e[n-i]) and its α,b,c coefficients. The error signal is obtained from ADC subsystem, while the α,b,c coefficients are found as 32, -62 and 31 respectively. These values have been inserted in the PID compensator subsystem (see Figure 15).

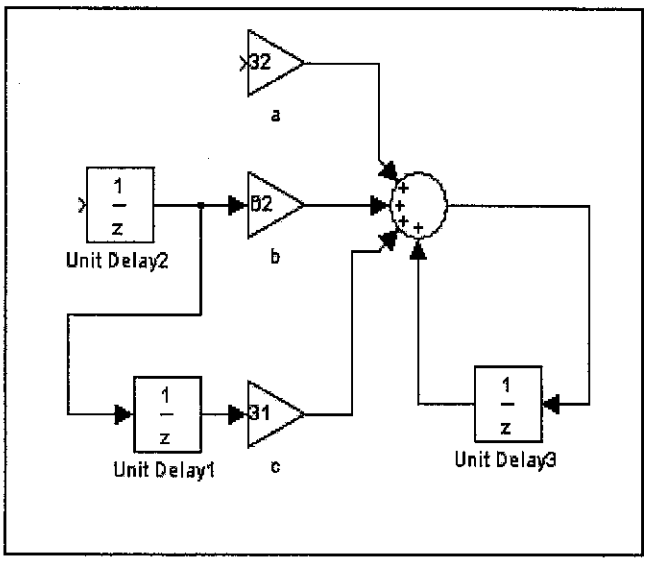


Figure 15 : PID compensator subsystem

3.5.5 The DPWM Subsystem

The DPWM subsystem which used to generate the DPWM signal is shown in Figure 16. It employs the same concept with the ADC subsystem except the upper limit of DPWM saturation block is set to 1 and the lower limit is to 0 instead of -4 to 4 for ADC subsystem. The actual quantization level of DPWM subsystem is 512 corresponds to 9 bits system. However, it quantization levels is limited from 0 to 1 as

this system is shifted from 8 bits (ADC subsystem) into 9 bits (DPWM subsystem).

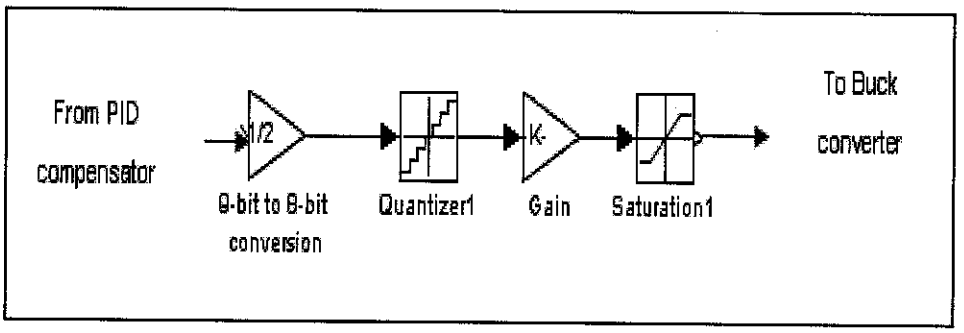


Figure 16 : The DPWM subsystem

Thus, the DPWM subsystem only sampled the signal in the range of 0 to 1 from PID compensator subsystem. The other signal that lies outside this range will be ignored from this system.

CHAPTER 4
RESULTS & DISCUSSIONS

4.1 The Buck Converter Parameters

The parameters of Buck circuit that obtained from the mathematical modelling stage of power converter are summarized in Table 5 below. These parameters are used as the settings for Buck converter circuit in the PSpice simulation.

Table 5 : The Buck converter parameters

Parameter	Value
Inductor, L	1.39 mH
Capacitor, C	1.31 μF
Resistor, R	12 Ω
Duty cycle, D	0.417
L_{CRIT}	53.9 μH

From the results stated in the Table 5, it is known that the Buck converter is operating in the CCM because its inductor value is greater that L_{CRIT}. Thus, it is expected that the inductor current does not reach zero axis during PSpice simulation as this Buck converter operates in CCM.

4.2 The Digital Controller Parameters

The parameters of digital controller part that obtained from the mathematical modelling stage of digital controller are summarized in Table 6 below. These parameters are used as the settings for the digital controller part in the MATLAB simulation.

Table 6 : The controller parameters

Parameter	Value
N_{ADC}	8 bits
N_{DPWM}	9 bits
K_{ADC}	50
K_{DPWM}	511
a	32
b	-62
c	31

4.3 PSpice Simulation Results

There are six waveforms that have been obtained in the PSpice simulation. These waveforms are used to determine the behavior of Buck converter circuit. In order to verify that the designed system has been meet the design requirements, the simulation results obtained in PSpice simulation are compared with its design requirements and calculated values. The acceptable limit for percentage difference between simulation results with the design requirements and calculation value is ±10 %. All the output waveforms presented in this section are captured during its steady state conditions.

4.3.1 The Switching Waveform

The location where the switching waveform is observed is as shown in Figure 17, which after the V_{pulse} component. The switching pulse is used to control the duty cycle and to turn on the switch (IRF044). In the design requirements, the duty cycle is 0.417, the switching frequency is 100 kHz, the switching time is 10μs and the gate voltage of the switch is set to 40 V. The switching waveform obtained from this particular point is shown in Figure 18.

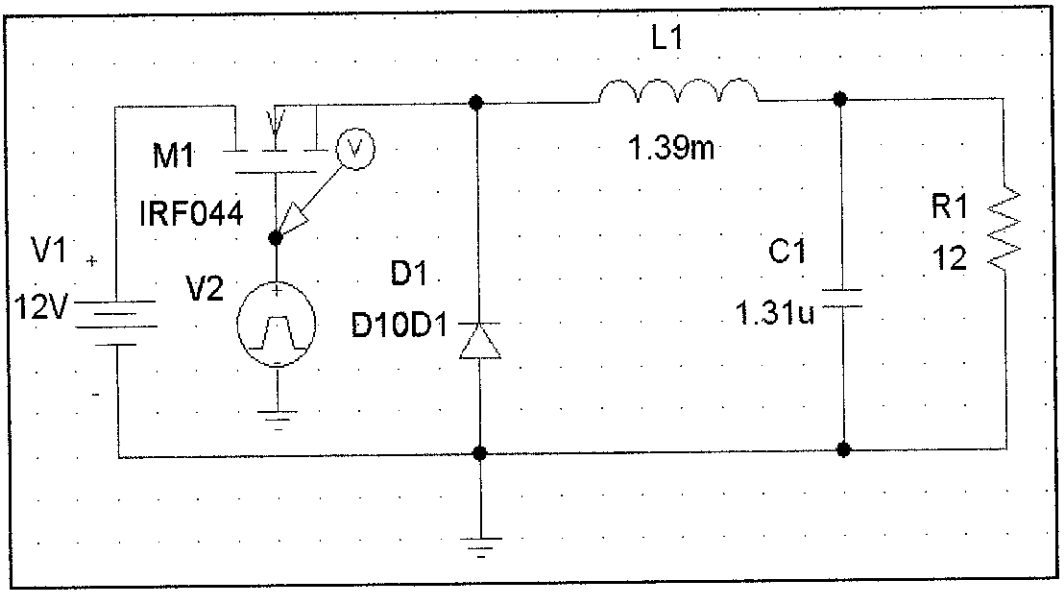


Figure 17 : The location of switching waveform observed

As shown in the Figure 18, the switching time is equal to 10μs and the switching frequency is equal to 100 kHz. The value of voltage that supplied to the switch is 40 V and it is adequate to turn on the MOSFET. All the values obtained in this graph satisfy the design requirements.

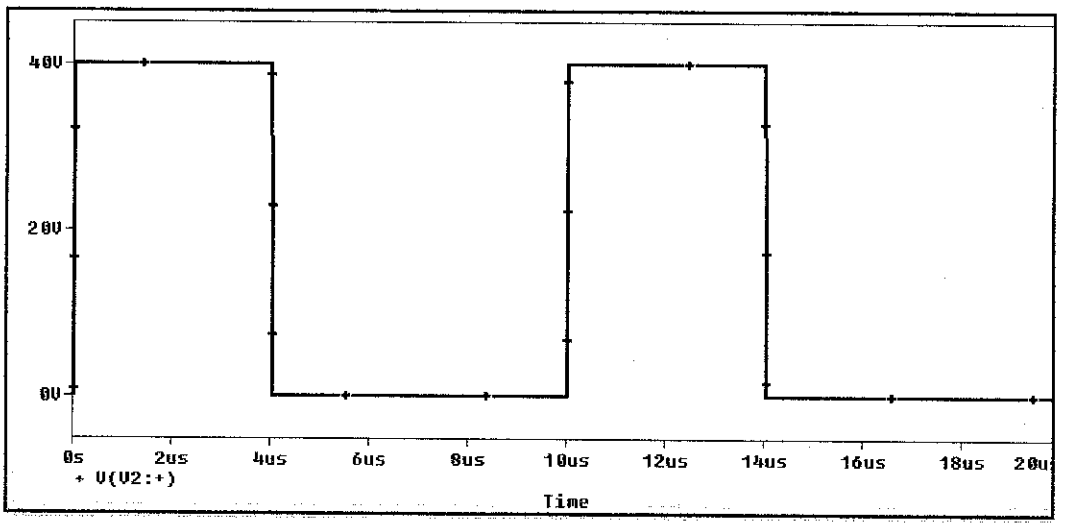


Figure 18 : The switching waveform

The Table 7 below gives the comparison between the simulation results with the design requirements for the switching waveform. The value of switching frequency and switching time obtained from PSpice simulation are accurately same with the design requirements. There is 4 % difference for the duty cycle value and this percentage difference is acceptable because it is in the allowable limit.

Table 7 : The comparison between design requirements and PSpice simulation for switching waveform

	PSpice Simulation	Design Requirements	% Differences
Switching frequency (*fs*)	100 kHz	100 kHz	0 %
Switching time (*ts*)	10 μs	10 μs	0 %
Duty cycle (*D*)	0.4	0.417	4 %

4.3.2 The Output Voltage Waveform

The location where output voltage is observed is as shown in Figure 19 which is in parallel with the load resistor. The output voltage waveform obtained from this particular point is shown in Figure 20.

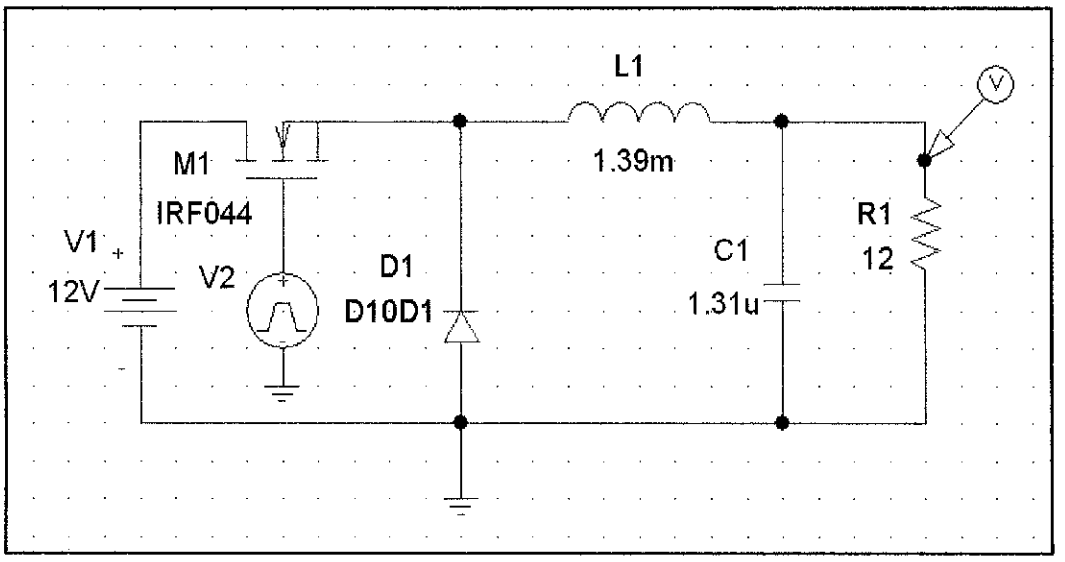


Figure 19 : The location of output voltage observed

The average output voltage waveform (see Figure 20) obtained from PSpice simulation is 4.6268 V and the output voltage ripple is 19.7 mV.

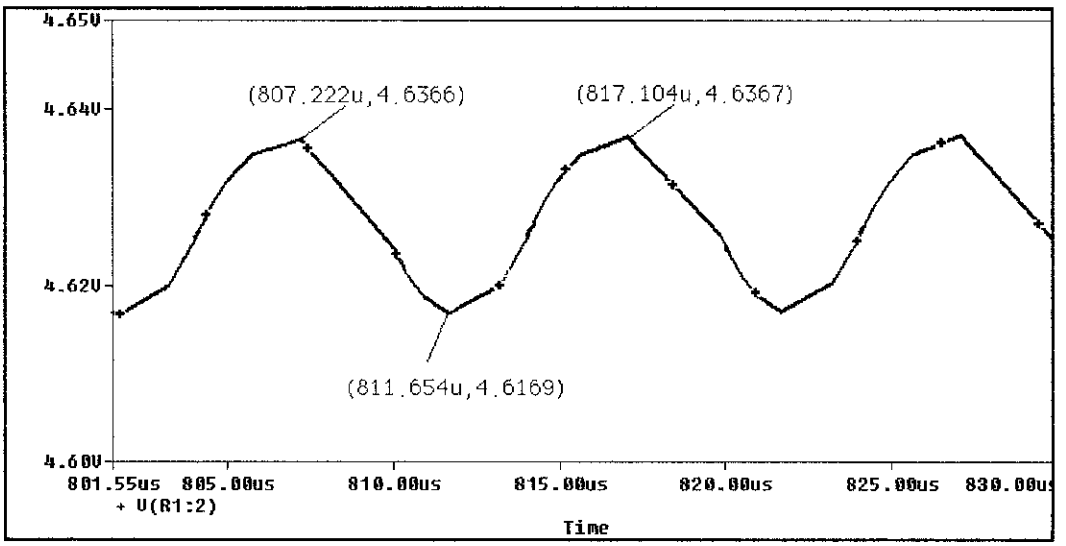


Figure 20 : The output voltage waveform

It also observed from Figure 20, that there are same variations for maximum and minimum output voltage value as the time increases. As example, during 807.222 μs, the maximum value of output voltage is 4.6366 V and during 817.104 μs, the maximum value of output voltage is increased to 4.6367 V. However, this value is acceptable as its variation is too small.

The comparison to show how accurate the simulation result with the design requirements for the output voltage is stated in Table 8. From the table, it is known that the output voltage waveform obtained in the PSpice simulation is 7.5 % less than the design requirement.

Table 8 : The comparison between the design requirements and PSpice simulation for output voltage

	Design Requirement	PSpice Simulation	% Differences
Output Voltage (V_{out})	5 V	4.6268 V	7.5 %
Output Voltage Ripple (ΔV_{out})	20 mV	19.7 mV	1.5%

4.3.3 The Output Current Waveform

The location where output current waveform is observed is as shown in the Figure 21 which is in series with the load resistor. The output current waveform that obtained from this particular point is shown in Figure 22.

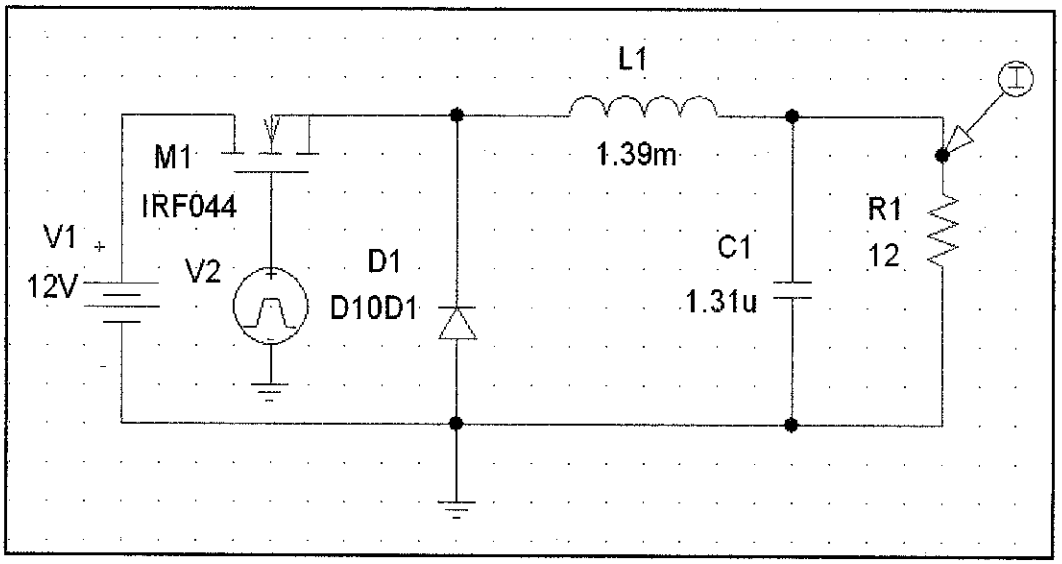


Figure 21 : The location of output current observed

The average output current (see Figure 22) obtained from PSpice simulation is 385.58 mA and the current ripple value is 1.665 mA.

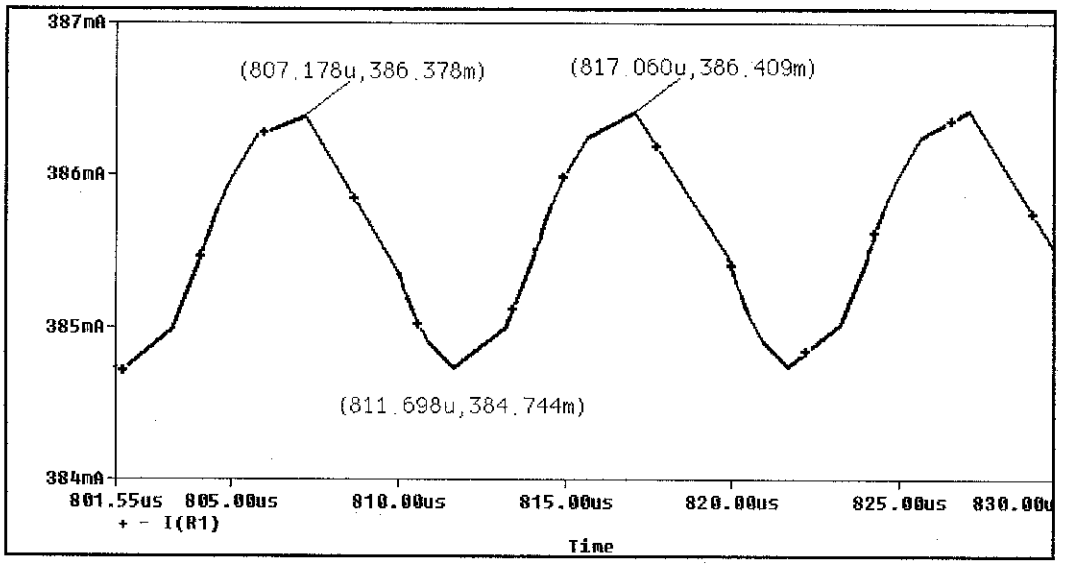


Figure 22 : The output current waveform

It also observed from Figure 22, that there are small variations of maximum and minimum output current value as the time increases. As example, during 807.178 μs, the output current value is 386. 378 mA and during 817.060 μs, the output current value increases to 386.409 mA. However, as this variation is too small which is about ±0.08 %, this simulation results is acceptable.

Table 9 below gives the comparison between the simulation result with the design requirements for output current waveform. The output current obtained from simulation is 7.5 % less than design requirements and the current ripple value is 21 % less than design requirements. The percentages difference for output ripple current is higher than allowable limit (±10 %) is expected due to high percentages differences of output voltage (7.5 %).

Table 9 : The comparison between design requirements and PSpice simulation for output current

	Design Requirement	PSpice Simulation	% Differences
Output Current (I_{out})	416.667 mA	385.58 mA	7.5 %
Output Current Ripple (ΔI_{out})	2.1 mA	1.665 mA	21 %

4.3.4 The Capacitor and Inductor Current

The location where capacitor current and inductor current are observed is as shown in the Figure 23 which is in series with the capacitor and inductor respectively. The output current waveform for capacitor and inductor that obtained in this particular simulation is shown together in Figure 24.

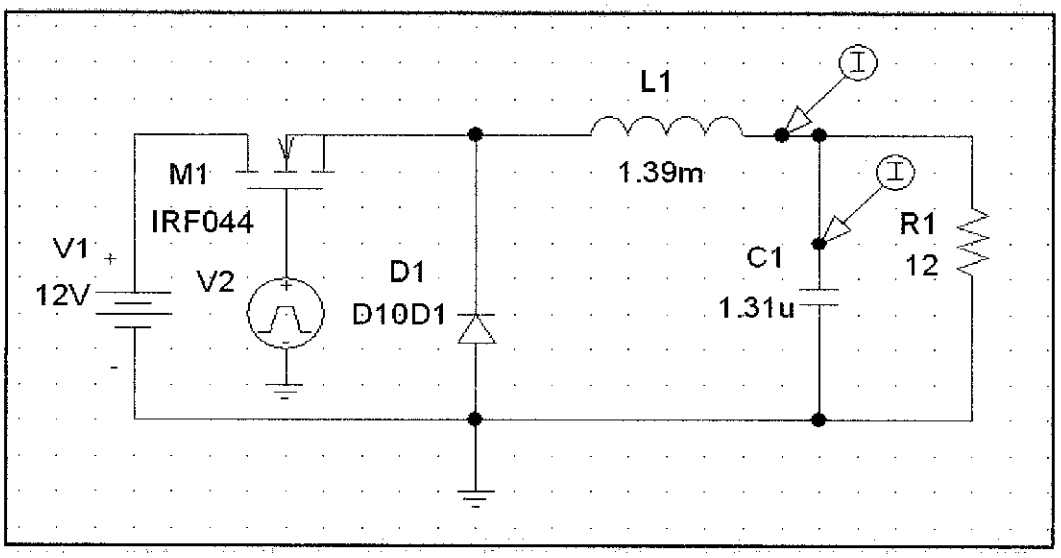


Figure 23 : The location of capacitor and inductor current observed

The minimum value of inductor current shown in the graph (see the second graph in Figure 24) is 375.046 mA. As this value is higher than zero ampere (0 A), it is verified the behavior of Buck converter operates in CCM.

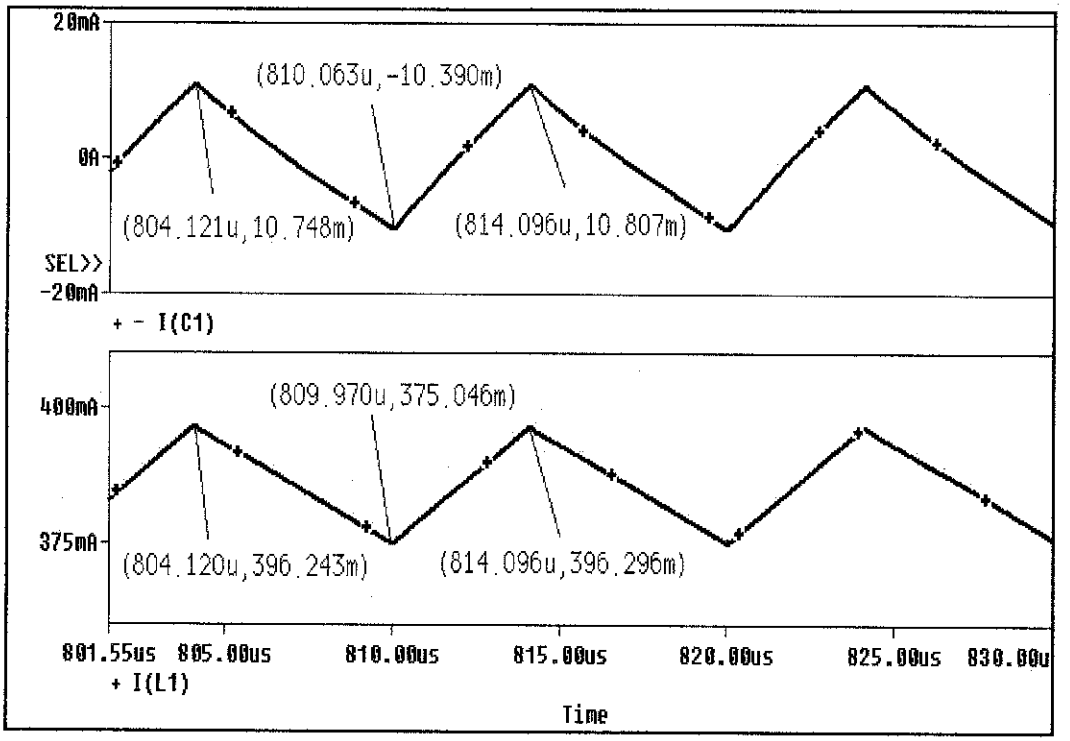


Figure 24 : The capacitor and inductor current

There is small negative value of minimum capacitor current observed (I_{cmin} = -10.390 mA) observed from Figure 24. This negative capacitor current will compensate the behavior of inductor current that does not reach zero axis during its commutation angles.

Table 10 provides comparison between the calculated values of inductor current with the simulation value. The minimum value of inductor current (I_{LMIN}) is 7.7 % less than its calculated value. Whereas, the maximum value of inductor current (I_{LMAX}) is 7.3% percentages less than the calculated value.

Table 10 : Comparison between calculated value and PSpice simulation for inductor current

	Calculation	Simulation	% Difference
I_{LMIN}	406.506 mA	375.046 mA	7.7 %
I_{LMAX}	427.494 mA	396.243 mA	7.3 %

4.3.5 Diode Reverse Recovery Region

The location where diode reverse recovery region is observed is as shown in Figure 25 where is in series connection with free-wheeling diode. The output current waveform for diode reverse recovery region observed from that particular point is shown in Figure 26.

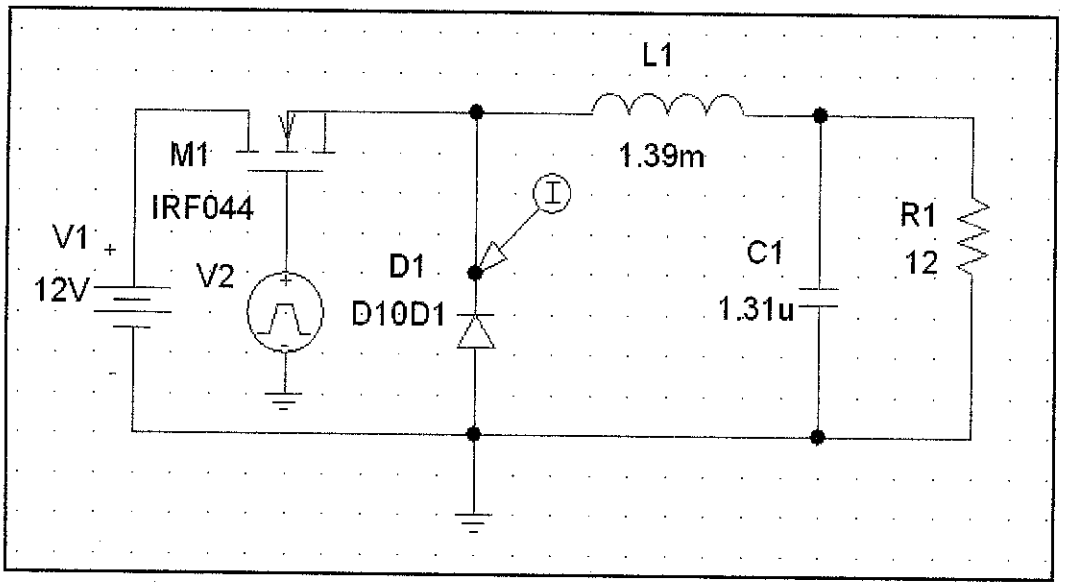


Figure 25 : The location of diode reverse recovery region observed

From Figure 21, it is known that the diode reverse recovery condition is occurred in very short and fast duration which is in 8 ns. The diode reverse recovery region is the nature phenomenon of the diode which occurred in the reverse bias condition. The short duration of reverse recovery region shows the free-wheeling diode (D10D1) is suitable for high switching frequency system of this project.

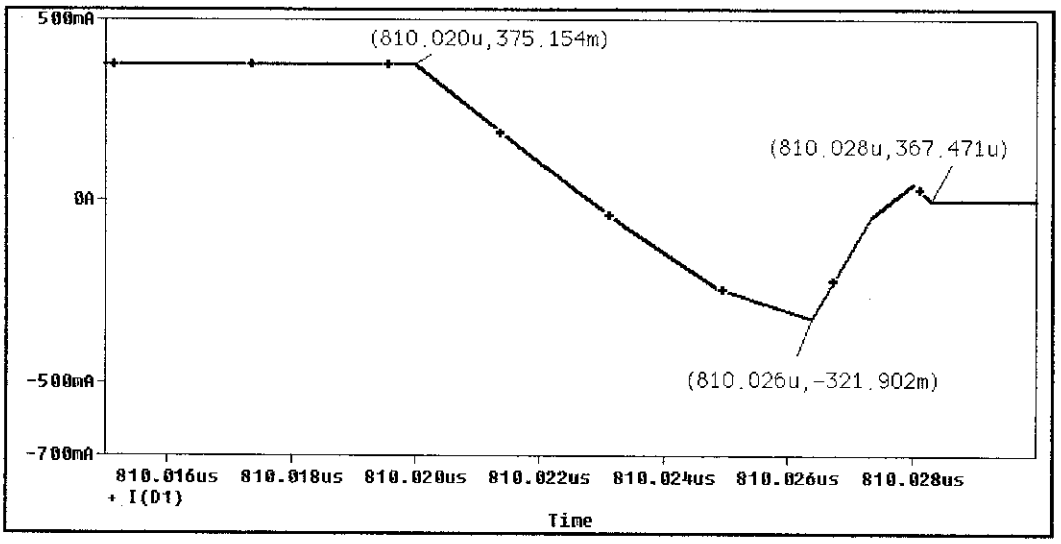


Figure 26 : The diode reverse recovery region

4.4 MATLAB/Simulink Simulation Results

There are three types of output waveforms that should be obtained from the MATLAB simulation. Those waveforms are output voltage waveform, DPWM waveform and ADC waveform. The location where those three waveforms are observed is shown in Figure 27 below.

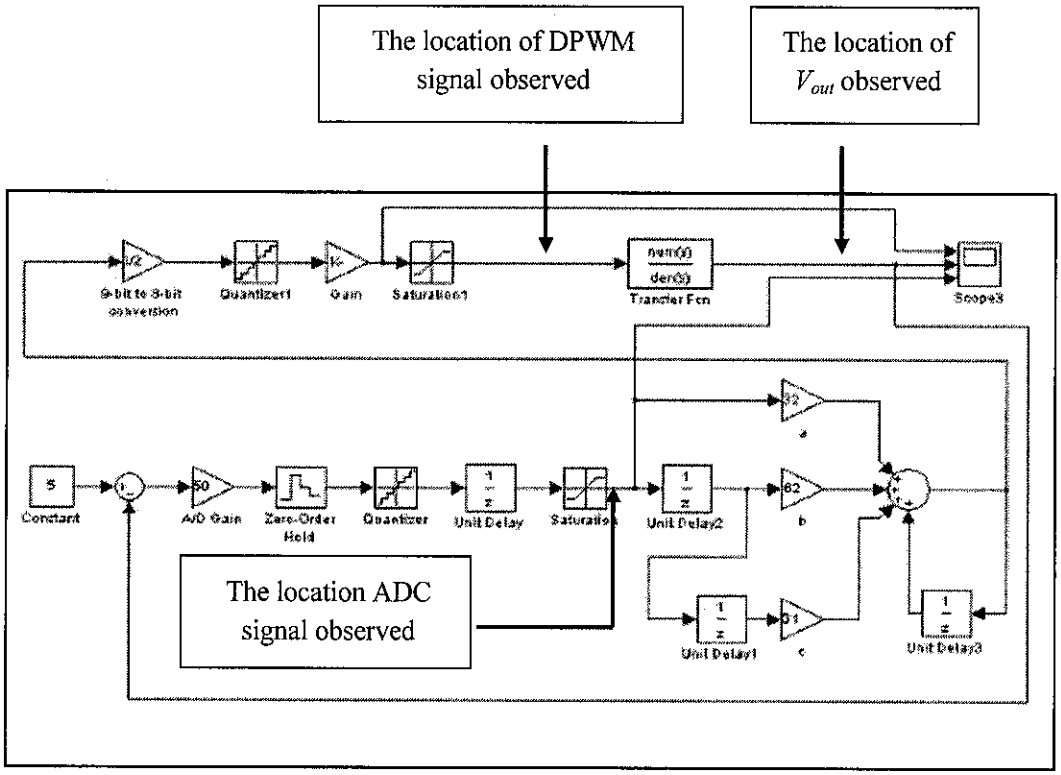


Figure 27 : The location of V_{out}, DPWM signal and ADC signal are observed

4.4.1 *Analysis of MATLAB/Simulink Simulation Results*

The analysis of the ADC, DPWM and V_{ou} cannot be performed in the MATLAB simulation because the simulation process is terminated due to infinite gain of the system. The simulation diagnostic window during the simulation process is terminated is as shown in Figure 28 below. This problem is expected comes from the wrong setting of PID compensator coefficients.

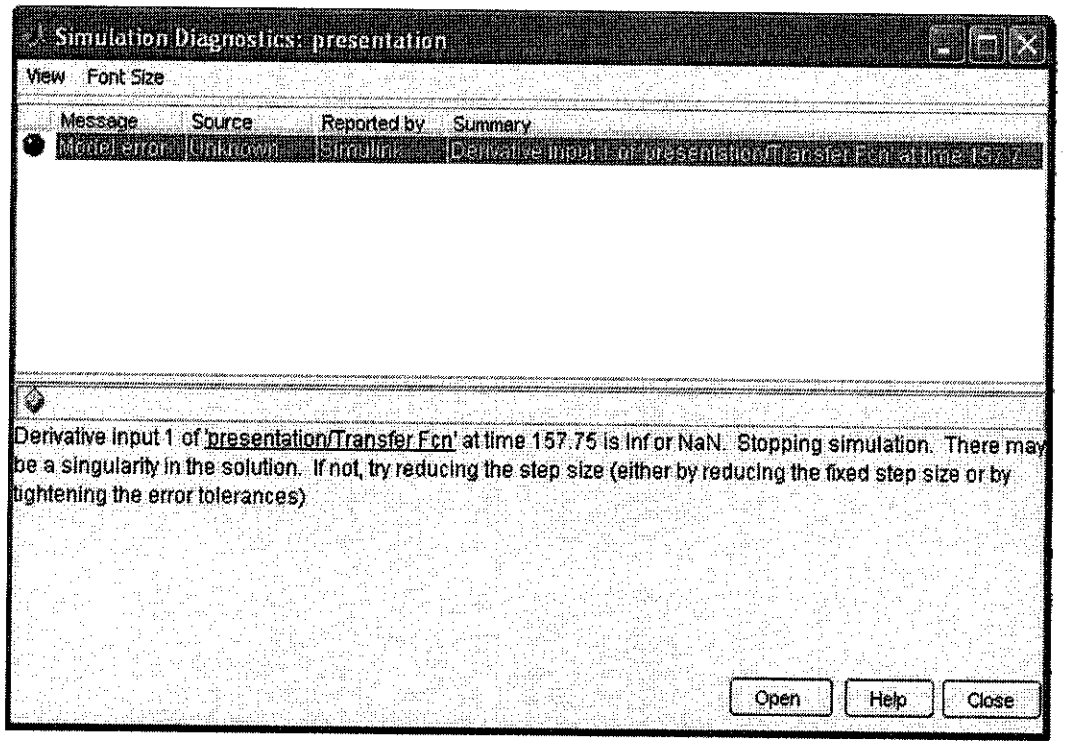


Figure 28 : The simulation diagnostic window

Thus, to solve the problem shown in the simulation diagnostic window, the fixed step size of the system is iteratively changed from 0.02 to 0.2 After changing the step size, the system is simulated once again and it is found that another problem has been appeared on the simulation diagnostic window (see Figure 30).

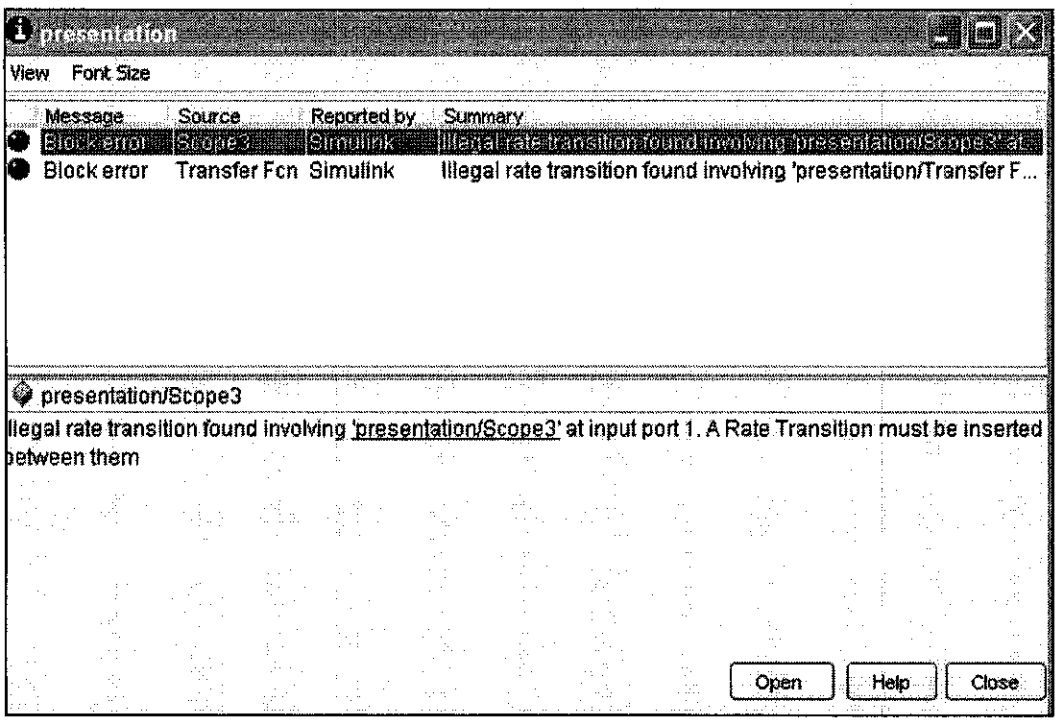


Figure 29 : The simulation diagnostic when fixed size is reduced to 0.2

In order to solve the problem shown simulation diagnostic window of Figure 29, the rate transition (see Figure 30) is inserted into the DPWM subsystem.

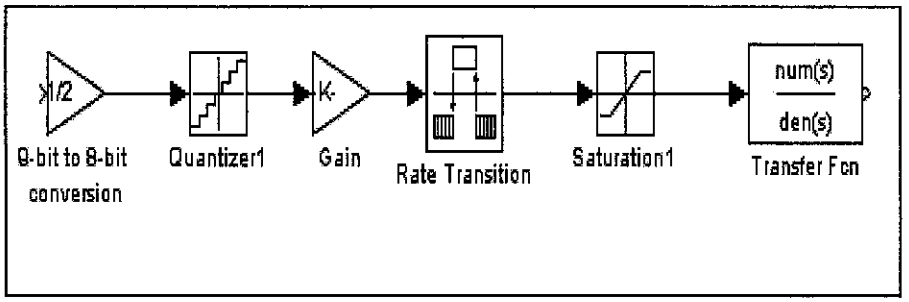


Figure 30 : Modify DPWM subsystem by inserting the rate transition block

As after modifying all these errors, the simulation process still does not complete, the simulation process does not proceed furthermore. This is because there are so many unknown errors that need to troubleshoot. It is expected that the simulation process is terminated not only because of the wrong setting of MATLAB parameters, but also because of the wrong settings of PID compensator coefficients (α,b,c).

In order to verify that this designed system can work on if the correct setting of PID

compensator coefficient used, it is simulated once again using the parameters found in the IEEE journal [12]. This simulation process has been successful complete without any termination or errors. The simulation results obtained in that simulation (see Figure 33) is same with the expected output waveforms in this project.

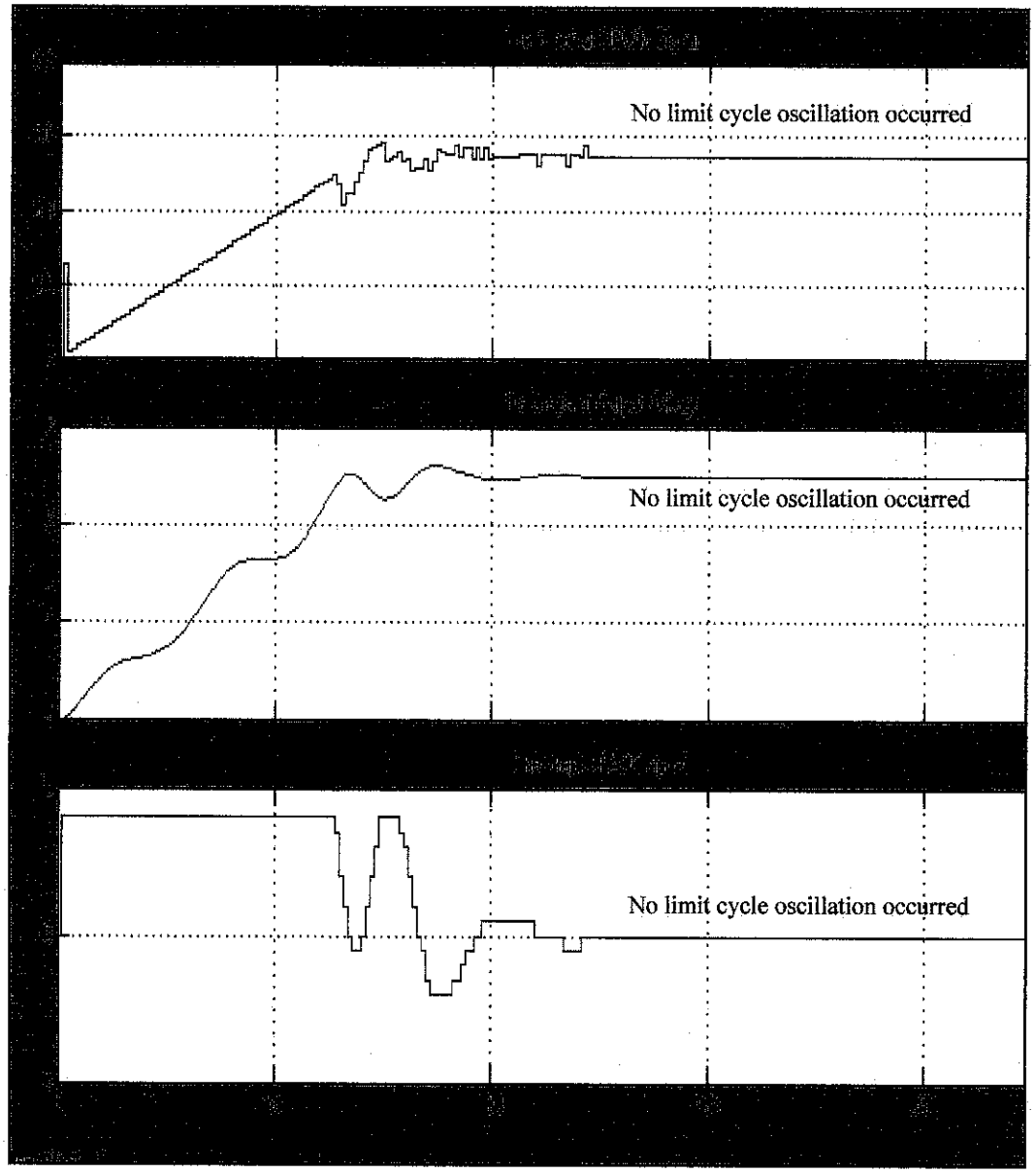


Figure 31 : The output waveform of DPWM , V_{out} and ADC signal

The analysis for DPWM, V_{out} and ADC output waveforms obtained by simulating the designed system in Figure 27 with the parameters found in IEEE journal are explained below:

- The DPWM waveform

The graph for DPWM waveform is available from 0 to 1 scales of the y-axis. This condition meets the quantization level for DPWM signal that set earlier which is between 0 to 1.The DPWM signal reaches its steady state condition in 120 μs.

- The output voltage waveform

  The value of output voltage obtained in this simulation is about 2.7 V and it meets the design requirements stated in the journal. As can be seen from the graph, several oscillations have been occurred to the output voltage before it reaches its steady state condition. After it reaches its steady state condition in 120 μs, there is no more oscillation found in the output voltage graph. During its steady state condition, the output voltage is regulated to 2.7 V.

  The same condition of output voltage should be obtained when simulating the overall system with the parameters set-up in the Table 4 and 5 of this report. The only difference is in this project, the output voltage should be regulated at 5 V.

- The ADC signal

  The ADC waveform is available between -4 to 4 of its y-axis. This value corresponds to the 9 possible quantization level of ADC signal which is between -4 to 4. Before it reaches its steady state condition, the ADC signal oscillates between -4 to 4 of the y-axis. When it reaches its steady state conditions in 120 μs of settling time, the ADC signal lies on 0 axis. This condition shows that there are no more differences between the actual output voltages from the Buck converter subsystem with the desired output voltage (reference signal).

CHAPTER 5
CONCLUSION & RECOMMENDATION

5.1 Conclusion

This project describes the digital controller design for low power DC-DC Buck converter. The digital controller scheme is designed using the DPWM technique. The DPWM signal is used to vary the ON and OFF condition of the power MOSFET switch and to control the Buck converter operation. The project work comprises two different types of simulation which are in the PSpice simulation and in the MATLAB simulation.

The purpose of doing the PSpice simulation is to verify whether the calculated parameters such as output resistor, output capacitor and output inductor can give the correct output waveform of Buck converter or not. All the waveforms obtained in the PSpice simulation have been verified the theoretical concept of Buck converter and it meets the design requirements. However, it is found that there are several differences occurred when comparing these output waveforms with the calculation. All these differences lie within the acceptable range of percentage differences (±10), except for the output current ripple. This problem is expected comes from the types of the MOSFET and free-wheeling diode used.

The overall digital control of switching power converter system that consists of Buck converter circuit and its digital controller part is designed in the MATLAB/Simulink. The results for the MATLAB simulation is not obtain because of the wrong setting of PID compensator coefficients. In order to verify that the designed system can work on if the correct setting of PID compensator is used, the MATLAB/Simulink has been done once again with the parameters found in the IEEE journal. The result for that simulation has been presented in *Section 4.3.1* of this report.

5.2 Recommendation

In the future work, there are four (4) improvements should be done to the system that has been designed in this project. The first recommendation is to decrease the large differences of simulation results as compared to its design requirements and calculated value. These differences need to be troubleshooting by changing the types of MOSFET (IRF044) and free-wheeling (D10D1) used in this project with the other type. The difference between simulation and calculated value of output voltage is not further investigated in this project because the main objective of this project is to design the digital control of switching power converter in the MATLAB/Simulink software.

The second recommendation is to reconfigure the PID compensator coefficients because it is expected that the wrong setting of PID compensator coefficients has been led to the termination of the simulation process. The third recommendation is to perform the experimental work and transfer the results obtained on the printed circuit board (PCB). It will add some more values to this project because the designed prototypes on the PCB can be used in the electronics industry. The fourth recommendation is to increase the switching frequency of the system to 1 MHz or higher value as the existing switching frequency is 100 kHz (0.1 MHz). Higher frequency will create fast response system.

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